Genesys Logic, Inc.

GL9711

PCI Express™ PIPE x1 PHY

Product Overview

Copyright

Ownership and Title

Genesys Logic, Inc. owns and retains of its right, title and interest in and to all materials provided herein. Genesys Logic, Inc. reserves all rights, including, but not limited to, all patent rights, trademarks, copyrights and any other propriety rights. No license is granted hereunder.

Disclaimer

All Materials are provided “as is”. Genesys Logic, Inc. makes no warranties, express, implied or otherwise, regarding their accuracy, merchantability, fitness for any particular purpose, and non-infringement of intellectual property. In no event shall Genesys Logic, Inc. be liable for any damages, including, without limitation, any direct, indirect, consequential, or incidental damages. The materials may contain errors or omissions. Genesys Logic, Inc. may make changes to the materials or to the products described herein at anytime without notice.

Genesys Logic, Inc.
12F., No. 205, Sec. 3, Beixin Rd., Xindian Dist. 231,
New Taipei City, Taiwan
Tel : (886-2) 8913-1888
Fax : (886-2) 6629-6168
http://www.genesyslogic.com

GENERAL DESCRIPTION

The GL9711 is a 1-lane PCI Express PHY Layer Controller, which is compliant with PCI Express Base Specification rev. 1.0a and Intel's PHY Interface for the PCI Express Architecture rev. 1.0. It integrates one SerDes and the Physical Coding Sublayer (PCS) which performs 8b/10b encoding and decoding, elastic buffer and receiver detection, data serialization and deserialization. The SerDes in the GL9711 supports an effective serial interface speed (2.5 Gb/s) of data bandwidth, intended for use in ultrahigh-speed bi-directional data transmission system. The GL9711 can also be externally configured for various parallel bus width which is flexible and suitable for implementation. It also supports four operational states for power management to minimize power consumption. For production and self-test purposes, the GL9711 provides BIST and an internal loopback capability.

The primary application of this chip is to provide very high-speed I/O data channels for point-to-point baseband data transmission over an on-chip termination resister of 50 Ohm +/- 10%.

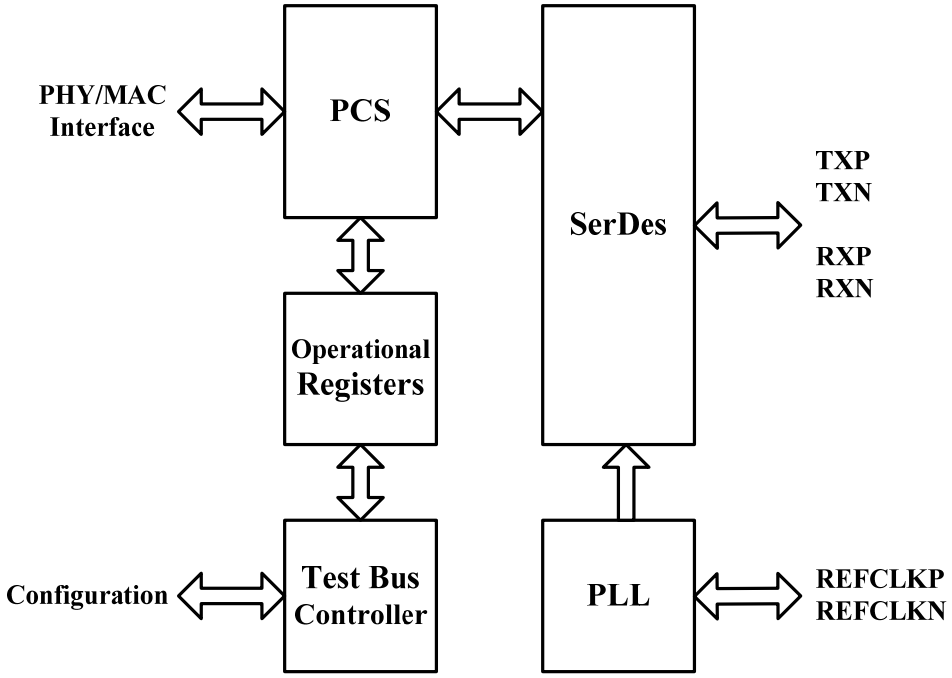
This device can also be used to replace parallel data transmission architectures by providing a reduction in the number of traces, connector pins, and transmit/receive pins. Parallel data loaded into the transmitter is delivered to the receiver over a serial channel. It is then reconstructed into its original parallel format. The maximum data transfer rate in each direction is 256M bytes per second. It also offers various power saving modes to significantly reduce power consumption as well as scalability for a higher data rate in the future.

FEATURES

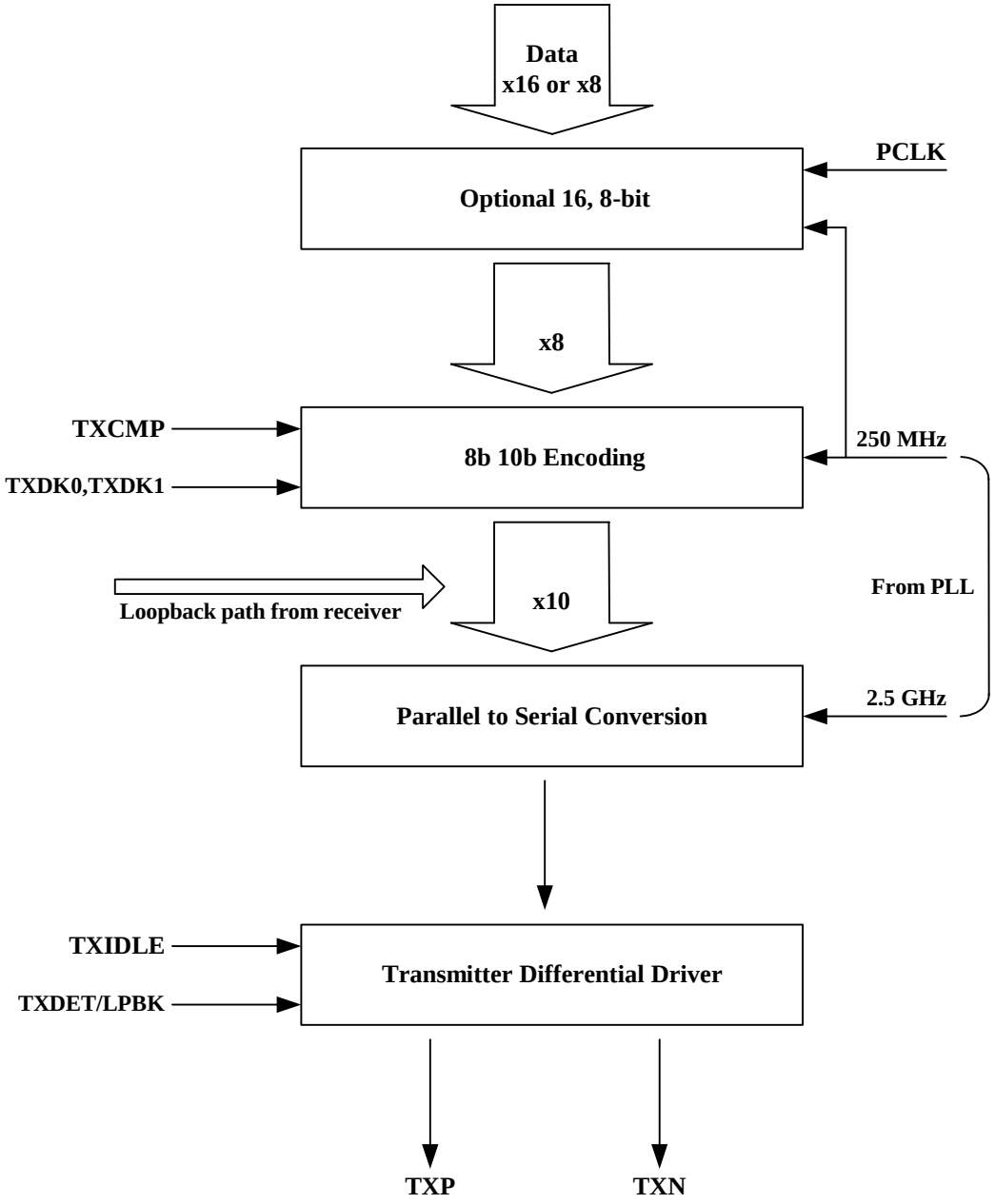
- Complies with PCI Express Base Specification rev. 1.1
- Complies with Intel's PHY Interface for PCI Express Architecture rev. 1.0
- Integrates 2.5 gigabit per second (Gpbs) Serializer/Deserializer
- Supports 8-bit @250MHz
- Supports 16-bit parallel interface @125MHz
- Support 16-bit source synchronous mode (2-Clock mode) @ 125MHz
- Supports DDR configuration for 8-bit mode
- Beacon transmission and reception
- Receiver detection
- Transmission and detection of electrical idle
- Clock tolerance for 600 ppm in frequencies between bit rates at the two end of a Link
- On-chip 8-bit/10-bit encoding/decoding and comma alignment
- On-chip PLL provides clock synthesis
- 1.8-V power supply for core
- 2.5-V power supply for IO
- Above 2.0 kV ESD protection
- 0.18 μm process
- Available in LFBGA 233 package and LQFP 128 package

BLOCK DIAGRAM

Simplified Diagram



Transmitter Data Path Per Lane



Receiver Data Path Per Lane