i-Chips

IMAGE PROCESSORS

IP00C753

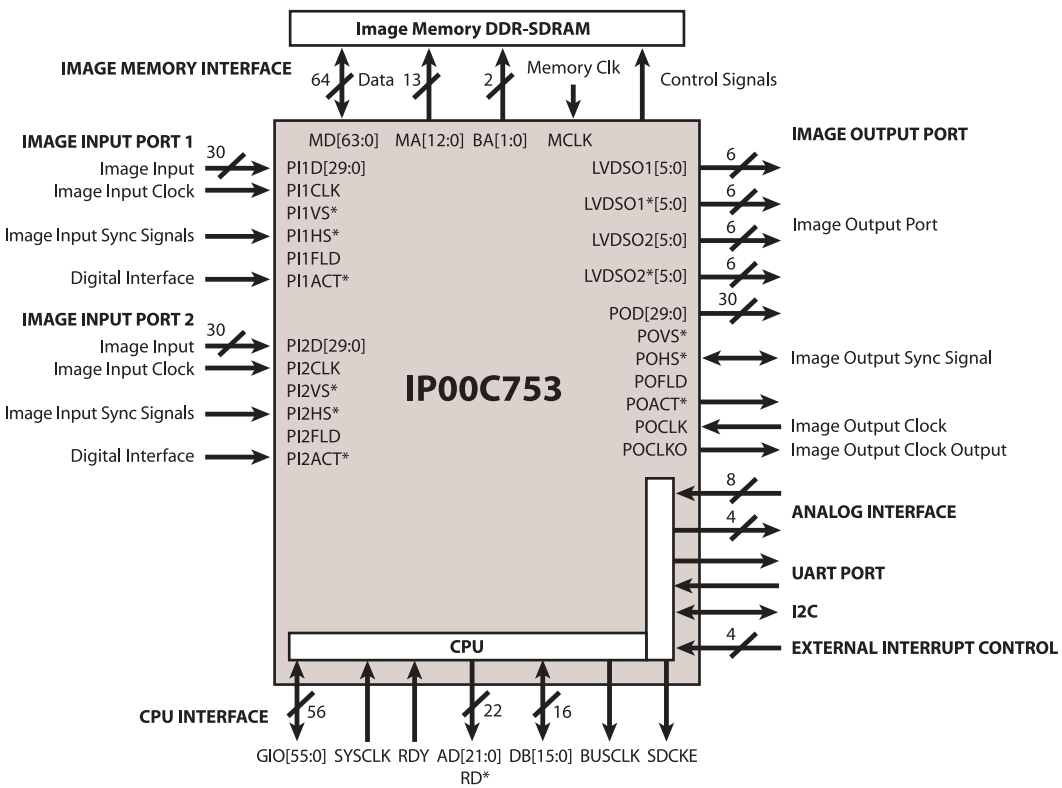
xvYCC Dual De-interlacer/Scaler with PiP

Summary

The IP00C753 is a complete PiP/PoP solution with 2 independent scalers and de-interlacers, an embedded CPU and an LVDS transmitter. It can handle 2 input video streams simultaneously, up to UXGA resolution in both interlace or progressive-scan formats. It can drive a high-resolution output display such as 1080p and Wide-UXGA. De-interlacing is performed by motion-adaptive filters on each input image to eliminate artifacts when handling interlaced video formats, in order to produce a high-quality output image. The IP00C753 also features MPEG noise reduction and combing processing capability for caption for smoother de-interlacing. It also supports the xvYCC extended color gamut.

Applications

- Digital Displays
- Video Processors/ Switchers
- Video Walls
- Video Projectors



IP00C753 Specifications

INPUT (2 PORTS)

RGB or YUV4:4:4 30 bits @ 162 MHz
YUV4:2:2 24 bits @ 162 MHz
YUV4:2:2 10 bits @ 162 MHz (BT656 input)

OUTPUT

RGB or YUV4:4:4 30 bits @ 162 MHz
FPD Link output, LVCMOS compatible

IMAGE SIZE

Channel 1: Up to 4096 pixels/line with 2048 active pixels max.*
Channel 2: Up to 4096 pixels/line with 1600 active pixels max.*
* Note: These limits are before the zoom, or after the shrink

DE-INTERLACING

3D motion-adaptive filter
Noise reduction filter
Diagonal line interpolation
3:2 and 2:2 pull down sequence detection
Combing filter for processing caption
MPEG noise reduction filter

IMAGE SCALING

Adaptive interpolation with FIR filter
Full 10-bit internal processing
Independent H and V scaling ratios
Non-linear H and V scaling (aspect ratio correction)
Dynamic scaling
Vertical keystone correction
90 image rotation – independent on each channel

PiP & PoP FUNCTIONS

Two (2) fully independent programmable video channels
Frame rate conversion with frame tear protection
α blending

SYNCHRONIZATION

Independent clock, HS, VS for each input image port, and for the output port
Progressive to interlace conversion supported

BITMAP OSD

256 colors
Support for user-specific fonts
Support for blinking and semi-transparent OSD

IMAGE QUALITY CONTROL

Horizontal and vertical edge enhancement circuits
Brightness & luminance in RGB or YUV, contrast adjustment
12-bit color Gamma correction tables (7 or 31 LUT's available)
Dithering for 12→10, 10→8 and 8→6
Color management function

EXTERNAL MEMORY

DDR-SDRAM 128Mbit x 32, 400 MHz with 64-bit memory bus

CPU INTERFACE

8-bit parallel or 4-bit serial
Interface to external Flash/SRAM/SDRAM memory
Address/Data bus width: 22 bits/16 bits
External interrupt line: 4 bits

EMBEDDED CPU

ARM946E-S core, with cache of 16KB instruction, 8KB data
Embedded work RAM of 64 KB
DMAC (2 ch) / UART (4 ch) / I2C (4 ch)
10-bit ADC (8 ch. muxed) / 8-bit DAC (4 ch)
Timer (4 ch) / Clock control / Interrupt control
CPU core operating speed: 150 MHz

POWER SUPPLY

3 power supplies: 3.3V, 2.5V and 1.2V

PACKAGE

900-pin plastic BGA; 31 mm x 31 mm (1mm pitch)

For more information please visit:
www.i-chips.com or **info@i-chips.com**

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IMAGE PROCESSORS

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