i-Chips
IMAGE PROCESSORS

IP00C812A

Dual Input/Output De-interlacer/Scaler

PRODUCT BRIEF

Product Description

The IP00C812A is a dual-input/dual-output de-interlacer and scaler on a single device. It features a built-in video decoder, ARM9 CPU, LVDS output, along with Ethernet and USB interfaces. Its inputs and outputs can be any interlaced format, SD or HD, or any progressive format, up to 1080P/WUXGA/2K1K.

The IP00C812A features 2 independent de-interlacer/scaler blocks, with full 10-bit internal processing. The IP00C812A can be configured in several ways. In the single-output mode, it can generate Picture-in-Picture, Picture-by-Picture output. In the dual-output mode, it can generate separate outputs at any resolution, or it can serve to drive directly a 3-D display, using its quad-LVDS output port.

The IP00C812A has a state-of-the art image processing algorithms, such as mirror image, 90-degree rotation, keystone correction and color uniformity control. It is energy-efficient, with its separate power blocks for CPU and image processing, thus greatly reducing stand-by power consumption.

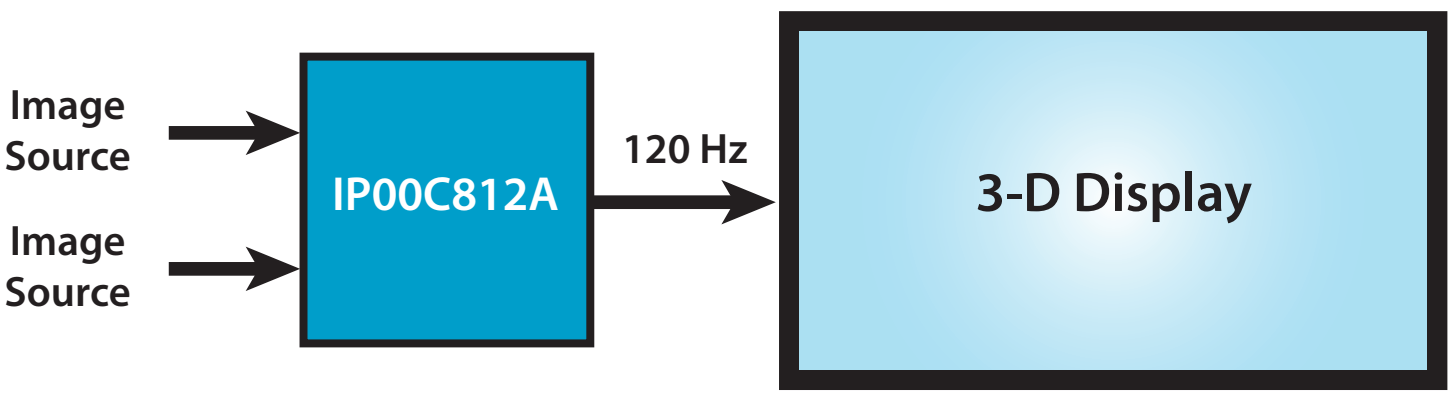
The IP00C812A is an ideal solution to drive a 3-D display, with no other components required, other than the front-end image signal receiver. The IP00C812A is a cost-effective way to eliminate FPGA resources by handling the common image processing tasks of 2 video channels on the board. The advantages of the IP00C812A are reduced board space, ease of programming, and cost.

Applications

Typical applications for the IP00C812A are:

- **3-D Display:** Convert the input from 2 input video channels to drive seamlessly a 3-D panel display.
- **4K2K/2560x1600 Display:** Convert any input image seamlessly to a high-resolution output, without the need for external glue logic.

Actual Size



IP00C812A FEATURES

INPUT
- 30-bit RGB/30-bit YUV 4:4:4/20-bit YUV 4:2:2/10-bit YUV 422 @ 166 MHz
- 60-bit RGB / 60-bit YUV 4:4:4/ 40-bit YUV 4:2:2 @ 83 MHz (Parallel)
- Analog: CVBS/S-Video
- 2176 pixels of active video

OUTPUT
- 30-bit RGB/30-bit YUV 4:4:4/20-bit YUV 4:2:2 @ 166 MHz
- Compatible with FPD link (2x2 only@135 MHz/each, no CMOS)
- 2176 pixels of active video

DE-INTERLACING
- Motion adaptive de-interlacer
- Diagonal line interpolation
- 3D/MPEG/mosquito/block noise reduction
- 2:2, 2:3 and multi cadence detection
- Chroma bug canceller

SCALING
- 6 symbol filter (horizontal only – 8 symbol) with FIR Filter
- Independent H and V scaling ratios (aspect ratio correction)
- Coefficient filter ROM embedded (64 set)
- 90 degree image rotation (image and OSD)
- Vertical keystone correction
- Edge-blending

VIDEO DECODER
- NTSC-M, JPN, 4.43 PAL-B, D, G, H, I, CombinationN, 60, & SECAM
- VBI (Closed caption/CGMS/WSS) data extraction
- Clamp Pulse Output
- Dot interference, cross color removal

PiP & PoP FUNCTIONS
- Two (2) fully independent video inputs
- Frame rate conversion with frame tear protection

BITMAP OSD
- 256 colors/High color OSD (RGB 565) compatible
- Embedded font engine (65536 words)
- Support for blinking and semi-transparent (4 color) OSD

EMBEDDED CPU
- ARM926EJ-S core with 16 KB instruction, 8 KB data
- Work RAM (64KB)
- Ethernet, USB 2.0 (host, function)
- DMAC (2ch)/UART (4ch)/I2C (master/slave)
- Timer (4ch)/Interruption control/IR remote control/RTC
- 10-bit ADC (8ch)/10-bit DAC (6ch)

3D
- HDMI 1.4a compatible (input & output)
- 120 Hz alternate output, 60 Hz simultaneous output

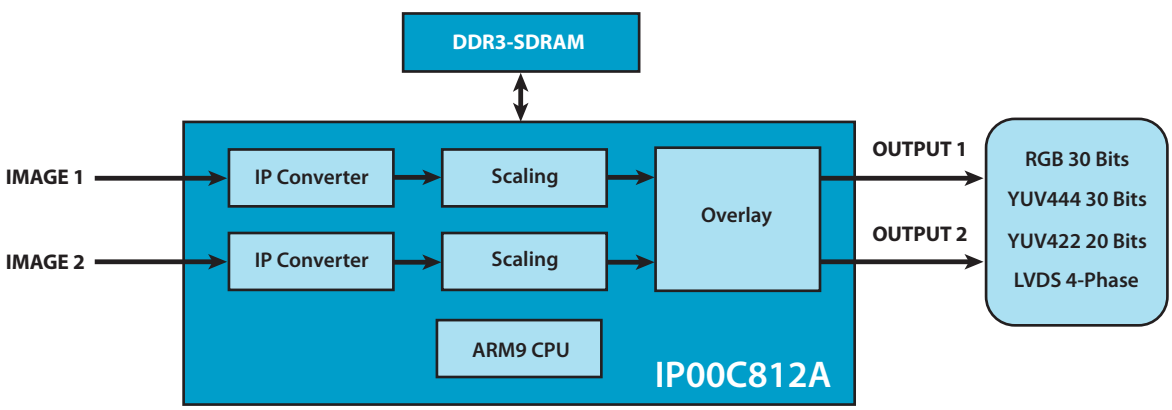
EXTERNAL CPU INTERFACE
- 8-bit parallel, 4-line serial (with external CPU)
- External connection to Flash/SRAM/SDRAM
- Address: 23-bit/Data: 16-bit
- External interruption input (4 line)

IMAGE QUALITY CONTROL
- Horizontal and vertical edge enhancement circuits
- 12-bit color gamma correction table x 2 (2, 7, or 31 set) x 2
- H and V edge enhancement function (9 symbols)
- Bias x 3, Gain x 2, CSC equipped for RGB <-> YUV
- Color management function
- Fully compatible with xvYCC
- Uniformity correction
- Input image detection of APL, Histogram, Min/Max, edge strength/position measurement, etc.

EXTERNAL MEMORY
- Memory-bus 64-bit 800MHz
- DDR3-SDRAM PC800 (1G/512M/bit x 16) x 4

POWER SUPPLY
- 3.3V, 1.5V and 1.2V
- Separate power consumption (Scaler and CPU)

PACKAGE
- 900-pin Plastic BGA; 35mm x 35mm (1mm pitch)



IP00C812A Block Diagram

For more information please visit:
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IMAGE PROCESSORS

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