EN71SN10E

1.8V NAND Flash + 1.8V Mobile DDR SDRAM Multi-Chip Package

Features

- Multi-Chip Package
  - NAND Flash Density: 1-Gbits
  - Mobile DDR SDRAM Density: 256-Mbit
- Device Packaging
  - 107 balls FBGA

  Area: 10.5x13 mm; Height: 1.2 mm
- Operating Voltage
  - NAND : 1.7V to 1.95V
  - Mobile DDR SDRAM : 1.7V to 1.95V
- Operating Temperature :-30 °C to +85 °C

NAND FLASH

- Voltage Supply: 1.7V ~ 1.95V
- Organization
  - Memory Cell Array :
    (128M + 4M) x 8bit for 1Gb
  - Multiplexed address/ data
  - Data Register : (2K + 64) x 8bit
- Automatic Program and Erase
  - Page Program : (2K + 64) bytes
  - Block Erase : (128K + 4K) bytes
- Page Read Operation
  - Page Size : (2K + 64) bytes
  - Random Read : 25μs (Max.)
  - Serial Access : 45ns (Min.)
- Memory Cell: 1bit/Memory Cell
- Fast Write Cycle Time
  - Page Program Time : 250μs (Typ.)
  - Block Erase Time : 2ms (Typ.)
- Command/Address/Data Multiplexed I/O Port
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
- Endurance:
  - 100K Program/Erase Cycles (with 1 bit/528 bytes ECC)
  - Data Retention: 10 Years
- Command Register Operation
- Automatic Page 0 Read at Power-Up Option
  - Boot from NAND support
  - Automatic Memory Download
- NOP: 4 cycles
- Cache Program/Read Operation
- Copy-Back Operation
- EDO mode
- OTP Operation

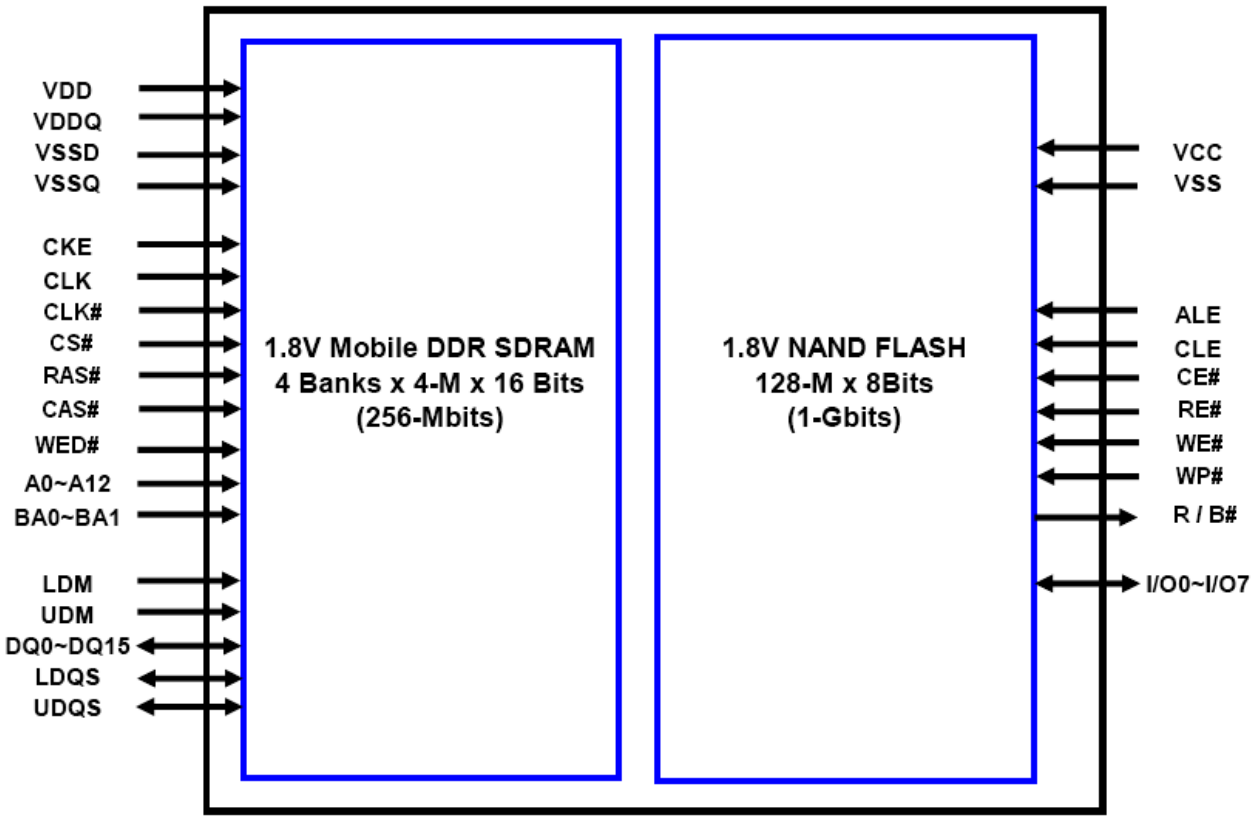
Mobile DDR SDRAM

- Density: 256M bits
- Organization: 4M words x16 bits x 4 banks
- Power supply: V_{DD}/V_{DDQ}= 1.70~1.95V
- Speed: 400Mbps (max.) for data rate
- Internal pipelined double-data-rate architecture, two data access per clock cycle
- Bi-directional data strobe (DQS)
- No DLL; CLK to DQS is not synchronized.
- Differential clock inputs (CLK and CLK#)
- Four bank operation
- CAS Latency: 3
- Burst Type : Sequential and Interleave
- Burst Length : 2, 4, 8, 16
- Special function support
  - PASR (Partial Array Self Refresh)
  - Internal TCSR (Temperature Compensated Self Refresh)
  - DS (Drive Strength)
- All inputs except data & DM are sampled at the rising edge of the system clock(CLK)
- DQS is edge-aligned with data for READ; center-aligned with data for WRITE
- Data mask (DM) for write masking only
- Auto & Self refresh
- 7.8us refresh interval (64ms refresh period, 8K cycle)
- LVCMOS-compatible inputs

Ordering Information

Product ID	NAND Flash		Mobile DDR SDRAM		Package	Operation Temperature Range
	Configuration	Speed	Configuration	Speed		
EN71SN10E-45CFWP	1Gb (128M X 8 bits)	45ns	256Mb (4 Banks X 4M X 16 bits)	200MHz	107 ball FBGA	Wireless

MCP Block Diagram



Ball Configuration

(TOP VIEW)

(FBGA 107, 10.5mmx13mmx1.2mm Boby, 0.8mm Ball Pitch)

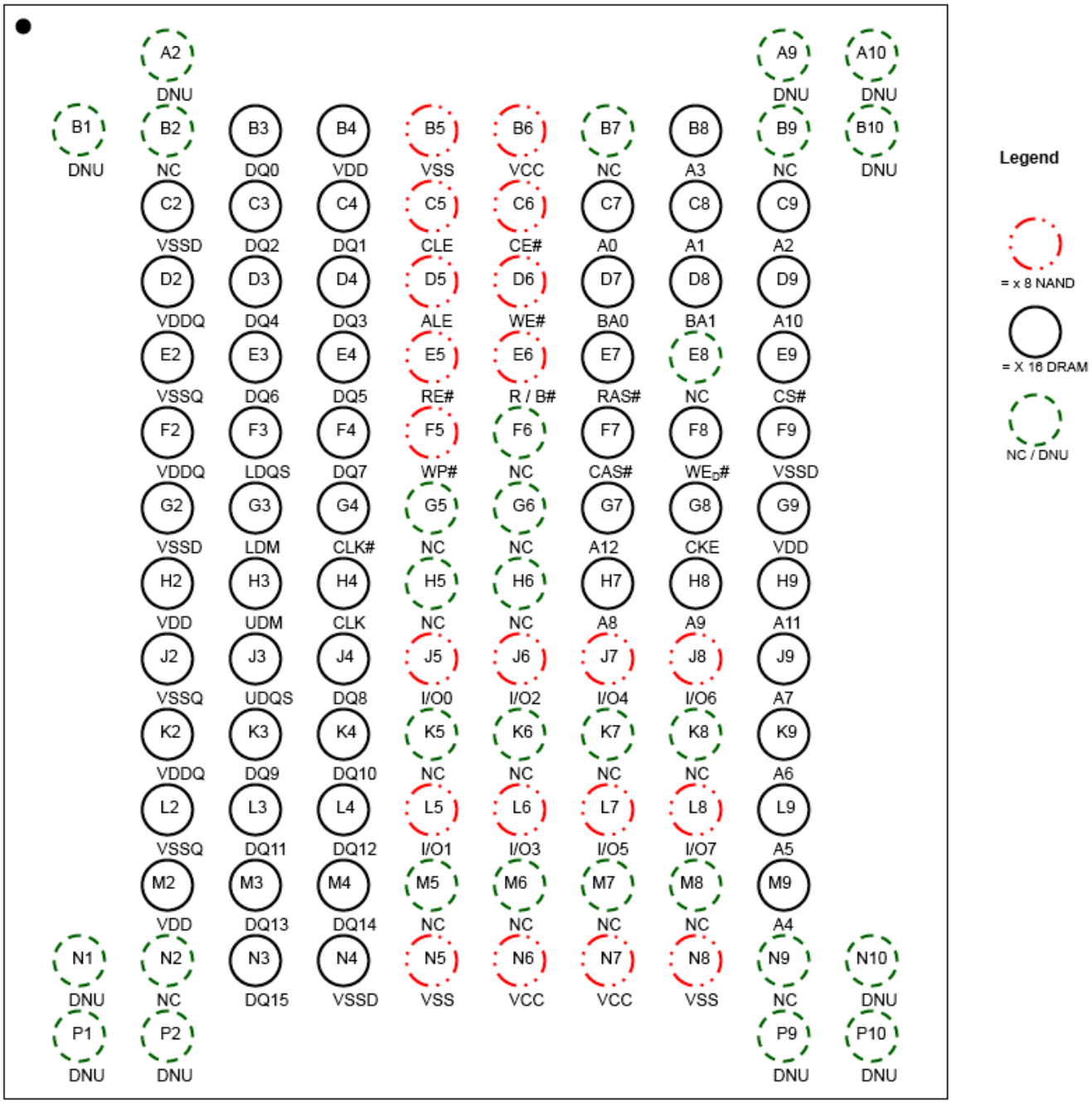
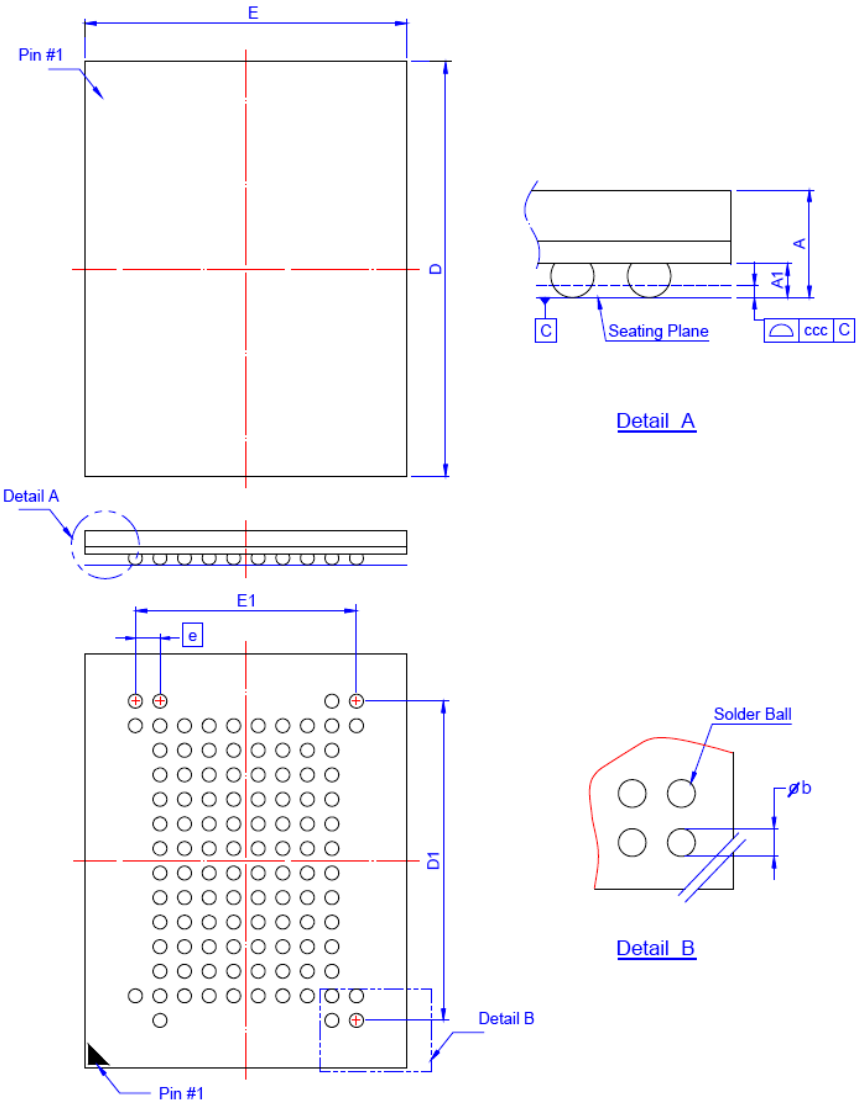


Table 1. Ball Description

Pin Name	Type	Function
NAND		
VCC	Supply	Supply Voltage
VSS	Supply	Ground
I/O0-7	Input/output	Data input/outputs, address inputs, or command inputs
ALE	Input	Address Latch Enable
CLE	Input	Command Latch Enable
CE#	Input	Chip Enable
RE#	Input	Read Enable
WE#	Input	Write Enable
WP#	Input	Write Protect
R / B#	Output	Ready/Busy (open-drain output)
Mobile DDR SDRAM		
VDD	Supply	Power Supply
VSSD	Supply	Ground
VDDQ	Supply	DQ's Power Supply: Isolated on the die for improved noise immunity.
VSSQ	Supply	Ground
CLK, CLK#	Input	CLK and CLK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CLK and negative edge of CLK# . Input and output data is referenced to the crossing of CLK and CLK# (both directions of crossing). Internal clock signals are derived from CLK, CLK#
CKE	Input	CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWERDOWN (row ACTIVE in any bank). CKE is synchronous for all functions except for SELF REFRESH EXIT, which is achieved asynchronously. Input buffers, excluding CLK, CLK# and CKE, are disabled during power-down and self refresh mode which are contrived for low standby power consumption.
CS#	Input	CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
RAS# , CAS# , WE_D#	Input	CAS#, RAS# , and WE_D# (along with CS#) define the command being entered.
A0-A12	Input	Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ / WRITE commands, to select one location out of the memory array in the respective bank. The address inputs also provide the opcode during a MODE REGISTER SET command.
BA0, BA1	Input	BA0 and BA1 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied.
DQ0-15	Input / Output	Data Input/Output pins operate in the same manner as on conventional DRAMs.
LDQS, UDQS	Input / Output	Output with read data, input with write data. Edge-aligned with read data, centered with write data. Used to capture write data. LDQS corresponds to the data on DQ0-DQ7, UDQS corresponds to the data on DQ8-DQ15.
LDM, UDM	Input	DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading matches the DQ and DQS loading. LDM corresponds to the data on DQ0-DQ7, UDM corresponds to the data on DQ8-DQ15.

PACKAGE DIMENSION
107-BALL FBGA (10.5x13 mm)



Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	1.07	1.14	1.21	0.042	0.045	0.048
A_1	0.35	0.40	0.45	0.014	0.016	0.018
Φb	0.45	0.50	0.55	0.018	0.020	0.022
D	12.90	13.00	13.10	0.508	0.512	0.516
E	10.40	10.50	10.60	0.409	0.413	0.417
D_1	10.40 BSC			0.409 BSC		
E_1	7.20 BSC			0.283 BSC		
e	0.80 BSC			0.031 BSC		
ccc	———	———	0.10	———	———	0.004

Controlling dimension : Millimeter.

NAND Flash Memory Operations

General Description

The NAND Flash is a 128Mx8bit with spare 4Mx8bit capacity. The NAND Flash is offered in 1.8V VCC Power Supply. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased.

The NAND Flash contains 1024 blocks, composed by 64 pages consisting in two NAND structures of 32 series connected Flash cells. A program operation allows to write the 1056-Word page in typical 250us and an erase operation can be performed in typical 2ms on a 128K-Byte for device block.

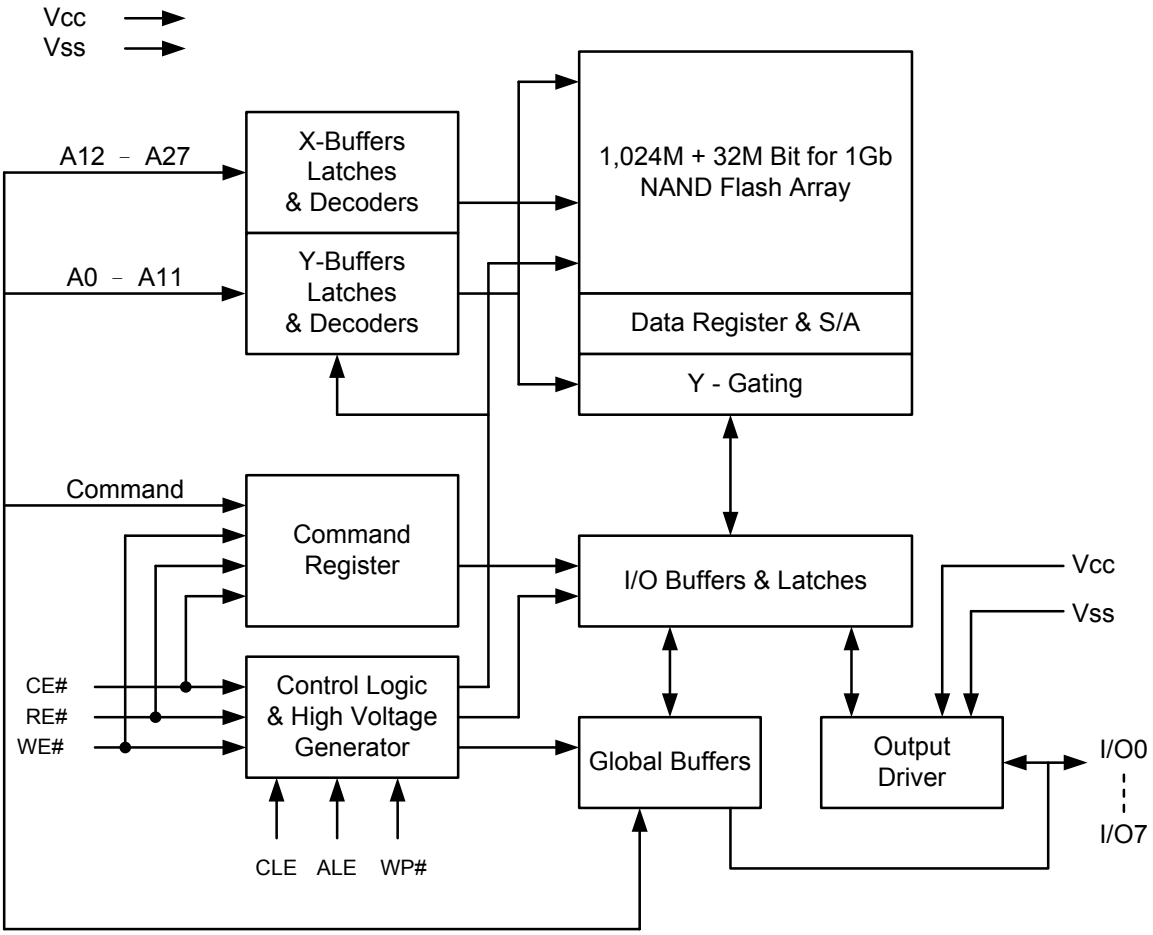
Data in the page mode can be read out at 45ns cycle time per Byte. The I/O pins serve as the ports for address and command inputs as well as data input/output. The copy back function allows the optimization of defective blocks management: when a page program operation fails the data can be directly programmed in another page inside the same array section without the time consuming serial data insertion phase. The cache program feature allows the data insertion in the cache register while the data register is copied into the Flash array. This pipelined program operation improves the program throughput when long files are written inside the memory. A cache read feature is also implemented. This feature allows to dramatically improving the read throughput when consecutive pages have to be streamed out. This NAND Flash includes extra feature: Automatic Read at Power Up.

Table 2. Pin Description

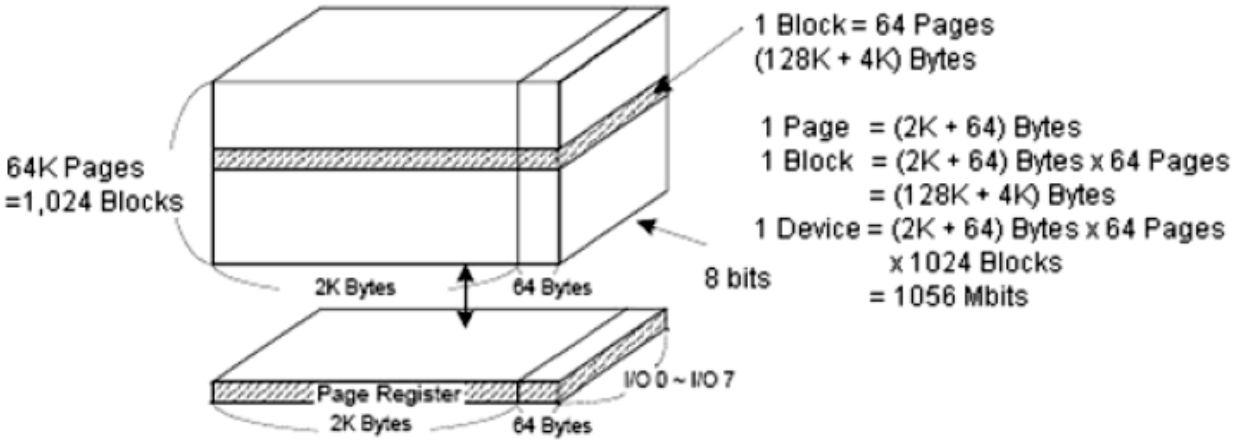
Symbol	Pin Name	Function
I/O0 – I/O7	Data Inputs/Outputs	The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to Hi-Z when the chip is deselected or when the outputs are disabled.
CLE	Command Latch Enable	The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the WE# signal.
ALE	Address Latch Enable	The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of WE# with ALE high.
CE#	Chip Enable	The CE# input is the device selection control. When the device is in the Busy state, CE# high is ignored, and the device does not return to standby mode in program or erase operation. Regarding CE# control during read operation, refer to 'Page read' section of Device operation.
RE#	Read Enable	The RE# input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid t_{REA} after the falling edge of RE# which also increments the internal column address counter by one.
WE#	Write Enable	The WE# input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the WE# pulse.
WP#	Write Protect	The WP# pin provides inadvertent program/erase protection during power transitions. The internal high voltage generator is reset when the WP# pin is active low.
R/B#	Ready/Busy Output	The R/B# output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to Hi-Z condition when the chip is deselected or when outputs are disabled.
V_{CC}	Power Supply	V_{CC} is the power supply for device.
V_{SS}	Ground	
NC	No Connection	Lead is not internally connected.

Note: Connect all V_{CC} and V_{SS} pins of each device to common power supply outputs. Do not leave V_{CC} or V_{SS} disconnected.

Block Diagram



Array Organization



Address Cycle Map

	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	Address
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7	**Column Address**
2nd Cycle	A8	A9	A10	A11	L*	L*	L*	L*	**Column Address**
3rd Cycle	A12	A13	A14	A15	A16	A17	A18	A19	**Row Address**
4th Cycle	A20	A21	A22	A23	A24	A25	A26	A27	**Row Address**

Note:

1. Column Address : Starting Address of the Register.
2. * L must be set to “Low”.
3. * The device ignores any additional input of address cycles than required.

Product Introduction

The NAND Flash is a 1,056Mbit memory organized as 64K rows (pages) by 2,112x8 columns. Spare 64x8 columns are located from column address of 2,048~2,111. A 2,112-byte data register is connected to memory cell arrays accommodating data transfer between the I/O buffers and memory during page read and page program operations. The program and read operations are executed on a page basis, while the erase operation is executed on a block basis. The memory array consists of 1,024 separately erasable 128K-byte blocks. It indicates that the bit-by-bit erase operation is prohibited on the NAND Flash.

The NAND Flash has addresses multiplexed into 8 I/Os. This scheme dramatically reduces pin counts and allows system upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through I/O's by bringing WE# to low while CE# is low. Those are latched on the rising edge of WE#. Command Latch Enable (CLE) and Address Latch Enable (ALE) are used to multiplex command and address respectively, via the I/O pins. Some commands require one bus cycle. For example, Reset Command, Status Read Command, etc require just one cycle bus. Some other commands, like page read and block erase and page program, require two cycles: one cycle for setup and the other cycle for execution.

In addition to the enhanced architecture and interface, the NAND Flash incorporates copy-back program feature from one page to another page without need for transporting the data to and from the external buffer memory.

Command Set

Function	1st Cycle	2nd Cycle	Acceptable Command during Busy
Read	00h	30h	
Read for Copy Back	00h	35h	
Read ID	90h	-	
Reset	FFh	-	O
Page Program	80h	10h	
Copy-Back Program	85h	10h	
Block Erase	60h	D0h	
Random Data Input (1)	85h	-	
Random Data Output (1)	05h	E0h	
Read Status	70h	-	O
Cache Program	80h	15h	
Cache Read	31h	-	
Read Start for Last Page Cache Read	3Fh	-	

Note:
1. Random Data Input / Output can be executed in a page.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_{CC}	-0.6 to +2.45	V
	V_{IN}	-0.6 to +2.45	
	$V_{I/O}$	-0.6 to VCC + 0.3 (< 2.45)	
Temperature Under Bias	T_{BIAS}	-40 to +125	℃
Storage Temperature	T_{STG}	-65 to +150	℃
Short Circuit Current	I_{OS}	5	mA

Note:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltage reference to GND, T_A = – 30°C to 85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	1.7	1.8	1.95	V
Supply Voltage	V_{SS}	0	0	0	V

DC AND OPERATION CHARACTERISTICS

(Recommended operating conditions otherwise noted)

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Operating Current	Page Read with Serial Access	I_{CC1}	t_{RC}=45ns, CE# =V_{IL}, I_{OUT}=0mA	-	15	30	mA
	Program	I_{CC2}	-	-	15	30	
	Erase	I_{CC3}	-	-	15	30	
Stand-by Current (TTL)		I_{SB1}	CE# =V_{IH}, WP# =0V/V_{CC}	-	-	1	mA
Stand-by Current (CMOS)		I_{SB2}	CE# = V_{CC} -0.2, WP# =0V/ V_{CC}	-	10	50	uA
Input Leakage Current		I_{LI}	V_{IN}=0 to V_{CC} (max)	-	-	±10	uA
Output Leakage Current		I_{LO}	V_{OUT}=0 to V_{CC} (max)	-	-	±10	uA
Input High Voltage		V_{IH} (1)	-	0.8 x V_{CC}	-	V_{CC} +0.3	V
Input Low Voltage, All inputs		V_{IL} (1)	-	-0.3	-	0.2 x V_{CC}	V
Output High Voltage Level		V_{OH}	I_{OH}=-100uA	V_{CC} -0.1	-	-	V
Output Low Voltage Level		V_{OL}	I_{OL}=+100uA	-	-	0.1	V
Output Low Current (R/B#)		I_{OL} (R /B#)	V_{OL}=0.1V	3	4	-	mA

Note:

1. V_{IL} can undershoot to -0.4V and V_{IH} can overshoot to V_{CC}+0.4V for durations of 20ns or less.
2. Typical value are measured at V_{CC} =1.8V, T_A = 25℃. And not 100% tested.

VALID BLOCK

Symbol	Min.	Typ.	Max.	Unit
N_{VB}	1,004	-	1,024	Blocks

Note:

1. The device may include initial invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented as first shipped. Invalid blocks are defined as blocks that contain one or more bad bits which cause status failure during program and erase operation. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for appropriate management of initial invalid blocks.
2. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block at the time of shipment and is guaranteed to be a valid block up to 1K program/erase cycles with 1 bit/528 bytes ECC.

AC TEST CONDITION

(T_A = – 30°C to 85°C, V_{CC}=1.7V~1.95V)

Parameter	Condition
Input Pulse Levels	0V to V_{CC}
Input Rise and Fall Times	5 ns
Input and Output Timing Levels	V_{CC} /2
Output Load	1 TTL Gate and C_L=30pF

Note:

* Refer to Ready / Busy# section, R/B# output's Busy to Ready time is decided by the pull-up resistor (R_P) tied to R/B# pin.

CAPACITANCE

(T_A = 25°C, V_{CC}=1.8V, f =1.0MHz)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input / Output Capacitance	$C_{I/O}$	V_{IL} = 0V	-	10	pF
Input Capacitance	C_{IN}	V_{IN} = 0V	-	10	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CLE	ALE	CE#	WE#	RE#	WP#	Mode	
H	L	L		H	X	Read Mode	Command Input
L	H	L		H	X		Address Input (4 clock)
H	L	L		H	H	Write Mode	Command Input
L	H	L		H	H		Address Input (4 clock)
L	L	L		H	H	Data Input	
L	L	L	H		X	Data Output	
X	X	X	X	H	X	During Read (Busy)	
X	X	X	X	X	H	During Program (Busy)	
X	X	X	X	X	H	During Erase (Busy)	
X	X (1)	X	X	X	L	Write Protect	
X	X	H	X	X	0V/V_{CC} (2)	Stand-by	

Note:
1. X can be V_{IL} or V_{IH}.
2. WP# should be biased to CMOS high or CMOS low for stand-by.

Program / Erase Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Program Time	t_{PROG}	-	250	700	us
Dummy Busy Time for Cache Program	t_{CBSY}	-	3	700	us
Number of Partial Program Cycles in the Same Page	N_{OP}	-	-	4	Cycle
Block Erase Time	t_{BERS}	-	2	10	ms

Note:
1. Typical program time is defined as the time within which more than 50% of the whole pages are programmed at 1.8V V_{CC} and 25°C temperature.
2. t_{PROG} is the average program time of all pages. Users should be noted that the program time variation from page to page is possible.
3. Max. time of t_{CBSY} depends on timing between internal program completion and data in.

AC Timing Characteristics for Command / Address / Data Input

Parameter	Symbol	Min.	Max.	Unit
CLE Setup Time	t_{CLS} (1)	25	-	ns
CLE Hold Time	t_{CLH}	10	-	ns
CE# Setup Time	t_{CS} (1)	35	-	ns
CE# Hold Time	t_{CH}	10	-	ns
WE# Pulse Width	t_{WP}	25	-	ns
ALE Setup Time	t_{ALS} (1)	25	-	ns
ALE Hold Time	t_{ALH}	10	-	ns
Data Setup Time	t_{DS} (1)	20	-	ns
Data Hold Time	t_{DH}	10	-	ns
Write Cycle Time	t_{WC}	45	-	ns
WE# High Hold Time	t_{WH}	15	-	ns
ALE to Data Loading Time	t_{ADL} (2)	100	-	ns

Note:

1. The transition of the corresponding control pins must occur only once while WE# is held low.
2. t_{ADL} is the time from the WE# rising edge of final address cycle to the WE# rising edge of first data cycle.

AC Characteristics for Operation

Parameter		Symbol	Min.	Max.	Unit
Data Transfer from Cell to Register		t_R	-	25	us
ALE to RE# Delay		t_{AR}	10	-	ns
CLE to RE# Delay		t_{CLR}	10	-	ns
Ready to RE# Low		t_{RR}	20	-	ns
RE# Pulse Width		t_{RP}	25	-	ns
WE# High to Busy		t_{WB}	-	100	ns
WP# Low to WE# Low (disable mode)		t_{WW}	100	-	ns
WP# High to WE# Low (enable mode)					
Read Cycle Time		t_{RC}	45	-	ns
RE# Access Time		t_{REA}	-	30	ns
CE# Access Time		t_{CEA}	-	45	ns
RE# High to Output Hi-Z		t_{RHZ}	-	100	ns
CE# High to Output Hi-Z		t_{CHZ}	-	30	ns
CE# High to ALE or CLE Don't Care		t_{CSD}	0	-	ns
RE# High to Output Hold		t_{RHOH}	15	-	ns
RE# Low to Output Hold		t_{RLOH}	5	-	ns
CE# High to Output Hold		t_{COH}	15	-	ns
RE# High Hold Time		t_{REH}	15	-	ns
Output Hi-Z to RE# Low		t_{IR}	0	-	ns
RE# High to WE# Low		t_{RHW}	100	-	ns
WE# High to RE# Low		t_{WHR}	60	-	ns
Device Resetting Time during ...	Read	t_{RST}	-	5	us
	Program		-	10	us
	Erase		-	500	us
	Ready		-	5(1)	us
Cache Busy in Read Cache (following 31h and 3Fh)		t_{DCBSYR}	-	30	us

Note:

1. If reset command (FFh) is written at Ready state, the device goes into Busy for maximum 5us.

NAND Flash Technical Notes

Mask Out Initial Invalid Block(s)

Initial invalid blocks are defined as blocks that contain one or more initial invalid bits whose reliability is not guaranteed by Eon. The information regarding the initial invalid block(s) is called as the initial invalid block information. Devices with initial invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An initial invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the initial invalid block(s) via address mapping.

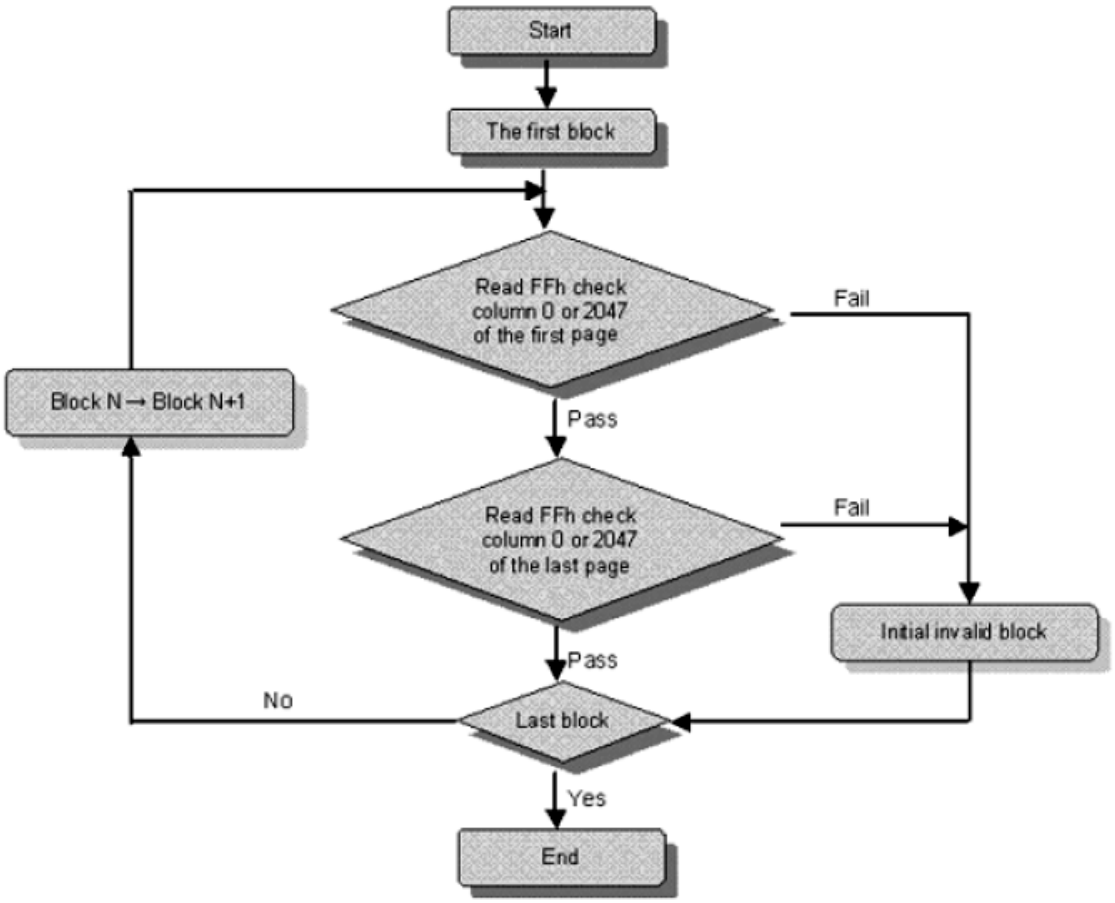
The 1st block, which is placed on 00h block address, is guaranteed to be a valid block up to 1K program/erase cycles with 1 bit/528 bytes ECC.

Identifying Initial Invalid Block(s) and Block Replacement Management

Unpredictable behavior may result from programming or erasing the defective blocks. The under figure illustrates an algorithm for searching factory-mapped defects, and the algorithm needs to be executed prior to any erase or program operations.

A host controller has to scan blocks from block 0 to the last block using page read command and check the data at the column address of 0 or 2,047. If the read data is not FFh, the block is interpreted as an invalid block. The initial invalid block information is erasable, and which is impossible to be recovered once it has been erased. Therefore, the host controller must be able to recognize the initial invalid block information and to create a corresponding table to manage block replacement upon erase or program error when additional invalid blocks develop with Flash memory usage.

Algorithm for Bad Block Scanning




```
For (i=0; i<Num_of_LUs; i++)
{
      For (j=0; j<Blocks_Per_LU; j++)
      {
            Defect_Block_Found=False;

            Read_Page(lu=i, block=j, page=0);
            If (Data[coloumn=0]!=FFh)     Defect_Block_Found=True;
            If (Data[coloumn=First_Byte_of_Spare_Area]!=FFh)   Defect_Block_Found=True;

            Read_Page(lu=i, block=j, page=Page_Per_Block-1);
            If (Data[coloumn=0]!=FFh)     Defect_Block_Found=True;
            If (Data[coloumn=First_Byte_of_Spare_Area]!=FFh)   Defect_Block_Found=True;

            If (Defect_Block_Found)       Mark_Block_as_Defective(lu=i, block=j);
       }
}
```

Error in Write or Read Operation

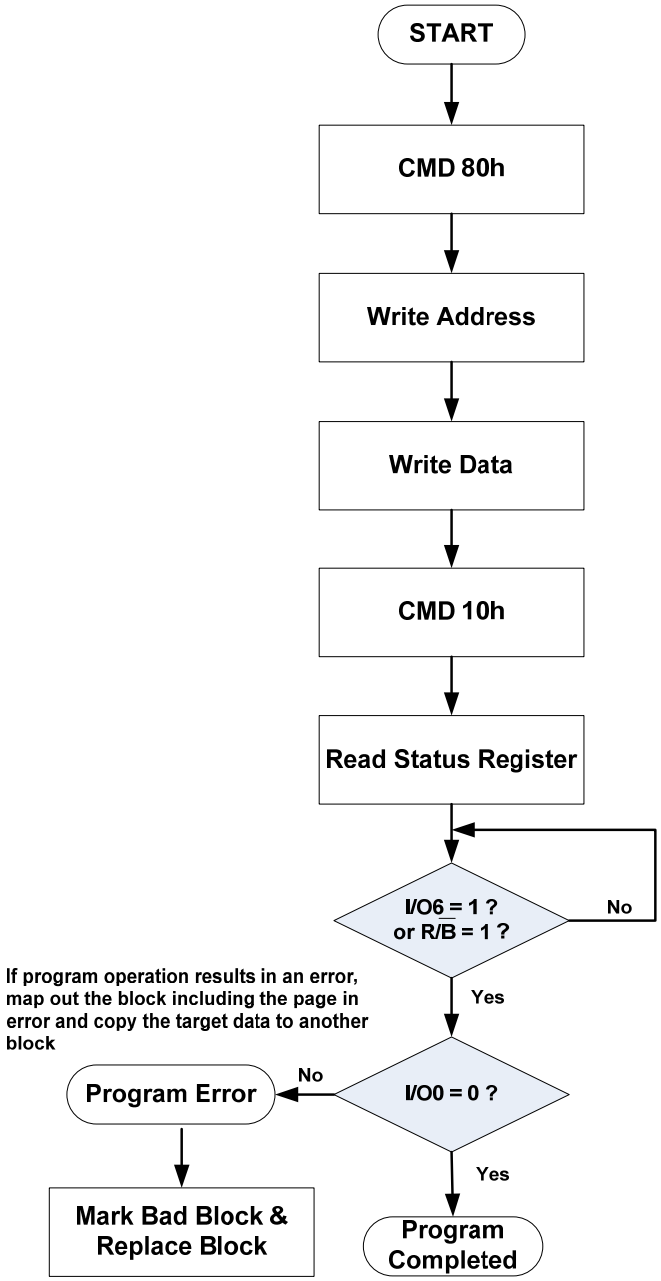
Within its lifetime, the additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the actual data. The following possible failure modes should be considered to implement a highly reliable system. In the case of status read failure after erase or program, block replacement should be done. Because program status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block. In case of Read, ECC must be employed. To improve the efficiency of memory space, it is recommended that the read or verification failure due to single bit error be reclaimed by ECC without any block replacement. The additional block failure rate does not include those reclaimed blocks.

Failure		Detection and Countermeasure sequence
Write	Erase Failure	Read Status after Erase → Block Replacement
	Program Failure	Read Status after Program → Block Replacement
Read	Single Bits Failure	Verify ECC → ECC Correction

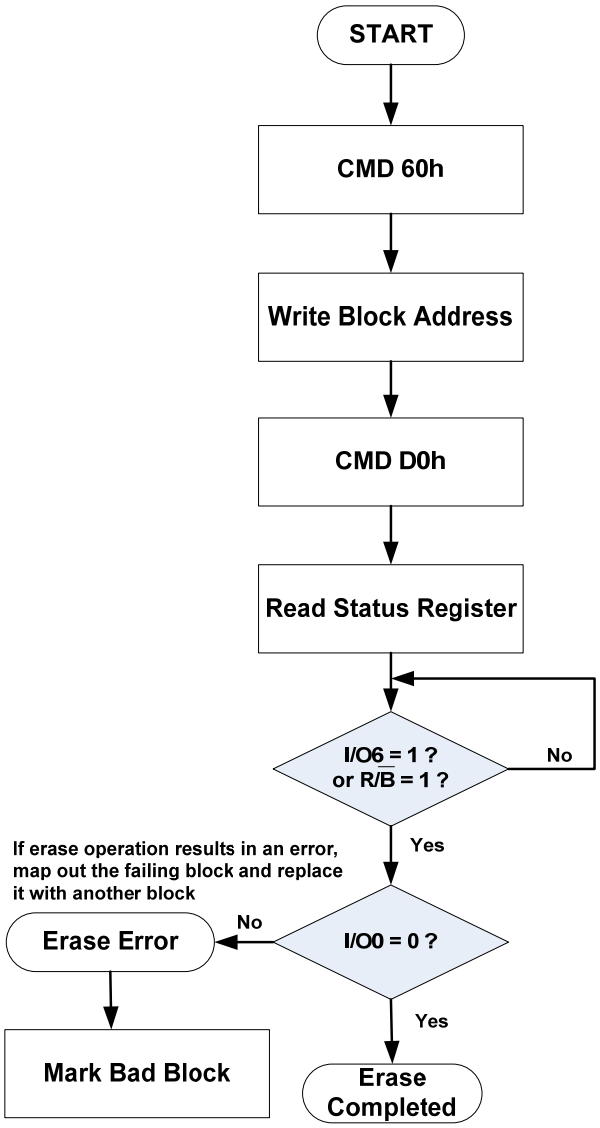
Note:

1. Error Correcting Code --> Hamming Code etc.
2. Example: 1bit correction / 528 Byte

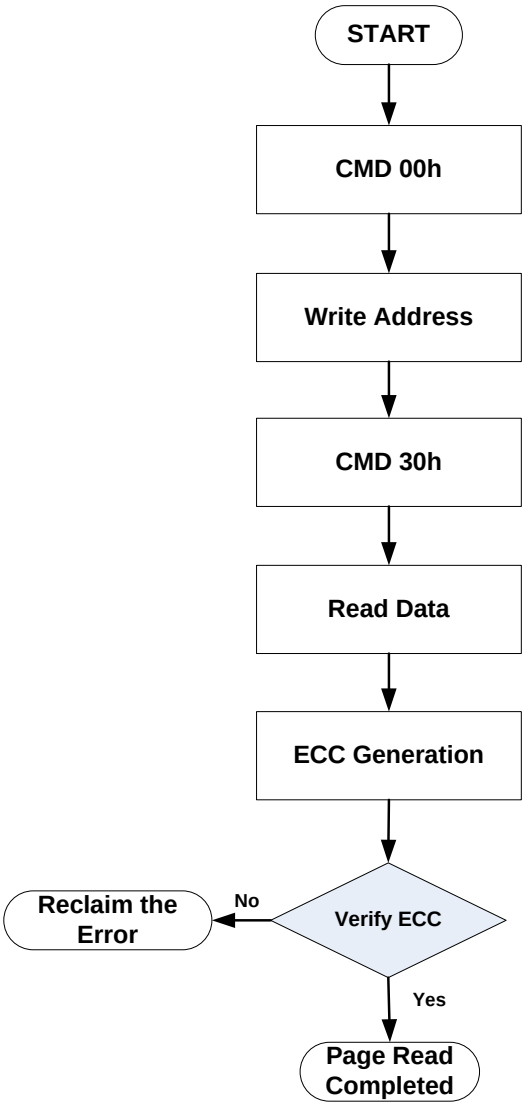
Program Flow Chart



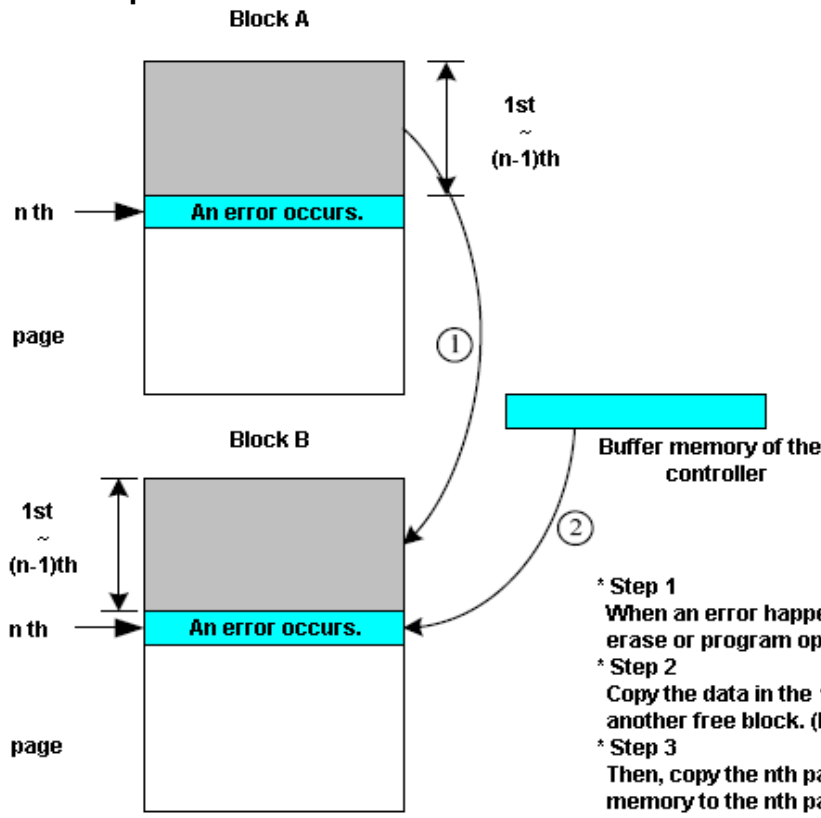
Erase Flow Chart



Read Flow Chart



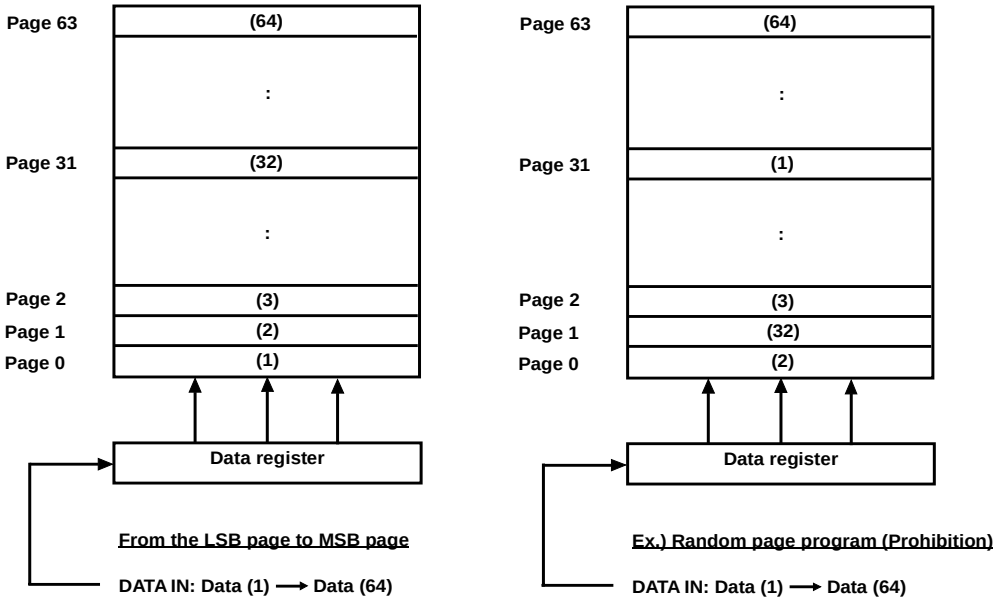
Block Replacement



* Step 1
When an error happens in the nth page of the Block 'A' during erase or program operation.
* Step 2
Copy the data in the 1st ~ (n-1)th page to the same location of another free block. (Block 'B')
* Step 3
Then, copy the nth page data of the Block 'A' in the buffer memory to the nth page of the Block 'B'.
* Step 4
Do not erase or program to Block 'A' by creating an 'invalid block' table or other appropriate scheme.

Addressing for program operation

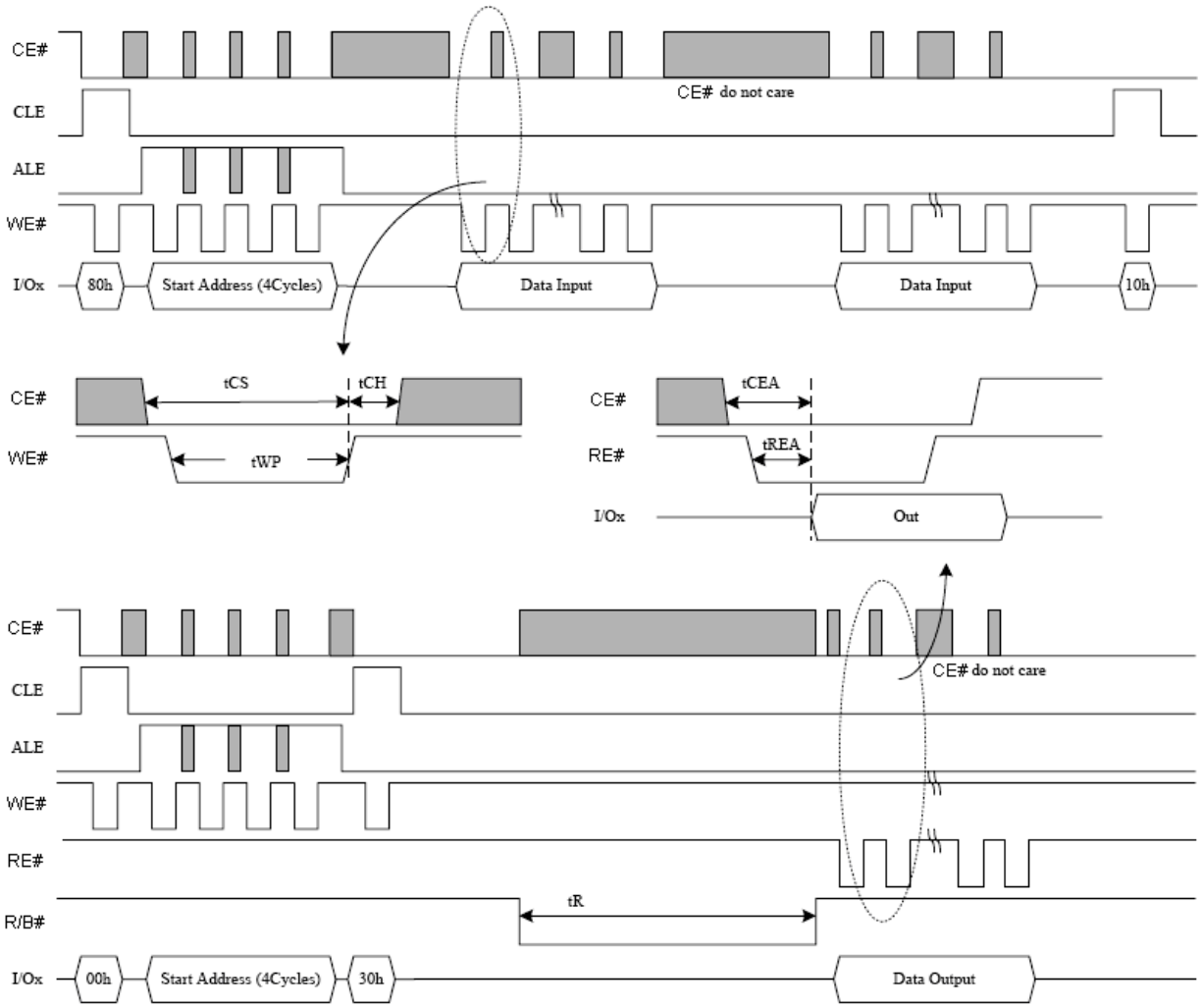
Within a block, the pages must be programmed consecutively from the LSB (Least Significant Bit) page of the block to MSB (Most Significant Bit) pages of the block. Random page address programming is prohibited. In this case, the definition of LSB page is the LSB among the pages to be programmed. Therefore, LSB page doesn't need to be page 0.



System Interface Using CE# don't-care

For an easier system interface, CE# may be inactive during the data-loading or serial access as shown below. The internal 2,112 bytes page registers are utilized as separate buffers for this operation and the system design gets more flexible. In addition, for voice or audio applications that use slow cycle time on the order of u-seconds, de-activating CE# during the data-loading and serial access would provide significant savings in power consumption.

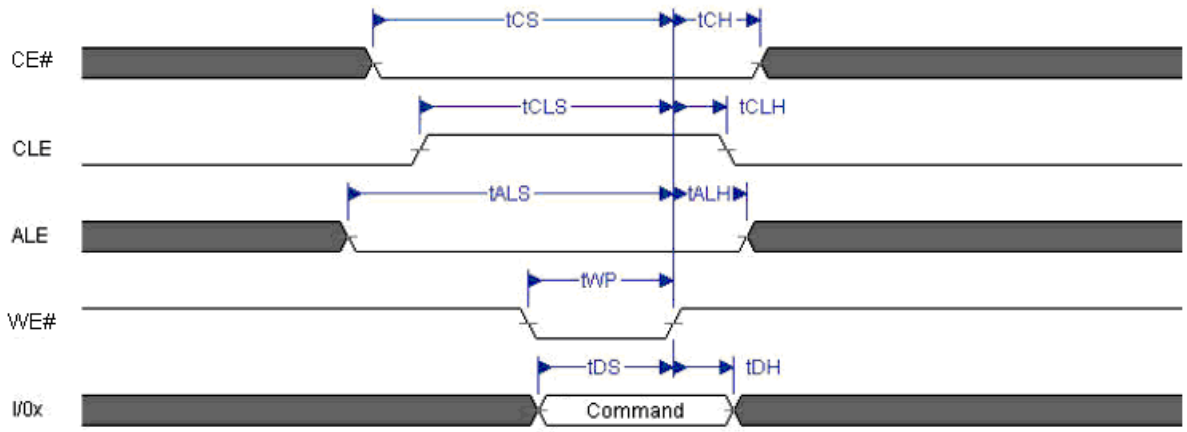
Program / Read Operation with "CE# not-care"



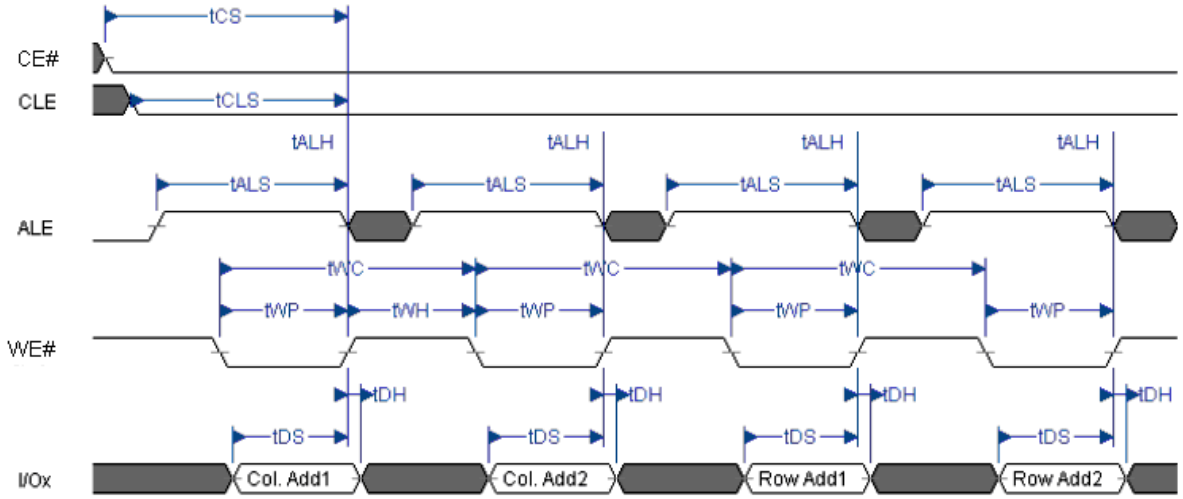
Address Information

DATA	I/O	ADDRESS			
Data In / Out	I/Ox	Col. Add1	Col. Add2	Row Add1	Row Add2
2,112 bytes	I/O0~ I/O7	A0 ~ A7	A8 ~ A11	A12 ~ A19	A20 ~ A27

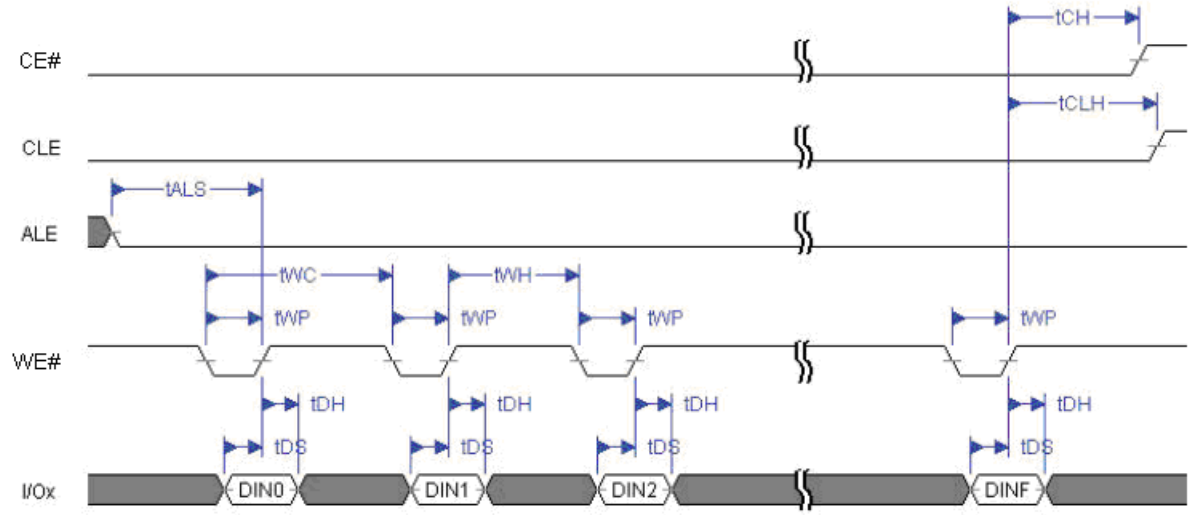
Command Latch Cycle



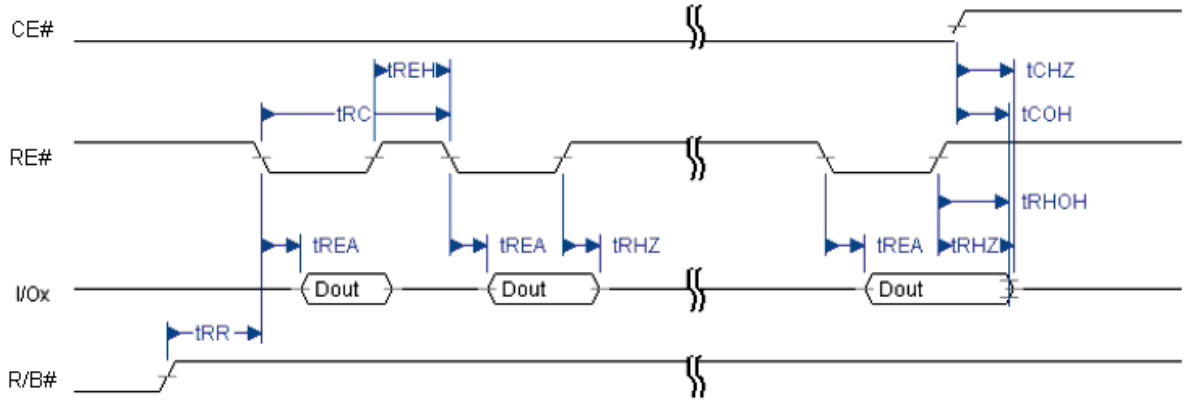
Address Latch Cycle



Input Data Latch Cycle

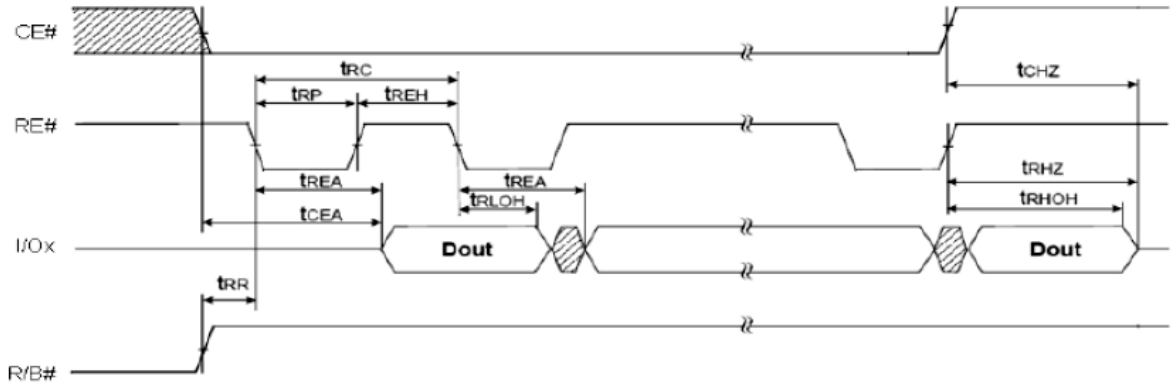


Serial access Cycle after Read (CLE = L, WE# = H, ALE = L)



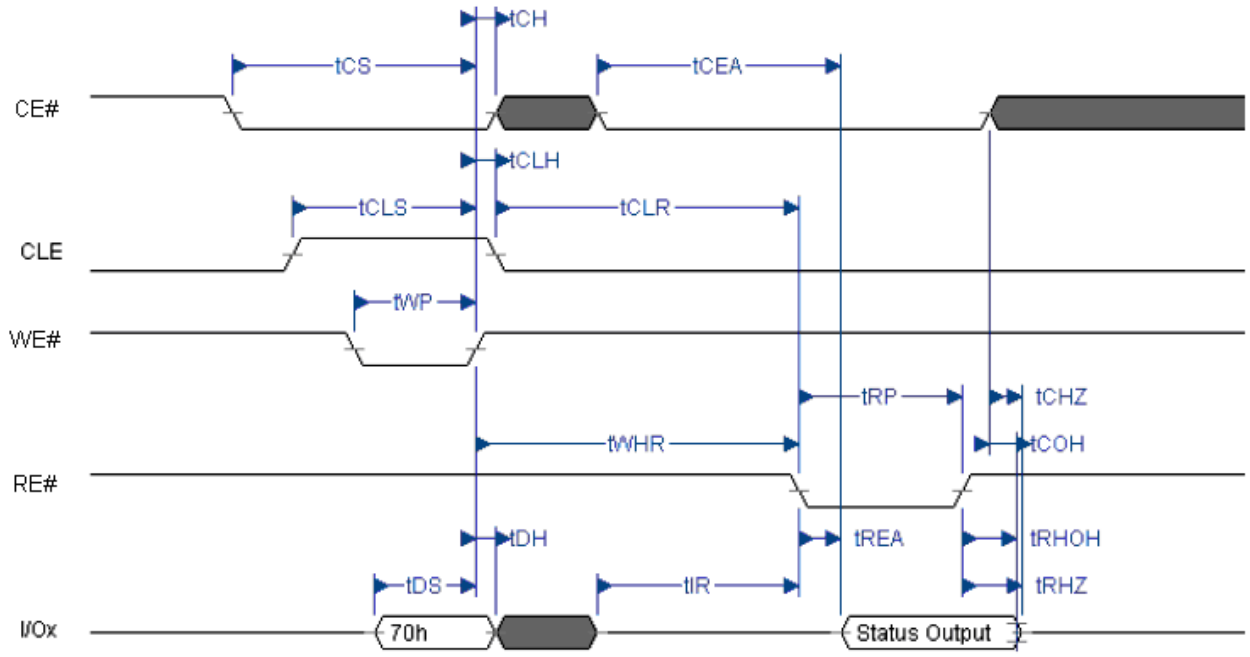
Note:
1. Dout transition is measured at ±200mV from steady state voltage at I/O with load.
2. t_{RHOH} starts to be valid when frequency is lower than 20MHz.

Serial access Cycle after Read (EDO Type CLE = L, WE# = H, ALE = L)

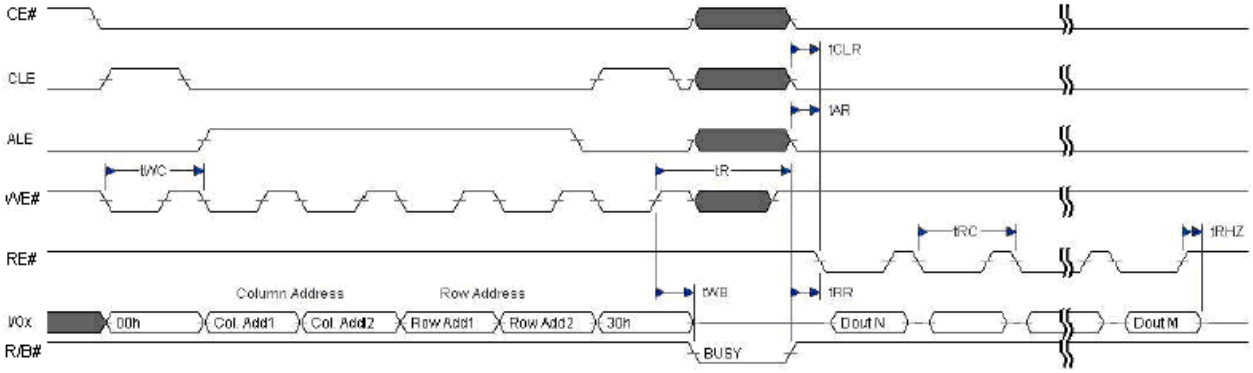


Note:
1. Transition is measured at ±200mV from steady state voltage with load.
2. This parameter is sampled and not 100% tested.
3. t_{RLOH} is valid when frequency is higher than 20MHz.
4. t_{RHOH} starts to be valid when frequency is lower than 20MHz.

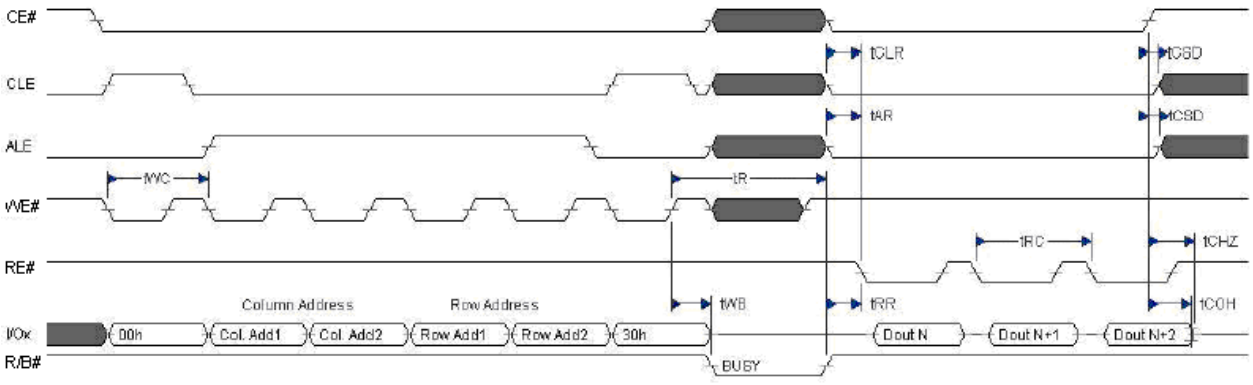
Status Read Cycle



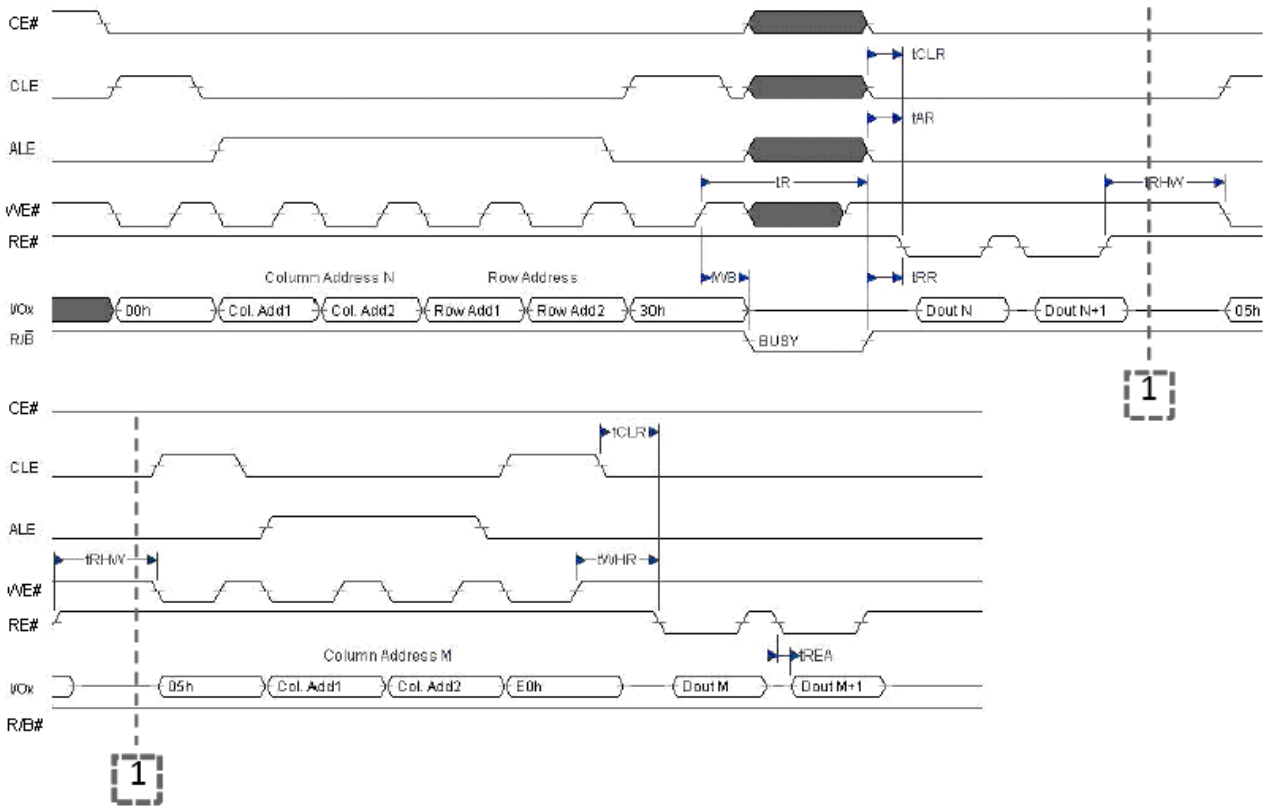
Read Operation



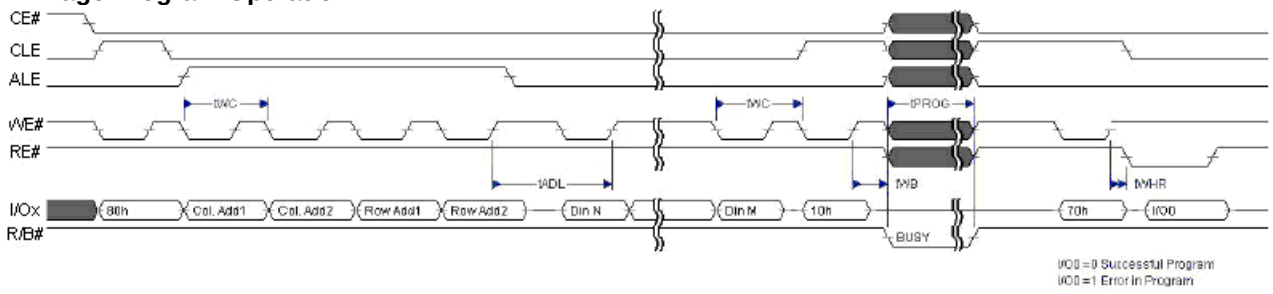
Read Operation (Intercepted by CE#)



Random Data Output In a Page

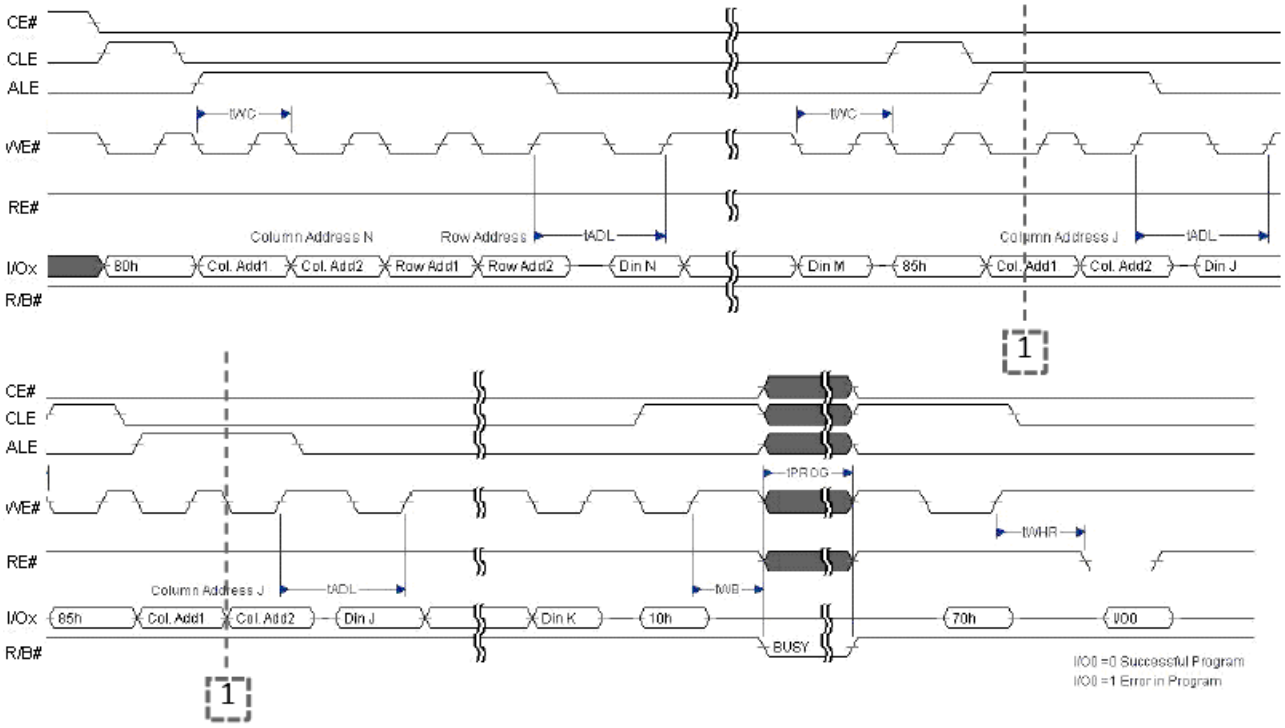


Page Program Operation



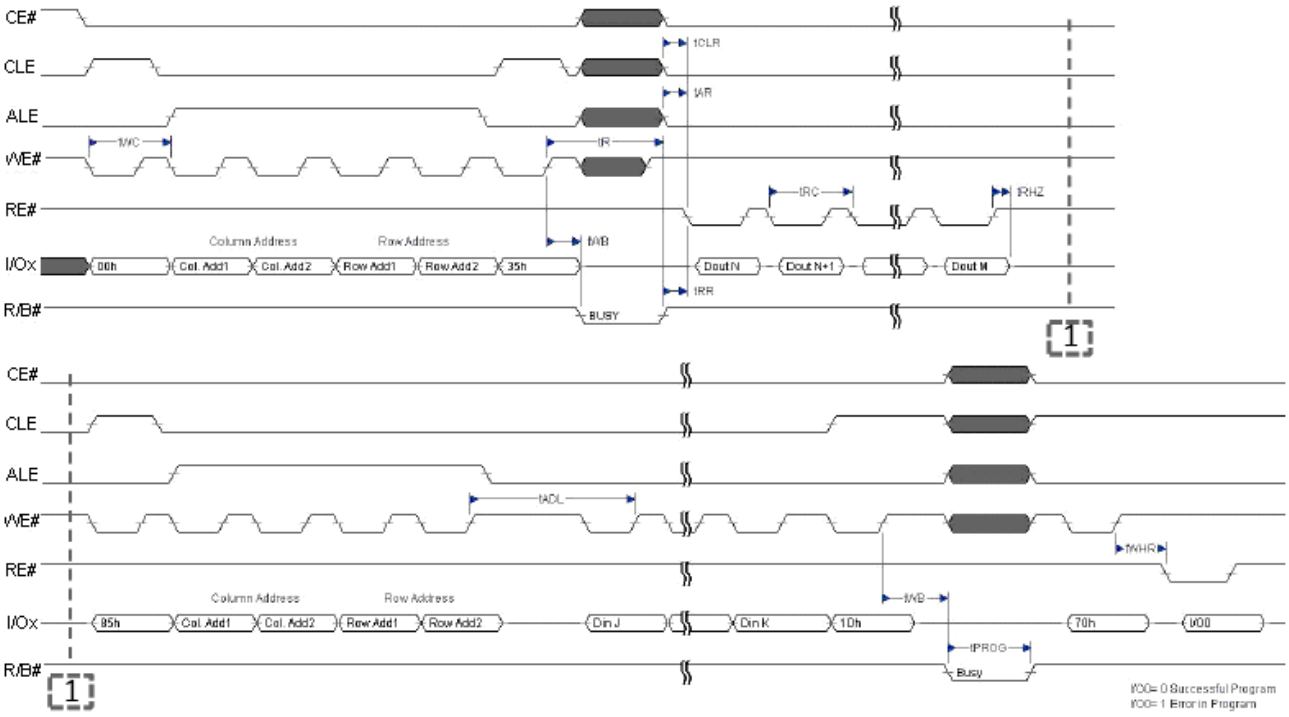
Note: t_{ADL} is the time from WE# rising edge of final address cycle to the WE# rising edge of first data cycle.

Page Program Operation with Random Data Input

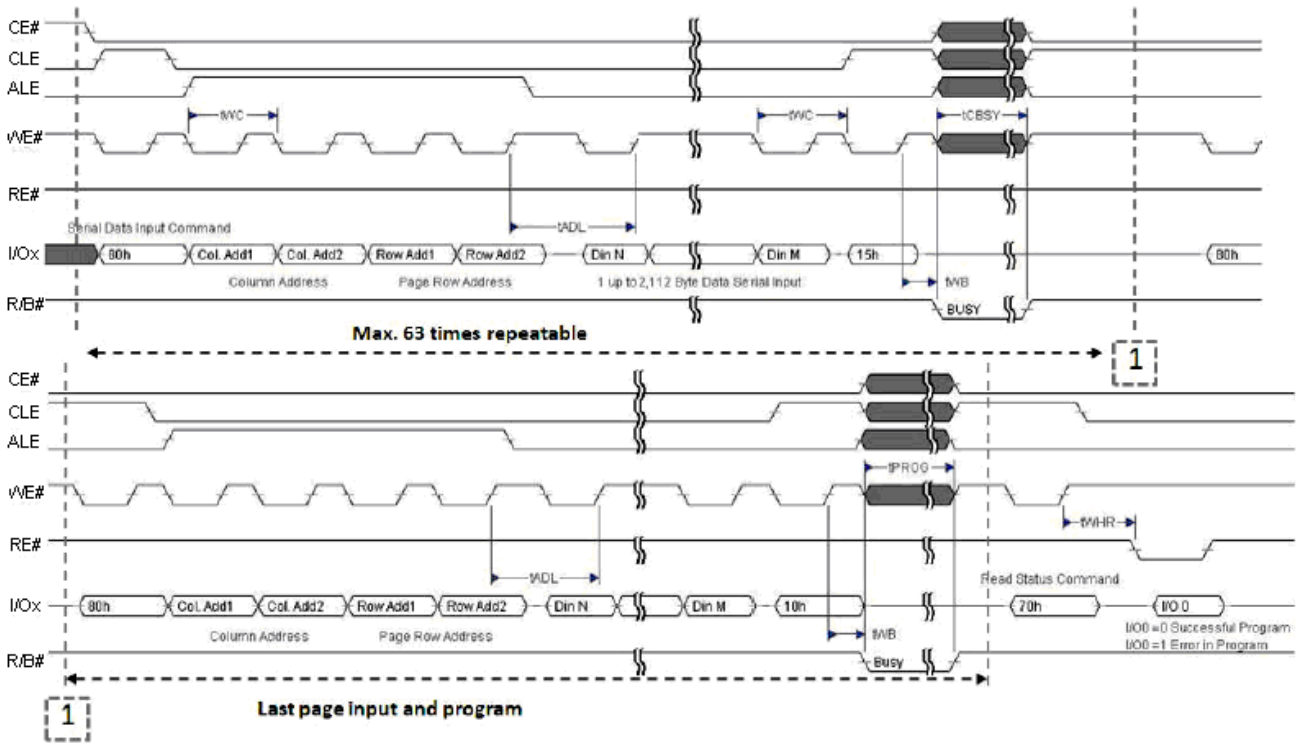


Note: t_{ADL} is the time from WE# rising edge of final address cycle to the WE# rising edge of first data cycle.

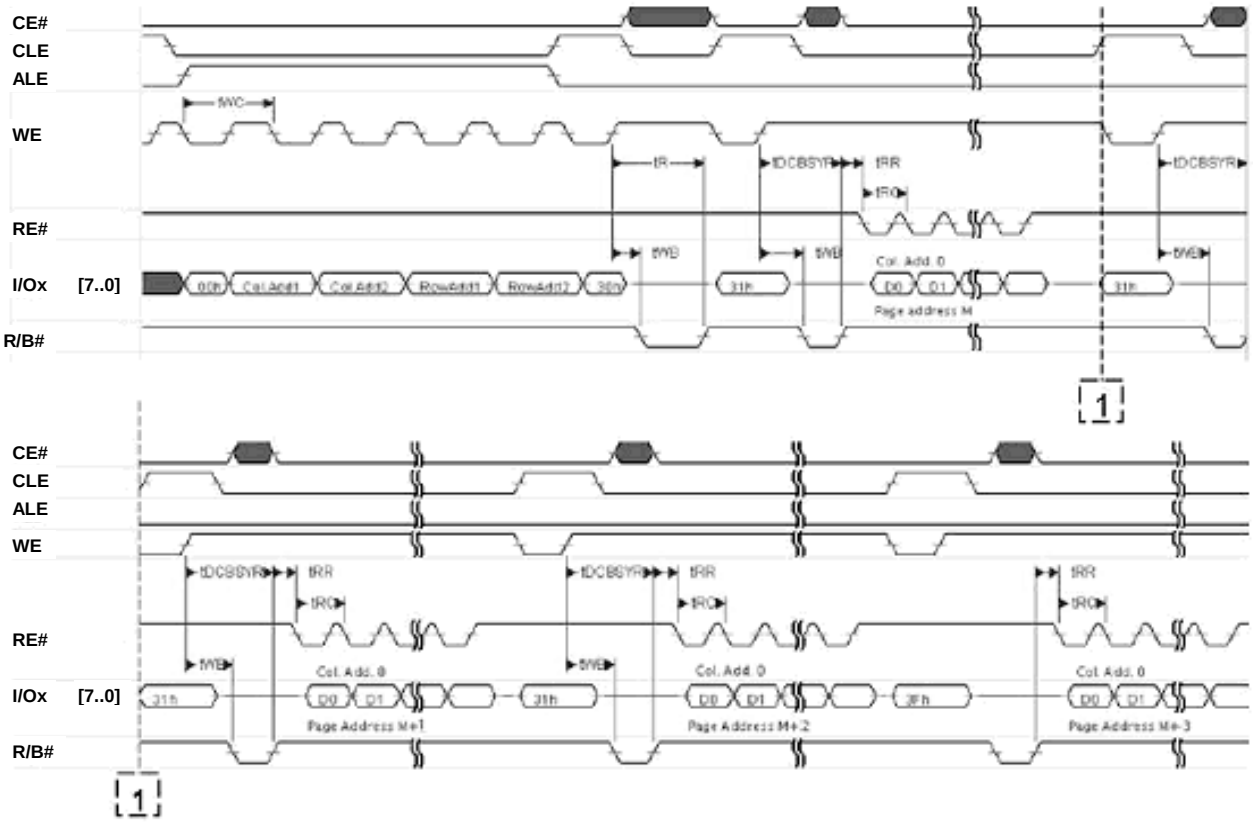
Copy-Back Program Operation with Random Data Input



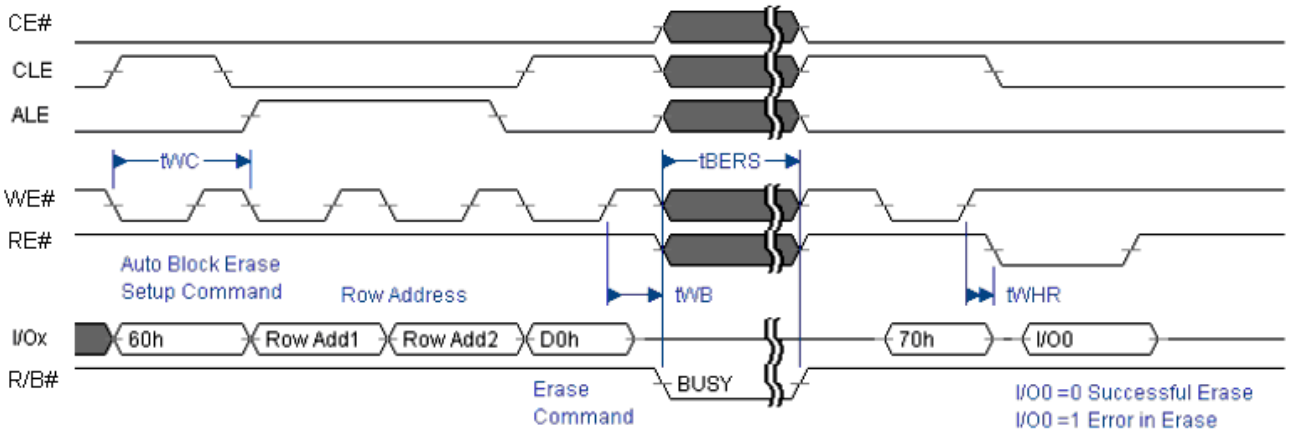
Cache Program Operation



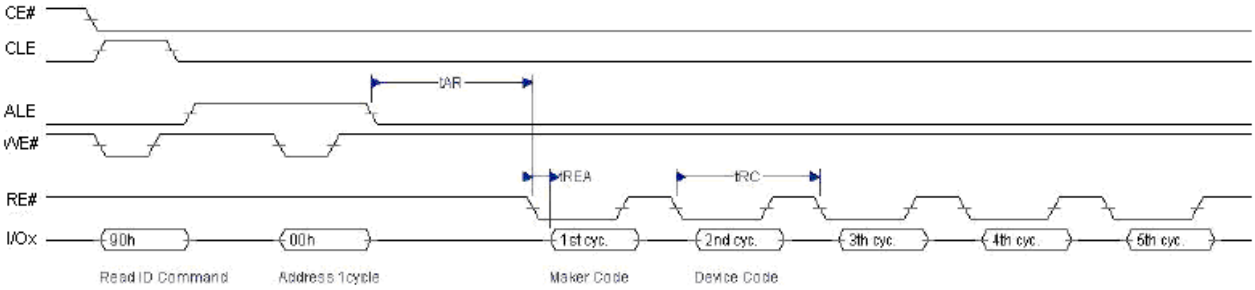
Cache Read Operation



Block Erase Operation



Read ID Operation



ID Definition Table

ID Access command = 90h

1st Cycle (Maker Code)	2nd Cycle (Device Code)	3rd Cycle	4th Cycle	5th Cycle
C8h	A1h	80h	15h	40h

	Description
1st Byte	Maker Code
2nd Byte	Device Code
3rd Byte	Internal Chip Number, Cell Type, Number of Simultaneously Programmed Pages, etc.
4th Byte	Page Size, Block Size, Redundant Area Size, Organization, Serial Access Minimum.
5th Byte	Plane Number, Plane Size

3rd ID Data

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Internal Chip Number	1 2 4 8							0 0 1 1	0 1 0 1
Cell Type	2 Level Cell 4 Level Cell 8 Level Cell 16 Level Cell					0 0 1 1	0 1 0 1		
Number of Simultaneously Programmed Page	1 2 4 8			0 0 1 1	0 1 0 1				
Interleave Program Between multiple chips	Not Support Support		0 1						
Cache Program	Not Support Support	0 1							

4th ID Data

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Page Size (w/o redundant area)	1KB 2KB 4KB 8KB							0 0 1 1	0 1 0 1
Redundant Area Size (byte/512byte)	8 16						0 1		
Block Size (w/o redundant area)	64KB 128KB 256KB 512KB			0 0 1 1	0 1 0 1				
Organization	x8 x16		0 1						
Serial Access Minimum	45ns Reserved Reserved Reserved	0 0 1 1				0 1 0 1			

5th ID Data

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
ECC Level	1 bit ECC/512Byte							0	0
	2 bit ECC/512Byte							0	1
	4 bit ECC/512Byte							1	0
	Reserved							1	1
Plane Number	1					0	0		
	2					0	1		
	4					1	0		
	8					1	1		
Plane Size (w/o redundant area)	64Mb		0	0	0				
	128Mb		0	0	1				
	256Mb		0	1	0				
	512Mb		0	1	1				
	1Gb		1	0	0				
	2Gb		1	0	1				
	4Gb		1	1	0				
	8Gb		1	1	1				
Reserved	Reserved	0							

DEVICE OPERATION

Page Read

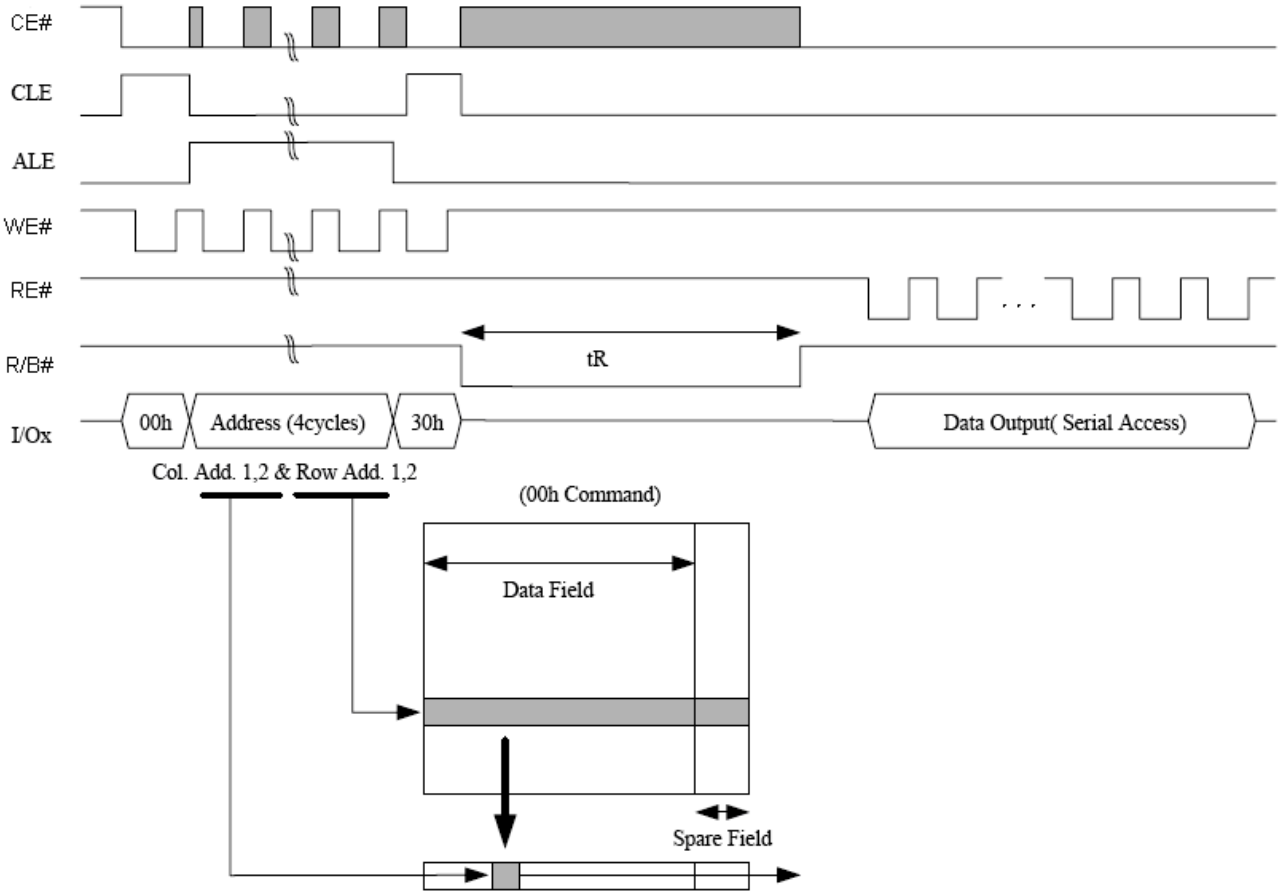
Upon initial device power up, the device defaults to Read mode. This operation is also initiated by writing 00h command, four-cycle address, and 30h command. After initial power up, the 00h command can be skipped because it has been latched in the command register. The 2,112Byte of data on a page are transferred to cache registers via data registers within 25us (t_R). Host controller can detect the completion of this data transfer by checking the R/B# output. Once data in the selected page have been loaded into cache registers, each Byte can be read out in 45ns cycle time by continuously pulsing RE#. The repetitive high-to-low transitions of RE# clock signal make the device output data starting from the designated column address to the last column address.

The device can output data at a random column address instead of sequential column address by using the Random Data Output command. Random Data Output command can be executed multiple times in a page.

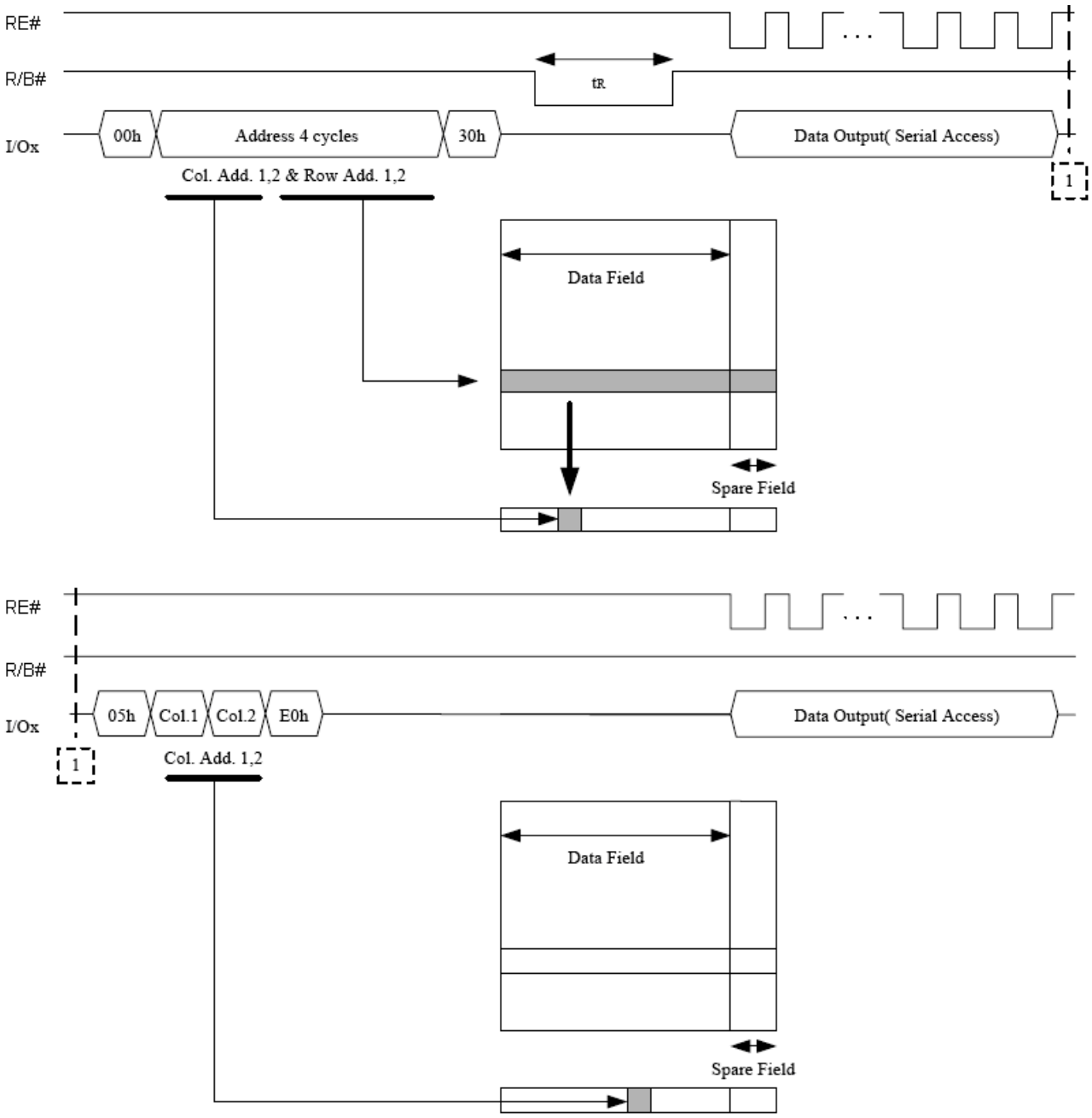
After power up, device is in read mode so 00h command cycle is not necessary to start a read operation.

A page read sequence is illustrated in under figure, where column address, page address are placed in between commands 00h and 30h. After t_R read time, the R/B# de-asserts to ready state. Read Status command (70h) can be issued right after 30h. Host controller can toggle RE# to access data starting with the designated column address and their successive bytes.

Read Operation



Random Data Output In a Page



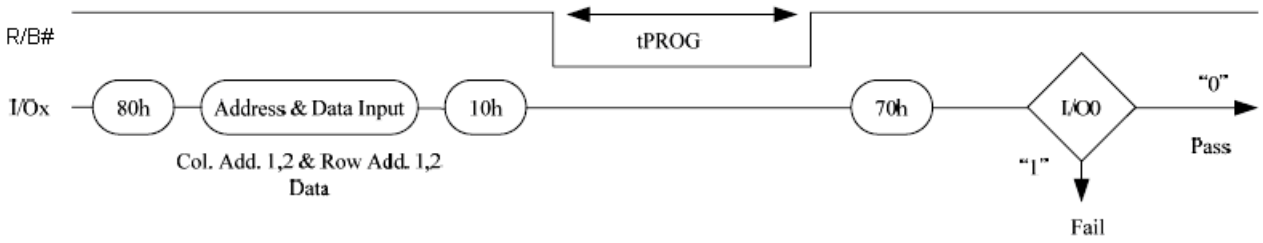
Page Program

The device is programmed based on the unit of a page, and consecutive partial page programming on one page without intervening erase operation is strictly prohibited. Addressing of page program operations within a block should be in sequential order. A complete page program cycle consists of a serial data input cycle in which up to 2,112 byte of data can be loaded into data register via cache register, followed by a programming period during which the loaded data are programmed into the designated memory cells.

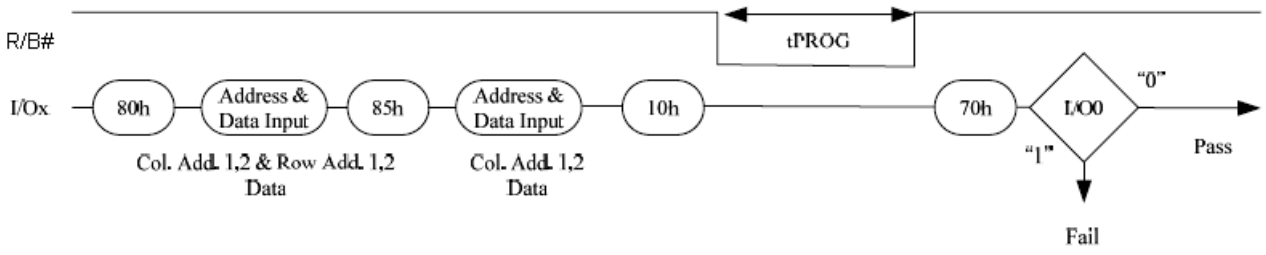
The serial data input cycle begins with the Serial Data Input command (80h), followed by a four-cycle address input and then serial data loading. The bytes not to be programmed on the page do not need to be loaded. The column address for the next data can be changed to the address follows Random Data Input command (85h). Random Data Input command may be repeated multiple times in a page. The Page Program Confirm command (10h) starts the programming process. Writing 10h alone without entering data will not initiate the programming process. The internal write engine automatically executes the corresponding algorithm and controls timing for programming and verification, thereby freeing the host controller for other tasks. Once the program process starts, the host controller can detect the completion of a program cycle by monitoring the R/B# output or reading the Status bit (I/O6) using the Read Status command. Only Read Status and Reset commands are valid during programming. When the Page Program operation is completed, the host controller can check the Status bit (I/O0) to see if the Page Program operation is successfully done. The command register remains the Read Status mode unless another valid command is written to it.

A page program sequence is illustrated in under figure, where column address, page address, and data input are placed in between 80h and 10h. After t_{PROG} program time, the R/B# de-asserts to ready state. Read Status command (70h) can be issued right after 10h.

Program & Read Status Operation



Random Data Input In a page

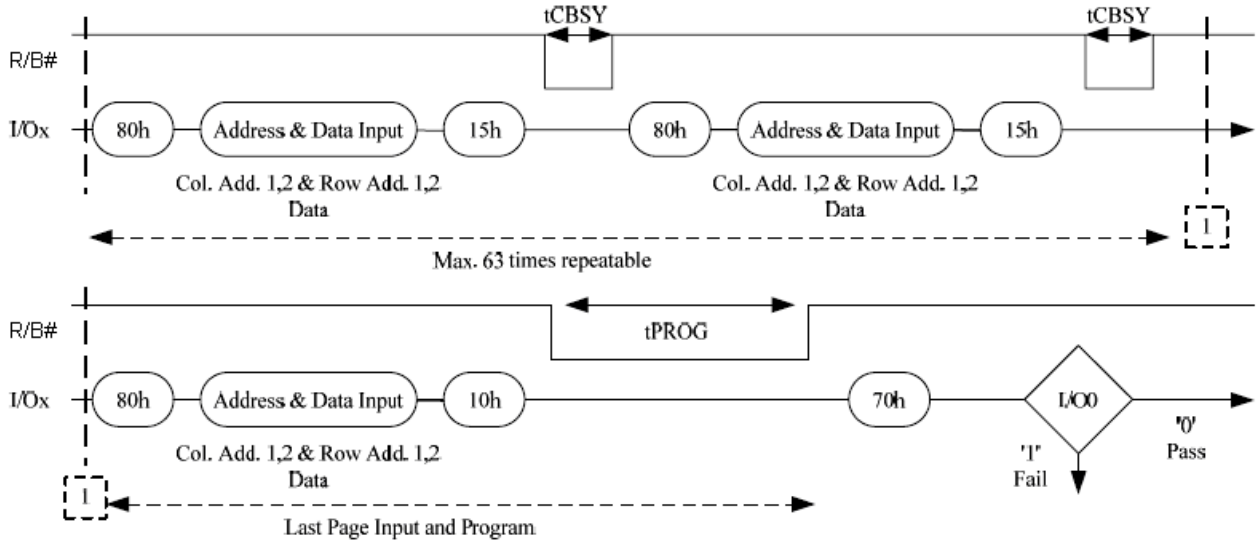


Cache Program

Cache Program is an extension of Page Program, which is executed with 2,112 byte data registers, and is available only within a block. Since the device has 1 page of cache memory, serial data input may be executed while data stored in data register are programmed into memory cell.

After writing the first set of data up to 2,112 bytes into the selected cache registers, Cache Program command (15h) instead of actual Page Program (10h) is inputted to make cache registers free and to start internal program operation. To transfer data from cache registers to data registers, the device remains in Busy state for a short period of time (t_{CBSY}) and has its cache registers ready for the next data-input while the internal programming gets started with the data loaded into data registers. Read Status command (70h) may be issued to find out when cache registers become ready by polling the Cache-Busy status bit (I/O6). Pass/fail status of only the previous page is available upon the return to Ready state. When the next set of data is inputted with the Cache Program command, t_{CBSY} is affected by the progress of pending internal programming. The programming of the cache registers is initiated only when the pending program cycle is finished and the data registers are available for the transfer of data from cache registers. The status bit (I/O5) for internal Ready/Busy may be polled to identity the completion of internal programming. If the system monitors the progress of programming only with R/B#, the last page of the target programming sequence must be programmed with actual Page Program command (10h).

Cache Program (available only within a block)



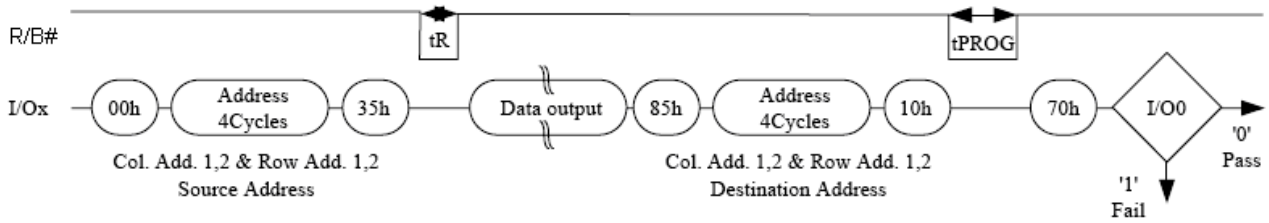
Note:

1. Since programming the last page does not employ caching, the program time has to be that of Page Program. However, if the previous program cycle with the cache data has not finished, the actual program cycle of the last page is initiated only after completion of the previous cycle, which can be expressed as the following formula.
2. t_{PROG} = Program time for the last page + Program time for the (last-1)th page – (Program command cycle time + Last page data loading time)

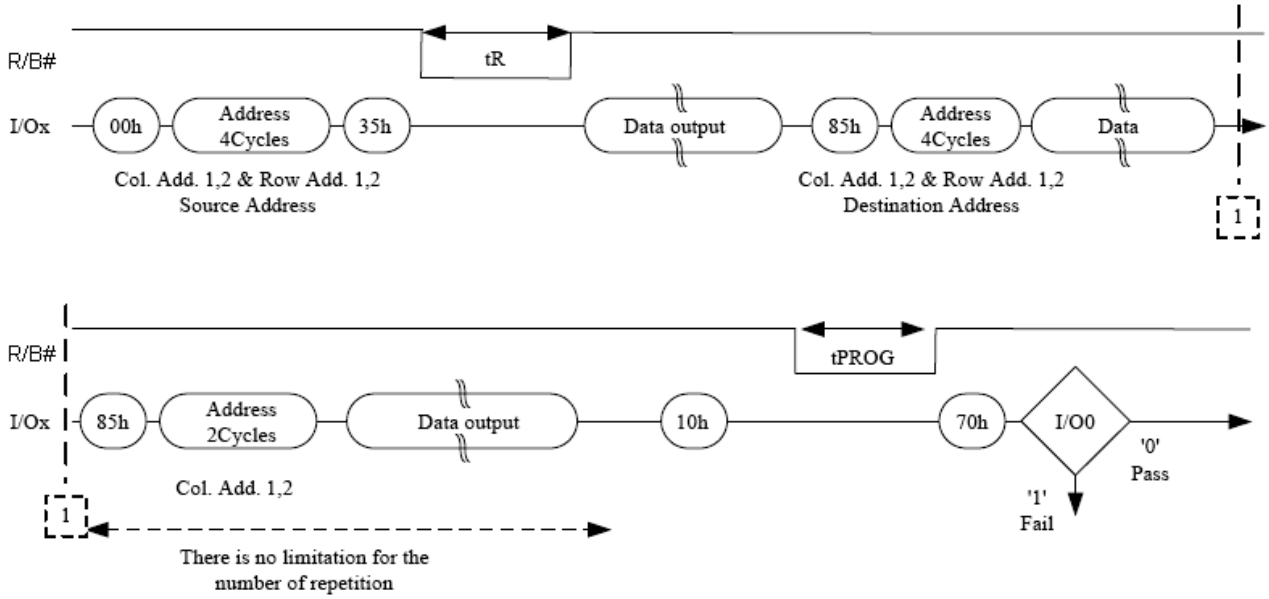
Copy-Back Program

Copy-Back Program is designed to efficiently copy data stored in memory cells without time-consuming data reloading when there is no bit error detected in the stored data. The benefit is particularly obvious when a portion of a block is updated and the rest of the block needs to be copied to a newly assigned empty block. Copy-Back operation is a sequential execution of Read for Copy-Back and of Copy-Back Program with Destination address. A Read for Copy-Back operation with “35h” command and the Source address moves the whole 2,112byte data into the internal buffer. The host controller can detect bit errors by sequentially reading the data output. Copy-Back Program is initiated by issuing Page-Copy Data-Input command (85h) with Destination address. If data modification is necessary to correct bit errors and to avoid error propagation, data can be reloaded after the Destination address. Data modification can be repeated multiple times as shown in under figure. Actual programming operation begins when Program Confirm command (10h) is issued. Once the program process starts, the Read Status command (70h) may be entered to read the status register. The host controller can detect the completion of a program cycle by monitoring the R/B# output, or the Status bit (I/O6) of the Status Register. When the Copy-Back Program is complete, the Status Bit (I/O0) may be checked. The command register remains Read Status mode until another valid command is written to it.

Page Copy-Back Program Operation



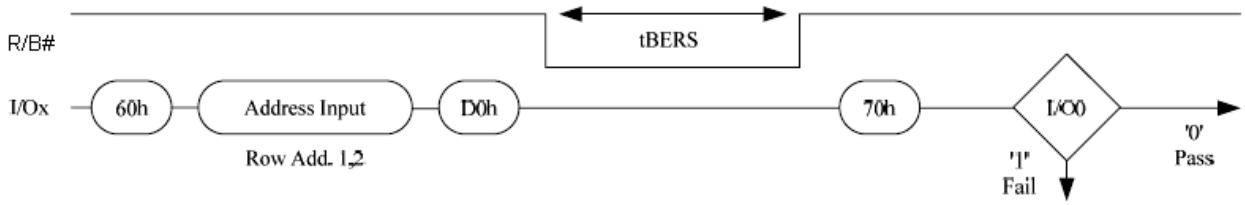
Page Copy-Back Program Operation with Random Data Input



Block Erase

The block-based Erase operation is initiated by an Erase Setup command (60h), followed by a two-cycle row address, in which only Plane address and Block address are valid while Page address is ignored. The Erase Confirm command (D0h) following the row address starts the internal erasing process. The two-step command sequence is designed to prevent memory content from being inadvertently changed by external noise. At the rising edge of WE# after the Erase Confirm command input, the internal control logic handles erase and erase-verify. When the erase operation is completed, the host controller can check Status bit (I/O0) to see if the erase operation is successfully done. The under figure illustrates a block erase sequence, and the address input (the first page address of the selected block) is placed in between commands 60h and D0h. After t_{BERASE} erase time, the R/B# de-asserts to ready state. Read Status command (70h) can be issued right after D0h to check the execution status of erase operation.

Block Erase Operation



Read Status

A status register on the device is used to check whether program or erase operation is completed and whether the operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the status register to I/O pins on the falling edge of CE# or RE#, whichever occurs last. These two commands allow the system to poll the progress of each device in multiple memory connections even when R/B# pins are common-wired. RE# or CE# does not need to toggle for status change.

The command register remains in Read Status mode unless other commands are issued to it. Therefore, if the status register is read during a random read cycle, a read command (00h) is needed to start read cycles.

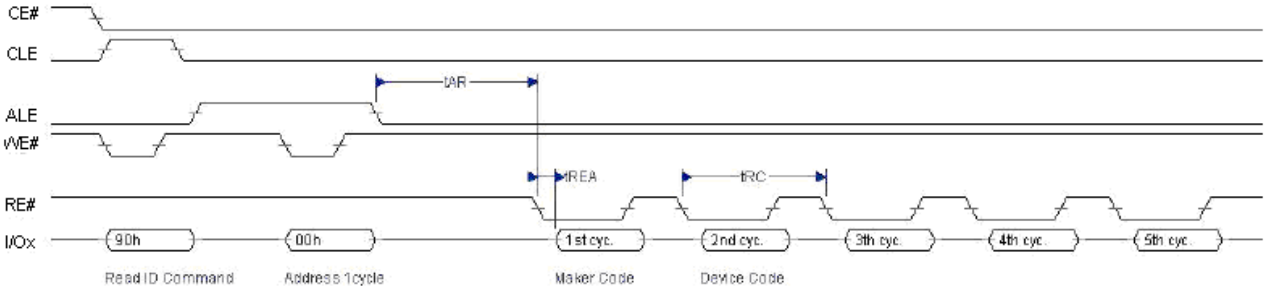
Status Register Definition for 70h Command

I/O	Page Program	Block Erase	Read	Cache Read	Definition
I/O0	Pass / Fail	Pass / Fail	NA	NA	Pass: 0 Fail: 1
I/O1	NA	NA	NA	NA	Don't cared
I/O2	NA	NA	NA	NA	Don't cared
I/O3	NA	NA	NA	NA	Don't cared
I/O4	NA	NA	NA	NA	Don't cared
I/O5	NA	NA	NA	True Ready / Busy	Busy: 0 Ready: 1
I/O6	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Busy: 0 Ready: 1
I/O7	Write Protect	Write Protect	Write Protect	Write Protect	Protected: 0 Not Protected: 1

Read ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Four read cycles sequentially output the manufacturer code (C8h), and the device code and 3rd, 4th and 5th cycle ID respectively. The command register remains in Read ID mode until further commands are issued to it.

Read ID Operation



ID Definition Table

Maker Code	Device Code	3rd Cycle	4th Cycle	5th Cycle
C8h	A1h	80h	15h	40h

RESET

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy State during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when WP# is high. If the device is already in reset state a new reset command will be accepted by the command register. The R/B# pin changes to low for t_{RST} after the Reset command is written. Refer to Figure below.

Reset Operation

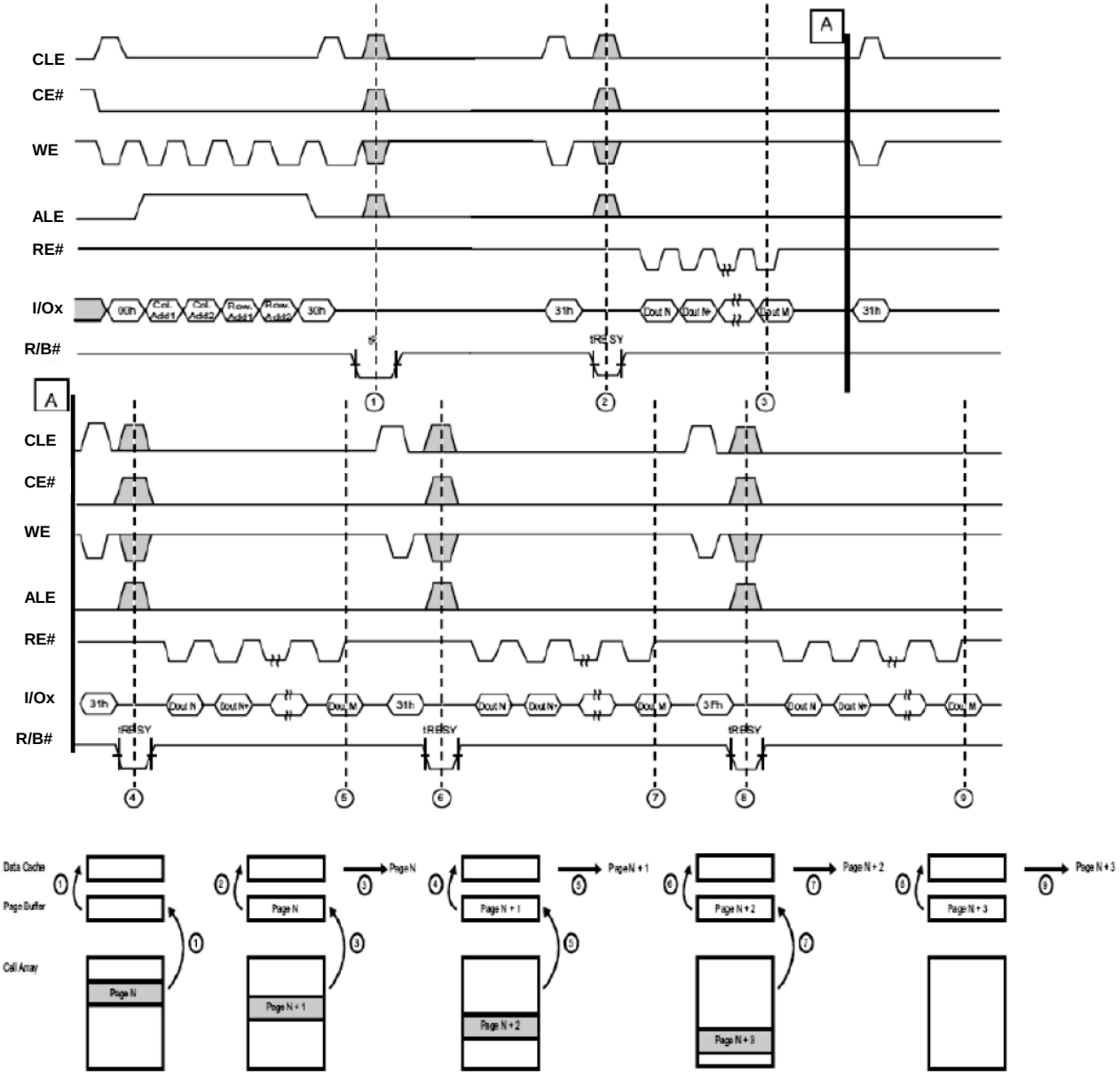
Device Status Table

	After Power-up	After Reset
Operation mode	00h Command is latched	Waiting for next command

Cache Read

Cache Read is an extension of Page Read, and is available only within a block. The normal Page Read command (00h-30h) is always issued before invoking Cache Read. After issuing the Cache Read command (31h), read data of the designated page (page N) are transferred from data registers to cache registers in a short time period of t_{DCBSYR}, and then data of the next page (page N+1) is transferred to data registers while the data in the cache registers are being read out. Host controller can retrieve continuous data and achieve fast read performance by iterating Cache Read operation. The Read Start for Last Page Cache Read command (3Fh) is used to complete data transfer from memory cells to data registers.

Read Operation with Cache Read



READY/BUSY#

The device has an R/B# output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/B# pin is normally high but transitions to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/B# outputs to be Or-tied. Because pull-up resistor value is related to tr (R/B#) and current drain during busy (ibusy), an appropriate value can be obtained with the following reference chart. Its value can be determined by the following guidance.

Ready/ Busy# Pin Electrical Specifications

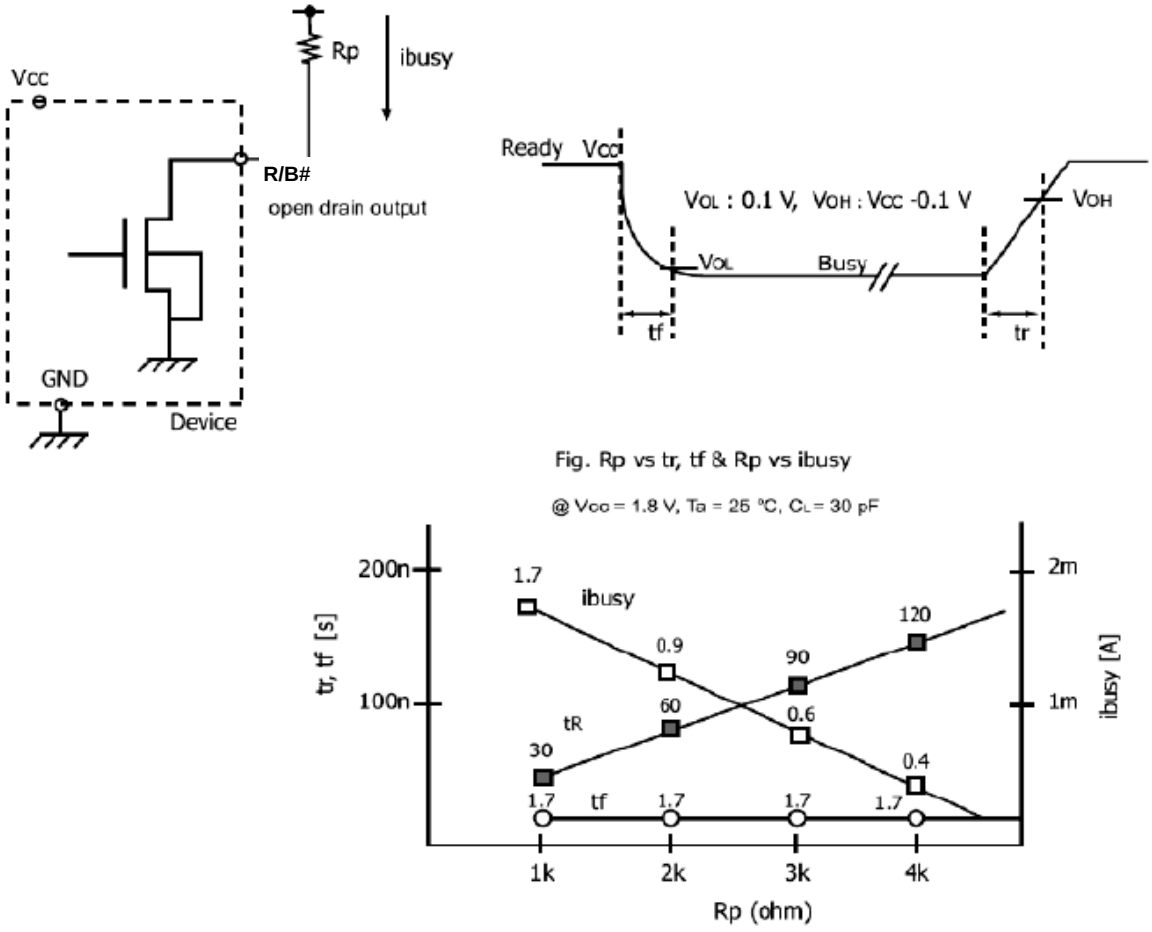


Fig. Rp vs tr, tf & Rp vs ibusy

@ Vcc = 1.8 V, Ta = 25 °C, CL = 30 pF

R_P value guidance

$$\text{Rp (min)} = \frac{V_{CC}(\text{Max.}) - V_{OL}(\text{Max.})}{I_{OL} + \Sigma I_L} = \frac{1.85V}{3\ mA + \Sigma I_L}$$

where I_L is the sum of the input currents of all devices tied to the R/ B# pin.
R_P (max) is determined by maximum permissible limit of tr

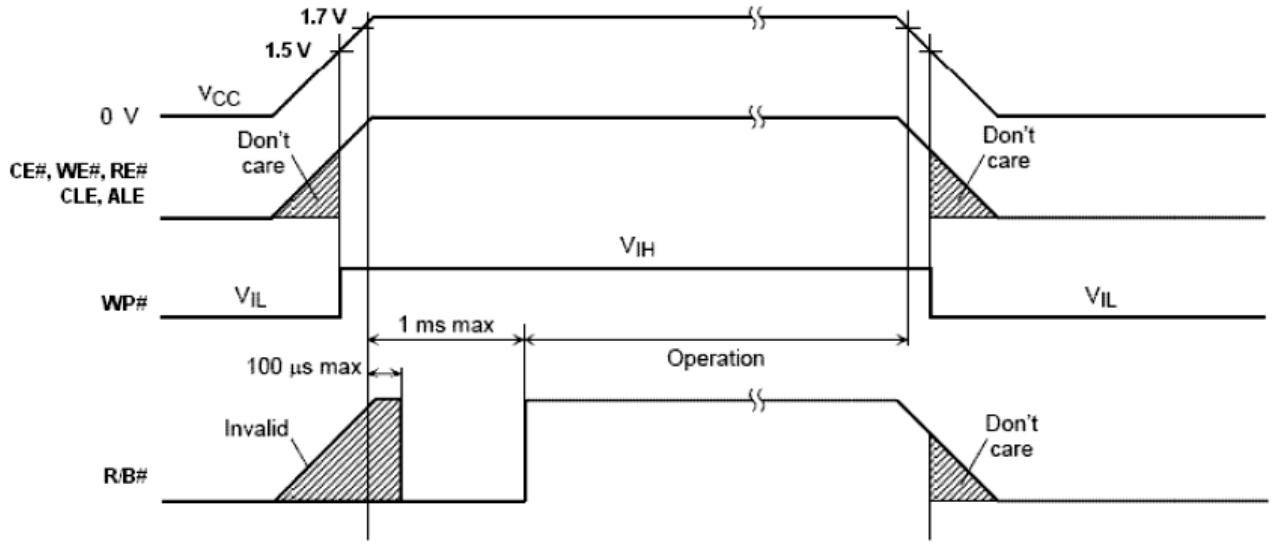
Data Protection & Power-up sequence

The timing sequence shown in the figure below is necessary for the power-on/off sequence.

The device internal initialization starts after the power supply reaches an appropriate level in the power on sequence. During the initialization the device R/B# signal indicates the Busy state as shown in the figure below. In this time period, the acceptable commands are 70h.

The WP# signal is useful for protecting against data corruption at power on/off.

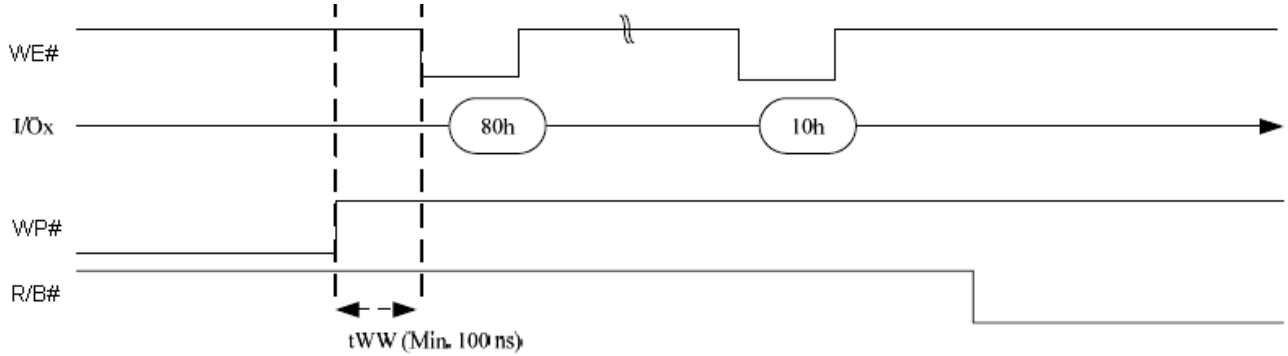
AC Waveforms for Power Transition



Write Protect Operation

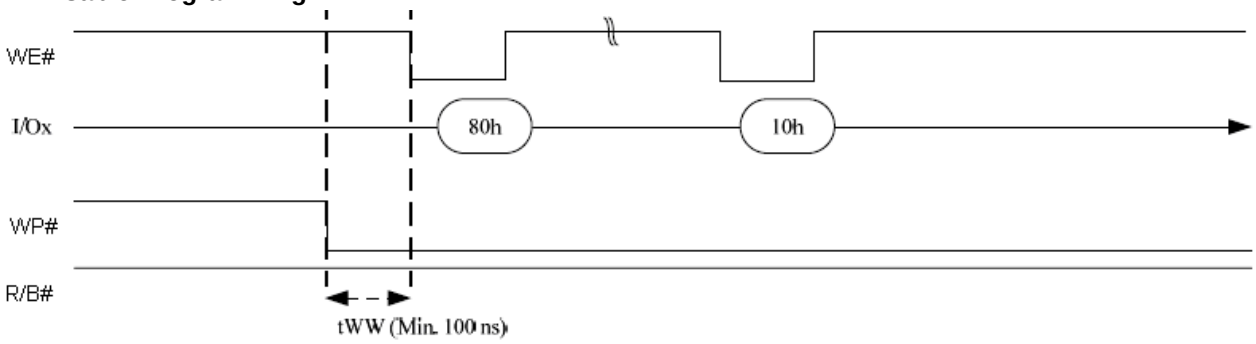
Enabling WP# during erase and program busy is prohibited. The erase and program operations are enabled and disabled as follows:

Enable Programming:

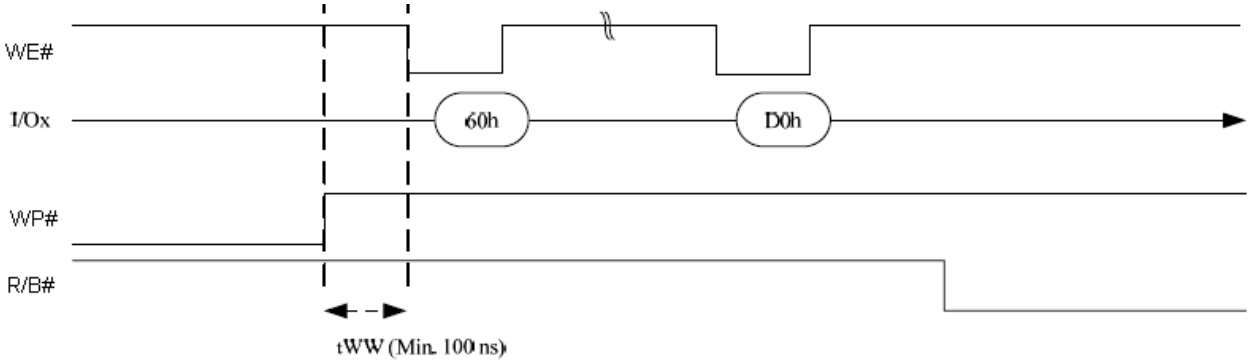


NOTE: WP# keeps "High" until programming finish.

Disable Programming:

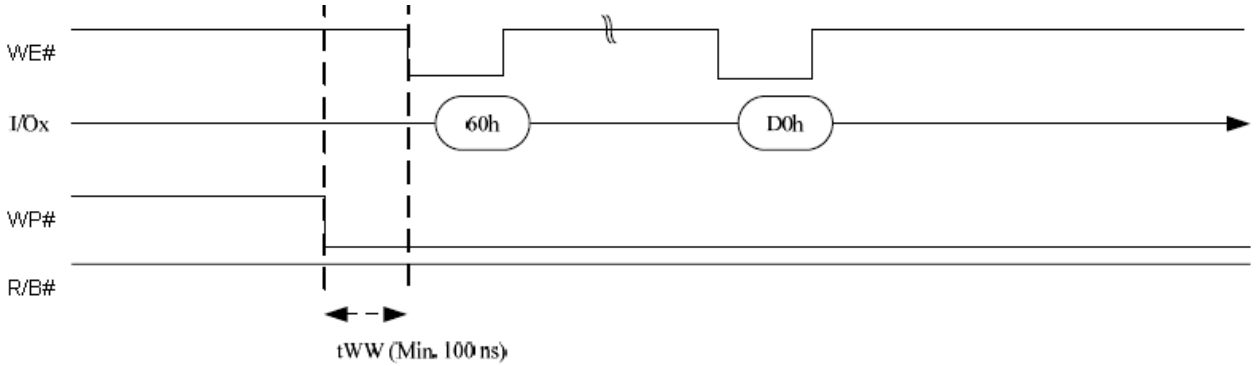


Enable Erasing:



NOTE: WP keeps “High” until erasing finish.

Disable Erasing:



One-Time Programmable (OTP) Operations

This flash device offers one-time programmable memory area. Thirty full pages of OTP data are available on the device, and the entire range is guaranteed to be good. The OTP area is accessible only through the OTP commands.

The OTP area leaves the factory in an unwritten state. The OTP area cannot be erased, whether it is protected or not. Protecting the OTP area prevents further programming of that area.

The OTP area is only accessible while in OTP operation mode. To set the device to OTP operation mode, issue the Set Feature (EFh-90h-01h) command. When the device is in OTP operation mode, subsequent Read and/or Page Program are applied to the OTP area. When you want to come back to normal operation, you need to use EFh-90h-00h for OTP mode release. Otherwise, device will stay in OTP mode.

To program an OTP page, issue the Serial Data Input (80h) command followed by 4 address cycles. The first two address cycles are column address. For the third cycle, select a page in the range of 00h through 1Dh. The fourth cycle is fixed at 00h. Next, up to 2,112 bytes of data can be loaded into data register. The bytes other than those to be programmed do not need to be loaded. This device supports Random Data Input (85h) command, which can be operated multiple times in a page. The column address for the next data to be entered may be changed to the address follows the Random Data Input command. The Page Program confirm (10h) command initiates the programming process. The internal control logic automatically executes the programming algorithm, timing and verification. Please note that no partial-page program is allowed in the OTP area. In addition, the OTP pages must be programmed in the ascending order. A programmed OTP page will be automatically protected.

Similarly, to read data from an OTP page, set the device to OTP operation mode and then issue the Read (00h-30h) command. The device may output random data (not in sequential order) in a page by writing Random Data Output (05h-E0h) command, which can be operated multiple times in a page. The column address for the next data to be output may be changed to the address follows the Random Data Output command.

All pages in the OTP area will be protected simultaneously by issuing the Set Feature (EFh-90h-03h) command to set the device to OTP protection mode. After the OTP area is protected, no page in the area is programmable and the whole area cannot be unprotected.

The Read Status (70h) command is the only valid command for reading status in OTP operation mode.

OTP Modes and Commands

	Set feature		Command
OTP Operation mode	Read	EFh-90h-01h	00h-30h
	Page Program	EFh-90h-01h	80h-10h
OTP Protection mode	Program Protect	EFh-90h-03h	80h-10h
OTP Release mode	Leave OTP mode	EFh-90h-00h	

OTP Area Details

Description	Value
Number of OTP pages	30
OTP page address	01h – 1Eh
Number of partial page programs for each page in the OTP area	1

Mobile DDR SDRAM Memory Operations

Absolute Maximum Rating

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 2.7	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	-0.5 ~ 2.7	V
Voltage on V_{DDQ} supply relative to V_{SS}	V_{DDQ}	-0.5 ~ 2.7	V
Operating ambient temperature	T_A	-30 ~ +85	°C
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1.0	W
Short circuit current	I_{OS}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommend operation condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC Operation Condition & Specifications

DC Operation Condition

Recommended operating conditions (Voltage reference to V_{SS} = 0V)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	V_{DD}	1.7	1.95	V	
I/O Supply voltage	V_{DDQ}	1.7	1.95	V	
Input logic high voltage (for Address and Command)	V_{IH} (DC)	0.8 x VDDQ	VDDQ + 0.3	V	
Input logic low voltage (for Address and Command)	V_{IL} (DC)	-0.3	0.2 x VDDQ	V	
Input logic high voltage (for DQ, DM, DQS)	V_{IHD} (DC)	0.7 x VDDQ	VDDQ + 0.3	V	
Input logic low voltage (for DQ, DM, DQS)	V_{ILD} (DC)	-0.3	0.3 x VDDQ	V	
Output logic high voltage	V_{OH} (DC)	0.9 x VDDQ	-	V	IOH = -0.1mA
Output logic low voltage	V_{OL} (DC)	-	0.1 x VDDQ	V	IOL = 0.1mA
Input Voltage Level, CLK and CLK inputs	V_{IN} (DC)	-0.3	VDDQ + 0.3	V	
Input Differential Voltage, CLK and CLK inputs	V_{ID} (DC)	0.4 x VDDQ	VDDQ + 0.6	V	1
Input leakage current	I_I	-2	2	µA	
Output leakage current	I_{OZ}	-5	5	µA	

Note:
1. V_{ID} is the magnitude of the difference between the input level on CLK and the input level on CLK#.

DC Characteristics

Recommended operating condition (Voltage reference to V_{SS} = 0V)

Parameter	Symbol	Test Condition		Version -5	Unit
Operating Current (One Bank Active)	I_{DD0}	t_{RC}= t_{RC} (min); t_{CK} = t_{CK} (min); CKE = HIGH; CS# = HIGH between valid commands; address inputs are SWITCHING; data input signals are STABLE		35	mA
Precharge Standby Current in power-down mode	I_{DD2P}	All banks idle, CKE = LOW; CS# = HIGH, t_{CK} = t_{CK} (min); address & control inputs are SWITCHING; data input signals are STABLE		300	µA
	I_{DD2PS}	All banks idle, CKE = LOW; CS# = HIGH, CLK = LOW, CLK# = HIGH; address & control inputs are SWITCHING; data input signals are STABLE		300	µA
Precharge Standby Current in non power-down mode	I_{DD2N}	All banks idle, CKE = HIGH; CS# = HIGH, t_{CK} = t_{CK} (min); address & control inputs are SWITCHING; data input signals are STABLE		9	mA
	I_{DD2NS}	All banks idle, CKE = HIGH; CS# = HIGH, CLK = LOW, CLK# = HIGH; address & control inputs are SWITCHING; data input signals are STABLE		2	mA
Active Standby Current in power-down mode	I_{DD3P}	One bank active, CKE = LOW; CS# = HIGH, t_{CK} = t_{CK} (min); address & control inputs are SWITCHING; data input signals are STABLE		2	mA
	I_{DD3PS}	One bank active, CKE = LOW; CS# = HIGH, CLK = LOW, CLK# = HIGH; address & control inputs are SWITCHING; data input signals are STABLE		2	mA
Active Standby Current in non power-down mode (One Bank Active)	I_{DD3N}	One bank active, CKE = HIGH, CS# = HIGH, t_{CK} = t_{CK} (min); address & control inputs are SWITCHING; data input signals are STABLE		25	mA
	I_{DD3NS}	One bank active, CKE = HIGH; CS# = HIGH, CLK= LOW, CLK# = HIGH; address & control inputs are SWITCHING; data input signals are STABLE		2	mA
Operating Current (Burst Mode)	I_{DD4R}	One bank active; BL=4; CL=3; t_{CK} = t_{CK} (min); continuous read bursts; I_{OUT} = 0 mA; address inputs are SWITCHING; 50% data changing each burst		100	mA
	I_{DD4W}	One bank active; BL=4; t_{CK} = t_{CK} (min); continuous write bursts; I_{OUT} = 0 mA; address inputs are SWITCHING; 50% data changing each burst		100	mA
Auto Refresh Current	I_{DD5}	Burst refresh; t_{CK} = t_{CK} (min); CKE = HIGH; address inputs are SWITCHING; data input signals are STABLE	t_{RFC}= t_{RFC}(min)	60	mA
	I_{DD5A}		t_{RFC}= t_{REFI}	9	mA

Self Refresh Current	I_{DD6}	CKE = LOW, CLK = LOW, CLK# = HIGH; EMRS set to all 0's; address & control & data bus inputs are STABLE	TCSR range	45	75	°C
			Full array	280	350	µA
			1/2 array	250	300	µA
			1/4 array	230	270	µA
			1/8 array	200	250	µA
			1/16 array	180	240	µA
Deep Power Down Current	I_{DD8}	address & control & data inputs are STABLE		10		µA

Note: 1. Input slew rate is 1V/ns.
2. I_{DD} specifications are tested after the device is properly initialized.
3. Definitions for I_{DD}: LOW is defined as V IN ≤ 0.1 * V_{DDQ};
HIGH is defined as V IN ≥ 0.9 * V_{DDQ};
STABLE is defined as inputs stable at a HIGH or LOW level;
SWITCHING is defined as: - address and command: inputs changing between HIGH and LOW once per two clock cycles;
- data bus inputs: DQ changing between HIGH and LOW once per clock cycle; DM and DQS are STABLE.

AC Operation Conditions & Timing Specification

AC Operation Conditions

Parameter	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	V_{IHD}(AC)	0.8 x V_{DDQ}	V_{DDQ}+0.3	V	
Input Low (Logic 0) Voltage, DQ, DQS and DM signals	V_{ILD}(AC)	-0.3	0.2 x V_{DDQ}	V	
Input Differential Voltage, CLK and CLK# inputs	V_{ID}(AC)	0.6 x V_{DDQ}	V_{DDQ}+0.6	V	1
Input Crossing Point Voltage, CLK and CLK# inputs	V_{IX}(AC)	0.4 x V_{DDQ}	0.6 x V_{DDQ}	V	2

Note: 1. V_{ID} is the magnitude of the difference between the input level on CLK and the input on CLK#.
2. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same.

Input / Output Capacitance

(V_{DD} = 1.8V, V_{DDQ} =1.8V, TA = 25 °C, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0~ A12, BA0~BA1, CKE, CS , RAS , CAS , WED)	C_{IN1}	2	5	pF
Input capacitance (CLK, CLK#)	C_{IN2}	4	7	pF
Data & DQS input/output capacitance	C_{OUT}	2	7	pF
Input capacitance (DM)	C_{IN3}	2	6	pF

AC Operating Test Conditions (V_{DD} = 1.7V~ 1.95V)

Parameter	Value	Unit
Input signal minimum slew rate	1.0	V/ns
Input levels (V_{IH}/V_{IL})	0.8 x V_{DDQ} / 0.2 x V_{DDQ}	V
Input timing measurement reference level	0.5 x V_{DDQ}	V
Output timing measurement reference level	0.5 x V_{DDQ}	V

AC Timing Parameter & Specifications
(V_{DD} = 1.7V~1.95V, V_{DDQ}=1.7V~1.95V)

Parameter	Symbol	-5		Unit	Note
		min	max		
Clock Period	t_{CK}	5	100	ns	12
Access time from CLK/ CLK#	t_{AC}	2	5	ns	
CLK high-level width	t_{CH}	0.45	0.55	t_{CK}	
CLK low-level width	t_{CL}	0.45	0.55	t_{CK}	
Data strobe edge to clock edge	t_{DQSCK}	2	5	ns	
Clock to first rising edge of DQS delay	t_{DQSS}	0.75	1.25	t_{CK}	
Data-in and DM setup time (to DQS) (fast slew rate)	t_{DS}	0.48		ns	13,14, 15
Data-in and DM hold time (to DQS) (fast slew rate)	t_{DH}	0.48		ns	13,14, 15
Data-in and DM setup time (to DQS) (slow slew rate)	t_{DS}	0.58		ns	13,14, 16
Data-in and DM hold time (to DQS) (slow slew rate)	t_{DH}	0.58		ns	13,14, 16
DQ and DM input pulse width (for each input)	t_{DIPW}	1.8		ns	17
Input setup time (fast slew rate)	t_{IS}	0.9		ns	15,18
Input hold time (fast slew rate)	t_{IH}	0.9		ns	15,18
Input setup time (slow slew rate)	t_{IS}	1.1		ns	16,18
Input hold time (slow slew rate)	t_{IH}	1.1		ns	16,18
Control and Address input pulse width	t_{IPW}	2.3		ns	17
DQS input high pulse width	t_{DQSH}	0.4		t_{CK}	
DQS input low pulse width	t_{DQSL}	0.4		t_{CK}	
DQS falling edge to CLK rising-setup time	t_{DSS}	0.2		t_{CK}	
DQS falling edge from CLK rising-hold time	t_{DSH}	0.2		t_{CK}	

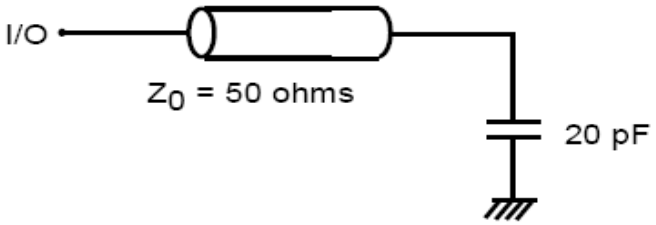
AC Timing Parameter & Specifications-continued

Parameter	Symbol	-5		Unit	Note
		min	max		
Data strobe edge to output data edge	t_{DQSQ}		0.4	ns	20
Data-out high-impedance window from CLK/ CLK#	t_{HZ}		5	ns	19
Data-out low-impedance window from CLK/ CLK#	t_{LZ}	1		ns	19
Half Clock Period	t_{HP}	t_{CL}min or t_{CH}min		ns	10,11
DQ-DQS output hold time	t_{QH}	t_{HP} - t_{QHS}		ns	11
Data hold skew factor	t_{QHS}		0.5	ns	11
ACTIVE to PRECHARGE command	t_{RAS}	40	70K	ns	
Row Cycle Time	t_{RC}	55		ns	
AUTO REFRESH Row Cycle Time	t_{RFC}	72		ns	
ACTIVE to READ,WRITE delay	t_{RCD}	15		ns	
PRECHARGE command period	t_{RP}	15		ns	
Minimum t_{CKE} High/Low time	t_{CKE}	1		t_{CK}	
ACTIVE bank A to ACTIVE bank B command	t_{RRD}	10		ns	
WRITE recovery time	t_{WR}	15		ns	
Write data in to READ command delay	t_{WTR}	2		t_{CK}	
Col. Address to Col. Address delay	t_{CCD}	1		t_{CK}	
Refresh period	t_{REF}		64	ms	
Average periodic refresh interval	t_{REFI}		7.8	μs	9
Write preamble	t_{WPRE}	0.25		t_{CK}	
Write postamble	t_{WPST}	0.4	0.6	t_{CK}	22
DQS read preamble	t_{RPRE}	0.9	1.1	t_{CK}	23
DQS read postamble	t_{RPST}	0.4	0.6	t_{CK}	
Clock to DQS write preamble setup time	t_{WPRES}	0		ns	21
Load Mode Register / Extended Mode register cycle time	t_{MRD}	2		t_{CK}	
Exit self refresh to first valid command	t_{XSR}	80		ns	24
Exit power-down mode to first valid command	t_{XP}	25		ns	25
Auto precharge write recovery + Precharge time	t_{DAL}	(t_{WR}/t_{CK}) + (t_{RP}/t_{CK})		ns	26

Notes:
1. All voltages referenced to V_{SS}.
2. All parameters assume proper device initialization.

3. Tests for AC timing may be conducted at nominal supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage and temperature range specified.
4. The circuit shown below represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to system environment. Manufacturers will correlate to their production test conditions (generally a coaxial transmission line terminated at the tester electronics). For the half strength driver with a nominal 10 pF load parameters tAC and tQH are expected to be in the same range. However, these parameters are not subject to production test but are estimated by design / characterization. Use of IBIS or other simulation tools for system design validation is suggested.

Timing Reference Load



5. The CLK/ CLK# input reference voltage level (for timing referenced to CLK/ CLK#) is the point at which CLK and CLK# cross; the input reference voltage level for signals other than CLK/ CLK# is $V_{DDQ}/2$.
6. The timing reference voltage level is $V_{DDQ}/2$.
7. AC and DC input and output voltage levels are defined in AC/DC operation conditions.
8. A CLK/ CLK# differential slew rate of 2.0 V/ns is assumed for all parameters.
9. A maximum of eight consecutive AUTO REFRESH commands (with t_{RFC}(min)) can be posted to any given Mobile DDR, meaning that the maximum absolute interval between any AUTO REFRESH command and the next AUTO REFRESH command is 8 x t_{REFI}.
10. Refer to the smaller of the actual clock low time and the actual clock high time as provided to the device.
11. $t_{QH} = t_{HP} - t_{QHS}$, where t_{HP} = minimum half clock period for any given cycle and is defined by clock high or clock low (t_{CL}, t_{CH}). t_{QHS} accounts for 1) the pulse duration distortion of on-chip clock circuits; and 2) the worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.
12. The only time that the clock frequency is allowed to change is during power-down or self-refresh modes.
13. The transition time for DQ, DM and DQS inputs is measured between V_{IL}(DC) to V_{IH}(AC) for rising input signals, and V_{IH}(DC) to V_{IL}(AC) for falling input signals.
14. DQS, DM and DQ input slew rate is specified to prevent double clocking of data and preserve setup and hold times. Signal transitions through the DC region must be monotonic.
15. Input slew rate ≥ 1.0 V/ns.
16. Input slew rate ≥ 0.5 V/ns and < 1.0 V/ns
17. These parameters guarantee device timing but they are not necessarily tested on each device.
18. The transition time for address and command inputs is measured between V_{IH} and V_{IL}.
19. t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).
20. t_{DQSQ} consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers for any given cycle.
21. The specific requirement is that DQS be valid (HIGH, LOW, or some point on a valid transition) on or before the corresponding CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on t_{DQSS}.

22. The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
23. A low level on DQS may be maintained during High-Z states (DQS drivers disabled) by adding a weak pull-down element in the system. It is recommended to turn off the weak pull-down element during read and write bursts (DQS drivers enabled).
24. There must be at least two clock pulses during the t_{XSR} period.
25. There must be at least one clock pulse during the t_{XP} period.
26. Minimum 3 clocks of t_{DAL} (= t_{WR} + t_{RP}) is required because it need minimum 2 clocks for t_{WR} and minimum 1 clock for t_{RP}. t_{DAL} = (t_{WR}/t_{CK}) + (t_{RP}/t_{CK}): for each of the terms above, if not already an integer, round to the next higher integer.

Command Truth Table

COMMAND			CKE n-1	CKEn	CS#	RAS#	CAS#	WE_D#	DM	BA0,1	A10/AP	A12~A11, A9~A0	Note
Register	Extended MRS		H	X	L	L	L	L	X	OP CODE			1,2
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1,2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A0~A8)	4
	Auto Precharge Enable										H		4
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	V	V	L	Column Address (A0~A8)	4,8
	Auto Precharge Enable										H		4,6,8
Deep Power Down Mode		Entry	H	L	L	H	H	L	X	X			
		Exit	L	H	H	X	X	X	X				
					L	H	H	H					
Burst Terminate			H	X	L	H	H	L	X	X			7
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		5
Active Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	H	H	H					
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	H	H	H					
Deselect (NOP)			H	X	H	X	X	X	X	X			
No Operation (NOP)					L	H	H	H					

(V = Valid, X = Don't Care, H = Logic High, L = Logic Low)

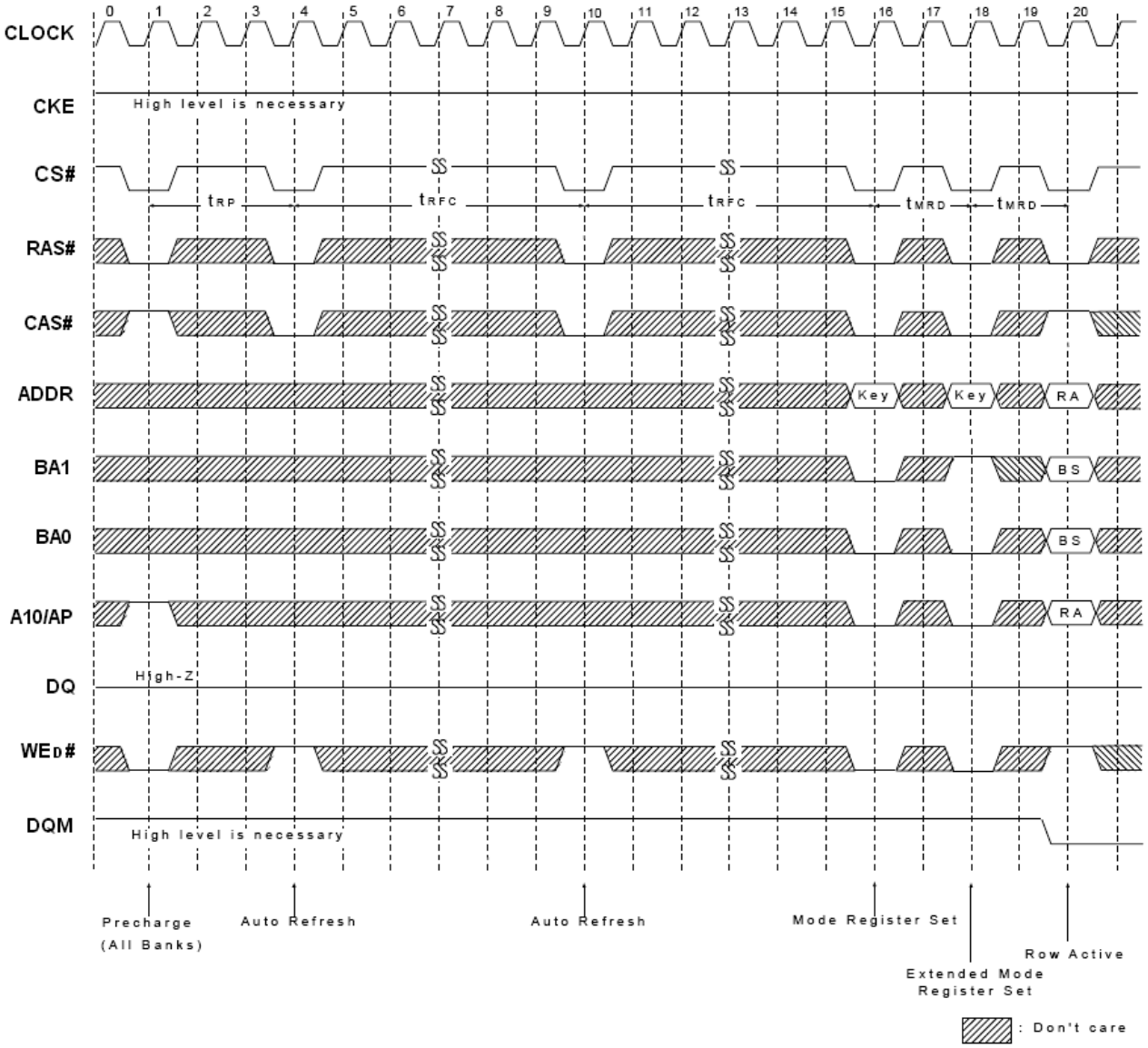
Notes:
1. OP Code: Operand Code. A0~ A12 & BA0~BA1: Program keys. (@EMRS/MRS)
2. EMRS/MRS can be issued only at all banks precharge state.
   A new command can be issued 2 clock cycles after EMRS or MRS.
3. Auto refresh functions are same as the CBR refresh of DRAM.
   The automatical precharge without row precharge command is meant by “Auto”.
   Auto/self refresh can be issued only at all banks precharge state.
4. BA0~BA1: Bank select addresses.
   If both BA0 and BA1 are “Low” at read, write, row active and precharge, bank A is selected.
   If BA0 is “High” and BA1 is “Low” at read, write, row active and precharge, bank B is selected.
   If BA0 is “Low” and BA1 is “High” at read, write, row active and precharge, bank C is selected.
   If both BA0 and BA1 are “High” at read, write, row active and precharge, bank D is selected.
5. If A10/AP is “High” at row precharge, BA0 and BA1 are ignored and all banks are selected.
6. New row active of the associated bank can be issued at t_{RP} after end of burst.
7. Burst Terminate command is valid at every burst length.
8. DM and Data-in are sampled at the rising and falling edges of the DQS. Data-in byte are masked if the corresponding and coincident DM is “High”. (Write DM latency is 0).

Basic Functionality

Power-Up and Initialization Sequence

The following sequence is required for POWER UP and Initialization.

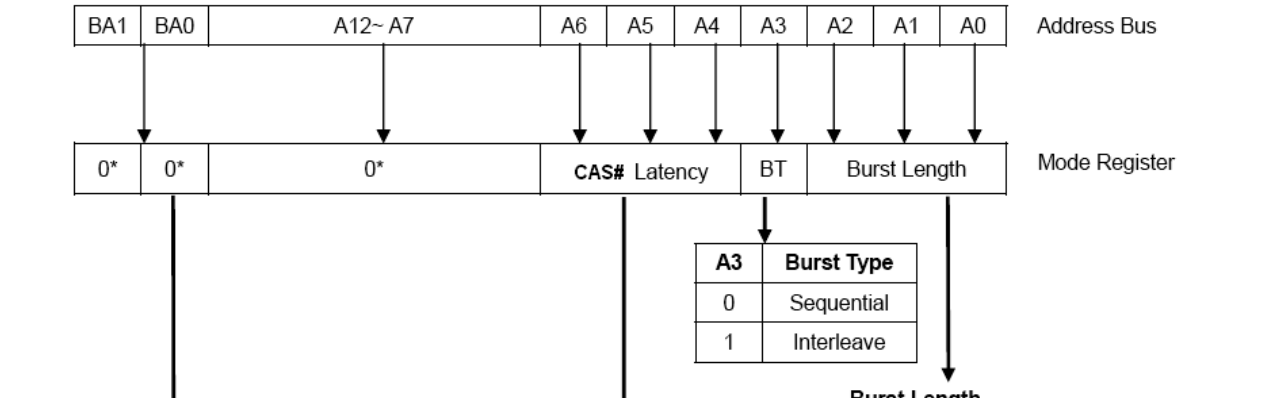
1. Apply power and attempt to maintain CKE at a high state (all other inputs may be undefined.)
   - Apply V_{DD} before or at the same time as V_{DDQ}.
2. Start clock and maintain stable condition for a minimum.
3. The minimum of 200us after stable power and clock (CLK, CLK#), apply NOP.
4. Issue precharge commands for all banks of the device.
5. Issue 2 or more auto-refresh commands.
6. Issue mode register set command to initialize the mode register.
7. Issue extended mode register set command to set PASR and DS.



Mode Register Definition

Mode Register Set (MRS)

The mode register stores the data for controlling the various operating modes of Mobile DDR SDRAM. It programs CAS# latency, addressing mode, burst length and various vendor specific options to make Mobile DDR SDRAM useful for variety of different applications. The default value of the register is not defined, therefore the mode register must be written in the power up sequence of Mobile DDR SDRAM. The mode register is written by asserting low on CS# , RAS# , CAS# , WE_D# and BA0~BA1 (The Mobile DDR SDRAM should be in all bank precharge with CKE already high prior to writing into the mode register). The state of address pins A0~A12 in the same cycle as CS#, RAS#, CAS#, WE_D# and BA0~BA1 going low is written in the mode register. Two clock cycles are requested to complete the write operation in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length uses A0~A2, addressing mode uses A3, CAS# latency (read latency from column address) uses A4~A6. A7~A12 is used for test mode. A7~A12 must be set to low for normal MRS operation. Refer to the table for specific codes for various burst length, addressing modes and CAS# latencies.



A3	Burst Type
0	Sequential
1	Interleave

BA1	BA0	Operating Mode
0	0	MRS Cycle
1	0	EMRS Cycle

CAS# Latency			
A6	A5	A4	Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Burst Length

A2	A1	A0	Length	
			Sequential	Interleave
0	0	0	Reserved	Reserved
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	16	16
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Reserved	Reserved

* BA0~BA1 and A12~A7 should stay “0” during MRS cycle

Burst Address Ordering for Burst Length

Burst Length	Starting Column Address				Sequential Mode	Interleave Mode
	A3	A2	A1	A0		
2				0	0, 1	0, 1
				1	1, 0	1, 0
4			0	0	0, 1, 2, 3	0, 1, 2, 3
			0	1	1, 2, 3, 0	1, 0, 3, 2
			1	0	2, 3, 0, 1	2, 3, 0, 1
			1	1	3, 0, 1, 2	3, 2, 1, 0
8		0	0	0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
		0	0	1	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
		0	1	0	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
		0	1	1	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
		1	0	0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
		1	0	1	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
		1	1	0	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
		1	1	1	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0
16	0	0	0	0	0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F	0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F
	0	0	0	1	1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F, 0	1, 0, 3, 2, 5, 4, 7, 6, 9, 8, B, A, D, C, F, E
	0	0	1	0	2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F, 0, 1	2, 3, 0, 1, 6, 7, 4, 5, A, B, 8, 9, E, F, C, D
	0	0	1	1	3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4, B, A, 9, 8, F, E, D, C
	0	1	0	0	4, 5, 6, 7, 8, 9, A, B, C, D, E, F, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3, C, D, E, F, 8, 9, A, B
	0	1	0	1	5, 6, 7, 8, 9, A, B, C, D, E, F, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2, D, C, F, E, 9, 8, B, A
	0	1	1	0	6, 7, 8, 9, A, B, C, D, E, F, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1, E, F, C, D, A, B, 8, 9
	0	1	1	1	7, 8, 9, A, B, C, D, E, F, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0, F, E, D, C, B, A, 9, 8
	1	0	0	0	8, 9, A, B, C, D, E, F, 0, 1, 2, 3, 4, 5, 6, 7	8, 9, A, B, C, D, E, F, 0, 1, 2, 3, 4, 5, 6, 7
	1	0	0	1	9, A, B, C, D, E, F, 0, 1, 2, 3, 4, 5, 6, 7, 8	9, 8, B, A, D, C, F, E, 1, 0, 3, 2, 5, 4, 7, 6
	1	0	1	0	A, B, C, D, E, F, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9	A, B, 8, 9, E, F, C, D, 2, 3, 0, 1, 6, 7, 4, 5
	1	0	1	1	B, C, D, E, F, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A	B, A, 9, 8, F, E, D, C, 3, 2, 1, 0, 7, 6, 5, 4
	1	1	0	0	C, D, E, F, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B	C, D, E, F, 8, 9, A, B, 4, 5, 6, 7, 0, 1, 2, 3
	1	1	0	1	D, E, F, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C	D, C, F, E, 9, 8, B, A, 5, 4, 7, 6, 1, 0, 3, 2
	1	1	1	0	E, F, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D	E, F, C, D, A, B, 8, 9, 6, 7, 4, 5, 2, 3, 0, 1
	1	1	1	1	F, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E	F, E, D, C, B, A, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0

Extended Mode Register Set (EMRS)

The extended mode register stores for selecting PASR and DS. The extended mode register set must be done before any active command after the power up sequence. The extended mode register is written by asserting low on CS# , RAS# , CAS# , WE_D# , BA0 and high on BA1 (The Mobile DDR SDRAM should be in all bank precharge with CKE already high prior to writing into the extended more register). The state of address pins A0~An in the same cycle as CS# , RAS# , CAS# , WE_D# going low is written in the extended mode register. Refer to the table for specific codes.
The extended mode register can be changed by using the same command and clock cycle requirements during operations as long as all banks are in the idle state.

Internal Temperature Compensated Self Refresh (TCSR)

1. In order to save power consumption, Mobile DDR SDRAM includes the internal temperature sensor and control units to control the self refresh cycle automatically according to the device temperature.
2. If the EMRS for external TCSR is issued by the controller, this EMRS code for TCSR is ignored.

BA1	BA0	A12 ~ A8	A7	A6	A5	A4	A3	A2	A1	A0	Address bus
1	0*	0*	DS			TCSR		PASR			Extended Mode Register Set

	A2-A0	Self Refresh Coverage
PASR	000	Full array
	001	1/2 array (BA1 = 0)
	010	1/4 array (BA1 = BA0 =0)
	011	Reserved
	100	Reserved
	101	1/8 array (BA1 = BA0 = Row Addr MSB** =0)
	110	1/16 array (BA1 = BA0 = Row Addr 2 MSB =0)
	111	Reserved

Internal TCSR

	A7-A5	Drive Strength
DS	000	Full Strength
	001	1/2 Strength
	010	1/4 Strength
	011	1/8 Strength
	100	3/4 Strength

* BA0 and A12~ A8 should stay “0” during EMRS cycle.
** MSB: most significant bit

Precharge

The precharge command is used to precharge or close a bank that has activated. The precharge command is issued when CS#, RAS# and WE_D# are low and CAS# is high at the rising edge of the clock. The precharge command can be used to precharge each bank respectively or all banks simultaneously. The bank select addresses (BA0, BA1) are used to define which bank is precharged when the command is initiated. For write cycle, t_{WR}(min.) must be satisfied until the precharge command can be issued. After t_{RP} from the precharge, an active command to the same bank can be initiated.

Burst Selection for Precharge by Bank address bits

A10/AP	BA1	BA0	Precharge
0	0	0	Bank A Only
0	0	1	Bank B Only
0	1	0	Bank C Only
0	1	1	Bank D Only
1	X	X	All Banks

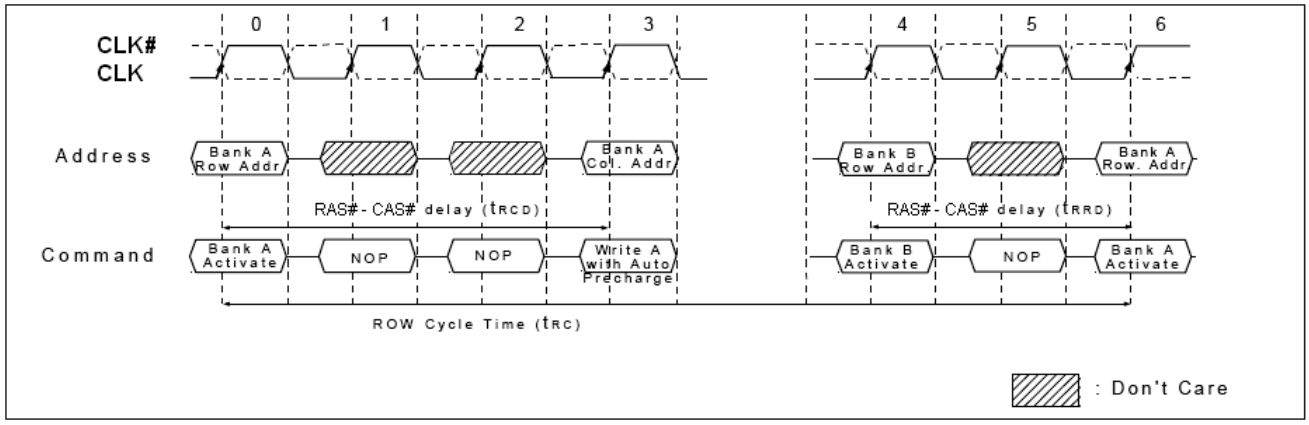
NOP & Device Deselect

The device should be deselected by deactivating the CS# signal. In this mode, Mobile DDR SDRAM should ignore all the control inputs. The Mobile DDR SDRAM is put in NOP mode when CS# is actived and by deactivating RAS#, CAS# and WE_D#. For both Deselect and NOP, the device should finish the current operation when this command is issued.

Row Active

The Bank Activation command is issued by holding CAS# and WE_D# high with CS# and RAS# low at the rising edge of the clock (CLK). The Mobile DDR SDRAM has four independent banks, so Bank Select addresses (BA0, BA1) are required. The Bank Activation command to the first read or write command must meet or exceed the minimum of RAS# to CAS# delay time (t_{RCD} min). Once a bank has been activated, it must be precharged before another Bank Activation command can be applied to the same bank. The minimum time interval between interleaved Bank Activation command (Bank A to Bank B and vice versa) is the Bank to Bank delay time (t_{RRD} min).

Bank Activation Command Cycle (CAS# Latency = 3)



Read Bank

This command is used after the row activate command to initiate the burst read of data. The read command is initiated by activating CS#, RAS#, CAS#, and deserting WE_D# at the same clock sampling (rising) edge as described in the command truth table. The length of the burst and the CAS latency time will be determined by the values programmed during the MRS command.

Write Bank

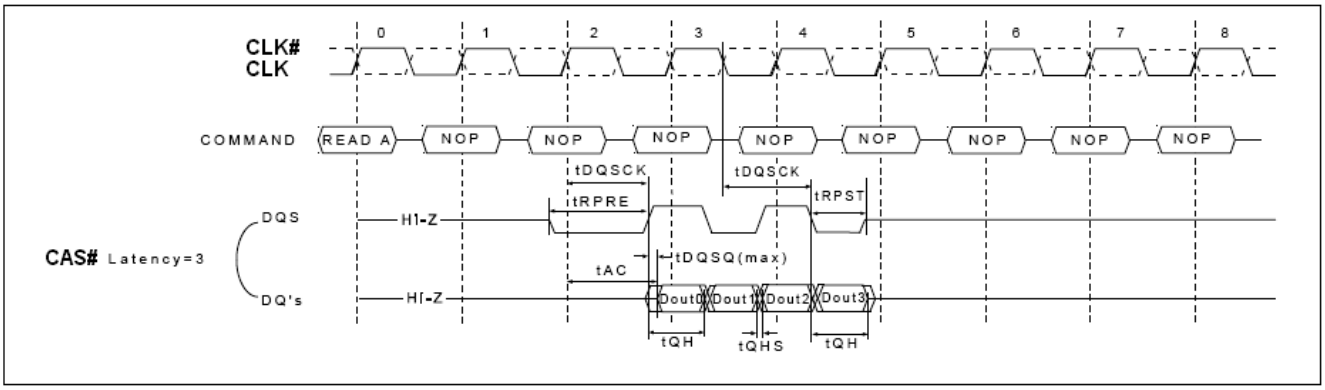
This command is used after the row activate command to initiate the burst write of data. The write command is initiated by activating CS#, RAS#, CAS#, and WE_D# at the same clock sampling (rising) edge as describe in the command truth table. The length of the burst will be determined by the values programmed during the MRS command.

Essential Functionality for Mobile DDR SDRAM

Burst Read Operation

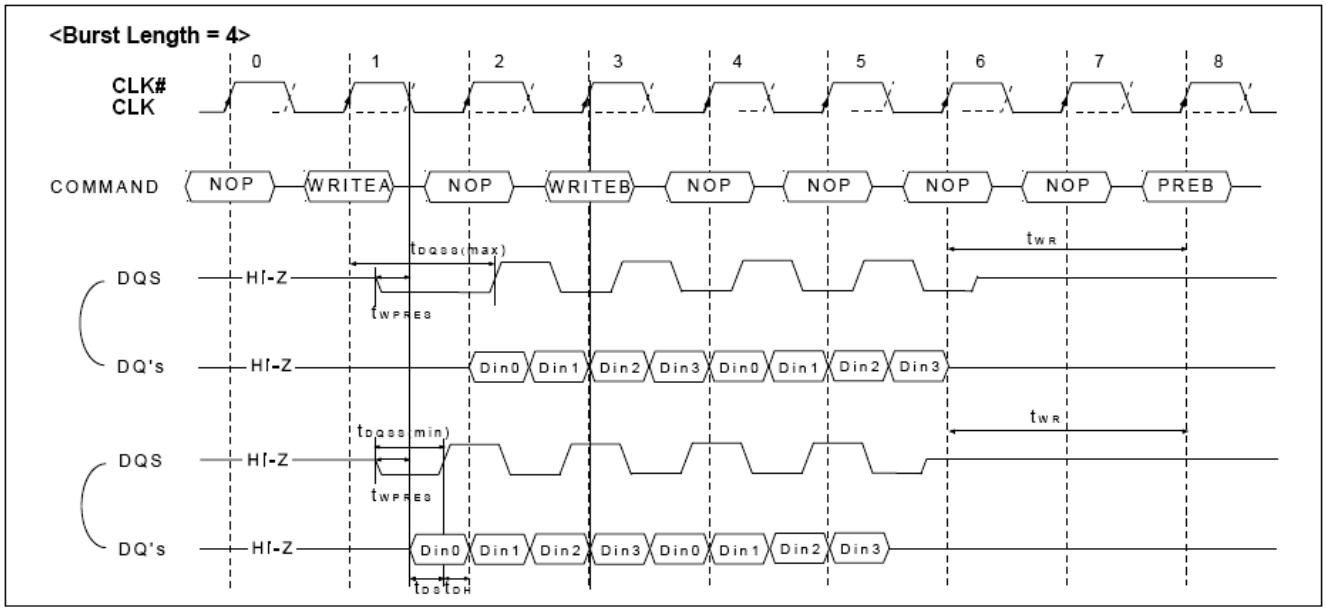
Burst Read operation in Mobile DDR SDRAM is in the same manner as the current Mobile DDR SDRAM such that the Burst read command is issued by asserting CS# and CAS# low while holding RAS# and WE_D# high at the rising edge of the clock (CLK) after t_{RCD} from the bank activation. The address inputs determine the starting address for the Burst, The Mode Register sets type of burst and burst length. The first output data is available after the CAS# Latency from the READ command, and the consecutive data are presented on the falling and rising edge of Data Strobe (DQS) adopted by Mobile DDR SDRAM until the burst length is completed.

<Burst Length = 4, CAS# Latency = 3>



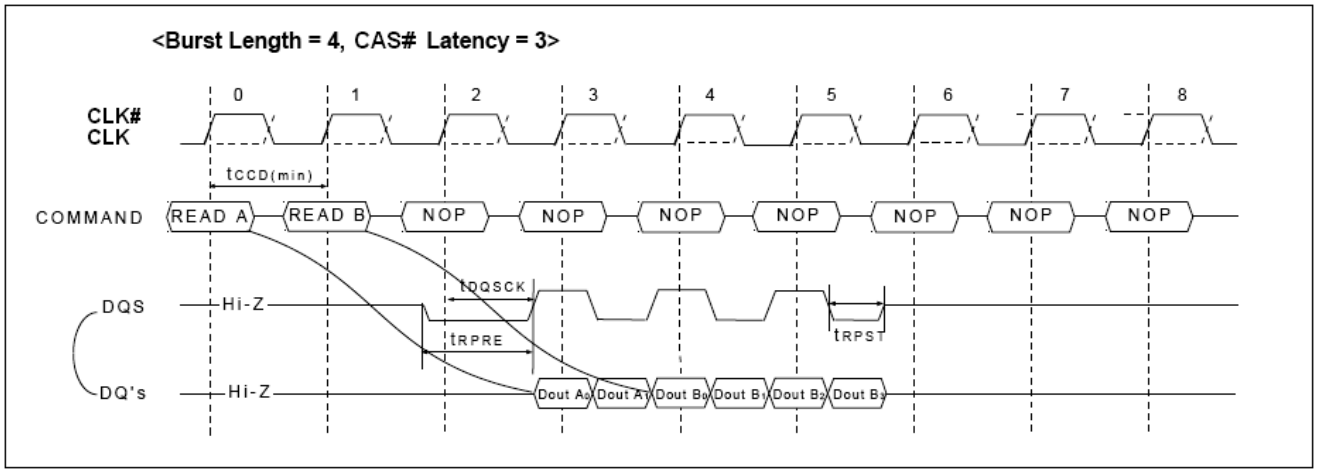
Burst Write Operation

The Burst Write command is issued by having CS#, CAS# and WE_D# low while holding RAS# high at the rising edge of the clock (CLK). The address inputs determine the starting column address. There is no write latency relative to DQS required for burst write cycle. The first data of a burst write cycle must be applied on the DQ pins tDS (Data-in setup time) prior to data strobe edge enabled after t_{DQSS} from the rising edge of the clock (CLK) that the write command is issued. The remaining data inputs must be supplied on each subsequent falling and rising edge of Data Strobe until the burst length is completed. When the burst has been finished, any additional data supplied to the DQ pins will be ignored.



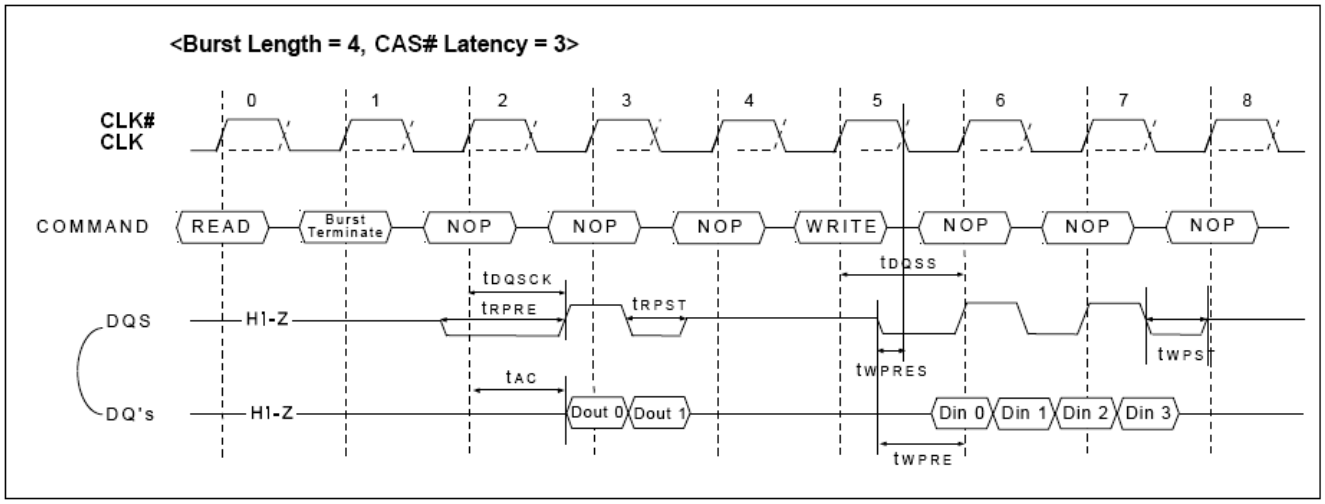
Read Interrupted by a Read

A Burst Read can be interrupted before completion of the burst by new Read command of any bank. When the previous burst is interrupted, the remaining addresses are overridden by the new address with the full burst length. The data from the first Read command continues to appear on the outputs until the CAS# latency from the interrupting Read command is satisfied. At this point the data from the interrupting Read command appears. Read to Read interval is minimum 1 clock.



Read Interrupted by a Write & Burst Terminate

To interrupt a burst read with a write command, Burst Terminate command must be asserted to avoid data contention on the I/O bus by placing the DQ's (Output drivers) in a high impedance state. To insure the DQ's are tri-stated one cycle before the beginning the write operation, Burt Terminate command must be applied at least RU(CL) clocks 〔RU means round up to the nearest integer〕 before the Write command.

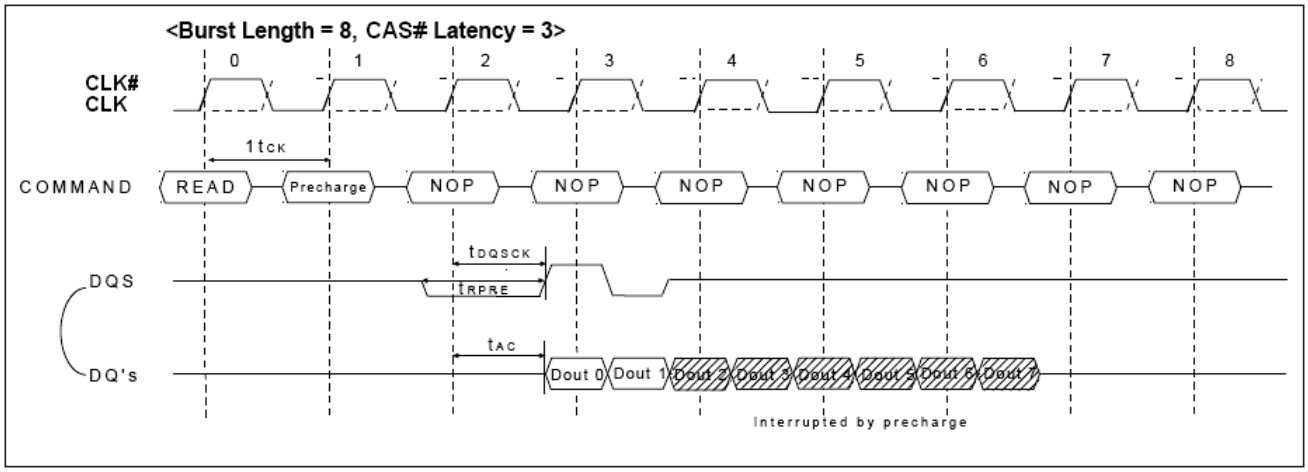


The following functionality establishes how a Write command may interrupt a Read burst.

1. For Write commands interrupting a Read burst, a Burst Terminate command is required to stop the read burst and tristate the DQ bus prior to valid input write data. Once the Burst Terminate command has been issued, the minimum delay to a Write command = RU (CL) [CL is the CAS# Latency and RU means round up to the nearest integer].
2. It is illegal for a Write and Burst Terminate command to interrupt a Read with auto precharge command.

Read Interrupted by a Precharge

A Burst Read operation can be interrupted by precharge of the same bank. The minimum 1 clock is required for the read to precharge intervals. A precharge command to output disable latency is equivalent to the CAS# latency.



When a burst Read command is issued to a Mobile DDR SDRAM, a Precharge command may be issued to the same bank before the Read burst is complete. The following functionality determines when a Precharge command may be given during a Read burst and when a new Bank Activate command may be issued to the same bank.

1. For the earliest possible Precharge command without interrupting a Read burst, the Precharge command may be given on the rising clock edge which is CL clock cycles before the end of the Read burst where CL is the CAS# Latency. A new Bank Activate command may be issued to the same bank after t_{RP} (RAS precharge time).

2. When a Precharge command interrupts a Read burst operation, the Precharge command may be given on the rising clock edge which is CL clock cycles before the last data from the interrupted Read burst where CL is the CAS# Latency. Once the last data word has been output, the output buffers are tristated. A new Bank Activate command may be issued to the same bank after t_{RP}.

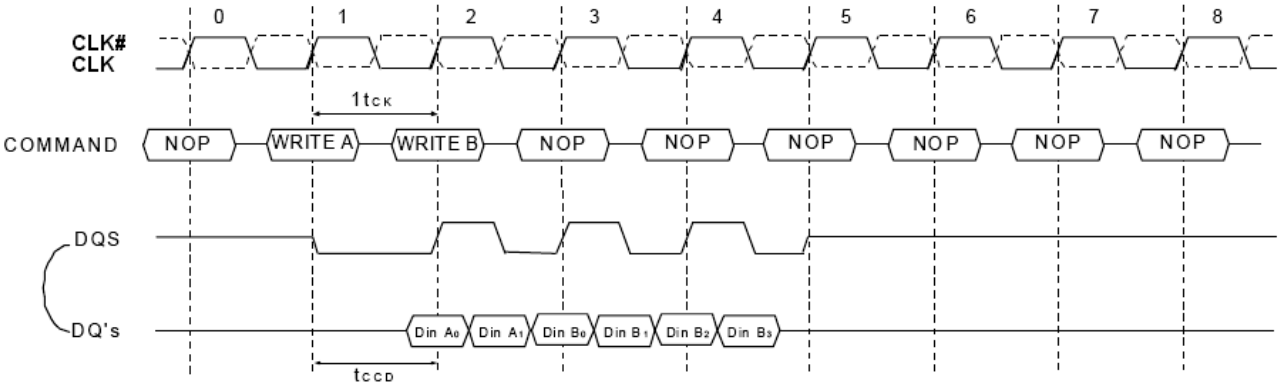
3. For a Read with auto precharge command, a new Bank Activate command may be issued to the same bank after t_{RP} where t_{RP} begins on the rising clock edge which is CL clock cycles before the end of the Read burst where CL is the CAS# Latency. During Read with auto precharge, the initiation of the internal precharge occurs at the same time as the earliest possible external Precharge command would initiate a precharge operation without interrupting the Read burst as described in 1 above.

4. For all cases above, t_{RP} is an analog delay that needs to be converted into clock cycles. The number of clock cycles between a Precharge command and a new Bank Activate command to the same bank equals t_{RP} / t_{CK} (where t_{CK} is the clock cycle time) with the result rounded up to the nearest integer number of clock cycles.
   In all cases, a Precharge operation cannot be initiated unless t_{RAS} (min) [minimum Bank Activate to Precharge time] has been satisfied. This includes Read with auto precharge commands where t_{RAS} (min) must still be satisfied such that a Read with auto precharge command has the same timing as a Read command followed by the earliest possible Precharge command which does not interrupt the burst.

Write Interrupted by a Write

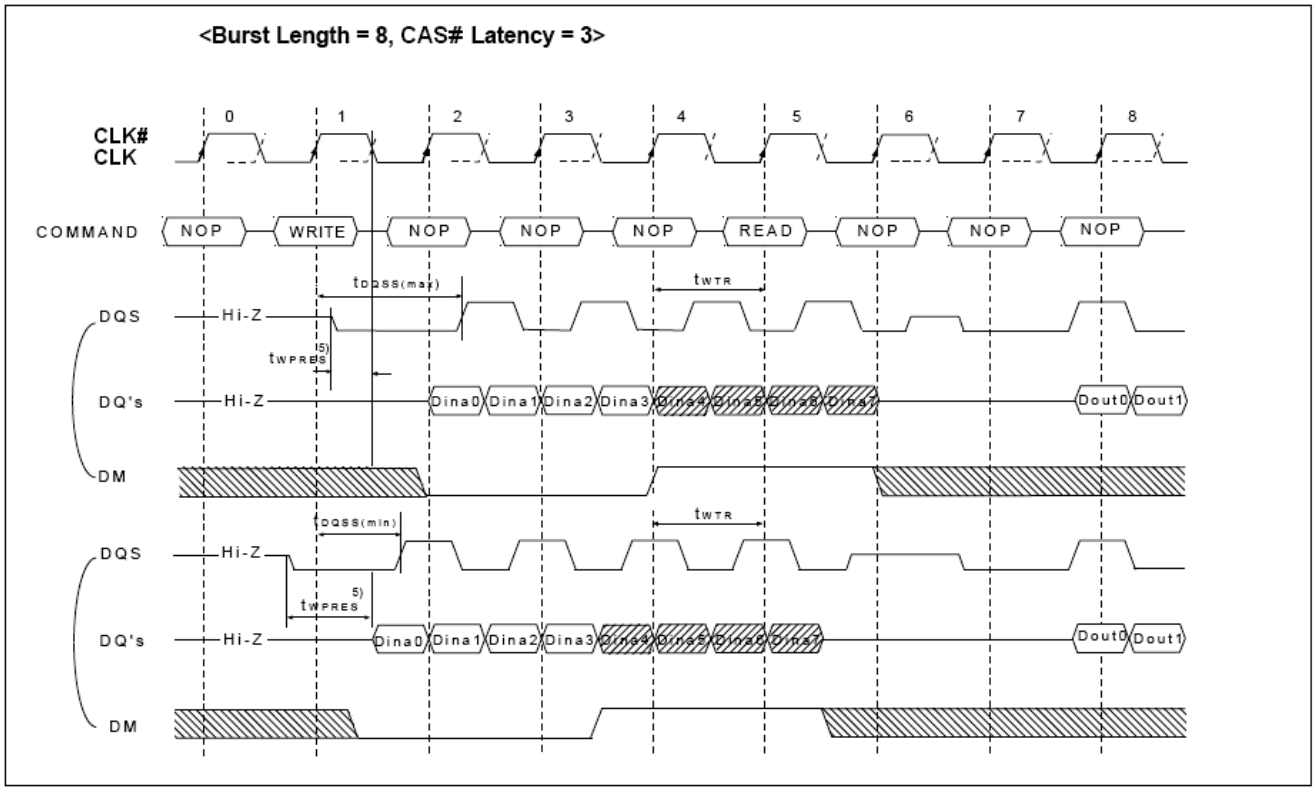
A Burst Write can be interrupted before completion of the burst by a new Write command, with the only restriction that the interval that separates the commands must be at least one clock cycle. When the previous burst is interrupted, the remaining addresses are overridden by the new address and data will be written into the device until the programmed burst length is satisfied.

<Burst Length = 4>



Write Interrupted by a Read & DM

A burst write can be interrupted by a read command of any bank. The DQ's must be in the high impedance state at least one clock cycle before the interrupting read data appear on the outputs to avoid data contention. When the read command is registered, any residual data from the burst write cycle must be masked by DM. The delay from the last data to read command (t_{WTR}) is required to avoid the data contention Mobile DDR SDRAM inside. Data that are presented on the DQ pins before the read command is initiated will actually be written to the memory. Read command interrupting write can not be issued at the next clock edge of that of write command.

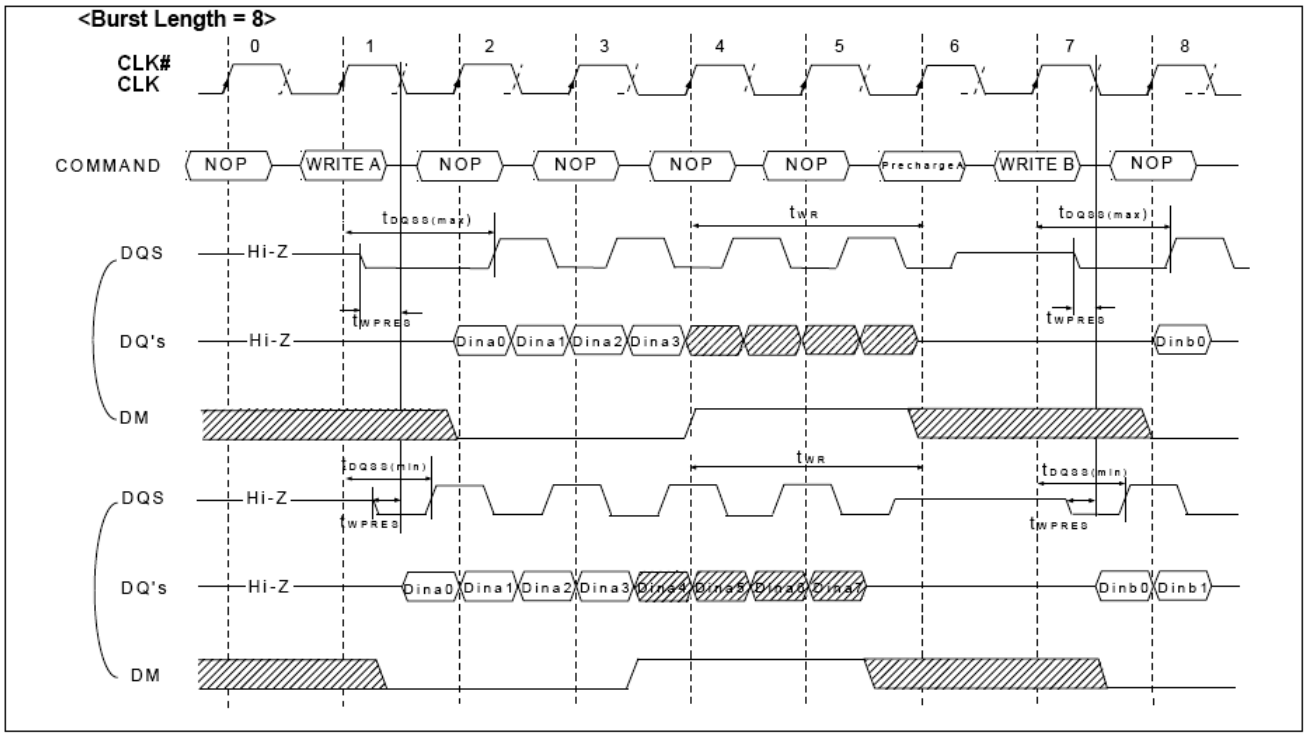


The following functionality established how a Read command may interrupt a Write burst and which input data is not written into the memory.

1. For Read commands interrupting a Write burst, the minimum Write to Read command delay is 2 clock cycles. The case where the Write to Read delay is 1 clock cycle is disallowed.
2. For read commands interrupting a Write burst, the DM pin must be used to mask the input data words which immediately precede the interrupting Read operation and the input data word which immediately follows the interrupting Read operation.
3. For all cases of a Read interrupting a Write, the DQ and DQS buses must be released by the driving chip (i.e., the memory controller) in time to allow the buses to turn around before the Mobile DDR SDRAM drives them during a read operation.
4. If input Write data is masked by the Read command, the DQS inputs are ignored by the Mobile DDR SDRAM.
5. It is illegal for a Read command interrupt a Write with auto precharge command.

Write Interrupted by a Precharge & DM

A burst write operation can be interrupted before completion of the burst by a precharge of the same bank. Random column access is allowed. A write recovery time (t_{WR}) is required from the last data to precharge command. When precharge command is asserted, any residual data from the burst write cycle must be masked by DM.



Precharge timing for Write operations in Mobile DDR SDRAM requires enough time to allow “Write recovery” which is the time required by a Mobile DDR SDRAM core to properly store a full “0” or “1” level before a Precharge operation. For Mobile DDR SDRAM, a timing parameter, t_{WR}, is used to indicate the required of time between the last valid write operation and a Precharge command to the same bank.

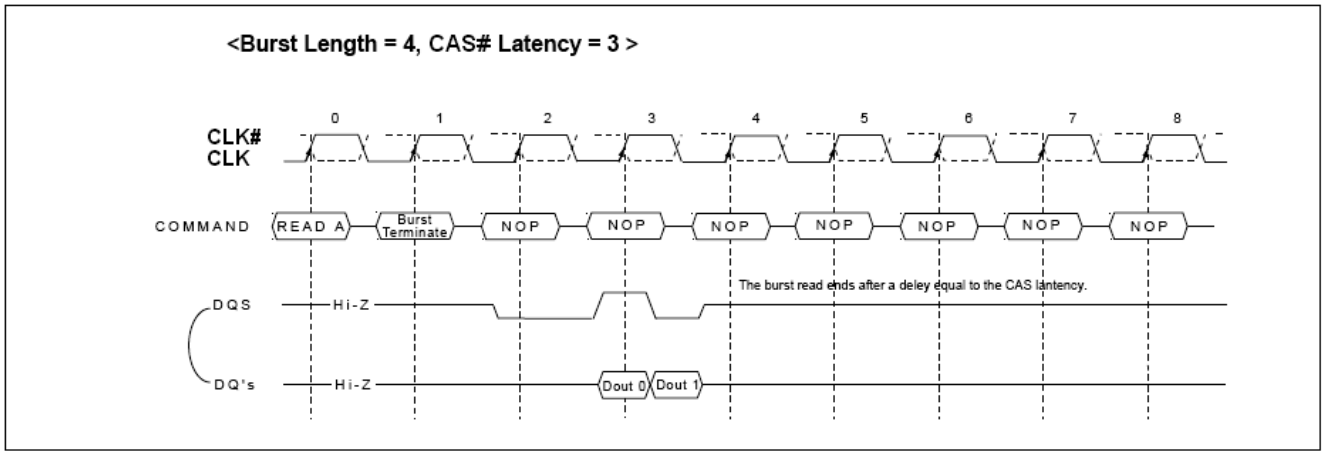
t_{WR} starts on the rising clock edge after the last possible DQS edge that strobed in the last valid and ends on the rising clock edge that strobes in the precharge command.

1. For the earliest possible Precharge command following a Write burst without interrupting the burst, the minimum time for write recovery is defined by t_{WR}.
2. When a precharge command interrupts a Write burst operation, the data mask pin, DM, is used to mask input data during the time between the last valid write data and the rising clock edge in which the Precharge command is given. During this time, the DQS input is still required to strobe in the state of DM. The minimum time for write recovery is defined by t_{WR}.
3. For a Write with auto precharge command, a new Bank Activate command may be issued to the same bank after $t_{WR} + t_{RP}$ where $t_{WR} + t_{RP}$ starts on the falling DQS edge that strobed in the last valid data and ends on the rising clock edge that strobes in the Bank Activate commands. During write with auto precharge, the initiation of the internal precharge occurs at the same time as the earliest possible external Precharge command without interrupting the Write burst as described in 1 above.
4. In all cases, a Precharge operation cannot be initiated unless t_{RAS} (min) [minimum Bank Activate to Precharge time] has been satisfied. This includes Write with auto precharge commands where t_{RAS} (min) must still be satisfied such that a Write with auto precharge command has the same timing

as a Write command followed by the earliest possible Precharge command which does not interrupt the burst.

Burst Terminate

The Burst Terminate command is initiated by having RAS# and CAS# high with CS# and WE_D# low at the rising edge of the clock (CLK). The Burst Terminate command has the fewest restriction making it the easiest method to use when terminating a burst read operation before it has been completed. When the Burst Terminate command is issued during a burst read cycle, the pair of data and DQS (Data Strobe) go to a high impedance state after a delay which is equal to the CAS latency set in the mode register. The Burst Terminate command, however, is not supported during a write burst operation.



The Burst Terminate command is a mandatory feature for Mobile DDR SDRAM. The following functionality is required.

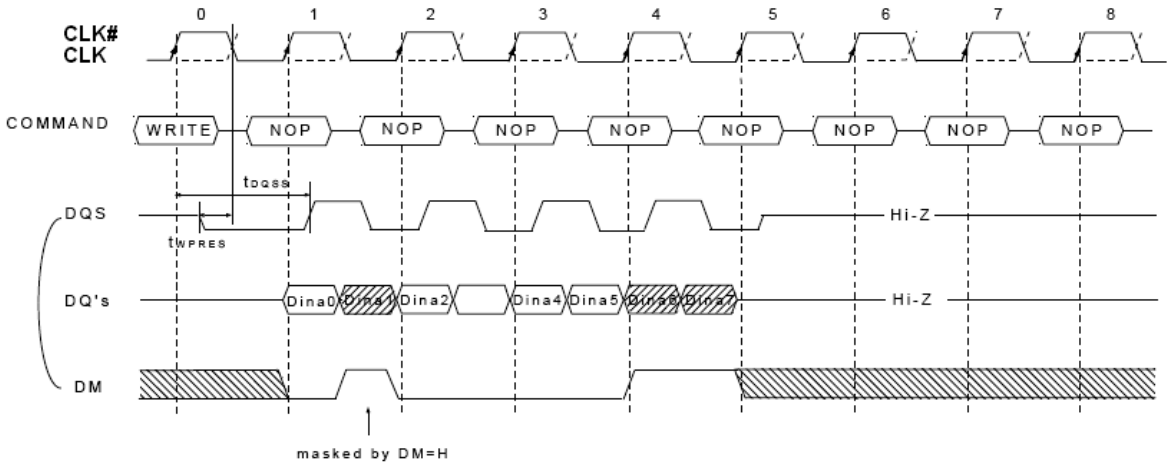
1. The BST command may only be issued on the rising edge of the input clock, CLK.
2. BST is only a valid command during Read burst.
3. BST during a Write burst is undefined and shall not be used.
4. BST applies to all burst lengths.
5. BST is an undefined command during Read with auto precharge and shall not be used.
6. When terminating a burst Read command, the BST command must be issued LBST (“BST Latency”) clock cycles before the clock edge at which the output buffers are tristated, where L_{BST} equals the CAS# latency for read operations.
7. When the burst terminates, the DQ and DQS pins are tristated.

The BST command is not byte controllable and applies to all bits in the DQ data word and the (all) DQS pin(s)

DM masking

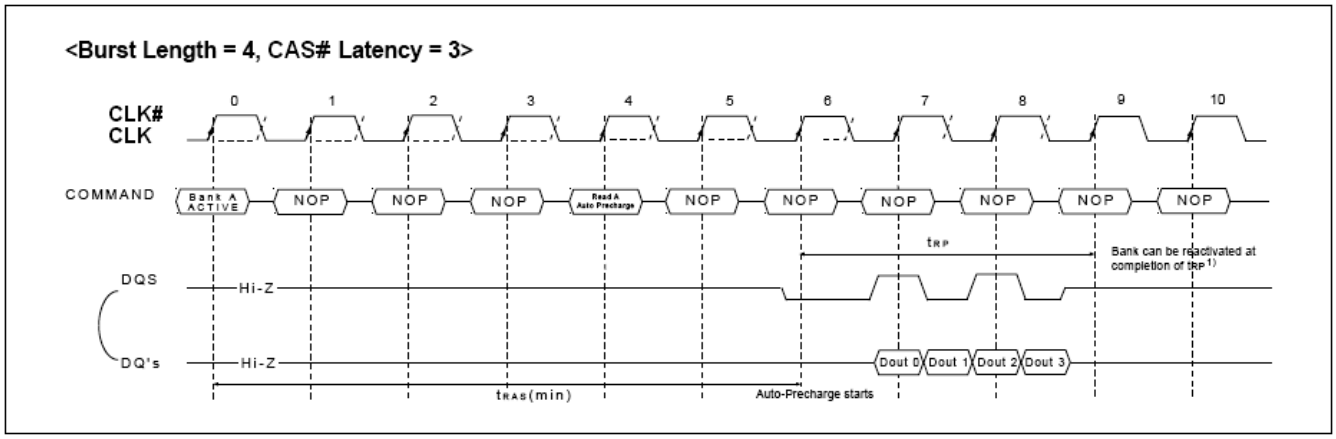
The Mobile DDR SDRAM has a data mask function that can be used in conjunction with data write cycle. Not read cycle. When the data mask is activated (DM high) during write operation, Mobile DDR SDRAM does not accept the corresponding data. (DM to data-mask latency is zero) DM must be issued at the rising or falling edge of data strobe.

<Burst Length = 8>



Read with Auto Precharge

If a read with auto precharge command is initiated, the Mobile DDR SDRAM automatically enters the precharge operation BL/2 clock later from a read with auto precharge command when t_{RAS} (min) is satisfied. If not, the start point of precharge operation will be delayed until t_{RAS} (min) is satisfied. Once the precharge operation has started the bank cannot be reactivated and the new command can not be asserted until the precharge time (t_{RP}) has been satisfied



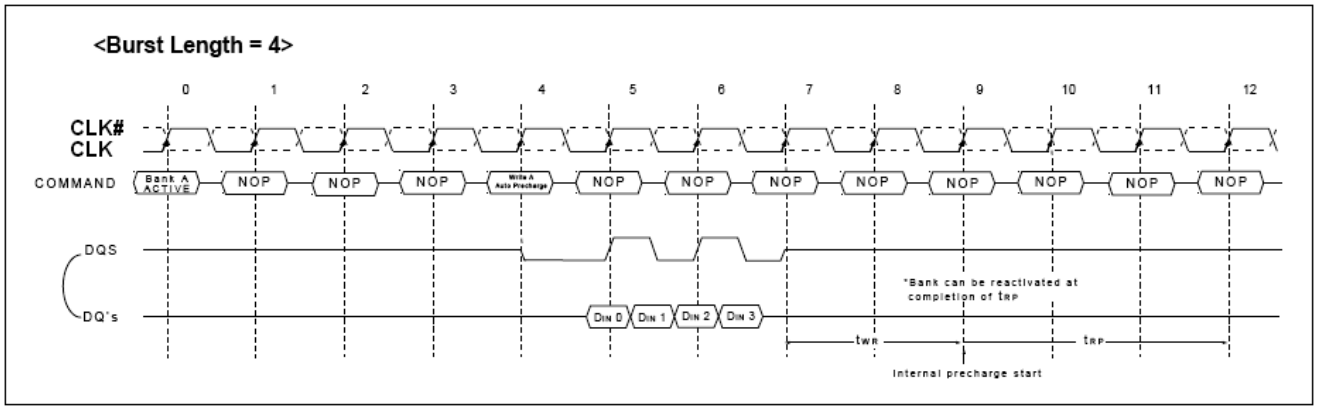
Note: The row active command of the precharge bank can be issued after tRP from this point.

Asserted Command	For Same Bank			For Different Bank		
	5	6	7	5	6	7
READ	READ + No AP	Illegal	Illegal	Legal	Legal	Legal
READ + AP1	READ + AP	Illegal	Illegal	Legal	Legal	Legal
Active	Illegal	Illegal	Illegal	Legal	Legal	Legal
Precharge	Legal	Legal	Illegal	Legal	Legal	Legal

Note: 1. AP = Auto Precharge

Write with Auto Precharge

If A10 is high when write command is issued, the write with auto precharge function is performed. Any new command to the same bank should not be issued until the internal precharge is completed. The internal precharge begins at the rising edge of the CLK with the t_{WR} delay after the last data-in.



Note: The row active command of the precharge bank can be issued after t_{RP} from this point.

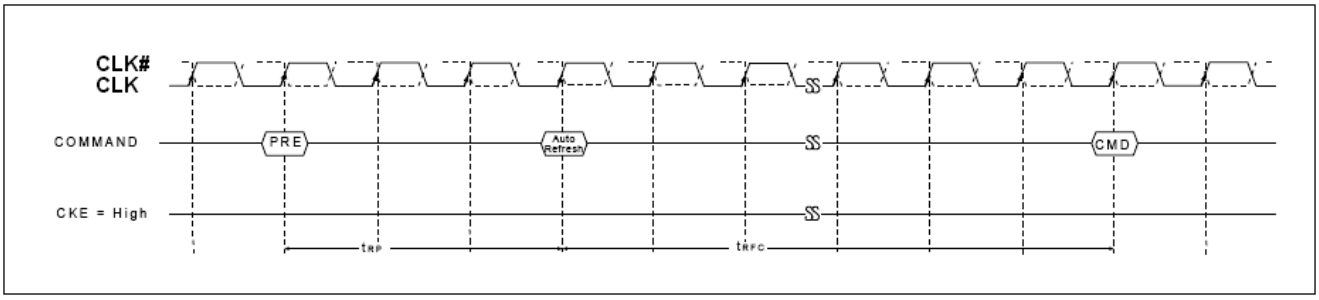
Asserted Command	For Same Bank						For Different Bank				
	5	6	7	8	9	10	5	6	7	8	9
WRITE	WRITE + NO AP	WRITE + NO AP	Illegal	Illegal	Illegal	Illegal	Legal	Legal	Legal	Legal	Legal
WRITE + AP[1]	WRITE + AP	WRITE + AP	Illegal	Illegal	Illegal	Illegal	Legal	Legal	Legal	Legal	Legal
READ	Illegal	READ + No AP + DM[2]	READ + No AP+ DM	READ + No AP	Illegal	Illegal	Illegal	Illegal	Illegal	Legal	Legal
READ + AP	Illegal	READ + AP+ DM	READ + AP+ DM	READ + AP	Illegal	Illegal	Illegal	Illegal	Illegal	Legal	Legal
Active	Illegal	Illegal	Illegal	Illegal	Illegal	Illegal	Legal	Legal	Legal	Legal	Legal
Precharge	Illegal	Illegal	Illegal	Illegal	Illegal	Illegal	Legal	Legal	Legal	Legal	Legal

Note: 1. AP = Auto Precharge
2. DM: Refer to “Write Interrupted by Precharge & DM”

Auto Refresh & Self Refresh

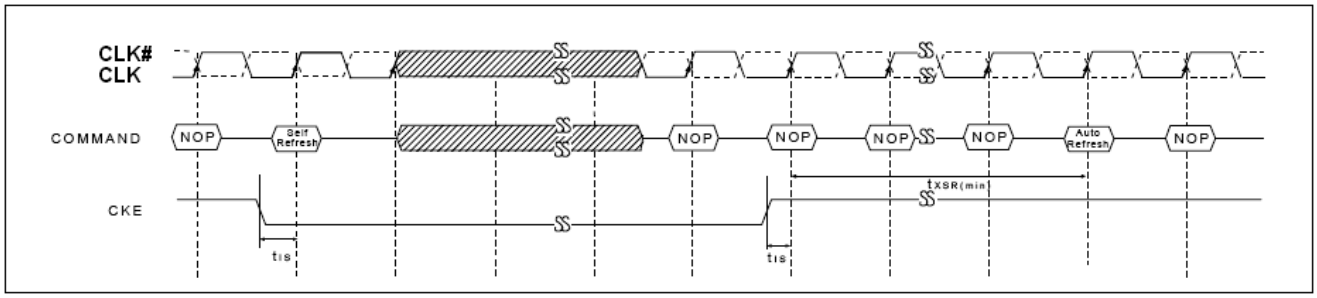
Auto Refresh

An auto refresh command is issued by having CS#, RAS# and CAS# held low with CKE and WE_D# high at the rising edge of the clock (CLK). All banks must be precharged and idle for t_{RP} (min) before the auto refresh command is applied. No control of the external address pins is requires once this cycle has started because of the internal address counter. When the refresh cycle has completed, all banks will be in the idle state. A delay between the auto refresh command and the next activate command or subsequent auto refresh command must be greater than or equal to the t_{RFC} (min). A maximum of eight consecutive AUTO REFRESH commands (with t_{RFC} (min)) can be posted to any given Mobile DDR, meaning that the maximum absolute interval between any AUTO REFRESH command and the next AUTO REFRESH command is 8 x t_{REFI}.



Self Refresh

A self refresh command is defines by having CS#, RAS#, CAS# and CKE held low with WE_D# high at the rising edge of the clock (CLK). Once the self refresh command is initiated, CKE must be held low to keep the device in self refresh mode. During the self refresh operation, all inputs except CKE are ignored. The clock is internally disabled during self refresh operation to reduce power consumption. The self refresh is exited by supplying stable clock input before returning CKE high, asserting deselect or NOP command and then asserting CKE high for longer than t_{XSR}.



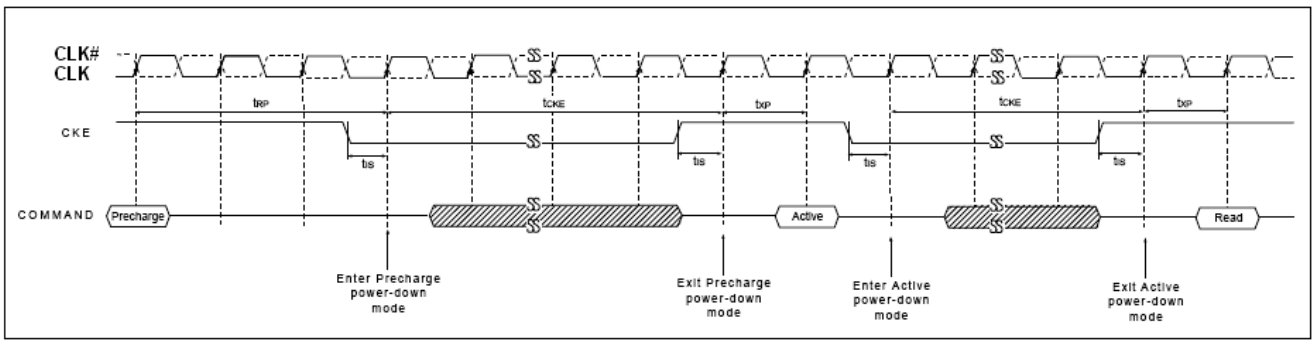
Note: After self refresh exit, input an auto refresh command immediately.

Power Down

Power down is entered when CKE is registered Low (no accesses can be in progress). If power down occurs when all banks are idle, this mode is referred to as precharge power-down; if power down occurs when there is a row active in any bank, this mode is referred to as active power-down.

Entering power down deactivates the input and output buffers, excluding CLK, CLK# and CKE. In power down mode, CKE Low must be maintained, and all other input signals are “Don’t Care”. The minimum power down duration is specified by t_{CKE}. However, power down duration is limited by the refresh requirements of the device.

The power down state is synchronously exited when CKE is registered High (along with a NOP or DESELECT command). A valid command may be applied t_{XP} after exit from power down.



Functional Truth Table

Truth Table – CKE [Note 1~10]

CKE n-1	CKE n	Current State	COMMAND n	ACTION n	NOTE
L	L	Power Down	X	Maintain Power Down	
L	L	Self Refresh	X	Maintain Self Refresh	
L	L	Deep Power Down	X	Maintain Deep Power Down	
L	H	Power Down	NOP or DESELECT	Exit Power Down	5,6,9
L	H	Self Refresh	NOP or DESELECT	Exit Self Refresh	5,7,10
L	H	Deep Power Down	NOP or DESELECT	Exit Deep Power Down	5,8
H	L	All Banks Idle	NOP or DESELECT	Precharge Power Down Entry	5
H	L	Bank(s) Active	NOP or DESELECT	Active Power Down Entry	5
H	L	All Banks Idle	AUTO REFRESH	Self Refresh Entry	
H	L	All Banks Idle	BURST TERMINATE	Enter Deep Power Down	
H	H	See the other Truth Tables			

Notes:
1. CKE n is the logic state of CKE at clock edge n; CKE n-1 was the state of CKE at the previous clock edge.
2. Current state is the state of Mobile DDR immediately prior to clock edge n.
3. COMMAND n is the command registered at clock edge n, and ACTION n is the result of COMMAND n.
4. All states and sequences not shown are illegal or reserved.
5. DESELECT and NOP are functionally interchangeable.
6. Power Down exit time (t_{XP}) should elapse before a command other than NOP or DESELECT is issued.
7. SELF REFRESH exit time (t_{XSR}) should elapse before a command other than NOP or DESELECT is issued.
8. The Deep Power Down exit procedure must be followed the figure of Deep Power Down Mode Entry & Exit Cycle.
9. The clock must toggle at least once during the t_{XP} period.
10. The clock must toggle at least once during the t_{XSR} time.

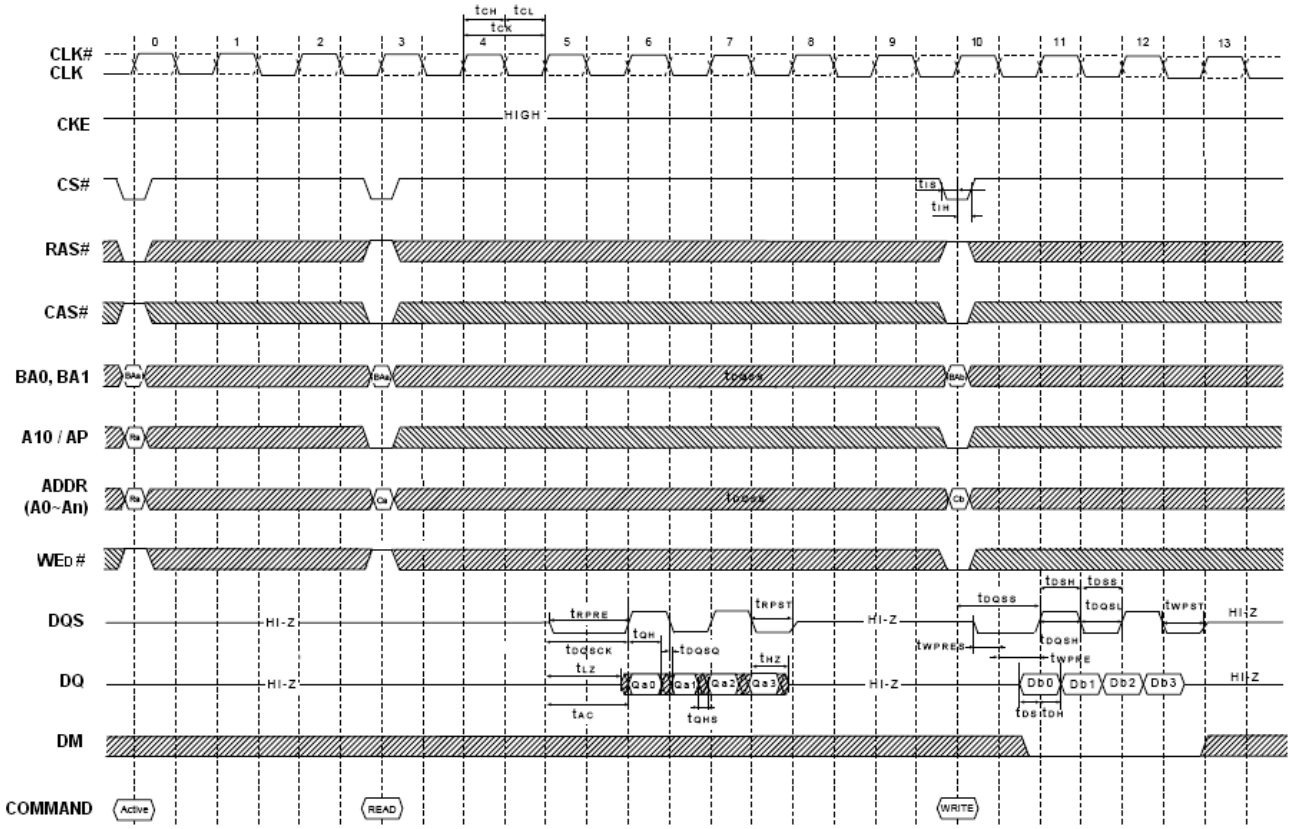
Truth Table – Current State Bank n

Current State	CS #	RAS #	CAS#	WE_D#	COMMAND / ACTION	NOTE
Command to Bank n [Note 1~12]						
Any	H	X	X	X	DESELECT (NOP / continue previous operation)	
	L	H	H	H	No Operation (NOP / continue previous operation)	
Idle	L	L	H	H	ACTIVE (select and activate row)	
	L	L	L	H	AUTO REFRESH	9
	L	L	L	L	MODE REGISTER SET	9
Row Active	L	H	L	H	READ (select column & start read burst)	
	L	H	L	L	WRITE (select column & start write burst)	
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	4
Read (Auto Precharge Disabled)	L	H	L	H	READ (select column & start new read burst)	5
	L	H	L	L	WRITE (select column & start write burst)	5, 12
	L	L	H	L	PRECHARGE (truncate read burst, start precharge)	
	L	H	H	L	BURST TERMINATE	10
Write (Auto Precharge Disabled)	L	H	L	H	READ (select column & start read burst)	5,11
	L	H	L	L	WRITE (select column & start new write burst)	5
	L	L	H	L	PRECHARGE (truncate write burst, start precharge)	11
Command to Bank m [Note 1~3,6, 11~16]						
Any	H	X	X	X	DESELECT (NOP / continue previous operation)	
	L	H	H	H	No Operation (NOP / continue previous operation)	
Idle	X	X	X	X	Any command allowed to bank m	
Row Activating, Active, or Precharging	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column & start read burst)	16
	L	H	L	L	WRITE (select column & start write burst)	16
	L	L	H	L	PRECHARGE	
Read (Auto Precharge disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column & start new read burst)	16
	L	H	L	L	WRITE (select column & start write burst)	12,16
	L	L	H	L	PRECHARGE	
Write (Auto Precharge disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column & start read burst)	11,16
	L	H	L	L	WRITE (select column & start new write burst)	16
	L	L	H	L	PRECHARGE	
Read with Auto Precharge	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column & start new read burst)	13,16
	L	H	L	L	WRITE (select column & start write burst)	12,13,16
	L	L	H	L	PRECHARGE	
Write with Auto Precharge	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column & start read burst)	13,16
	L	H	L	L	WRITE (select column & start new write burst)	13,16
	L	L	H	L	PRECHARGE	

Notes:

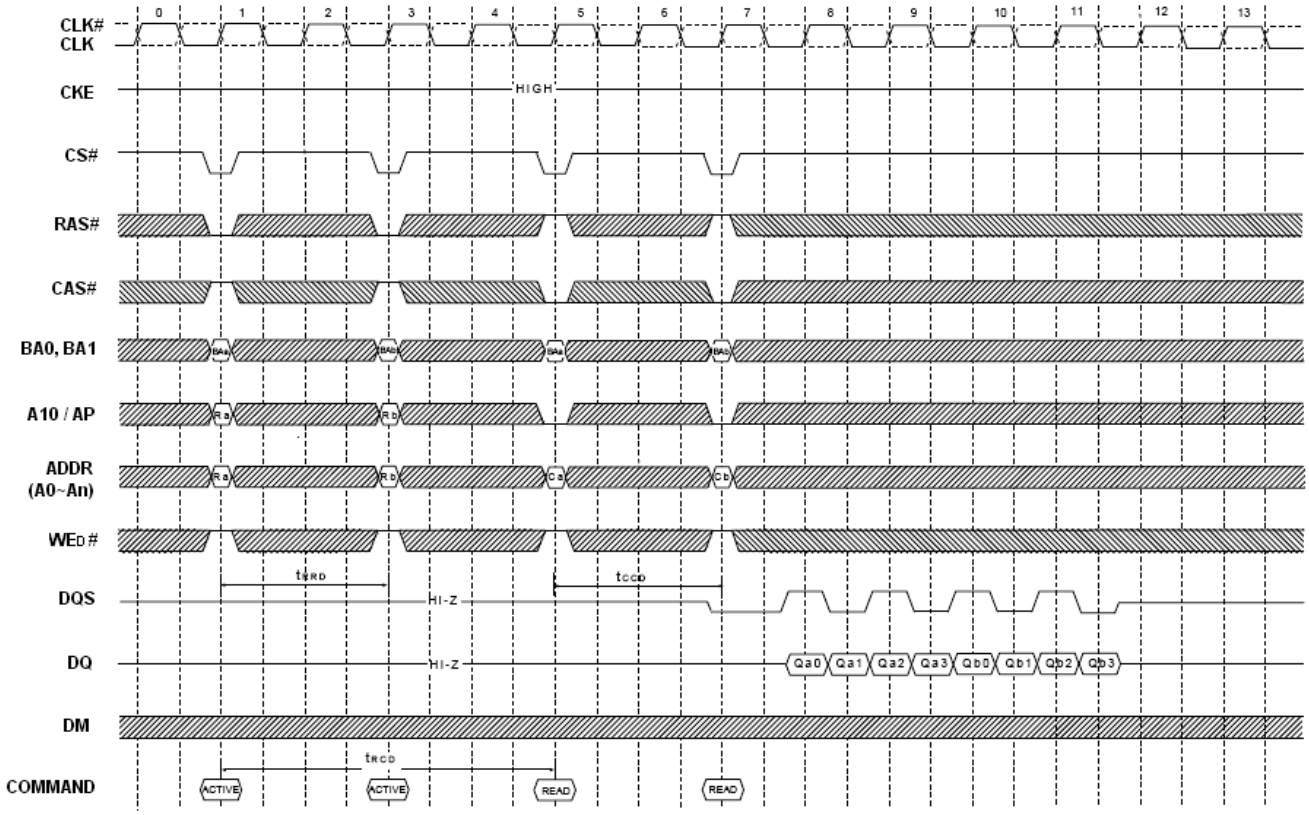
1. The table applies when both CKE n-1 and CKE n are HIGH, and after t_{XSR} or t_{XP} has been met if the previous state was Self Refresh or Power Down.
2. DESELECT and NOP are functionally interchangeable.
3. All states and sequences not shown are illegal or reserved.
4. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
5. The new Read or Write command could be Auto Precharge enabled or Auto Precharge disabled.
6. Current State Definitions:
   Idle: The bank has been precharged, and t_{RP} has been met.
   Row Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts / accesses and no register accesses are in progress.
   Read: A READ burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   Write: a WRITE burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
7. The following states must not be interrupted by a command issued to the same bank. DESELECT or NOP commands or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and the part of Command to Bank n, according to the part of Command to Bank m.
   Precharging: starts with the registration of a PRECHARGE command and ends when t_{RP} is met. Once t_{RP} is met, the bank will be in the idle state.
   Row Activating: starts with registration of an ACTIVE command and ends when t_{RCD} is met. Once t_{RCD} is met, the bank will be in the 'row active' state.
   Read with AP Enabled: starts with the registration of the READ command with Auto Precharge enabled and ends when t_{RP} has been met. Once t_{RP} has been met, the bank will be in the idle state.
   Write with AP Enabled: starts with registration of a WRITE command with Auto Precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank will be in the idle state.
8. The following states must not be interrupted by any executable command; DESELECT or NOP commands must be applied to each positive clock edge during these states.
   Refreshing: starts with registration of an AUTO REFRESH command and ends when t_{RFC} is met. Once t_{RFC} is met, the device will be in an 'all banks idle' state.
   Accessing Mode Register: starts with registration of a MODE REGISTER SET command and ends when t_{MRD} has been met. Once t_{MRD} is met, the device will be in an 'all banks idle' state.
   Precharging All: starts with registration of a PRECHARGE ALL command and ends when t_{RP} is met. Once t_{RP} is met, the bank will be in the idle state.
9. Not bank-specific; requires that all banks are idle and no bursts are in progress.
10. Not bank-specific. BURST TERMINATE affects the most recent read burst, regardless of bank.
11. Requires appropriate DM masking.
12. A WRITE command may be applied after the completion of data output, otherwise a BURST TERMINATE command must be issued to end the READ prior to asserting a WRITE command.
13. Read with AP enabled and Write with AP enabled: the Read with Auto Precharge enabled or Write with Auto Precharge enabled states can be broken into two parts: the access period and the precharge period. For Read with AP, the precharge period is defined as if the same burst was executed with Auto Precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all the data in the burst. For Write with AP, the precharge period begins when t_{WR} ends, with t_{WR} measured as if Auto Precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or t_{RP}) begins. During the precharge period of the Read with AP enabled or Write with AP enabled states, ACTIVE, PRECHARGE, READ, and WRITE commands to the other bank may be applied; during the access period, only ACTIVE and PRECHARGE commands to the other banks may be applied. In either case, all other related limitations apply (e.g. contention between READ data and WRITE data must be avoided).
14. AUTO REFRESH, SELF REFRESH, and MODE REGISTER SET commands may only be issued when all bank are idle.
15. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
16. READs or WRITEs listed in the Command column include READs and WRITEs with Auto Precharge enabled and READs and WRITEs with Auto Precharge disabled.

Basic Timing (Setup, Hold and Access Time @ BL=4, CL=3)



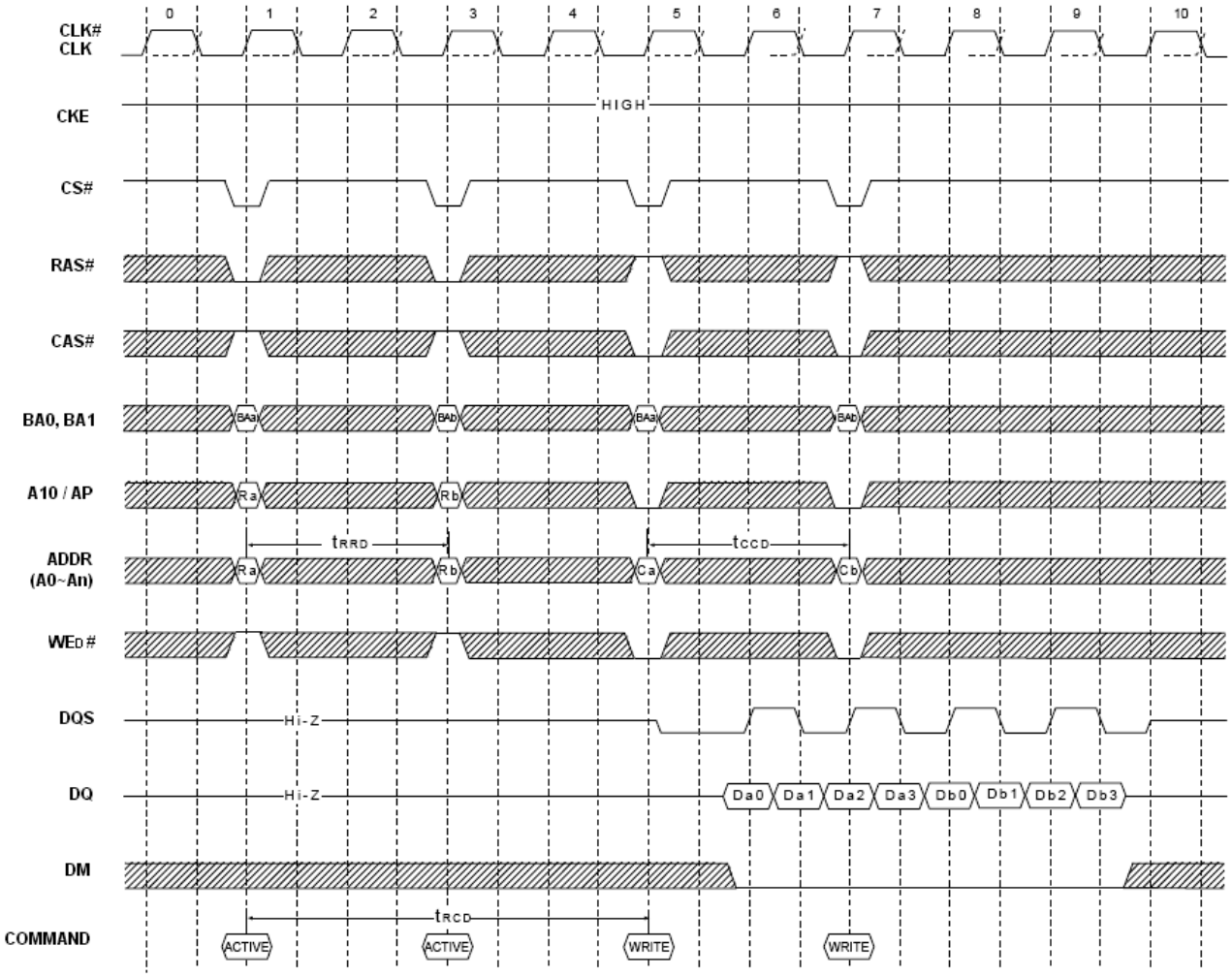
Note: t_{HP} is lesser of t_{CL} or t_{CH} clock transition collectively when a bank is active.

Multi Bank Interleaving READ (@BL=4, CL=3)

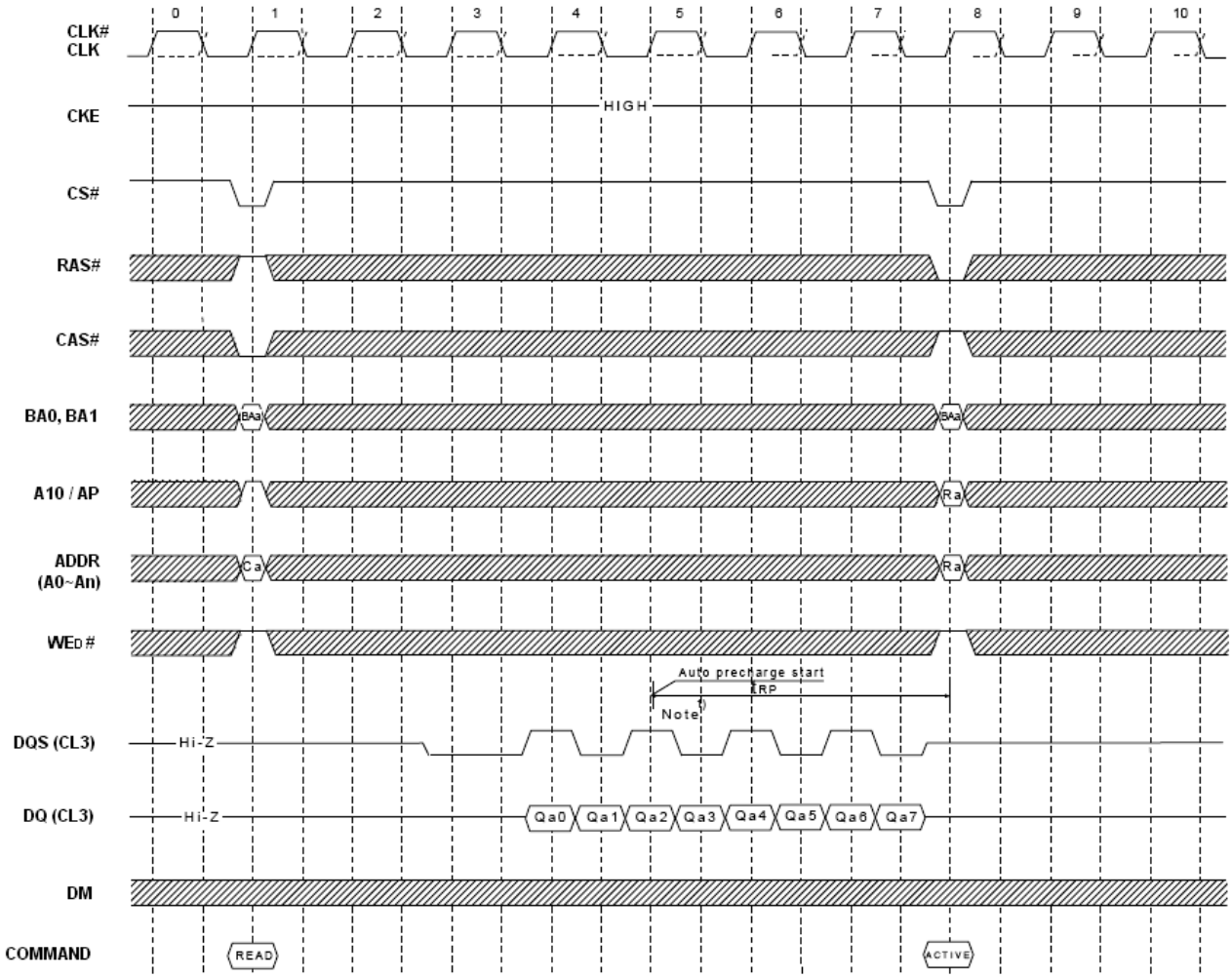


Note: t_{HP} is lesser of t_{CL} or t_{CH} clock transition collectively when a bank is active.

Multi Bank Interleaving WRITE (@BL=4)

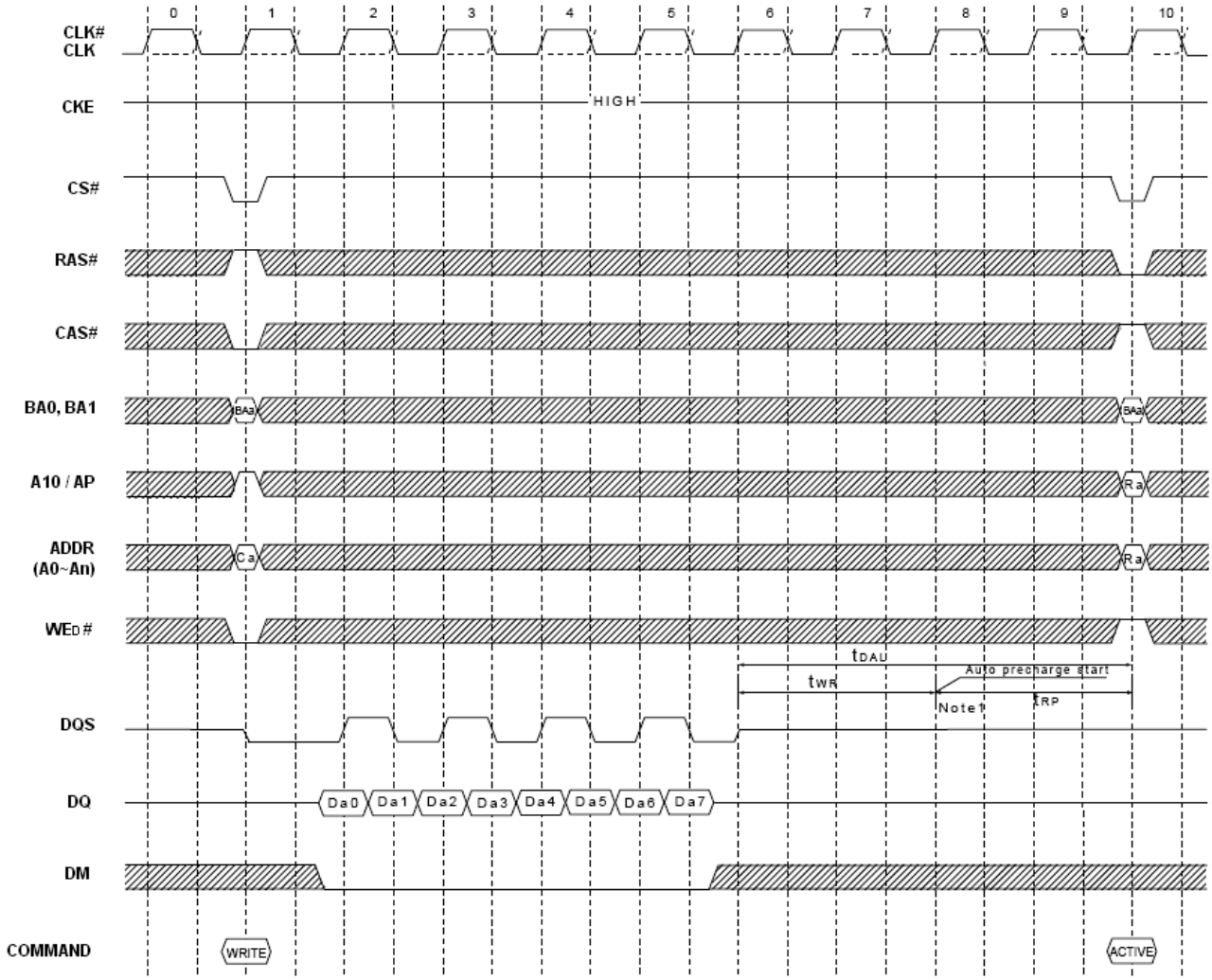


Read with Auto Precharge (@BL=8)



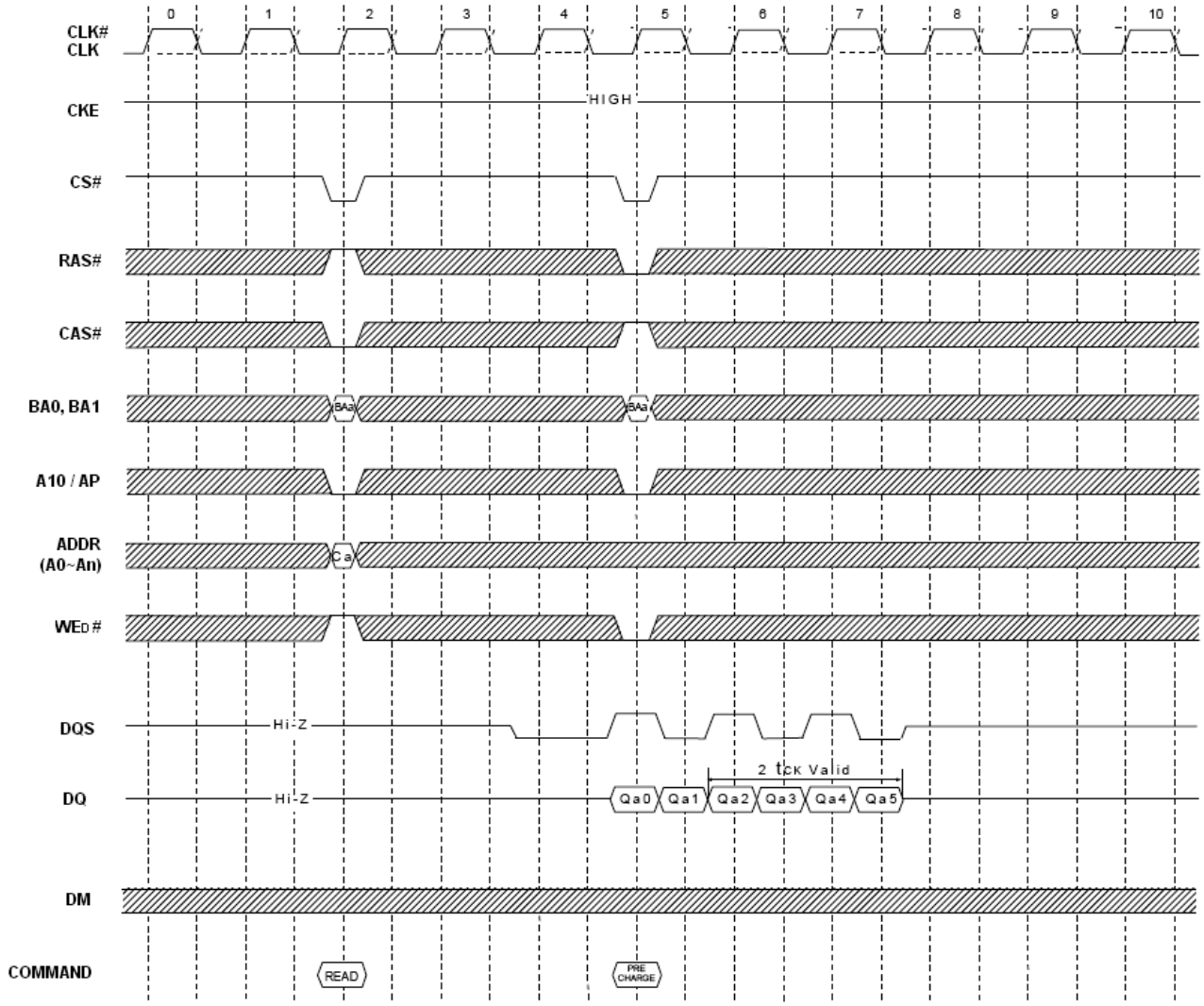
Note: The row active command of the precharge bank can be issued after t_{RP} from this point.

Write with Auto Precharge (@BL=8)

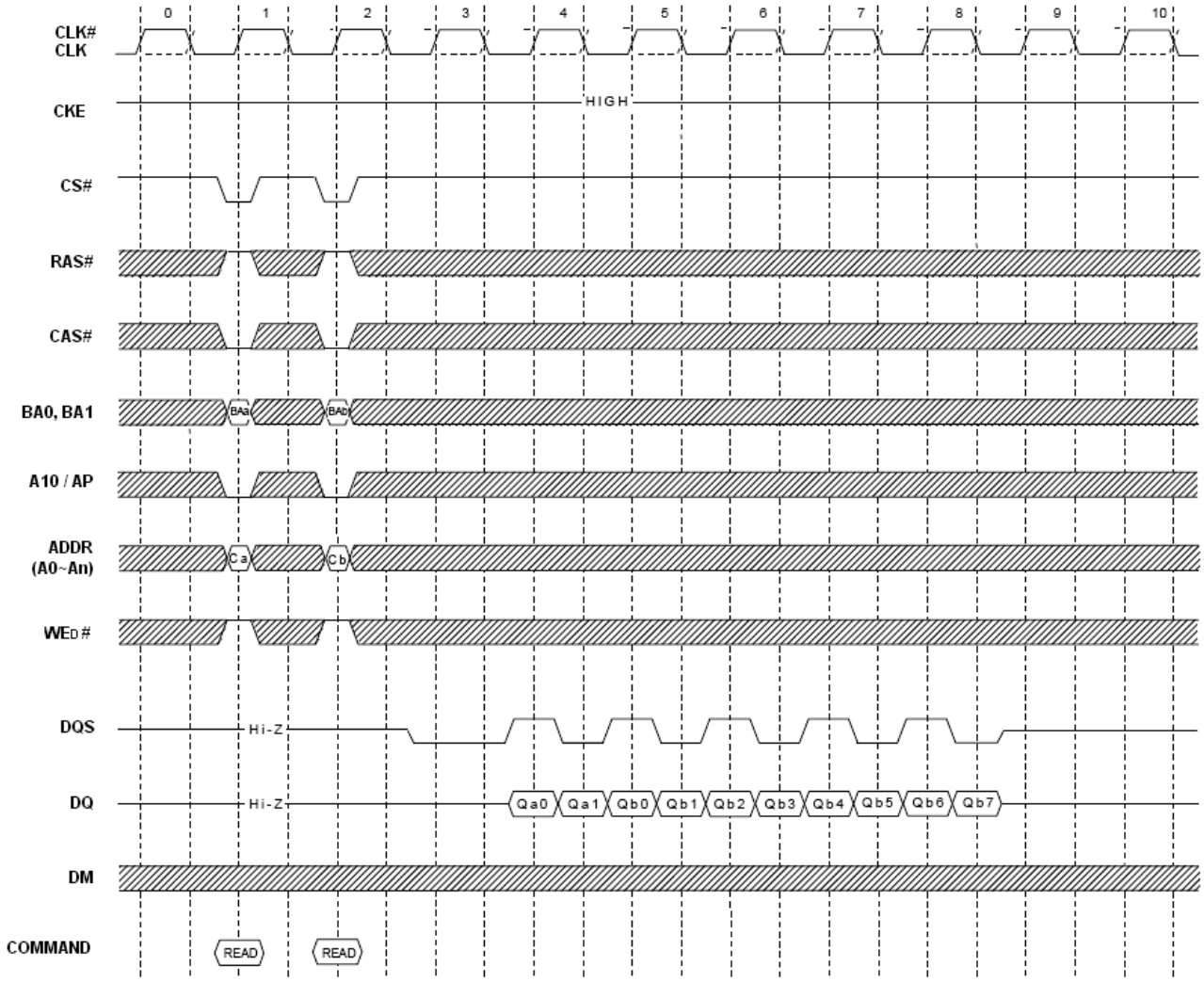


Note: The row active command of the precharge bank can be issued after t_{RP} from this point.

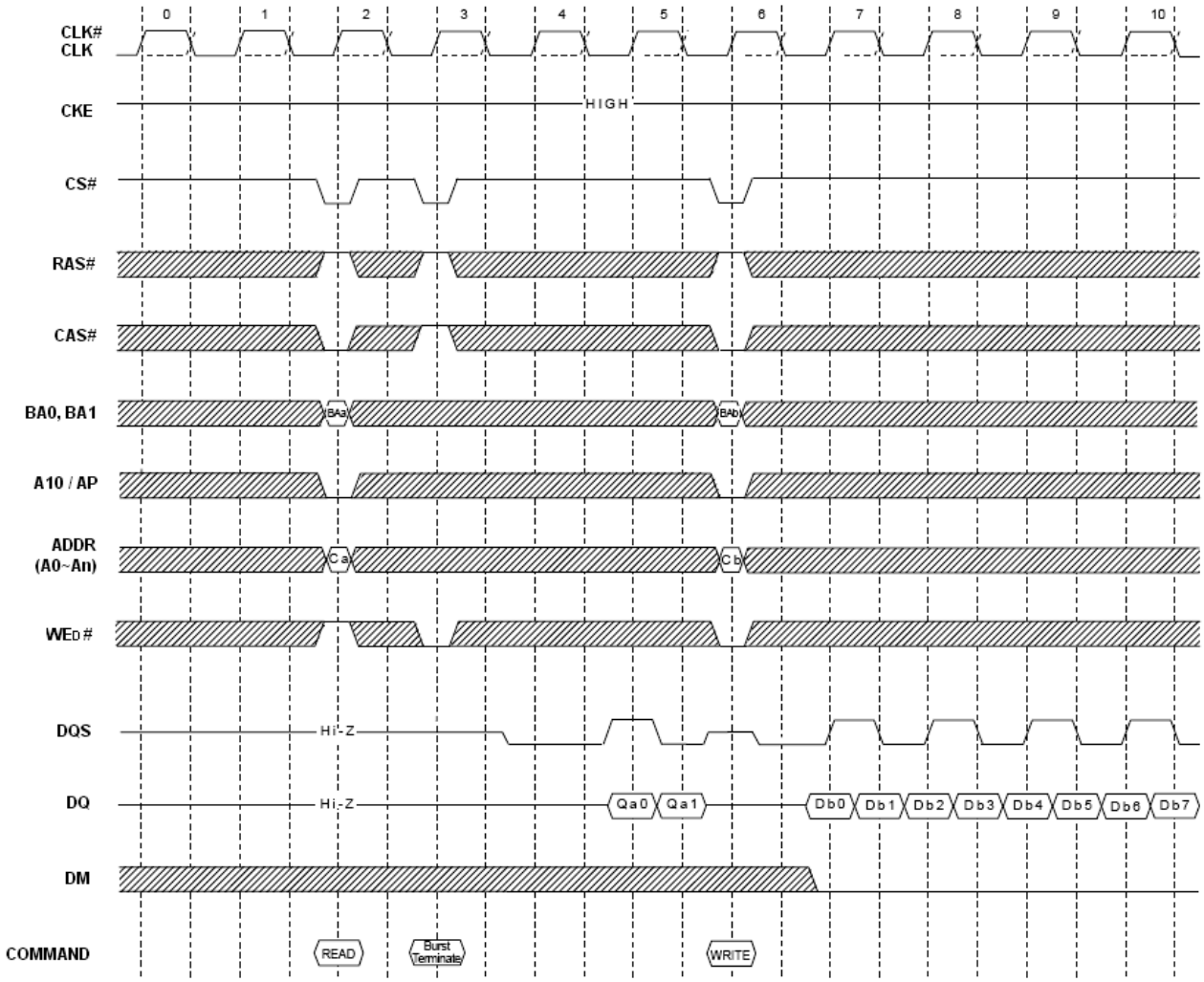
Read Interrupted by Precharge (@BL=8)



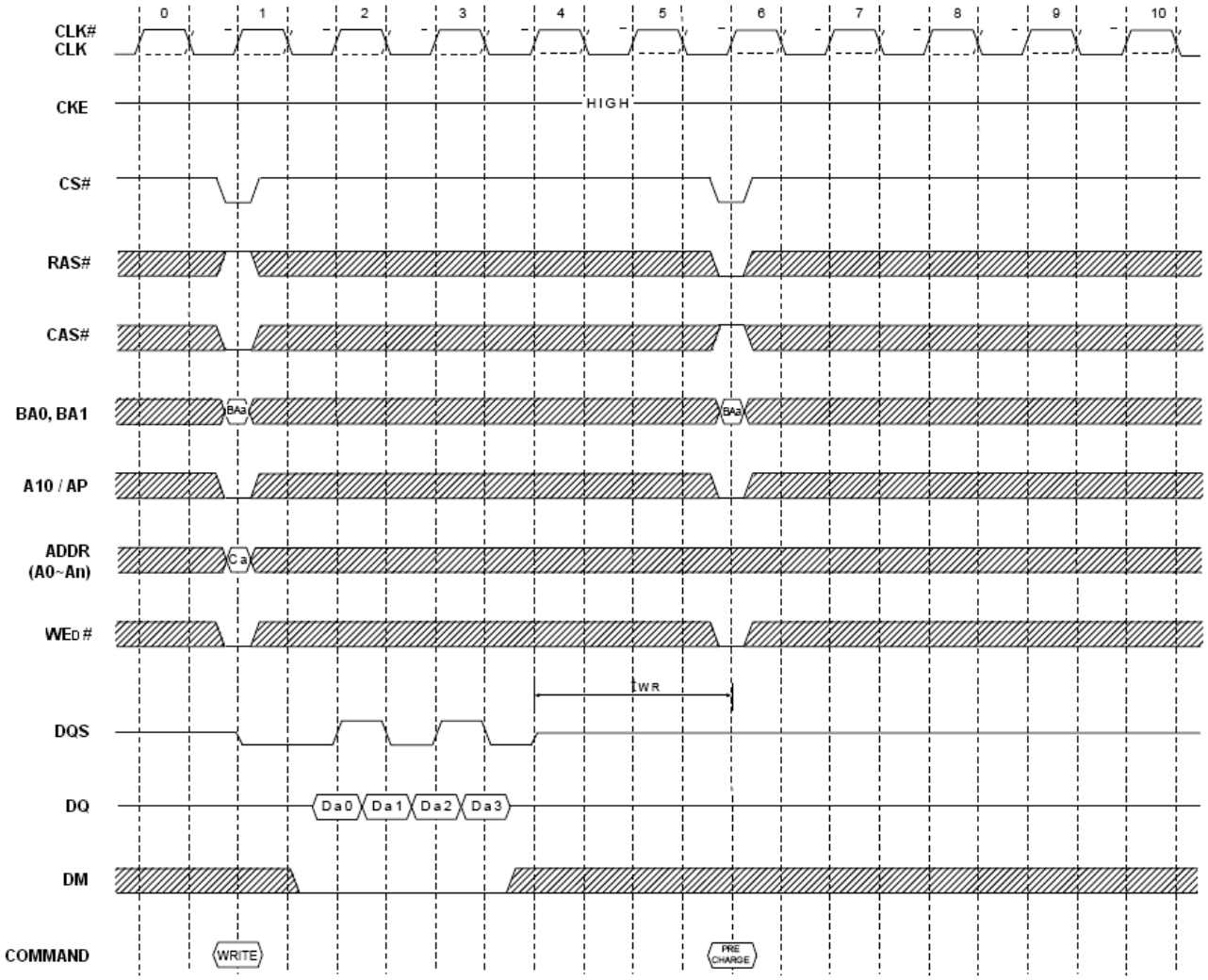
Read Interrupted by a Read (@BL=8, CL=3)



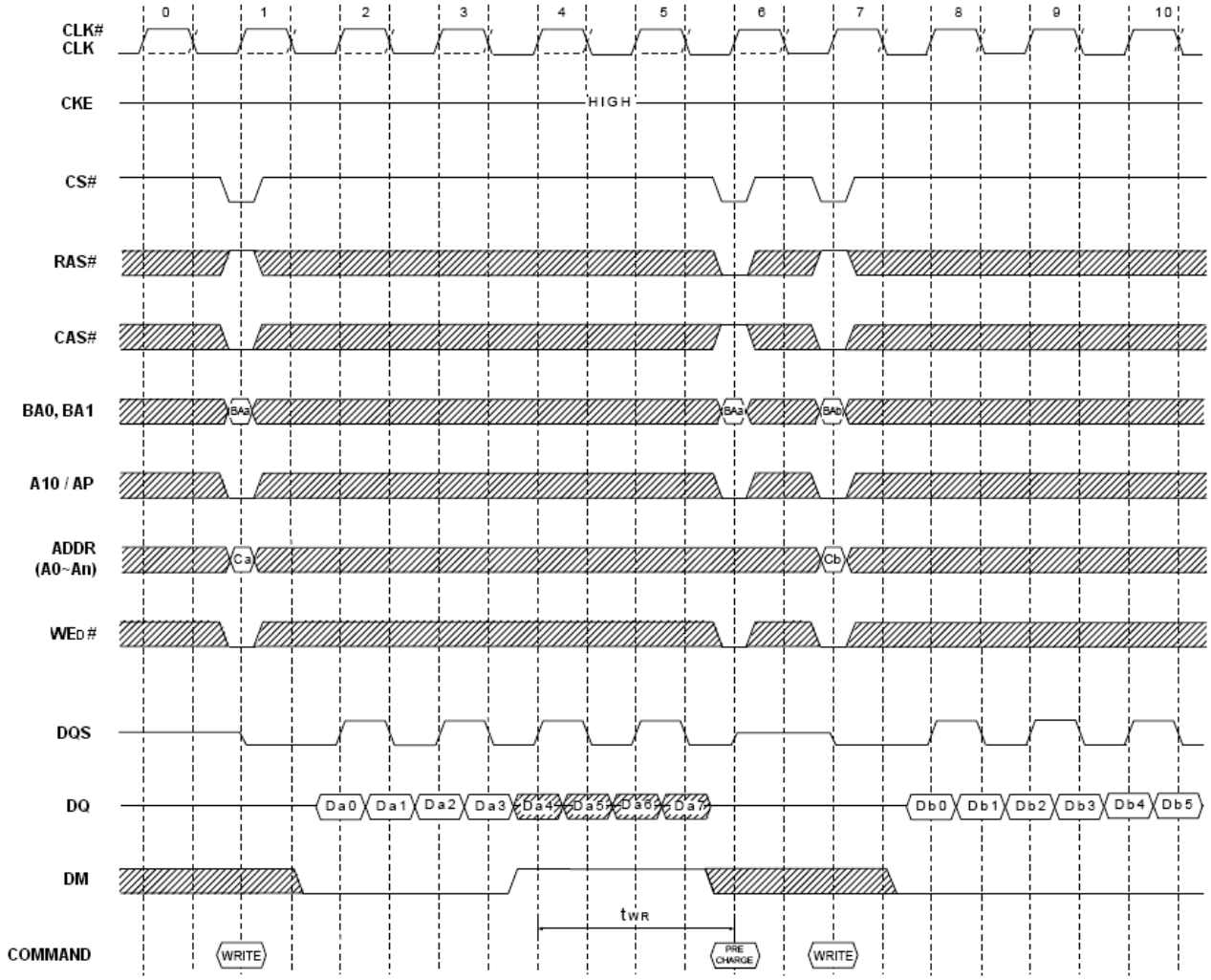
Read Interrupted by a Write & Burst Terminate (@BL=8, CL=3)



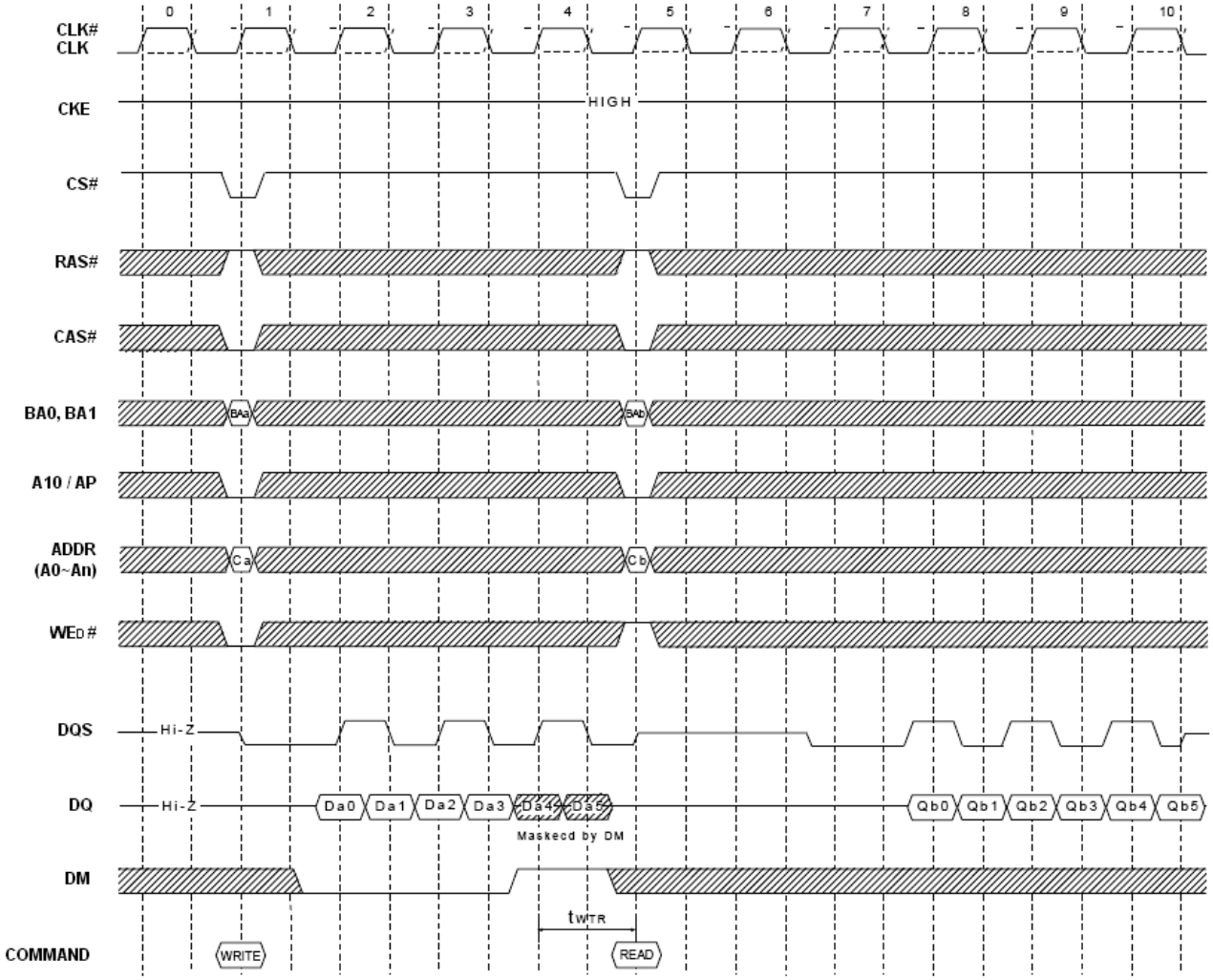
Write followed by Precharge (@BL=4)



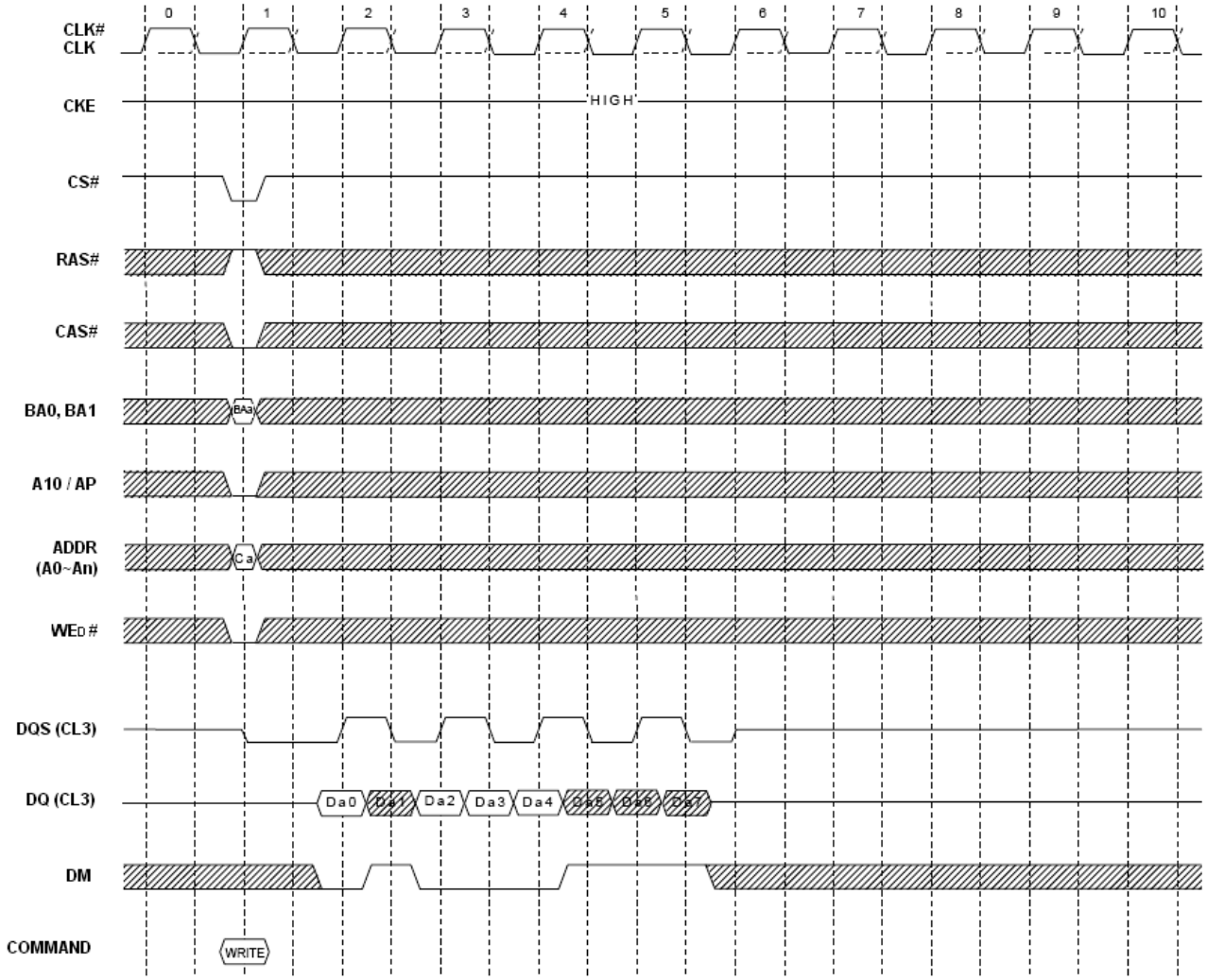
Write Interrupted by Precharge & DM (@BL=8)



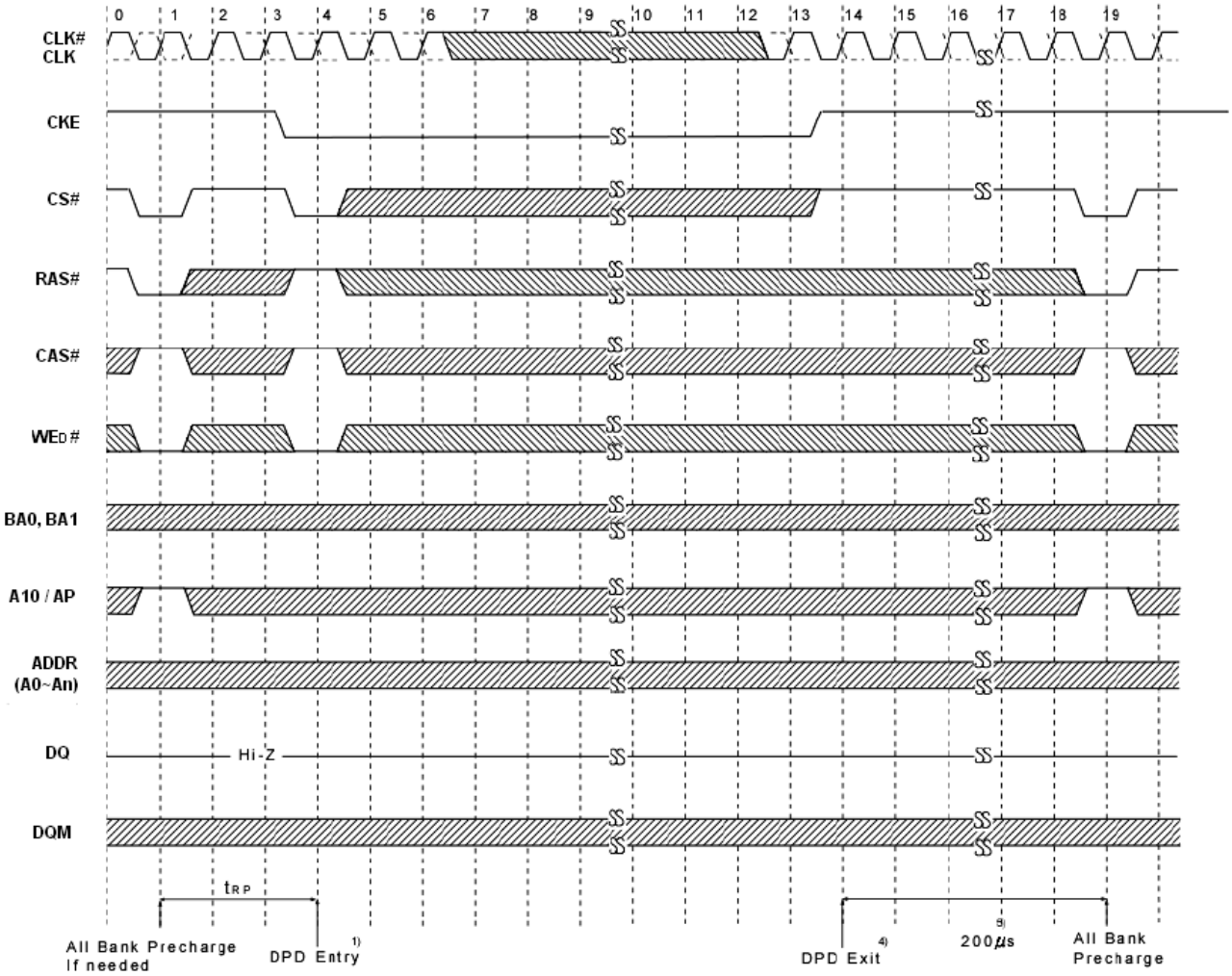
Write Interrupted by a Read (@BL=8, CL=3)



DM Function (@BL=8) only for write



Deep Power Down Mode Entry & Exit Cycle



Note:

DEFINITION OF DEEP POWER MODE FOR Mobile DDR SDRAM:
Deep Power Down Mode is an operating mode to achieve maximum power reduction by cutting the power of the whole memory of the device. Once the device enters in Deep Power Down Mode, data will not be retained. Full initialization is required when the device exits from Deep Power Down Mode.

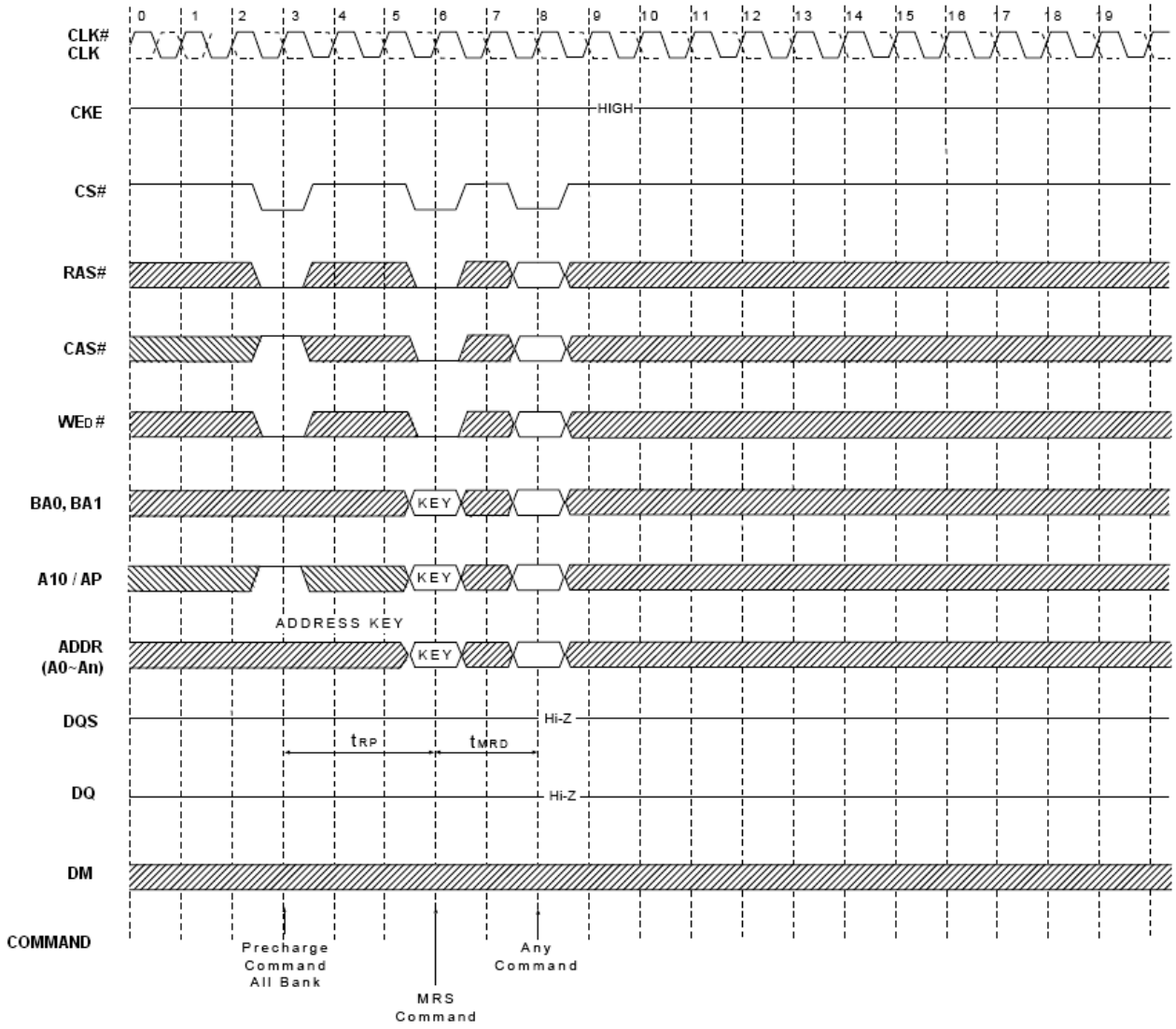
TO ENTER DEEP POWER DOWN MODE

1) The deep power down mode is entered by having CS# and WE_D# held low with RAS# and CAS# high at the rising edge of the clock. While CKE is low.
2) Clock must be stable before exited deep power down mode.
3) Device must be in the all banks idle state prior to entering Deep Power Down mode.

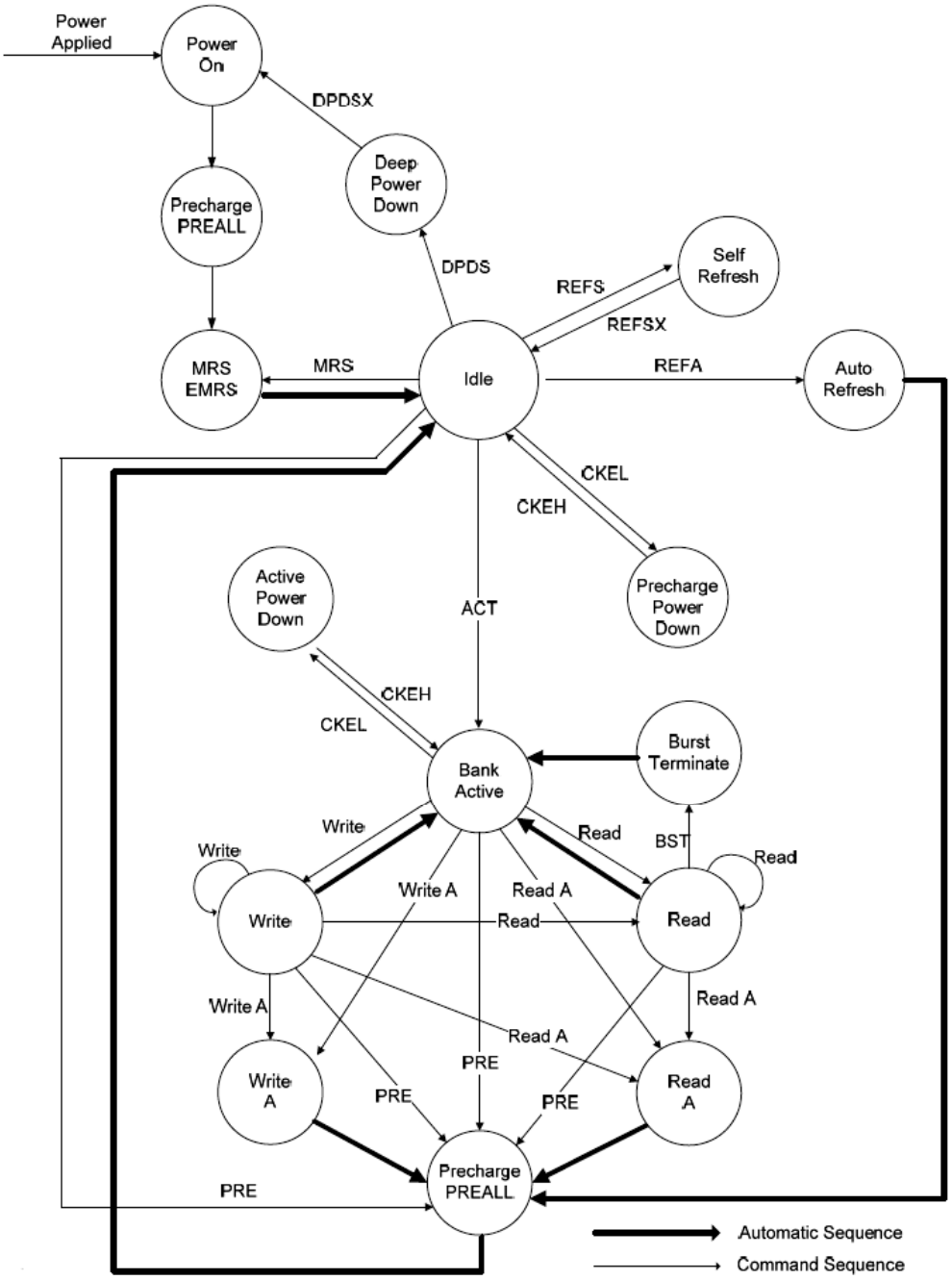
TO EXIT DEEP POWER DOWN MODE

4) The deep power down mode is exited by asserting CKE high.
5) 200μs wait time is required to exit from Deep Power Down.
6) Upon exiting deep power down an all bank precharge command must be issued followed by two auto refresh commands and a load mode register sequence.

Mode Register Set



Simplified State Diagram



PREALL = Precharge All Banks
MRS = Mode Register Set
EMRS = Extended Mode Register Set
REFS = Enter Self Refresh
REFSX = Exit Self Refresh
REFA = Auto Refresh
CKEL = Enter Power Down
CKEH = Exit Power Down
ACT = Active

Write = Write w/o Auto Precharge
Write A = Write with Auto Precharge
Read = Read w/o Auto Precharge
Read A = Read with Auto Precharge
PRE = Precharge
BST = Burst Terminate
DPDS = Enter Deep Power-Down
DPDSX = Exit Deep Power-Down

Revisions List

Revision No	Description	Date
Preliminary 0.0	Initial Release	2012/08/03
A	Update datasheet version from Preliminary 0.0 to A.	2012/12/07