



**EN71NS128B0 Base MCP  
Stacked Multi-Chip Product (MCP) Flash Memory and RAM  
128 Megabit (8M x 16-bit) CMOS 1.8 Volt-only Simultaneous  
Operation Burst Mode Flash Memory and  
32 Megabit (2M x 16-bit) Pseudo Static RAM**

**Distinctive Characteristics  
MCP Features**

- **Power supply voltage of 1.7V to 1.95V**
- **High performance**
  - 70 ns @ random access
  - 7 ns @ burst access (108MHz)
- **Package**
  - 6.2 x 7.7 x 1.0mm 56 ball BGA
- **Operating Temperature**
  - 25°C to +85°C

**General Description**

The EN71NS series is a product line of stacked Multi-Chip Product (MCP) packages and consists of:

- E29NS128 (Burst mode) Flash memory die.
- Pseudo SRAM.

For detailed specifications, Please refer to the individual datasheets listed in the following table.

Device	Document
NOR Flash	EN29NS128
Pseudo SRAM	ENPSS32

**Product Selector Guide**

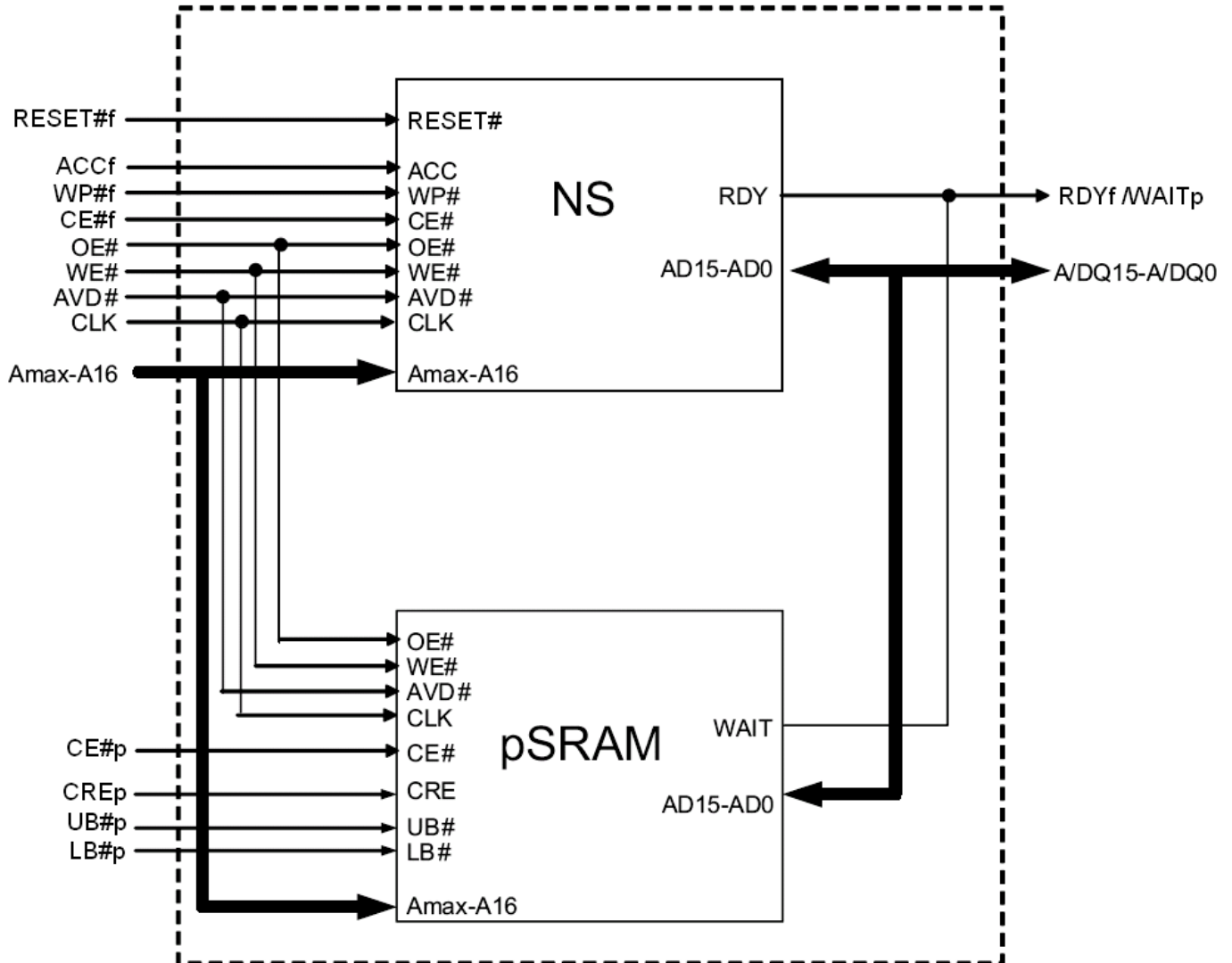
**128 Mb Flash Memories**

<b>Device-Model#</b>	EN71NS128B0	<b>pSRAM density</b>	32M pSRAM
<b>Flash Access time</b>	70ns at Async. Mode 7ns at Burst Read	<b>pSRAM Access time</b>	70ns at Async. Mode 7ns at Burst Read
<b>pSRAM Burst mode max frequency</b>	108MHz	<b>pSRAM Burst mode max frequency</b>	108MHz
<b>Package</b>	56-ball BGA		



### MCP Block Diagram

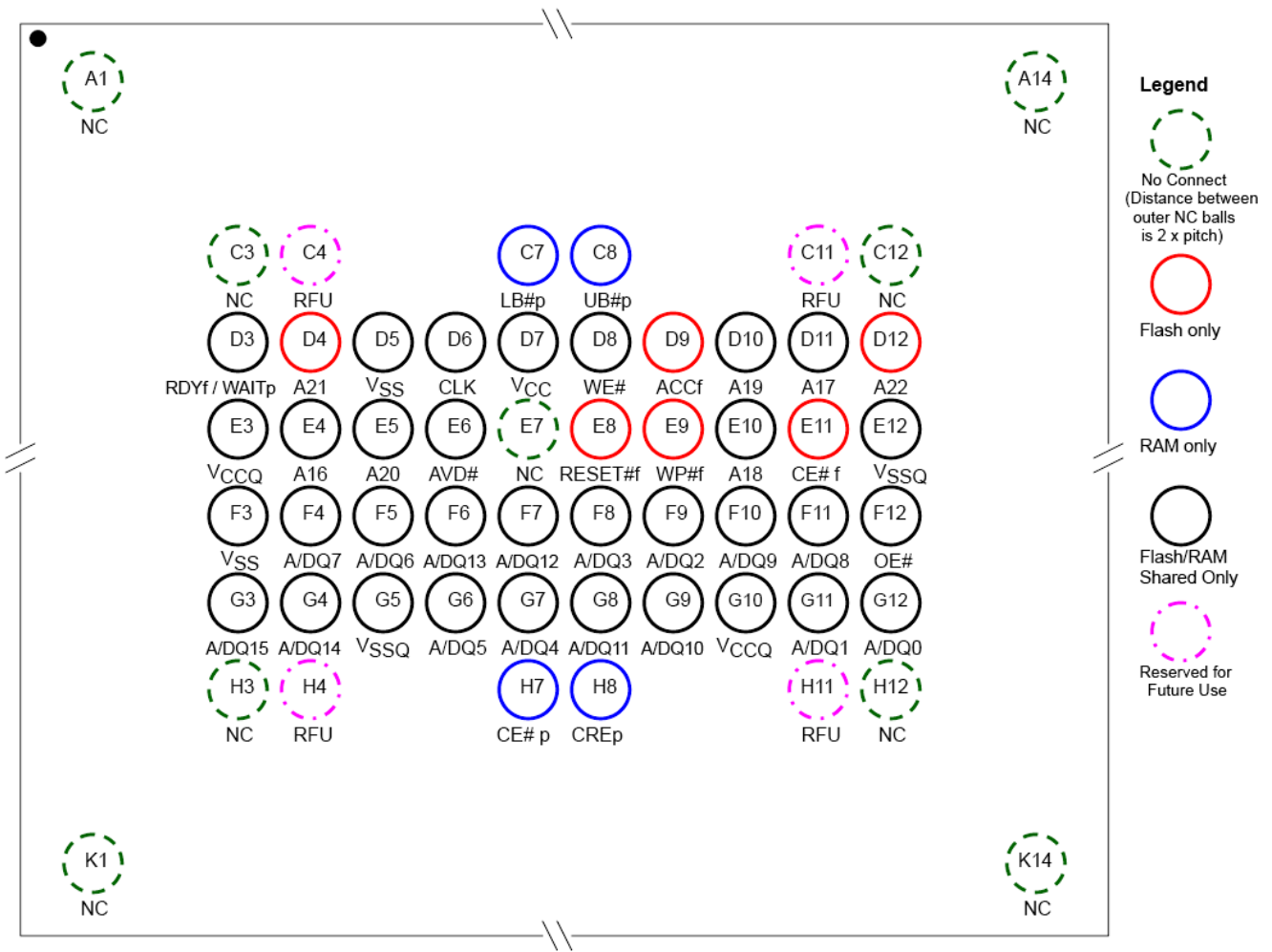
### NOR FLASH + PSRAM DIAGRAM



**Note:** Amax = A22



Connection Diagram



MCP	Flash-only Addresses	Shared Addresses	Shared ADQ Pins
EN71NS128B0	A22 – A21	A20 – A16	ADQ15 – ADQ0



## Pin Description

Symbol	Description	Flash	pSRAM
A22–A16	Address Inputs	•	•
ADQ15–ADQ0	Multiplexed Address/Data	•	•
OE#	Output Enable input. Asynchronous relative to CLK for the Burst mode.	•	•
WE#	Write Enable input.	•	•
VSSQ/VSS	Ground	•	•
VCCQ/VCC	Device Power Supply (1.7 V–1.95 V).	•	•
NC	Not Contact; pin not connected internally	•	•
RDYf/WAITp	Ready output; indicates the status of the Burst read. Flash Memory RDY (using default “Active HIGH” configuration) $V_{OL}$ = data invalid, $V_{OH}$ = data valid. Note: The default polarity for the pSRAM WAIT signal is opposite the default polarity of the Flash RDY signal.  pSRAM WAIT (using default “Active HIGH” configuration) $V_{OL}$ = data valid, $V_{OH}$ = data invalid. To match polarities, change bit 10 of the pSRAM Bus Configuration Register to 0 (Active LOW WAIT). Alternately, change bit 10 of the Flash Configuration Register to 0 (Active LOW RDY)	•	•
CLK	Clock input. In burst mode, after the initial word is output, subsequent active edges of CLK increment the internal address counter. Should be at $V_{OL}$ or $V_{IH}$ while in asynchronous mode.	•	•
AVD#	Address Valid input. Indicates to device that the valid address is present on the address inputs. $V_{IL}$ = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched on rising edge of CLK. $V_{IH}$ = device ignores address inputs	•	•
RESET# f	Hardware reset input. $V_{IL}$ = device resets and returns to reading array data	•	
WP#f	Hardware write protect input. $V_{IL}$ = disables program and erase functions in the four outermost sectors. Should be at $V_{IH}$ for all other conditions.	•	
ACCf	Accelerated input. At $V_{HH}$ , accelerates programming; automatically places device in Accelerated Program mode. At $V_{IL}$ , disables all program and erase functions. Should be at $V_{IH}$ for all other conditions. (Applying high voltage on MCP package is prohibited; otherwise, internal RAM may be damaged easily!)	•	
CE# p	Chip Enable Input for pSRAM.		•
CE# f	Chip Enable Input for Flash. Asynchronous relative to CLK for the Burst mode.	•	
CREp	Control register enable (pSRAM).		•
LB#p	Lower byte enable. DQ7~DQ0 (pSRAM)		•
UB#p	Upper byte enable. DQ15~DQ8 (pSRAM)		•
RFU	Reserved for Future Use		



**Operating Mode (For Asynchronous mode)**

Asynchronous Mode BCR[15]=1	Power	CLK	ADV#	CE#	OE#	WE#	CRE	UB#/ LB#	WAIT2	A/DQ[15:0]
Read	Active	X		L	L	H	L	L	Low-z	Data out
Write	Active	X		L	X	L	L	L	High-z	Data in
Standby	Standby	H or L	X	H	X	X	L	X	High-z	High-z
No operation	Idle	X	X	L	X	X	L	X	Low-z	X
Configuration register write	Active	X		L	H	L	H	X	Low-z	High-z
Configuration register read	Active	X		L	L	H	H	L	Low-z	Config. Reg.out

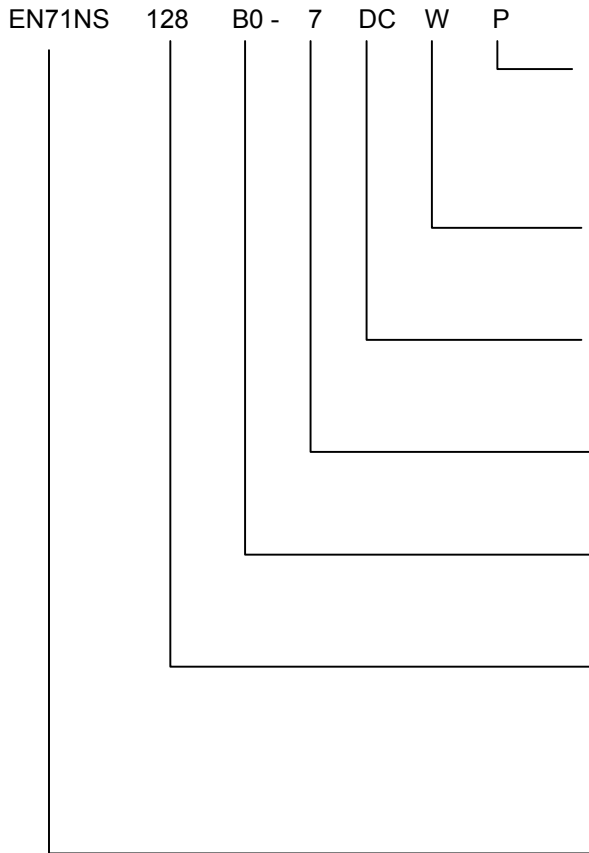
**Operating Mode (For Synchronous Burst mode)**

Burst Mode BCR[15]=0	Power	CLK	ADV#	CE#	OE#	WE#	CRE	UB#/ LB#	WAIT	A/DQ[15:0]
Async read	Active	H or L		L	L	H	L	L	Low-z	Data out
Async write	Active	H or L		L	X	L	L	L	High-z	Data in
Standby	Standby	H or L	X	H	X	X	L	X	High-z	High-z
No operation	Idle	H or L	X	L	X	X	L	X	Low-z	X
Initial burst read	Active		L	L	X	H	L	L	Low-z	Address
Initial burst write	Active		L	L	H	L	L	X	Low-z	Address
Burst continue	Active		H	L	X	X	X	L	Low-z	Data out or Data in
Configuration register write	Active		L	L	H	L	H	X	Low	High-z
Configuration register read	Active		L	L	L	H	H	L	Low	Config. Reg.out

**Note:** X=don't care. H=logic high. L=logic low. V= Valid data



**ORDERING INFORMATION**



**PACKAGING CONTENT**

P = RoHS compliant

**TEMPERATURE RANGE**

W = Wireless (-25°C to +85°C)

**PACKAGE**

DC = 56-Ball BGA  
0.50mm pitch, 6.2mm x 7.7mm package

**BURST READ ACCESS TIME**

7 = 108 MHz

**Pseudo SRAM density**

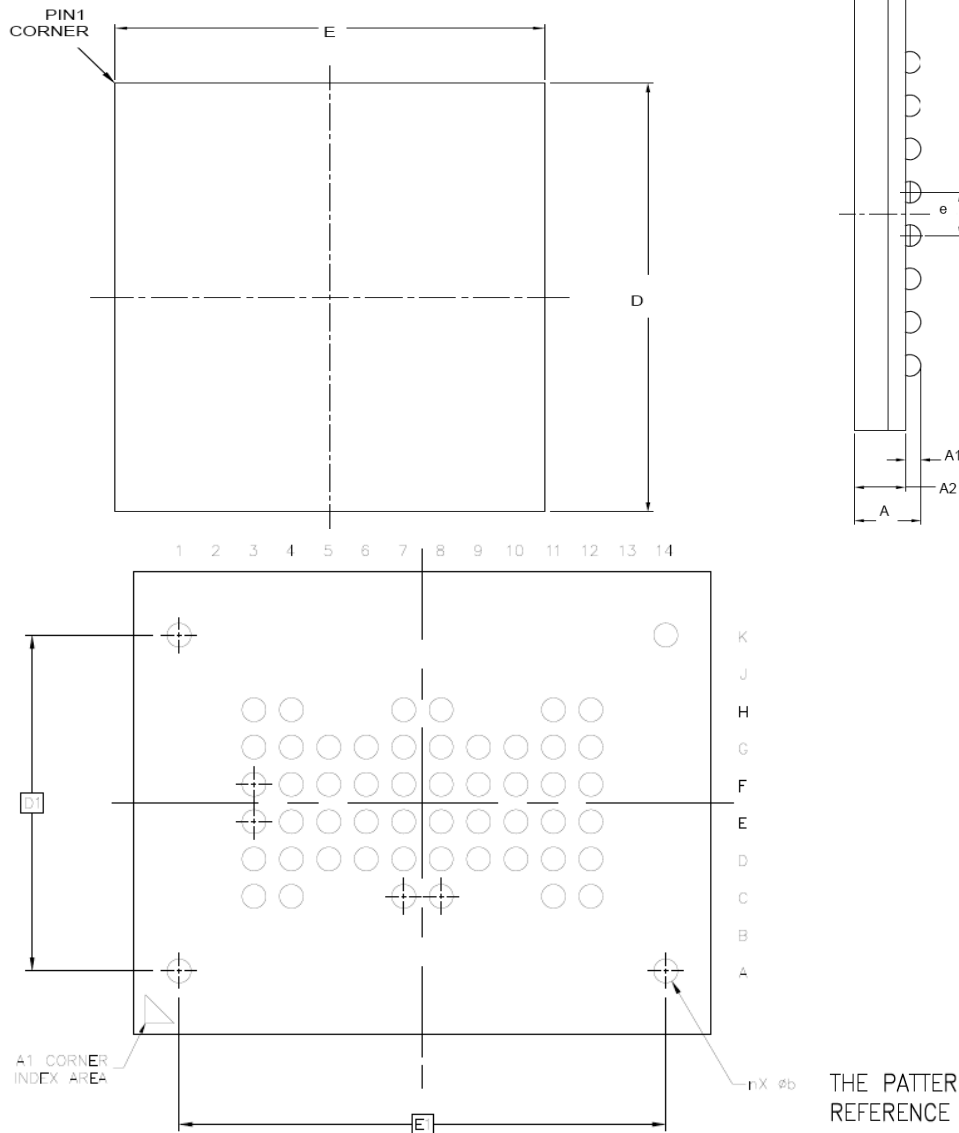
B0 = 32Mb

**DENSITY**

128 = 128Megabit (8M x 16 Bit)

**BASE PART NUMBER**

EN = Eon Silicon Solution Inc.  
71NS = Multi-chip Product (MCP)  
1.8V Simultaneous Read/Write,  
Burst-mode Multiplexed Flash and RAM

**PACKAGE MECHANICAL**
**56-ball Ball Grid Array (BGA) 6.2 x 7.7 x 1.0mm Package, pitch: 0.5mm, ball: 0.3mm**


SYMBOL	DIMENSION IN MM		
	MIN.	NOR	MAX
A	---	---	1.00
A1	0.16	---	0.26
A2	0.676		
D	6.10	6.20	6.30
E	7.60	7.70	7.80
D1	4.5 BSC		
E1	6.5 BSC		
e	0.5 BSC		
b	0.27	---	0.37

**Note : 1. Coplanarity: 0.1 mm**



**Revisions List**

<b>Revision No</b>	<b>Description</b>	<b>Date</b>
A	Initial Release	2009/07/24
B	Update the package size and ball assignment from "8 x 9.2mm 56 ball FBGA" to "8 x 6mm 52 ball BGA".	2009/12/01
C	Change the package option from 52 ball BGA to 56 ball BGA and related information.	2010/08/20