FUJITSU SEMICONDUCTOR
DATA SHEET

DS601-00003-0v01-E

Semicustom

CMOS

Standard Cell

CS251 Series

■ DESCRIPTION

The CS251 series of 55 nm standard cells is a line of CMOS ASICs that satisfy demands for lower power consumption, higher speed and higher integration.

These cells offer the minimum level of leakage current in the semiconductor industry, and are able to implement a mixture of three types of core transistors with different threshold voltages, as appropriate for the applications ranging from handheld terminals to digital audiovisual equipment.

The integration level in this series is approximately 1.2 times the CS201 series, the previous product of 65 nm standard cells, with approximately 20% less power consumption by power reduction of the SRAMs.

In this series, IPs for CS201 series developed by customers can be implemented.

■ FEATURES

- Technology : 55 nm Si gate CMOS
  6 to 12 layers of metal wiring.
  Three different types of core transistors (low leak, standard and high speed) can be used on the same chip.
- Power supply voltage : + 1.2V ± 0.1 V
- Junction temperature range : − 40 °C to + 125 °C (standard specification)
- Support high-quality, various types of cell sets developed by FUJITSU SEMICONDUCTOR (from low power versions to high speed versions).
- Support SRAMs with sleep-mode for lower power consumption memories.
- Support Clock Gating, multi-Vth and power supply isolation block (multi-V_{DD}, power gating) for circuit technology to reduce power consumption.
- Support a design flow where CPF, the industry standard power format, is adopted for a design environment of circuit technology to reduce power consumption.
- Compiled cells (RAM, ROM, others)
- Support special interfaces (LVDS, SSTL, others).
- Support boundary SCAN test.
- Support t use of industry standard libraries.
- Support use of industry standard tools.
- Short-term development using a physical prototyping tool
- One pass design using a physical synthesis tool
- Hierarchical design environment for supporting large-scale circuits
- Support Signal Integrity, EMI noise reduction.
- Support static timing sign-off.
- Improve timing convergence by using Statistical Static Timing Analysis (SSTA).

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- Design For Manufacturing (DFM) enables stable product-supply and reduced variation.
- Package lineup: FBGA, PBGA, TEBGA, FC-BGA

Note: Items under development are included.

■ MACRO LIBRARIES (INCLUDING MACROS CURRENTLY BEING PREPARED)

1. Logic cells (about 400 types)

Library sets having three different threshold voltages of core transistors.

- Adder
- AND
- AND-OR
- AND-OR Inverter
- Buffer
- Clock-Buffer
- Delay Buffer
- ENOR
- EOR
- Inverter
- Latch
- NAND
- NOR
- OR
- OR-AND
- OR-AND Inverter
- SCAN Flip flop
- Non-SCAN Flip flop
- Multiplexer
- Others

2. IP macros

CPU/DSP	ARM™* cores (ARM7TDMI-S™*, ARM946E-S™*, ARM926EJ-S™*, ARM1176JZF-S™*, Cortex-M0™*, Cortex-M0+™*, Cortex-M3™*, Cortex-R4F™*, Cortex-A5™*, Cortex-A7™*, Cortex-A9™*, Cortex-A15™*), Peripherals IP
Mixed signal macro	ADC, DAC, OPAMP, others
Compiled macro	SRAM (1 Port, 2 Port), ROM, others
PLL	Analog PLL

*: ARM, ARM7TDMI-S, ARM946E-S, ARM926EJ-S, ARM1176JZF-S, Cortex-M0, Cortex-M0+, Cortex-M3, Cortex-R4F, Cortex-A5, Cortex-A7, Cortex-A9 and Cortex-A15 are the trademarks of ARM Limited in the EU and other countries.

3. Special I/O interface macro

Special I/O	LVDS, SSTL18, PCI, I^2C
Interface macro	USB2.0 Device/host, Serial-ATA, PCI-Express, DDR2, HDMI, others

■ COMPILED CELLS

Compiled cells are macro cells that can be automatically generated by specifying the bit/word configuration.

The following compiled cells are available for the CS251 series (Note that the bit/word ranges for each macro vary depending on the column type).

1. Clock synchronous single-port RAM (1 address : 1 read/write)

• High Density type

Column type	Memory capacity (bit)	Word range (word)	Bit range (bit)
4	32 to 640 K	32 to 8 K	1 to 80
8	64 to 640 K	64 to 16 K	1 to 40

• High Density, Redundant type

Column type	Memory capacity (bit)	Word range (word)	Bit range (bit)
4	256 to 640 K	32 to 8 K	8 to 80
8	256 to 640 K	64 to 16 K	4 to 40

• Large Scale, Redundant type

Column type	Memory capacity (bit)	Word range (word)	Bit range (bit)
16	64 K to 8 M	8 K to 64 K	8 to 128

• High Speed type

Column type	Memory capacity (bit)	Word range (word)	Bit range (bit)
4	128 to 144 K	64 to 2 K	8 to 72

2. Clock synchronous dual port RAM (2 addresses : 2 read/write)

Column type	Memory capacity (bit)	Word range (word)	Bit range (bit)
2	32 to 72 K	16 to 512	2 to 144
4	64 to 72 K	32 to 1 K	2 to 72
8	128 to 72 K	64 to 2 K	2 to 36
16	256 to 72 K	128 to 4 K	2 to 18

3. Clock synchronous ROM

Column type	Memory capacity (bit)	Word range (word)	Bit range (bit)
16	256 to 1 M	128 to 8 K	2 to 128
64	1 K to 1 M	512 to 32 K	2 to 32

4. Clock synchronous register file (2 addresses : 1 read, 1 write)

Column type	Memory capacity (bit)	Word range (word)	Bit range (bit)
1	16 to 18 K	8 to 128	2 to 144

5. Clock synchronous register file (4 addresses : 2 read, 2 write)

Column type	Memory capacity (bit)	Word range (word)	Bit range (bit)
1	16 to 18 K	8 to 128	2 to 144

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{DD}	− 0.5	+ 1.8	V	*2
		− 0.5	+ 2.5		*3
		− 0.5	+ 4.6		*4
Input voltage*1	VI	− 0.5	V_{DD} + 0.5 (≤ 2.5V)	V	*3
		− 0.5	V_{DD} + 0.5 (≤ 4.6V)		*4
Output voltage*1	VO	− 0.5	V_{DD} + 0.5 (≤ 2.5V)	V	*3
		− 0.5	V_{DD} + 0.5 (≤ 4.6V)		*4
Storage temperature	T_{STG}	− 55	+ 125	°C	
Operation junction temperature	Tj	− 40	+ 125	°C	

*1: V_{SS} = 0 V

*2: Internal gates

*3: 1.8 V interface on dual-power supply system

*4: 3.3 V interface on dual-power supply system

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

• Dual power supply (V_{DDE} = 1.8 V ± 0.15 V, V_{DDI} = 1.2 V ± 0.1 V, V_{SS} = 0 V)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
Power supply voltage		V_{DDE}	1.65	1.8	1.95	V
		V_{DDI}	1.1	1.2	1.3	V
"H" level input voltage	1.8V CMOS Normal	V_{IH}	$V_{DDE} \times 0.65$	—	$V_{DDE} + 0.3$	V
	1.8V CMOS Schmitt		$V_{DDE} \times 0.70$	—	$V_{DDE} + 0.3$	V
"L" level input voltage	1.8V CMOS Normal	V_{IL}	− 0.3	—	$V_{DDE} \times 0.35$	V
	1.8V CMOS Schmitt		− 0.3	—	$V_{DDE} \times 0.30$	V
Schmitt hysteresis voltage		VH	$V_{DDE} \times 0.10$	—	$V_{DDE} \times 0.40$	V
Junction temperature		Tj	− 40	—	+ 125	°C

• Dual power supply (V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.2 V ± 0.1 V, V_{SS} = 0 V)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
Power supply voltage		V_{DDE}	3.0	3.3	3.6	V
		V_{DDI}	1.1	1.2	1.3	V
"H" level input voltage	3.3 V CMOS Normal	V_{IH}	2.0	—	$V_{DDE} + 0.3$	V
	3.3 V CMOS Schmitt		2.1	—	$V_{DDE} + 0.3$	V
"L" level input voltage	3.3 V CMOS Normal	V_{IL}	− 0.3	—	+ 0.8	V
	3.3 V CMOS Schmitt		− 0.3	—	+ 0.7	V
Schmitt hysteresis voltage		VH	0.2	—	1.4	V
Junction temperature		Tj	− 40	—	+ 125	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

- Dual power supply (V_{DDE} = 3.3 V, V_{DDI} = 1.2 V)
  Measurement conditions : V_{DDE} = 3.3 ± 0.3 V, V_{DDI} = 1.2 V ± 0.1 V, V_{SS} = 0 V, Tj = − 40 °C to + 125 °C

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
"H" level output voltage	V_{OH}	3.3 V output I_{OH} = -100 µA	V_{DDE} − 0.2	—	V_{DDE}	V
"L" level output voltage	V_{OL}	3.3 V output I_{OL} = 100 µA	0	—	0.2	V
Input leakage current	IL	VI = 0 V or VI = V_{DDE}	− 10	—	+ 10	µA
Pull-up resistor	Rpu	V_{IL} = 0 V	—	33	—	kΩ
Pull-down resistor	Rpd	V_{IH} = V_{DDE}	—	33	—	kΩ

■ DESIGN METHODS

Fujitsu Semiconductor's Reference Design Flow provides the following functions that help reduce the development time of large scale, high quality LSIs.

- Statistical Static Timing Analysis (SSTA) improves timing convergence.
- Physical Prototyping enables more accurate estimation of highly reliable designs.
- Layout synthesis with optimized timing is realized by Physical Synthesis Tool.
- High accuracy design environment where drop in power supply voltage, signal noise, delay penalty and crosstalk are considered
- I/O design environment (power line design, assignment and selection of I/Os, package selection) where noise is considered

■ PACKAGES

The CS251 series can use the same packages that were available for the previous series, allowing a smooth transition from previously developed models. For details of delivery times, contact the sales representative.

- FBGA packages
- PBGA packages
- TEBGA packages
- FC-BGA packages

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