ASSP for Power Management Applications

5ch System Power Management IC for LCD Panel with VCOM Regulator

MB39A302

■ DESCRIPTION

MB39A302 is a 5ch system power supply management IC. It consists of 1ch Buck converter, 1ch Boost converter, 2ch charge pump, 1ch LDO, an operational amplifier for VCOM calibration and a gate voltage shaping circuit. The Buck converter is a voltage mode asynchronous converter with integrated switching FET. The Boost converter equips integrated switching FET with voltage mode control. It is most suitable for large size LCD panel power supply.

■ FEATURES

• Power supply voltage range (VIN=V_{INVL}=V_{IN2})	: 8V to14V
• Boost Converter included SW FET (Vs)	: output 20V Max 1.5A Max
• Buck Converter included SW FET (Vlogic)	: output 1.8V to 3.3V 1.1A Max
• Negative charge pump with output voltage feedback (VGL)	: output current 250mA Max
• Positive charge pump with output voltage feedback (VGH)	: output current 250mA Max
• Low dropout regulator (Vref_o)	: output current 60mA Max
• High performance operational amplifier (VCOM)	: output current ±75mA Max, 20MHz Gain bandwidth
• Feedback threshold voltage	: 1.25V ±1% (Vs) : 1.25V ±1% (Vlogic) : 0.25V ±40mV (VGL) : 1.25V ±2% (VGH) : 1.25V ±0.5% (Vref_o)

- Built-in soft-start circuit independent of loading (Vs - programmable, Vlogic, VGL, VGH)
- Excellent line regulation by the feed-forward method (Vs, Vlogic)
- Built-in output over voltage protection (Vs, Vlogic)
- Built-in output under voltage and short circuit protection (Vs, Vlogic, VGL, VGH)
- Built-in current limit protection (Vs - programmable, Vlogic, Vref_o, OPO)
- Built-in external p-channel gate control for Vs sequencing
- Integrated gate voltage shaping circuitry with adjustable turn on delay
- Built-in under voltage lock out protection function
- Built-in over temperature protection
- Selectable 500kHz/750kHz switching frequency
- Package: QFN-48 Exposed PAD

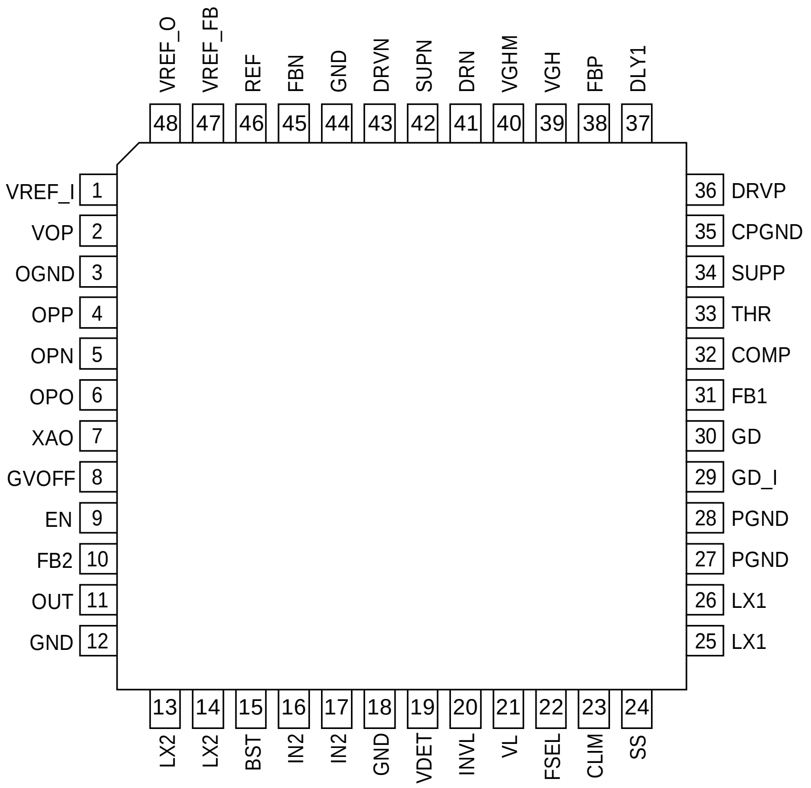
■ APPLICATIONS

Power supply of LCD panel for TV and monitor

2012.6

■ PIN ASSIGNMENTS

(TOP VIEW)



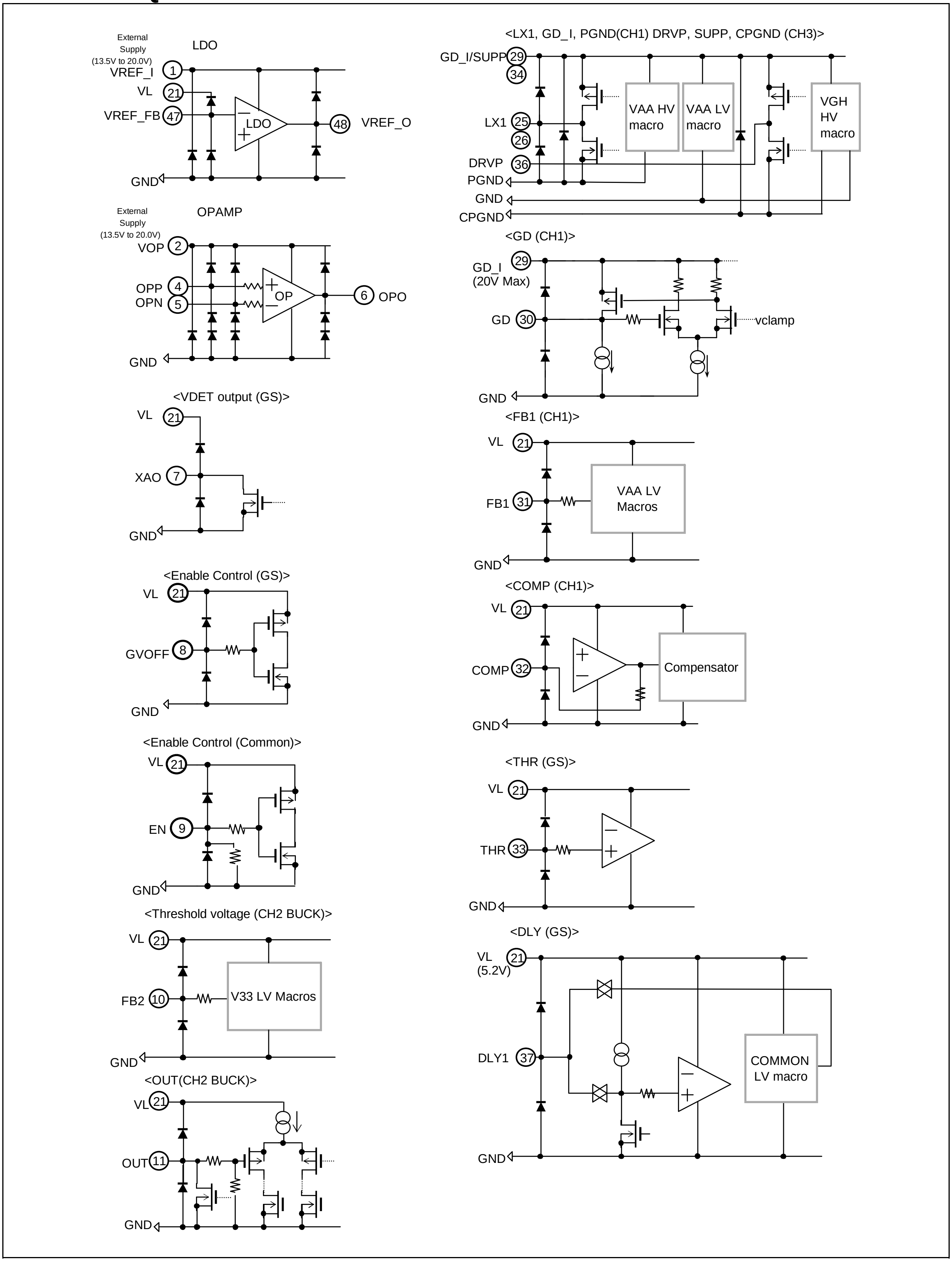
(LCC-48P-M11)

■ PIN DESCRIPTION

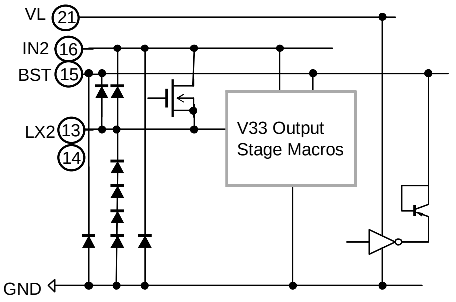
Block	Pin No.	Pin Name	I/O	Description
Vs (Boost DC/DC)	23	CLIM	I	Boost converter current limit setting pin
	24	SS	I	Boost converter soft start timing control pin
	25	LX1	O	Boost converter inductor connection pin
	26	LX1		
	29	GD_I	I	External isolation PMOS source terminal connection and VGH supply pin
	30	GD	O	External isolation PMOS gate terminal connection pin
	31	FB1	I	Boost converter Error Amp input pin
	32	COMP	O	Boost converter frequency compensation pin
Vlogic (Buck DC/DC)	10	FB2	I	Buck converter Error Amp input pin
	11	OUT	I	Buck converter regulated output sense pin
	13	LX2	O	Buck converter inductor connection pin
	14	LX2		
	15	BST	I/O	Buck converter gate drive boot pin
VGL (Negative Charge Pump)	42	SUPN	O	V_{GL} power supply decoupling capacitor connection pin
	43	DRVN	O	V_{GL} external pumping capacitor connection pin
	45	FBN	I	V_{GL} Error Amp input pin
	46	REF	O	Reference voltage output pin
VGH (Positive Charge Pump)	36	DRVP	O	V_{GH} external pumping capacitor connection pin
	34	SUPP	O	V_{GH} power supply decoupling capacitor connection pin
	38	FBP	I	V_{GH} Error Amp input pin
Gate Voltage Shaping	39	VGH	I	Gate shaping circuit high voltage input pin
	40	VGHM	I/O	Gate voltage shaping circuit output pin
	41	DRN	I/O	Gate voltage shaping discharge slope adjustment pin
	8	GVOFF	I	Gate voltage shaping circuit control pin
	33	THR	I	Gate voltage shaping circuit output lower limit control pin (10xTHR)
	37	DLY1	I	Time delay control pin for gate voltage shaping circuit
Vref_o (LDO)	47	VREF_FB	I	LDO feedback input pin
	48	VREF_O	O	LDO output pin
VCOM (OPAMP)	4	OPP	I	VCOMP OPAMP non-inverting input pin
	5	OPN	I	VCOMP OPAMP inverting input pin
	6	OPO	O	VCOMP OPAMP output pin
Misc.	21	VL	O	Internal 5.2V regulator output pin
Control Pin	7	XAO	O	Open drain output of power supply detection circuit
	9	EN	I	5.2V rated Boost converter enable pin
	19	VDET	I	Power supply detection input pin
	22	FSEL	I	Switching frequency select pin

Block	Pin No.	Pin Name	I/O	Description
Power	1	VREF_I	I	VREF LDO supply pin
	2	VOP	I	VCOMP OPAMP supply pin
	16	IN2	I	Buck converter and VGL power supply pin
	17	IN2	I	Buck converter and VGL power supply pin
	20	INVL	I	Common and Internal 5.2V regulator supply pin
	27	PGND	-	High Current Boost Ground pin
	28	PGND	-	
	35	CPGND		VGH Ground pin
	44	GND		Analog ground pin
	3	OGND	-	VCOM OPAMP ground pin
	12	GND	-	Analog ground pin
	18	GND	-	Analog ground pin

■ I/O PIN EQUIVALENT CIRCUIT DIAGRAM



<IN2, LX2 (CH2)>Note: IN2=SUPN (see pin42 for other connectivity)



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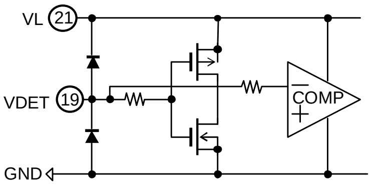

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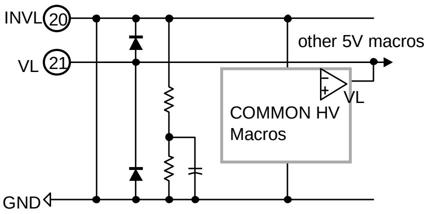

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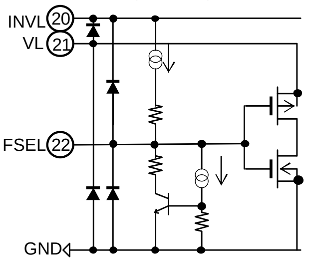

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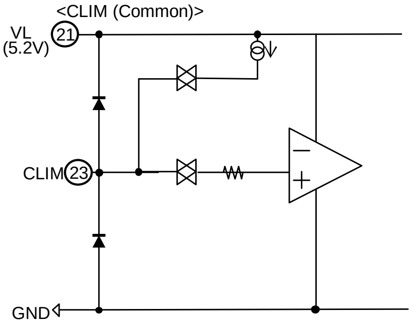

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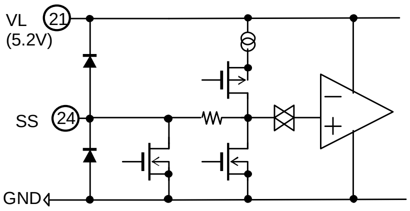

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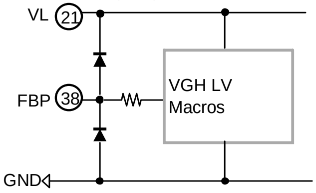
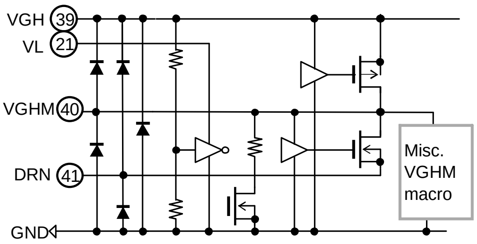
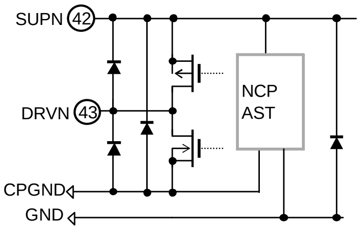


<VGH, VGHM, DRN (GS)>



<SUPN, DRVN (CH3)>Note: IN2=SUPN (see pin16 for other connectivity)



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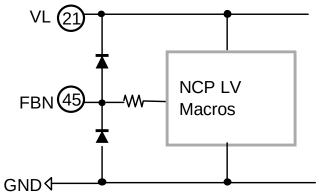

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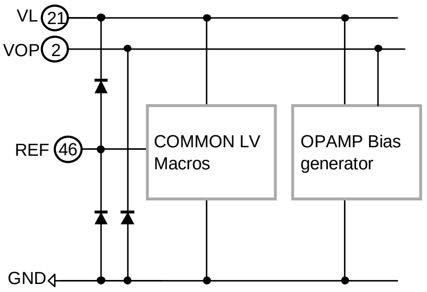
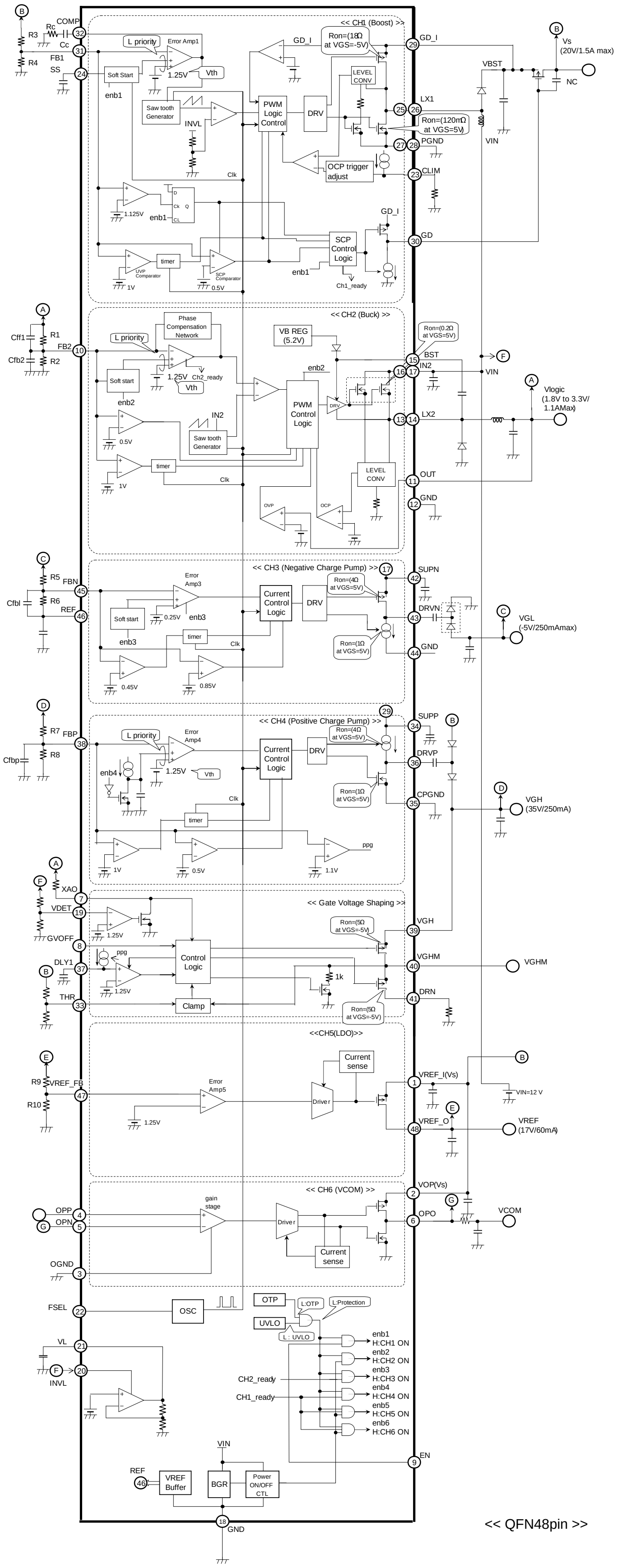


■ BLOCK DIAGRAM



■ FUNCTIONAL DESCRIPTIONS

CH1 (Vs): Boost Converter

The Boost converter features fixed frequency pulse width modulated (PWM) control with integrated NMOS power switch. The switching frequency can be set to either 500 kHz or 750 kHz via the FSEL pin. The converter operates as an asynchronous Boost converter with external Schottky diode. The use of voltage mode control with input feed forward improves line regulation performance. In addition, the converter is designed with external frequency compensation that allows flexibility on selecting external component values. A PMOS switch with on resistance of 18Ω connects between LX1 and GD_I pin so that it operates in parallel with the external Schottky diode. At high loading current, most of the inductor current flows through the external Schottky diode. At light load, the PMOS switch provides a conduction path that allows the inductor current flow in reverse direction. As a result, the converter stays in continuous conduction mode for most of the load current range and allows the use of simple frequency compensation scheme.

Soft Start (Boost Converter)

The build in soft start circuit limits the inrush current at start up. The soft start cycle starts after EN is asserted and the duration can be set by user through the capacitor connected to SS pin.

(1) When SS pin capacitor value > 220pF, soft start time is set externally. Charging current is 5μA and trigger threshold is 1.25V.

(2) When SS pin capacitor value < 220pF or SS pin is open, soft start time is fixed internally at 10ms.

Protection (Boost Converter)

The Boost converter has built in over voltage protection to prevent MB39A302 from being damaged due to excessive voltage stress under fault conditions such as FB1 pin is left floating or short to ground. The protection circuitry monitors the Boost converter output via GD_I pin and shut down the NMOS power FET that connects to LX1 pin when the voltage on GD_I pin is higher than 21.5V. As a result, the inductor current starts to fall and the output of the Boost converter follows. The Boost converter resumes normal operation when the voltage at GD_I pin falls below the protection threshold.

The Boost converter has built in under voltage protection and short circuit protection to prevent MB39A302 from damage due to low voltage stress under fault conditions. The protection circuitry monitors the Boost converter output via FB1 pin and the Under Voltage Protection activates when the voltage on FB1 pin is lower than 1V and the NMOS power FET will be shut down after 50ms. The Short Circuit Protection will activate when the voltage of FB1 pin is lower than 0.5V and the NMOS power FET will be shut down immediately.
In addition, Boost converter has programmable over current protection that turns off the power FET to prevent excessive output current from damaging internal IC and external components.

Gate Drive Pin (GD)

GD pin voltage is pulled down by 10μA (Typ) internal current source after EN pin is asserted. The external PMOS turns on and connects the cathode of the Boost converter Schottky catch diode to the Boost converter load capacitors when GD falls below the turn-on threshold of the external PMOS. When VGD reaches VGD_I-6V, the Boost converter regulator is enabled and initiates a soft-start routine. Startup SCP protection is included to protect external PMOS from permanent damage in the event that Boost output is initially shorted to GND upon power up. When not using this feature, leave GD high impedance and connect GD_I to the output of the Boost converter.

CH2 (V_{logic}): Buck Converter

The Buck converter is a fixed frequency PWM control asynchronous converter with integrated NMOS power switch. It features voltage mode control with input feed forward to improve line regulation performance. The main switch of the converter is a 3.2A rated power NMOS with gate drive circuit reference to LX2 pin (source terminal of the NMOS power FET). The gate drive circuit is powered from an internal 5V regulator and is bootstrapped from LX2 pin via an external capacitor to achieve driving capability beyond the supply rail.

Soft Start (Buck Converter)

The build in soft start circuit limits the inrush current at start up. The soft start cycle start after power supply is asserted and the duration is internally set to 3ms.

Protection (Buck Converter)

The Buck converter has built in over voltage protection to prevent MB39A302 from being damaged due to excessive voltage stress under fault conditions such as FB2 pin is left floating or short to ground. The protection circuitry monitors the Buck converter output voltage via OUT pin and shut down the NMOS power FET that connects to LX2 pin when the voltage on OUT pin is higher than 3.7V. As a result, the inductor current starts to fall and the output of the Buck converter follows. The Buck converter resumes normal operation when the voltage at OUT pin falls below the protection threshold.

The Buck converter has built in under voltage protection and short circuit protection to prevent MB39A302 from damage due to low voltage stress under fault conditions. The protection circuitry monitors the Buck converter output voltage via FB2 pin and the Under Voltage Protection activates when the voltage on FB2 pin is lower than 1V and the NMOS power FET will be shut down after 50ms. The Short Circuit Protection will activate when the voltage of FB2 pin is lower than 0.5V and the NMOS power FET will be shut down immediately.

In addition, Buck converter has over current protection that turns off the power FET to prevent excessive output current from damaging internal IC and external components.

CH3 (V_{GL}): Negative Charge Pump

The negative charge pump uses fixed switching frequency controlled architecture. The output voltage is set externally by a resistor divider. Regulation is done by controlling the pump current in the driver. The charge pump uses external diodes, pumping capacitor and output filter capacitor. Since the input of the charge pump and the driver is connected to the supply pin (VIN), the maximum negative output voltage is -VIN +Vloss. Vloss includes voltage drop in external diodes and gate driver. Additional charge pump stage can be added to generate larger negative voltage.

Protection (Negative Charge Pump)

The negative charge pump has built in under voltage protection and short circuit protection. The protection circuitry monitors the charge pump output voltage via FBN pin and the Under Voltage Protection activates when the voltage on REF-FBN pin is lower than 0.8V and the power FETs will be shut down after 50ms. The Short Circuit Protection will activate when the voltage of REF-FBN pin is lower than 0.4V and the power FETs will be shut down immediately.

CH4 (V_{GH}): Positive Charge Pump

The positive charge pump uses fixed switching frequency controlled architecture. The output voltage is set externally by a resistor divider. Regulation is done by controlling the pump current in the driver. The charge pump uses external diodes, pumping capacitor and output filter capacitor. The input of the charge pump is connected to the VS (Boost converter output) and the pump capacitor is charged to VS during charging phase. As the supply to the driver (SUPP pin) can be either the VS (Boost converter output) or the VIN (Power supply) of MB39A302, the maximum output voltage is VSUPP + VS - Vloss. Vloss includes voltage drop in external diodes and gate driver. Additional charge pump stage can be added to increase the maximum output voltage.

Protection (Positive Charge Pump)

The positive charge pump has built in under voltage protection and short circuit protection. The protection circuitry monitors the charge pump output voltage via FBP pin and the Under Voltage Protection activates when the voltage on FBP pin is lower than 1V and the power FETs will be shut down after 50ms. The Short Circuit Protection will activate when the voltage of FBP pin is lower than 0.5V and the power FETs will be shut down immediately.

CH5 (V_{ref_o}): Low Dropout regulator (LDO)

The integrated low noise low drop out regulator (LDO) is available with 60mA current capability. It has built in over current protection circuit to prevent the LDO from being damaged under fault conditions. This LDO can be stable with 1μF to 10μF output ceramic capacitor.

CH6 (OPO): VCOM Operational Amplifier

The integrated low input offset voltage operational amplifier (OP Amp) is available with ±75mA current capability. It can be stable with 3Ω to 10Ω load resistor in series with 1μF to 150μF output capacitor. There is also built in over current protection to prevent this amplifier from being damaged under fault conditions.

Gate Voltage Shaping

The ability to control the falling edge of the gate drive signal is essential for reduction of flicking on LCD display. The gate voltage shaping circuit provides timing and slew rate control for the gate drive signal and an isolation switch to protect circuit powered from VGH.

Upon initial startup, VGHM output stays low until after XAO is released (pulled low), VGH reached power good and the capacitor on DLY1 pin past 1.25V. Then, VGHM would be dictated by the logic level on GVOFF and the cut threshold dictated by THR pin voltage. After this, if XAO is pulled low, then VGH and VGHM are shorted together as long as there is enough supply voltage to maintain the circuit operation.

XAO

XAO is an open-drain output that externally connects through a resistor to Vlogic. Upon startup, XAO follow VLOGIC output. When VLOGIC and VGL reaches 90% of its final output, XAO control is passed to VDET pin. When VDET sense that VIN is below desired voltage (defined by external resistor divider), XAO is pulled low immediately.

Common Block

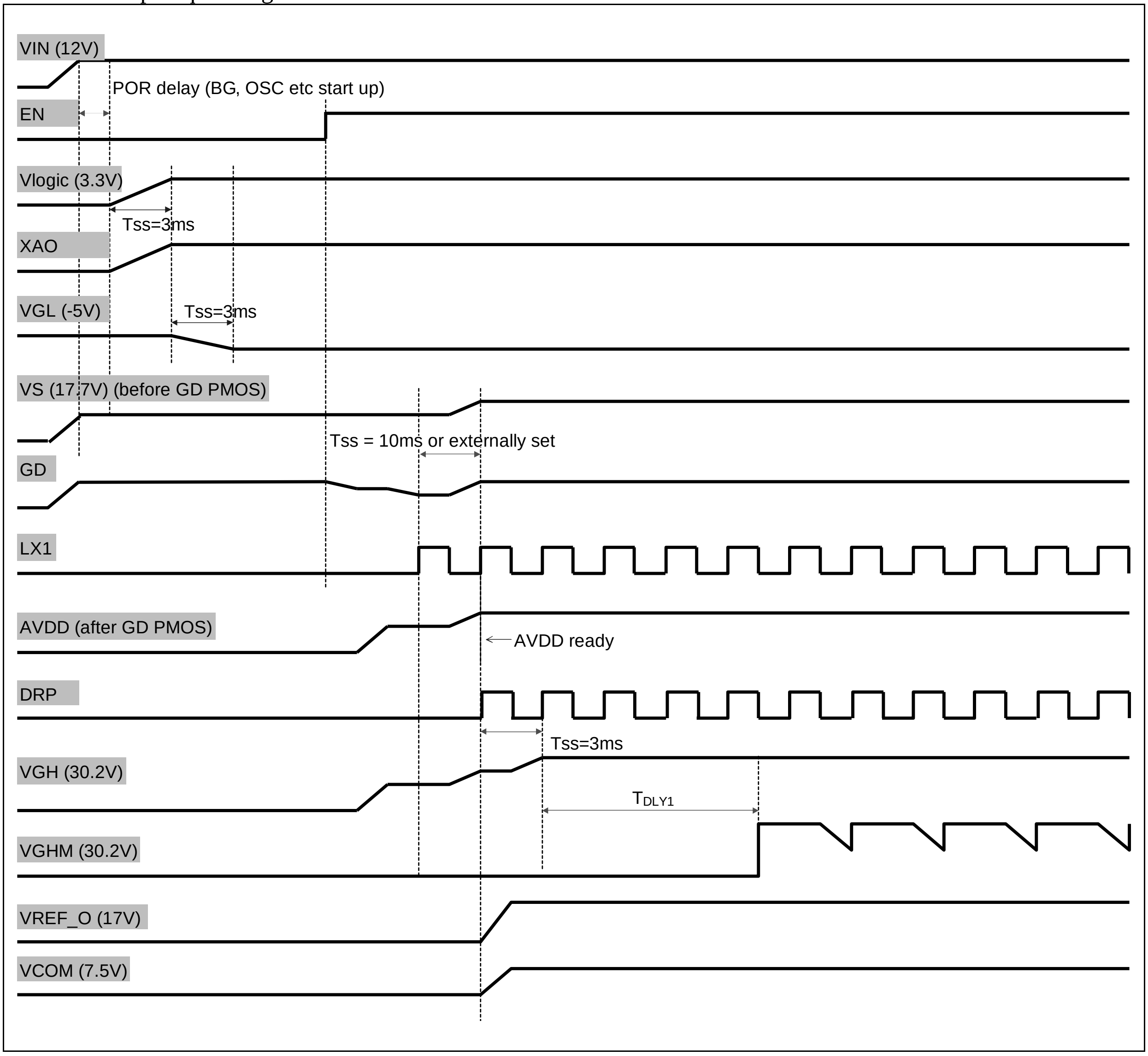
Under Voltage Lockout Protection

MB39A302 will shutdown when the supply voltage below 6V to prevent improper operation of the device.

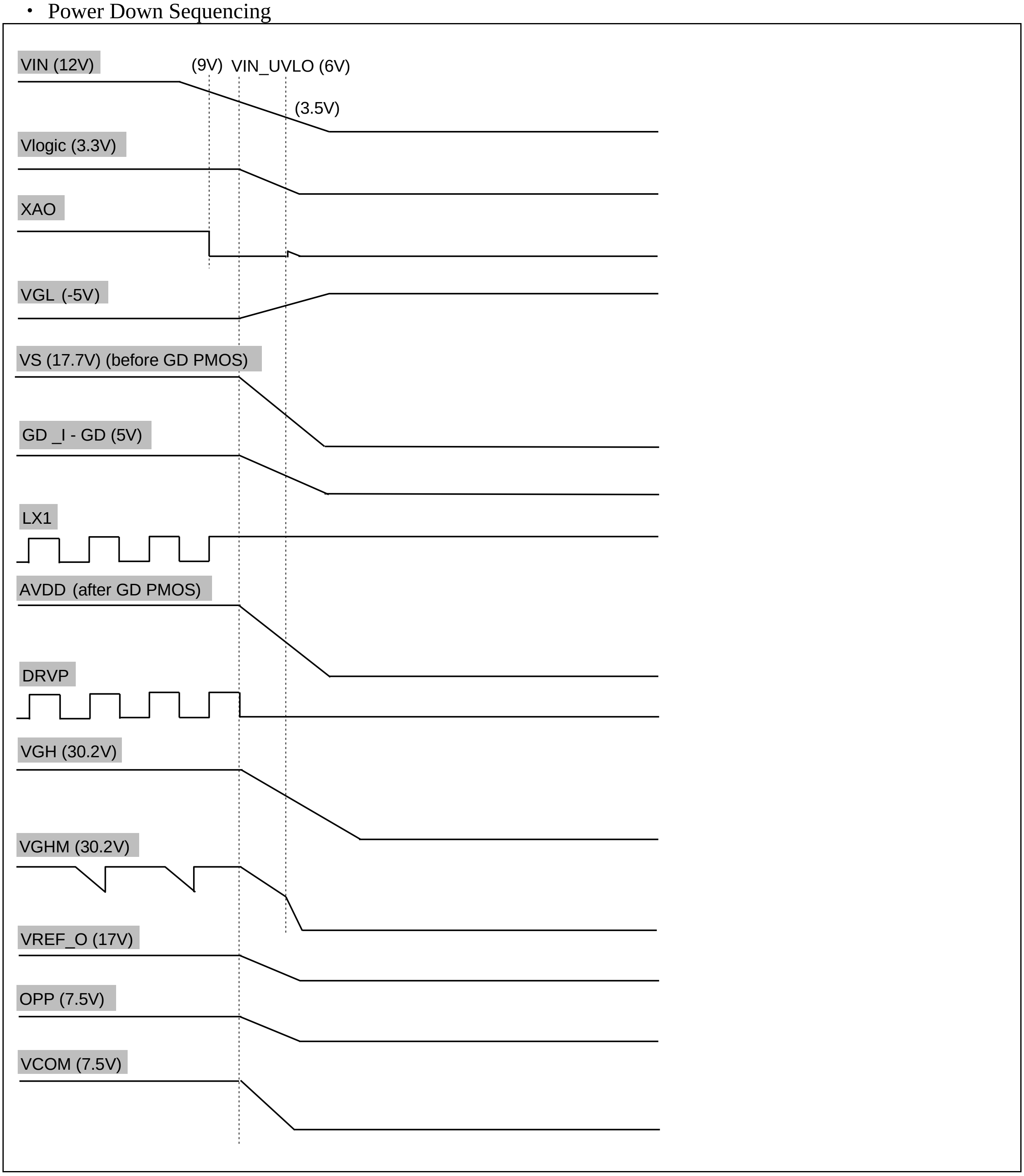
Over Temperature Protection

When the junction temperature rises above +150°C, most of the active circuitries are shutdown to prevent damage from excessive power dissipation beyond safety limits.

- Power Up Sequencing



- Power Down Sequencing



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating		Unit
			Min	Max	
Power supply voltage	VDD	IN2, INVL	-0.3	+20	V
	VBOOT	BST	-0.3	+25	V
	AVDD	SUPP, VREF_I, VOP	-0.3	+25	V
Input/Output voltage	VLV_IN	CLIM, SS, FB1, FB2, FBN, FBP, GVOFF, THR, DLY1, VREF_FB, EN, VDET, OUT	-0.3	+5.5	V
	VLV_OUT	COMP, REF, XAO, VL	-0.3	+5.5	V
	VHV_IN	FSEL	-0.3	+20	V
	VGL_OUT	DRVN	-0.3	+20	V
	VGH_OUT	DRVP	-0.3	+25	V
	VGH	VGH	-0.3	+40	V
	VGS	VGHM, DRN	-0.3	+40	V
	VREFO	VREF_O	-0.3	+20	V
	VOPP	OPP	-0.3	+25	V
	VOPN	OPN	-1	+25	V
	VOPO	OPO	-1	+25	V
	SUPN	SUPN	-0.3	+20	V
	VGD	GD, GD_I	-0.3	+25	V
SW voltage	VLX	LX1	-0.3	+25	V
	VLX	LX2	-2	+20	V
SW peak current	ILX	LX1 AC	-	4.2	A
	ILX	LX2 AC	-	3.9	A
Power dissipation	PD	Ta ≤ +85°C	-	1.51	W
Storage temperature	TSTG	-	-55	+125	°C

*: When mounted on a 100mm ×100 mm: 4 layer (2S2P JEDEC).
θja: 26.5°CW^{-1}, θjc: 0.5°CW^{-1}

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power supply voltage	VIN	IN2, INVL, SUPN	8	12*[1]	14	V
	VBOOT	BST	-	-	19	V
	VSUP	SUPP, VREF_I, VOP	8	-	20	V
Input voltage	VSS	SS, DLY1	0	-	5	V
	VTHR	THR	0	-	5	V
	VILIM	CLIM	0	-	5	V
	VFB	FB1, FB2, FBN, FBP, VREF_FB, OUT	0	-	5	V
	VGD	GD, GD_I	0	-	20	V
	VEN	EN, GVOFF	0	-	5	V
	VFSEL	FSEL	0	-	20	V
	VGH	VGH	0	-	37	V
	VCOM	OPP, OPN	0	-	20	V
	VXAO	VDET	0	-	3.7	V
Output voltage	VO1	V_S: Boost DC/DC	-	17.7	-	V
	VO2	V_{LOGIC}: Buck DC/DC	-	3.3	-	V
	VO3	VGL	-	-5.5	-	V
	VO4	VGH, VGHM	-	30	-	V
	VO5	VREF_O: LDO (Io = 1mA to 60mA)	-	17	-	V
	VO6	OPO: Opamp (Io = 1mA to 25mA)	-	7.5	-	V
	VOX	XAO	0	-	5	V
Output current	IO1	V_S: BOOST DC	0	-	1.5*[2]	A
	IO2	V_{LOGIC}: BUCK DC	0	-	1.1	A
	IO3	VGL DC	-	0.1	0.25*[3]	A
	IO4	DRN pin Peak	-0.25	-	-	A
	IO4	VGH DC	-	0.1	0.25*[4],*[5]	A
	IO5	Vref DC: VREF_O	0.5	-	60	mA
	IO6	VCOMP DC: OPO	-75	-	75	mA
	IO6	VCOMP AC: OPO	-200	-	200	mA
	IGD	GD	-	10	-	µA
	IGDI	GD_I (light load)	-100	-	100	mA
	IDRVN	DRVN	-500	-	500	mA
	IDRVP	DRVP	-500	-	500	mA
REF pin output current	IREF	REF	-50	-	0	µA
SW inductor	LX1	LX1	-	6.8	-	µH
	LX2	LX2	-	10	-	µH
BOOT pin capacitor	CBOOT	BST	0.01	0.10	1.00	µF
SUPP pin capacitor	CSUPP	SUPP	-	1	-	µF
GD pin capacitor	CGD1, CGD2	GD	-	10	-	µF
DRP, DRN pins capacitor	CDRV	DRVP, DRVN	-	0.47	-	µF
SUPN pin capacitor	CSUPN	SUPN	-	1	-	µF
REF pin capacitor	CREF	REF	-	1	-	µF
VL pin capacitor	CVL	VL	-	1	-	µF

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
INVL pin capacitor	CINVL	INVL	-	1	-	µF
VREFI pin capacitor	CVREFI	VREFI	-	1	-	µF
VOP pin capacitor	CVOP	VOP	-	1	-	µF
IN2 pin capacitor	CIN2	IN2	10	40	70	µF
CLIM pin resistor	RCLIM	CLIM	60	-	-	kΩ
V_S output filter capacitor	Cout1	V_S: Boost DC/DC	-	60	-	µF
V_{LOGIC} output filter capacitor	Cout2	V_{LOGIC}: Buck DC/DC	-	2×10	-	µF
VGL output filter capacitor	Cout3	NCP	1	-	20	µF
VGH output filter capacitor	Cout4	PCP	0.47	-	10.00	µF
VGHM output capacitor	Cscan	In series with Rscan	1	-	1000	nF
LDO output filter capacitor	Cout5	VREF_O: LDO	1	4.7	10	µF
VCOMP output filter capacitor	Cout6	In series with Rout	1	10	150	µF
VGHM output resistance	Rscan	VGHM	-	1.61	-	kΩ
VGHM output resistance	Rdrn	DRN	200	-	3000	Ω
VCOMP output filter resistance	Rout6	In series with Cout	3	-	10	Ω
Charge/Discharge cycle frequency	Fscan	-	40	-	70	kHz
Discharge duration	Tdscan	-	1	-	10	µs
Operating ambient temperature	Ta	-	-30	+25	+85	°C

*1: Performance is guaranteed for 12V±10%

*2: Maximum current is only guaranteed if OCP is not triggered. ILIM> Vo1 × Io1max/VIN + VIN × (Vo1-VIN) /L/fosc/Vo1/2
For: VIN=8V, Iomax=1A, VIN=10V, Iomax=1.2A, VIN ≥ 12V, Iomax=1.5A

*3: Maximum current is only guranteed if VIN-|Vo3|>Rdsonmax (Hiside + Loside) × 2 × Imax + 2 × Vdiode + Imax / (fosc × Cpump) (for doubler).
For Vo3 = -5.5V: VIN>12V, Iomax=250mA, VIN=10V, Iomax=150mA, VIN=8V, Iomax=80mA

*4: Maximum current is only guaranteed if 2 × Vo1 - Vo4 > Rdsonmax (Hiside + Loside) × 2 × Imax + 2 × Vdiode + Imax/(fosc × Cpump) (for doubler).
For Vo1=17.7V: Iomax=150mA

*5: Maximum current is only guaranteed if VIN+2 × Vo1 - Vo4 > Rdsonmax (Hiside + Loside) × 4 × Imax + 4 × Vdiode + 3 × Imax/(fosc × Cpump) (for Tripler)

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.
Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.
No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

(Ta=0°C to +85°C, VIN=IN2=INVL=12V, SUPP=VREF_I=VOP=17.7V.
Typical values are at Ta=+25°C unless noted otherwise)

Parameter		Symbol	Pin	Condition	Value			Unit
					Min	Typ	Max	
REF Block [REF]	REF output voltage	REF	46	IREF=0mA	-2%	1.25	+2%	V
	REF load regulation	REF	46	0<IREF<50µA	-	-	15	mV
Under Voltage Lockout Protection Circuit Block [UVLO]	INVL UVLO threshold	UVLOIN	16,17	INVL= ↓	5.3	6	6.7	V
	INVL hysteresis width	INHYS	16,17	-	-	0.5	-	V
	VL UVLO threshold	UVLOVL	21	VL= ↓	3	3.4	3.8	V
	VL hysteresis width	VLHYS	21	-	-	0.5	-	V
Over Temperature Protection Block [OTP]	Stop temperature	TOTPH	-	T junction ↓	-	150*	-	°C
	Hysteresis width	T_{OTPHYS}	-	-	-	20*	-	°C
Control Block [CTL]	Input voltage threshold	VIH	8,9,22	EN, GVOFF, FSEL ON	2	-	-	V
		VIL	8,9,22	EN, GVOFF, FSEL OFF	-	-	0.9	V
	EN pulldown resistance	REN	9	EN	-	800	-	kΩ
	FSEL pullup current	IFSEL	22	FSEL	1.4	2.4	4.0	µA
General	INVL + IN2 quiescent current	IQ	16,17, 20	FB1 = FBP = 1.5V, FBN = 0, EN = VL, FSEL = H (Only LX2 switching)	-	5	-	mA
	INVL + IN2 standby current	ISB	16,17, 20	FB1 = FB2 = FBP = 1.5V, FBN = 0, EN = VL, FSEL = H (No switching)	-	4	-	mA
Oscillator Block [OSC]	Output frequency	fosc	13, 14 25, 26 36, 43	FSEL = "H"	630	750	870	kHz
				FSEL = "L"	420	500	580	kHz
VL Regulator [VL]	VL output voltage	VL	21	IL = 0mA	4.9	5.2	5.5	V
	VL load regulation	VL	21	0 < IVL < 30mA	-	-	300	mV

(Ta=0°C to +85°C, VIN=IN2=INVL=12V, SUPP=VREF_I=VOP=17.7V.
Typical values are at Ta=+25°C unless noted otherwise)

Parameter		Symbol	Pin	Condition	Value			Unit
					Min	Typ	Max	
V_S [Boost DC/DC]	Line regulation	Vline1	29,34	VIN=10.8V to 13.2V	-	-	0.15	%/V
	Load regulation	Vload1	29,34	Io1= 150mA to 1.5A	-1	-	+1	%/A
	Threshold voltage	VTH1	31	FB1	-1%	1.25	+1%	V
	Input bias current	IB1	31	FB1 =0V	-100	0	100	nA
	SW NMOS-Tr On resistance	RON1	25, 26 27, 28	LX1=500mA VGS=5V	-	120	185	mΩ
	SW PMOS-Tr On resistance	RON1	25,26, 29	GD_I=-200mA VGS=5V	-	18	36	Ω
	SW PMOS-Tr Leak current	ILEAK1	29	EN=0V GD_I=15V LX1=0V	-	-	10	µA
	SW NMOS-Tr Leak current	ILEAK1	25,26	EN=0V LX1=15V	-	-	10	µA
	Output OCP threshold	ILIM1	25,26	LX1, RCLIM > 60kΩ	2.8-60.5kΩ/RCLIM	3.5-60.5kΩ/RCLIM	4.2-60.5kΩ/RCLIM	A
	Output UVP threshold	Vuvp1	31	FB1	0.96	1	1.04	V
	Output UVP delay time	Td,uvp1	-	-	42	50	58	ms
	Output OVP threshold	Vovp1	34	SUPP	21	21.5	22	V
	Output SCP threshold	Vscp1	31	FB1	0.4	0.5	0.6	V
	Soft-start time	Tss1	24	SS: CSS>220pF SS charge current	3.8	5	6	µA
				SS: CSS<220pF V(GD)-V(GD_I)> 4V to 95% VO1	-	10	-	ms
	GD clamp voltage	VGD1	29,30	V(GD) - V(GD_I)	-7	-6	-5	V
	GD discharge current	IGD1	30	GD	4	10	16	µA

(Ta=0°C to +85°C, VIN=IN2=INVL=12V, SUPP=VREF_I=VOP=17.7V.
Typical values are at Ta=+25°C unless noted otherwise)

Parameter		Symbol	Pin	Condition	Value			Unit
					Min	Typ	Max	
V_{logic} [Buck DC/DC]	Bootstrap output	VBST	15	FB2=5V	-	4.5	-	V
	Threshold voltage	VTH2	10	FB2	-1%	1.25	+1%	V
	Input Bias current	IB2	10	FB2=0V	-100	0	+100	nA
	SW NMOS-Tr (upper) On resistance	RON2	13,14, 16,17	LX2=0.2A VGS=5V	-	200	300	mΩ
	SW NMOS-Tr (upper) Leak current	ILEAK2	13,14, 16,17	LX2=0V	-10	-	-	μA
	OUT to GND switch on resistance	ROUT	11	OUT	70	125	210	kΩ
	Output OVP threshold	Vovp2	11	OUT DC	3.5	3.7	3.9	V
	Output UVP threshold	Vuvp2	10	FB2	0.96	1.00	1.04	V
	Output UVP delay time	Td, uvp2	-	-	42	50	58	ms
	Output OCP threshold	ILIM2	13, 14	LX2	2.2	3.2	3.9	A
	Output SCP threshold	Vscp2	10	FB2	0.4	0.5	0.6	V
	Load regulation	Vload2	11	Io2=150mA to 1.1A	-	-	0.5	%/A
	Line regulation	Vline2	11	VIN: 10.8 to 13.2V	-	-	0.1	%/V
	Soft-start time	Tss2	10	0 to 99% VO2	-	3	-	ms
V_{GL} [Negative Charge Pump]	Threshold voltage	VTH3	45	FBN	210	250	290	mV
	Input bias current	IB3	45	FBN=0V	-100	0	+100	nA
	SW NMOS-Tr On resistance	RON3	43, 44	Iout=100mA	-	1.5	3	Ω
	SW PMOS-Tr On resistance	RON3	42, 43	Iout=100mA	-	3.5	7	Ω
	Output UVP threshold	Vuvp3	45,46	REF-FBN	0.768	0.800	0.832	V
	Output UVP delay time	Td, uvp3	-	-	42	50	58	ms
	Output SCP threshold	Vscp3	45,46	REF-FBN	0.3	0.4	0.5	V
	Soft start up time	Tss3	45	0% to 95% VO3	-	3	-	ms

(Ta=0°C to +85°C, VIN=IN2=INVL=12V, SUPP=VREF_I=VOP=17.7V.
Typical values are at Ta=+25°C unless noted otherwise)

Parameter		Symbol	Pin	Condition	Value			Unit
					Min	Typ	Max	
V_{GH} [Positive Charge Pump]	Threshold voltage	VTH4	38	FBP	-2%	1.25	+2%	V
	GD_I input supply current	IGDI	29	FBP = 1.5V (not switching)	-	0.4	-	mA
	Input bias current	IB4	38	FBP=0V	-100	0	+100	nA
	SW NMOS-Tr On resistance	RON4	25, 26 27, 28	Iout=100mA	-	1.5	3	Ω
	SW PMOS-Tr On resistance	RON4	25, 26 27, 28	Iout=100mA	-	3.5	7	Ω
	Output UVP threshold	Vuvp4	38	FBP	0.96	1	1.04	V
	Output UVP delay time	Td,uvp4	-	-	42	50	58	ms
	Output SCP threshold	Vscp4	45,46	FBP	0.4	0.5	0.6	V
	Soft start up time	Tss4	38	90% VO1 to 95% VO4	-	3	-	ms

(Ta=0°C to +85°C, VIN=IN2=INVL=12V, SUPP=VREF_I=VOP=17.7V.
Typical values are at Ta=+25°C unless noted otherwise)

Parameter		Symbol	Pin	Condition	Value			Unit
					Min	Typ	Max	
VGHM [Gate Voltage Shaping]	VGH supply current	IVGH	39	GVOFF=0V	-	0.1	-	mA
	Rdson charge	Rchg5	39, 40	Ichg=100mA	-	5	10	Ω
	Rdson discharge	Rdis5	40, 41	Idischg=100mA	-	20	50	Ω
	VGHM to ground discharge resistance	Rvghm	40	DLY1=GND, VGHM=1V	10	14	20	kΩ
	GVOFF to VGHM rise propagation delay	Trise	8,40	RDRN=1k, VGHM noload, GVOFF rising edge to VGHM×0.2	-	60	120	ns
	GVOFF to VGHM fall propagation delay	Tfall	8,40	RDRN=1k, VGHM noload, GVOFF falling edge to VGHM×0.8	-	280	500	ns
	DLY1 charge current	Idly1	37	-	6	8	10	μA
	DLY1 voltage threshold	Vdly1	37	-	1.19	1.25	1.31	V
	Slider Stop Voltage	Vslide5	33	R_{DRN}=1kΩ, R_{scan}=1.6kΩ, C_{scan}=1.3nF	9.4	10	10.6	V/V
	VDET threshold voltage	VDET	19	VDET ↑	1.275	1.300	1.325	V
	VDET hysteresis	VDEThyst	19	VDET	-	50	-	mV
	VDET output voltage	VXAO5	7	VDET = GND, IXAO = 1mA	-	-	0.4	V
	VDET output current	IXAO	7	VDET=1.5V, VXAO=3.3V	-	-	100	nA
VREF [LDO]	VREF_I supply current	IREFI	1	No load, open loop, VFB=1.5V	-	0.15	-	mA
	Line regulation	Vline5	48	VREF_I= 13.5V to 20V	-	0.02	-	%
	Load regulation	Vload5	48	Io=1mA to 30mA	-	0.3	-	%
	Threshold voltage	VTH5	47	VREF_FB	- 0.5%	1.25	+ 0.5%	V
	Drop out voltage	Vload5	48	IO=60mA VREF_I=VREF_O	-	-	500	mV
	PSRR	PSRR5	48	f=50KHz/ 500KHz/750kHz, Io=10mA, 30mA, VREF_I=Vo5+0.7V, Reference to VREF_I	-	40 (50kHz) 50 (500/ 750kHz)	-	dB
	Output SCP protection current	Iscp5	48	VREF_O = 0V	60	100	150	mA

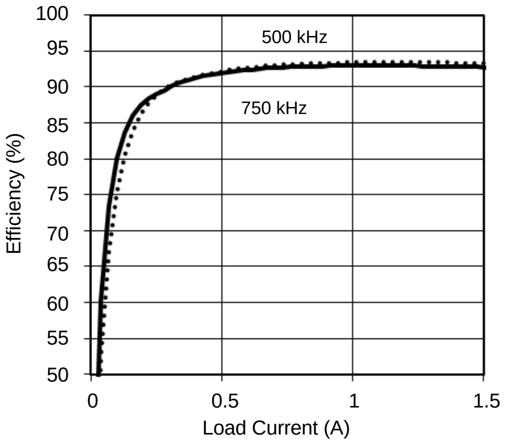
(Ta=0°C to +85°C, VIN=IN2=INVL=12V, SUPP=VREF_I=VOP=17.7V.
Typical values are at Ta=+25°C unless noted otherwise)

Parameter		Symbol	Pin	Condition	Value			Unit
					Min	Typ	Max	
VCOM [VCOMP OPAMP]	VOP supply current	IVOP	2	Buffer configuration, OPP=OPN=VOP/2, no load	-	3	-	mA
	Line regulation	Vline6	6	VOP 13.5V to 20V, OPP=7.5V	-	0.02	-	%/V
	Load regulation	Vload6	6	IOP 1mA to 75mA, OPP=7.5V	-0.4	-	+0.4	%
	Dropout voltage (sinking)	Vdrop6	6	IOP=-10mA	40	90	180	mV
	Dropout voltage (sourcing)	Vdrop6	6	IOP=+10mA	40	90	180	mV
	Unit gain bandwidth (sourcing)	f_{u66}	6	Unit gain configuration Ro=10Ω, Co=0.1µF,Io=75mA, OPP=6V	-	10	-	MHz
	Unit gain bandwidth (sinking)	f_{u66}	6	Unit gain configuration Ro=10Ω, Co=0.1µF, Io=-75mA, OPP=6V	-	20	-	MHz
	PSRR	PSRR6	6	f=50KHz/ 500KHz/750kHz, Io6=10mA,100mA dynamic or Io6=30mA static, VOP=8V, reference to VOP	-	60	-	dB
	Input offset voltage	Vos6	4, 5	OPO = 6 to 9V	-15	-	+15	mV
	Slew rate	Vslew6	-	Ro=10Ω, Co=0.1µF, OPP from 6V ↔ 8V	-	40	-	V/µs
	Output short circuit current	Iscp6	6	OPO	-	±200	-	mA

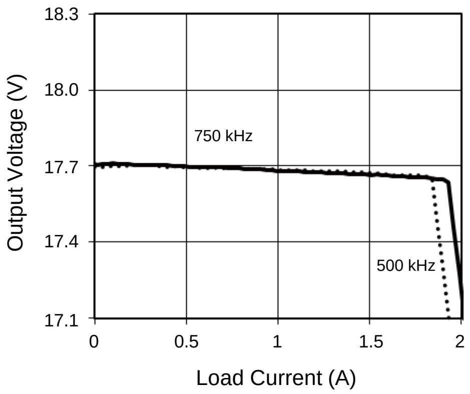
*: Standard design value

■ TYPICAL CHARACTERISTICS

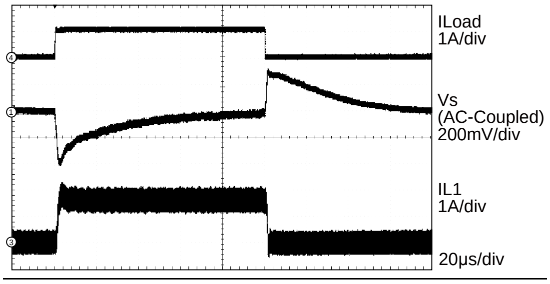
Boost Converter (Vs)



Efficiency vs. Load Current



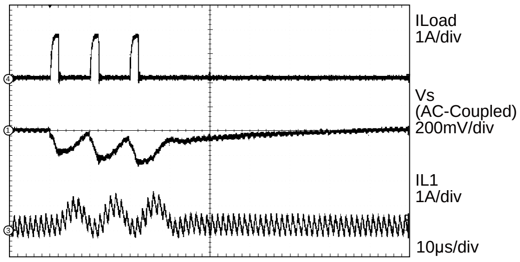
Output Voltage vs. Load Current



Load Transient Response

(Switching Load Current=0.1A to 1.1A)

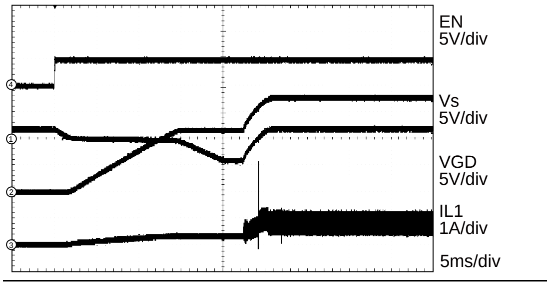
L=6.8µH, Freq=750 kHz



Load Transient Response

(Pulsed Load Current=0.1A to 1.9A)

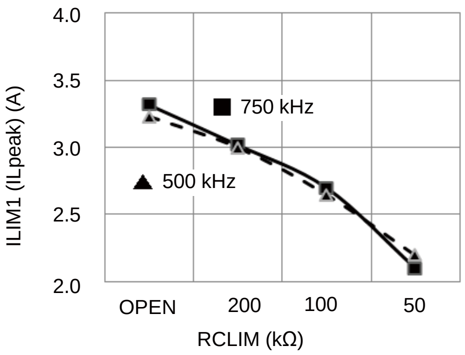
L=6.8µH, Freq=750 kHz



Heavy Load Soft-start

(Load Current=0.5A)

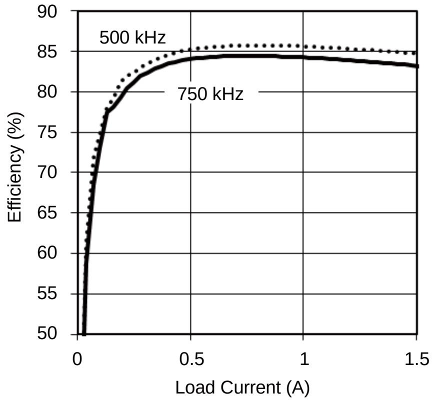
L=6.8µH, C_{SS} =22nF



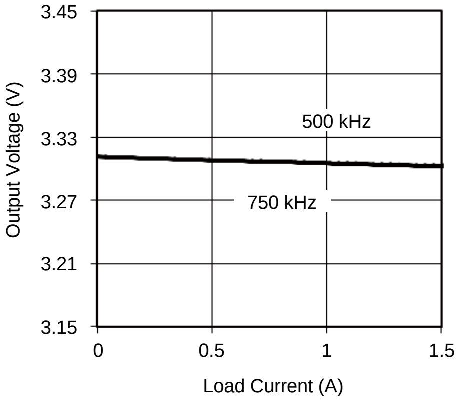
ILIM1 (ILpeak) vs. RCLIM

Buck Converter (Vlogic)

Efficiency vs. Load Current



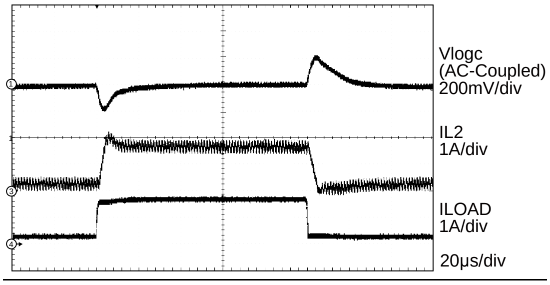
Output Voltage vs. Load Current



Load Transient Response

(Switching Load Current=0.3A to 1.8A)

L=10µH, Freq=750 kHz



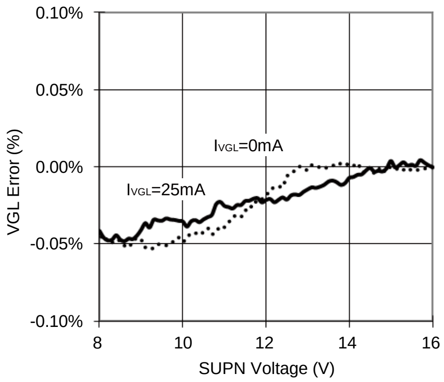
Heavy-load Soft-start

(Load Current=1A)

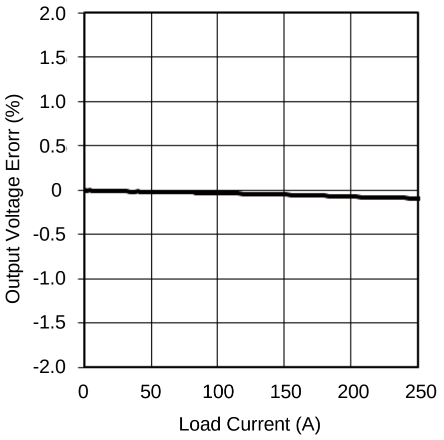
L=10µH, Freq=750kHz

Negative Charge-pump (VGL)

Normalized Line Regulation

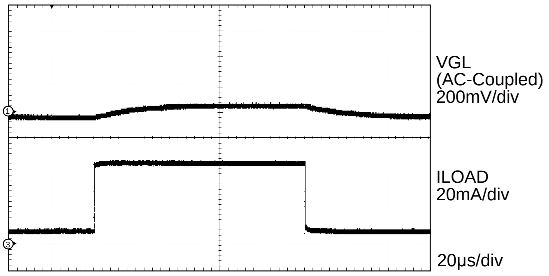


Output Voltage vs. Load Current (VIN = 12V)



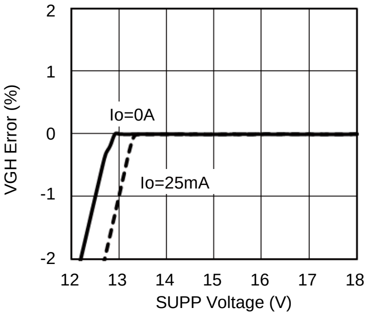
Load Transient Response

(Switching Load Current=10mA to 60mA)



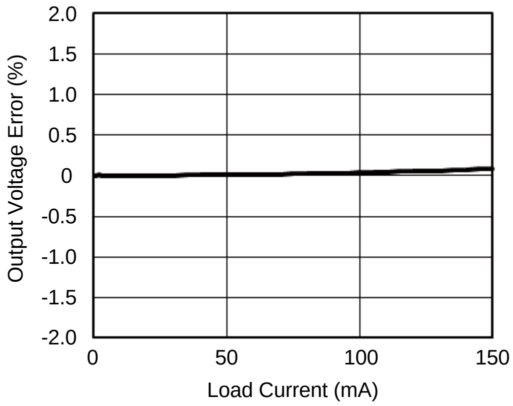
Positive Charge-pump (VGH)

Normalized Line Regulation



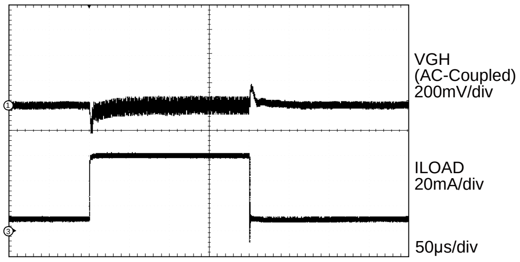
Positive Charge-pump (VGH)

Output Voltage vs. Load Current



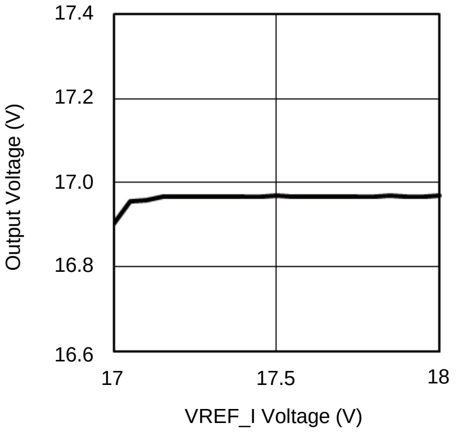
Load Transient Response

(Switching Load Current = 10mA to 60mA)

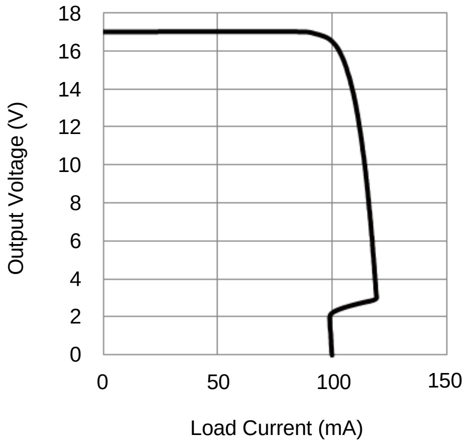


Low Dropout regulator (LDO)

Line Regulation (Load Current=20mA)

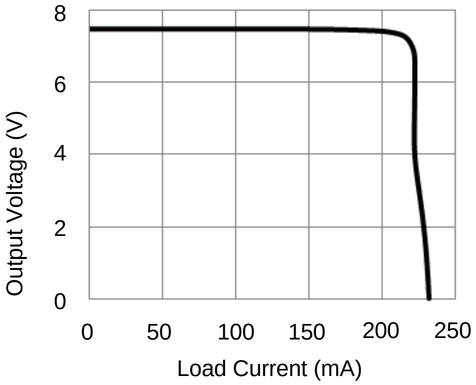


Output Voltage vs. Load Current

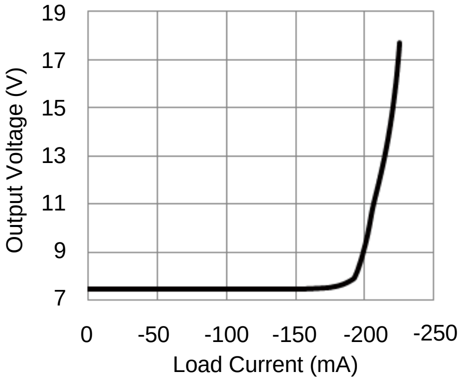


Op-amp (VCOM)

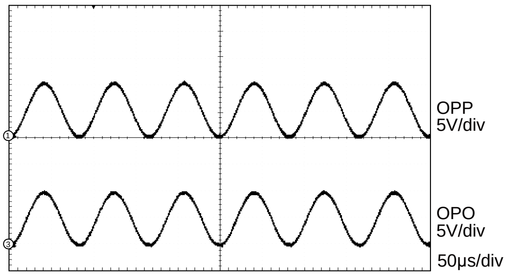
Output Voltage vs. Load Current (Source)



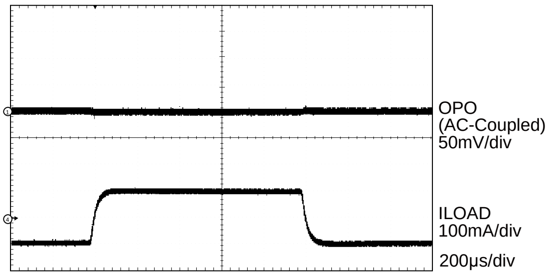
Output Voltage vs. Load Current (Sink)



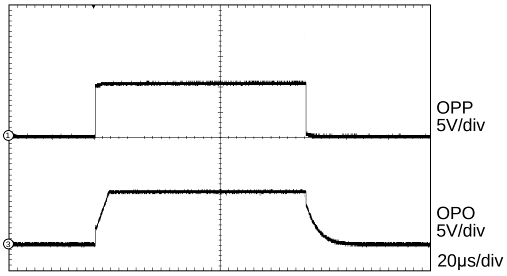
Rail-to-rail Input / Output Waveforms



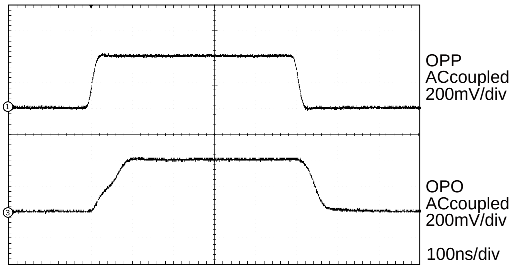
Load Transient Response



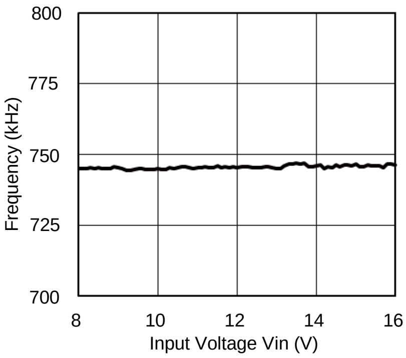
Large-signal Step Response



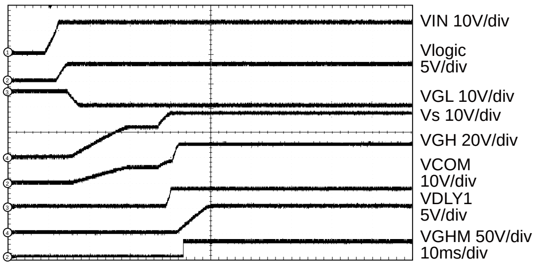
Small-signal Step Response



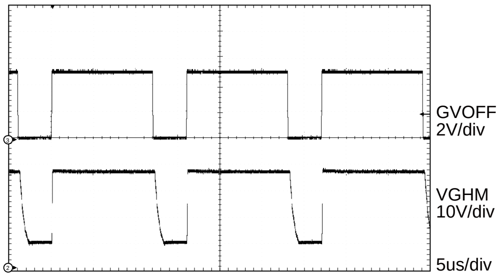
Switching Frequency vs. Input Voltage



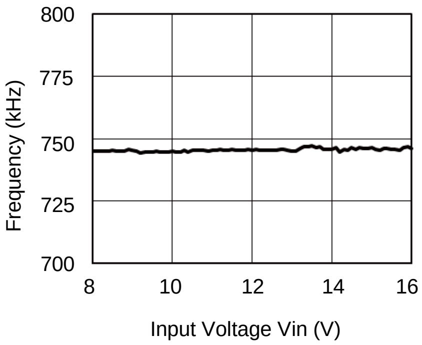
Power-up Sequence of All Supply Outputs



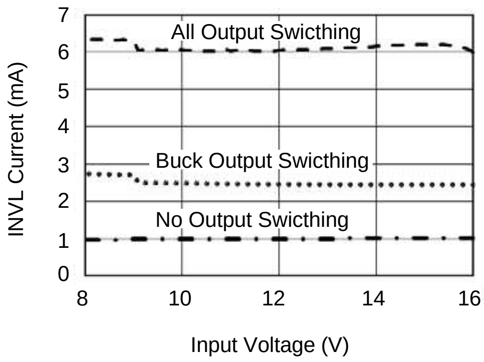
Gate Voltage Shaping (VGHM)
(VGHM with 470pF Load)



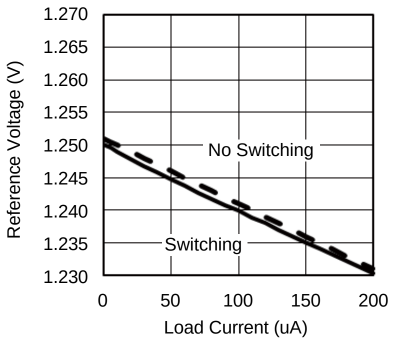
Switching Frequency vs. Input Voltage

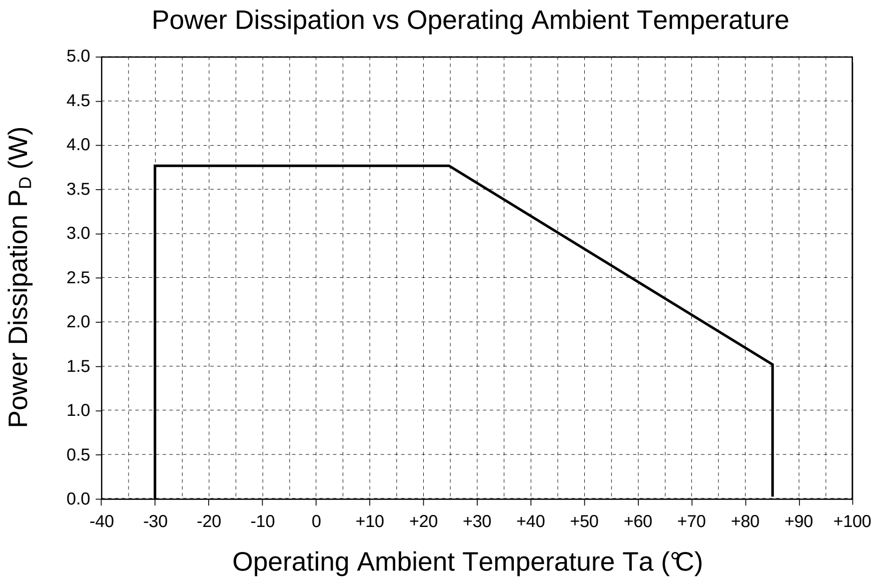


VIN Supply Current vs. VIN Voltage



Reference Voltage Load Regulation




Power Dissipation vs Operating Ambient Temperature
Power Dissipation P_D (W)
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
-40
-30
-20
-10
0
+10
+20
+30
+40
+50
+60
+70
+80
+90
+100
Operating Ambient Temperature Ta (℃)

■ SETUP

1. Setting Control Pin

Pin	Channels	Standby	operating
IN2, INVL	V_{logic}: Buck Converter V_{GL}: Negative Charge Pump	L	>6V
EN	V_S: Boost Converter V_{GH}: Positive Charge Pump VREF_O: LDO OPO: VCOMP OP	L	H

2. Setting Switching Frequency

Pin	Setting	Internal oscillator frequency
FSEL	H/Float	750kHz
	L	500kHz

3. Protection Circuitry

(1) IC

Under voltage lock out protection: VIN ≤ 6V, all circuits shut down
Over temperature protection: Junction Temp > +150°C, all circuits shut down

(2) V_S: Boost converter

Over voltage protection: GD_I pin ≥ 21.5V, protection circuit active
Over current protection: threshold value is set by user
Short circuit protection: FB1 pin voltage < 1V for 50ms or FB1 pin voltage < 0.5V, protection circuit active. Boost, VGH, VGL are turned off (stop switching) immediately. External GDFET open.
Startup short circuit protection: If VS short to ground before power on, IC would trigger protection as VIN is pulled low and disable all channels immediately

(3) V_{LOGIC}: Buck converter

Over voltage protection: OUT > 3.7V, protection circuit active
Over current protection: ILX2 > 3.2A, protection circuit active
Short circuit protection: FB2 pin voltage < 1V for 50ms or FB2 pin voltage < 0.5V, protection circuit active. Buck, Boost, VGH, VGL are turned off (stop switching) immediately. External GDFET open.

(4) V_{GL}: Negative Charge Pump

Short circuit protection: REF-FBN voltage < 0.8V for 50ms or REF-FBN voltage < 0.4V, protection circuit active. Boost, VGH, VGL are turned off (stop switching) immediately. External GDFET open.

(5) V_{GH}: Positive Charge Pump

Short circuit protection: FBP pin voltage < 1V for 50ms or FBP pin voltage < 0.5V, protection circuit active. Boost, VGH, VGL are turned off (stop switching) immediately. External GDFET open.
Power down: When XAO is pulled low, VGHM is shorted to VGH internally.

(6) V_{REF_O}: LDO

Short current protection: Io > 100mA, protection circuit active.

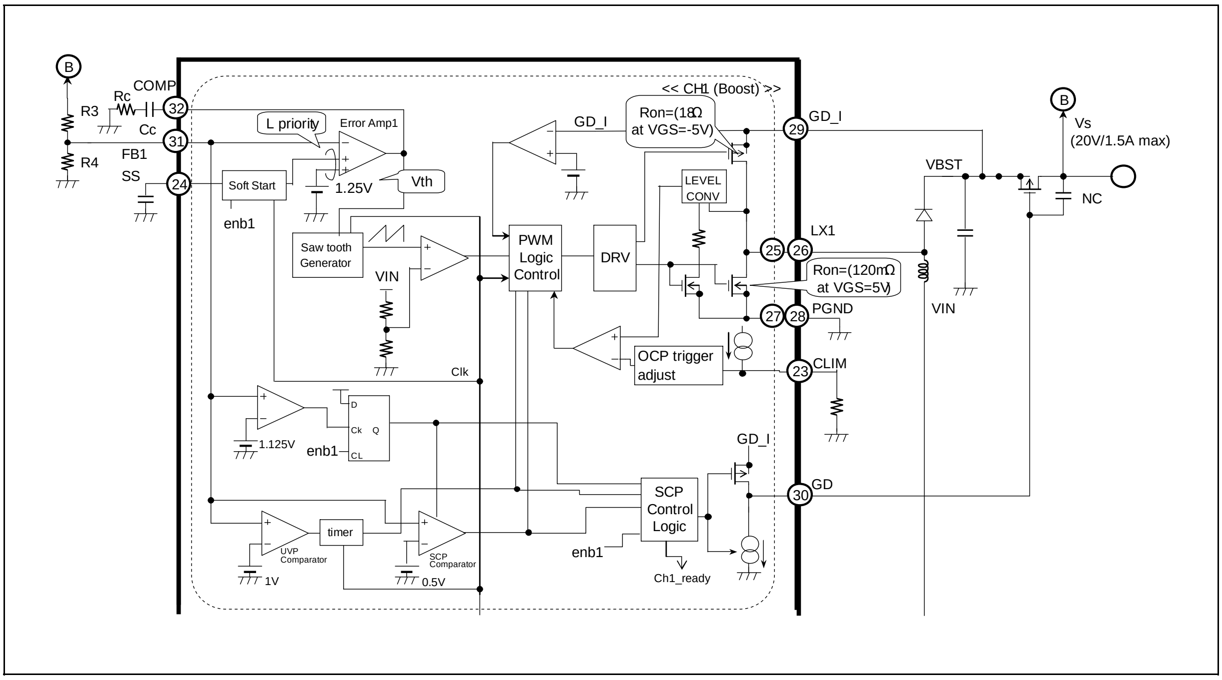
(7) V_{COM}: VCOMP OP

Over current protection: Io > 200mA, protection circuit active.

■ APPLICATION NOTE

Boost Converter Design

- Boost Converter Block Diagram



Output voltage selection

The Boost converter output voltage V_S can be set by external resistor divider as below:

$$V_S = 1.25 \times \left(1 + \frac{R3}{R4}\right)$$

Feedback resistor

Resistor values R3 and R4 do not have direct impact on compensation. However, to minimize noise pickup on FB1 without degrading light load efficiency, it is recommended that the equivalent values be set around 100kΩ.

Compensation (COMP) Capacitor Selection

The regulator compensation is adjusted by an external component connected to the COMP-pin. This pin is the output of internal trans-conductance error amplifier. By adding a resistor in series will change the internal zero to achieve a stable mid-frequency gain. The formula below give the frequency (Fz) at which the resistor increases the high-frequency gain.

$$F_Z = \frac{1}{2 \times \pi \times C_C \times (R_C + 115k)}$$

For 6.8µH inductor & 60µF output capacitor, we recommend using Cc=680pF and Rc=30kΩ, resulting in fz = 1.5kHz.

Over current protection selection

The Over current protection for the Boost converter limits the maximum switching current I_{SWMAX}. The current limit value can be programmed by an external resistor RCLIM.

$$ILIM1 = 3.5 - \frac{60.5k}{RCLIM}$$

When RCLIM is open, the OCP will set to ILIM1=3.5A. It is recommended that RCLIM be > 60kΩ.

Peak inductor current

It is necessary to verify the maximum output current of this converter whether it meets the application requirements. The efficiency of the Boost converter can be read from the graph or employ a worst-case assumption of 80%.

Duty cycle: $D = 1 - \frac{V_{in} \times \eta}{V_s}$

Maximum output current: $I_{Smax} = (1\text{-}D) \times \left(I_{SWLIM} - \frac{V_{in} \times D}{2 \times f_{osc} \times L}\right)$

$$= \frac{V_{in}}{V_s} \times \left(I_{SWLIM} - \frac{V_{in} \times D}{2 \times f_{osc} \times L}\right)$$

Peak switching/inductor current: $I_{SWMAX} = \frac{V_{in} \times D}{2 \times f_{osc} \times L} + \frac{I_{Smax}}{1\text{-}D}$

Where
D = Duty cycle
fosc = Switching frequency [Hz] (500kHz or 750kHz)
L = Inductor value [H]
η = Estimated Boost converter efficiency (typically 80% minimum)
I_{SWLIM} = Minimum switch current limit of LX1-pin [A] (= 2.8A)

I_{Smax} = Maximum output current possible under minimum switch current limit of LX1-pin [A]
The selected components, including the embedded switch, the inductor and external Schottky Diode must be able to handle the peak switching current. The estimation should be based on the minimum input voltage, since the switching current will be the highest in this case.

Inductor Selection

Typical inductor value is 6.8µH. When selects the inductor, chooses an inductor that has saturation current higher than the peak switch current (I_{SWMAX}) as calculated below. Extra margin is required to cope with high current transients. A more conservative design is to use the maximum SW current limit of 4.2A as saturation current rating of inductor. Another parameter for choosing inductor is the DC resistance. Usually, lower the DC resistance can result in higher converter efficiency.

Rectifier Diode Selection

Schottky diode should be used to attain high efficiency. The reverse voltage rating of the diode must be higher than the maximum output voltage of the converter. The required averaged rectified forward current of the Schottky diode is the product of off-time of Boost converter and the maximum switch current at LX1 pin. The peak rectifier forward current is the same as inductor peak current, I_{swmax}, determined above.

Off-time of Boost converter: $D' = 1 - D = \dfrac{V_{in}}{V_s}$

Average rectifier forward current: $I_{Dmax} = I_{smax} \times D'$

The rectifier diode selected must have average current rating exceeding I_{Dmax} and repetitive peak current rating exceeding I_{swmax}. A Schottky diode with maximum rectified forward-current of 2A should be sufficient for most applications. Another requirement for Schottky diode is the power dissipation. The power dissipation can be calculated from the formula below:

$$P_D = I_{DMAX} \times V_F = (1-D) \times \left(I_{SWLIM} - \frac{V_{in} \times D}{2 \times f_{osc} \times L}\right) \times V_F$$

Where
P_D = Power dissipation of the diode [W]
V_F = Diode forward voltage [V]
I_{SWLIM} = Minimum over current protection of LX1-pin [A] (3A)

Output Capacitor Selection

Capacitors with low ESR are recommended. Ceramic capacitor which has low ESR is particularly suitable for this purpose. Typically, six 10µF ceramic capacitors connected in parallel are placed at the converter output. More capacitance can be added so as to reduce voltage drop during heavy load transients.

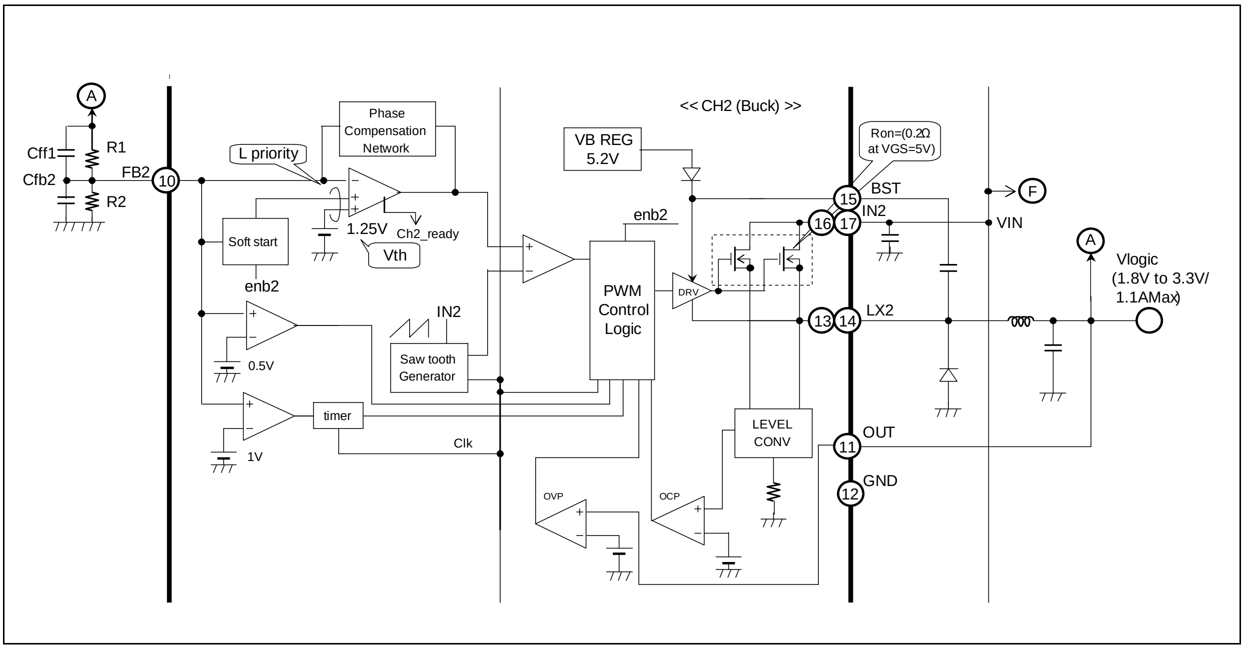
Soft Start Capacitor Selection

SS pin capacitor is used for defining the soft start time of Boost converter. The Boost converter soft start time, Tss, is determined by the user when SS pin capacitor value, Css, is higher than 220pF. And the Boost converter soft start time is determined internally when SS pin capacitor value is lower than 220pF or SS pin is open and fixed at 10ms.

$C_{SS} \leq 220pF$	$T_{SS} = 10ms$
$C_{SS} > 220pF$	$T_{SS} = C_{SS} \times 1.25/5u$

Buck Converter Design

- Buck Converter Block Diagram



Output voltage selection

The Buck converter output voltage V_{logic} can be set by external resistor divider as below:

$$V_{logic} = 1.25\times\left(1+\frac{R1}{R2}\right)$$

Softstart

Internal preset.
The soft start starts after internal POR and UVLO checks are completed and the duration is set to 3ms.

Rectifier Diode Selection

Schottky diode should be used to attain high efficiency. The reverse voltage rating of the diode must be higher then the maximum output voltage of the converter. The required averaged rectified forward current of diode is the product of off-time of Buck converter and the maximum switch current at SWB pin.

Off-time of Buck converter: $D' = 1-\frac{V_{out}}{V_{in}} = 1-D$

Maximum output current: $I_{avg} = (1-D)\times I_{SWLIM} = (1-\frac{V_{in}}{V_{out}})\times I_{SWLIM}$

A Schottky diode with maximum rectified forward-current of 1.5A to 2A should be sufficient for most of applications. The diode forward voltage should be less than 0.7V in order to prevent damage to IC. Another requirement for Schottky diode is the power dissipation. The power dissipation can be calculated from the formula below:

$P_D = I_{avg}\times V_F = (1-D)\times I_{SWLIM}\times V_F$

Where
P_D = Power dissipation of the diode [W]
V_F = Diode forward voltage [V]
I_{SWLIM} = Minimum over current protection of SWB-pin [A] (2.5A)

Feedforward capacitor selection

A feed forward capacitor (Cff1) is added parallel to the upper resistor (R1). The Cff1 sets a zero in the transfer function. This will improve the load transient response and stabilize the converter loop. The value of Cff1 is depending on the value of output inductor and capacitor used.

For 10µH inductor & 20µF output capacitor, a double pole, f_{LC}, is formed at 11 kHz. For stability, a zero, fz, is recommended to be placed at approximately 70% of f_{LC} = 8 kHz;

$$C_{ff} = \frac{1}{2 \times \pi \times R1 \times f_Z} = \frac{1}{2 \times \pi \times 2k\Omega \times 8kHz} = 9.9nF \approx 10nF$$

A capacitor value close to the calculated value is chosen.

A small capacitor to ground, Cfb2, can be added to FB2 node to filter out high frequency noise on the FB2 node. Ensure the low pass filtering pole formed by this R2 and Cfb2 is >> 200 kHz to not impact system stability.

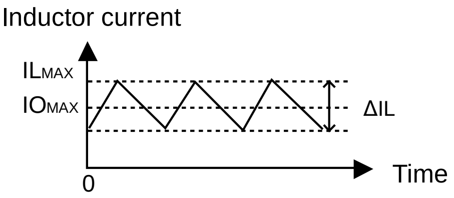
Inductor Selection

Typical inductor value is 10µH. The current flow through the inductor must be below the saturation current rating of the inductor. The maximum current flowing through the inductor can be found from the following formula:

$$IL_{MAX} \geq IO_{MAX} + \frac{\Delta IL}{2}$$

$$\Delta IL = \frac{V_{in} - V_{out}}{L} \times \frac{V_{out}}{V_{in} \times f_{osc}}$$

Where:
IL_{MAX} = Maximum current through inductor [A]
IO_{MAX} = Maximum load current [A]
ΔIL = Inductor ripple current peak-to-peak value [A]
Vin = Input voltage [V]
Vout = Output voltage [V]
fosc = Switching frequency [Hz] (500kHz or 750kHz)



Bootstrap Capacitor Selection

Bootstrap capacitor connected to BST pin is charged by integrated synchronous diode with 4.5V internal supply. Ceramic capacitor is recommended for less leakage current.

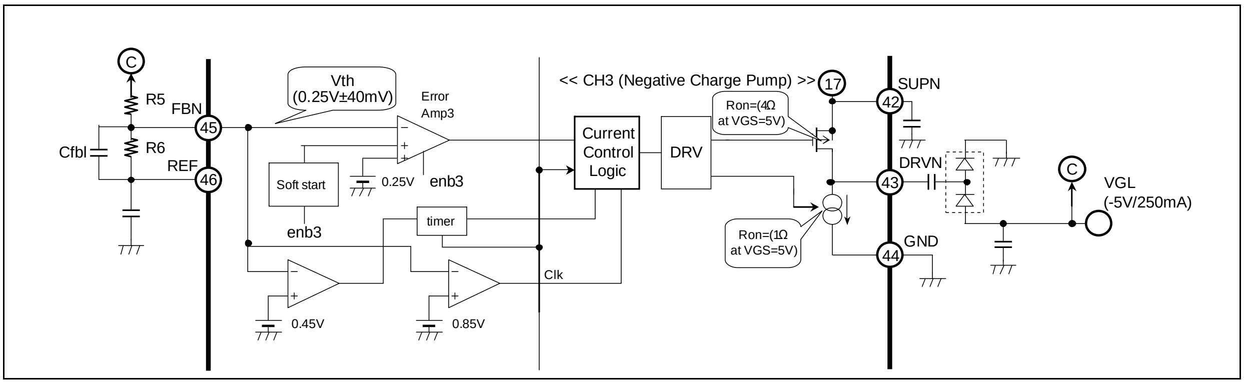
0.1μF bootstrap capacitor is recommended for Buck converter in MB39A302. The bootstrap capacitor voltage rating is suggested to be higher than input voltage.

Output Capacitor Selection

This IC is designed to work best with ceramic output capacitor. Two 10μF ceramic output capacitors are recommended for most application. More capacitance can be added so as to reduce voltage drop during load transients.

Negative Charge Pump Design

- Negative Charge Pump Block Diagram



Output Voltage Selection

Recall from functional description, the maximum negative output voltage is - VDRN + 2Vdiode ideally, which is -12V + 0.8V = -11.2V. Similar to Positive Charge Pump, the regulated output voltage can be set by equation below:

$$V_{GL}= 0.25 - \frac{R5}{R6}$$

Pumping Capacitor and Output Capacitor Selection

Selection of pumping capacitor and output capacitor are similar to Positive Charge Pump design.

For -5V output, $\Delta V_{DRN} = |-V_{GL}| - V_{diode} = 5V - 0.4V = 4.6V$. The pumping capacitor and output filtering capacitor can be estimated for required application.

The minimum pumping capacitor is determined by following equation.

$$C \geq \frac{I_{out}}{f \times \Delta V_{DRN}} ,$$

Where:
Iout = The output current
f = Switching frequency (750kHz/500kHz)
ΔV_{DRN} = Pumping clock voltage

The charge stored on pumping capacitor is transferred to output capacitor cycle-by-cycle. Output capacitor determines output ripple voltage of charge pump. The ripple voltage is estimated by:

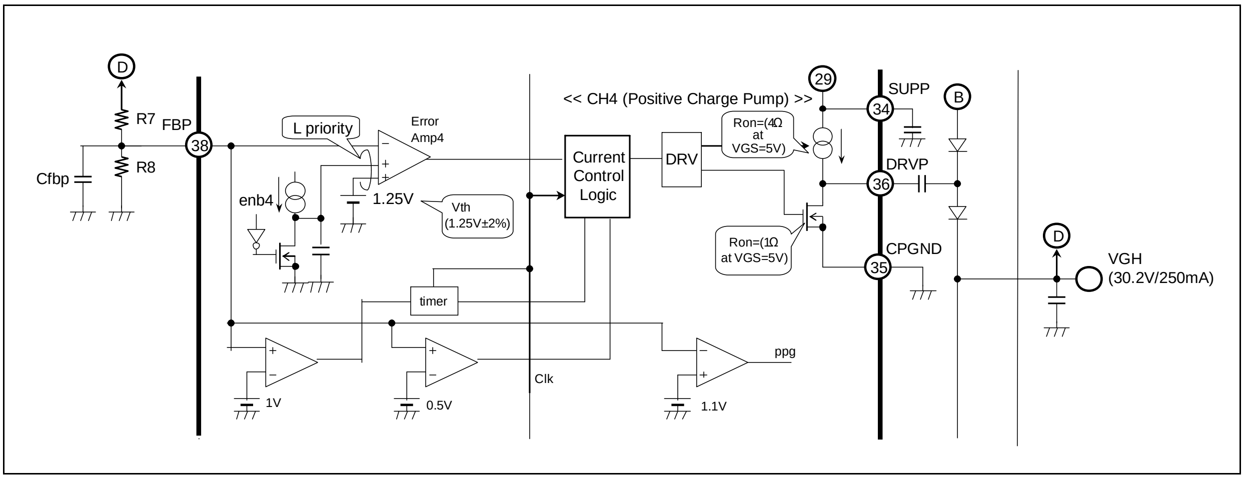
$$V_{ripple} = \frac{I_{out}}{2f \times C_{out}} + I_{out} \times ESR_{Cout}$$

Where:
Cout=Output filtering capacitance
ESRCout = Equivalent series resistance of output filtering capacitor

A small capacitor, Cfbl, can be added between FBN and REF node to filter out high frequency noise on the FBN node. A 22pF capacitor is suitable for most applications.

Positive Charge Pump Design

- Positive Charge Pump Block Diagram



Output Voltage Selection

Theoretically, the maximum output voltage is the sum of input voltage and pumping clock voltage of a charge pump. In MB39A302, the maximum output voltage is VS (Boost converter output voltage) + VSUP - 2Vdiode which is 17.7V + 17.7V – 2 (0.4V) = 34.6V with typical setting. Due to the regulated voltage control, the output voltage can be configured by equation below:

$$V_{GH} = V_{ref} \times \left(1 + \frac{R7}{R8}\right) = 1.25 \times \left(1 + \frac{R7}{R8}\right)$$

Pumping Capacitor and Output Capacitor Selection

Ceramic capacitor is recommended for its non-polarized, more stable over temperature, low leakage and small ESR. Choosing a pumping capacitor should consider the required voltage rating and output current loading. For 30.2V output voltage setting, the pumping clock voltage is calculated below.

$\Delta V_{DRP} = V_{GH} - V_S + V_{diode} = 30.2V - 17.7V + 0.4V = 12.9V$

The minimum pumping capacitor is determined by following equation.

$$C \geq \frac{I_{out}}{f \times \Delta V_{DRP}} \quad ,$$

Where:
Iout = The output current
f = Switching frequency (750kHz/500kHz)
ΔV_{DRP} = Pumping clock voltage

The charge stored on pumping capacitor is transferred to output capacitor cycle-by-cycle. Output capacitor determines output ripple voltage of charge pump. The ripple voltage is estimated by:

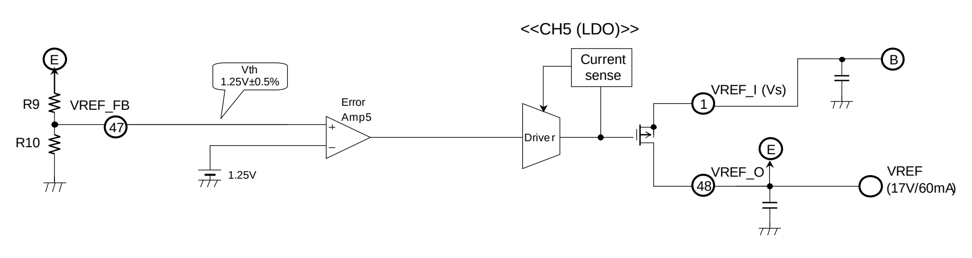
$$V_{ripple} = \frac{I_{out}}{2f \times C_{out}} + I_{out} \times ESR_{Cout}$$

Where:
Cout = Output filtering capacitance
ESR_{Cout} = Equivalent series resistance of output filtering capacitor

A small capacitor, Cfbp, can be added between FBP and GND node to filter out high frequency noise on the FBP node. A 22pF capacitor is suitable for most applications.

Low Dropout Regulator Design (LDO)

- Low Dropout Regulator Block Diagram



MB39A302 includes a voltage regulator (Low Dropout Regulator, LDO) to supply the Gamma Buffer with a very stable voltage. The LDO is designed to operate typically with a 4.7μF ceramic output capacitor (any value between 1μF and 10μF works properly) and a ceramic bypass capacitor of minimum 1μF on its input VREF_I connected to ground. The output of the Boost converter VS is usually connected to the input VREF_I. The LDO has an internal soft-start feature to limit the inrush current.

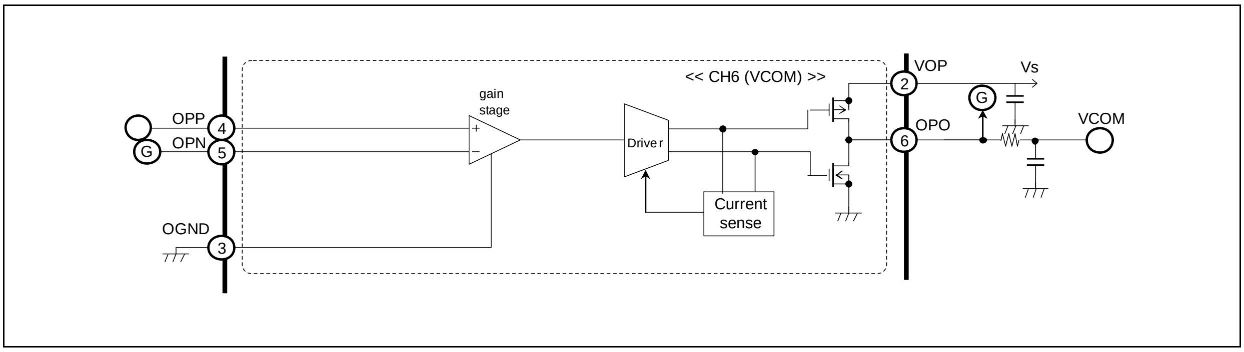
Output voltage selection

The Boost converter output voltage can be set by external resistor divider as below:

$$V_{ref\_o} = 1.25 \times \left(1 + \frac{R9}{R10}\right)$$

VCOM Operational Amplifier

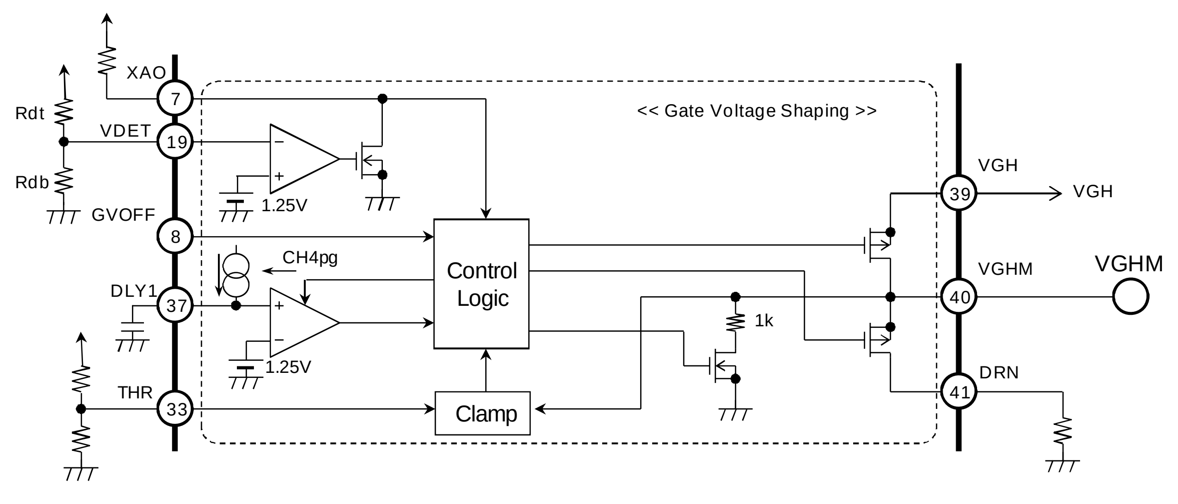
- VCOM Operational Amplifier Block Diagram



The operational amplifier use Vs for power supply, to get better performance and smaller output noise, a 1μF filter ceramic capacitor should be placed between VOP and GND. The input pin OPP can either feed by a resistor divider from VREFO or an external voltage reference. This operational amplifier is optimized to drive the LCD backplane (VCOM), so it is not stable to drive a pure capacitor load, but series a 3 to 10 Ω small resistor with the load capacitor will provide the stable operation.

VGHM: Gate Voltage Shaping

- Gate Voltage Shaping Block Diagram



DLY1 Capacitor Selection

Refer to "Power Up Sequence" section, GateShape block power up sequence timing is set by capacitor at DLY1 pin. The delay capacitor can be estimated by following equation.

$$C_{delay} = \frac{8\mu A \times t_{delay}}{V_{ref}}$$

Where:
t_{delay} = Delay time
C_{delay} = Capacitor connected to DLY1-pin
V_{ref} = 1.25V

XAO

The XAO threshold, VINpg, can be set via a VIN resistive divider connecting to on the VDET pin.
If we select Rdb in the 10kΩ to 50kΩ range, then Rdt can be determined as:

$$\frac{Rdt}{Rdb} = \frac{VINpg}{1.25V} - 1$$

where VINpg is the desired XAO threshold level. Note that Rdt and Rdb should be placed close to the IC.

XAO pin is open drain. Please ensure it is pull up to 3.3V or 5.2V supply.

VDET pin threshold voltage is 1.25V typically. When using Gate voltage shaping and XAO output, please set $1.25V < V_{DET} < 3.7V$.

When not using Gate voltage shaping and XAO output, please set VDET pin to ground.

Others

Input capacitor Selection

It is recommended to use low ESR capacitor like ceramic capacitor for the input filtering. For INVL terminal, a 1µF capacitance connected from INVL to ground is needed. For the Buck converter, use typically four 10µF and one 0.1uF ceramic capacitors connected from IN2 pin to ground.

Output capacitor Selection

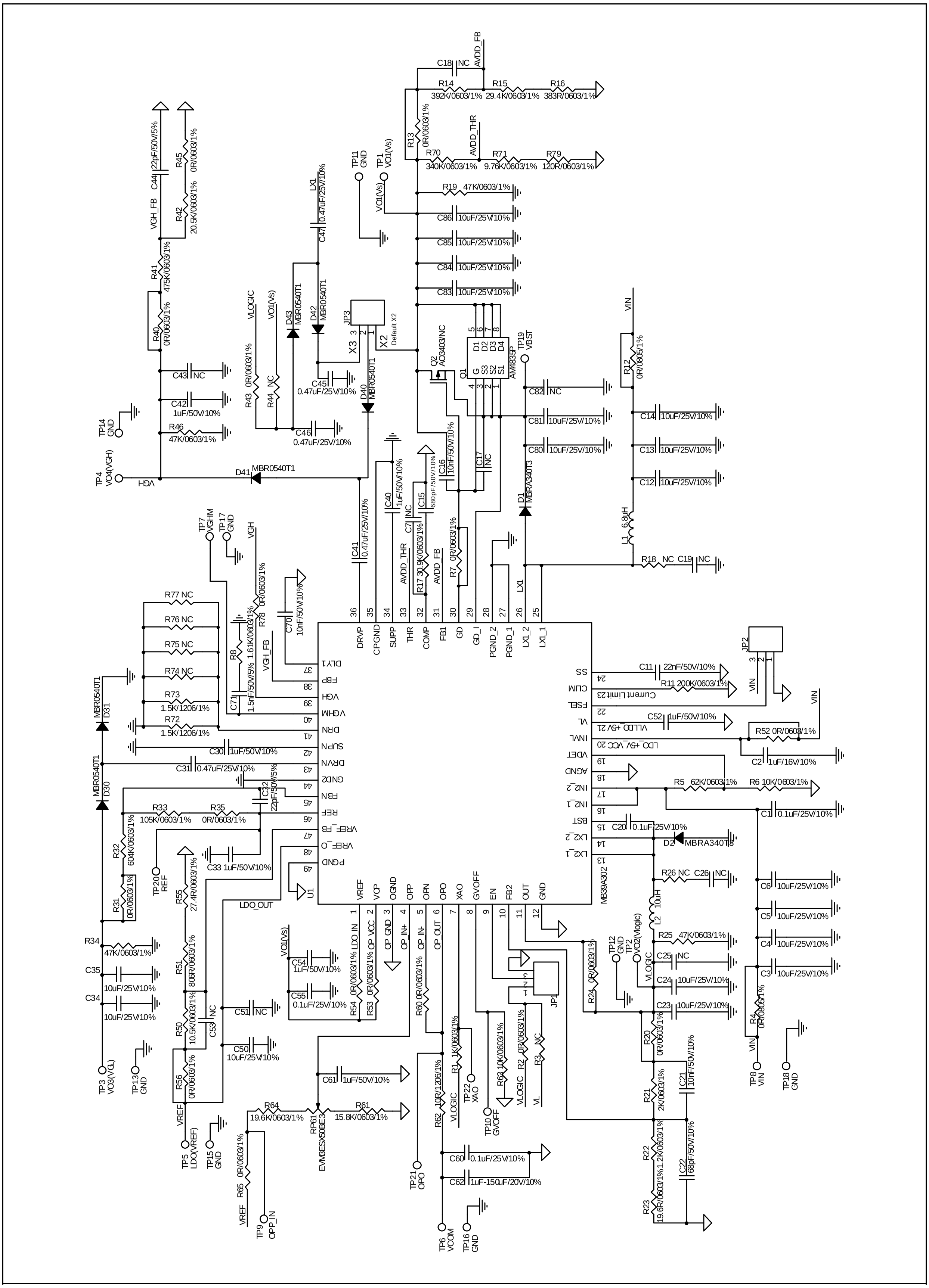
Similarly, ceramic capacitors are recommended. For VL pin, a 1µF capacitance connected from VL to ground is recommended. For REF pin, a 1µF capacitance connected from VL to ground is recommended.

PCB Layout Recommendation

PCB layout is significant for power supply design. Poor layout would result in generating unwanted voltage and current spikes. This will not only affect DC output voltage, but also radiate EMI to adjacent equipment. Sufficient grounding and minimize parasitic inductance can reduce DC/DC converter switching spike noise.

■ CIRCUIT DIAGRAM

MB39A302 EVB-01 Rev2.0



Part List

Count	Designator	Item Specification	Part Value	Package	Part number	Vendor	Description
1	U1	IC, Power supply of LCD panel	MB39A302	QFN-48	MB39A302	Fujitsu	Power IC
4	C1, C20, C55, C60	1608, 10%, X7R, 50V, 100nF	0.1µF	0603	CC0603KRX7R9BB104	Yageo	Capacitor
1	C2	1608, 20%, X5R, 16V, 1µF	1µF	0603	CC0603KRX5R7BB105	Yageo	Capacitor
18	C3, C4, C5, C6, C12, C13, C14, C23, C24, C34, C35, C50, C80, C81, C83, C84, C85, C86	3216, 10%, X5R, 25V, 10µF	10µF	1206	CC1206KKX5R8BB106	Yageo	Capacitor
1	C11	1608, 10%, X7R, 50V, 22nF	22nF	0603	CC0603KKX7R9BB223	Yageo	Capacitor
1	C15	1608, 5%, NPO, 50V, 680pF	680pF	0603	CC0603JRNPO9BN681	Yageo	Capacitor
2	C16, C21	1608, 10%, X7R, 50V, 10nF	10nF	0603	CC0603KRX7R9BB103	Yageo	Capacitor
1	C22	1608, 5%, NPO, 50V, 68pF	68pF	0603	CC0603JRNPO9BN680	Yageo	Capacitor
7	C30, C33, C40, C42, C52, C54, C61	3216,10%,X7R,50V, 1µF	1µF	1206	CC1206KKX7R9BB105	Yageo	Capacitor
5	C31, C41, C45, C46, C47	3216,10%,X7R,50V, 470nF	0.47µF	1206	CC1206KKX7R9BB474	Yageo	Capacitor
2	C32, C44	1608,5%,NPO,50V, 22pF	22pF	0603	CC0603JRNPO9BN220	Yageo	Capacitor
1	C62	3216,10%,X7R,50V, 1µF	1µF	1206	CC1206KKX7R9BB105	AVX	TanCapacitor
1	C70	1608,10%,X7R,50V, 10nF	10nF	0603	CC0603KRX7R9BB103	Yageo	Capacitor
1	C71	1608,10%,X7R,50V, 1.5nF	1.5nF	0603	CC0603KRX7R9BB152	Yageo	Capacitor
2	D1, D2	Diode, Schottky Rectifier, 3A, 40V	MBRA340T3G	SMA-403D	MBRA340T3	OnSemi	Diode
6	D30, D31, D40, D41, D42, D43	Diode, Schottky, 500mA, 40V	MBR0540T1G	SOD-123	MBR0540T1G	OnSemi	MBR0540T1G
3	JP1, JP2, JP3	Jumper	-	HDR1X3	Standard	-	HEADER1X3
1	L1	Inductor, SMT, 4.4A, 35mΩ	6.8µH	10.3×10.5	SDCS104R-6R8	Chilisin	Inductor
1	L2	Inductor, SMT, 4.4A, 35mΩ	10µH	10.3×10.5	SDCS104R-100	Chilisin	Inductor
1	Q1	MOSFET P-ch	AM4835P	SO-8	AM4835P	Analog Power	MOSFET P-ch
1	RP61	Potentiometer,chip, 1%	EVM3ESX50BE3	Standard	EVM3ESX50BE3	Panasonic	Potentiometer
1	R1	Resistor, Chip, 1%	1K	0603	RC0603FR_1KL	Yageo	Resistor
8	R2, R35, R43, R53, R54, R60, R65, R78	Resistor, Chip, 1%	0R	0603	RC0603FR_0RL	Yageo	Resistor
1	R5	Resistor, Chip, 1%	62K	0603	RC0603FR_62KL	Yageo	Resistor
2	R6, R63	Resistor, Chip, 1%	10K	0603	RC0603FR_10KL	Yageo	Resistor
1	R8	Resistor, Chip, 1%	1.61K	0603	RC0603FR_1K61L	Yageo	Resistor
1	R11	Resistor, Chip, 1%	200K	0603	RC0603FR_200KL	Yageo	Resistor
1	R14	Resistor, Chip, 1%	392K	0603	RC0603FR_392KL	Yageo	Resistor
1	R15	Resistor, Chip, 1%	29.4K	0603	RC0603FR_29K4L	Yageo	Resistor
1	R16	Resistor, Chip, 1%	383R	0603	RC0603FR_383RL	Yageo	Resistor
1	R17	Resistor, Chip, 1%	30.9K	0603	RC0603FR_30K9L	Yageo	Resistor
4	R19, R25, R34, R46	Resistor, Chip, 1%	47K	0603	RC0603FR_47KL	Yageo	Resistor

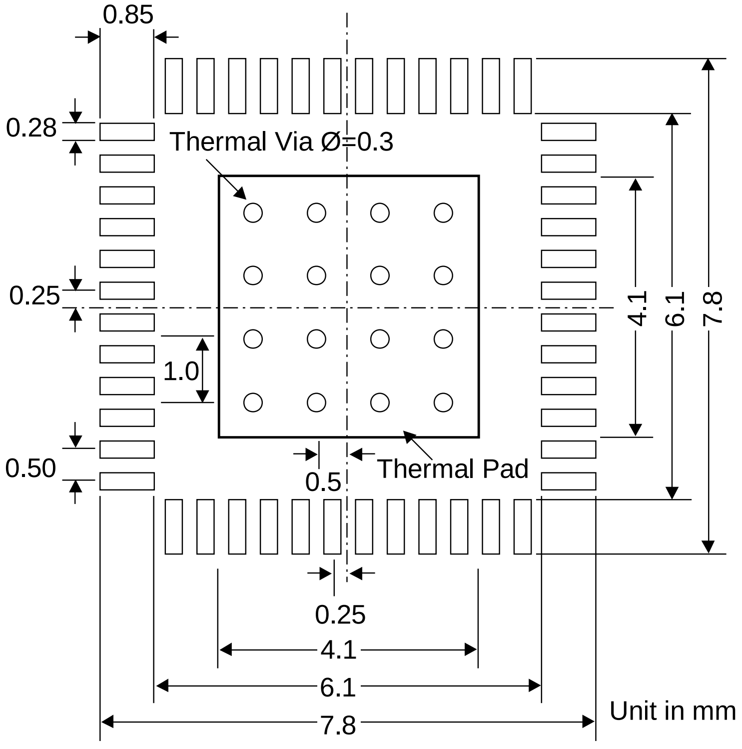
Count	Designator	Item Specification	Part Value	Package	Part number	Vendor	Description
1	R21	Resistor, Chip, 1%	2K	0603	RC0603FR_2KL	Yageo	Resistor
1	R22	Resistor, Chip, 1%	1.2K	0603	RC0603FR_1K2L	Yageo	Resistor
1	R23	Resistor, Chip, 1%	19.6R	0603	RC0603FR_19R6L	Yageo	Resistor
1	R32	Resistor, Chip, 1%	604K	0603	RC0603FR_604KL	Yageo	Resistor
1	R33	Resistor, Chip, 1%	105K	0603	RC0603FR_105KL	Yageo	Resistor
1	R41	Resistor, Chip, 1%	475K	0603	RC0603FR_475KL	Yageo	Resistor
1	R42	Resistor, Chip, 1%	20.5K	0603	RC0603FR_20K5L	Yageo	Resistor
1	R45	Resistor, Chip, 1%	0R	0603	RC0603FR_0RL	Yageo	Resistor
1	R50	Resistor, Chip, 1%	10.5K	0603	RC0603FR_10K5L	Yageo	Resistor
1	R51	Resistor, Chip, 1%	806R	0603	RC0603FR_806RL	Yageo	Resistor
1	R55	Resistor, Chip, 1%	27.4R	0603	RC0603FR_27R4L	Yageo	Resistor
1	R61	Resistor, Chip, 1%	15.8K	0603	RC0603FR_15K8L	Yageo	Resistor
1	R62	Resistor, Chip, 1%	10R	1206	RC1206FR_10RL	Yageo	Resistor
1	R64	Resistor, Chip, 1%	19.6K	0603	RC0603FR_19K6L	Yageo	Resistor
1	R70	Resistor, Chip, 1%	340K	0603	RC0603FR_340KL	Yageo	Resistor
1	R71	Resistor, Chip, 1%	9.76K	0603	RC0603FR_9K76L	Yageo	Resistor
2	R72, R73	Resistor, Chip, 1%, 1/4W	1.5K	1206	RC1206FR_1K5L	Yageo	Resistor
1	R79	Resistor, Chip, 1%	120R	0603	RC0603FR_120RL	Yageo	Resistor
19	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19	Connecting pins	-	-	-	-	Pins
3	TP20, TP21, TP22	Connecting pins	-	-	-	-	Test Pad
Not Mounted	C7, C17, C18, C19, C26, C53	-	-	-	-	-	Capacitor
Not Mounted	C25, C51, C82	3216, 10%, X5R, 25V, 10μF	10μF	1206	CC1206KKX5R8BB106	Yageo	Capacitor
Not Mounted	C43	3216, 10%, X7R, 50V, 1μF	1μF	1206	CC1206KKX7R9BB105	Yageo	Capacitor
Not Mounted	R3, R44	Resistor, Chip, 1%	0R	0603	RC0603FR_0RL	Yageo	Resistor
Not Mounted	R18, R26	-	-	-	-	-	Resistor
Not Mounted	R74, R75, R76, R77	Resistor, Chip, 1%	1.5K	1206	RC1206FR_1K5L	Yageo	Resistor
Not Mounted	Q2	MOSFET P-ch	AO3403	sot23	AO3403	Alpha & Omega	MOSFET P-ch
Pattern Short	R4, R12	-	-	-	-	-	-
Pattern Short	R7, R13, R20, R24, R31, R40, R52, R56	-	-	-	-	-	-

Fujitsu: Fujitsu Semiconductor Limited
Yageo: YAGEO Corporation
AVX: AVX Corporation
OnSemi: ON Semiconductor
Chilisin: Chilisin Electronics Corp.
AnalogPower: Analog Power
Panasonic: Panasonic Corporation
Alpha & Omega: Alpha & Omega Semiconductor

■ LAND PATTERN

The MB30A302 has an exposed thermal pad zone on the bottom side of the IC. This area has to be soldered onto the PCB board to enhance heat dissipation.

The via should be placed in the thermal pad. These via assist heat dissipation towards the bottom layer of the PCB. Via and copper pad size may be adjusted according to PCB constraints.



■ USAGE PRECAUTION

1. Never use setting exceeding maximum rated conditions.
   Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Use the devices within recommended conditions
   It is recommended that devices be operated within recommended conditions.
   Exceeding the recommended operating condition may adversely affect devices reliability.
   Nominal electrical characteristics are warranted within the range of recommended operating conditions otherwise specified on each parameter in the section of electrical characteristics.

3. Design the ground line on printed circuit boards with consideration of common impedance.

4. Take appropriate static electricity measures.
   Containers for semiconductor materials should have anti-static protection or be made of conductive material.
   After mounting, printed circuit boards should be stored and shipped in conductive bags or containers.
   Work platforms, tools, and instruments should be properly grounded.
   Working personnel should be grounded with resistance of 250 kΩ to 1 MΩ between body and ground.

5. Do not apply negative voltages.
   The use of negative voltages below -0.3 V may activate parasitic transistors on the device, which can cause abnormal operation.

■ ORDERING INFORMATION

Part number	Packege	Remarks
MB39A302WQN	48-pin plastic QFN (LCC-48P-M11)	

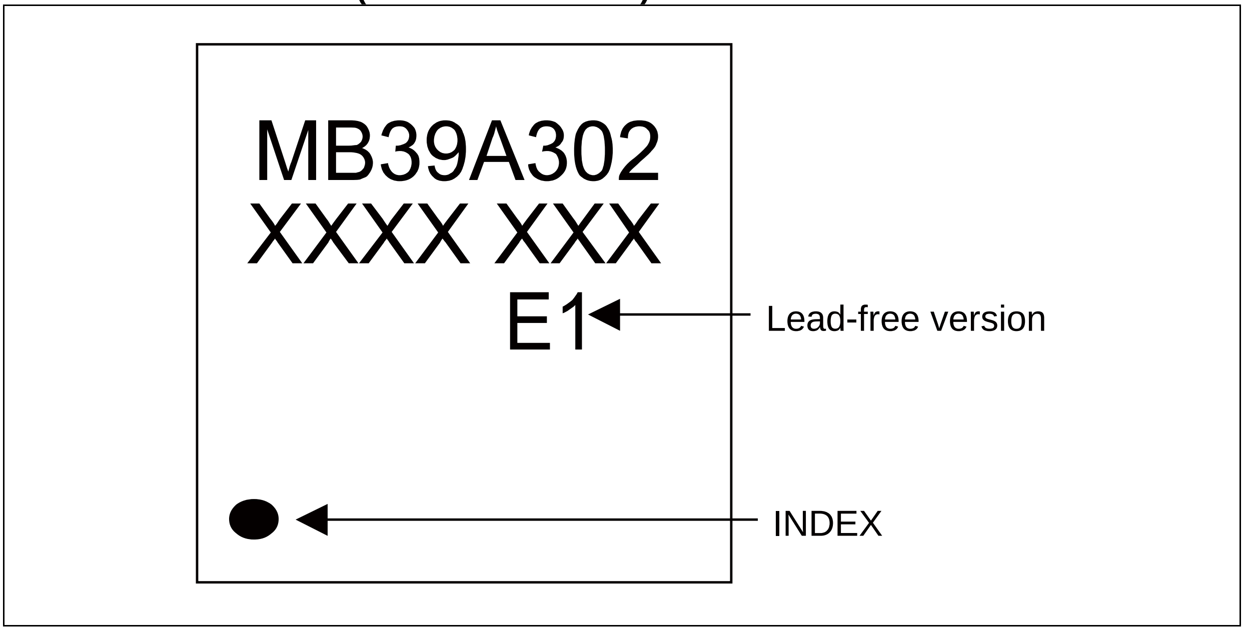
■ EV BOARD ORDERING INFORMATION

EV board number	EV board version No.	Remarks
MB39A302-EVB-01	MB39A302 EVB-01 Rev1.2	QFN-48 Exposed PAD

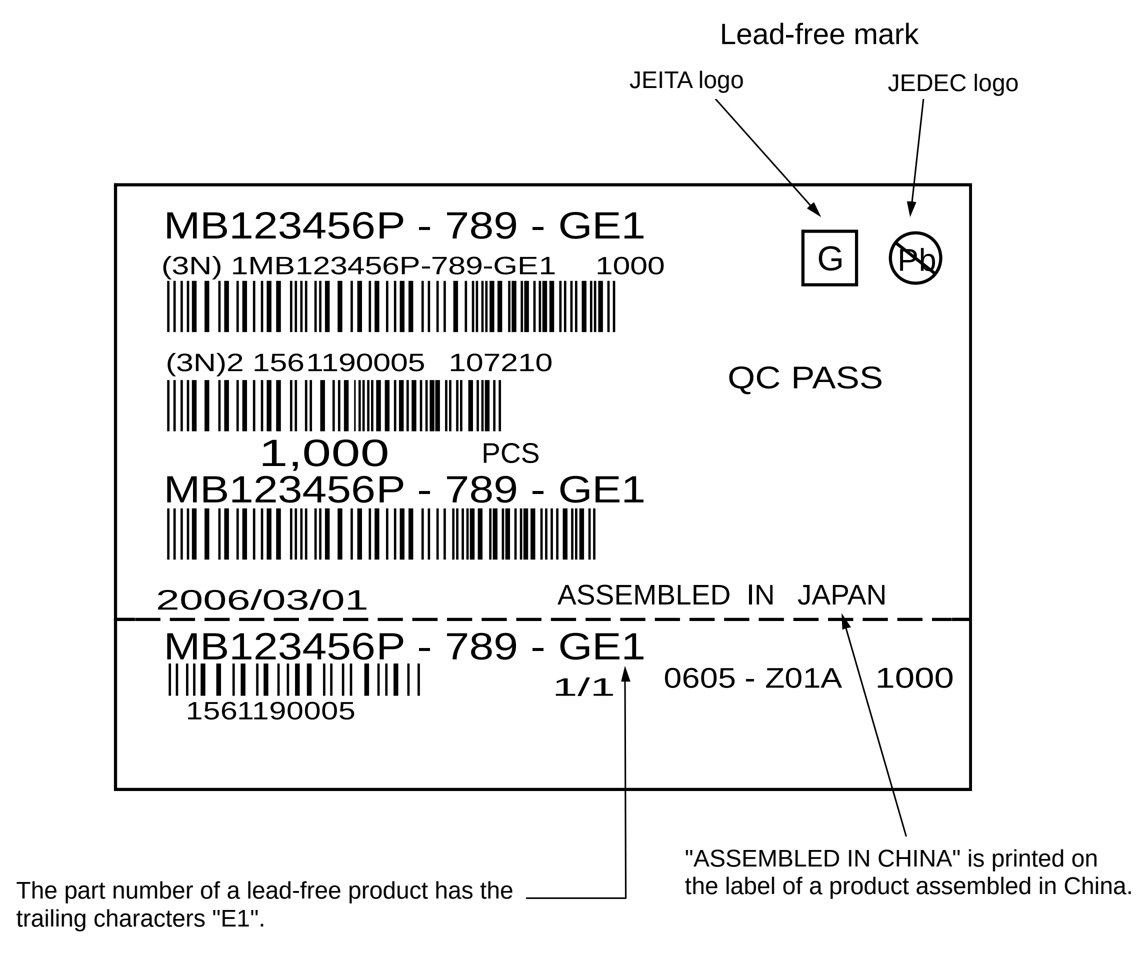
■ RoHS COMPLIANCE INFORMATION OF LEAD (Pb) FREE VERSION

The LSI products of FUJITSU SEMICONDUCTOR with “E1” are compliant with RoHS Directive, and has observed the standard of lead, cadmium, mercury, Hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE). A product whose part number has trailing characters “E1” is RoHS compliant.

■ MARKING FORMAT (Lead Free version)



■ LABELING SAMPLE (Lead free version)



■MB39A302 RECOMMENDED CONDITIONS OF MOISTURE SENSITIVITY LEVEL

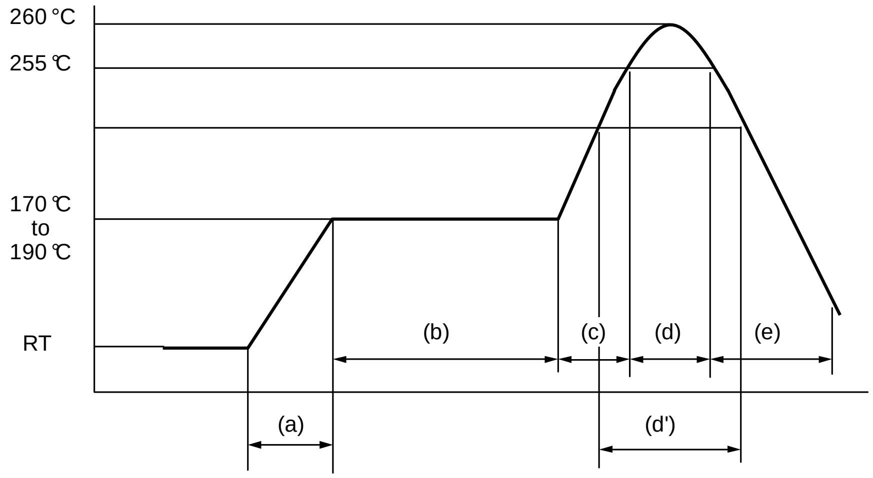
[FUJITSU SEMICONDUCTOR Recommended Mounting Conditions]

Item	Condition	
Mounting Method	IR (infrared reflow), warm air reflow	
Mounting times	2 times	
Storage period	Before opening	Please use it within two years after manufacture.
	From opening to the 2nd reflow	Less than 8 days
	When the storage period after opening was exceeded	Please process within 8 days after baking (125°C ± 3°C, 24hrs + 2H/-0H) Baking can be performed up to two times.*
Storage conditions	5°C to 30°C, 70% RH or less (the lowest possible humidity)	

*: When taping is used as the shipping form, baking should be performed individually.

[Parameters for Each Mounting Method]

IR (infrared reflow)



H rank: 260℃ Max

(a) Temperature Increase gradient : Average 1℃/s to 4℃/s

(b) Preliminary heating : Temperature 170℃ to 190℃, 60s to 180s

(c) Temperature Increase gradient : Average 1℃/s to 4℃/s

(d) Actual heating : Temperature 260℃ Max; 255℃ or more, 10s or less

(d’) : Temperature 230℃ or more, 40s or less
or
Temperature 225℃ or more, 60s or less
or
Temperature 220℃ or more, 80s or less

(e) Cooling : Natural cooling or forced cooling

Note : Temperature : the top of the package body

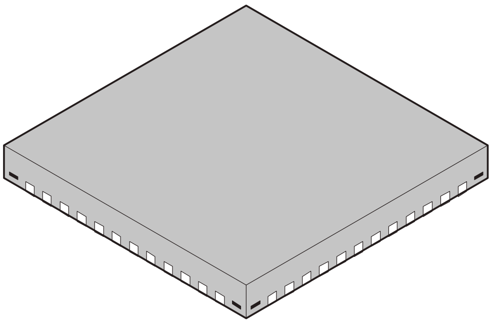
JEDEC standard: Moisture Sensitivity Level 3 (IPC/JEDEC J-STD-020D)

Recommended manual soldering (partial heating method)

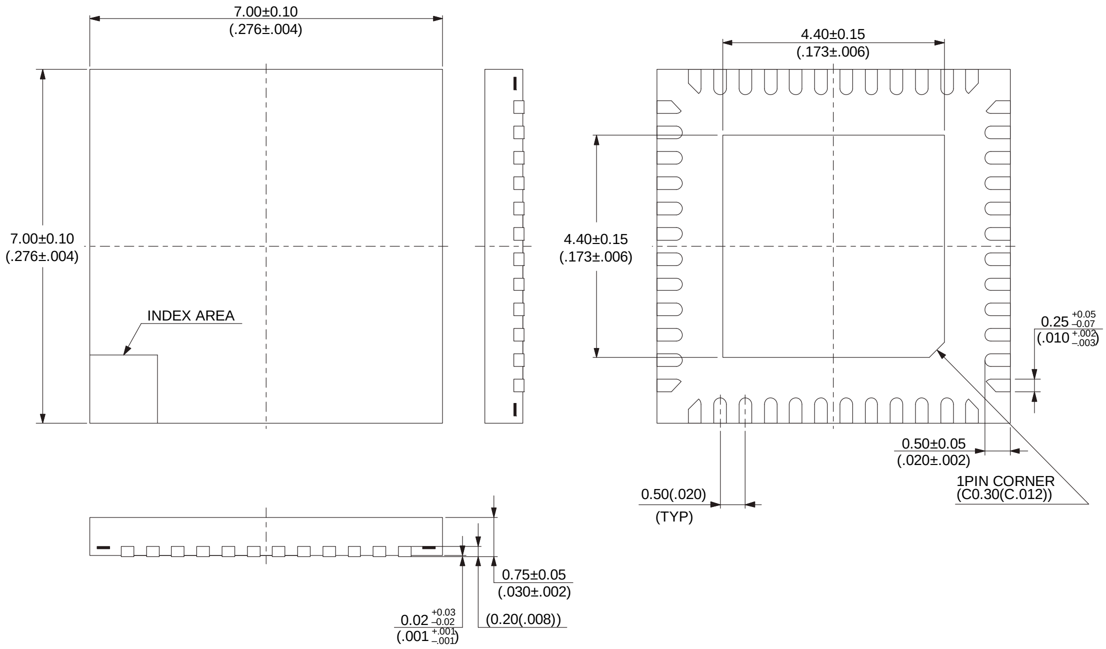
Item	Condition	
Storage period	Before opening	Within two years after manufacture.
	Between opening and mounting	Within two years after manufacture. (No need to control moisture during the storage period because of the partial heating method.)
Storage conditions	5°C to 30°C, 70% RH or less (the lowest possible humidity)	
Mounting conditions	Temperature at the tip of a soldering iron: 400°C max Time: Five seconds or below per pin*	

*: Make sure that the tip of a soldering iron does not come in contact with the package body.

■ PACKAGE DIMENSIONS

<table>
<tr><td rowspan="7">48-pin plastic QFN

(LCC-48P-M11)</td><td>Lead pitch</td><td>0.50 mm</td></tr>
<tr><td>Package width × package length</td><td>7.00 mm × 7.00 mm</td></tr>
<tr><td>Sealing method</td><td>Plastic mold</td></tr>
<tr><td>Mounting height</td><td>0.80 mm MAX</td></tr>
<tr><td>Weight</td><td>0.12 g</td></tr>
<tr><td></td><td></td></tr>
<tr><td></td><td></td></tr>
</table>

48-pin plastic QFN
(LCC-48P-M11)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

MEMO

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