

32-bit Microcontrollers

CMOS

FR80 MB91645A Series

MB91F647A/V650

■ DESCRIPTION

The MB91645A series is a line of Fujitsu Microelectronics microcontrollers based on a 32-bit RISC CPU core that feature a variety of peripheral functions for embedded applications that demand high-performance and high-speed CPU processing.

This series is based on the FR80* family CPU and is implemented as a single chip.

* : FR is a line of products of FUJITSU MICROELECTRONICS Limited.

■ FEATURES

- FR80 CPU
 - 32-bit RISC, load/store architecture, five-stage pipeline
 - General-purpose registers : 32-bit × 16
 - 16-bit fixed-length instructions (basic instructions) : 1 instruction per cycle
 - Instructions suitable for embedded applications
 - Memory-to-memory transfer, bit processing, barrel shift instructions, etc.
 - Instruction support for high level languages
 - Function entry and exit instructions, instructions for register multi-load and multi-store
 - Bit search instruction
 - "1" detection, "0" detection, transition point detection
 - Branch instructions with delay slots
 - Reduced overhead when processing branches

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For the information for microcontroller supports, see the following web site.

This web site includes the "**Customer Design Review Supplement**" which provides the latest cautions on system development and the minimal requirements to be checked to prevent problems before the system development.

<http://edevice.fujitsu.com/micom/en-support/>

MB91645A Series

- Register interlock functions
Facilitate coding in assembly language
- Built-in multiplier/instruction-level support
 - Signed 32-bit multiplication : 5 cycles
 - Signed 16-bit multiplication : 3 cycles
- Interrupts (save PC and PS) : 6 cycles, 16 priority levels
- Harvard architecture allowing program access and data access to be executed simultaneously
- Instruction prefetch function has been added with 4 word instruction queue of CPU

- Instruction compatible with FR family CPU
 - Additional bit search instructions
 - No resource instructions and coprocessor instructions

- Maximum operating frequency

- CPU : 60 MHz
- Resources : 40 MHz
- External bus : 40 MHz

Note: The PLL clock specification of MB91645A series

In MB91645A series, PLL clock specification has been modified from MB91645 series. The setting of dividing by 1 of PLL macro oscillation clock divide configuration value is prohibited.

Therefore, please use the device with setting as dividing by 2 to 4 by ODS0 or ODS1 bit in the PLL configuration register (PLLCCR) . For more details, refer to “4.4.4 PLL Configuration Register (PLLCCR) ” in the “Hardware Manual”.

- External bus interface
 - Operating frequency : Max 40 MHz
 - 24 address lines, 8- or 16-bit data I/O (separate busses or multiplexed bus)
 - Chip select output available for 4 independent programmable areas
Programmable automatic wait cycle insertion for each area
- DMA controller (DMAC)
 - 8 channels
 - Address space : 32 bits (4 Gbytes)
 - Transfer modes : Block transfer/burst transfer/demand transfer
 - Address update : Increment/decrement/fixed (increment/decrement step size of 1, 2, or 4)
 - Transfer data length : Selectable from 8-bit, 16-bit, 32-bit
 - Block size : 1 to 16
 - Number of transfers : 1 to 65535
 - Transfer requests
 - Requests from software
 - Interrupt requests from peripheral resources (interrupt requests are shared, including external interrupts)
 - Requests from external pins
 - Reload functions : Reload can be specified on all channels
 - Priority order : Fixed (ch.0 > ch.1 > ch.2 > ch.3 > ...) or round-robin
 - Interrupt requests : Interrupts can be generated for transfer complete, transfer error, and transfer interrupted.

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- Multifunction serial interface
 - 4 channels with 16-byte FIFO, 8 channels without FIFO
 - Operation mode is selectable from the followings for each channel (For ch.0, I²C is not available.)
 - UART
 - Full-duplex double buffer
 - Selectable parity on/off
 - Built-in dedicated baud rate generator
 - External clock can be used as a serial clock
 - Error detection function for parity, frame and overrun errors
 - CSIO
 - Full-duplex double buffer
 - Built-in dedicated baud rate generator
 - Overrun error detection function
 - I²C
 - Supports both standard mode (Max 100 kbps) and Fast mode (Max 400 kbps)
 - Some channels are 5 V tolerant
- Interrupts
 - Total of 32 external interrupts (some pins are 5 V tolerant)
 - Interrupts from peripheral resources
 - Programmable interrupt levels (16 levels)
 - Can be used to return from stop mode, sleep mode
- A/D converter
 - 32 channels, 2 units
 - 10-bit resolution
 - Conversion time : approx. 1.2 μ s (PCLK = 33 MHz)
 - Priority conversion (2 levels)
 - Conversion modes : Single-shot conversion mode, scan conversion mode
 - Activation sources : Software, external trigger, base timer
 - Built-in FIFO for storing conversion data (for scan conversion:16, for priority conversion:4)
- D/A converter
 - 3 channels
 - 8-bit resolution
- Base timer
 - 16 channels
 - Operation mode is selectable from the followings for each channel
 - 16/32-bit reload timer
 - 16-bit PWM timer
 - 16/32-bit PWC timer
 - 16-bit PPG timer
 - Cascading connection between 2 channels allows them to be used as one 32-bit timer
 - Multiple channels can be started simultaneously
 - Input/output select function

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- 16-bit reload timer
 - 3 channels (including 1 channel for REALOS)
 - Interval timer function
 - Count clock select function (peripheral clock (PCLK) divided by 2 to 64)

- Compare timer
 - 32-bit input capture : 8 channels
 - 32-bit output compare : 8 channels
 - 32-bit free-run timer : 2 channels

- Other interval timers
 - Up/down counter : 4 channels
 - Watch counter : 1 channel
 - Watchdog timer : 1 channel

- Main timer
 - 1 channel
 - Counts the oscillation stabilization wait time of the main clock (MCLK)
 - Counts the oscillation stabilization wait time of the PLL clock (PLLCLK)
 - Can be used as an interval timer while the main clock (MCLK) oscillations is stable

- Sub timer
 - 1 channel
 - Counts the oscillation stabilization wait time of the sub clock (SBCLK)
 - Can be used as an interval timer while the sub clock (SBCLK) oscillations is stable

- Clock generation
 - Main clock (MCLK) oscillator
 - Sub clock (SBCLK) oscillator
 - PLL clock (PLLCLK) oscillator

- Low-power dissipation mode
 - Stop mode
 - Watch mode
 - Sleep mode
 - Doze mode
 - Clock division function

- Other features
 - I/O port
 - $\overline{\text{INIT}}$ pin is provided as a reset pin
 - Watchdog timer reset, software reset
 - Delay interrupt
 - Power supply : Dual power supply (I/O part : 2.7 V to 3.6 V, internal: 1.65 V to 1.95 V)

MB91645A Series

■ PRODUCT LINEUP

Product Name Items	MB91V650	MB91F647A
Product type	Evaluation product	Flash memory product
Built-in program memory capacity	— (Support by emulation memory)	512 K bytes (Flash)
Built-in RAM capacity	128 K bytes	48 K bytes
External bus interface	Yes	
DMA controller (DMAC)	8 channels	
Base timer	16 channels	
Multifunction serial interface	Without FIFO : 8 channels (ch.0 to ch.7) With FIFO : 4 channels (ch.8 to ch.11)	
External interrupt	32 (some pins are 5 V tolerant)	
10-bit A/D converter	32 channels, 2 units	
8-bit D/A converter	3 channels	
16-bit reload timer	3 channels	
32-bit input capture	8 channels	
32-bit output compare	8 channels	
32-bit free-run timer	2 channels	
Up/Down counter	4 channels	
Watch counter	1 channel	
I/O port	154	153
Main timer	1 channel	
Sub timer	1 channel	
Wild register	16 channels	
Debug function	DSU4	—

■ PACKAGES

Product name Package	MB91F647A
FPT-176P-M07 (LQFP-0.50mm)	○
BGA-176P-M04 (PFBGA-0.80mm)	○

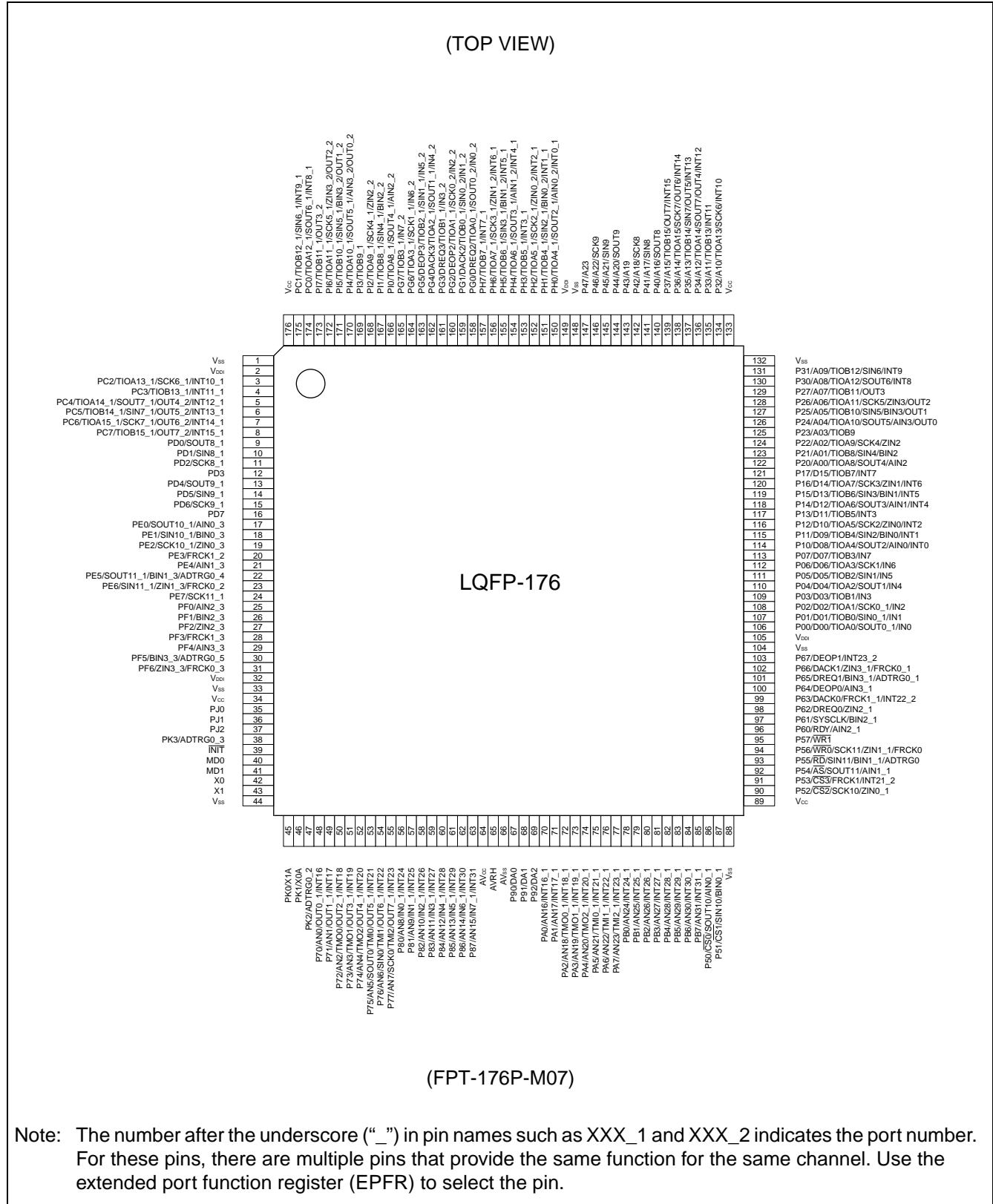
○ : Supported

Note: Refer to "■ PACKAGE DIMENSION" for detailed information on each package.

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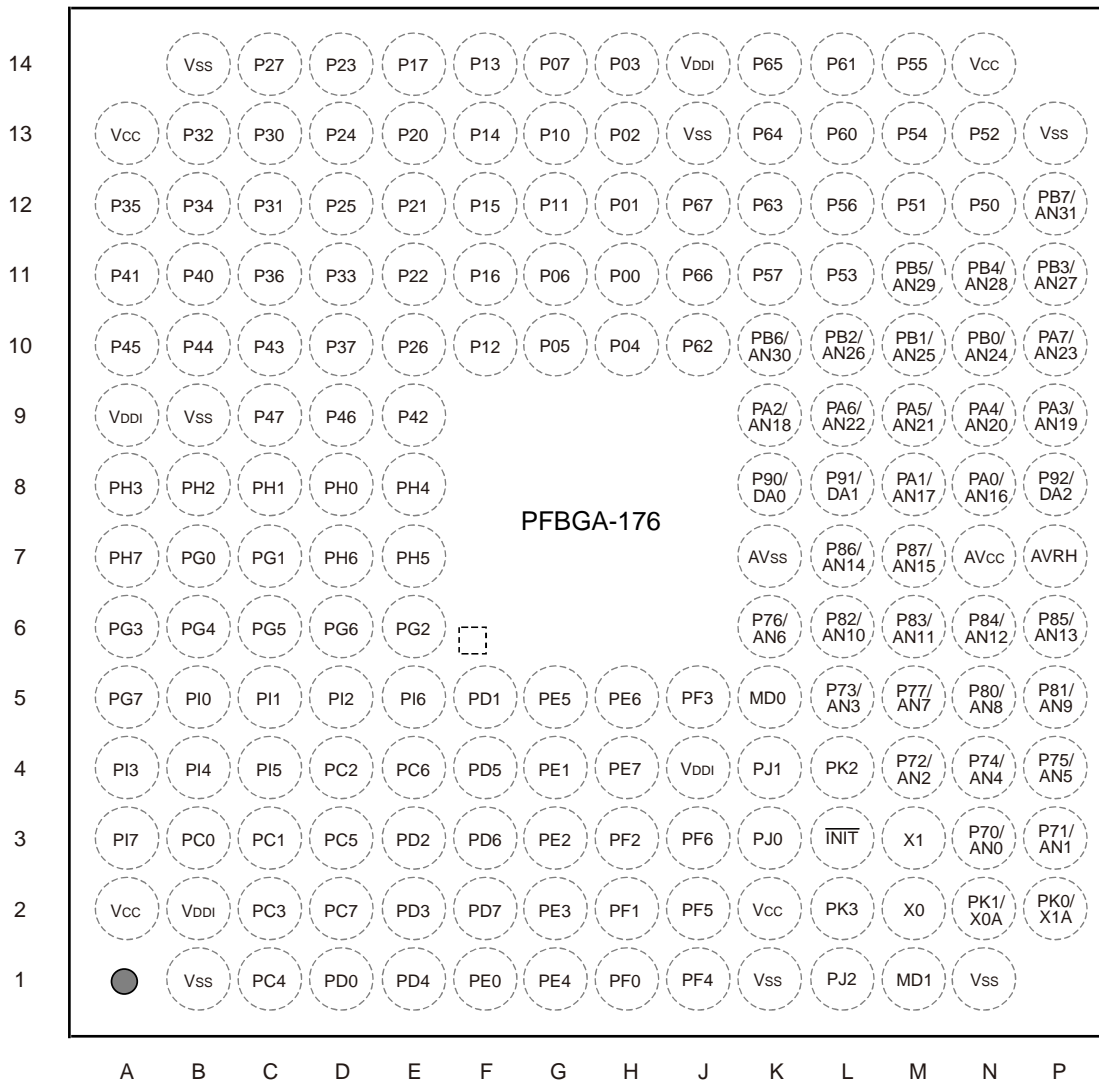
PIN ASSIGNMENT

LQFP-176



PFBGA-176

(TOP VIEW)



(BGA-176P-M04)

Note: Due to the space limitation, the pin assignment for the PFBGA-176 only shows representative names for each of the pins such as port names. Refer to "■ PIN DESCRIPTION" for the pin names.

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■ PIN DESCRIPTION

The number after the underscore (“_”) in pin names such as XXX_1 and XXX_2 indicates the port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin no.		Pin name	I/O circuit type*3	Function	CMOS level input	CMOS level hysteresis input
LQFP*1	PFBGA*2					
1	B1	V _{SS}	—	GND pin	—	—
2	B2	V _{DDI}	—	1.8V power supply pin	—	—
3	D4	PC2	C	General-purpose I/O port	—	○
		TIOA13_1		Base timer ch.13 TIOA pin (Port 1)	—	○
		SCK6_1 (SCL6_1)		Multifunction serial interface ch.6 clock I/O pin (Port 1). This pin operates as SCK6_1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL6_1 when it is used in an I ² C (operation mode 4).	—	○
		INT10_1		External interrupt request 10 input pin (Port 1)	—	○
4	C2	PC3	C	General-purpose I/O port	—	○
		TIOB13_1		Base timer ch.13 TIOB pin (Port 1)	—	○
		INT11_1		External interrupt request 11 input pin (Port 1)	—	○
5	C1	PC4	C	General-purpose I/O port	—	○
		TIOA14_1		Base timer ch.14 TIOA pin (Port 1)	—	—
		SOUT7_1 (SDA7_1)		Multifunction serial interface ch.7 output pin (Port 1). This pin operates as SOUT7_1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA7_1 when it is used in an I ² C (operation mode 4).	—	○
		OUT4_2		32-bit output compare ch.4 output pin (Port 2)	—	—
		INT12_1		External interrupt request 12 input pin (Port 1)	—	○

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Pin no.		Pin name	I/O circuit type*3	Function	CMOS level input	CMOS level hysteresis input
LQFP*1	PFBGA*2					
6	D3	PC5	C	General-purpose I/O port	—	○
		TIOB14_1		Base timer ch.14 TIOB pin (Port 1)	—	○
		SIN7_1		Multifunction serial interface ch.7 input pin (Port 1)	—	○
		OUT5_2		32-bit output compare ch.5 output pin (Port 2)	—	—
		INT13_1		External interrupt request 13 input pin (Port 1)	—	○
7	E4	PC6	C	General-purpose I/O port	—	○
		TIOA15_1		Base timer ch.15 TIOA pin (Port 1)	—	○
		SCK7_1 (SCL7_1)		Multifunction serial interface ch.7 clock I/O pin (Port 1). This pin operates as SCK7_1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL7_1 when it is used in an I ² C (operation mode 4).	—	○
		OUT6_2		32-bit output compare ch.6 output pin (Port 2)	—	—
		INT14_1		External interrupt request 14 input pin (Port 1)	—	○
8	D2	PC7	C	General-purpose I/O port	—	○
		TIOB15_1		Base timer ch.15 TIOB pin (Port 1)	—	○
		OUT7_2		32-bit output compare ch.7 output pin (Port 2)	—	—
		INT15_1		External interrupt request 15 input pin (Port 1)	—	○
9	D1	PD0	C	General-purpose I/O port	—	○
		SOUT8_1 (SDA8_1)		Multifunction serial interface ch.8 output pin (Port 1). This pin operates as SOUT8_1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA8_1 when it is used in an I ² C (operation mode 4).	—	○
10	F5	PD1	C	General-purpose I/O port	—	○
		SIN8_1		Multifunction serial interface ch.8 input pin (Port 1)	—	○

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Pin no.		Pin name	I/O circuit type*3	Function	CMOS level input	CMOS level hysteresis input
LQFP*1	PFBGA*2					
11	E3	PD2	C	General-purpose I/O port	—	○
		SCK8_1 (SCL8_1)		Multifunction serial interface ch.8 clock I/O pin (Port 1). This pin operates as SCK8_1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL8_1 when it is used in an I ² C (operation mode 4).	—	○
12	E2	PD3	C	General-purpose I/O port	—	○
13	E1	PD4	C	General-purpose I/O port	—	○
		SOUT9_1 (SDA9_1)		Multifunction serial interface ch.9 output pin (Port 1). This pin operates as SOUT9_1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA9_1 when it is used in an I ² C (operation mode 4).	—	○
14	F4	PD5	C	General-purpose I/O port	—	○
		SIN9_1		Multifunction serial interface ch.9 input pin (Port 1)	—	○
15	F3	PD6	C	General-purpose I/O port	—	○
		SCK9_1 (SCL9_1)		Multifunction serial interface ch.9 clock I/O pin (Port 1). This pin operates as SCK9_1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL9_1 when it is used in an I ² C (operation mode 4).	—	○
16	F2	PD7	C	General-purpose I/O port	—	○
17	F1	PE0	C	General-purpose I/O port	—	○
		SOUT10_1 (SDA10_1)		Multifunction serial interface ch.10 output pin (Port 1). This pin operates as SOUT10_1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA10_1 when it is used in an I ² C (operation mode 4).	—	○
		AIN0_3		Up/Down counter ch.0 AIN input pin (Port 3)	—	○

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Pin no.		Pin name	I/O circuit type*3	Function	CMOS level input	CMOS level hysteresis input
LQFP*1	PFBGA*2					
18	G4	PE1	C	General-purpose I/O port	—	○
		SIN10_1		Multifunction serial interface ch.10 input pin (Port 1)	—	○
		BIN0_3		Up/Down counter ch.0 BIN input pin (Port 3)	—	○
19	G3	PE2	C	General-purpose I/O port	—	○
		SCK10_1 (SCL10_1)		Multifunction serial interface ch.10 clock I/O pin (Port 1). This pin operates as SCK10_1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL10_1 when it is used in an I ² C (operation mode 4).	—	○
		ZIN0_3		Up/Down counter ch.0 ZIN input pin (Port 3)	—	○
20	G2	PE3	C	General-purpose I/O port	—	○
		FRCK1_2		32-bit free-run timer ch.1 external clock input pin (Port 2)	—	○
21	G1	PE4	C	General-purpose I/O port	—	○
		AIN1_3		Up/Down counter ch.1 AIN input pin (Port 3)	—	○
22	G5	PE5	C	General-purpose I/O port	—	○
		SOUT11_1 (SDA11_1)		Multifunction serial interface ch.11 output pin (Port 1). This pin operates as SOUT11_1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA11_1 when it is used in an I ² C (operation mode 4).	—	○
		BIN1_3		Up/Down counter ch.1 BIN input pin (Port 3)	—	○
		ADTRG0_4		10-bit A/D converter external trigger input pins (Port 4).	—	○
23	H5	PE6	C	General-purpose I/O port	—	○
		SIN11_1		Multifunction serial interface ch.11 input pin (Port 1)	—	○
		ZIN1_3		Up/Down counter ch.1 ZIN input pin (Port 3)	—	○
		FRCK0_2		32-bit free-run timer ch.0 external clock input pin (Port 2)	—	○

(Continued)

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Pin no.		Pin name	I/O circuit type*3	Function	CMOS level input	CMOS level hysteresis input
LQFP*1	PFBGA*2					
24	H4	PE7	C	General-purpose I/O port	—	○
		SCK11_1 (SCL11_1)		Multifunction serial interface ch.11 clock I/O pin (Port 1). This pin operates as SCK11_1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL11_1 when it is used in an I ² C (operation mode 4).	—	○
25	H1	PF0	C	General-purpose I/O port	—	○
		AIN2_3		Up/Down counter ch.2 AIN input pin (Port 3)	—	○
26	H2	PF1	C	General-purpose I/O port	—	○
		BIN2_3		Up/Down counter ch.2 BIN input pin (Port 3)	—	○
27	H3	PF2	C	General-purpose I/O port	—	○
		ZIN2_3		Up/Down counter ch.2 ZIN input pin (Port 3)	—	○
28	J5	PF3	C	General-purpose I/O port	—	○
		FRCK1_3		32-bit free-run timer ch.1 external clock input pin (Port 3)	—	○
29	J1	PF4	C	General-purpose I/O port	—	○
		AIN3_3		Up/Down counter ch.3 AIN input pin (Port 3)	—	○
30	J2	PF5	C	General-purpose I/O port	—	○
		BIN3_3		Up/Down counter ch.3 BIN input pin (Port 3)	—	○
		ADTRG0_5		10-bit A/D converter external trigger input pins (Port 5).	—	○
31	J3	PF6	C	General-purpose I/O port	—	○
		ZIN3_3		Up/Down counter ch.3 ZIN input pin (Port 3)	—	○
		FRCK0_3		32-bit free-run timer ch.0 external clock input pin (Port 3)	—	○
32	J4	V _{DDI}	—	1.8V power supply pin	—	—
33	K1	V _{SS}	—	GND pin	—	—
34	K2	V _{CC}	—	3.3V power supply pin	—	—
35	K3	PJ0	C	General-purpose I/O port	—	○
36	K4	PJ1	C	General-purpose I/O port	—	○

(Continued)

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Pin no.		Pin name	I/O circuit type*3	Function	CMOS level input	CMOS level hysteresis input
LQFP*1	PFBGA*2					
37	L1	PJ2	C	General-purpose I/O port	—	○
38	L2	PK3	C	General-purpose I/O port	—	○
		ADTRG0_3		10-bit A/D converter external trigger input pins (Port 3).	—	○
39	L3	$\overline{\text{INIT}}$	P	External reset input pin. A reset is valid when $\overline{\text{INIT}}=\text{L}$. The I/O circuit type for the flash memory products is P.	—	○
40	K5	MD0	P	Mode 0 pin. The I/O circuit type for the flash memory products is P. During normal operation, MD0=L must be input. During serial programming to flash memory, MD0=H must be input.	—	○
41	M1	MD1	P	Mode 1 pin. "L" level must be always input. The I/O circuit type for the flash memory products is P.	—	○
42	M2	X0	A	Main clock (oscillation) input pin	—	○
43	M3	X1	A	Main clock (oscillation) I/O pin	—	—
44	N1	V _{SS}	—	GND pin	—	—
45	P2	PK0	I	General-purpose I/O port	—	○
		X1A		Sub clock (oscillation) I/O pin	—	—
46	N2	PK1	I	General-purpose I/O port	—	○
		X0A		Sub clock (oscillation) input pin	—	○
47	L4	PK2	C	General-purpose I/O port	—	○
		ADTRG0_2		10-bit A/D converter external trigger input pins (Port 2).	—	○
48	N3	P70	E	General-purpose I/O port	—	○
		AN0		10-bit A/D converter ch.0 analog input pin	—	—
		OUT0_1		32-bit output compare ch.0 output pin (Port 1)	—	—
		INT16		External interrupt request 16 input pin	—	○

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Pin no.		Pin name	I/O circuit type*3	Function	CMOS level input	CMOS level hysteresis input
LQFP*1	PFBGA*2					
49	P3	P71	E	General-purpose I/O port	—	○
		AN1		10-bit A/D converter ch.1 analog input pin	—	—
		OUT1_1		32-bit output compare ch.1 output pin (Port 1)	—	—
		INT17		External interrupt request 17 input pin	—	○
50	M4	P72	E	General-purpose I/O port	—	○
		AN2		10-bit A/D converter ch.2 analog input pin.	—	—
		TMO0		16-bit reload timer ch.0 output pin	—	—
		OUT2_1		32-bit output compare ch.2 output pin (Port 1)	—	—
		INT18		External interrupt request 18 input pin	—	○
51	L5	P73	E	General-purpose I/O port	—	○
		AN3		10-bit A/D converter ch.3 analog input pin	—	—
		TMO1		16-bit reload timer ch.1 output pin	—	—
		OUT3_1		32-bit output compare ch.3 output pin (Port 1)	—	—
		INT19		External interrupt request 19 input pin	—	○
52	N4	P74	E	General-purpose I/O port	—	○
		AN4		10-bit A/D converter ch.4 analog input pin	—	—
		TMO2		16-bit reload timer ch.2 output pin	—	—
		OUT4_1		32-bit output compare ch.4 output pin (Port 1)	—	—
		INT20		External interrupt request 20 input pin	—	○

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Pin no.		Pin name	I/O circuit type*3	Function	CMOS level input	CMOS level hysteresis input
LQFP*1	PFBGA*2					
53	P4	P75	E	General-purpose I/O port	—	○
		AN5		10-bit A/D converter ch.5 analog input pin	—	—
		SOUT0		Multifunction serial interface ch.0 output pin. This pin operates as SOUT0 when it is used in a UART/CSIO (operation modes 0 to 2).	—	—
		TMI0		16-bit reload timer ch.0 input pin	—	○
		OUT5_1		32-bit output compare ch.5 output pin (Port 1)	—	—
		INT21		External interrupt request 21 input pin	—	○
54	K6	P76	E	General-purpose I/O port	—	○
		AN6		10-bit A/D converter ch.6 analog input pin	—	—
		SIN0		Multifunction serial interface ch.0 input pin	—	○
		TMI1		16-bit reload timer ch.1 input pin	—	○
		OUT6_1		32-bit output compare ch.6 output pin (Port 1)	—	—
		INT22		External interrupt request 22 input pin	—	○
55	M5	P77	E	General-purpose I/O port	—	○
		AN7		10-bit A/D converter ch.7 analog input pin	—	—
		SCK0		Multifunction serial interface ch.0 clock I/O pin. This pin operates as SCK0 when it is used in a UART/CSIO (operation modes 0 to 2).	—	○
		TMI2		16-bit reload timer ch.2 input pin	—	○
		OUT7_1		32-bit output compare ch.7 output pin (Port 1)	—	—
		INT23		External interrupt request 23 input pin	—	○

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Pin no.		Pin name	I/O circuit type*3	Function	CMOS level input	CMOS level hysteresis input
LQFP*1	PFBGA*2					
56	N5	P80	E	General-purpose I/O port	—	○
		AN8		10-bit A/D converter ch.8 analog input pin	—	—
		IN0_1		32-bit input capture ch.0 input pin (Port 1)	—	○
		INT24		External interrupt request 24 input pin	—	○
57	P5	P81	E	General-purpose I/O port	—	○
		AN9		10-bit A/D converter ch.9 analog input pin	—	—
		IN1_1		32-bit input capture ch.1 input pin (Port 1)	—	○
		INT25		External interrupt request 25 input pin	—	○
58	L6	P82	E	General-purpose I/O port	—	○
		AN10		10-bit A/D converter ch.10 analog input pin	—	—
		IN2_1		32-bit input capture ch.2 input pin (Port 1)	—	○
		INT26		External interrupt request 26 input pin	—	○
59	M6	P83	E	General-purpose I/O port	—	○
		AN11		10-bit A/D converter ch.11 analog input pin	—	—
		IN3_1		32-bit input capture ch.3 input pin (Port 1)	—	○
		INT27		External interrupt request 27 input pin	—	○
60	N6	P84	E	General-purpose I/O port	—	○
		AN12		10-bit A/D converter ch.12 analog input pin	—	—
		IN4_1		32-bit input capture ch.4 input pin (Port 1)	—	○
		INT28		External interrupt request 28 input pin	—	○

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MB91645A Series

Pin no.		Pin name	I/O circuit type*3	Function	CMOS level input	CMOS level hysteresis input
LQFP*1	PFBGA*2					
61	P6	P85	E	General-purpose I/O port	—	○
		AN13		10-bit A/D converter ch.13 analog input pin	—	—
		IN5_1		32-bit input capture ch.5 input pin (Port 1)	—	○
		INT29		External interrupt request 29 input pin	—	○
62	L7	P86	E	General-purpose I/O port	—	○
		AN14		10-bit A/D converter ch.14 analog input pin	—	—
		IN6_1		32-bit input capture ch.6 input pin (Port 1)	—	○
		INT30		External interrupt request 30 input pin	—	○
63	M7	P87	E	General-purpose I/O port	—	○
		AN15		10-bit A/D converter ch.15 analog input pin	—	—
		IN7_1		32-bit input capture ch.7 input pin (Port 1)	—	○
		INT31		External interrupt request 31 input pin	—	○
64	N7	AV _{CC}	—	10-bit A/D converter and 8-bit D/A converter analog power pin	—	—
65	P7	AVRH	—	10-bit A/D converter analog reference voltage input pin	—	—
66	K7	AV _{SS}	—	10-bit A/D converter and 8-bit D/A converter GND pin	—	—
67	K8	P90	F	General-purpose I/O port	—	○
		DA0		Analog output pins of the 8-bit D/A converter ch.0.	—	—
68	L8	P91	F	General-purpose I/O port	—	○
		DA1		Analog output pins of the 8-bit D/A converter ch.1.	—	—
69	P8	P92	F	General-purpose I/O port	—	○
		DA2		Analog output pins of the 8-bit D/A converter ch.2.	—	—

(Continued)

MB91645A Series

Pin no.		Pin name	I/O circuit type*3	Function	CMOS level input	CMOS level hysteresis input
LQFP*1	PFBGA*2					
70	N8	PA0	E	General-purpose I/O port	—	○
		AN16		10-bit A/D converter ch.16 analog input pin	—	—
		INT16_1		External interrupt request 16 input pin (Port 1)	—	○
71	M8	PA1	E	General-purpose I/O port	—	○
		AN17		10-bit A/D converter ch.17 analog input pin	—	—
		INT17_1		External interrupt request 17 input pin (Port 1)	—	○
72	K9	PA2	E	General-purpose I/O port	—	○
		AN18		10-bit A/D converter ch.18 analog input pin	—	—
		TMO0_1		16-bit reload timer ch.0 output pin (Port 1)	—	—
		INT18_1		External interrupt request 18 input pin (Port 1)	—	○
73	P9	PA3	E	General-purpose I/O port	—	○
		AN19		10-bit A/D converter ch.19 analog input pin	—	—
		TMO1_1		16-bit reload timer ch.1 output pin (Port 1)	—	—
		INT19_1		External interrupt request 19 input pin (Port 1)	—	○
74	N9	PA4	E	General-purpose I/O port	—	○
		AN20		10-bit A/D converter ch.20 analog input pin	—	—
		TMO2_1		16-bit reload timer ch.2 output pin (Port 1)	—	—
		INT20_1		External interrupt request 20 input pin (Port 1)	—	○
75	M9	PA5	E	General-purpose I/O port	—	○
		AN21		10-bit A/D converter ch.21 analog input pin	—	—
		TMI0_1		16-bit reload timer ch.0 input pin (Port 1)	—	○
		INT21_1		External interrupt request 21 input pin (Port 1)	—	○

(Continued)

MB91645A Series

Pin no.		Pin name	I/O circuit type*3	Function	CMOS level input	CMOS level hysteresis input
LQFP*1	PFBGA*2					
76	L9	PA6	E	General-purpose I/O port	—	○
		AN22		10-bit A/D converter ch.22 analog input pin	—	—
		TMI1_1		16-bit reload timer ch.1 input pin (Port 1)	—	○
		INT22_1		External interrupt request 22 input pin (Port 1)	—	○
77	P10	PA7	E	General-purpose I/O port	—	○
		AN23		10-bit A/D converter ch.23 analog input pin	—	—
		TMI2_1		16-bit reload timer ch.2 input pin (Port 1)	—	○
		INT23_1		External interrupt request 23 input pin (Port 1)	—	○
78	N10	PB0	E	General-purpose I/O port	—	○
		AN24		10-bit A/D converter ch.24 analog input pin	—	—
		INT24_1		External interrupt request 24 input pin (Port 1)	—	○
79	M10	PB1	E	General-purpose I/O port	—	○
		AN25		10-bit A/D converter ch.25 analog input pin	—	—
		INT25_1		External interrupt request 25 input pin (Port 1)	—	○
80	L10	PB2	E	General-purpose I/O port	—	○
		AN26		10-bit A/D converter ch.26 analog input pin	—	—
		INT26_1		External interrupt request 26 input pin (Port 1)	—	○
81	P11	PB3	E	General-purpose I/O port	—	○
		AN27		10-bit A/D converter ch.27 analog input pin	—	—
		INT27_1		External interrupt request 27 input pin (Port 1)	—	○
82	N11	PB4	E	General-purpose I/O port	—	○
		AN28		10-bit A/D converter ch.28 analog input pin	—	—
		INT28_1		External interrupt request 28 input pin (Port 1)	—	○

(Continued)

MB91645A Series

Pin no.		Pin name	I/O circuit type*3	Function	CMOS level input	CMOS level hysteresis input
LQFP*1	PFBGA*2					
83	M11	PB5	E	General-purpose I/O port	—	○
		AN29		10-bit A/D converter ch.29 analog input pin	—	—
		INT29_1		External interrupt request 29 input pin (Port 1)	—	○
84	K10	PB6	E	General-purpose I/O port	—	○
		AN30		10-bit A/D converter ch.30 analog input pin	—	—
		INT30_1		External interrupt request 30 input pin (Port 1)	—	○
85	P12	PB7	E	General-purpose I/O port	—	○
		AN31		10-bit A/D converter ch.31 analog input pin	—	—
		INT31_1		External interrupt request 31 input pin (Port 1)	—	○
86	N12	P50	C	General-purpose I/O port	—	○
		$\overline{CS0}$		External bus interface chip select 0 output pin	—	—
		SOUT10 (SDA10)		Multifunction serial interface ch.10 output pin. This pin operates as SOUT10 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA10 when it is used in an I ² C (operation mode 4).	—	○
		AIN0_1		Up/Down counter ch.0 AIN input pin (Port 1)	—	○
87	M12	P51	C	General-purpose I/O port	—	○
		$\overline{CS1}$		External bus interface chip select 1 output pin	—	—
		SIN10		Multifunction serial interface ch.10 input pin	—	○
		BIN0_1		Up/Down counter ch.0 BIN input pin (Port 1)	—	○
88	P13	V _{ss}	—	GND pin	—	—
89	N14	V _{cc}	—	3.3V power supply pin	—	—

(Continued)

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Pin no.		Pin name	I/O circuit type*3	Function	CMOS level input	CMOS level hysteresis input
LQFP*1	PFBGA*2					
90	N13	P52	C	General-purpose I/O port	—	○
		$\overline{CS2}$		External bus interface chip select 2 output pin	—	—
		SCK10 (SCL10)		Multifunction serial interface ch.10 clock I/O pin. This pin operates as SCK10 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL10 when it is used in an I ² C (operation mode 4).	—	○
		ZIN0_1		Up/Down counter ch.0 ZIN input pin (Port 1)	—	○
91	L11	P53	C	General-purpose I/O port	—	○
		$\overline{CS3}$		External bus interface chip select 3 output pin	—	—
		FRCK1		32-bit free-run timer ch.1 external clock input pin	—	○
		INT21_2		External interrupt request 21 input pin (Port 2)	—	○
92	M13	P54	C	General-purpose I/O port	—	○
		\overline{AS}		External bus interface address strobe output pin	—	—
		SOUT11 (SDA11)		Multifunction serial interface ch.11 output pin. This pin operates as SOUT11 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA11 when it is used in an I ² C (operation mode 4).	—	○
		AIN1_1		Up/Down counter ch.1 AIN input pin (Port 1)	—	○
93	M14	P55	C	General-purpose I/O port	—	○
		\overline{RD}		External bus interface read strobe output pin	—	—
		SIN11		Multifunction serial interface ch.11 input pin	—	○
		BIN1_1		Up/Down counter ch.1 BIN input pin (Port 1)	—	○
		ADTRG0		10-bit A/D converter external trigger input pin	—	○

(Continued)

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Pin no.		Pin name	I/O circuit type*3	Function	CMOS level input	CMOS level hysteresis input
LQFP*1	PFBGA*2					
94	L12	P56	C	General-purpose I/O port	—	○
		$\overline{WR0}$		External bus interface write strobe 0 output pin	—	—
		SCK11 (SCL11)		Multifunction serial interface ch.11 clock I/O pin. This pin operates as SCK11 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL11 when it is used in an I ² C (operation mode 4).	—	○
		ZIN1_1		Up/Down counter ch.1 ZIN input pin (Port 1)	—	○
		FRCK0		32-bit free-run timer ch.0 external clock input pin	—	○
95	K11	P57	C	General-purpose I/O port	—	○
		$\overline{WR1}$		External bus interface write strobe 1 output pin	—	—
96	L13	P60	B	General-purpose I/O port	—	○
		RDY		External bus interface ready input pin	○	—
		AIN2_1		Up/Down counter ch.2 AIN input pin (Port 1)	—	○
97	L14	P61	C	General-purpose I/O port	—	○
		SYSCLK		External bus interface bus clock output pin	—	—
		BIN2_1		Up/Down counter ch.2 BIN input pin (Port 1)	—	○
98	J10	P62	C	General-purpose I/O port	—	○
		DREQ0		DMA controller (DMAC) ch.0 transfer request input pin	—	○
		ZIN2_1		Up/Down counter ch.2 ZIN input pin (Port 1)	—	○
99	K12	P63	C	General-purpose I/O port	—	○
		DACK0		DMA controller (DMAC) ch.0 transfer request acceptance signal output pin	—	—
		FRCK1_1		32-bit free-run timer ch.1 external clock input pin (Port 1)	—	○
		INT22_2		External interrupt request 22 input pin (Port 2)	—	○

(Continued)

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Pin no.		Pin name	I/O circuit type*3	Function	CMOS level input	CMOS level hysteresis input
LQFP*1	PFBGA*2					
100	K13	P64	C	General-purpose I/O port	—	○
		DEOP0		DMA controller (DMAC) ch.0 last transfer signal output pin	—	—
		AIN3_1		Up/Down counter ch.3 AIN input pin (Port 1)	—	○
101	K14	P65	C	General-purpose I/O port	—	○
		DREQ1		DMA controller (DMAC) ch.1 transfer request input pin	—	○
		BIN3_1		Up/Down counter ch.3 BIN input pin (Port 1)	—	○
		ADTRG0_1		10-bit A/D converter external trigger input pin (Port 1)	—	○
102	J11	P66	C	General-purpose I/O port	—	○
		DACK1		DMA controller (DMAC) ch.1 transfer request acceptance signal output pin	—	—
		ZIN3_1		Up/Down counter ch.3 ZIN input pin (Port 1)	—	○
		FRCK0_1		32-bit free-run timer ch.0 external clock input pin (Port 1)	—	○
103	J12	P67	C	General-purpose I/O port	—	○
		DEOP1		DMA controller (DMAC) ch.1 last transfer signal output pin	—	—
		INT23_2		External interrupt request 23 input pin (Port 2)	—	○
104	J13	V _{SS}	—	GND pin	—	—
105	J14	V _{DDI}	—	1.8V power supply pin	—	—
106	H11	P00	B	General-purpose I/O port	—	○
		D00		External bus interface data bus bit0	○	—
		TIOA0		Base timer ch.0 TIOA pin	—	—
		SOUT0_1		Multifunction serial interface ch.0 output pin (Port 1). This pin operates as SOUT0_1 when it is used in a UART/CSIO (operation modes 0 to 2).	—	—
		IN0		32-bit input capture ch.0 input pin	—	○

(Continued)

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Pin no.		Pin name	I/O circuit type*3	Function	CMOS level input	CMOS level hysteresis input
LQFP*1	PFBGA*2					
107	H12	P01	B	General-purpose I/O port	—	○
		D01		External bus interface data bus bit1	○	—
		TIOB0		Base timer ch.0 TIOB pin	—	○
		SIN0_1		Multifunction serial interface ch.0 input pin (Port 1)	—	○
		IN1		32-bit input capture ch.1 input pin	—	○
108	H13	P02	B	General-purpose I/O port	—	○
		D02		External bus interface data bus bit2	○	—
		TIOA1		Base timer ch.1 TIOA pin	—	○
		SCK0_1		Multifunction serial interface ch.0 clock I/O pin (Port 1). This pin operates as SCK0_1 when it is used in a UART/CSIO (operation modes 0 to 2).	—	○
		IN2		32-bit input capture ch.2 input pin	—	○
109	H14	P03	B	General-purpose I/O port	—	○
		D03		External bus interface data bus bit3	○	—
		TIOB1		Base timer ch.1 TIOB pin	—	○
		IN3		32-bit input capture ch.3 input pin	—	○
110	H10	P04	B	General-purpose I/O port	—	○
		D04		External bus interface data bus bit4	○	—
		TIOA2		Base timer ch.2 TIOA pin	—	—
		SOUT1 (SDA1)		Multifunction serial interface ch.1 output pin. This pin operates as SOUT1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA1 when it is used in an I ² C (operation mode 4).	—	○
		IN4		32-bit input capture ch.4 input pin	—	○
111	G10	P05	B	General-purpose I/O port	—	○
		D05		External bus interface data bus bit5	○	—
		TIOB2		Base timer ch.2 TIOB pin	—	○
		SIN1		Multifunction serial interface ch.1 input pin	—	○
		IN5		32-bit input capture ch.5 input pin	—	○

(Continued)

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Pin no.		Pin name	I/O circuit type*3	Function	CMOS level input	CMOS level hysteresis input
LQFP*1	PFBGA*2					
112	G11	P06	B	General-purpose I/O port	—	○
		D06		External bus interface data bus bit6	○	—
		TIOA3		Base timer ch.3 TIOA pin	—	○
		SCK1 (SCL1)		Multifunction serial interface ch.1 clock I/O pin. This pin operates as SCK1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL1 when it is used in an I ² C (operation mode 4).	—	○
		IN6		32-bit input capture ch.6 input pin	—	○
113	G14	P07	B	General-purpose I/O port	—	○
		D07		External bus interface data bus bit7	○	—
		TIOB3		Base timer ch.3 TIOB pin	—	○
		IN7		32-bit input capture ch.7 input pin	—	○
114	G13	P10	B	General-purpose I/O port	—	○
		D08		External bus interface data bus bit8	○	—
		TIOA4		Base timer ch.4 TIOA pin	—	—
		SOUT2 (SDA2)		Multifunction serial interface ch.2 output pin. This pin operates as SOUT2 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA2 when it is used in an I ² C (operation mode 4).	—	○
		AIN0		Up/Down counter ch.0 AIN input pin	—	○
		INT0		External interrupt request 0 input pin	—	○
115	G12	P11	B	General-purpose I/O port	—	○
		D09		External bus interface data bus bit9	○	—
		TIOB4		Base timer ch.4 TIOB pin	—	○
		SIN2		Multifunction serial interface ch.2 input pin	—	○
		BIN0		Up/Down counter ch.0 BIN input pin	—	○
		INT1		External interrupt request 1 input pin	—	○

(Continued)

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Pin no.		Pin name	I/O circuit type*3	Function	CMOS level input	CMOS level hysteresis input
LQFP*1	PFBGA*2					
116	F10	P12	B	General-purpose I/O port	—	○
		D10		External bus interface data bus bit10	○	—
		TIOA5		Base timer ch.5 TIOA pin	—	○
		SCK2 (SCL2)		Multifunction serial interface ch.2 clock I/O pin. This pin operates as SCK2 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL2 when it is used in an I ² C (operation mode 4).	—	○
		ZIN0		Up/Down counter ch.0 ZIN input pin	—	○
		INT2		External interrupt request 2 input pin	—	○
117	F14	P13	B	General-purpose I/O port	—	○
		D11		External bus interface data bus bit11	○	—
		TIOB5		Base timer ch.5 TIOB pin	—	○
		INT3		External interrupt request 3 input pin	—	○
118	F13	P14	B	General-purpose I/O port	—	○
		D12		External bus interface data bus bit12	○	—
		TIOA6		Base timer ch.6 TIOA pin	—	—
		SOUT3 (SDA3)		Multifunction serial interface ch.3 output pin. This pin operates as SOUT3 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA3 when it is used in an I ² C (operation mode 4).	—	○
		AIN1		Up/Down counter ch.1 AIN input pin	—	○
		INT4		External interrupt request 4 input pin	—	○
119	F12	P15	B	General-purpose I/O port	—	○
		D13		External bus interface data bus bit13	○	—
		TIOB6		Base timer ch.6 TIOB pin	—	○
		SIN3		Multifunction serial interface ch.3 input pin	—	○
		BIN1		Up/Down counter ch.1 BIN input pin	—	○
		INT5		External interrupt request 5 input pin	—	○

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Pin no.		Pin name	I/O circuit type*3	Function	CMOS level input	CMOS level hysteresis input
LQFP*1	PFBGA*2					
120	F11	P16	B	General-purpose I/O port	—	○
		D14		External bus interface data bus bit14	○	—
		TIOA7		Base timer ch.7 TIOA pin	—	○
		SCK3 (SCL3)		Multifunction serial interface ch.3 clock I/O pin. This pin operates as SCK3 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL3 when it is used in an I ² C (operation mode 4).	—	○
		ZIN1		Up/Down counter ch.1 ZIN input pin	—	○
		INT6		External interrupt request 6 input pin	—	○
121	E14	P17	B	General-purpose I/O port	—	○
		D15		External bus interface data bus bit15	○	—
		TIOB7		Base timer ch.7 TIOB pin	—	○
		INT7		External interrupt request 7 input pin	—	○
122	E13	P20	D*4	General-purpose I/O port	—	○
		A00		External bus interface address bus bit0	—	—
		TIOA8		Base timer ch.8 TIOA pin	—	—
		SOUT4 (SDA4)		Multifunction serial interface ch.4 output pin. This pin operates as SOUT4 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA4 when it is used in an I ² C (operation mode 4).	—	○
		AIN2		Up/Down counter ch.2 AIN input pin	—	○
123	E12	P21	D*4	General-purpose I/O port	—	○
		A01		External bus interface address bus bit1	—	—
		TIOB8		Base timer ch.8 TIOB pin	—	○
		SIN4		Multifunction serial interface ch.4 input pin	—	○
		BIN2		Up/Down counter ch.2 BIN input pin	—	○

(Continued)

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Pin no.		Pin name	I/O circuit type*3	Function	CMOS level input	CMOS level hysteresis input
LQFP*1	PFBGA*2					
124	E11	P22	D*4	General-purpose I/O port	—	○
		A02		External bus interface address bus bit2	—	—
		TIOA9		Base timer ch.9 TIOA pin	—	○
		SCK4 (SCL4)		Multifunction serial interface ch.4 clock I/O pin. This pin operates as SCK4 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL4 when it is used in an I ² C (operation mode 4).	—	○
		ZIN2		Up/Down counter ch.2 ZIN input pin	—	○
125	D14	P23	D*4	General-purpose I/O port	—	○
		A03		External bus interface address bus bit3	—	—
		TIOB9		Base timer ch.9 TIOB pin	—	○
126	D13	P24	D*4	General-purpose I/O port	—	○
		A04		External bus interface address bus bit4	—	—
		TIOA10		Base timer ch.10 TIOA pin	—	—
		SOUT5 (SDA5)		Multifunction serial interface ch.5 output pin. This pin operates as SOUT5 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA5 when it is used in an I ² C (operation mode 4).	—	○
		AIN3		Up/Down counter ch.3 AIN input pin	—	○
		OUT0		32-bit output compare ch.0 output pin	—	—
127	D12	P25	D*4	General-purpose I/O port	—	○
		A05		External bus interface address bus bit5	—	—
		TIOB10		Base timer ch.10 TIOB pin	—	○
		SIN5		Multifunction serial interface ch.5 input pin	—	○
		BIN3		Up/Down counter ch.3 BIN input pin	—	○
		OUT1		32-bit output compare ch.1 output pin	—	—

(Continued)

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Pin no.		Pin name	I/O circuit type*3	Function	CMOS level input	CMOS level hysteresis input
LQFP*1	PFBGA*2					
128	E10	P26	D*4	General-purpose I/O port	—	○
		A06		External bus interface address bus bit6	—	—
		TIOA11		Base timer ch.11 TIOA pin	—	○
		SCK5 (SCL5)		Multifunction serial interface ch.5 clock I/O pin. This pin operates as SCK5 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL5 when it is used in an I ² C (operation mode 4).	—	○
		ZIN3		Up/Down counter ch.3 ZIN input pin	—	○
		OUT2		32-bit output compare ch.2 output pin	—	—
129	C14	P27	D*4	General-purpose I/O port	—	○
		A07		External bus interface address bus bit7	—	—
		TIOB11		Base timer ch.11 TIOB pin	—	○
		OUT3		32-bit output compare ch.3 output pin	—	—
130	C13	P30	D*4	General-purpose I/O port	—	○
		A08		External bus interface address bus bit8	—	—
		TIOA12		Base timer ch.12 TIOA pin	—	—
		SOUT6 (SDA6)		Multifunction serial interface ch.6 output pin. This pin operates as SOUT6 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA6 when it is used in an I ² C (operation mode 4).	—	○
		INT8		External interrupt request 8 input pin	—	○
131	C12	P31	D*4	General-purpose I/O port	—	○
		A09		External bus interface address bus bit9	—	—
		TIOB12		Base timer ch.12 TIOB pin	—	○
		SIN6		Multifunction serial interface ch.6 input pin	—	○
		INT9		External interrupt request 9 input pin	—	○
132	B14	V _{ss}	—	GND pin	—	—
133	A13	V _{cc}	—	3.3V power supply pin	—	—

(Continued)

MB91645A Series

Pin no.		Pin name	I/O circuit type*3	Function	CMOS level input	CMOS level hysteresis input
LQFP*1	PFBGA*2					
134	B13	P32	D*4	General-purpose I/O port	—	○
		A10		External bus interface address bus bit10	—	—
		TIOA13		Base timer ch.13 TIOA pin	—	○
		SCK6 (SCL6)		Multifunction serial interface ch.6 clock I/O pin. This pin operates as SCK6 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL6 when it is used in an I ² C (operation mode 4).	—	○
		INT10		External interrupt request 10 input pin	—	○
135	D11	P33	D*4	General-purpose I/O port	—	○
		A11		External bus interface address bus bit11	—	—
		TIOB13		Base timer ch.13 TIOB pin	—	○
		INT11		External interrupt request 11 input pin	—	○
136	B12	P34	D*4	General-purpose I/O port	—	○
		A12		External bus interface address bus bit12	—	—
		TIOA14		Base timer ch.14 TIOA pin	—	—
		SOUT7 (SDA7)		Multifunction serial interface ch.7 output pin. This pin operates as SOUT7 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA7 when it is used in an I ² C (operation mode 4).	—	○
		OUT4		32-bit output compare ch.4 output pin	—	—
		INT12		External interrupt request 12 input pin	—	○

(Continued)

MB91645A Series

Pin no.		Pin name	I/O circuit type*3	Function	CMOS level input	CMOS level hysteresis input
LQFP*1	PFBGA*2					
137	A12	P35	D*4	General-purpose I/O port	—	○
		A13		External bus interface address bus bit13	—	—
		TIOB14		Base timer ch.14 TIOB pin	—	○
		SIN7		Multifunction serial interface ch.7 input pin	—	○
		OUT5		32-bit output compare ch.5 output pin	—	—
		INT13		External interrupt request 13 input pin	—	○
138	C11	P36	D*4	General-purpose I/O port	—	○
		A14		External bus interface address bus bit14	—	—
		TIOA15		Base timer ch.15 TIOA pin	—	○
		SCK7 (SCL7)		Multifunction serial interface ch.7 clock I/O pin. This pin operates as SCK7 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL7 when it is used in an I ² C (operation mode 4).	—	○
		OUT6		32-bit output compare ch.6 output pin	—	—
		INT14		External interrupt request 14 input pin	—	○
139	D10	P37	D*4	General-purpose I/O port	—	○
		A15		External bus interface address bus bit15	—	—
		TIOB15		Base timer ch.15 TIOB pin	—	○
		OUT7		32-bit output compare ch.7 output pin	—	—
		INT15		External interrupt request 15 input pin	—	○

(Continued)

MB91645A Series

Pin no.		Pin name	I/O circuit type*3	Function	CMOS level input	CMOS level hysteresis input
LQFP*1	PFBGA*2					
140	B11	P40	D*4	General-purpose I/O port	—	○
		A16		External bus interface address bus bit16	—	—
		SOUT8 (SDA8)		Multifunction serial interface ch.8 output pin. This pin operates as SOUT8 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA8 when it is used in an I ² C (operation mode 4).	—	○
141	A11	P41	D*4	General-purpose I/O port	—	○
		A17		External bus interface address bus bit17	—	—
		SIN8		Multifunction serial interface ch.8 input pin	—	○
142	E9	P42	D*4	General-purpose I/O port	—	○
		A18		External bus interface address bus bit18	—	—
		SCK8 (SCL8)		Multifunction serial interface ch.8 clock I/O pin. This pin operates as SCK8 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL8 when it is used in an I ² C (operation mode 4).	—	○
143	C10	P43	D*4	General-purpose I/O port	—	○
		A19		External bus interface address bus bit19	—	—
144	B10	P44	D*4	General-purpose I/O port	—	○
		A20		External bus interface address bus bit20	—	—
		SOUT9 (SDA9)		Multifunction serial interface ch.9 output pin. This pin operates as SOUT9 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA9 when it is used in an I ² C (operation mode 4).	—	○
145	A10	P45	D*4	General-purpose I/O port	—	○
		A21		External bus interface address bus bit21	—	—
		SIN9		Multifunction serial interface ch.9 input pin	—	○

(Continued)

MB91645A Series

Pin no.		Pin name	I/O circuit type*3	Function	CMOS level input	CMOS level hysteresis input
LQFP*1	PFBGA*2					
146	D9	P46	D*4	General-purpose I/O port	—	○
		A22		External bus interface address bus bit22	—	—
		SCK9 (SCL9)		Multifunction serial interface ch.9 clock I/O pin. This pin operates as SCK9 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL9 when it is used in an I ² C (operation mode 4).	—	○
147	C9	P47	D*4	General-purpose I/O port	—	○
		A23		External bus interface address bus bit23	—	—
148	B9	V _{SS}	—	GND pin	—	—
149	A9	V _{DDI}	—	1.8 V power supply pin	—	—
150	D8	PH0	D*4	General-purpose I/O port	—	○
		TIOA4_1		Base timer ch.4 TIOA pin (Port 1)	—	—
		SOUT2_1 (SDA2_1)		Multifunction serial interface ch.2 output pin (Port 1). This pin operates as SOUT2_1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA2_1 when it is used in an I ² C (operation mode 4).	—	○
		AIN0_2		Up/Down counter ch.0 AIN input pin (Port 2)	—	○
		INT0_1		External interrupt request 0 input pin (Port 1)	—	○
151	C8	PH1	D*4	General-purpose I/O port	—	○
		TIOB4_1		Base timer ch.4 TIOB pin (Port 1)	—	○
		SIN2_1		Multifunction serial interface ch.2 input pin (Port 1)	—	○
		BIN0_2		Up/Down counter ch.0 BIN input pin (Port 2)	—	○
		INT1_1		External interrupt request 1 input pin (Port 1)	—	○

(Continued)

MB91645A Series

Pin no.		Pin name	I/O circuit type*3	Function	CMOS level input	CMOS level hysteresis input
LQFP*1	PFBGA*2					
152	B8	PH2	D*4	General-purpose I/O port	—	○
		TIOA5_1		Base timer ch.5 TIOA pin (Port 1)	—	○
		SCK2_1 (SCL2_1)		Multifunction serial interface ch.2 clock I/O pin (Port 1). This pin operates as SCK2_1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL2_1 when it is used in an I ² C (operation mode 4).	—	○
		ZIN0_2		Up/Down counter ch.0 ZIN input pin (Port 2)	—	○
		INT2_1		External interrupt request 2 input pin (Port 1)	—	○
153	A8	PH3	D*4	General-purpose I/O port	—	○
		TIOB5_1		Base timer ch.5 TIOB pin (Port 1)	—	○
		INT3_1		External interrupt request 3 input pin (Port 1)	—	○
154	E8	PH4	D*4	General-purpose I/O port	—	○
		TIOA6_1		Base timer ch.6 TIOA pin (Port 1)	—	—
		SOUT3_1 (SDA3_1)		Multifunction serial interface ch.3 output pin (Port 1). This pin operates as SOUT3_1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA3_1 when it is used in an I ² C (operation mode 4).	—	○
		AIN1_2		Up/Down counter ch.1 AIN input pin (Port 2)	—	○
		INT4_1		External interrupt request 4 input pin (Port 1)	—	○
155	E7	PH5	D*4	General-purpose I/O port	—	○
		TIOB6_1		Base timer ch.6 TIOB pin (Port 1)	—	○
		SIN3_1		Multifunction serial interface ch.3 input pin (Port 1)	—	○
		BIN1_2		Up/Down counter ch.1 BIN input pin (Port 2)	—	○
		INT5_1		External interrupt request 5 input pin (Port 1)	—	○

(Continued)

MB91645A Series

Pin no.		Pin name	I/O circuit type*3	Function	CMOS level input	CMOS level hysteresis input
LQFP*1	PFBGA*2					
156	D7	PH6	D*4	General-purpose I/O port	—	○
		TIOA7_1		Base timer ch.7 TIOA pin (Port 1)	—	○
		SCK3_1 (SCL3_1)		Multifunction serial interface ch.3 clock I/O pin (Port 1). This pin operates as SCK3_1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL3_1 when it is used in an I ² C (operation mode 4).	—	○
		ZIN1_2		Up/Down counter ch.1 ZIN input pin (Port 2)	—	○
		INT6_1		External interrupt request 6 input pin (Port 1)	—	○
157	A7	PH7	D*4	General-purpose I/O port	—	○
		TIOB7_1		Base timer ch.7 TIOB pin (Port 1)	—	○
		INT7_1		External interrupt request 7 input pin (Port 1)	—	○
158	B7	PG0	D*4	General-purpose I/O port	—	○
		DREQ2		DMA controller (DMAC) ch.2 transfer request input pin	—	○
		TIOA0_1		Base timer ch.0 TIOA pin (Port 1)	—	—
		SOUT0_2		Multifunction serial interface ch.0 output pin (Port 2). This pin operates as SOUT0_2 when it is used in a UART/CSIO (operation modes 0 to 2).	—	—
		IN0_2		32-bit input capture ch.0 input pin (Port 2)	—	○
159	C7	PG1	D*4	General-purpose I/O port	—	○
		DACK2		DMA controller (DMAC) ch.2 transfer request acceptance signal output pin	—	—
		TIOB0_1		Base timer ch.0 TIOB pin (Port 1)	—	○
		SIN0_2		Multifunction serial interface ch.0 input pin (Port 2)	—	○
		IN1_2		32-bit input capture ch.1 input pin (Port 2)	—	○

(Continued)

MB91645A Series

Pin no.		Pin name	I/O circuit type*3	Function	CMOS level input	CMOS level hysteresis input
LQFP*1	PFBGA*2					
160	E6	PG2	D*4	General-purpose I/O port	—	○
		DEOP2		DMA controller (DMAC) ch.2 last transfer signal output pin	—	—
		TIOA1_1		Base timer ch.1 TIOA pin (Port 1)	—	○
		SCK0_2		Multifunction serial interface ch.0 clock I/O pin (Port 2). This pin operates as SCK0_2 when it is used in a UART/CSIO (operation modes 0 to 2).	—	○
		IN2_2		32-bit input capture ch.2 input pin (Port 2)	—	○
161	A6	PG3	D*4	General-purpose I/O port	—	○
		DREQ3		DMA controller (DMAC) ch.3 transfer request input pin	—	○
		TIOB1_1		Base timer ch.1 TIOB pin (Port 1)	—	○
		IN3_2		32-bit input capture ch.3 input pin (Port 2)	—	○
162	B6	PG4	D*4	General-purpose I/O port	—	○
		DACK3		DMA controller (DMAC) ch.3 transfer request acceptance signal output pin	—	—
		TIOA2_1		Base timer ch.2 TIOA pin (Port 1)	—	—
		SOUT1_1 (SDA1_1)		Multifunction serial interface ch.1 output pin (Port 1). This pin operates as SOUT1_1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA1_1 when it is used in an I ² C (operation mode 4).	—	○
		IN4_2		32-bit input capture ch.4 input pin (Port 2)	—	○

(Continued)

MB91645A Series

Pin no.		Pin name	I/O circuit type*3	Function	CMOS level input	CMOS level hysteresis input
LQFP*1	PFBGA*2					
163	C6	PG5	D*4	General-purpose I/O port	—	○
		DEOP3		DMA controller (DMAC) ch.3 last transfer signal output pin	—	—
		TIOB2_1		Base timer ch.2 TIOB pin (Port 1)	—	○
		SIN1_1		Multifunction serial interface ch.1 input pin (Port 1)	—	○
		IN5_2		32-bit input capture ch.5 input pin (Port 2)	—	○
164	D6	PG6	D*4	General-purpose I/O port	—	○
		TIOA3_1		Base timer ch.3 TIOA pin (Port 1)	—	○
		SCK1_1 (SCL1_1)		Multifunction serial interface ch.1 clock I/O pin (Port 1). This pin operates as SCK1_1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL1_1 when it is used in an I ² C (operation mode 4).	—	○
		IN6_2		32-bit input capture ch.6 input pin (Port 2)	—	○
165	A5	PG7	D*4	General-purpose I/O port	—	○
		TIOB3_1		Base timer ch.3 TIOB pin (Port 1)	—	○
		IN7_2		32-bit input capture ch.7 input pin (Port 2)	—	○
166	B5	PI0	D*4	General-purpose I/O port	—	○
		TIOA8_1		Base timer ch.8 TIOA pin (Port 1)	—	—
		SOUT4_1 (SDA4_1)		Multifunction serial interface ch.4 output pin (Port 1). This pin operates as SOUT4_1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA4_1 when it is used in an I ² C (operation mode 4).	—	○
		AIN2_2		Up/Down counter ch.2 AIN input pin (Port 2)	—	○
167	C5	PI1	D*4	General-purpose I/O port	—	○
		TIOB8_1		Base timer ch.8 TIOB pin (Port 1)	—	○
		SIN4_1		Multifunction serial interface ch.4 input pin (Port 1)	—	○
		BIN2_2		Up/Down counter ch.2 BIN input pin (Port 2)	—	○

(Continued)

MB91645A Series

Pin no.		Pin name	I/O circuit type*3	Function	CMOS level input	CMOS level hysteresis input
LQFP*1	PFBGA*2					
168	D5	PI2	D*4	General-purpose I/O port	—	○
		TIOA9_1		Base timer ch.9 TIOA pin (Port 1)	—	○
		SCK4_1 (SCL4_1)		Multifunction serial interface ch.4 clock I/O pin (Port 1). This pin operates as SCK4_1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL4_1 when it is used in an I ² C (operation mode 4).	—	○
		ZIN2_2		Up/Down counter ch.2 ZIN input pin (Port 2)	—	○
169	A4	PI3	D*4	General-purpose I/O port	—	○
		TIOB9_1		Base timer ch.9 TIOB pin (Port 1)	—	○
170	B4	PI4	D*4	General-purpose I/O port	—	○
		TIOA10_1		Base timer ch.10 TIOA pin (Port 1)	—	—
		SOUT5_1 (SDA5_1)		Multifunction serial interface ch.5 output pin (Port 1). This pin operates as SOUT5_1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA5_1 when it is used in an I ² C (operation mode 4).	—	○
		AIN3_2		Up/Down counter ch.3 AIN input pin (Port 2)	—	○
		OUT0_2		32-bit output compare ch.0 output pin (Port 2)	—	—
171	C4	PI5	D*4	General-purpose I/O port	—	○
		TIOB10_1		Base timer ch.10 TIOB pin (Port 1)	—	○
		SIN5_1		Multifunction serial interface ch.5 input pin (Port 1)	—	○
		BIN3_2		Up/Down counter ch.3 BIN input pin (Port 2)	—	○
		OUT1_2		32-bit output compare ch.1 output pin (Port 2)	—	—

(Continued)

MB91645A Series

(Continued)

Pin no.		Pin name	I/O circuit type*3	Function	CMOS level input	CMOS level hysteresis input
LQFP*1	PFBGA*2					
172	E5	PI6	D*4	General-purpose I/O port	—	○
		TIOA11_1		Base timer ch.11 TIOA pin (Port 1)	—	○
		SCK5_1 (SCL5_1)		Multifunction serial interface ch.5 clock I/O pin (Port 1). This pin operates as SCK5_1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL5_1 when it is used in an I ² C (operation mode 4).	—	○
		ZIN3_2		Up/Down counter ch.3 ZIN input pin (Port 2)	—	○
		OUT2_2		32-bit output compare ch.2 output pin (Port 2)	—	—
173	A3	PI7	D*4	General-purpose I/O port	—	○
		TIOB11_1		Base timer ch.11 TIOB pin (Port 1)	—	○
		OUT3_2		32-bit output compare ch.3 output pin (Port 2)	—	—
174	B3	PC0	C	General-purpose I/O port	—	○
		TIOA12_1		Base timer ch.12 TIOA pin (Port 1)	—	—
		SOUT6_1 (SDA6_1)		Multifunction serial interface ch.6 output pin (Port 1). This pin operates as SOUT6_1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA6_1 when it is used in an I ² C (operation mode 4).	—	○
		INT8_1		External interrupt request 8 input pin (Port 1)	—	○
175	C3	PC1	C	General-purpose I/O port	—	○
		TIOB12_1		Base timer ch.12 TIOB pin (Port 1)	—	○
		SIN6_1		Multifunction serial interface ch.6 input pin (Port 1)	—	○
		INT9_1		External interrupt request 9 input pin (Port 1)	—	○
176	A2	V _{cc}	—	3.3 V power supply pin	—	—

*1: FPT-176P-M07

*2: BGA-176P-M04

*3: Refer to “■ I/O CIRCUIT TYPE” for details on the I/O circuit types.

*4: 5 V tolerant pin

MB91645A Series

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		<ul style="list-style-type: none"> • Oscillation feedback resistance approx. 1 MΩ • With standby control
B		<ul style="list-style-type: none"> • CMOS level output • CMOS level input • CMOS level hysteresis input • With pull-up control • With standby control <p>Notes:</p> <ul style="list-style-type: none"> • CMOS level input when input data, RDY pin of external bus interface. Input other than above situations, CMOS level hysteresis input. • When this pin is used as an I²C pin, the digital output P-ch transistor is always off.

(Continued)

Type	Circuit	Remarks
C	<p style="text-align: center;"> P-ch P-ch Digital output N-ch Digital output Pull-up control Digital input Standby control </p>	<ul style="list-style-type: none"> • CMOS level output • CMOS level hysteresis input • With pull-up control • With standby control <p>Note: When this pin is used as an I²C pin, the digital output P-ch transistor is always off.</p>
D	<p style="text-align: center;"> P-ch Digital output N-ch Digital output Digital input Standby control </p>	<ul style="list-style-type: none"> • CMOS level output • CMOS level hysteresis input • 5 V tolerant input • With standby control <p>Note: When this pin is used as an I²C pin, the digital output P-ch transistor is always off.</p>

(Continued)

MB91645A Series

Type	Circuit	Remarks
E	<p>The circuit diagram for Type E shows a CMOS output stage. It features a pull-up resistor connected to the input of a P-channel MOSFET. The gates of both P-channel and N-channel MOSFETs are driven by a common input signal. The P-channel MOSFET's source is connected to VDD, and its drain is connected to the output node. The N-channel MOSFET's source is connected to ground, and its drain is also connected to the output node. A resistor R is connected between the input and the gates of the MOSFETs. The input signal is also connected to a digital input pin with a pull-up resistor and an analog input pin with a pull-up resistor. Control signals include Input control, Digital input, Standby control, and Analog input.</p>	<ul style="list-style-type: none"> • CMOS level output • CMOS level hysteresis input • With input control • Analog input • With pull-up control • With standby control
F	<p>The circuit diagram for Type F is similar to Type E, but the output is an analog output. It features a pull-up resistor connected to the input of a P-channel MOSFET. The gates of both P-channel and N-channel MOSFETs are driven by a common input signal. The P-channel MOSFET's source is connected to VDD, and its drain is connected to the output node. The N-channel MOSFET's source is connected to ground, and its drain is also connected to the output node. A resistor R is connected between the input and the gates of the MOSFETs. The input signal is also connected to a digital input pin with a pull-up resistor and an analog output pin with a pull-up resistor. Control signals include Output control, Digital input, Standby control, and Analog output.</p>	<ul style="list-style-type: none"> • CMOS level output • CMOS level hysteresis input • With input control • Analog output • With pull-up control • With standby control

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Type	Circuit	Remarks
I	<p>The diagram for Type I shows two input pins, X1A and X0A. X1A is connected to a P-channel MOSFET (Digital output) and an N-channel MOSFET (Digital output). It also has a pull-up resistor (R) connected to a digital input and a standby control input. X0A is connected to a P-channel MOSFET (Digital output) and an N-channel MOSFET (Digital output). It also has a pull-up resistor (R) connected to a digital input and a standby control input. A clock input is also shown, connected to an inverter and an AND gate. The standby control signal is connected to an AND gate and an inverter.</p>	<ul style="list-style-type: none"> • Oscillation feedback resistance approx. 10 MΩ • CMOS level output • CMOS level hysteresis input • With standby control
P	<p>The diagram for Type P shows a stack of four N-channel MOSFETs. The top MOSFET is connected to a control pin. The bottom MOSFET is connected to a mode input with a pull-up resistor (R). The gates of the MOSFETs are connected to a common node.</p>	<ul style="list-style-type: none"> • Flash memory product only • CMOS level hysteresis input • High voltage control for testing Flash memory

■ PRECAUTIONS FOR HANDLING THE DEVICES

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your FUJITSU MICROELECTRONICS semiconductor devices.

1. Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

- Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

- Recommended Operating Conditions

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

- Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

- (1) Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

- (2) Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device. Therefore, avoid this type of connection.

- (3) Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

- Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNP junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

Note: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

- (a) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
- (b) Be sure that abnormal current flows do not occur during the power-on sequence.

- Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

- Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

- Precautions Related to Usage of Devices

FUJITSU MICROELECTRONICS semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with FUJITSU MICROELECTRONICS sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

2. Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under FUJITSU MICROELECTRONICS's recommended conditions. For detailed information about mount conditions, contact your sales representative.

- Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder.

In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

- Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. FUJITSU MICROELECTRONICS recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with FUJITSU MICROELECTRONICS ranking of recommended conditions.

- Lead-Free Packaging

Note: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

- Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

- (a) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
- (b) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5 °C and 30 °C. When you open Dry Package that recommends humidity 40% to 70% relative humidity.
- (c) When necessary, FUJITSU MICROELECTRONICS packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
- (d) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

- Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the FUJITSU MICROELECTRONICS recommended conditions for baking.

Condition: 125 °C/24 h

- Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

- (a) Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
- (b) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
- (c) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ). Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
- (d) Ground all fixtures and instruments, or protect with anti-static measures.
- (e) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

3. Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above. For reliable performance, do the following:

- (1) Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

- (2) Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

- (3) Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

- (4) Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

- (5) Smoke, Flame

Note: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of FUJITSU MICROELECTRONICS products in other special environmental conditions should consult with sales representatives.

MB91645A Series

■ HANDLING DEVICES

• Power supply pins

In products with multiple V_{CC} , V_{DDI} and V_{SS} pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with the V_{CC} , V_{DDI} and V_{SS} pins of this device at low impedance.

It is also advisable that a ceramic capacitor of approximately $0.1 \mu\text{F}$ be connected as a bypass capacitor between V_{CC} and V_{SS} pins, and V_{DDI} and V_{SS} pins near this device.

• Noise measurement of V_{DDI} pins (recommended)

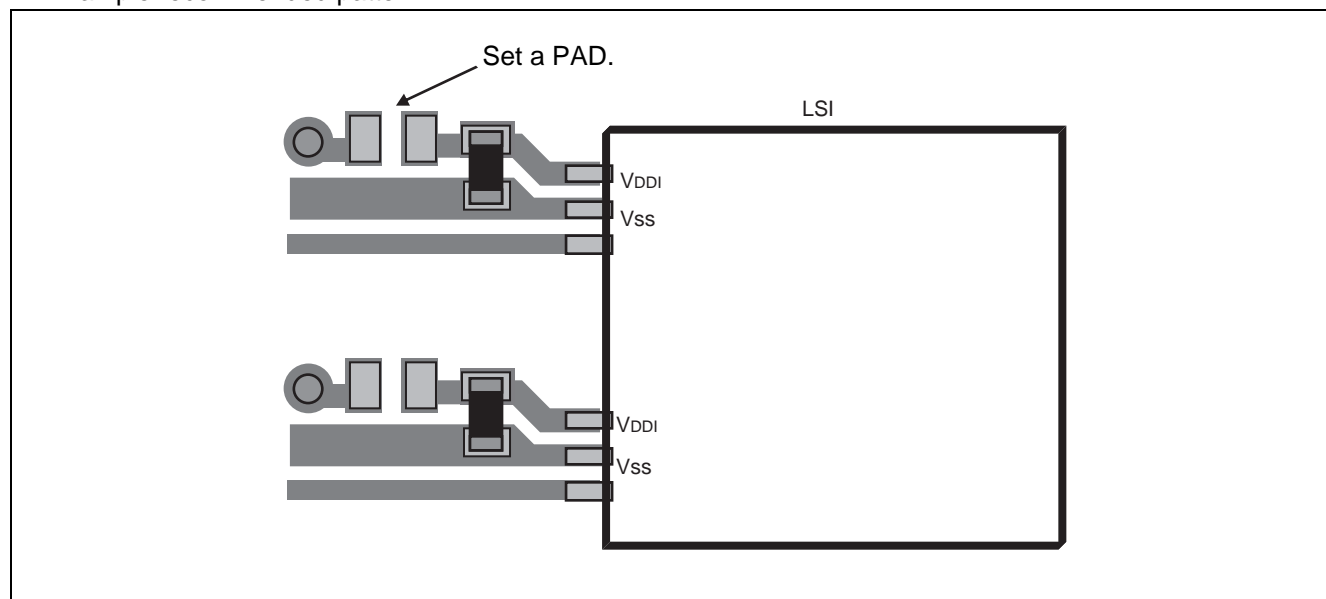
V_{DDI} pins are affected with a noise because internal core type of power-supply is used, and it may be a problem related with a radiated noise.

It is recommended to set a pad (land) to each V_{DDI} in advance, so that ferrites (beads) can be input (set decoupling capacitors and ferrites very close to LSI).

If a problem occurs with the radiated noise, insert ferrite parts.

(Connect the pads with 0Ω connector if ferrite parts are no longer required.)

Example recommended pattern



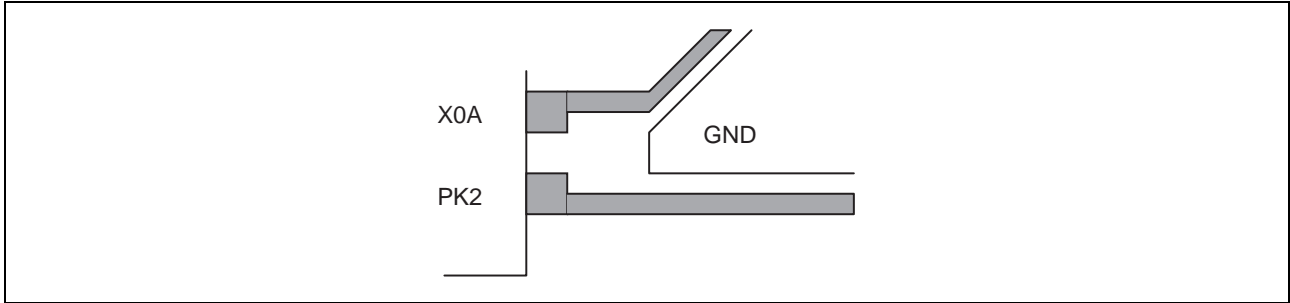
- Crystal oscillator circuit

Noise near the X0 and X1 pins may cause the device to malfunction. Design the printed circuit board so that X0, X1, the crystal oscillator (or ceramic oscillator), and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended that the PC board artwork be designed such that the X0 and X1 pins are surrounded by ground plane as this is expected to produce stable operation.

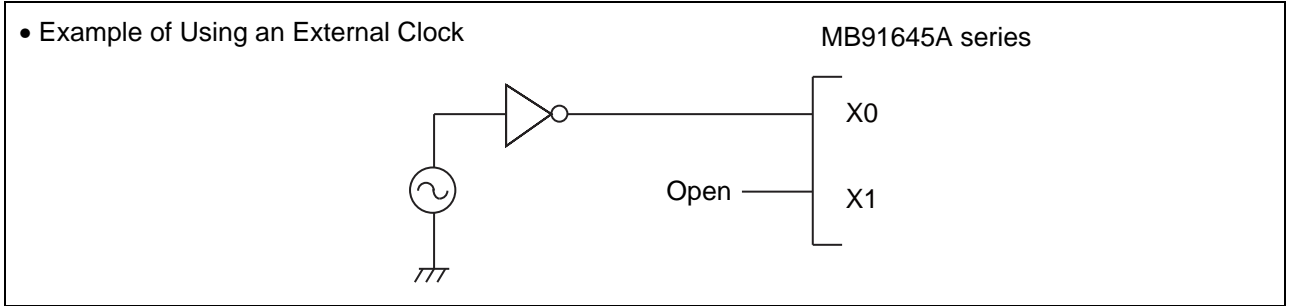
If a 32 kHz oscillator is used (X0A, X1A), use the PK2 pin for an input that changes as infrequently as possible. Furthermore, take steps such as shown in the following figure to prevent the X0A and PK2 wiring from running parallel to each other.

If 32 kHz oscillation is not used, there are no limitations.



- Using an external clock

When using an external clock, the clock signal should be input to the X0 pin only and the X1 should be kept open.



- Mode pins (MD0, MD1)

Connect the MD pin (MD0, MD1) directly to V_{CC} or V_{SS} pins. Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and V_{CC} pins or V_{SS} pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

MB91645A Series

- Notes on power-on
 - To ensure that the oscillator have stabilized immediately after the power is turned on, keep an “L” level input connected to the $\overline{\text{INIT}}$ pin for the duration of the oscillator start time of the oscillator + the main oscillator stabilization wait time.
 - Turn power on/off in the following order
 Turning on : $V_{\text{DDI}} \rightarrow V_{\text{CC}} \rightarrow AV_{\text{CC}} \rightarrow AVR_{\text{H}}$
 Turning off : $AVR_{\text{H}} \rightarrow AV_{\text{CC}} \rightarrow V_{\text{CC}} \rightarrow V_{\text{DDI}}$
- Release the reset ($\overline{\text{INIT}}$ pin “L” level to “H” level) after the power supply has stabilized.

- Caution on Operations during PLL Clock Mode

On this microcontroller, if in case the crystal oscillator breaks off or an external reference clock input stops while the PLL clock mode is selected, a self-oscillator circuit contained in the PLL may continue its operation at its self-running frequency.

However, Fujitsu Microelectronics will not guarantee results of operations if such failure occurs.

Note: Changes of PLL clock specification from MB91645 series

Product type	PLL macro oscillation clock frequency	Temperature range	PLL macro oscillation clock divider	PLL multiple rate
MB91F647	16 MHz to 60 MHz	- 20 °C to + 85 °C	Divided by 1 to 4	Multiplied by 15
	50 MHz to 60 MHz	- 40 °C to + 85 °C		
MB91F647A	80 MHz to 120 MHz	- 40 °C to + 85 °C	Divided by 2 to 4	Multiplied by 30

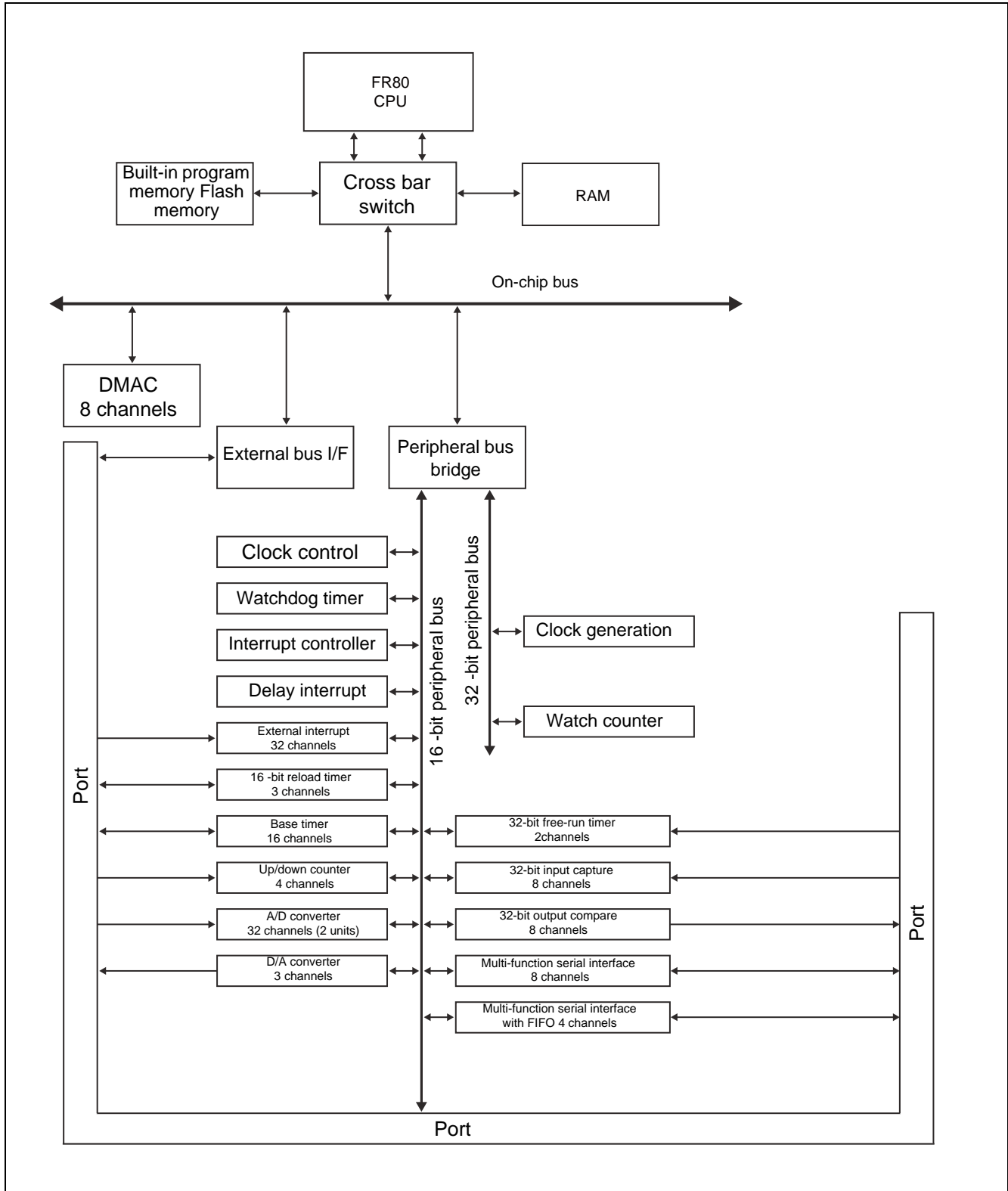
MB91645A series has been modified, and specifications of the PLL macro oscillation clock frequency, temperature range, PLL macro oscillation clock division value, and PLL multiple rate prohibit the setting of dividing by 1.

Therefore, please use the device with setting as dividing by 2 to 4 by ODS0 or ODS1 bit in the PLL configuration register (PLLCR).

Example) To use the PLL clock at 60MHz

Product type	PLL input clock frequency	PDS	ODS	PMS	PLL macro oscillation clock frequency
MB91F647	4 MHz	0000	00	1110	60 MHz
MB91F647A	4 MHz	0000	01	1110	120 MHz

■ BLOCK DIAGRAM



■ MEMORY SPACE

1. Memory Space

The FR family has 4 Gbytes of logical address space (2^{32} addresses) available to the CPU by linear access.

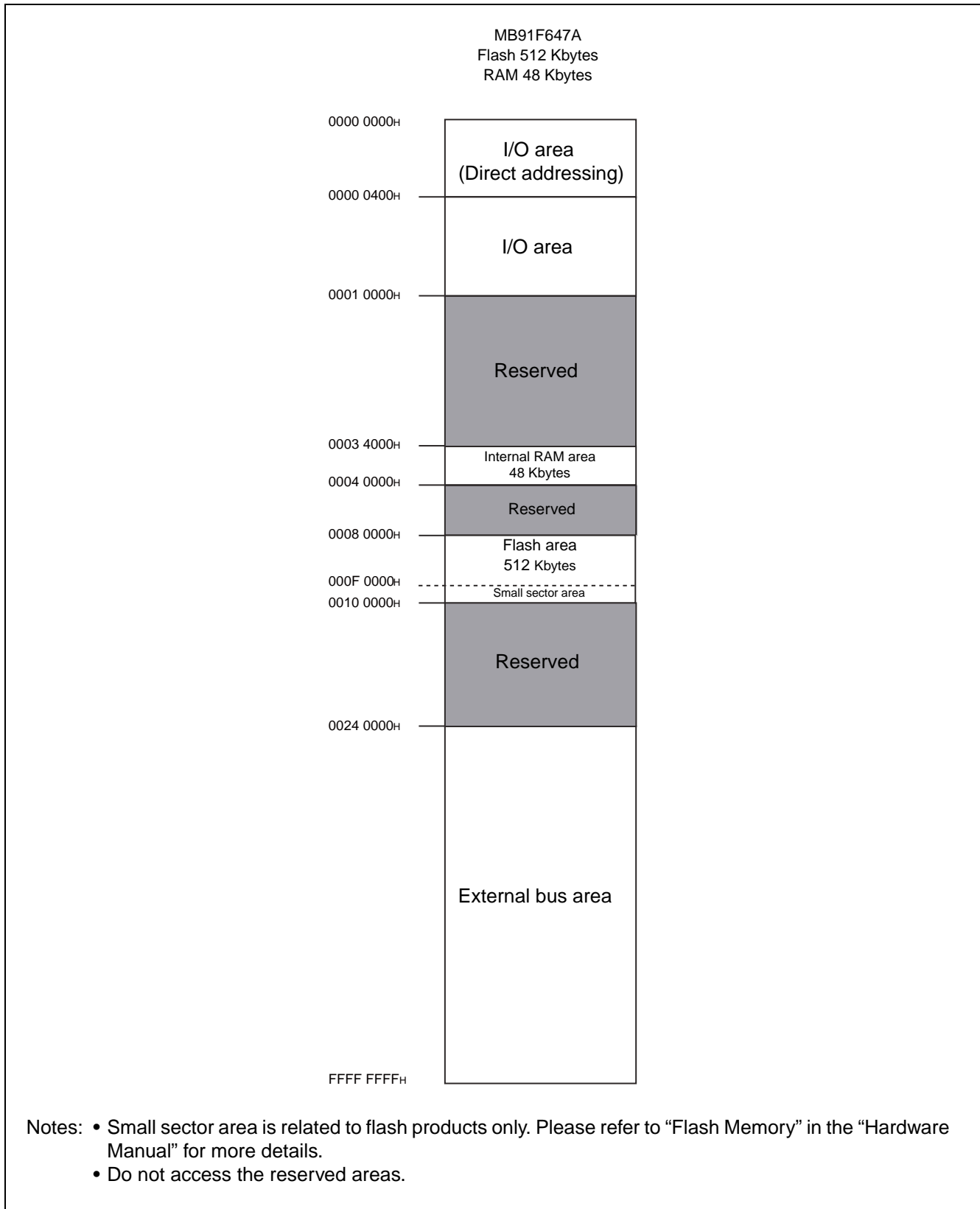
- Direct Addressing Areas

The following areas in the address space are used as I/O areas.

These areas are called direct addressing areas, and the address of an operand in these areas can be specified directly within an instruction. The size of the directly addressable area depends on the length of the data being accessed as follows.

- Byte data access : 0000 0000_H to 0000 00FF_H
- Half word data access : 0000 0000_H to 0000 01FF_H
- Word data access : 0000 0000_H to 0000 03FF_H

2. Memory Map



MB91645A Series

■ I/O MAP

[How to read the table]

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 0000 _H	PDR0 [R/W] B, H XXXXXXXX	PDR1 [R/W] B, H XXXXXXXX	PDR2 [R/W] B, H XXXXXXXXXXXX	PDR3 [R/W] B, H XXXXXXXX	Port data register
0000 003C _H	WDTCR0 [R/W] B, H -0--0000	WDTCPR0 [R/W] B, H 00000000	—		Watchdog timer
0000 0040 _H	EIRRO [R/W] B, H, W 000 0000	ENIRO [R/W] B, H, W 00000000	ELVR0 [R/W] B, H, W 00000000 00000000		External interrupt 0 to 7

Initial value after reset
 "1" : Initial value "1"
 "0" : Initial value "0"
 "X" : Initial value undefined
 "-" : Reserved bit or undefined bit

Access unit
 (B : byte, H : half word, W : word)

Read/write attribute
 "R" : Indicates that there is a read only bit.
 "R/W" : Indicates that there is a read/write bit.
 "W" : Indicates that there is a write only bit.

Register name (column 1 of the register is at address 4n, column 2 is at address 4n + 2...)

Leftmost register address (For word-length access, column 1 of the register is the MSB of the data.)

- Notes:
- When performing a data access, the addresses should be as below.
 - Word access : Address should be multiples of 4 (least significant 2 bits should be "00_b")
 - Half word access : Address should be multiples of 2 (least significant bit should be "0_b")
 - Byte access : —
 - Do not access the reserved areas.

MB91645A Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 0000 _H	PDR0 [R/W] B,H XXXXXXXX	PDR1 [R/W] B,H XXXXXXXX	PDR2 [R/W] B,H XXXXXXXX	PDR3 [R/W] B,H XXXXXXXX	Port data register
0000 0004 _H	PDR4 [R/W] B,H XXXXXXXX	PDR5 [R/W] B,H XXXXXXXX	PDR6 [R/W] B,H XXXXXXXX	PDR7[R/W] B,H XXXXXXXX	
0000 0008 _H	PDR8 [R/W] B,H XXXXXXXX	PDR9 [R/W] B,H ----XXX	PDRA [R/W] B,H XXXXXXXX	PDRB[R/W] B,H XXXXXXXX	
0000 000C _H	PDRC [R/W] B,H XXXXXXXX	PDRD [R/W] B,H XXXXXXXX	PDRE [R/W] B,H XXXXXXXX	PDRF [R/W] B,H -XXXXXXXX	
0000 0010 _H	PDRG [R/W] B,H XXXXXXXX	PDRH [R/W] B,H XXXXXXXX	PDRI [R/W] B,H XXXXXXXX	PDRJ [R/W] B,H ----XXX	
0000 0014 _H	PDRK [R/W] B ----XXXX	—			
0000 0018 _H to 0000 001C _H	—				Reserved
0000 0020 _H to 0000 0038 _H	—				
0000 003C _H	WDTCR0[R/W] B,H -0--0000	WDTCPR0[R/W] B,H 00000000	—		Watchdog timer
0000 0040 _H	EIRR0[R/W] B,H,W 00000000	ENIR0[R/W] B,H,W 00000000	ELVR0[R/W] B,H,W 00000000 00000000		External interrupt 0 to 7
0000 0044 _H	DICR [R/W] B -----0	—			Delay interrupt
0000 0048 _H	TMRLRA0 [R/W] H XXXXXXXX XXXXXXXX		TMR0 [R] H XXXXXXXX XXXXXXXX		16-bit reload timer ch.0
0000 004C _H	—		TMCSR0 [R/W] H --000000 --000000		
0000 0050 _H	TMRLRA1 [R/W] H XXXXXXXX XXXXXXXX		TMR1 [R] H XXXXXXXX XXXXXXXX		16-bit reload timer ch.1
0000 0054 _H	—		TMCSR1 [R/W] H --000000 --000000		
0000 0058 _H	TMRLRA2 [R/W] H XXXXXXXX XXXXXXXX		TMR2 [R] H XXXXXXXX XXXXXXXX		16-bit reload timer ch.2
0000 005C _H	—		TMCSR2 [R/W] H --000000 --000000		

(Continued)

MB91645A Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 0060 _H	SCR0 [R/W] B,H,W 0--00000	SMR0 [R/W] B,H,W 000-0000	SSR0 [R,R/W] B,H,W 0-000011	ESCR0 [R/W] B,H,W -0000000	Multi-function serial interface ch.0
0000 0064 _H	RDR0[R]/TDR0[W] B,H,W*1 -----0 00000000		BGR10[R/W] H,W 00000000	BGR00[R/W] H,W 00000000	
0000 0068 _H	SCR1 [R/W] / IBCR1 [R,R/W] B,H,W*2 0--00000	SMR1 [R/W] B,H,W 000-0000	SSR1 [R,R/W] B,H,W 0-000011	ESCR1 [R/W]/ IBSR1 [R,R/W] B,H,W*2 -0000000	Multi-function serial interface ch.1
0000 006C _H	RDR1[R]/TDR1[W] B,H,W*1 -----0 00000000		BGR11[R/W] H,W 00000000	BGR01[R/W] H,W 00000000	
0000 0070 _H	ISMK1 [R/W] B,H*2 -----	ISBA1 [R/W] B,H*2 -----	—		
0000 0074 _H	SCR2 [R/W] / IBCR2 [R,R/W] B,H,W*2 0--00000	SMR2 [R/W] B,H,W 000-0000	SSR2 [R,R/W] B,H,W 0-000011	ESCR2 [R/W]/ IBSR2 [R,R/W] B,H,W*2 -0000000	Multi-function serial interface ch.2
0000 0078 _H	RDR2[R]/TDR2[W] B,H,W*1 -----0 00000000		BGR12[R/W] H,W 00000000	BGR02[R/W] H,W 00000000	
0000 007C _H	ISMK2 [R/W] B,H*2 -----	ISBA2 [R/W] B,H*2 -----	—		
0000 0080 _H	SCR3 [R/W] / IBCR3 [R,R/W] B,H,W*2 0--00000	SMR3 [R/W] B,H,W 000-0000	SSR3 [R,R/W] B,H,W 0-000011	ESCR3 [R/W]/ IBSR3 [R,R/W] B,H,W*2 -0000000	Multi-function serial interface ch.3
0000 0084 _H	RDR3[R]/TDR3[W] B,H,W*1 -----0 00000000		BGR13[R/W] H,W 00000000	BGR03[R/W] H,W 00000000	
0000 0088 _H	ISMK3 [R/W] B,H*2 -----	ISBA3 [R/W] B,H*2 -----	—		
0000 008C _H	SCR4 [R/W] / IBCR4 [R,R/W] B,H,W*2 0--00000	SMR4 [R/W] B,H,W 000-0000	SSR4 [R,R/W] B,H,W 0-000011	ESCR4 [R/W] / IBSR4 [R,R/W] B,H,W*2 -0000000	Multi-function serial interface ch.4
0000 0090 _H	RDR4[R]/TDR4[W] B,H,W*1 -----0 00000000		BGR14[R/W] H,W 00000000	BGR04[R/W] H,W 00000000	
0000 0094 _H	ISMK4 [R/W] B,H*2 -----	ISBA4 [R/W] B,H*2 -----	—		

(Continued)

MB91645A Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 0098 _H	SCR5 [R/W]/ IBCR5 [R,R/W] B,H,W*2 0--00000	SMR5 [R/W] B,H,W 000-0000	SSR5 [R,R/W] B,H,W 0-000011	ESCR5 [R/W]/ IBSR5 [R,R/W] B,H,W*2 -0000000	Multi-function serial interface ch.5
0000 009C _H	RDR5[R]/TDR5[W] B,H,W*1 -----0 00000000		BGR15 [R/W] H,W 00000000	BGR05 [R/W] H,W 00000000	
0000 00A0 _H	ISMK5 [R/W] B,H*2 -----	ISBA5 [R/W] B,H*2 -----	—		
0000 00A4 _H	SCR6 [R/W]/ IBCR6 [R,R/W] B,H,W*2 0--00000	SMR6 [R/W] B,H,W 000-0000	SSR6 [R,R/W] B,H,W 0-000011	ESCR6 [R/W]/ IBSR6 [R,R/W] B,H,W*2 -0000000	Multi-function serial interface ch.6
0000 00A8 _H	RDR6[R]/TDR6[W] B,H,W*1 -----0 00000000		BGR16 [R/W] H,W 00000000	BGR06 [R/W] H,W 00000000	
0000 00AC _H	ISMK6 [R/W] B,H*2 -----	ISBA6 [R/W] B,H*2 -----	—		
0000 00B0 _H	SCR7 [R/W]/ IBCR7 [R,R/W] B,H,W*2 0--00000	SMR7 [R/W] B,H,W 000-0000	SSR7 [R,R/W] B,H,W 0-000011	ESCR7 [R/W]/ IBSR7 [R,R/W] B,H,W*2 -0000000	Multi-function serial interface ch.7
0000 00B4 _H	RDR7[R]/TDR7[W] B,H,W*1 -----0 00000000		BGR17 [R/W] H,W 00000000	BGR07 [R/W] H,W 00000000	
0000 00B8 _H	ISMK7 [R/W] B,H*2 -----	ISBA7 [R/W] B,H*2 -----	—		
0000 00BC _H	—				Reserved
0000 00C0 _H	RDRM0 [R]/ TDRM0 [W] B,H,W 00000000	RDRM1 [R]/ TDRM1 [W] B,H,W 00000000	RDRM2 [R]/ TDRM2 [W] B,H,W 00000000	RDRM3 [R]/ TDRM3 [W] B,H,W 00000000	Multi-function serial interface data register (mirror)
0000 00C4 _H	RDRM4 [R]/ TDRM4 [W] B,H,W 00000000	RDRM5 [R]/ TDRM5 [W] B,H,W 00000000	RDRM6 [R]/ TDRM6 [W] B,H,W 00000000	RDRM7 [R]/ TDRM7 [W] B,H,W 00000000	
0000 00C8 _H	SSEL0123 [R/W] B -----00	—	SSEL4567 [R/W] B -----00	—	Multi-function serial interface serial clock selection
0000 00CC _H	—				Reserved

(Continued)

MB91645A Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 00D0 _H	SCR8 [R/W]/ IBCR8 [R,R/W] B,H,W*2 0--00000	SMR8 [R/W] B,H,W 000-0000	SSR8 [R,R/W] B,H,W 0-000011	ESCR8 [R/W]/ IBSR8 [R,R/W] B,H,W*2 -0000000	Multi-function serial interface ch. 8 (FIFO)
0000 00D4 _H	RDR8[R]/TDR8[W] B,H,W*1 -----0 00000000		BGR18 [R/W] H,W 00000000	BGR08 [R/W] H,W 00000000	
0000 00D8 _H	ISMK8 [R/W] B,H*2 -----	ISBA8 [R/W] B,H*2 -----	—		
0000 00DC _H	FCR18 [R/W] B,H,W ---00100	FCR08 [R,R/W] B,H,W -0000000	FBYTE28 [R/W] B,H,W 00000000	FBYTE18 [R/W] B,H,W 00000000	
0000 00E0 _H	SCR9 [R/W]/ IBCR9 [R,R/W] B,H,W*2 0--00000	SMR9 [R/W] B,H,W 000-0000	SSR9 [R,R/W] B,H,W 0-000011	ESCR9 [R/W]/ IBSR9 [R,R/W] B,H,W*2 -0000000	Multi-function serial interface ch. 9 (FIFO)
0000 00E4 _H	RDR9[R]/TDR9[W] B,H,W*1 -----0 00000000		BGR19 [R/W] H,W 00000000	BGR09 [R/W] H,W 00000000	
0000 00E8 _H	ISMK9 [R/W] B,H*2 -----	ISBA9 [R/W] B,H*2 -----	—		
0000 00EC _H	FCR19 [R/W] B,H,W ---00100	FCR09 [R,R/W] B,H,W -0000000	FBYTE29 [R/W] B,H,W 00000000	FBYTE19 [R/W] B,H,W 00000000	
0000 00F0 _H	SCR10 [R/W]/ IBCR10 [R,R/W] B,H,W*2 0--00000	SMR10 [R/W] B,H,W 000-0000	SSR10 [R,R/W] B,H,W 0-000011	ESCR10 [R/W]/ IBSR10 [R,R/W] B,H,W*2 -0000000	Multi-function serial interface ch.10 (FIFO)
0000 00F4 _H	RDR10[R]/TDR10[W] B,H,W*1 -----0 00000000		BGR110 [R/W] H,W 00000000	BGR010 [R/W] H,W 00000000	
0000 00F8 _H	ISMK10 [R/W] B,H*2 -----	ISBA10 [R/W] B,H*2 -----	—		
0000 00FC _H	FCR110 [R/W] B,H,W ---00100	FCR010 [R,R/W] B,H,W -0000000	FBYTE210 [R/W] B,H,W 00000000	FBYTE110 [R/W] B,H,W 00000000	

(Continued)

MB91645A Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 0100 _H	SCR11 [R/W]/ IBCR11 [R,R/W] B,H,W*2 0--00000	SMR11 [R/W] B,H,W 000-0000	SSR11 [R,R/W] B,H,W 0-000011	ESCR11 [R/W]/ IBSR11 [R,R/W] B,H,W*2 -0000000	Multi-function serial interface ch.11 (FIFO)
0000 0104 _H	RDR11[R]/TDR11[W] B,H,W*1 -----0 00000000		BGR111 [R/W] H,W 00000000	BGR011 [R/W] H,W 00000000	
0000 0108 _H	ISMK11 [R/W] B,H*2 -----	ISBA11 [R/W] B,H*2 -----	—		
0000 010C _H	FCR111 [R/W] B,H,W ---00100	FCR011 [R,R/W] B,H,W -0000000	FBYTE211 [R/W] B,H,W 00000000	FBYTE111 [R/W] B,H,W 00000000	
0000 0110 _H	EIRR1[R/W] B,H,W 00000000	ENIR1[R/W] B,H,W 00000000	ELVR1[R/W] B,H,W 00000000 00000000		External interrupt 8 to 15
0000 0114 _H	EIRR2[R/W] B,H,W 00000000	ENIR2[R/W] B,H,W 00000000	ELVR2[R/W] B,H,W 00000000 00000000		External interrupt 16 to 23
0000 0118 _H	EIRR3[R/W] B,H,W 00000000	ENIR3[R/W] B,H,W 00000000	ELVR3[R/W] B,H,W 00000000 00000000		External interrupt 24 to 31
0000 011C _H	—				Reserved
0000 0120 _H	ADCR0[R/W] B,H 000-0000	ADSR0[R,R/W] B,H 00---000	—		A/D converter unit 0
0000 0124 _H	SCCR0[R,R/W] B,H 1000-000	SFNS0[R/W] B,H ----0000	SCFD0[R] B,H XXXXXXXX XX-XXXXX		
0000 0128 _H	SCIS30[R/W] B,H,W 00000000	SCIS20[R/W] B,H,W 00000000	SCIS10[R/W] B,H,W 00000000	SCIS00[R/W] B,H,W 00000000	
0000 012C _H	PCCR0[R,R/W] B,H 1000-000	PFNS0[R/W] B,H -----00	PCFD0[R] B,H XXXXXXXX XXXXXXXX		
0000 0130 _H	PCIS0[R/W] B 00000000	—	CMPD0[R/W] B,H 00000000	CMPCR0[R/W] B,H 00000000	
0000 0134 _H	ADSS30[R/W] B,H,W 00000000	ADSS20[R/W] B,H,W 00000000	ADSS10[R/W] B,H,W 00000000	ADSS00[R/W] B,H,W 00000000	
0000 0138 _H	ADST00[R/W] B,H 00100000	ADST10[R/W] B,H 00100000	ADCT0[R/W] B -----111	—	

(Continued)

MB91645A Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 013C _H	—				Reserved
0000 0140 _H	BT0TMR[R]H 00000000 00000000		BT0TMCR[R/W] B,H -0000000 00000000		Base timer ch.0
0000 0144 _H	—	BT0STC[R/W]B 0000-000	—		
0000 0148 _H	BT0PCSR/BT0PRL[R/W]H XXXXXXXX XXXXXXXX		BT0PDUT/BT0PRLH/BT0DTBF[R/W]H XXXXXXXX XXXXXXXX		
0000 014C _H	—				
0000 0150 _H	BT1TMR[R]H 00000000 00000000		BT1TMCR[R/W] B,H -0000000 00000000		Base timer ch.1
0000 0154 _H	—	BT1STC[R/W]B 0000-000	—		
0000 0158 _H	BT1PCSR/BT1PRL[R/W]H XXXXXXXX XXXXXXXX		BT1PDUT/BT1PRLH/BT1DTBF[R/W]H XXXXXXXX XXXXXXXX		
0000 015C _H	—				
0000 0160 _H	BT2TMR[R]H 00000000 00000000		BT2TMCR [R/W] B,H -0000000 00000000		Base timer ch.2
0000 0164 _H	—	BT2STC[R/W]B 0000-000	—		
0000 0168 _H	BT2PCSR/BT2PRL[R/W]H XXXXXXXX XXXXXXXX		BT2PDUT/BT2PRLH/BT2DTBF[R/W]H XXXXXXXX XXXXXXXX		
0000 016C _H	—				
0000 0170 _H	BT3TMR[R]H 00000000 00000000		BT3TMCR[R/W] B,H -0000000 00000000		Base timer ch.3
0000 0174 _H	—	BT3STC[R/W]B 0000-000	—		
0000 0178 _H	BT3PCSR/BT3PRL[R/W]H XXXXXXXX XXXXXXXX		BT3PDUT/BT3PRLH/BT3DTBF[R/W]H XXXXXXXX XXXXXXXX		
0000 017C _H	BTSEL0123 [R/W] B 00000000	—			
0000 0180 _H	DACR0[R/W] B,H,W -----0	DADR0[R/W] B,H,W XXXXXXXX	DACR1[R/W] B,H,W -----0	DADR1[R/W] B,H,W XXXXXXXX	D/A converter
0000 0184 _H	DACR2[R/W] B,H -----0	DADR2[R/W] B,H XXXXXXXX	—		
0000 0188 _H to 0000 018C _H	—				

(Continued)

MB91645A Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 0190 _H	ADCR1[R/W] B,H 000-0000	ADSR1[R,R/W] B,H 00---000	—		A/D converter unit 1
0000 0194 _H	SCCR1[R,R/W] B,H 1000-000	SFNS1[R/W] B,H ----0000	SCFD1[R] B,H XXXXXXXX XX-XXXXX		
0000 0198 _H	SCIS31[R/W] B,H,W 00000000	SCIS21[R/W] B,H,W 00000000	SCIS11[R/W] B,H,W 00000000	SCIS01[R/W] B,H,W 00000000	
0000 019C _H	PCCR1[R,R/W] B,H 1000-000	PFNS1[R/W] B,H -----00	PCFD1[R] B,H XXXXXXXX XXXXXXXX		
0000 01A0 _H	PCIS1[R/W] B 00000000	—	CMPD1[R/W] B,H 00000000	CMPCR1[R/W] B,H 00000000	
0000 01A4 _H	ADSS31[R/W] B,H,W 00000000	ADSS21[R/W] B,H,W 00000000	ADSS11[R/W] B,H,W 00000000	ADSS01[R/W] B,H,W 00000000	
0000 01A8 _H	ADST01[R/W] B,H 00100000	ADST11[R/W] B,H 00100000	ADCT1[R/W] B ----111	—	
0000 01AC _H	ADCHE [R/W] B,H,W 11111111 11111111 11111111 11111111				A/D channel enable
0000 01B0 _H	IRPR0H [R] B 000-----	—	IRPR1H [R] B,H 000-000-	IRPR1L [R] B,H 000-000-	Interrupt request batch read function
0000 01B4 _H	IRPR2H [R] B,H,W 0000----	IRPR2L [R] B,H,W 000-----	IRPR3H [R] B,H,W 0000----	IRPR3L [R] B,H,W 00000---	
0000 01B8 _H	IRPR4H [R] B,H,W 0000----	IRPR4L [R] B,H,W 000000--	IRPR5H [R] B,H,W 0000----	IRPR5L [R] B,H,W 0000----	
0000 01BC _H	IRPR6H [R] B,H,W 0000----	IRPR6L [R] B,H,W 0000----	IRPR7H [R] B,H,W 0000----	IRPR7L [R] B,H,W 0000----	
0000 01C0 _H	RCRH0 [W] H,W 00000000	RCRL0 [W] B,H,W 00000000	UDCRH0 [R] H,W 00000000	UDCRL0 [R] B,H,W 00000000	Up/down counter ch.0
0000 01C4 _H	CCR0 [R,R/W] B,H 00000000 -0001000		—	CSR0 [R,R/W] B 00000000	
0000 01C8 _H	—				Reserved
0000 01CC _H	—				

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MB91645A Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 01D0 _H	RCRH1 [W] H,W 00000000	RCRL1 [W] B,H,W 00000000	UDCRH1 [R] H,W 00000000	UDCRL1 [R] B,H,W 00000000	Up/down counter ch.1
0000 01D4 _H	CCR1 [R,R/W] B,H 00000000 -0001000		—	CSR1 [R,R/W] B 00000000	
0000 01D8 _H	—				
0000 01DC _H	—				Reserved
0000 01E0 _H	RCRH2 [W] H,W 00000000	RCRL2 [W] B,H,W 00000000	UDCRH2 [R] H,W 00000000	UDCRL2 [R] B,H,W 00000000	Up/down counter ch.2
0000 01E4 _H	CCR2 [R,R/W] B,H 00000000 -0001000		—	CSR2 [R,R/W] B 00000000	
0000 01E8 _H	—				
0000 01EC _H	—				Reserved
0000 01F0 _H	RCRH3 [W] H,W 00000000	RCRL3 [W] B,H,W 00000000	UDCRH3 [R] H,W 00000000	UDCRL3 [R] B,H,W 00000000	Up/down counter ch.3
0000 01F4 _H	CCR3 [R,R/W] B,H 00000000 -0001000		—	CSR3 [R,R/W] B 00000000	
0000 01F8 _H	—				
0000 01FC _H	—				Reserved
0000 0200 _H	CPCLR0 [R/W] W 11111111 11111111 11111111 11111111				32-bit Free-run timer ch.0
0000 0204 _H	TCDT0 [R/W] W 00000000 00000000 00000000 00000000				
0000 0208 _H	TCCSH0 [R/W] B,H 0-----00	TCCSL0 [R/W] B,H -1-00000	—		
0000 020C _H	IPCP0 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				32-bit Input capture ch.0 to ch.3
0000 0210 _H	IPCP1 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0214 _H	IPCP2 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0218 _H	IPCP3 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 021C _H	—	ICS01 [R/W] B 00000000	—	ICS23 [R/W] B 00000000	

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MB91645A Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 0220 _H	IPCP4 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				32-bit Input capture ch.4 to ch.7
0000 0224 _H	IPCP5 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0228 _H	IPCP6 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 022C _H	IPCP7 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0230 _H	—	ICS45 [R/W] B 00000000	—	ICS67 [R/W] B 00000000	
0000 0234 _H	OCCP0 [R/W] W 00000000 00000000 00000000 00000000				32-bit Output compare ch.0 to ch.3
0000 0238 _H	OCCP1 [R/W] W 00000000 00000000 00000000 00000000				
0000 023C _H	OCCP2 [R/W] W 00000000 00000000 00000000 00000000				
0000 0240 _H	OCCP3 [R/W] W 00000000 00000000 00000000 00000000				
0000 0244 _H	OCSH1 [R/W] B,H,W ---0--00	OCSL0 [R/W] B,H,W 0000--00	OCSH3 [R/W] B,H,W ---0--00	OCSL2 [R/W] B,H,W 0000--00	
0000 0248 _H	OCCP4 [R/W] W 00000000 00000000 00000000 00000000				32-bit Output compare ch.4 to ch.7
0000 024C _H	OCCP5 [R/W] W 00000000 00000000 00000000 00000000				
0000 0250 _H	OCCP6 [R/W] W 00000000 00000000 00000000 00000000				
0000 0254 _H	OCCP7 [R/W] W 00000000 00000000 00000000 00000000				
0000 0258 _H	OCSH5 [R/W] B,H,W --0--00	OCSL4 [R/W] B,H,W 0000--00	OCSH7 [R/W] B,H,W ---0--00	OCSL6 [R/W] B,H,W 0000--00	
0000 025C _H	FRTSEL [R/W] B -----00	—			Free-run timer selector
0000 0260 _H	CPCLR1 [R/W] W 11111111 11111111 11111111 11111111				32-bit Free-run timer ch.1
0000 0264 _H	TCDT1 [R/W] W 00000000 00000000 00000000 00000000				
0000 0268 _H	TCCSH1 [R/W] B,H 0----00	TCCSL1 [R/W] B,H -1-0000	—		

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MB91645A Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 026C _H to 0000 031C _H	—				Reserved
0000 0320 _H	FCTLR[R/W] H -0--1011 -----		—	FSTR[R] B -----1	Flash memory control
0000 0324 _H to 0000 0334 _H	—				Reserved
0000 0338 _H	—		WREN[R/W] B,H 00000000 00000000		Wild register
0000 033C _H	—				
0000 0340 _H to 0000 037C _H	—				Reserved
0000 0380 _H	WRAR00[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				Wild register
0000 0384 _H	WRDR00[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0388 _H	WRAR01[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0000 038C _H	WRDR01[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0390 _H	WRAR02[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0000 0394 _H	WRDR02[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0398 _H	WRAR03[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0000 039C _H	WRDR03[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03A0 _H	WRAR04[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0000 03A4 _H	WRDR04[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03A8 _H	WRAR05[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0000 03AC _H	WRDR05[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03B0 _H	WRAR06[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				

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MB91645A Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 03B4 _H	WRDR06[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Wild register
0000 03B8 _H	WRAR07[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0000 03BC _H	WRDR07[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03C0 _H	WRAR08[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0000 03C4 _H	WRDR08[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03C8 _H	WRAR09[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0000 03CC _H	WRDR09[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03D0 _H	WRAR10[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0000 03D4 _H	WRDR10[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03D8 _H	WRAR11[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0000 03DC _H	WRDR11[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03E0 _H	WRAR12[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0000 03E4 _H	WRDR12[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03E8 _H	WRAR13[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0000 03EC _H	WRDR13[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03F0 _H	WRAR14[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0000 03F4 _H	WRDR14[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03F8 _H	WRAR15[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0000 03FC _H	WRDR15[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

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MB91645A Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 0400 _H	DDR0 [R/W] B,H 00000000	DDR1 [R/W] B,H 00000000	DDR2 [R/W] B,H 00000000	DDR3 [R/W] B,H 00000000	Data direction register
0000 0404 _H	DDR4 [R/W] B,H 00000000	DDR5 [R/W] B,H 00000000	DDR6 [R/W] B,H 00000000	DDR7[R/W] B,H 00000000	
0000 0408 _H	DDR8 [R/W] B,H 00000000	DDR9 [R/W] B,H ----000	DDRA [R/W] B,H 00000000	DDRB[R/W] B,H 00000000	
0000 040C _H	DDRC [R/W] B,H 00000000	DDRD [R/W] B,H 00000000	DDRE [R/W] B,H 00000000	DDRF [R/W] B,H -0000000	
0000 0410 _H	DDRG [R/W] B,H 00000000	DDRH [R/W] B,H 00000000	DDRI [R/W] B,H 00000000	DDRJ [R/W] B,H ----000	
0000 0414 _H	DDRK [R/W] B ----0000	—			
0000 0418 _H to 0000 041C _H	—				
0000 0420 _H	PCR0 [R/W] B,H 00000000	PCR1 [R/W] B,H 00000000	—		Pull-up control register
0000 0424 _H	—	PCR5 [R/W] B 00000000	PCR6 [R/W] B,H 00000000	PCR7[R/W] B,H 00000000	
0000 0428 _H	PCR8 [R/W] B,H 00000000	PCR9 [R/W] B,H ----000	PCRA [R/W] B,H 00000000	PCRB[R/W] B,H 00000000	
0000 042C _H	PCRC [R/W] B,H 00000000	PCRD [R/W] B,H 00000000	PCRE [R/W] B,H 00000000	PCRF [R/W] B,H -0000000	
0000 0430 _H	—			PCRJ [R/W] B ----000	
0000 0434 _H	PCRK [R/W] B ----00--	—			
0000 0438 _H to 0000 043C _H	—				

(Continued)

MB91645A Series

Address	Register				Block	
	+ 0	+ 1	+ 2	+ 3		
0000 0440 _H	ICR00 [R,R/W] B,H,W ---11111	ICR01 [R,R/W] B,H,W ---11111	ICR02 [R,R/W] B,H,W ---11111	ICR03 [R,R/W] B,H,W ---11111	Interrupt control	
0000 0444 _H	ICR04 [R,R/W] B,H,W ---11111	ICR05 [R,R/W] B,H,W ---11111	ICR06 [R,R/W] B,H,W ---11111	ICR07 [R,R/W] B,H,W ---11111		
0000 0448 _H	ICR08 [R,R/W] B,H,W ---11111	ICR09 [R,R/W] B,H,W ---11111	ICR10 [R,R/W] B,H,W ---11111	ICR11 [R,R/W] B,H,W ---11111		
0000 044C _H	ICR12 [R,R/W] B,H,W ---11111	ICR13 [R,R/W] B,H,W ---11111	ICR14 [R,R/W] B,H,W ---11111	ICR15 [R,R/W] B,H,W ---11111		
0000 0450 _H	ICR16 [R,R/W] B,H,W ---11111	ICR17 [R,R/W] B,H,W ---11111	ICR18 [R,R/W] B,H,W ---11111	ICR19 [R,R/W] B,H,W ---11111		
0000 0454 _H	ICR20 [R,R/W] B,H,W ---11111	ICR21 [R,R/W] B,H,W ---11111	ICR22 [R,R/W] B,H,W ---11111	ICR23 [R,R/W] B,H,W ---11111		
0000 0458 _H	ICR24 [R,R/W] B,H,W ---11111	ICR25 [R,R/W] B,H,W ---11111	ICR26 [R,R/W] B,H,W ---11111	ICR27 [R,R/W] B,H,W ---11111		
0000 045C _H	ICR28 [R,R/W] B,H,W ---11111	ICR29 [R,R/W] B,H,W ---11111	ICR30 [R,R/W] B,H,W ---11111	ICR31 [R,R/W] B,H,W ---11111		
0000 0460 _H	ICR32 [R,R/W] B,H,W ---11111	ICR33 [R,R/W] B,H,W ---11111	ICR34 [R,R/W] B,H,W ---11111	ICR35 [R,R/W] B,H,W ---11111		
0000 0464 _H	ICR36 [R,R/W] B,H,W ---11111	ICR37 [R,R/W] B,H,W ---11111	ICR38 [R,R/W] B,H,W ---11111	ICR39 [R,R/W] B,H,W ---11111		
0000 0468 _H	ICR40 [R,R/W] B,H,W ---11111	ICR41 [R,R/W] B,H,W ---11111	ICR42 [R,R/W] B,H,W ---11111	ICR43 [R,R/W] B,H,W ---11111		
0000 046C _H	ICR44 [R,R/W] B,H,W ---11111	ICR45 [R,R/W] B,H,W ---11111	ICR46 [R,R/W] B,H,W ---11111	ICR47 [R,R/W] B,H,W ---11111		
0000 0470 _H to 0000 047C _H	—					Reserved
0000 0480 _H	RSTRR [R] B,H,W 11-X---X*3	RSTCR [R/W] B,H,W 000----0	STBCR [R/W] B,H,W 0000--11	SLPRR [R/W] B,H,W 00000000		Reset control/ Power consumption control
0000 0484 _H	—					

(Continued)

MB91645A Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 0488 _H	DIVR0 [R/W] B,H 000-----	DIVR1 [R/W] B,H 0001----	DIVR2 [R/W] B 0011----	—	Clock division control
0000 048C _H	—				
0000 0490 _H	IORR0 [R/W] B,H,W -0000000	IORR1 [R/W] B,H,W -0000000	IORR2 [R/W] B,H,W -0000000	IORR3 [R/W] B,H,W -0000000	Peripheral DMA transmission request control
0000 0494 _H	IORR4 [R/W] B,H,W -0000000	IORR5 [R/W] B,H,W -0000000	IORR6 [R/W] B,H,W -0000000	IORR7 [R/W] B,H,W -0000000	
0000 0498 _H to 0000 049C _H	—				Reserved
0000 04A0 _H	PFR0 [R/W] B,H 00000000	PFR1 [R/W] B,H 00000000	PFR2 [R/W] B,H 00000000	PFR3 [R/W] B,H 00000000	Port function register
0000 04A4 _H	PFR4 [R/W] B,H 00000000	PFR5 [R/W] B,H 00000000	PFR6 [R/W] B,H 00-00-0-	PFR7[R/W] B,H 00000000	
0000 04A8 _H	PFR8 [R/W] B 00000000	—	PFRA [R/W] B 00-00000	—	
0000 04AC _H	PFRC [R/W] B,H 0000-0-0	PFRD [R/W] B,H -0-0-0-0	PFRE [R/W] B 0-0--0-0	—	
0000 04B0 _H	PFRG [R/W] B,H -000-000	PFRH [R/W] B,H 00-0-0-0	PFRI [R/W] B 0000-0-0	—	
0000 04B4 _H	—				
0000 04B8 _H	EPFR0 [R/W] B,H --000000	EPFR1 [R/W] B,H --000000	EPFR2 [R/W] B,H --000000	EPFR3 [R/W] B,H --000000	Extended port function register
0000 04BC _H	EPFR4 [R/W] B,H 00000000	EPFR5 [R/W] B,H 00000000	EPFR6 [R/W] B,H 00000000	EPFR7 [R/W] B,H ---00000	
0000 04C0 _H	EPFR8 [R/W] B,H ---00000	EPFR9 [R/W] B,H ---00000	EPFR10 [R/W] B,H ---00000	EPFR11 [R/W] B,H ---00000	
0000 04C4 _H	EPFR12 [R/W] B,H ---00000	EPFR13 [R/W] B,H ---00000	EPFR14 [R/W] B,H ---00000	EPFR15 [R/W] B,H ---00000	
0000 04C8 _H	EPFR16 [R/W] B,H ---00000	EPFR17 [R/W] B,H ---00000	EPFR18 [R/W] B,H 00000000	EPFR19 [R/W] B,H -0000001	
0000 04CC _H	EPFR20 [R/W] B,H --000000	EPFR21 [R/W] B,H --000000	EPFR22 [R/W] B,H --000000	EPFR23 [R/W] B,H --000000	
0000 04D0 _H	EPFR24 [R/W] B,H --000000	EPFR25 [R/W] B,H --000000	EPFR26 [R/W] B,H --000000	EPFR27 [R/W] B,H --000000	
0000 04D4 _H	EPFR28 [R/W] B,H 00000000	EPFR29 [R/W] B,H 00000000	EPFR30 [R/W] B,H ----0000	EPFR31 [R/W] B,H -0000000	
0000 04D8 _H	EPFR32 [R/W] B,H 00000000	EPFR33 [R/W] B,H --000000	EPFR34 [R/W] B -0000000	—	
0000 04DC _H	—				

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MB91645A Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 04E0 _H to 0000 04EC _H	—				Reserved
0000 04F0 _H	ICSEL0[R/W] B,H,W ----000	ICSEL1[R/W] B,H,W ----000	ICSEL2[R/W] B,H,W ----000	ICSEL3[R/W] B,H,W ----000	DMA start request clear select function
0000 04F4 _H	ICSEL4[R/W] B,H,W ----00	ICSEL5[R/W] B,H,W ----000	ICSEL6[R/W] B,H,W ----00	ICSEL7[R/W] B,H,W ----00	
0000 04F8 _H	ICSEL8[R/W] B,H,W ----00	ICSEL9[R/W] B,H,W ----000	ICSEL10[R/W] B,H,W ----0000	ICSEL11[R/W] B,H,W ----0000	
0000 04FC _H	ICSEL12[R/W] B,H ----0000	ICSEL13[R/W] B,H ----0-0	ICSEL14[R/W] B ----00	—	
0000 0500 _H to 0000 050C _H	—				Reserved
0000 0510 _H	CSELR [R/W] B,H,W 001---00	CMONR [R] B,H,W 001---00	MTMCR [R/W] B,H,W 00001111	STMCR [R/W] B,H,W 0000-111	Clock generation/ Main timer/ Sub timer
0000 0514 _H	PLLCR [R/W] B,H --000000 11110000		CSTBR [R/W] B -0000000	—	
0000 0518 _H	WCRD [R] B,H --000000	WCRL [R/W] B,H --000000	WCCR [R,R/W] B 00--0000	—	Clock counter
0000 051C _H to 0000 05FC _H	—				Reserved
0000 0600 _H	ASR0 [R/W] W 00000000 00000000 ----- 1111-001				External bus I/F
0000 0604 _H	ASR1 [R/W] W XXXXXXXX XXXXXXXX ----- XXXX-XX0				
0000 0608 _H	ASR2 [R/W] W XXXXXXXX XXXXXXXX ----- XXXX-XX0				
0000 060C _H	ASR3 [R/W] W XXXXXXXX XXXXXXXX ----- XXXX-XX0				
0000 0610 _H to 0000 063C _H	—				

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MB91645A Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 0640 _H	ACR0[R/W] W ----- 00--00-0				External bus I/F
0000 0644 _H	ACR1[R/W] W ----- XX--XX-X				
0000 0648 _H	ACR2[R/W] W ----- XX--XX-X				
0000 064C _H	ACR3[R/W] W ----- XX--XX-X				
0000 0650 _H to 0000 067C _H	—				
0000 0680 _H	AWR0 [R/W] W ----1111 00000000 11110000 00000-0-				
0000 0684 _H	AWR1 [R/W] W ---XXXX XXXXXXXX XXXXXXXX XXXXX-X-				
0000 0688 _H	AWR2 [R/W] W ---XXXX XXXXXXXX XXXXXXXX XXXXX-X-				
0000 068C _H	AWR3 [R/W] W ---XXXX XXXXXXXX XXXXXXXX XXXXX-X-				
0000 0690 _H to 0000 06BC _H	—				
0000 06C0 _H	DMAR0 [R/W] W -----0000				
0000 06C4 _H	DMAR1 [R/W] W -----0000				
0000 06C8 _H	DMAR2 [R/W] W -----0000				
0000 06CC _H	DMAR3 [R/W] W -----0000				
0000 06D0 _H to 0000 06FC _H	—				Reserved
0000 0700 _H to 0000 0BFC _H	—				Reserved

(Continued)

MB91645A Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 0C00 _H	DCCR0 [R/W] W 0----000 --00--00 00000000 0-000000				DMAC
0000 0C04 _H	DCSR0 [R, R/W] H 0-----000		DTCR0 [R/W] H 00000000 00000000		
0000 0C08 _H	DSAR0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C0C _H	DDAR0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C10 _H	DCCR1 [R/W] W 0----000 --00--00 00000000 0-000000				
0000 0C14 _H	DCSR1 [R, R/W] H 0-----000		DTCR1 [R/W] H 00000000 00000000		
0000 0C18 _H	DSAR1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C1C _H	DDAR1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C20 _H	DCCR2 [R/W] W 0----000 --00--00 00000000 0-000000				
0000 0C24 _H	DCSR2 [R, R/W] H 0-----000		DTCR2 [R/W] H 00000000 00000000		
0000 0C28 _H	DSAR2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C2C _H	DDAR2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C30 _H	DCCR3 [R/W] W 0----000 --00--00 00000000 0-000000				
0000 0C34 _H	DCSR3 [R, R/W] H 0-----000		DTCR3 [R/W] H 00000000 00000000		
0000 0C38 _H	DSAR3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C3C _H	DDAR3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C40 _H	DCCR4 [R/W] W 0----000 --00--00 00000000 0-000000				
0000 0C44 _H	DCSR4 [R, R/W] H 0-----000		DTCR4 [R/W] H 00000000 00000000		
0000 0C48 _H	DSAR4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C4C _H	DDAR4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

(Continued)

MB91645A Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 0C50 _H	DCCR5 [R/W] W 0----000 --00--00 00000000 0-000000				DMAC
0000 0C54 _H	DCSR5 [R, R/W] H 0-----000		DTCR5 [R/W] H 00000000 00000000		
0000 0C58 _H	DSAR5 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C5C _H	DDAR5 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C60 _H	DCCR6 [R/W] W 0----000 --00--00 00000000 0-000000				
0000 0C64 _H	DCSR6 [R, R/W] H 0-----000		DTCR6 [R/W] H 00000000 00000000		
0000 0C68 _H	DSAR6 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C6C _H	DDAR6 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C70 _H	DCCR7 [R/W] W 0----000 --00--00 00000000 0-000000				
0000 0C74 _H	DCSR7 [R, R/W] H 0-----000		DTCR7 [R/W] H 00000000 00000000		
0000 0C78 _H	DSAR7 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C7C _H	DDAR7 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C80 _H to 0000 0DF0 _H	—				
0000 0DF4 _H	—		DILVR [R,R/W] B ---11111		
0000 0DF8 _H	DMACR [R/W] W 0-----0000 0-----0000				
0000 0DFC _H to 0000 0F3C _H	—				

(Continued)

MB91645A Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 0F40 _H	BT4TMR[R]H 00000000 00000000		BT4TMCR[R/W] B,H -00000000 00000000		Base timer ch.4
0000 0F44 _H	—	BT4STC[R/W]B 0000-000	—		
0000 0F48 _H	BT4PCSR/BT4PRLL[R/W]H XXXXXXXX XXXXXXXXX		BT4PDUT/BT4PRLH/BT4DTBF[R/W]H XXXXXXXX XXXXXXXXX		
0000 0F4C _H	—				
0000 0F50 _H	BT5TMR[R]H 00000000 00000000		BT5TMCR[R/W] B,H -00000000 00000000		Base timer ch.5
0000 0F54 _H	—	BT5STC[R/W]B 0000-000	—		
0000 0F58 _H	BT5PCSR/BT5PRLL[R/W]H XXXXXXXX XXXXXXXXX		BT5PDUT/BT5PRLH/BT5DTBF[R/W]H XXXXXXXX XXXXXXXXX		
0000 0F5C _H	—				
0000 0F60 _H	BT6TMR[R]H 00000000 00000000		BT6TMCR[R/W] B,H -00000000 00000000		Base timer ch.6
0000 0F64 _H	—	BT6STC[R/W]B 0000-000	—		
0000 0F68 _H	BT6PCSR/BT6PRLL[R/W]H XXXXXXXX XXXXXXXXX		BT6PDUT/BT6PRLH/BT6DTBF[R/W]H XXXXXXXX XXXXXXXXX		
0000 0F6C _H	—				
0000 0F70 _H	BT7TMR[R]H 00000000 00000000		BT7TMCR[R/W] B,H -00000000 00000000		Base timer ch.7
0000 0F74 _H	—	BT7STC[R/W]B 0000-000	—		
0000 0F78 _H	BT7PCSR/BT7PRLL[R/W]H XXXXXXXX XXXXXXXXX		BT7PDUT/BT7PRLH/BT7DTBF[R/W]H XXXXXXXX XXXXXXXXX		
0000 0F7C _H	BTSEL4567 [R/W]B 00000000	—			
0000 0F80 _H	BT8TMR[R]H 00000000 00000000		BT8TMCR[R/W] B,H -00000000 00000000		Base timer ch.8
0000 0F84 _H	—	BT8STC[R/W]B 0000-000	—		
0000 0F88 _H	BT8PCSR/BT8PRLL[R/W]H XXXXXXXX XXXXXXXXX		BT8PDUT/BT8PRLH/BT8DTBF[R/W]H XXXXXXXX XXXXXXXXX		
0000 0F8C _H	—				

(Continued)

MB91645A Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 0F90 _H	BT9TMR[R]H 00000000 00000000		BT9TMCR[R/W] B,H -0000000 00000000		Base timer ch.9
0000 0F94 _H	—	BT9STC[R/W]B 0000-000	—		
0000 0F98 _H	BT9PCSR/BT9PRL[R/W]H XXXXXXXX XXXXXXXX		BT9PDUT/BT9PRLH/BT9DTBF[R/W]H XXXXXXXX XXXXXXXX		
0000 0F9C _H	—				
0000 0FA0 _H	BTATMR[R]H 00000000 00000000		BTATMCR[R/W] B,H -0000000 00000000		Base timer ch.10
0000 0FA4 _H	—	BTASTC[R/W]B 0000-000	—		
0000 0FA8 _H	BTAPCSR/BTAPRL[R/W]H XXXXXXXX XXXXXXXX		BTAPDUT/BTAPRLH/BTADTBF [R/W]H XXXXXXXX XXXXXXXX		
0000 0FAC _H	—				
0000 0FB0 _H	BTBTMR[R]H 00000000 00000000		BTBTMCR[R/W] B,H -0000000 00000000		Base timer ch.11
0000 0FB4 _H	—	BTBSTC[R/W]B 0000-000	—		
0000 0FB8 _H	BTBPCSR/BTBPRLL[R/W]H XXXXXXXX XXXXXXXX		BTBPDUT/BTBPRLLH/BTBDTBF [R/W]H XXXXXXXX XXXXXXXX		
0000 0FBC _H	BTSEL89AB[R/W]B 00000000	—			
0000 0FC0 _H	BTCTMR[R]H 00000000 00000000		BTCTMCR[R/W] B,H -0000000 00000000		Base timer ch.12
0000 0FC4 _H	—	BTCSTC[R/W]B 0000-000	—		
0000 0FC8 _H	BTCPCSR/BTCPRL[R/W]H XXXXXXXX XXXXXXXX		BTCPDUT/BTCPRLH/BTCDTBF [R/W]H XXXXXXXX XXXXXXXX		
0000 0FCC _H	—				
0000 0FD0 _H	BTD TMR[R]H 00000000 00000000		BTD TMCR[R/W] B,H -0000000 00000000		Base timer ch.13
0000 0FD4 _H	—	BTDSTC[R/W]B 0000-000	—		
0000 0FD8 _H	BTDPCSR/BTDPRLL[R/W]H XXXXXXXX XXXXXXXX		BTDPDUT/BTDPRLLH/BTD DDTBF [R/W]H XXXXXXXX XXXXXXXX		
0000 0FDC _H	—				

(Continued)

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 0FE0 _H	BTETMR[R]H 00000000 00000000		BTETMCR[R/W] B,H -00000000 00000000		Base timer ch.14
0000 0FE4 _H	—	BTESTC[R/W]B 0000-000	—		
0000 0FE8 _H	BTEPCSR/BTEPRLL[R/W]H XXXXXXXX XXXXXXXX		BTEPDUT/BTEPRLLH/BTEDTBF [R/W]H XXXXXXXX XXXXXXXX		
0000 0FEC _H	—				
0000 0FF0 _H	BTFTMR[R]H 00000000 00000000		BTFTMCR[R/W] B,H -00000000 00000000		Base timer ch.15
0000 0FF4 _H	—	BTFSTC[R/W]B 0000-000	—		
0000 0FF8 _H	BTFPCSR/BTFPRLL[R/W]H XXXXXXXX XXXXXXXX		BTFPDUT/BTFPRLLH/BTFDDBF [R/W]H XXXXXXXX XXXXXXXX		
0000 0FFC _H	BTSELCDEF [R/W] B 00000000	—	BTSSSR [W] H XXXXXXXX XXXXXXXX		
0000 1000 _H to 0000 FFFC _H	—				Reserved

*1 : Byte access is available only when accessing the lower 8 bits within 9 bits.

*2 : The register of I²C can not be read immediate after reset.

*3 : Value just after reset by $\overline{\text{INIT}}$ pin.

Do not access the reserved areas.

MB91645A Series

■ VECTOR TABLE

Interrupt source (Peripheral resource)	Interrupt number		Interrupt level setting register	Offset	Address of TBR default
	Decimal	Hexa-decimal			
Reset	0	00	—	3FC _H	000F FFFC _H
System reserved	1	01	—	3F8 _H	000F FFF8 _H
System reserved	2	02	—	3F4 _H	000F FFF4 _H
System reserved	3	03	—	3F0 _H	000F FFF0 _H
System reserved	4	04	—	3EC _H	000F FFEC _H
System reserved	5	05	—	3E8 _H	000F FFE8 _H
System reserved	6	06	—	3E4 _H	000F FFE4 _H
System reserved	7	07	—	3E0 _H	000F FFE0 _H
System reserved	8	08	—	3DC _H	000F FFDC _H
INTE instruction	9	09	—	3D8 _H	000F FFD8 _H
System reserved	10	0A	—	3D4 _H	000F FFD4 _H
System reserved	11	0B	—	3D0 _H	000F FFD0 _H
Step trace trap	12	0C	—	3CC _H	000F FFCC _H
System reserved	13	0D	—	3C8 _H	000F FFC8 _H
Undefined instruction exception	14	0E	—	3C4 _H	000F FFC4 _H
—	15	0F	15(F _H) fixed	3C0 _H	000F FFC0 _H
External interrupt request ch.0 to ch.7	16	10	ICR00	3BC _H	000F FFBC _H
External interrupt request ch.8 to ch.15	17	11	ICR01	3B8 _H	000F FFB8 _H
External interrupt request ch.16 to ch.23	18	12	ICR02	3B4 _H	000F FFB4 _H
External interrupt request ch.24 to ch.31	19	13	ICR03	3B0 _H	000F FFBO _H
16-bit reload timer ch.0 to ch.2	20	14	ICR04	3AC _H	000F FFAC _H
Reception interrupt request of UART/CSIO ch.0	21	15	ICR05	3A8 _H	000F FFA8 _H
Transmission interrupt request of UART/CSIO ch.0 Transmission bus idle interrupt request of UART/CSIO ch.0	22	16	ICR06	3A4 _H	000F FFA4 _H
Reception interrupt request of UART/CSIO/ I ² C ch.1	23	17	ICR07	3A0 _H	000F FFA0 _H
Transmission interrupt request of UART/CSIO/ I ² C ch.1 Transmission bus idle interrupt request of UART/CSIO ch.1	24	18	ICR08	39C _H	000F FF9C _H
Status interrupt request of I ² C ch.1	25	19	ICR09	398 _H	000F FF98 _H
Reception interrupt request of UART/CSIO/I ² C ch.2	26	1A	ICR10	394 _H	000F FF94 _H
Transmission interrupt request of UART/CSIO/I ² C ch.2 Transmission bus idle interrupt request of UART/CSIO ch.2	27	1B	ICR11	390 _H	000F FF90 _H

(Continued)

Interrupt source (Peripheral resource)	Interrupt number		Interrupt level setting register	Offset	Address of TBR default
	Decimal	Hexa-decimal			
Status interrupt request of I ² C ch.2	28	1C	ICR12	38C _H	000F FF8C _H
Reception interrupt request of UART/CSIO/I ² C ch.3	29	1D	ICR13	388 _H	000F FF88 _H
Transmission interrupt request of UART/CSIO/I ² C ch.3 Transmission bus idle interrupt request of UART/CSIO ch.3 Status interrupt request of I ² C ch.3	30	1E	ICR14	384 _H	000F FF84 _H
Reception interrupt request of UART/CSIO/I ² C ch.4	31	1F	ICR15	380 _H	000F FF80 _H
Transmission interrupt request of UART/CSIO/I ² C ch.4 Transmission bus idle interrupt request of UART/CSIO ch.4 Status interrupt request of I ² C ch.4	32	20	ICR16	37C _H	000F FF7C _H
Reception interrupt request of UART/CSIO/I ² C ch.5	33	21	ICR17	378 _H	000F FF78 _H
Transmission interrupt request of UART/CSIO/I ² C ch.5 Transmission bus idle interrupt request of UART/CSIO ch.5 Status interrupt request of I ² C ch.5	34	22	ICR18	374 _H	000F FF74 _H
Reception interrupt request of UART/CSIO/ I ² C ch.6	35	23	ICR19	370 _H	000F FF70 _H
Transmission interrupt request of UART/CSIO/I ² C ch.6 Transmission bus idle interrupt request of UART/CSIO ch.6 Status interrupt request of I ² C ch.6	36	24	ICR20	36C _H	000F FF6C _H
Reception interrupt request of UART/CSIO/I ² C ch.7 32-bit input capture ch.4 to ch.7	37	25	ICR21	368 _H	000F FF68 _H
Transmission interrupt request of UART/CSIO/I ² C ch.7 Transmission bus idle interrupt request of UART/CSIO ch.7 Status interrupt request of I ² C ch.7 32-bit output compare ch.4 to ch.7	38	26	ICR22	364 _H	000F FF64 _H
Reception interrupt request of UART/CSIO/I ² C ch.8 to ch.11 Transmission interrupt request of UART/CSIO/I ² C ch.8 to ch.11 Transmission bus idle interrupt request of UART/CSIO ch.8 to ch.11 Transmission FIFO interrupt request UART/CSIO/I ² C ch.8 to ch.11 Status interrupt request of I ² C ch.8 to ch.11	39	27	ICR23	360 _H	000F FF60 _H
16-bit up/down counter ch.0 to ch.3	40	28	ICR24	35C _H	000F FF5C _H
Main timer/Sub timer/Watch counter	41	29	ICR25	358 _H	000F FF58 _H
Unit 0 of 10-bit A/D converter <ul style="list-style-type: none"> • Scan conversion interrupt request • Priority conversion interrupt request • FIFO overrun interrupt request • Conversion result compare interrupt request 	42	2A	ICR26	354 _H	000F FF54 _H
32-bit free run timer ch.0, ch.1	43	2B	ICR27	350 _H	000F FF50 _H
32-bit input capture ch.0 to ch.3	44	2C	ICR28	34C _H	000F FF4C _H
32-bit output compare ch.0 to ch.3	45	2D	ICR29	348 _H	000F FF48 _H

(Continued)

MB91645A Series

(Continued)

Interrupt source (Peripheral resource)	Interrupt number		Interrupt level setting register	Offset	Address of TBR default
	Decimal	Hexa-decimal			
Base timer ch.0	46	2E	ICR30	344 _H	000F FF44 _H
Base timer ch.1	47	2F	ICR31	340 _H	000F FF40 _H
Base timer ch.2	48	30	ICR32	33C _H	000F FF3C _H
Base timer ch.3	49	31	ICR33	338 _H	000F FF38 _H
Base timer ch.4, ch.5	50	32	ICR34	334 _H	000F FF34 _H
Base timer ch.6, ch.7	51	33	ICR35	330 _H	000F FF30 _H
Base timer ch.8, ch.9	52	34	ICR36	32C _H	000F FF2C _H
Base timer ch.10, ch.11	53	35	ICR37	328 _H	000F FF28 _H
Base timer ch.12	54	36	ICR38	324 _H	000F FF24 _H
Base timer ch.13	55	37	ICR39	320 _H	000F FF20 _H
Base timer ch.14, ch.15	56	38	ICR40	31C _H	000F FF1C _H
DMA controller (DMAC) ch.0	57	39	ICR41	318 _H	000F FF18 _H
DMA controller (DMAC) ch.1	58	3A	ICR42	314 _H	000F FF14 _H
DMA controller (DMAC) ch.2	59	3B	ICR43	310 _H	000F FF10 _H
DMA controller (DMAC) ch.3	60	3C	ICR44	30C _H	000F FF0C _H
DMA controller (DMAC) ch.4 to ch.7	61	3D	ICR45	308 _H	000F FF08 _H
Unit 1 of 10-bit A/D converter <ul style="list-style-type: none"> • Scan conversion interrupt request • Priority conversion interrupt request • FIFO overrun interrupt request • Conversion result compare interrupt request 	62	3E	ICR46	304 _H	000F FF04 _H
Delay interrupt	63	3F	ICR47	300 _H	000F FF00 _H
System reserved (Used by REALOS)	64	40	—	2FC _H	000F FEF8 _H
System reserved (Used by REALOS)	65	41	—	2F8 _H	000F FEF4 _H
Used by INT instruction	66 to 255	42 to FF	—	2F4 _H to 000 _H	000F FEF4 _H to 000F FC00 _H

■ PIN STATUS IN EACH CPU STATE

The terms used for pin status have the following meanings.

- When $\overline{\text{INIT}} = \text{"L"}$

This is the period when the $\overline{\text{INIT}}$ pin is the "L" level.

- When $\overline{\text{INIT}} = \text{"H"}$

The status immediately after the $\overline{\text{INIT}}$ pin changes from the "L" level to the "H" level.

- SLVL1

This bit is a standby level setting bit in the standby mode control register (STBCR).

- Input enabled

Indicates that the input function can be used.

- Input disabled

Indicates that the input function cannot be used.

- Output Hi-Z

Indicates that the output drive transistor is disabled and the pin is put in the Hi-Z state.

- Maintain previous state

Maintains the state that was being output immediately prior to entering the current mode.

If a built-in peripheral function is operating, the output follows the peripheral function.

If the pin is being used as a port, that output is maintained.

- Internal input fixed at "0"

The input gate connected to the pin is disconnected from the external input and internally connected to "0".

- Input enabled when interrupt function selected and enabled

Inputs are allowed only when the pin is configured as an external interrupt request input pin and the external interrupt request is enabled.

MB91645A Series

• List of pin status

Pin name	Function	During initialization		Sleep Mode	Standby Mode	
		$\overline{\text{INIT}} = \text{“L”}$	$\overline{\text{INIT}} = \text{“H”}$		SLVL1 = 0	SLVL1 = 1
$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	—	—	Input enabled	Input enabled	Input enabled
X0	X0	Input enabled	Input enabled		Hi-Z or Input enabled	Hi-Z or Input enabled
X1	X1	Input enabled	Input enabled		“H” output or Input enabled	“H” output or Input enabled
X0A	X0A (When $\overline{\text{INIT}}$ input, see PK1. When port selected, input disabled)	Input disabled	Input disabled		Hi-Z or Input enabled	Hi-Z or Input enabled
X1A	X1A (When $\overline{\text{INIT}}$ input, see PK0. When port selected, input disabled)	Input disabled	Input disabled		“H” output or Input enabled	“H” output or Input enabled
MD0	MD0	Input enabled	Input enabled		Input enabled	Input enabled
MD1	MD1	Input enabled	Input enabled			
P00	P00/D00/TIOA0/SOUT0_1/IN0	Output Hi-Z	Output Hi-Z/ Input enabled		Maintain previous state	Maintain previous state
P01	P01/D01/TIOB0/SIN0_1/IN1					
P02	P02/D02/TIOA1/SCK0_1/IN2					
P03	P03/D03/TIOB1/IN3					
P04	P04/D04/TIOA2/SOUT1/IN4					
P05	P05/D05/TIOB2/SIN1/IN5					
P06	P06/D06/TIOA3/SCK1/IN6					
P07	P07/D07/TIOB3/IN7					

(Continued)

MB91645A Series

Pin name	Function	During initialization		Sleep Mode	Standby Mode	
		$\overline{\text{INIT}} = \text{"L"}$	$\overline{\text{INIT}} = \text{"H"}$		SLVL1 = 0	SLVL1 = 1
P10	P10/D08/TIOA4/SOUT2/AIN0/INT0	Output Hi-Z	Output Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0" Input enabled when interrupt function selected and enabled
P11	P11/D09/TIOB4/SIN2/BIN0/INT1					
P12	P12/D10/TIOA5/SCK2/ZIN0/INT2					
P13	P13/D11/TIOB5/INT3					
P14	P14/D12/TIOA6/SOUT3/AIN1/INT4					
P15	P15/D13/TIOB6/SIN3/BIN1/INT5					
P16	P16/D14/TIOA7/SCK3/ZIN1/INT6					
P17	P17/D15/TIOB7/INT7					
P20	P20/A00/TIOA8/SOUT4/AIN2	Output Hi-Z	Output Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0"
P21	P21/A01/TIOB8/SIN4/BIN2					
P22	P22/A02/TIOA9/SCK4/ZIN2					
P23	P23/A03/TIOB9					
P24	P24/A04/TIOA10/SOUT5/AIN3/ OUT0					
P25	P25/A05/TIOB10/SIN5/BIN3/OUT1					
P26	P26/A06/TIOA11/SCK5/ZIN3/ OUT2					
P27	P27/A07/TIOB11/OUT3					
P30	P30/A08/TIOA12/SOUT6/INT8	Output Hi-Z	Output Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0" Input enabled when interrupt function selected and enabled
P31	P31/A09/TIOB12/SIN6/INT9					
P32	P32/A10/TIOA13/SCK6/INT10					
P33	P33/A11/TIOB13/INT11					
P34	P34/A12/TIOA14/SOUT7/OUT4/ INT12					
P35	P35/A13/TIOB14/SIN7/OUT5/ INT13					
P36	P36/A14/TIOA15/SCK7/OUT6/ INT14					
P37	P37/A15/TIOB15/OUT7/INT15					

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MB91645A Series

Pin name	Function	During initialization		Sleep Mode	Standby Mode	
		$\overline{\text{INIT}} = \text{"L"}$	$\overline{\text{INIT}} = \text{"H"}$		SLVL1 = 0	SLVL1 = 1
P40	P40/A16/SOUT8	Output Hi-Z	Output Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0"
P41	P41/A17/SIN8					
P42	P42/A18/SCK8					
P43	P43/A19					
P44	P44/A20/SOUT9					
P45	P45/A21/SIN9					
P46	P46/A22/SCK9					
P47	P47/A23					
P50	P50/ $\overline{\text{CS0}}$ /SOUT10/AIN0_1	Output Hi-Z	Output Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0"
P51	P51/ $\overline{\text{CS1}}$ /SIN10/BIN0_1					
P52	P52/ $\overline{\text{CS2}}$ /SCK10/ZIN0_1					
P53	P53/ $\overline{\text{CS3}}$ /FRCK1/INT21_2					Input enabled when interrupt function selected and enabled
P54	P54/ $\overline{\text{AS}}$ /SOUT11/AIN1_1					
P55	P55/ $\overline{\text{RD}}$ /SIN11/BIN1_1/ADTRG0					Output Hi-Z/ Internal input fixed at "0"
P56	P56/ $\overline{\text{WR0}}$ /SCK11/ZIN1_1/FRCK0					
P57	P57/ $\overline{\text{WR1}}$					

(Continued)

MB91645A Series

Pin name	Function	During initialization		Sleep Mode	Standby Mode	
		$\overline{\text{INIT}} = \text{"L"}$	$\overline{\text{INIT}} = \text{"H"}$		SLVL1 = 0	SLVL1 = 1
P60	P60/RDY/AIN2_1	Output Hi-Z	Output Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0"
P61	P61/SYSCLK/BIN2_1					
P62	P62/DREQ0/ZIN2_1					
P63	P63/DACK0/FRCK1_1/INT22_2					Input enabled when interrupt function selected and enabled
P64	P64/DEOP0/AIN3_1					
P65	P65/DREQ1/BIN3_1/ADTRG0_1					Output Hi-Z/ Internal input fixed at "0"
P66	P66/DACK1/ZIN3_1/FRCK0_1					
P67	P67/DEOP1/INT23_2	Output Hi-Z/ Internal input fixed at "0"	Input enabled when interrupt function selected and enabled			

(Continued)

MB91645A Series

Pin name	Function	During initialization		Sleep Mode	Standby Mode	
		$\overline{\text{INIT}} = \text{“L”}$	$\overline{\text{INIT}} = \text{“H”}$		SLVL1 = 0	SLVL1 = 1
P70	P70/AN0/OUT0_1/INT16	Output Hi-Z	Output Hi-Z/ Input disabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at “0” Input enabled when interrupt function selected and enabled
P71	P71/AN1/OUT1_1/INT17					
P72	P72/AN2/TMO0/OUT2_1/INT18					
P73	P73/AN3/TMO1/OUT3_1/INT19					
P74	P74/AN4/TMO2/OUT4_1/INT20					
P75	P75/AN5/SOUT0/TMI0/ OUT5_1/INT21					
P76	P76/AN6/SIN0/TMI1/OUT6_1/ INT22					
P77	P77/AN7/SCK0/TMI2/OUT7_1/ INT23					
P80	P80/AN8/IN0_1/INT24	Output Hi-Z	Output Hi-Z/ Input disabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at “0” Input enabled when interrupt function selected and enabled
P81	P81/AN9/IN1_1/INT25					
P82	P82/AN10/IN2_1/INT26					
P83	P83/AN11/IN3_1/INT27					
P84	P84/AN12/IN4_1/INT28					
P85	P85/AN13/IN5_1/INT29					
P86	P86/AN14/IN6_1/INT30					
P87	P87/AN15/IN7_1/INT31					
P90	P90/DA0	Output Hi-Z	Output Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at “0”
P91	P91/DA1					
P92	P92/DA2					
PA0	PA0/AN16/INT16_1	Output Hi-Z	Output Hi-Z/ Input disabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at “0” Input enabled when interrupt function selected and enabled
PA1	PA1/AN17/INT17_1					
PA2	PA2/AN18/TMO0_1/INT18_1					
PA3	PA3/AN19/TMO1_1/INT19_1					
PA4	PA4/AN20/TMO2_1/INT20_1					
PA5	PA5/AN21/TMI0_1/INT21_1					
PA6	PA6/AN22/TMI1_1/INT22_1					
PA7	PA7/AN23/TMI2_1/INT23_1					

(Continued)

MB91645A Series

Pin name	Function	During initialization		Sleep Mode	Standby Mode	
		INIT = "L"	INIT = "H"		SLVL1 = 0	SLVL1 = 1
PB0	PB0/AN24/INT24_1	Output Hi-Z	Output Hi-Z/ Input disabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0" Input enabled when interrupt function selected and enabled
PB1	PB1/AN25/INT25_1					
PB2	PB2/AN26/INT26_1					
PB3	PB3/AN27/INT27_1					
PB4	PB4/AN28/INT28_1					
PB5	PB5/AN29/INT29_1					
PB6	PB6/AN30/INT30_1					
PB7	PB7/AN31/INT31_1					
PC0	PC0/TIOA12_1/SOUT6_1/INT8_1	Output Hi-Z	Output Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0" Input enabled when interrupt function selected and enabled
PC1	PC1/TIOB12_1/SIN6_1/INT9_1					
PC2	PC2/TIOA13_1/SCK6_1/INT10_1					
PC3	PC3/TIOB13_1/INT11_1					
PC4	PC4/TIOA14_1/SOUT7_1/ OUT4_2/INT12_1					
PC5	PC5/TIOB14_1/SIN7_1/OUT5_2/ INT13_1					
PC6	PC6/TIOA15_1/SCK7_1/OUT6_2/ INT14_1					
PC7	PC7/TIOB15_1/OUT7_2/INT15_1					
PD0	PD0/SOUT8_1	Output Hi-Z	Output Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0"
PD1	PD1/SIN8_1					
PD2	PD2/SCK8_1					
PD3	PD3					
PD4	PD4/SOUT9_1					
PD5	PD5/SIN9_1					
PD6	PD6/SCK9_1					
PD7	PD7					

(Continued)

MB91645A Series

Pin name	Function	During initialization		Sleep Mode	Standby Mode	
		INIT = "L"	INIT = "H"		SLVL1 = 0	SLVL1 = 1
PE0	PE0/SOUT10_1/AIN0_3	Output Hi-Z	Output Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0"
PE1	PE1/SIN10_1/BIN0_3					
PE2	PE2/SCK10_1/ZIN0_3					
PE3	PE3/FRCK1_2					
PE4	PE4/AIN1_3					
PE5	PE5/SOUT11_1/BIN1_3/ ADTRG0_4					
PE6	PE6/SIN11_1/ZIN1_3/FRCK0_2					
PE7	PE7/SCK11_1					
PF0	PF0/AIN2_3	Output Hi-Z	Output Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0"
PF1	PF1/BIN2_3					
PF2	PF2/ZIN2_3					
PF3	PF3/FRCK1_3					
PF4	PF4/AIN3_3					
PF5	PF5/BIN3_3/ADTRG0_5					
PF6	PF6/ZIN3_3/FRCK0_3					
PG0	PG0/DREQ2/TIOA0_1/SOUT0_2/ IN0_2	Output Hi-Z	Output Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0"
PG1	PG1/DACK2/TIOB0_1/SIN0_2/ IN1_2					
PG2	PG2/DEOP2/TIOA1_1/SCK0_2/ IN2_2					
PG3	PG3/DREQ3/TIOB1_1/IN3_2					
PG4	PG4/DACK3/TIOA2_1/SOUT1_1/ IN4_2					
PG5	PG5/DEOP3/TIOB2_1/SIN1_1/ IN5_2					
PG6	PG6/TIOA3_1/SCK1_1/IN6_2					
PG7	PG7/TIOB3_1/IN7_2					

(Continued)

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Pin name	Function	During initialization		Sleep Mode	Standby Mode	
		$\overline{\text{INIT}} = \text{“L”}$	$\overline{\text{INIT}} = \text{“H”}$		SLVL1 = 0	SLVL1 = 1
PH0	PH0/TIOA4_1/SOUT2_1/AIN0_2/ INT0_1	Output Hi-Z	Output Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at “0” Input enabled when interrupt function selected and enabled
PH1	PH1/TIOB4_1/SIN2_1/BIN0_2/ INT1_1					
PH2	PH2/TIOA5_1/SCK2_1/ZIN0_2/ INT2_1					
PH3	PH3/TIOB5_1/INT3_1					
PH4	PH4/TIOA6_1/SOUT3_1/AIN1_2/ INT4_1					
PH5	PH5/TIOB6_1/SIN3_1/BIN1_2/ INT5_1					
PH6	PH6/TIOA7_1/SCK3_1/ZIN1_2/ INT6_1					
PH7	PH7/TIOB7_1/INT7_1					
PI0	PI0/TIOA8_1/SOUT4_1/AIN2_2	Output Hi-Z	Output Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at “0”
PI1	PI1/TIOB8_1/SIN4_1/BIN2_2					
PI2	PI2/TIOA9_1/SCK4_1/ZIN2_2					
PI3	PI3/TIOB9_1					
PI4	PI4/TIOA10_1/SOUT5_1/AIN3_2/ OUT0_2					
PI5	PI5/TIOB10_1/SIN5_1/BIN3_2/ OUT1_2					
PI6	PI6/TIOA11_1/SCK5_1/ZIN3_2/ OUT2_2					
PI7	PI7/TIOB11_1/OUT3_2					
PJ0	PJ0	Output Hi-Z	Output Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at “0”
PJ1	PJ1					
PJ2	PJ2					
PK0	PK0	Output Hi-Z	Output Hi-Z/ Internal input fixed at “0”	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at “0”
PK1	PK1		Output Hi-Z/ Input enabled			
PK2	PK2/ADTRG0_2					
PK3	PK3/ADTRG0_3					

MB91645A Series

- List of pin status (serial write mode)

Pin name	Function	During initialization	During asynchronous write operation	During synchronous write operation
		$\overline{\text{INIT}} = \text{“L”}$	$\overline{\text{INIT}} = \text{“H”}$	
$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	—	—	—
X0	X0	Input enabled	Input enabled	Input enabled
X1	X1	Input enabled	Input enabled	Input enabled
X0A	X0A (When $\overline{\text{INIT}}$ input, see PK1. When port selected, input disabled)	Input disabled	Input disabled	Input disabled
X1A	X1A (When $\overline{\text{INIT}}$ input, see PK0. When port selected, input disabled)	Input disabled	Input disabled	Input disabled
MD0	MD0	Input enabled	Input enabled	Input enabled
MD1	MD1	Input enabled	Input enabled	Input enabled
P00	P00/D00/TIOA0/SOUT0_1/IN0	Output Hi-Z	Output Hi-Z/ Input enabled	Output Hi-Z/ Input enabled
P01	P01/D01/TIOB0/SIN0_1/IN1			
P02	P02/D02/TIOA1/SCK0_1/IN2			
P03	P03/D03/TIOB1/IN3			
P04	P04/D04/TIOA2/SOUT1/IN4			
P05	P05/D05/TIOB2/SIN1/IN5			
P06	P06/D06/TIOA3/SCK1/IN6			
P07	P07/D07/TIOB3/IN7			
P10	P10/D08/TIOA4/SOUT2/AIN0/ INT0	Output Hi-Z	Output Hi-Z/ Input enabled	Output Hi-Z/ Input enabled
P11	P11/D09/TIOB4/SIN2/BIN0/ INT1			
P12	P12/D10/TIOA5/SCK2/ZIN0/ INT2			
P13	P13/D11/TIOB5/INT3			
P14	P14/D12/TIOA6/SOUT3/AIN1/ INT4			
P15	P15/D13/TIOB6/SIN3/BIN1/ INT5			
P16	P16/D14/TIOA7/SCK3/ZIN1/ INT6			
P17	P17/D15/TIOB7/INT7			

(Continued)

MB91645A Series

Pin name	Function	During initialization	During asynchronous write operation	During synchronous write operation
		$\overline{\text{INIT}} = \text{“L”}$	$\overline{\text{INIT}} = \text{“H”}$	
P20	P20/A00/TIOA8/SOUT4/AIN2	Output Hi-Z	Output Hi-Z/ Input enabled	Output Hi-Z/ Input enabled
P21	P21/A01/TIOB8/SIN4/BIN2			
P22	P22/A02/TIOA9/SCK4/ZIN2			
P23	P23/A03/TIOB9			
P24	P24/A04/TIOA10/SOUT5/AIN3/ OUT0			
P25	P25/A05/TIOB10/SIN5/BIN3/ OUT1			
P26	P26/A06/TIOA11/SCK5/ZIN3/ OUT2			
P27	P27/A07/TIOB11/OUT3	Output Hi-Z	Output Hi-Z/ Input enabled	Output Hi-Z/ Input enabled
P30	P30/A08/TIOA12/SOUT6/INT8			
P31	P31/A09/TIOB12/SIN6/INT9			
P32	P32/A10/TIOA13/SCK6/INT10			
P33	P33/A11/TIOB13/INT11			
P34	P34/A12/TIOA14/SOUT7/OUT4/ INT12			
P35	P35/A13/TIOB14/SIN7/OUT5/ INT13			
P36	P36/A14/TIOA15/SCK7/OUT6/ INT14	Output Hi-Z	Output Hi-Z/ Input enabled	Output Hi-Z/ Input enabled
P37	P37/A15/TIOB15/OUT7/INT15			
P40	P40/A16/SOUT8			
P41	P41/A17/SIN8			
P42	P42/A18/SCK8			
P43	P43/A19			
P44	P44/A20/SOUT9			
P45	P45/A21/SIN9	Output Hi-Z	Output Hi-Z/ Input enabled	Output Hi-Z/ Input enabled
P46	P46/A22/SCK9			
P47	P47/A23			

(Continued)

MB91645A Series

Pin name	Function	During initialization	During asynchronous write operation	During synchronous write operation
		$\overline{\text{INIT}} = \text{“L”}$	$\overline{\text{INIT}} = \text{“H”}$	
P50	P50/ $\overline{\text{CS0}}$ /SOUT10/AIN0_1	Output Hi-Z	Output Hi-Z/ Input enabled	Output Hi-Z/ Input enabled
P51	P51/ $\overline{\text{CS1}}$ /SIN10/BIN0_1			
P52	P52/ $\overline{\text{CS2}}$ /SCK10/ZIN0_1			
P53	P53/ $\overline{\text{CS3}}$ /FRCK1/INT21_2			
P54	P54/ $\overline{\text{AS}}$ /SOUT11/AIN1_1			
P55	P55/ $\overline{\text{RD}}$ /SIN11/BIN1_1/ ADTRG0			
P56	P56/ $\overline{\text{WR0}}$ /SCK11/ZIN1_1/ FRCK0			
P57	P57/ $\overline{\text{WR1}}$	Output Hi-Z	Output Hi-Z/ Input enabled	Output Hi-Z/ Input enabled
P60	P60/RDY/AIN2_1			
P61	P61/SYSCLK/BIN2_1			
P62	P62/DREQ0/ZIN2_1			
P63	P63/DACK0/FRCK1_1/INT22_2			
P64	P64/DEOP0/AIN3_1			
P65	P65/DREQ1/BIN3_1/ ADTRG0_1			
P66	P66/DACK1/ZIN3_1/FRCK0_1	Output Hi-Z	Output Hi-Z/ Input disabled	Output Hi-Z/ Input disabled
P67	P67/DEOP1/INT23_2			
P70	P70/AN0/OUT0_1/INT16			
P71	P71/AN1/OUT1_1/INT17			
P72	P72/AN2/TMO0/OUT2_1/INT18			
P73	P73/AN3/TMO1/OUT3_1/INT19	Output Hi-Z/ Input enabled	Output	Output
P74	P74/AN4/TMO2/OUT4_1/INT20			
P75	P75/AN5/SOUT0/TMI0/ OUT5_1/INT21	Output Hi-Z	Output Hi-Z/ Input enabled	Output Hi-Z/ Input enabled
P76	P76/AN6/SIN0/TMI1/OUT6_1/ INT22		Output Hi-Z/ Input disabled	Output Hi-Z/ Input enabled
P77	P77/AN7/SCK0/TMI2/OUT7_1/ INT23			

(Continued)

MB91645A Series

Pin name	Function	During initialization	During asynchronous write operation	During synchronous write operation
		$\overline{\text{INIT}} = \text{“L”}$	$\overline{\text{INIT}} = \text{“H”}$	
P80	P80/AN8/IN0_1/INT24	Output Hi-Z	Output Hi-Z/ Input disabled	Output Hi-Z/ Input disabled
P81	P81/AN9/IN1_1/INT25			
P82	P82/AN10/IN2_1/INT26			
P83	P83/AN11/IN3_1/INT27			
P84	P84/AN12/IN4_1/INT28			
P85	P85/AN13/IN5_1/INT29			
P86	P86/AN14/IN6_1/INT30			
P87	P87/AN15/IN7_1/INT31			
P90	P90/DA0	Output Hi-Z	Output Hi-Z/ Input enabled	Output Hi-Z/ Input enabled
P91	P91/DA1			
P92	P92/DA2			
PA0	PA0/AN16/INT16_1	Output Hi-Z	Output Hi-Z/ Input disabled	Output Hi-Z/ Input disabled
PA1	PA1/AN17/INT17_1			
PA2	PA2/AN18/TMO0_1/INT18_1			
PA3	PA3/AN19/TMO1_1/INT19_1			
PA4	PA4/AN20/TMO2_1/INT20_1			
PA5	PA5/AN21/TMI0_1/INT21_1			
PA6	PA6/AN22/TMI1_1/INT22_1			
PA7	PA7/AN23/TMI2_1/INT23_1			
PB0	PB0/AN24/INT24_1	Output Hi-Z	Output Hi-Z/ Input disabled	Output Hi-Z/ Input disabled
PB1	PB1/AN25/INT25_1			
PB2	PB2/AN26/INT26_1			
PB3	PB3/AN27/INT27_1			
PB4	PB4/AN28/INT28_1			
PB5	PB5/AN29/INT29_1			
PB6	PB6/AN30/INT30_1			
PB7	PB7/AN31/INT31_1			

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MB91645A Series

Pin name	Function	During initialization	During asynchronous write operation	During synchronous write operation
		$\overline{\text{INIT}} = \text{“L”}$	$\overline{\text{INIT}} = \text{“H”}$	
PC0	PC0/TIOA12_1/SOUT6_1/ INT8_1	Output Hi-Z	Output Hi-Z/ Input enabled	Output Hi-Z/ Input enabled
PC1	PC1/TIOB12_1/SIN6_1/INT9_1			
PC2	PC2/TIOA13_1/SCK6_1/ INT10_1			
PC3	PC3/TIOB13_1/INT11_1			
PC4	PC4/TIOA14_1/SOUT7_1/ OUT4_2/INT12_1			
PC5	PC5/TIOB14_1/SIN7_1/ OUT5_2/INT13_1			
PC6	PC6/TIOA15_1/SCK7_1/ OUT6_2/INT14_1			
PC7	PC7/TIOB15_1/OUT7_2/ INT15_1			
PD0	PD0/SOUT8_1	Output Hi-Z	Output Hi-Z/ Input enabled	Output Hi-Z/ Input enabled
PD1	PD1/SIN8_1			
PD2	PD2/SCK8_1			
PD3	PD3			
PD4	PD4/SOUT9_1			
PD5	PD5/SIN9_1			
PD6	PD6/SCK9_1			
PD7	PD7			
PE0	PE0/SOUT10_1/AIN0_3	Output Hi-Z	Output Hi-Z/ Input enabled	Output Hi-Z/ Input enabled
PE1	PE1/SIN10_1/BIN0_3			
PE2	PE2/SCK10_1/ZIN0_3			
PE3	PE3/FRCK1_2			
PE4	PE4/AIN1_3			
PE5	PE5/SOUT11_1/BIN1_3/ ADTRG0_4			
PE6	PE6/SIN11_1/ZIN1_3/FRCK0_2			
PE7	PE7/SCK11_1			

(Continued)

MB91645A Series

Pin name	Function	During initialization	During asynchronous write operation	During synchronous write operation
		$\overline{\text{INIT}} = \text{“L”}$	$\overline{\text{INIT}} = \text{“H”}$	
PF0	PF0/AIN2_3	Output Hi-Z	Output Hi-Z/ Input enabled	Output Hi-Z/ Input enabled
PF1	PF1/BIN2_3			
PF2	PF2/ZIN2_3			
PF3	PF3/FRCK1_3			
PF4	PF4/AIN3_3			
PF5	PF5/BIN3_3/ADTRG0_5			
PF6	PF6/ZIN3_3/FRCK0_3			
PG0	PG0/DREQ2/TIOA0_1/ SOUT0_2/IN0_2	Output Hi-Z	Output Hi-Z/ Input enabled	Output Hi-Z/ Input enabled
PG1	PG1/DACK2/TIOB0_1/SIN0_2/ IN1_2			
PG2	PG2/DEOP2/TIOA1_1/SCK0_2/ IN2_2			
PG3	PG3/DREQ3/TIOB1_1/IN3_2			
PG4	PG4/DACK3/TIOA2_1/ SOUT1_1/IN4_2			
PG5	PG5/DEOP3/TIOB2_1/SIN1_1/ IN5_2			
PG6	PG6/TIOA3_1/SCK1_1/IN6_2			
PG7	PG7/TIOB3_1/IN7_2			
PH0	PH0/TIOA4_1/SOUT2_1/ AIN0_2/INT0_1	Output Hi-Z	Output Hi-Z/ Input enabled	Output Hi-Z/ Input enabled
PH1	PH1/TIOB4_1/SIN2_1/BIN0_2/ INT1_1			
PH2	PH2/TIOA5_1/SCK2_1/ZIN0_2/ INT2_1			
PH3	PH3/TIOB5_1/INT3_1			
PH4	PH4/TIOA6_1/SOUT3_1/ AIN1_2/INT4_1			
PH5	PH5/TIOB6_1/SIN3_1/BIN1_2/ INT5_1			
PH6	PH6/TIOA7_1/SCK3_1/ZIN1_2/ INT6_1			
PH7	PH7/TIOB7_1/INT7_1			

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MB91645A Series

(Continued)

Pin name	Function	During initialization	During asynchronous write operation	During synchronous write operation
		$\overline{\text{INIT}} = \text{“L”}$	$\overline{\text{INIT}} = \text{“H”}$	
PI0	PI0/TIOA8_1/SOUT4_1/AIN2_2	Output Hi-Z	Output Hi-Z/ Input enabled	Output Hi-Z/ Input enabled
PI1	PI1/TIOB8_1/SIN4_1/BIN2_2			
PI2	PI2/TIOA9_1/SCK4_1/ZIN2_2			
PI3	PI3/TIOB9_1			
PI4	PI4/TIOA10_1/SOUT5_1/ AIN3_2/OUT0_2			
PI5	PI5/TIOB10_1/SIN5_1/BIN3_2/ OUT1_2			
PI6	PI6/TIOA11_1/SCK5_1/ZIN3_2/ OUT2_2			
PI7	PI7/TIOB11_1/OUT3_2			
PJ0	PJ0	Output Hi-Z	Output Hi-Z/ Input enabled	Output Hi-Z/ Input enabled
PJ1	PJ1			
PJ2	PJ2			
PK0	PK0	Output Hi-Z	Output Hi-Z/ Input enabled	Output Hi-Z/ Input enabled
PK1	PK1			
PK2	PK2/ADTRG0_2			
PK3	PK3/ADTRG0_3			

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1, *2	V _{CC}	V _{SS} – 0.3	V _{SS} + 4.0	V	
	V _{DDI}	V _{SS} – 0.3	V _{SS} + 2.5	V	
Analog power supply voltage*1, *3	AV _{CC}	V _{SS} – 0.3	V _{SS} + 4.0	V	
Analog reference voltage*1, *3	AVRH	V _{SS} – 0.3	V _{SS} + 4.0	V	
Input voltage*1	V _I	V _{SS} – 0.3	V _{CC} + 0.3 (≤ 4.0)	V	*7
		V _{SS} – 0.3	V _{SS} + 6.0	V	5 V tolerant
Analog pin input voltage*1	V _{IA}	V _{SS} – 0.3	V _{SS} + 4.0	V	
Output voltage*1	V _O	V _{SS} – 0.3	V _{CC} + 0.3	V	
Maximum clamp current	I _{CLAMP}	– 4	+ 4	mA	*8
Total maximum clamp current	Σ I _{CLAMP}	—	40	mA	*8
“L” level maximum output current*4	I _{OL}	—	10	mA	
“L” level average output current*5	I _{OLAV}	—	4	mA	
“L” level total maximum output current	ΣI _{OL}	—	100	mA	
“L” level total average output current*6	ΣI _{OLAV}	—	50	mA	
“H” level maximum output current*4	I _{OH}	—	– 10	mA	
“H” level average output current*5	I _{OHAV}	—	– 4	mA	
“H” level total maximum output current	ΣI _{OH}	—	– 100	mA	
“H” level total average output current*6	ΣI _{OHAV}	—	– 50	mA	
Power consumption	P _D	—	500	mW	
Operating temperature	T _a	– 40	+ 85	°C	
Storage temperature	T _{STG}	– 55	+ 125	°C	

*1 : The parameter is based on V_{SS} = AV_{SS} = 0.0 V.

*2 : V_{CC} must not drop below V_{SS} – 0.3 V.

*3 : Be careful not to exceed V_{CC} + 0.3 V, for example, when the power is turned on.

*4 : The maximum output current is the peak value for a single pin.

*5 : The average output is the average current for a single pin over a period of 100 ms.

*6 : The total average output current is the average current for all pins over a period of 100 ms.

*7 : If the input current or the maximum input current are limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

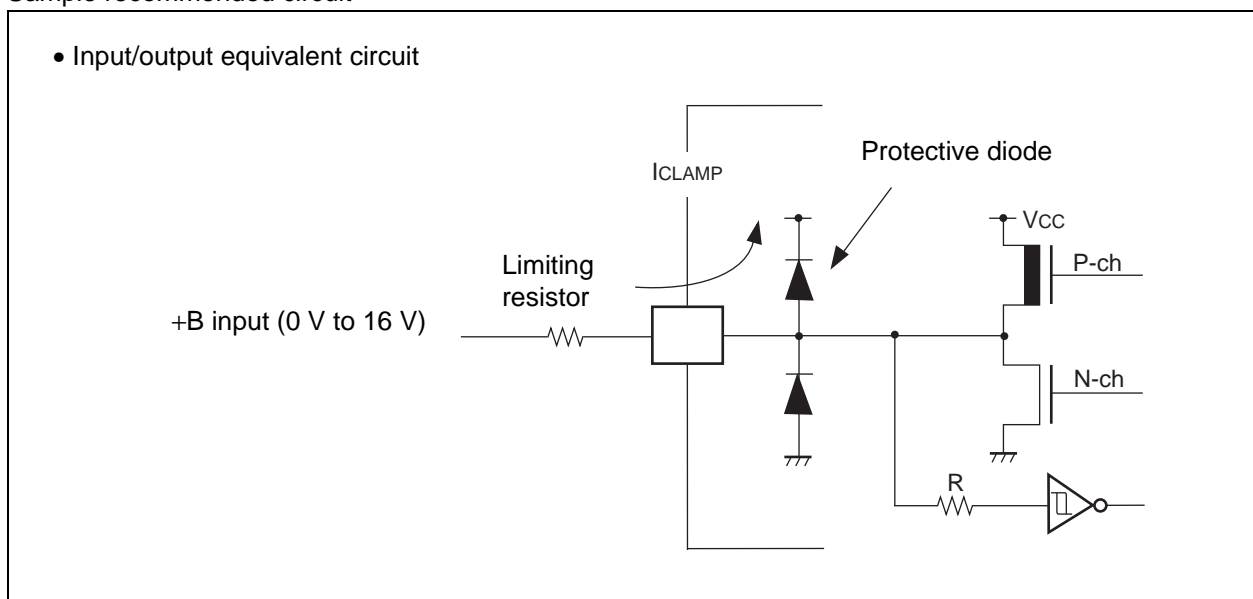
(Continued)

MB91645A Series

(Continued)

*8 : • Corresponding pins : P14 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P62, P67, PC0 to PC7, PD0 to PD7, PE0 to PE7, PF0 to PF6, PG0 to PG7, PH0 to PH7, PI0 to PI7, PJ0 to PJ2, PK2, PK3

- Use within recommended operating conditions.
- Use at DC voltage (current).
- The +B signal should always be applied by connecting a limiting resistor between the +B signal and the microcontroller.
- The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed rated values at any time regardless of instantaneously or constantly when the +B signal is input.
- Note that when the microcontroller drive current is low, such as in the low power consumption modes, the +B input potential can increase the potential at the V_{CC} pin via a protective diode, possibly affecting other devices.
- Note that if the +B signal is input when the microcontroller is off (not fixed at 0V), since the power is supplied through the pin, the microcontroller may operate incompletely.
- Do not leave +B input pins open.
- Sample recommended circuit



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

($V_{SS} = AV_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	2.7	3.6	V	
	V_{DDI}	1.65	1.95	V	
Analog power supply voltage	AV_{CC}	2.7	3.6	V	$AV_{CC} \leq V_{CC}$
Analog reference voltage	AV_{RH}	AV_{SS}	AV_{CC}	V	
Operating temperature	T_a	- 40	+ 85	°C	

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

MB91645A Series

3. DC Characteristics

($V_{CC} = AV_{CC} = 2.7\text{ V to }3.6\text{ V}$, $V_{DDI} = 1.65\text{ V to }1.95\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current (Flash product)	I_{CC}	V_{CC}	Normal operation	—	10	15	mA	CPU: 60MHz Peripheral: 30 MHz*3,*11
	I_{CCS}		SLEEP mode	—	10	15	mA	Peripheral: 30 MHz*3,*11
	I_{CCL}		Sub operation	—	15	100	μA	CPU: 32 kHz Peripheral: 32 kHz *1,*2,*4
	I_{CCT}		Watch mode	—	15	100	μA	*1,*2,*4
	I_{CCH}		STOP mode	—	10	80	μA	*1,*2
	I_{DDI}	V_{DDI}	Normal operation	—	70	90	mA	CPU: 60 MHz Peripheral: 30 MHz*3,*11
	I_{DDIS}		SLEEP mode	—	20	26	mA	Peripheral: 30 MHz*3,*11
	I_{DDIL}		Sub operation	—	150	550	μA	CPU: 32 kHz Peripheral: 32 kHz *1,*2,*4
	I_{DDIT}		Watch mode	—	50	450	μA	*1,*2,*4
	I_{DDIH}		STOP mode	—	50	450	μA	*1,*2
"H" level input voltage	V_{IH}	P00 to P07*5, P10 to P17*6, P60*7	—	$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$	V	
"L" level input voltage	V_{IL}	P00 to P07*5, P10 to P17*6, P60*7	—	$V_{SS} - 0.3$	—	$V_{CC} \times 0.3$	V	

(Continued)

MB91645A Series

($V_{CC} = AV_{CC} = 2.7\text{ V to }3.6\text{ V}$, $V_{DDI} = 1.65\text{ V to }1.95\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage (hysteresis input)	V_{IHS}	P00 to P07*8, P10 to P17*9, P50 to P57, P60*10 P61 to P67, P70 to P77, P80 to P87, P90 to P92, PA0 to PA7, PB0 to PB7, PC0 to PC7, PD0 to PD7, PE0 to PE7, PF0 to PF6, PJ0 to PJ2, PK0 to PK3, \overline{INIT} , MD0, MD1	—	$V_{CC} \times 0.8$	—	$V_{CC} + 0.3$	V	
		P20 to P27, P30 to P37, P40 to P47, PG0 to PG7, PH0 to PH7, PI0 to PI7	—	$V_{CC} \times 0.8$	—	$V_{SS} + 5.5$	V	5 V tolerant

(Continued)

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Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"L" level input voltage (hysteresis input)	V_{ILS}	P00 to P07*8, P10 to P17*9, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60*10, P61 to P67, P70 to P77, P80 to P87, P90 to P92, PA0 to PA7, PB0 to PB7, PC0 to PC7, PD0 to PD7, PE0 to PE7, PF0 to PF6, PJ0 to PJ2, PG0 to PG7, PH0 to PH7, PI0 to PI7, PK0 to PK3, \overline{INIT} , MD0, MD1	—	$V_{SS} - 0.3$	—	$V_{CC} \times 0.2$	V	
"H" level output voltage	V_{OH}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P92, PA0 to PA7, PB0 to PB7, PC0 to PC7, PD0 to PD7, PE0 to PE7, PF0 to PF6, PJ0 to PJ2, PG0 to PG7, PH0 to PH7, PI0 to PI7, PK0 to PK3	$V_{CC} = 2.7\text{ V}$ $I_{OH} = -4\text{ mA}$	$V_{CC} - 0.5$	—	V_{CC}	V	
"L" level output voltage	V_{OL}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P92, PA0 to PA7, PB0 to PB7, PC0 to PC7, PD0 to PD7, PE0 to PE7, PF0 to PF6, PJ0 to PJ2, PG0 to PG7, PH0 to PH7, PI0 to PI7, PK0 to PK3	$V_{CC} = 2.7\text{ V}$ $I_{OL} = 4\text{ mA}$	V_{SS}	—	0.4	V	
Input leak current	I_{IL}	—	—	- 5	—	+ 5	μA	Digital pin
				- 10	—	+ 10	μA	Analog pin

(Continued)

(Continued)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Pull-up resistance value	R _{PU}	Pull-up pin	—	16.6	33	66	kΩ	
Input capacitance	C _{IN}	Other than V _{CC} , V _{DDI} , V _{SS} , AV _{CC} , AV _{SS} , AVRH	—	—	10	15	pF	

*1 : When opened, all ports are fixed to output

*2 : Ta = + 25 °C, V_{DDI} = 1.8 V and V_{CC} = 3.3 V

*3 : X0 = 15 MHz, CPU clock = 60 MHz and X0A = when stopped

*4 : X0 = STOP and X0A = 32 kHz

*5 : When using as D00 to D07 pin

*6 : When using as D08 to D15 pin

*7 : When using as RDY input

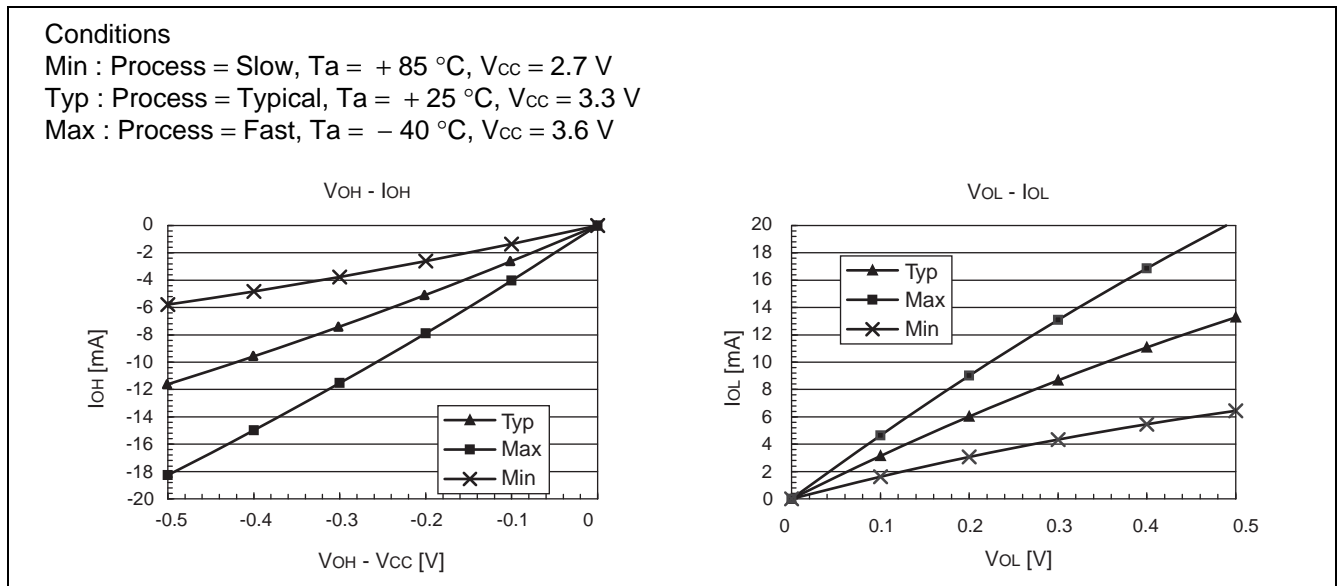
*8 : When using other than D00 to D07 pin

*9 : When using other than D08 to D15 pin

*10 : When using other than RDY input

*11 : When 50 pins with an external capacitor of 50 pF each output at the frequency of 1 MHz.

• V-I characteristics



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4. AC Characteristics

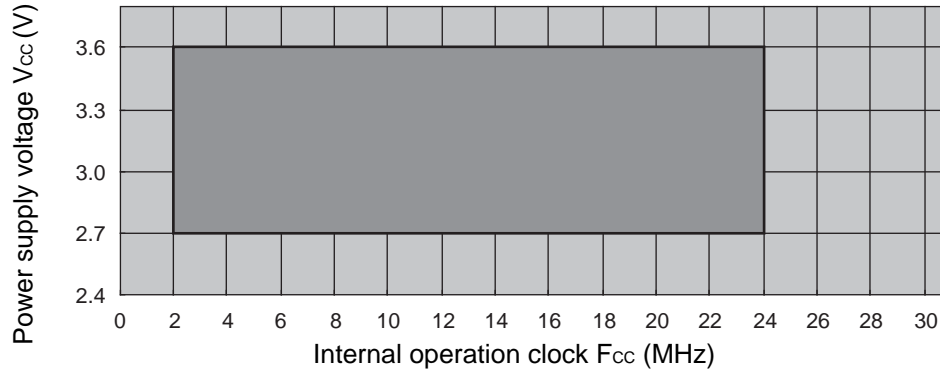
(1) Main Clock (MCLK) Input Standard

($V_{CC} = AV_{CC} = 2.7\text{ V to }3.6\text{ V}$, $V_{DDI} = 1.65\text{ V to }1.95\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$)

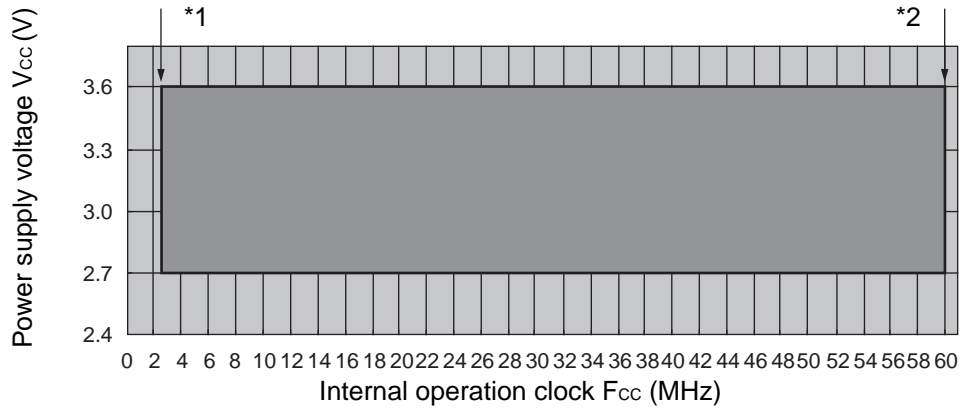
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	F_{CH}	X0, X1	—	4	48	MHz	When crystal oscillator is connected
			—	4	48	MHz	When using external clock
Input clock cycle	t_{CYLH}		—	20.83	250	ns	When using external clock
Input clock pulse width	—		P_{WH}/t_{CYLH} P_{WL}/t_{CYLH}	45	55	%	When using external clock
Input clock rise time and fall time	t_{CF} t_{CR}		—	—	5	ns	When using external clock
Internal operating clock frequency	F_{CS}	—	—	—	60	MHz	Source clock
	F_{CC}	—	—	—	60	MHz	CPU clock
	F_{CP}	—	—	—	40	MHz	Peripheral bus clock
	F_{CT}	—	—	—	40	MHz	External bus clock
Internal operating clock cycle time	t_{CYCS}	—	—	16.7	—	ns	Source clock
	t_{CYCC}	—	—	16.7	—	ns	CPU clock
	t_{CYCP}	—	—	25	—	ns	Peripheral bus clock
	t_{CYCT}	—	—	25	—	ns	External bus clock

- Operation Guaranteed Range

- When the main clock is selected (DIVB = 000)



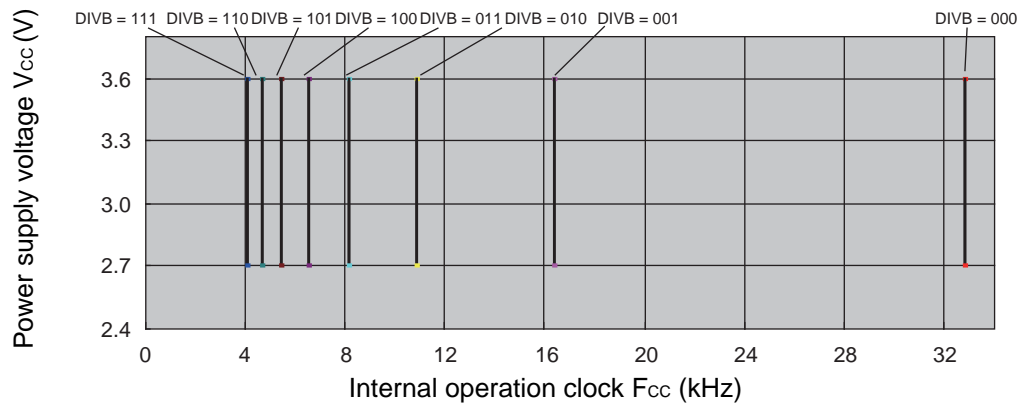
- When the PLL clock is selected



*1 : DIVB = 111, ODS = 11, and PLL macro oscillation frequency = 80 MHz

*2 : DIVB = 000, ODS = 01, and PLL macro oscillation frequency = 120 MHz

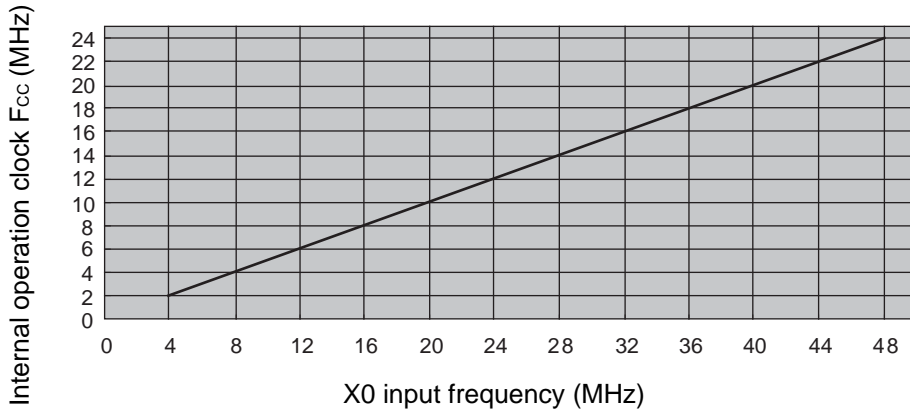
- When the sub clock is selected ($F_{CL} = 32.768$ kHz)



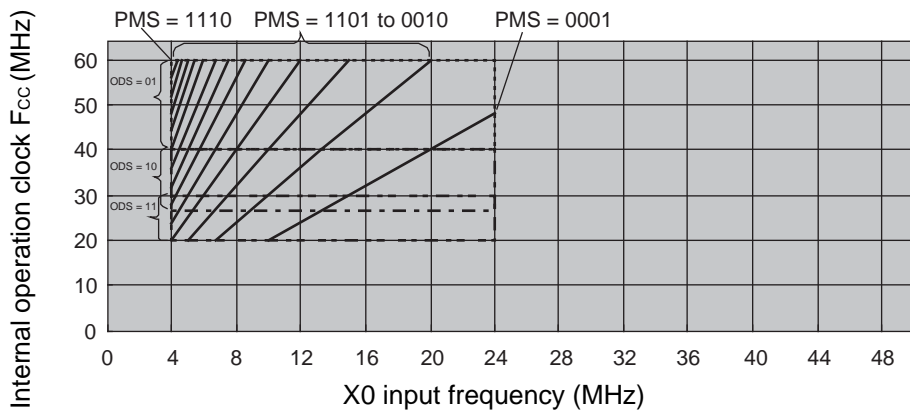
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- Example of configuration

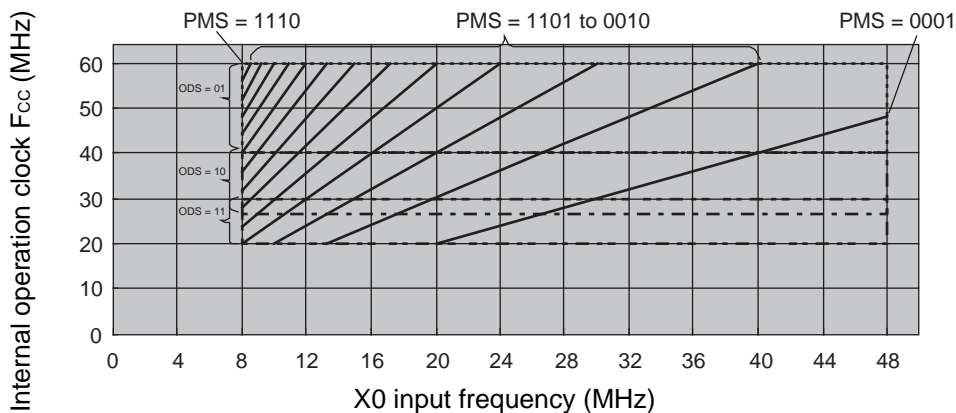
- When the main clock is selected (DIVB = 000 *1)



- When the PLL clock is selected (DIVB = 000 *1, PDS = 0000 *2)



- When the PLL clock is selected (DIVB = 000 *1, PDS = 0001 *2)



*1 : The values other than DIVB = 000 are omitted.

*2 : The values other than PDS = 0000 and 0001 are omitted.

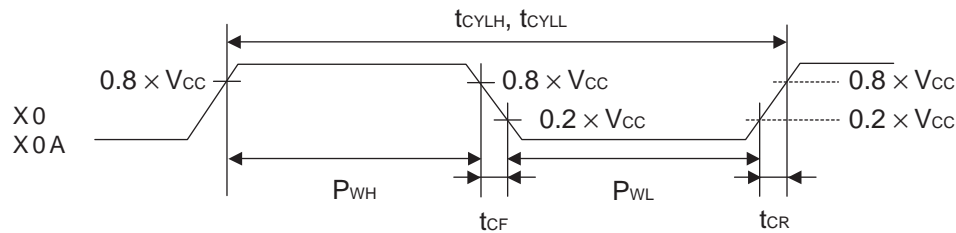
Note: DIVB : Base clock division configuration bit
 ODS : PLL macro oscillation clock division rate select bit
 PDS : PLL input clock division select bit
 PMS : PLL clock multiple rate select bit

(2) Sub Clock (SBCLK) Input Standard

($V_{CC} = AV_{CC} = 2.7\text{ V to }3.6\text{ V}$, $V_{DDI} = 1.65\text{ V to }1.95\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Condi-tions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	F_{CL}	X0A, X1A	—	—	32.768	—	kHz	When crystal oscillator is connected
			—	—	32.768	—		kHz
Input clock cycle	t_{CYLL}		—	—	30.518	—	μs	When using external clock
Input clock pulse width	—		P_{WH}/t_{CYLL} P_{WL}/t_{CYLL}	45	—	55	%	When using external clock
Input clock rise time and fall time	t_{CF} , t_{CR}		—	—	—	200	ns	When using external clock

<When external clock input>



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(3) Conditions of PLL

($V_{CC} = AV_{CC} = 2.7\text{ V to }3.6\text{ V}$, $V_{DDI} = 1.65\text{ V to }1.95\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Condi- tions	Value			Unit	Remarks
			Min	Typ	Max		
PLL oscillation stabilization wait time (LOCK UP time)	t_{LOCK}	—	600	—	—	μs	Time from when the PLL starts operating until the oscillation stabilizes
PLL input clock frequency	f_{PLLI}	—	4	—	24	MHz	
PLL multiple rate	—	—	4	—	30	multiplied by	ODS \times PMS
PLL macro oscillation clock frequency	f_{PLLO}	—	80	—	120	MHz	

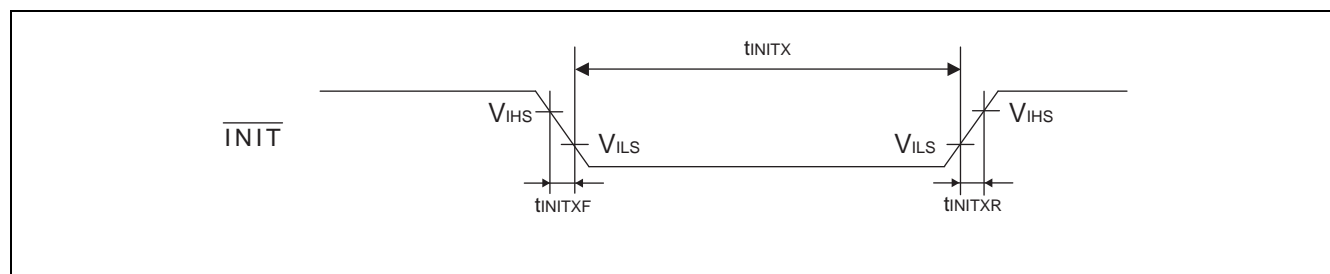
(4) Reset Input Standards

($V_{CC} = AV_{CC} = 2.7\text{ V to }3.6\text{ V}$, $V_{DDI} = 1.65\text{ V to }1.95\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condi- tions	Value		Unit	Remarks
				Min	Max		
Reset input time (At power-on, main oscillation stop mode)	t_{INITX}	$\overline{\text{INIT}}$	—	Oscillation time of oscillator + 10 t_{CYLH}	—	ns	*
Reset input time (At other times)				10 t_{CYLH}	—	ns	
Reset input rise time and fall time	t_{INITXF} t_{INITXR}			—	—	10	ms

* : To make $\overline{\text{INIT}} = \text{"L"}$ during below state, hold the input 50 μs or over to the INIT pin.

- At power-on
- When in stop mode



(5) Clock Output Timing

- $t_{CHCL} : t_{CLCH} = 1 : 1$ (divided by 1, 2, 4, 6, 8)

($V_{CC} = AV_{CC} = 2.7\text{ V to }3.6\text{ V}$, $V_{DDI} = 1.65\text{ V to }1.95\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Cycle time	t_{CYC}	SYSCLK	$F_{CT} = F_{CC}$, $F_{CT} = F_{CC}/2$	t_{CYCT}	—	ns
SYSCLK \uparrow →SYSCLK \downarrow	t_{CHCL}			$t_{CYC} / 2 - 5$	$t_{CYC} / 2 + 5$	ns
SYSCLK \downarrow →SYSCLK \uparrow	t_{CLCH}			$t_{CYC} / 2 - 5$	$t_{CYC} / 2 + 5$	ns

Notes: • t_{CYC} is a frequency of 1 clock cycle indicating gear ratio.

- When DIVT = 000, be sure to set as DIVB=000.

- $t_{CHCL} : t_{CLCH} = 1 : 2$ (divided by 3)

($V_{CC} = AV_{CC} = 2.7\text{ V to }3.6\text{ V}$, $V_{DDI} = 1.65\text{ V to }1.95\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Cycle time	t_{CYC}	SYSCLK	$F_{CT} = F_{CC}$, $F_{CT} = F_{CC}/2$	t_{CYCT}	—	ns
SYSCLK \uparrow →SYSCLK \downarrow	t_{CHCL}			$1 / 3 t_{CYC} - 5$	$1 / 3 t_{CYC} + 5$	ns
SYSCLK \downarrow →SYSCLK \uparrow	t_{CLCH}			$2 / 3 t_{CYC} - 5$	$2 / 3 t_{CYC} + 5$	ns

Note: t_{CYC} is a frequency of 1 clock cycle indicating gear ratio.

- $t_{CHCL} : t_{CLCH} = 2 : 3$ (divided by 5)

($V_{CC} = AV_{CC} = 2.7\text{ V to }3.6\text{ V}$, $V_{DDI} = 1.65\text{ V to }1.95\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Cycle time	t_{CYC}	SYSCLK	$F_{CT} = F_{CC}$, $F_{CT} = F_{CC}/2$	t_{CYCT}	—	ns
SYSCLK \uparrow →SYSCLK \downarrow	t_{CHCL}			$2 / 5 t_{CYC} - 5$	$2 / 5 t_{CYC} + 5$	ns
SYSCLK \downarrow →SYSCLK \uparrow	t_{CLCH}			$3 / 5 t_{CYC} - 5$	$3 / 5 t_{CYC} + 5$	ns

Note: t_{CYC} is a frequency of 1 clock cycle indicating gear ratio.

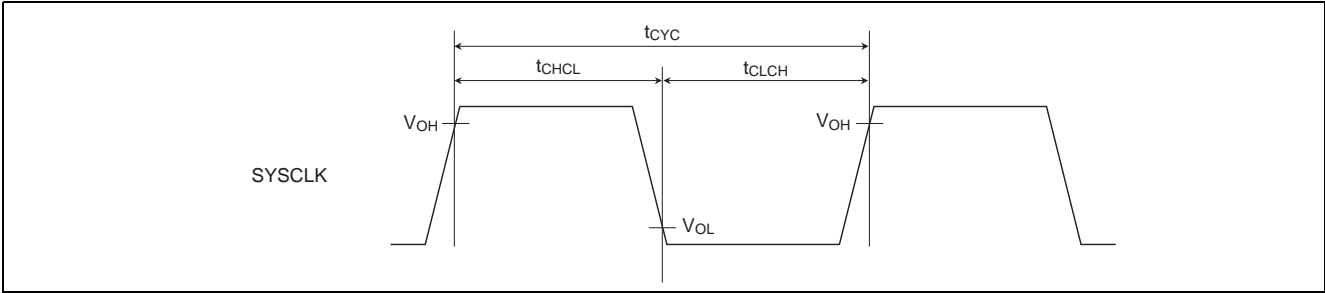
- $t_{CHCL} : t_{CLCH} = 3 : 4$ (divided by 7)

($V_{CC} = AV_{CC} = 2.7\text{ V to }3.6\text{ V}$, $V_{DDI} = 1.65\text{ V to }1.95\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Cycle time	t_{CYC}	SYSCLK	$F_{CT} = F_{CC}$, $F_{CT} = F_{CC}/2$	t_{CYCT}	—	ns
SYSCLK \uparrow →SYSCLK \downarrow	t_{CHCL}			$3 / 7 t_{CYC} - 5$	$3 / 7 t_{CYC} + 5$	ns
SYSCLK \downarrow →SYSCLK \uparrow	t_{CLCH}			$4 / 7 t_{CYC} - 5$	$4 / 7 t_{CYC} + 5$	ns

Note: t_{CYC} is a frequency of 1 clock cycle indicating gear ratio.

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(6) Split Bus Access Read/Write Operation

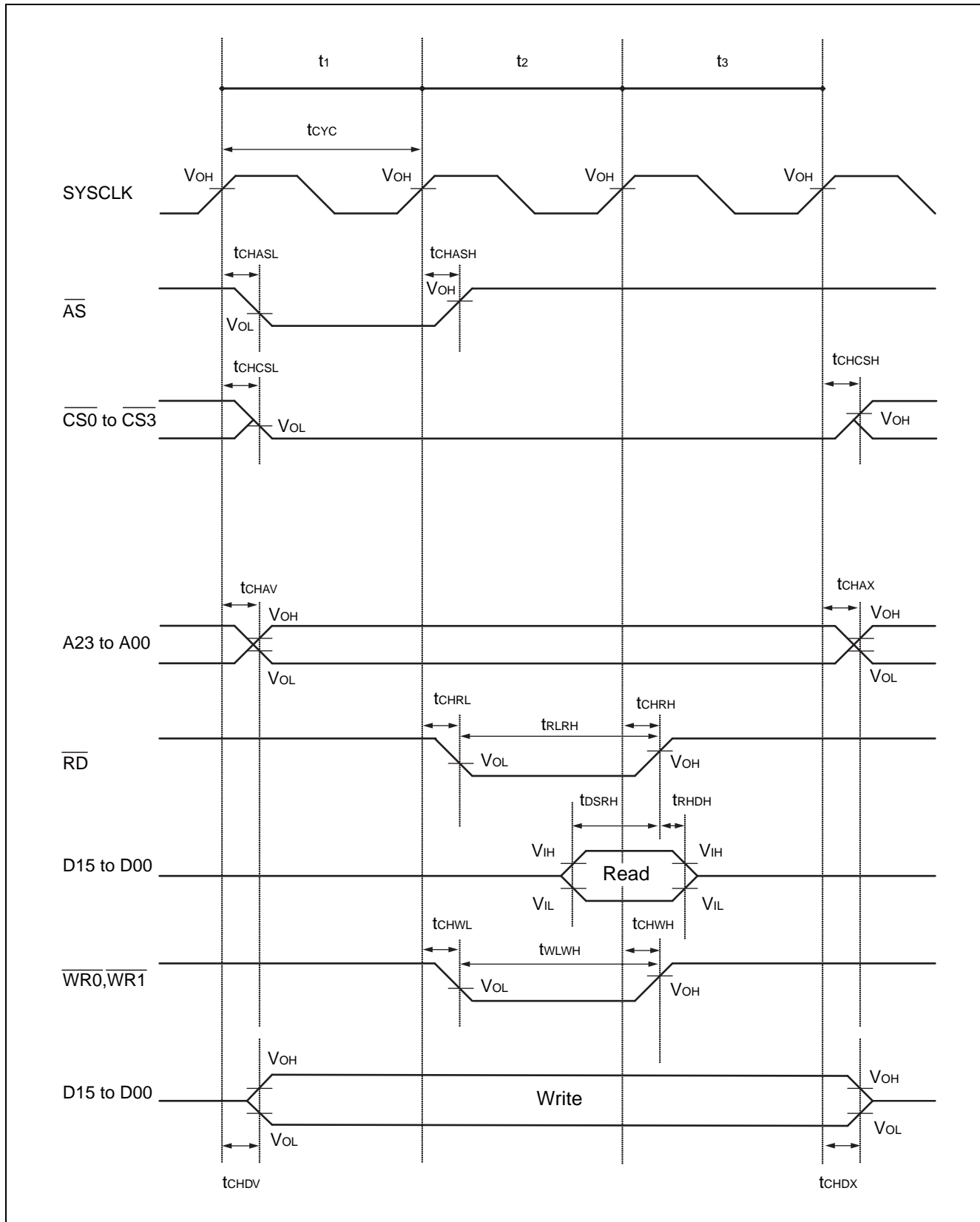
($V_{CC} = AV_{CC} = 2.7\text{ V to }3.6\text{ V}$, $V_{DDI} = 1.65\text{ V to }1.95\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Condi- tions	Value		Unit	Remarks
				Min	Max		
\overline{AS} delay time	t_{CHASL}	SYSCLK \overline{AS}	—	0.6	10	ns	
	t_{CHASH}						
$\overline{CS0}$ to $\overline{CS3}$ delay time	t_{CHCSL}	SYSCLK $\overline{CS0}$ to $\overline{CS3}$		0.6	10	ns	
	t_{CHCSH}						
Address delay time	t_{CHAV}	SYSCLK A23 to A00		0.6	10	ns	
	t_{CHAX}						
\overline{RD} delay time	t_{CHRL}	SYSCLK \overline{RD}		0.6	10	ns	
	t_{CHRH}						
\overline{RD} minimum pulse width	t_{RLRH}	\overline{RD}		$t_{CYC} - 10$	—	ns	*
Data setup $\rightarrow \overline{RD}\uparrow$ time	t_{DSRH}	\overline{RD}		18	—	ns	
$\overline{RD}\uparrow \rightarrow$ data hold time	t_{RHDX}	D15 to D00		0	—	ns	
$\overline{WR0}$, $\overline{WR1}$ delay time	t_{CHWL}	SYSCLK $\overline{WR0}$, $\overline{WR1}$		0.6	10	ns	
	t_{CHWH}						
$\overline{WR0}$, $\overline{WR1}$ minimum pulse width	t_{WLWH}	$\overline{WR0}$, $\overline{WR1}$	$t_{CYC} - 10$	—	ns	*	
$\text{SYSCLK}\uparrow \rightarrow$ Data output time	t_{CHDV}	SYSCLK	0.6	15	ns		
$\text{SYSCLK}\uparrow \rightarrow$ Data hold time	t_{CHDX}	D15 to D00	0.6	15	ns		

* : When the bus timing is delayed by an automatic wait insertion or RDY input, add the time ($t_{CYC} \times$ the number of delay cycles added) to this rating.

Note: When the external load capacitance $C = 50\text{ pF}$.

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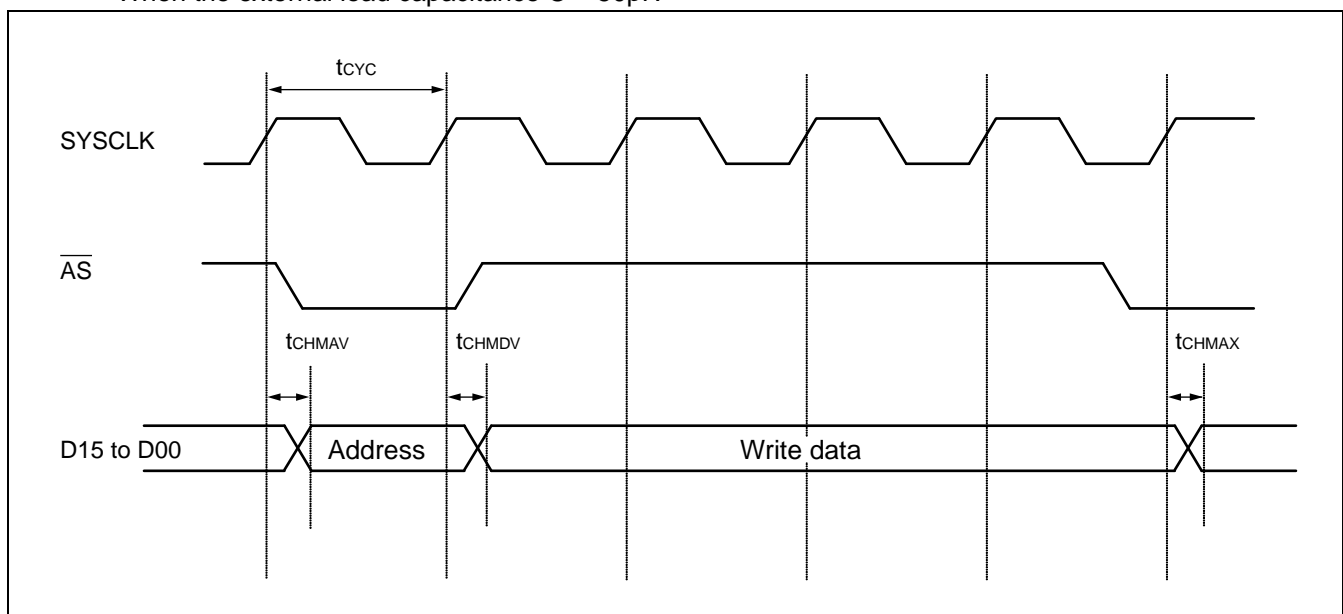
(7) Multiplexed Bus Access Read/Write Operation

($V_{CC} = AV_{CC} = 2.7\text{ V to }3.6\text{ V}$, $V_{DDI} = 1.65\text{ V to }1.95\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
SYSCLK \uparrow → D15 to D00 address delay time	t_{CHMAV}	SYSCLK D15 to D00 (address)	—	0.6	15	ns
	t_{CHMAX}					
SYSCLK \uparrow → D15 to D00 data delay time	t_{CHMDV}			0.6	15	ns

Notes: • The ratings not listed here are the same as the split bus interface.

• When the external load capacitance $C = 50\text{ pF}$.

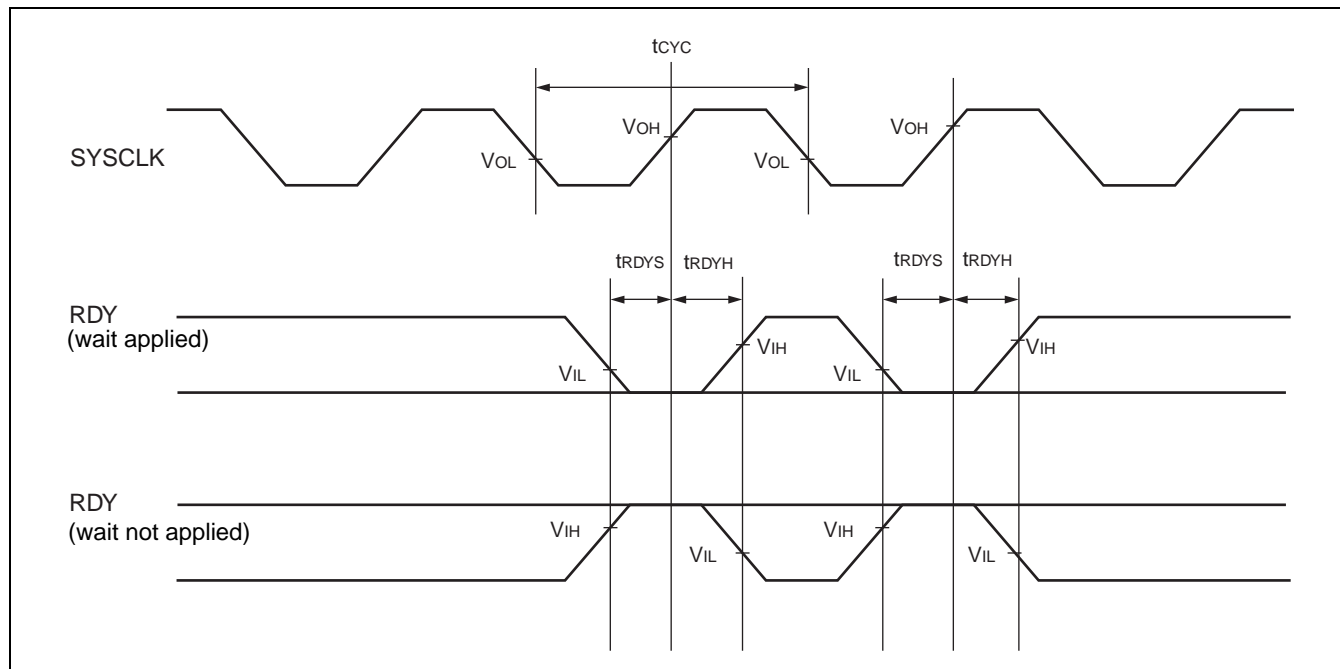


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(8) Ready Input Timing

($V_{CC} = AV_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$, $V_{DDI} = 1.65 \text{ V to } 1.95 \text{ V}$, $V_{SS} = AV_{SS} = 0 \text{ V}$, $T_a = -40 \text{ }^\circ\text{C to } +85 \text{ }^\circ\text{C}$)

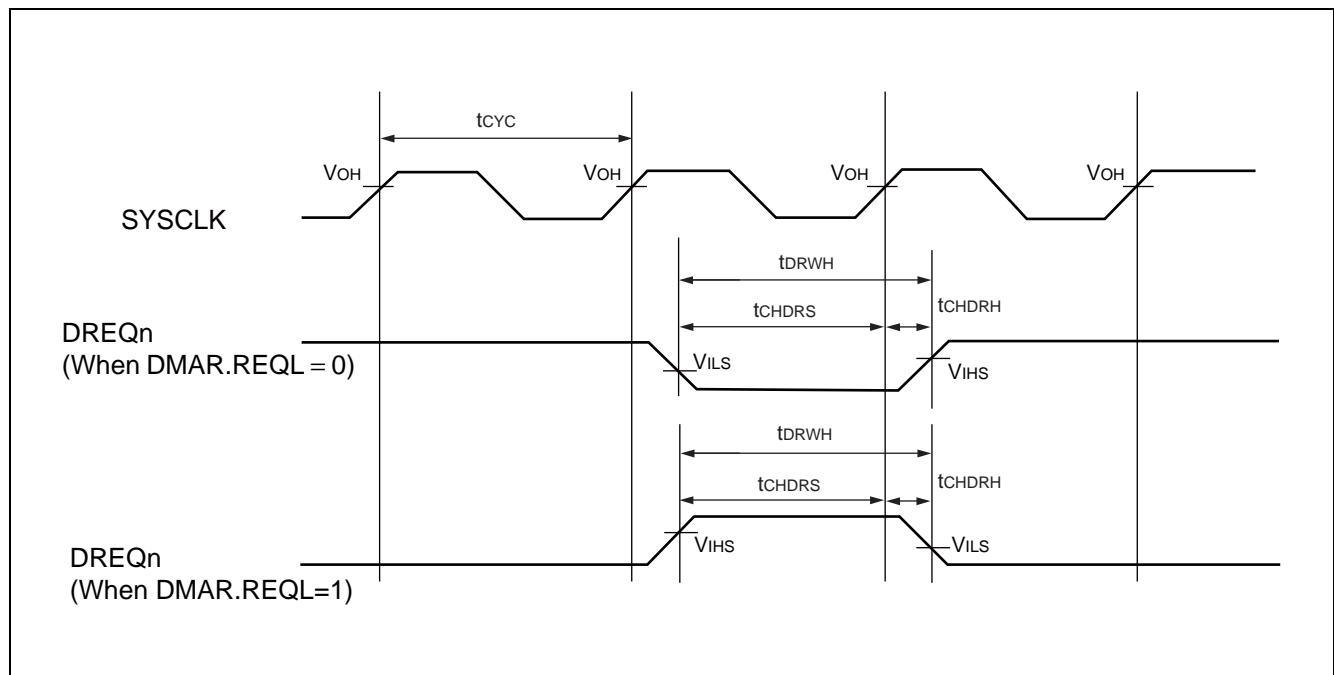
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
RDY setup time \rightarrow SYSCLK \uparrow	t_{RDYS}	SYSCLK RDY	—	18	—	ns
SYSCLK \uparrow \rightarrow RDY hold time	t_{RDYH}	SYSCLK RDY		0	—	ns



(9) DMA Controller Timing

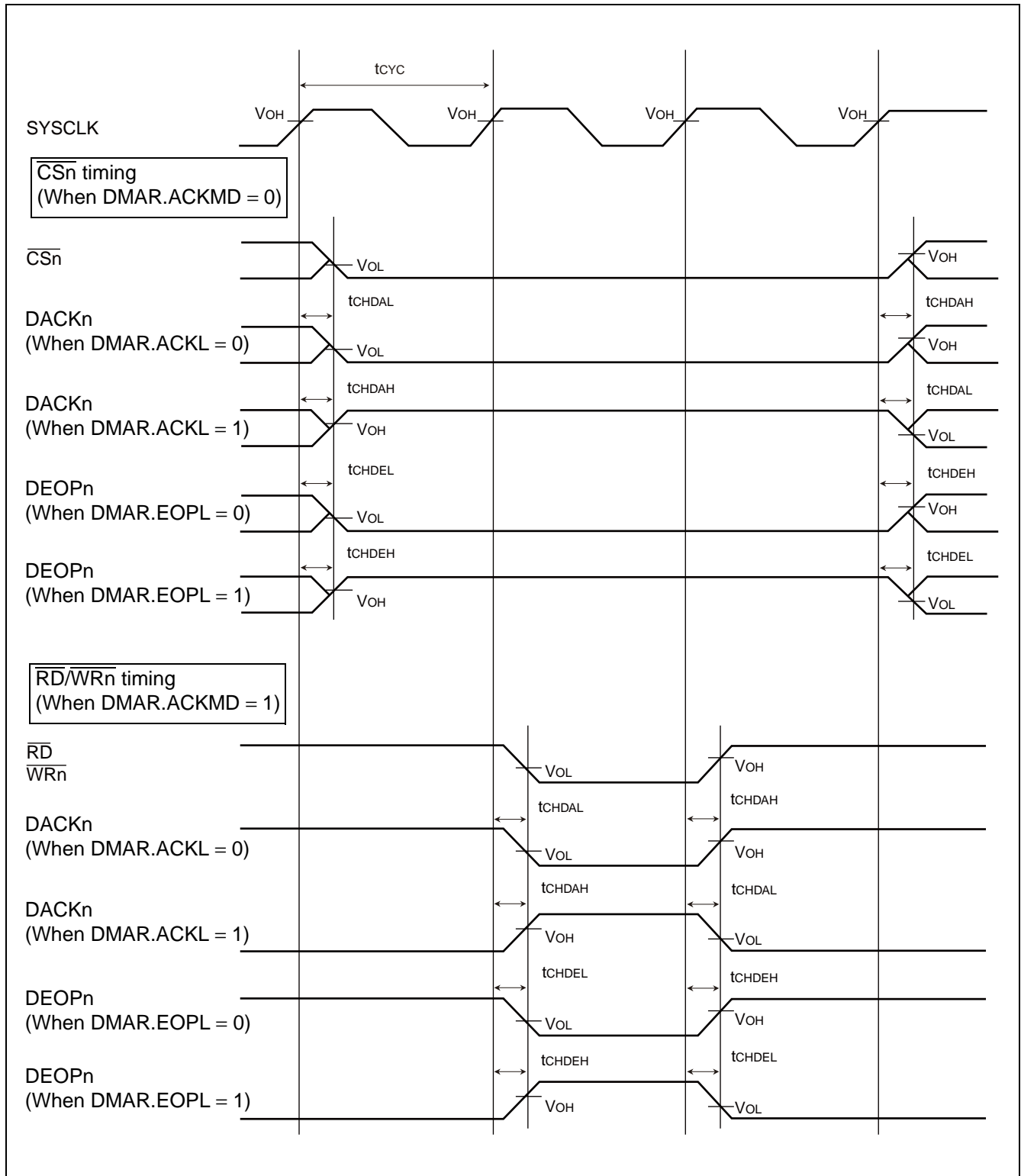
($V_{CC} = AV_{CC} = 2.7\text{ V to }3.6\text{ V}$, $V_{DDI} = 1.65\text{ V to }1.95\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
DREQ input pulse width	t_{DRWH}	DREQn	—	$2 t_{CYCT}$	—	ns
DACK delay time	t_{CHDAL}	SYSCLK DACKn		0.6	10	ns
	t_{CHDAH}					
DEOP delay time	t_{CHDEL}	SYSCLK DEOPn		0.6	10	ns
	t_{CHDEH}					
DREQ setup time	t_{CHDRS}	SYSCLK DREQn		18	—	ns
DREQ hold time	t_{CHDRH}	SYSCLK DREQn	0	—	ns	



Note: When the external load capacitance $C = 50\text{ pF}$.

MB91645A Series

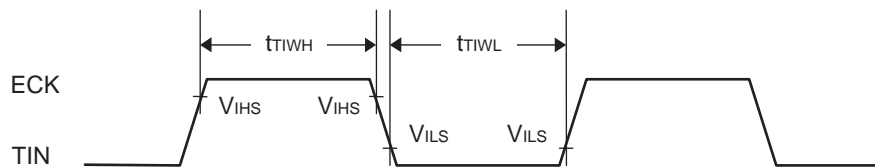


(10) Base Timer Input Timing

- Timer input timing

($V_{CC} = AV_{CC} = 2.7\text{ V to }3.6\text{ V}$, $V_{DD1} = 1.65\text{ V to }1.95\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$)

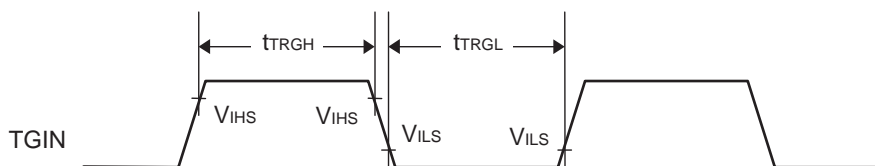
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	TIOAn/TIOBn (When used as ECK, TIN)	—	$2 t_{CYCP}$	—	ns



- Trigger Input Timing

($V_{CC} = AV_{CC} = 2.7\text{ V to }3.6\text{ V}$, $V_{DD1} = 1.65\text{ V to }1.95\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Input pulse width	t_{TRGH} t_{TRGL}	TIOAn/TIOBn (When used as TGIN)	—	$2 t_{CYCP}$	—	ns



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(11) Synchronous serial (CSIO) timing

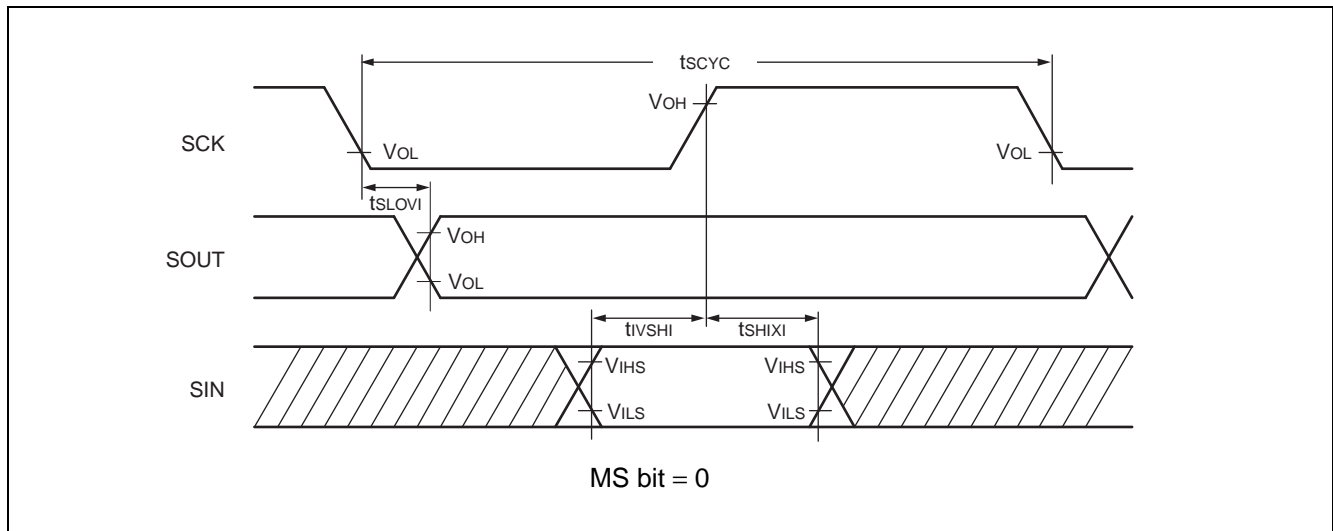
($V_{CC} = AV_{CC} = 2.7\text{ V to }3.6\text{ V}$, $V_{DD1} = 1.65\text{ V to }1.95\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$)

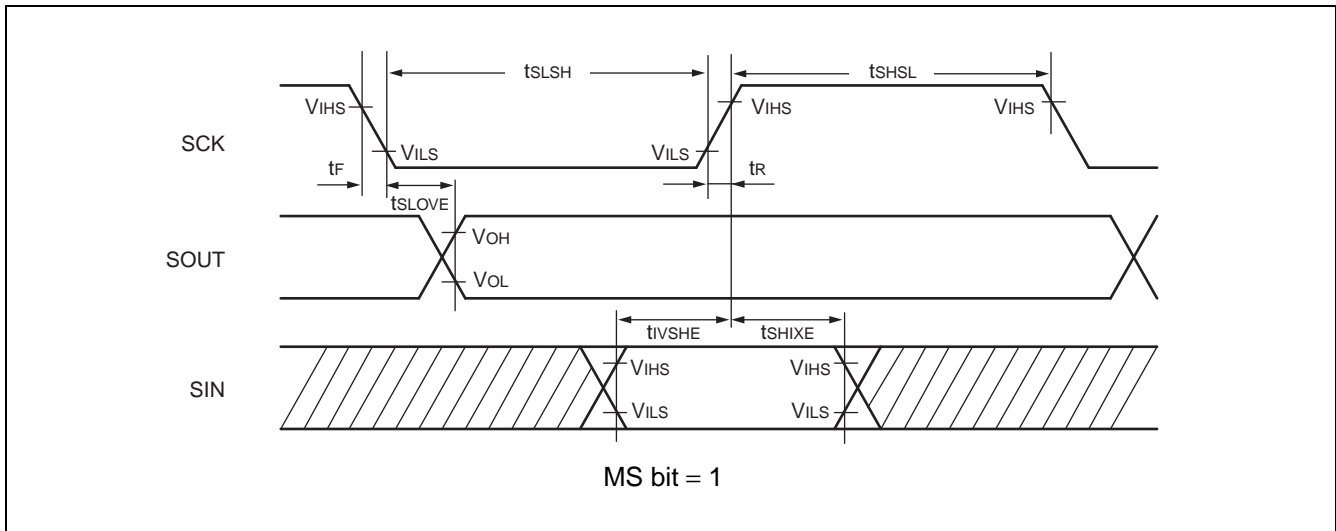
- Synchronous serial (SPI = 0, SCINV = 0)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCKn	Internal shift clock operation	$4t_{CYCP}$	—	ns
SCK ↓ → SOUT delay time	t_{SLOVI}	SCKn SOUTn		- 30	+ 30	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKn SINn		45	—	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKn SINn		0	—	ns
Serial clock "L" pulse width	t_{LSLH}	SCKn	External shift clock operation	$2t_{CYCP} - 10$	—	ns
Serial clock "H" pulse width	t_{HSLH}	SCKn		$t_{CYCP} + 10$	—	ns
SCK ↓ → SOUT delay time	t_{SLOVE}	SCKn SOUTn		—	40	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKn SINn		15	—	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKn SINn		20	—	ns
SCK fall time	t_F	SCKn	—	—	5	ns
SCK rise time	t_R	SCKn	—	—	5	ns

Notes: • The above standards apply to CLK synchronous mode.

- t_{CYCP} indicates the peripheral clock cycle time.
- When the external load capacitance $C = 50\text{ pF}$.





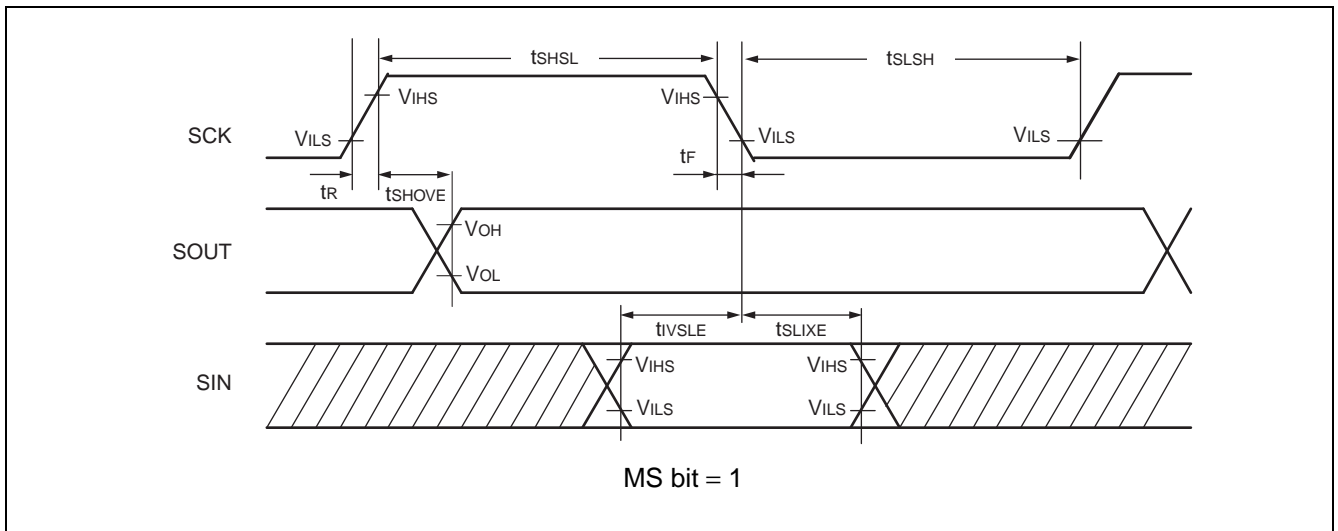
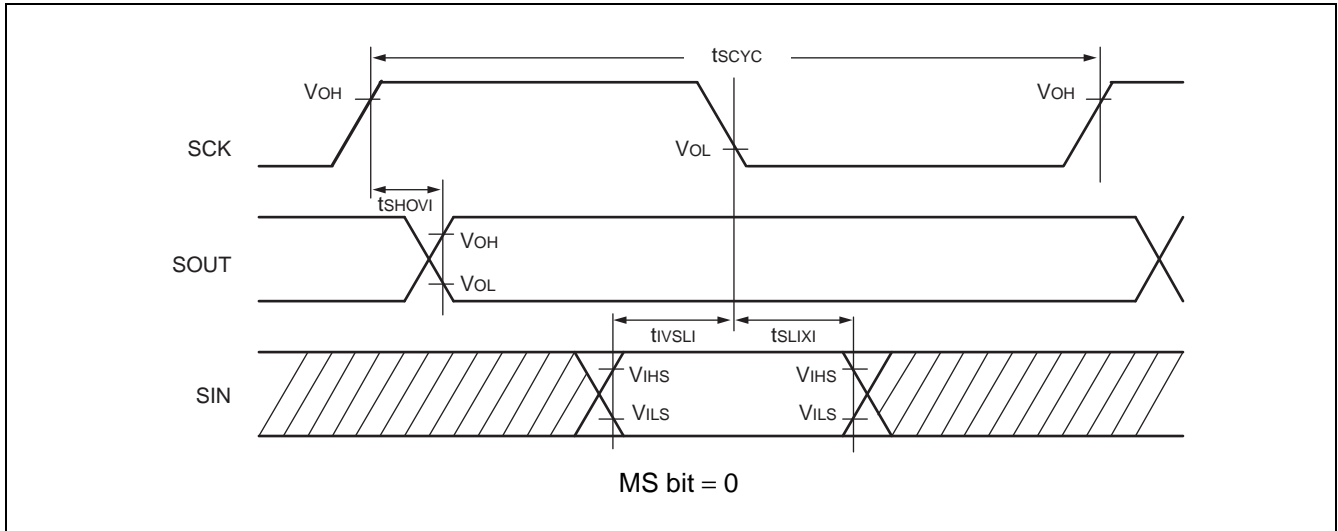
- Synchronous serial (SPI = 0, SCINV = 1)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCKn	Internal shift clock operation	$4t_{CYCP}$	—	ns
SCK \uparrow → SOUT delay time	t_{SHOVI}	SCKn SOUTn		- 30	+ 30	ns
SIN → SCK \downarrow setup time	t_{IVSLI}	SCKn SINn		45	—	ns
SCK \downarrow → SIN hold time	t_{SLIXI}	SCKn SINn		0	—	ns
Serial clock “L” pulse width	t_{LSH}	SCKn	External shift clock operation	$2t_{CYCP} - 10$	—	ns
Serial clock “H” pulse width	t_{HSL}	SCKn		$t_{CYCP} + 10$	—	ns
SCK \uparrow → SOUT delay time	t_{SHOVE}	SCKn SOUTn		—	40	ns
SIN → SCK \downarrow setup time	t_{IVSLE}	SCKn SINn		15	—	ns
SCK \downarrow → SIN hold time	t_{SLIXE}	SCKn SINn		20	—	ns
SCK fall time	t_F	SCKn		—	5	ns
SCK rise time	t_R	SCKn		—	5	ns

Notes: • The above standards apply to CLK synchronous mode.

- t_{CYCP} indicates the peripheral clock cycle time.
- When the external load capacitance $C = 50\text{pF}$.

MB91645A Series

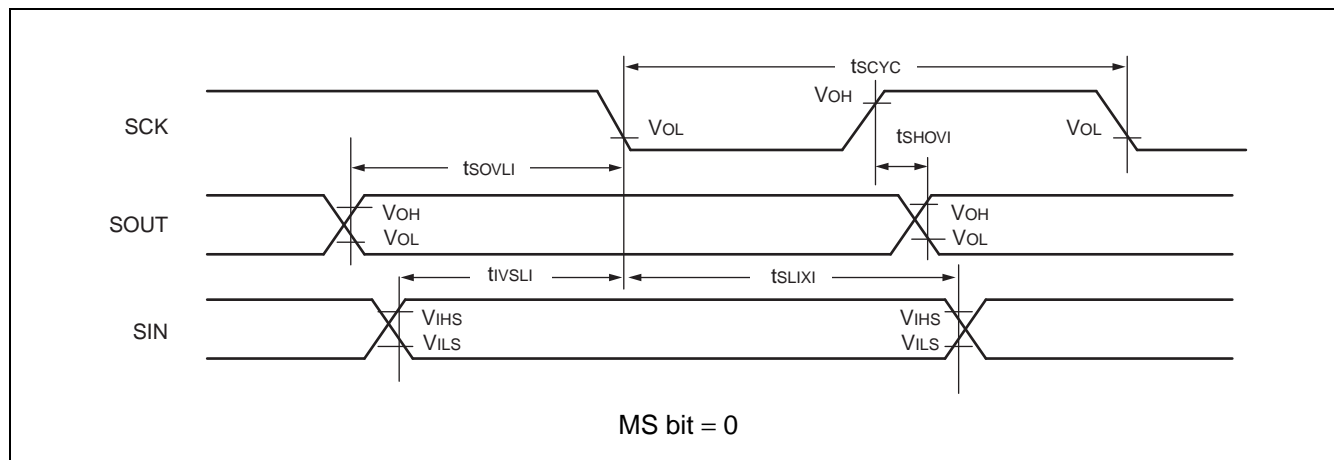


- Synchronous serial (SPI = 1, SCINV = 0)

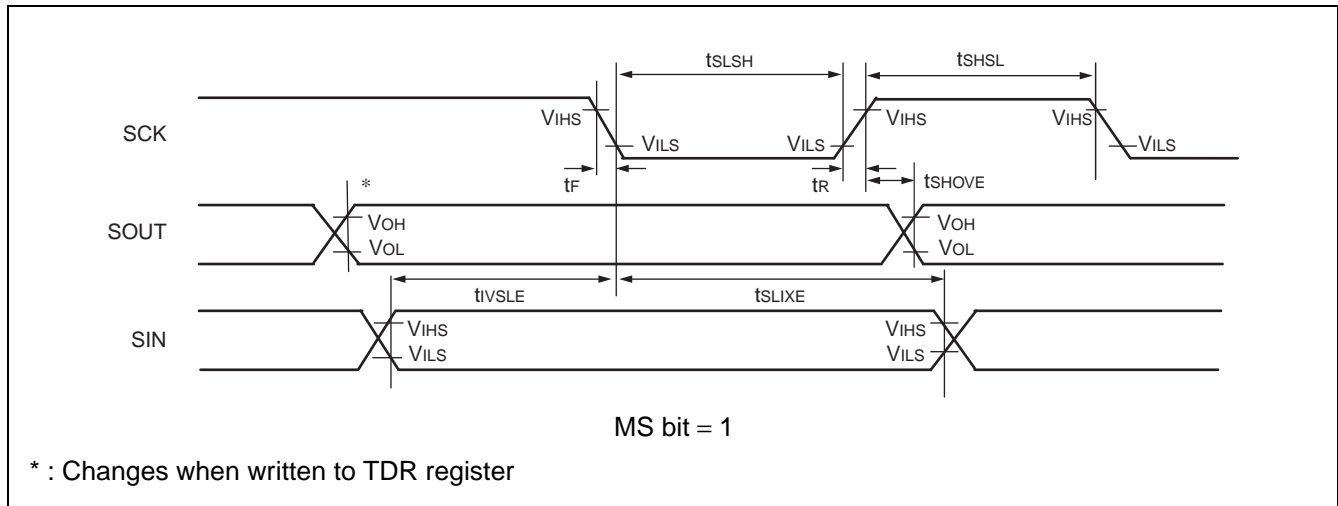
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCKn	Internal shift clock operation	4tcycp	—	ns
SCK \uparrow \rightarrow SOUT delay time	t_{SHOVI}	SCKn SOUTn		- 30	+ 30	ns
SIN \rightarrow SCK \downarrow setup time	t_{IVSLI}	SCKn SINn		45	—	ns
SCK \downarrow \rightarrow SIN hold time	t_{SLIXI}	SCKn SINn		0	—	ns
SOUT \rightarrow SCK \downarrow delay time	t_{SOVLI}	SCKn SOUTn		2tcycp - 30	—	ns
Serial clock "L" pulse width	t_{SLSH}	SCKn		2tcycp - 10	—	ns
Serial clock "H" pulse width	t_{SHSL}	SCKn	tcycp + 10	—	ns	
SCK \uparrow \rightarrow SOUT delay time	t_{SHOVE}	SCKn SOUTn	External shift clock operation	—	40	ns
SIN \rightarrow SCK \downarrow setup time	t_{IVSLE}	SCKn SINn		15	—	ns
SCK \downarrow \rightarrow SIN hold time	t_{SLIXE}	SCKn SINn		20	—	ns
SCK fall time	t_F	SCKn		—	5	ns
SCK rise time	t_R	SCKn		—	5	ns

Notes: • The above standards apply to CLK synchronous mode.

- t_{CYCP} indicates the peripheral clock cycle time.
- When the external load capacitance $C = 50\text{pF}$.



MB91645A Series

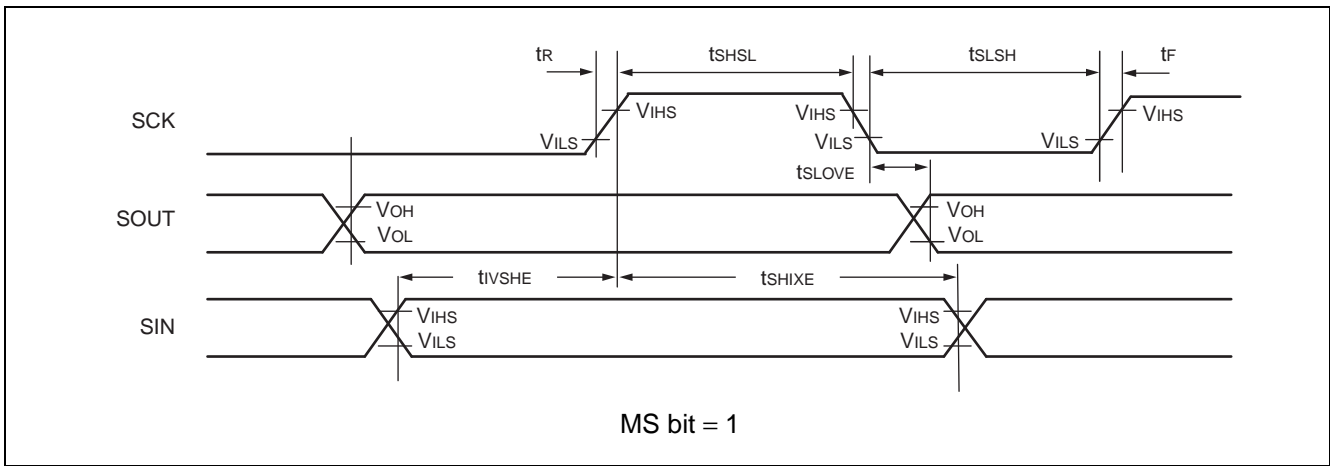
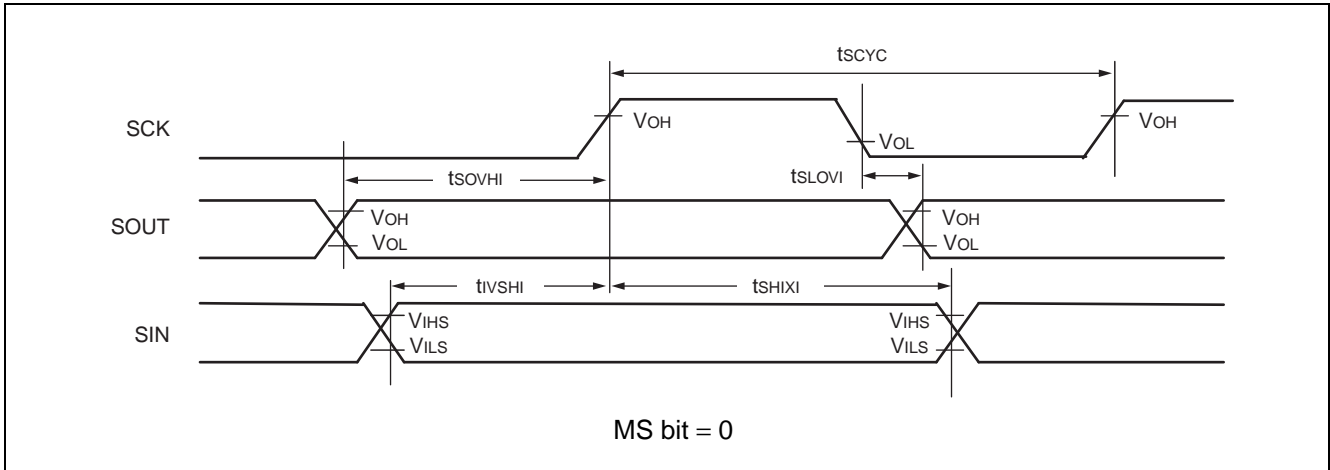


- Synchronous serial (SPI = 1, SCINV = 1)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCKn	Internal shift clock operation	4tcycp	—	ns
SCK ↓ → SOUT delay time	t_{SLOVI}	SCKn SOUTn		- 30	+ 30	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKn SINn		45	—	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKn SINn		0	—	ns
SOUT → SCK ↑ delay time	t_{SOVHI}	SCKn SOUTn		2tcycp - 30	—	ns
Serial clock "L" pulse width	t_{SLSH}	SCKn		2tcycp - 10	—	ns
Serial clock "H" pulse width	t_{SHSL}	SCKn	External shift clock operation	tcycp + 10	—	ns
SCK ↓ → SOUT delay time	t_{SLOVE}	SCKn SOUTn		—	40	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKn SINn		15	—	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKn SINn		20	—	ns
SCK fall time	t_F	SCKn		—	5	ns
SCK rise time	t_R	SCKn		—	5	ns

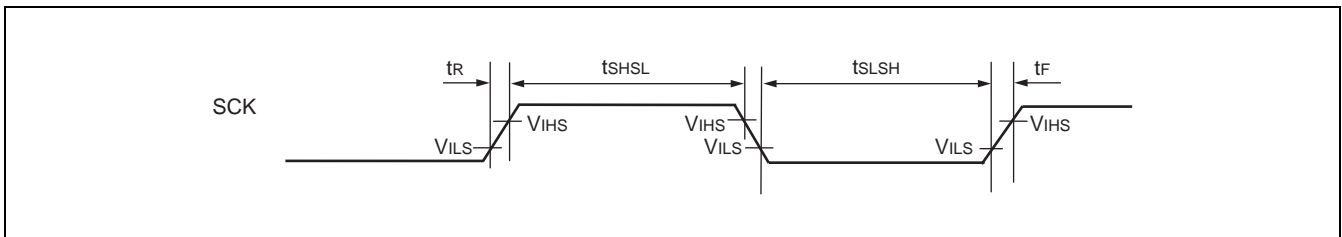
Notes: • The above standards apply to CLK synchronous mode.

- t_{CYCP} indicates the peripheral clock cycle time.
- When the external load capacitance $C = 50pF$.



• External clock (EXT = 1) : asynchronous only

Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
Serial clock "L" pulse width	t_{SLSH}	$C_L = 50 \text{ pF}$	$t_{cycp} + 10$	—	ns
Serial clock "H" pulse width	t_{SHSL}		$t_{cycp} + 10$	—	ns
SCK fall time	t_F		—	5	ns
SCK rise time	t_R		—	5	ns



MB91645A Series

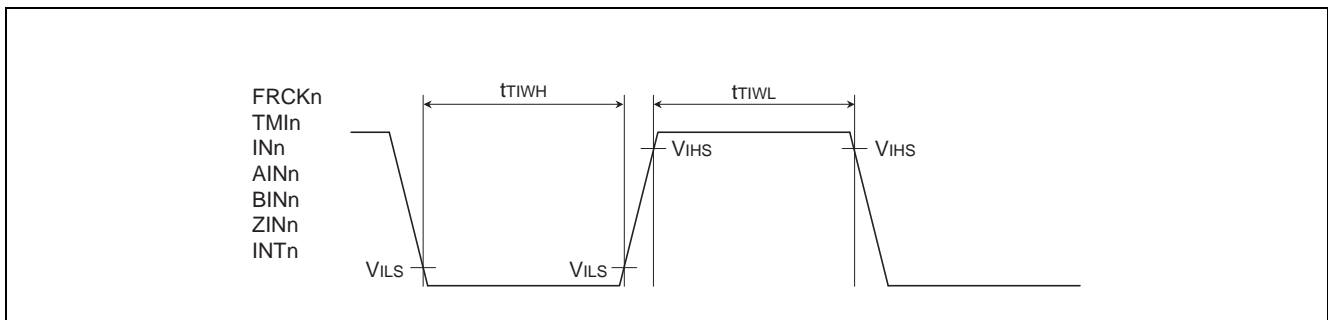
(12) Free-run Timer Clock, Reload Timer Event Input, Up/down Counter Input, Input Capture Input, Interrupt Input Timing

($V_{CC} = AV_{CC} = 2.7\text{ V to }3.6\text{ V}$, $V_{DDI} = 1.65\text{ V to }1.95\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condi- tions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH} t_{TIWL}	FRCKn TMIn INn AINn BINn ZINn	—	$2 t_{CYCP}$	—	ns	*1
		INTn	—	$3 t_{CYCP}$	—	ns	*1
			—	1.0	—	μs	*2

*1 : t_{CYCP} indicates peripheral clock cycle time, except when in stop mode, in main timer mode and in watch mode.

*2 : When in stop mode, in main timer mode, or in watch mode.

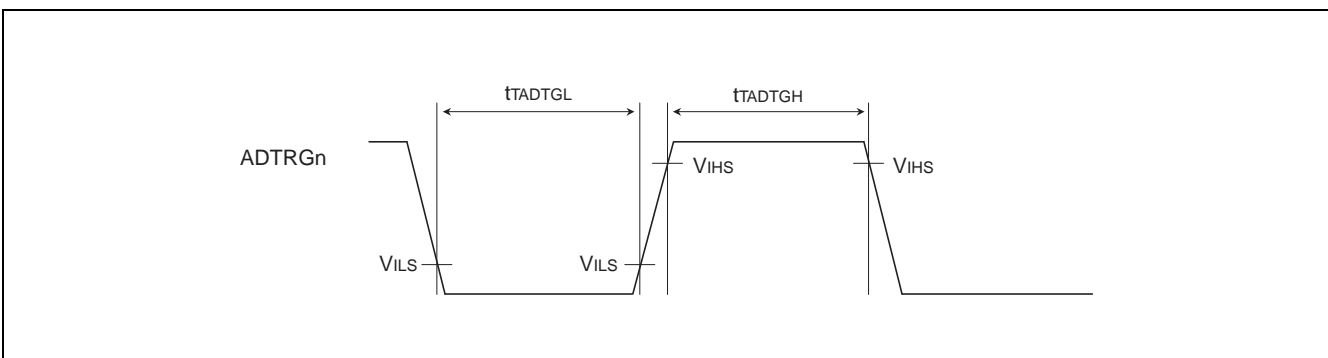


(13) A/D Converter Trigger Input Timing

($V_{CC} = AV_{CC} = 2.7\text{ V to }3.6\text{ V}$, $V_{DDI} = 1.65\text{ V to }1.95\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condi- tions	Value		Unit	Remarks
				Min	Max		
A/D converter trigger input	t_{TADTGL} t_{TADTGH}	ADTRGn	—	$2 t_{CYCP}$	—	ns	*

* : t_{CYCP} indicates peripheral clock cycle time.



(14) I²C Timing

(V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{DDI} = 1.65 V to 1.95 V, V_{SS} = AV_{SS} = 0 V, Ta = -40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Typical mode		High-speed mode		Unit
				Min	Max	Min	Max	
SCL clock frequency	f _{SCL}	SCKn (SCLn)	C _L = 50 pF R = (V _p /I _{oL})* ¹	0	100	0	400	kHz
“(Repeated) START condition” hold time SDA ↓ → SCL ↓	t _{HDSTA}	SOUTn (SDAn) SCKn (SCLn)		4.0	—	0.6	—	μs
SCL clock “L” width	t _{LOW}	SCKn (SCLn)		4.7	—	1.3	—	μs
SCL clock “H” width	t _{HIGH}	SCKn (SCLn)		4.0	—	0.6	—	μs
“(Repeated START condition)” setup time SCL ↑ → SDA ↓	t _{SUSTA}	SCKn (SCLn)		4.7	—	0.6	—	μs
Data hold time SCL ↓ → SDA ↓ ↑	t _{HDDAT}	SOUTn (SDAn) SCKn (SCLn)		0	3.45* ²	0	0.9* ³	μs
Data setup time SDA ↓ ↑ → SCL ↑	t _{SUDAT}	SOUTn (SDAn) SCKn (SCLn)		250	—	100	—	ns
“(STOP condition)” setup time SCL ↑ → SDA ↑	t _{SUSTO}	SOUTn (SDAn) SCKn (SCLn)		4.0	—	0.6	—	μs
Bus free time between “STOP condition” and “START condition”	t _{BUF}	—		4.7	—	1.3	—	μs
Noise filter	t _{SP}	—	—	2t _{cyCP} * ⁴	—	2t _{cyCP} * ⁴	—	ns

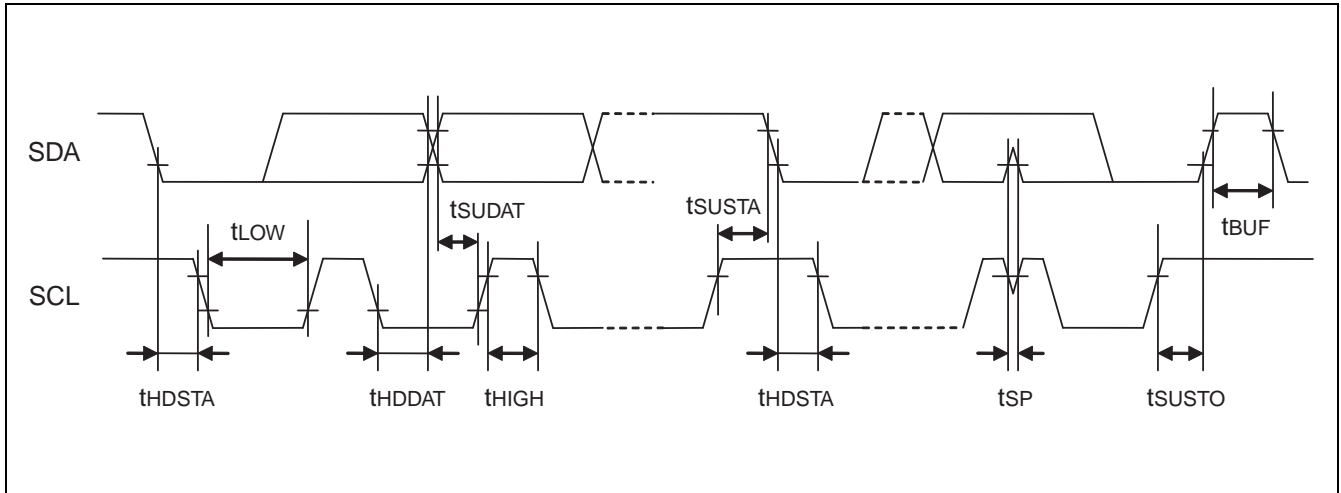
*1 : R and C represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. V_p indicates the power supply voltage of the pull-up resistance and I_{oL} indicates V_{oL} guaranteed current.

*2 : The maximum t_{HDDAT} must satisfy that it doesn't extend at least “L” period (t_{LOW}) of device's SCL signal.

*3 : A high-speed mode I²C bus device can be used on a standard mode I²C bus system as long as the device satisfies the requirement of “t_{SUDAT} ≥ 250 ns”.

*4 : t_{cyCP} is the peripheral clock cycle time. To use I²C, set the peripheral bus clock at 8 MHz or more.

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5. Electrical Characteristics for the A/D Converter

($V_{CC} = AV_{CC} = 2.7\text{ V to }3.6\text{ V}$, $V_{DDI} = 1.65\text{ V to }1.95\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$)

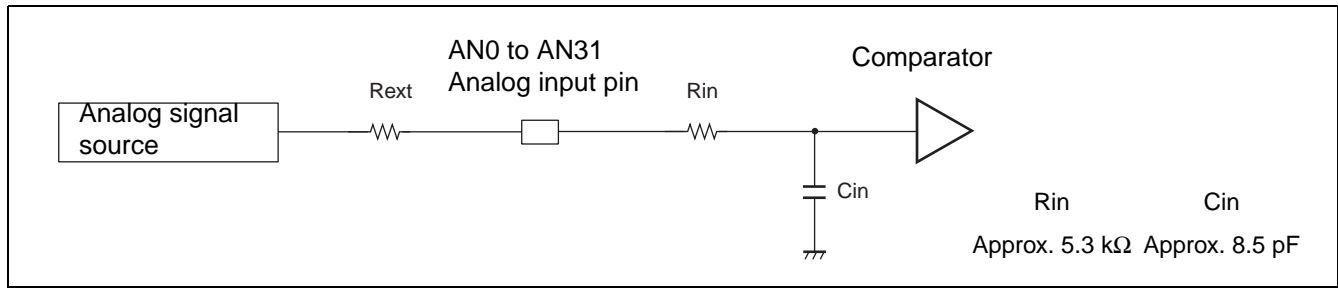
Parameter	Pin name	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	10	bit	
Total error	—	- 5.0	—	+ 5.0	LSB	AV _{CC} = 3.3 V, AV _{RH} = 3.3 V
Linearity error	—	- 3.5	—	+ 3.5	LSB	
Differential linearity error	—	- 3	—	+ 3	LSB	
Zero transition voltage	AN0 to AN31	- 1.5	+ 0.5	+ 4	LSB	
Full transition voltage	AN0 to AN31	AV _{RH} - 4	AV _{RH} - 1.5	AV _{RH} + 0.5	LSB	
Compare time	—	0.72* ³	—	—	μs	PCLK = 33 MHz
Conversion time	—	1.2* ¹	—	—	μs	PCLK = 33 MHz
Power supply current (analog + digital)	AV _{CC}	—	—	7	mA	When operating 2 A/D units (with D/A stopped)
		—	—	11	μA	At power-down* ²
Reference power supply current (between AV _{RH} and AV _{SS})	AV _{RH}	—	—	1.2	mA	When operating 2 A/D units AV _{RH} = 3.0 V
		—	—	5	μA	At power-down* ²
Analog input capacitance	—	—	—	8.5	pF	
Interchannel disparity	—	—	—	4	LSB	
Analog port input current	AN0 to AN31	—	—	10	μA	
Analog input voltage	AN0 to AN31	AV _{SS}	—	AV _{RH}	V	
Reference voltage	AV _{RH}	AV _{SS}	—	AV _{CC}	V	

*1 : It depends on the actual external load and the clock cycle supplied to peripheral resources. Make sure to satisfy PCLK cycle × 4 or over + below (Equation 1). The condition of minimum conversion time is the value when PCLK = 33 MHz, sampling time: 0.424 μs, external impedance: 1.4k Ω or below, compare time: 0.72 μs.

*2 : The current when the CPU is in stop mode and the A/D converter is not operating.

*3 : Compare time = {(CT + 1) × 10 + 4} × peripheral clock (PCLK) period. (CT indicates compare time setting bits.)
The condition of the minimum compare time is when CT = 1 and PCLK = 33 MHz.

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The output impedance of the external circuit connected to the analog input affects the sampling time of the A/D converter. Design the output impedance of the output circuit such that the required sampling time is less than the value of T_s calculated from the following equation.

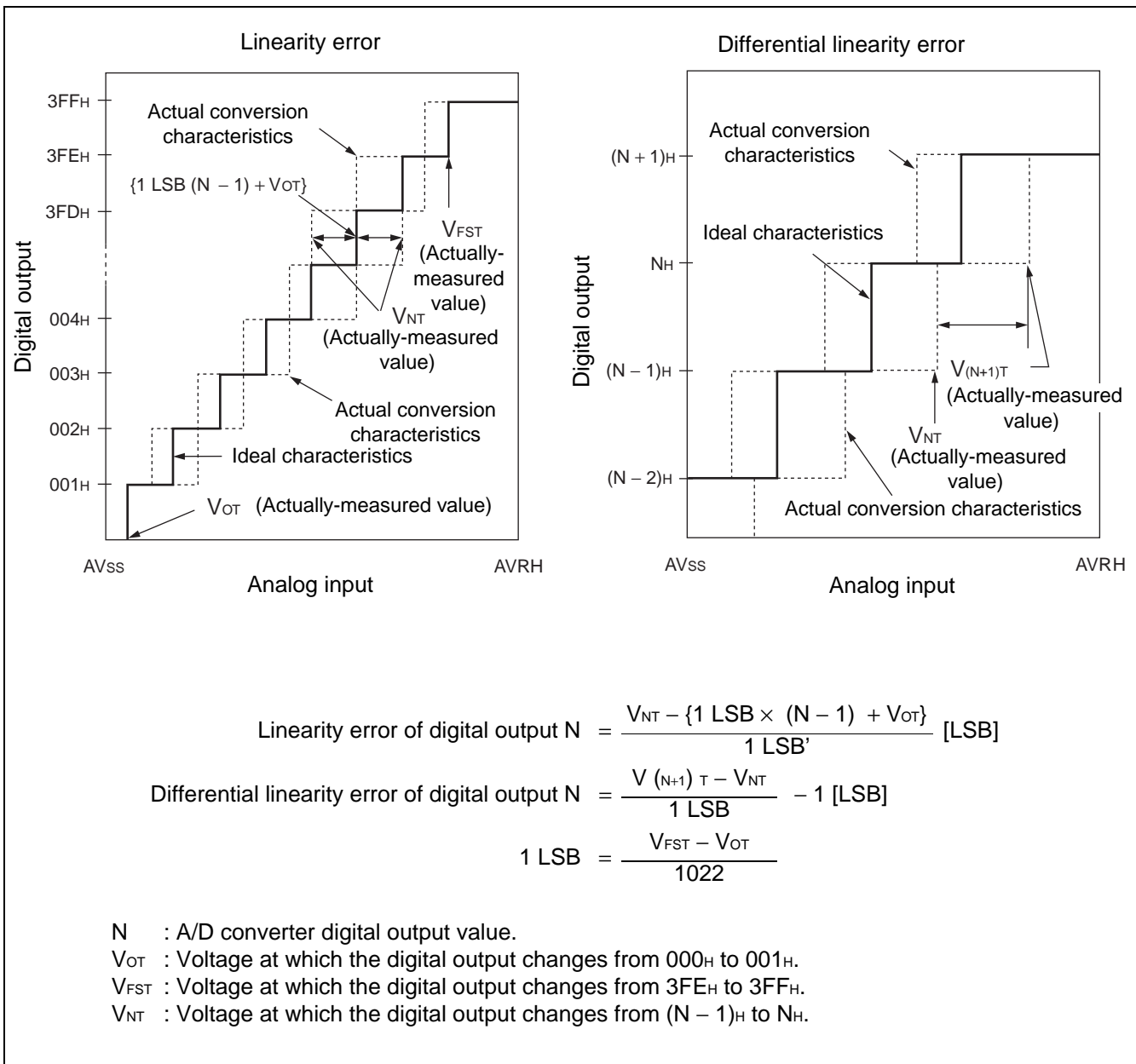
(Equation1) $T_s = (R_{in} + R_{ext}) \times C_{in} \times 8$
 T_s : Sampling time
 R_{in} : Input resistance of A/D = 5.3 kΩ
 C_{in} : Input capacitance of A/D = 8.5 pF
 R_{ext} : Output impedance of external circuit

If the sampling time is set as 600 ns,
 $600 \text{ ns} \geq (5.3 \text{ k}\Omega + R_{ext}) \times 8.5 \text{ pF} \times 8$
 $\therefore R_{ext} \leq 3.5 \text{ k}\Omega$

And the impedance of the external circuit therefore needs to be 3.5 kΩ or less.

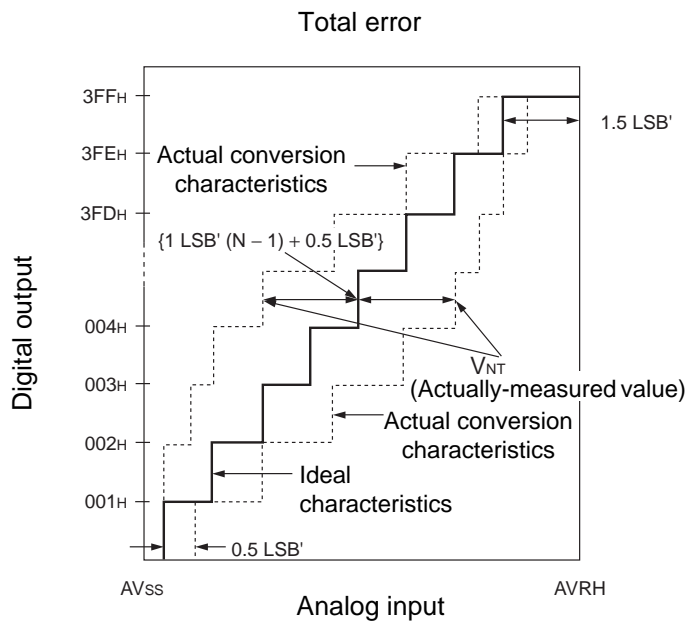
Definition of 10-bit A/D Converter Terms

- Resolution : Analog variation that is recognized by an A/D converter.
- Linearity error : Deviation of the line between the zero-transition point (000000000←→000000001) and the full-scale transition point (111111110←→111111111) from the actual conversion characteristics.
- Differential linearity error : Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.
- Total error : Difference between the actual value and the theoretical value. The total error includes zero transition error, full-scale transition error, and linear error.



(Continued)

(Continued)



$$1 \text{ LSB}' (\text{Ideal value}) = \frac{AVRH - AV_{SS}}{1024} [\text{V}]$$

$$\text{Total error of digital output } N = \frac{V_{NT} - \{1 \text{ LSB}' \times (N - 1) + 0.5 \text{ LSB}'\}}{1 \text{ LSB}'}$$

N : A/D converter digital output value.

V_{NT} : Voltage at which the digital output changes from $(N + 1)_H$ to N_H .

V_{OT}' (Ideal value) = $AV_{SS} + 0.5 \text{ LSB}'$ [V]

V_{FST}' (Ideal value) = $AVRH - 1.5 \text{ LSB}'$ [V]

6. Electrical Characteristics for the D/A Converter

($V_{CC} = AV_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$, $V_{DDI} = 1.65 \text{ V to } 1.95 \text{ V}$, $V_{SS} = AV_{SS} = 0 \text{ V}$, $T_a = -40 \text{ }^\circ\text{C to } +85 \text{ }^\circ\text{C}$)

Parameter	Pin name	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	8	bit	
Linearity error	—	-2.0	—	+2.0	LSB	When the output is unloaded
Differential linearity error	—	-1.0	—	+1.0	LSB	When the output is unloaded
Conversion time	—	—	0.6	—	μs	When load capacitance (C_L) = 20 pF
	—	—	3.0	—	μs	When load capacitance (C_L) = 100 pF
Analog output impedance	DA0 to DA2	3.19	3.51	5.85	k Ω	
Analog current	AV_{CC}	—	450	—	μA	10 μs conversion, when the output is unloaded (When 3 channels operating, A/D stopped)
		—	—	3600*	μA	When the input digital code is fixed at 7A _H or 85 _H (When 3 channels operating, A/D stopped)
		—	—	11	μA	At power-down (When A/D stopped)

* : The current consumption of the D/A converter varies with input digital code. The standard value indicates the current consumed when the digital code that maximizes the current consumption is input.

MB91645A Series

7. Flash Memory Write/Erase Characteristics

($V_{CC} = 3.3\text{ V}$, $V_{DDI} = 1.8\text{ V}$, $T_a = +25\text{ }^\circ\text{C}$)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	—	0.5	2.0	s	Excludes write time prior to internal erase
Half word (16 bit) write time	—	6	100	μs	Not including system-level overhead time.
Chip erase time*1	—	8	32	s	Excludes write time prior to internal erase
Erase/write cycles	10000	—	—	cycle	Average $T_a \leq +85\text{ }^\circ\text{C}$
Flash memory data hold time	10^{*2}	—	—	year	Average $T_a \leq +85\text{ }^\circ\text{C}$

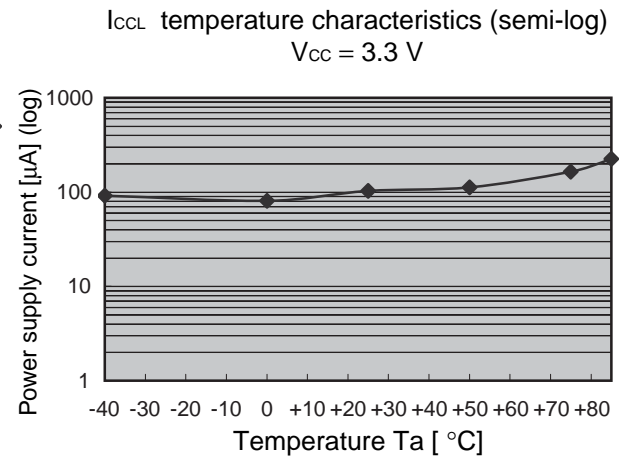
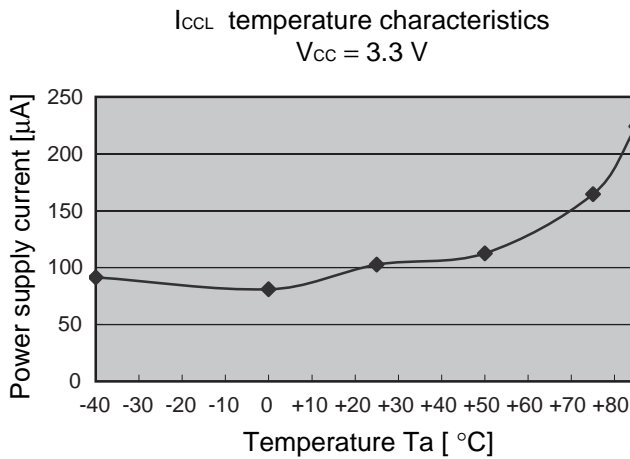
*1: The chip erase time is the sector erase time multiplied across all sectors.

*2: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at $+85\text{ }^\circ\text{C}$).

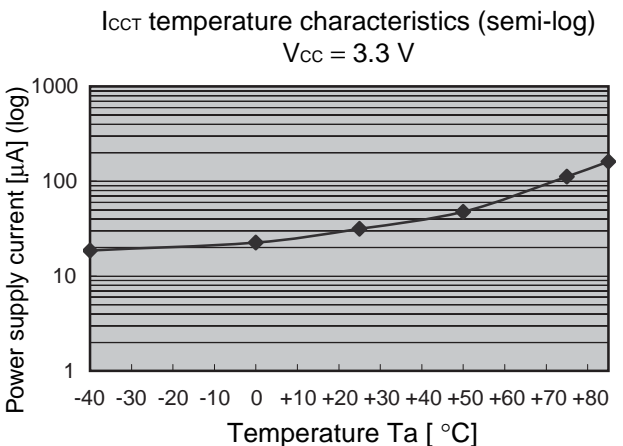
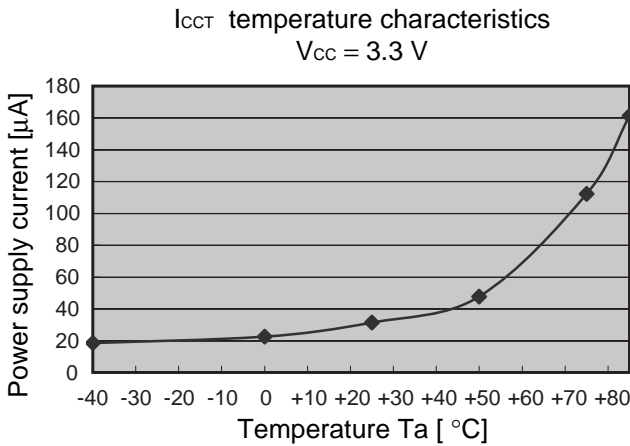
CHARACTERISTICS

- Characteristics of MB91F647A

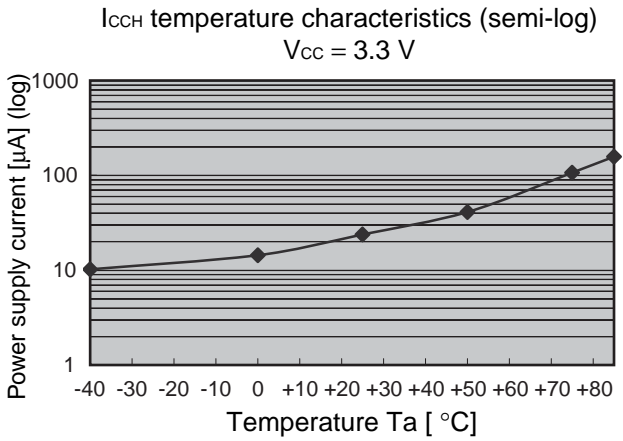
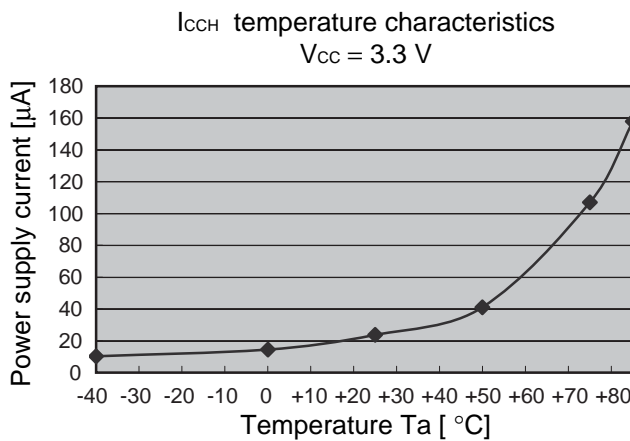
Power supply current (sub operation)



Power supply current (watch mode)



Power supply current (stop mode)

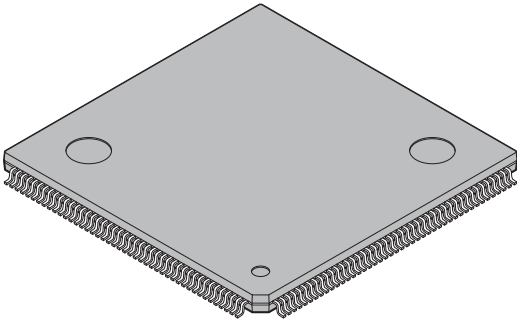


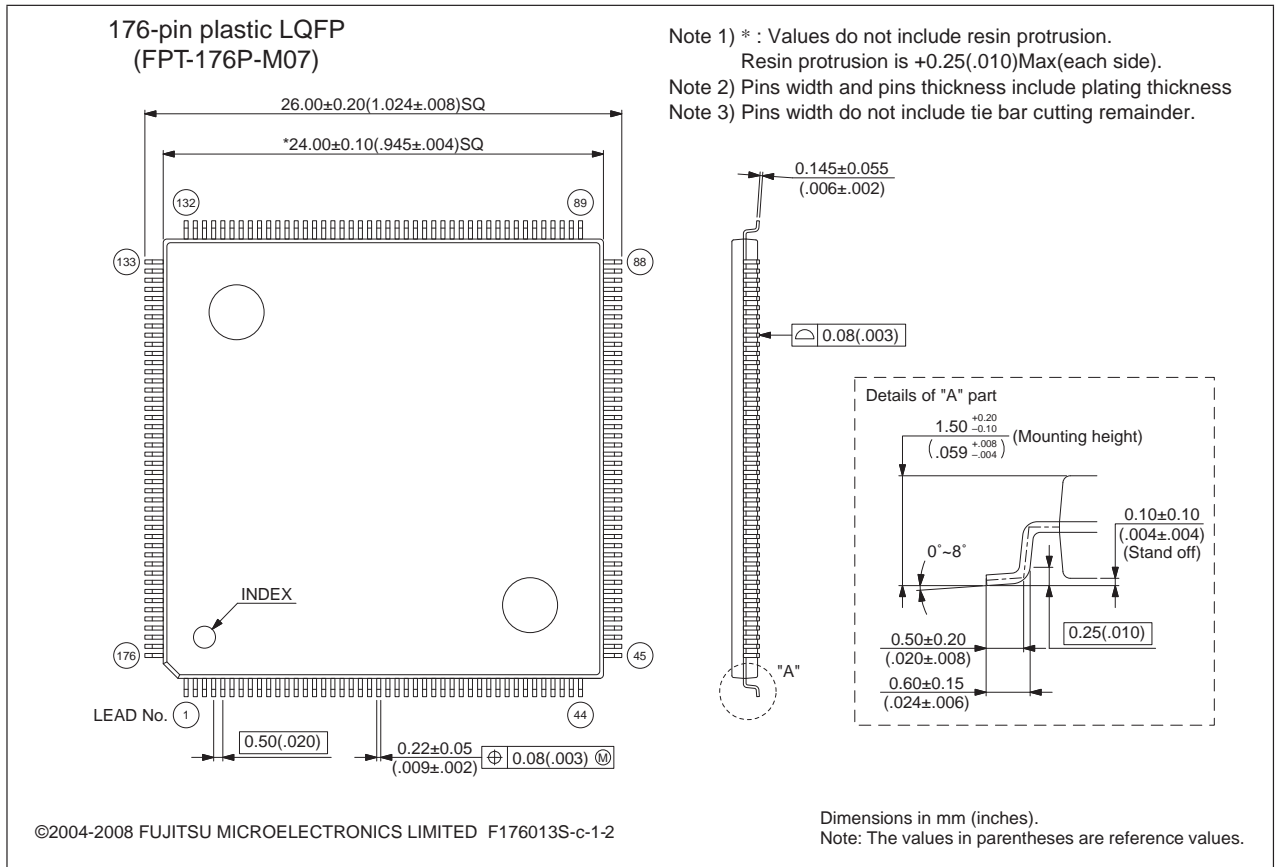
MB91645A Series

■ ORDERING INFORMATION

Part number	Package
MB91F647APMC	176-pin plastic LQFP (FPT-176P-M07)
MB91F647ABGL	176-pin plastic PFBGA (BGA-176P-M04)

PACKAGE DIMENSION

<p>176-pin plastic LQFP</p>  <p>(FPT-176P-M07)</p>	Lead pitch	0.50 mm
	Package width × package length	24.0 × 24.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Code (Reference)	P-LQFP-0176-2424-0.50

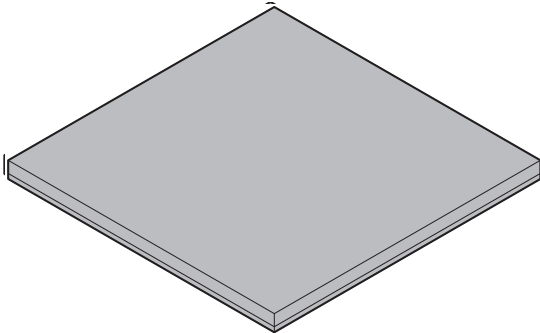


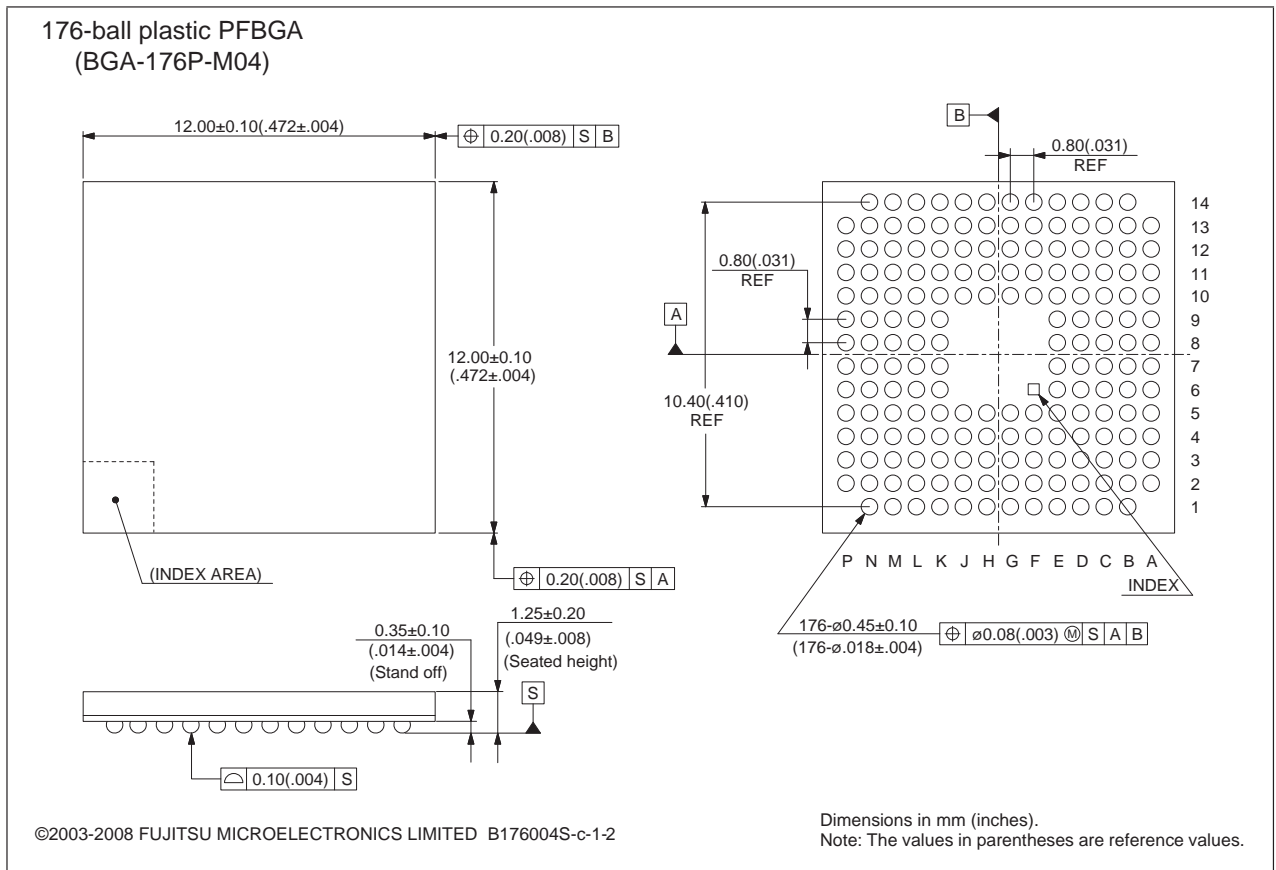
Please confirm the latest Package dimension by following URL.
<http://edevic.fujitsu.com/package/en-search/>

(Continued)

MB91645A Series

(Continued)

<p>176-ball plastic PFBGA</p>  <p>(BGA-176P-M04)</p>	Ball pitch	0.80 mm
	Package width × package length	12.00 × 12.00 mm
	Lead shape	Soldering ball
	Sealing method	Plastic mold
	Ball size	∅0.45 mm
	Mounting height	1.45 mm Max.
	Weight	0.32 g



Please confirm the latest Package dimension by following URL.
<http://edevic.fujitsu.com/package/en-search/>

MEMO

MB91645A Series

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