

## 32-bit Microcontrollers

CMOS

# FR80 MB91625 Series

## MB91627/F627/F625/V650

### ■ DESCRIPTION

The MB91625 series is a line of FUJITSU SEMICONDUCTOR microcontrollers based on a 32-bit RISC CPU core that feature a variety of peripheral functions for embedded applications that demand high-performance and high-speed CPU processing.

This series is based on the FR80\* family CPU and is implemented as a single chip.

\* : FR, the abbreviation of FUJITSU RISC controller, is a line of products of Fujitsu Semiconductor Limited.

### ■ FEATURES

- FR80 CPU
  - 32-bit RISC, load/store architecture, five-stage pipeline
  - General-purpose registers : 32-bit × 16
  - 16-bit fixed-length instructions (basic instructions) : 1 instruction per cycle
  - Instructions suitable for embedded applications
    - Memory-to-memory transfer, bit processing, barrel shift instructions, etc.
    - Instruction support for high level languages
      - Function entry and exit instructions, instructions for register multi-load and multi-store
    - Bit search instruction
      - "1" detection, "0" detection, transition point detection
    - Branch instructions with delay slots
      - Reduced overhead when processing branches
    - Register interlock functions
      - Facilitate coding in assembly language
    - Built-in multiplier/instruction-level support
      - Signed 32-bit multiplication : 5 cycles
      - Signed 16-bit multiplication : 3 cycles
    - Interrupts (save PC and PS) : 6 cycles, 16 priority levels
    - Harvard architecture allowing program access and data access to be executed simultaneously
    - Instruction prefetch function has been added with 4 word instruction queue of CPU

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For the information for microcontroller supports, see the following web site.

This web site includes the "**Customer Design Review Supplement**" which provides the latest cautions on system development and the minimal requirements to be checked to prevent problems before the system development.

<http://edevice.fujitsu.com/micom/en-support/>

# MB91625 Series

- Instruction compatible with FR family CPU
  - Additional bit search instructions
  - No resource instructions and coprocessor instructions
- Maximum operating frequency
  - CPU : 60 MHz
  - Resources : 40 MHz
- DMA controller (DMAC)
  - 8 channels
  - Address space : 32 bits (4 Gbytes)
  - Transfer modes : Block transfer/burst transfer/demand transfer
  - Address update : Increment/decrement/fixed (increment/decrement step size of 1, 2, or 4)
  - Transfer data length : Selectable from 8-bit, 16-bit, 32-bit
  - Block size : 1 to 16
  - Number of transfers : 1 to 65535
  - Transfer requests
    - Requests from software
    - Interrupt requests from peripheral resources (interrupt requests are shared, including external interrupts)
  - Reload functions : Reload can be specified on all channels
  - Priority order : Fixed (ch.0 > ch.1 > ch.2 > ch.3 > ...) or round-robin
  - Interrupt requests : Interrupts can be generated for transfer complete, transfer error, and transfer interrupted.
- Multifunction serial interface
  - 4 channels with 16-byte FIFO, 8 channels without FIFO
  - Operation mode is selectable from the followings for each channel (For ch.0, I<sup>2</sup>C is not available.)
    - UART
      - Full-duplex double buffer
      - Selectable parity on/off
      - Built-in dedicated baud rate generator
      - External clock can be used as a serial clock
      - Error detection function for parity, frame and overrun errors
    - CSIO
      - Full-duplex double buffer
      - Built-in dedicated baud rate generator
      - Overrun error detection function
    - I<sup>2</sup>C
      - Supports both standard mode (Max 100 kbps) and Fast mode (Max 400 kbps)
      - Some channels are 5 V tolerant
- Interrupts
  - Total of 32 external interrupts (some pins are 5 V tolerant)
  - Interrupts from peripheral resources
  - Programmable interrupt levels (16 levels)
  - Can be used to return from stop mode, sleep mode

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- A/D converter
  - 16 channels, 1 unit
  - 10-bit resolution
  - Conversion time : approx. 1.2  $\mu$ s (PCLK = 33 MHz)
  - Priority conversion (2 levels)
  - Conversion modes : Single-shot conversion mode, scan conversion mode
  - Activation sources : Software, external trigger, base timer
  - Built-in FIFO for storing conversion data (for scan conversion:16, for priority conversion:4)
- D/A converter
  - 2 channels
  - 8-bit resolution
- Base timer
  - 16 channels
  - Operation mode is selectable from the followings for each channel
    - 16/32-bit reload timer
    - 16-bit PWM timer
    - 16/32-bit PWC timer
    - 16-bit PPG timer
  - Cascading connection between 2 channels allows them to be used as one 32-bit timer
  - Multiple channels can be started simultaneously
  - Input/output select function
- 16-bit reload timer
  - 3 channels (including 1 channel for REALOS)
  - Interval timer function
  - Count clock select function (peripheral clock (PCLK) divided by 2 to 64)
- Compare timer
  - 32-bit input capture : 8 channels
  - 32-bit output compare : 8 channels
  - 32-bit free-run timer : 2 channels
- Other interval timers
  - Up/down counter : 4 channels
  - Watch counter : 1 channel
  - Watchdog timer : 1 channel
- Main timer
  - 1 channel
  - Counts the oscillation stabilization wait time of the main clock (MCLK)
  - Counts the oscillation stabilization wait time of the PLL clock (PLLCLK)
  - Can be used as an interval timer while the main clock (MCLK) oscillations is stable
- Sub timer
  - 1 channel
  - Counts the oscillation stabilization wait time of the sub clock (SBCLK)
  - Can be used as an interval timer while the sub clock (SBCLK) oscillations is stable

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# MB91625 Series

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- Clock generation
  - Main clock (MCLK) oscillator
  - Sub clock (SBCLK) oscillator
  - PLL clock (PLLCLK) oscillator
- Low-power dissipation mode
  - Stop mode
  - Watch mode
  - Sleep mode
  - Doze mode
  - Clock division function
- Other features
  - I/O port
  - $\overline{\text{INIT}}$  pin is provided as a reset pin
  - Watchdog timer reset, software reset
  - Delay interrupt
  - Power supply : Single power supply (2.7 V to 3.6 V)

# MB91625 Series

## ■ PRODUCT LINEUP

Product Name Items	MB91V650	MB91F627	MB91627	MB91F625
Product type	Evaluation product	Flash memory product	MASK ROM product	Flash memory product
Built-in program memory size	— (Supports by emulation memory)	512 K bytes (Flash)	512 K bytes (ROM)	256 K bytes (Flash)
Built-in RAM capacity	128 K bytes	48 K bytes		32 K bytes
External bus interface	Supported	Not supported		
DMA controller (DMAC)	8 channels			
Base timer	16 channels			
Multifunction serial interface	without FIFO: 8 channels (ch.0 to ch.7) with FIFO: 4 channels (ch.8 to ch.11)			
External interrupt	32 (Some pins support 5V tolerant)			
10-bit A/D converter	32 channels, 2 units	16 channels, 1 unit		
8-bit D/A converter	3 channels	2 channels		
16-bit reload timer	3 channels			
32-bit input capture	8 channels			
32-bit output compare	8 channels			
32-bit free-run timer	2 channels			
Up/down counter	4 channels			
Watch counter	1 channel			
I/O port	154	86		
Main timer	1 channel			
Sub timer	1 channel			
Wild register	16 channels			
Debug function	DSU4	—		

## ■ PACKAGES

Product name Package	MB91F627	MB91627	MB91F625
FPT-100P-M20	○	○	○

○ : Supported

Note: Refer to “■ PACKAGE DIMENSION” for detailed information on each package.



## ■ PIN DESCRIPTION

The number after the underscore (“\_”) in pin names such as XXX\_1 and XXX\_2 indicates the port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin no.	Pin name	I/O circuit type*1	Function	CMOS level input	CMOS level hysteresis input
LQFP-100					
1	V <sub>SS</sub>	—	GND pin	—	—
2	C	—	Power stabilization capacity pin	—	—
3	P27	D*2	General-purpose I/O port	—	○
	TIOB11		Base timer ch.11 TIOB pin	—	○
	OUT3		32-bit output compare ch.3 output pin	—	—
4	P30	D*2	General-purpose I/O port	—	○
	TIOA12		Base timer ch.12 TIOA pin	—	—
	SOUT6 (SDA6)		Multifunction serial interface ch.6 output pin. This pin operates as SOUT6 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA6 when it is used in an I <sup>2</sup> C (operation mode 4).	—	○
	INT8		External interrupt request 8 input pin	—	○
5	P31	D*2	General-purpose I/O port	—	○
	TIOB12		Base timer ch.12 TIOB pin	—	○
	SIN6		Multifunction serial interface ch.6 input pin	—	○
	INT9		External interrupt request 9 input pin	—	○
6	P32	D*2	General-purpose I/O port	—	○
	TIOA13		Base timer ch.13 TIOA pin	—	○
	SCK6 (SCL6)		Multifunction serial interface ch.6 clock I/O pin. This pin operates as SCK6 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL6 when it is used in an I <sup>2</sup> C (operation mode 4).	—	○
	INT10		External interrupt request 10 input pin	—	○
7	P33	D*2	General-purpose I/O port	—	○
	TIOB13		Base timer ch.13 TIOB pin	—	○
	INT11		External interrupt request 11 input pin	—	○

(Continued)

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Pin no.	Pin name	I/O circuit type*1	Function	CMOS level input	CMOS level hysteresis input
LQFP-100					
8	P34	D*2	General-purpose I/O port	—	○
	TIOA14		Base timer ch.14 TIOA pin	—	—
	SOUT7 (SDA7)		Multifunction serial interface ch.7 output pin. This pin operates as SOUT7 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA7 when it is used in an I <sup>2</sup> C (operation mode 4).	—	○
	OUT4		32-bit output compare ch.4 output pin	—	—
	INT12		External interrupt request 12 input pin	—	○
9	P35	D*2	General-purpose I/O port	—	○
	TIOB14		Base timer ch.14 TIOB pin	—	○
	SIN7		Multifunction serial interface ch.7 input pin	—	○
	OUT5		32-bit output compare ch.5 output pin	—	—
	INT13		External interrupt request 13 input pin	—	○
10	P36	D*2	General-purpose I/O port	—	○
	TIOA15		Base timer ch.15 TIOA pin	—	○
	SCK7 (SCL7)		Multifunction serial interface ch.7 clock I/O pin. This pin operates as SCK7 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL7 when it is used in an I <sup>2</sup> C (operation mode 4).	—	○
	OUT6		32-bit output compare ch.6 output pin	—	—
	INT14		External interrupt request 14 input pin	—	○
11	P37	D*2	General-purpose I/O port	—	○
	TIOB15		Base timer ch.15 TIOB pin	—	○
	OUT7		32-bit output compare ch.7 output pin	—	—
	INT15		External interrupt request 15 input pin	—	○
12	P40	D*2	General-purpose I/O port	—	○
	SOUT8 (SDA8)		Multifunction serial interface ch.8 output pin. This pin operates as SOUT8 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA8 when it is used in an I <sup>2</sup> C (operation mode 4).	—	○

(Continued)

Pin no.	Pin name	I/O circuit type*1	Function	CMOS level input	CMOS level hysteresis input
LQFP-100					
13	P41	D*2	General-purpose I/O port	—	○
	SIN8		Multifunction serial interface ch.8 input pin	—	○
14	P42	D*2	General-purpose I/O port	—	○
	SCK8 (SCL8)		Multifunction serial interface ch.8 clock I/O pin. This pin operates as SCK8 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL8 when it is used in an I <sup>2</sup> C (operation mode 4).	—	○
15	P43	D*2	General-purpose I/O port	—	○
16	P44	D*2	General-purpose I/O port	—	○
	SOUT9 (SDA9)		Multifunction serial interface ch.9 output pin. This pin operates as SOUT9 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA9 when it is used in an I <sup>2</sup> C (operation mode 4).	—	○
17	P45	D*2	General-purpose I/O port	—	○
	SIN9		Multifunction serial interface ch.9 input pin	—	○
18	P46	D*2	General-purpose I/O port	—	○
	SCK9 (SCL9)		Multifunction serial interface ch.9 clock I/O pin. This pin operates as SCK9 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL9 when it is used in an I <sup>2</sup> C (operation mode 4).	—	○
19	P47	D*2	General-purpose I/O port	—	○
20	$\overline{\text{INIT}}$	H, P	External reset input pin. A reset is valid when $\overline{\text{INIT}} = \text{L}$ . The I/O circuit type for the Flash memory products is P.	—	○
21	MD0	H, P	Mode 0 pin. The I/O circuit type for the Flash memory products is P. During normal operation, MD0 = L must be input. During serial programming to Flash memory, MD0 = H must be input.	—	○
22	MD1	H, P	Mode 1 pin. Input must always be at the "L" level. The I/O circuit type for the Flash memory products is P.	—	○
23	X0	A	Main clock (oscillation) input pin	—	○
24	X1	A	Main clock (oscillation) I/O pin	—	—
25	V <sub>SS</sub>	—	GND pin	—	—

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Pin no.	Pin name	I/O circuit type*1	Function	CMOS level input	CMOS level hysteresis input
LQFP-100					
26	PK0	I	General-purpose I/O port	—	○
	X1A		Sub clock (oscillation) I/O pin	—	—
27	PK1	I	General-purpose I/O port	—	○
	X0A		Sub clock (oscillation) input pin	—	○
28	PK2	C	General-purpose I/O port	—	○
	ADTRG0_2		10-bit A/D converter external trigger input pin (Port 2)	—	○
29	P70	E	General-purpose I/O port	—	○
	AN0		10-bit A/D converter ch.0 analog input pin	—	—
	OUT0_1		32-bit output compare ch.0 output pin (Port 1)	—	—
	INT16		External interrupt request 16 input pin	—	○
30	P71	E	General-purpose I/O port	—	○
	AN1		10-bit A/D converter ch.1 analog input pin	—	—
	OUT1_1		32-bit output compare ch.1 output pin (Port 1)	—	—
	INT17		External interrupt request 17 input pin	—	○
31	P72	E	General-purpose I/O port	—	○
	AN2		10-bit A/D converter ch.2 analog input pin	—	—
	TMO0		16-bit reload timer ch.0 output pin	—	—
	OUT2_1		32-bit output compare ch.2 output pin (Port 1)	—	—
	INT18		External interrupt request 18 input pin	—	○
32	P73	E	General-purpose I/O port	—	○
	AN3		10-bit A/D converter ch.3 analog input pin	—	—
	TMO1		16-bit reload timer ch.1 output pin	—	—
	OUT3_1		32-bit output compare ch.3 output pin (Port 1)	—	—
	INT19		External interrupt request 19 input pin	—	○
33	P74	E	General-purpose I/O port	—	○
	AN4		10-bit A/D converter ch.4 analog input pin	—	—
	TMO2		16-bit reload timer ch.2 output pin	—	—
	OUT4_1		32-bit output compare ch.4 output pin (Port 1)	—	—
	INT20		External interrupt request 20 input pin	—	○

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Pin no.	Pin name	I/O circuit type*1	Function	CMOS level input	CMOS level hysteresis input
LQFP-100					
34	P75	E	General-purpose I/O port	—	○
	AN5		10-bit A/D converter ch.5 analog input pin	—	—
	SOUT0		Multifunction serial interface ch.0 output pin. This pin operates as SOUT0 when it is used in a UART/CSIO (operation modes 0 to 2).	—	—
	TMI0		16-bit reload timer ch.0 input pin	—	○
	OUT5_1		32-bit output compare ch.5 output pin (Port 1)	—	—
	INT21		External interrupt request 21 input pin	—	○
35	P76	E	General-purpose I/O port	—	○
	AN6		10-bit A/D converter ch.6 analog input pin	—	—
	SIN0		Multifunction serial interface ch.0 input pin	—	○
	TMI1		16-bit reload timer ch.1 input pin	—	○
	OUT6_1		32-bit output compare ch.6 output pin (Port 1)	—	—
	INT22		External interrupt request 22 input pin	—	○
36	P77	E	General-purpose I/O port	—	○
	AN7		10-bit A/D converter ch.7 analog input pin	—	—
	SCK0		Multifunction serial interface ch.0 clock I/O pin. This pin operates as SCK0 when it is used in a UART/CSIO (operation modes 0 to 2).	—	○
	TMI2		16-bit reload timer ch.2 input pin	—	○
	OUT7_1		32-bit output compare ch.7 output pin (Port 1)	—	—
	INT23		External interrupt request 23 input pin	—	○
37	P80	E	General-purpose I/O port	—	○
	AN8		10-bit A/D converter ch.8 analog input pin	—	—
	INO_1		32-bit input capture ch.0 input pin (Port 1)	—	○
	INT24		External interrupt request 24 input pin	—	○

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# MB91625 Series

Pin no.	Pin name	I/O circuit type*1	Function	CMOS level input	CMOS level hysteresis input
LQFP-100					
38	P81	E	General-purpose I/O port	—	○
	AN9		10-bit A/D converter ch.9 analog input pin	—	—
	IN1_1		32-bit input capture ch.1 input pin (Port 1)	—	○
	INT25		External interrupt request 25 input pin	—	○
39	P82	E	General-purpose I/O port	—	○
	AN10		10-bit A/D converter ch.10 analog input pin	—	—
	IN2_1		32-bit input capture ch.2 input pin (Port 1)	—	○
	INT26		External interrupt request 26 input pin	—	○
40	P83	E	General-purpose I/O port	—	○
	AN11		10-bit A/D converter ch.11 analog input pin	—	—
	IN3_1		32-bit input capture ch.3 input pin (Port 1)	—	○
	INT27		External interrupt request 27 input pin	—	○
41	P84	E	General-purpose I/O port	—	○
	AN12		10-bit A/D converter ch.12 analog input pin	—	—
	IN4_1		32-bit input capture ch.4 input pin (Port 1)	—	○
	INT28		External interrupt request 28 input pin	—	○
42	P85	E	General-purpose I/O port	—	○
	AN13		10-bit A/D converter ch.13 analog input pin	—	—
	IN5_1		32-bit input capture ch.5 input pin (Port 1)	—	○
	INT29		External interrupt request 29 input pin	—	○
43	P86	E	General-purpose I/O port	—	○
	AN14		10-bit A/D converter ch.14 analog input pin	—	—
	IN6_1		32-bit input capture ch.6 input pin (Port 1)	—	○
	INT30		External interrupt request 30 input pin	—	○
44	P87	E	General-purpose I/O port	—	○
	AN15		10-bit A/D converter ch.15 analog input pin	—	—
	IN7_1		32-bit input capture ch.7 input pin (Port 1)	—	○
	INT31		External interrupt request 31 input pin	—	○
45	AV <sub>CC</sub>	—	10-bit A/D converter and 8-bit D/A converter analog power pin	—	—
46	AVRH	—	10-bit A/D converter analog reference voltage input pin	—	—
47	AV <sub>SS</sub>	—	10-bit A/D converter and 8-bit D/A converter GND pin	—	—

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# MB91625 Series

Pin no.	Pin name	I/O circuit type*1	Function	CMOS level input	CMOS level hysteresis input
LQFP-100					
48	P90	F	General-purpose I/O port	—	○
	DA0		8-bit D/A converter ch.0 analog output pin	—	—
49	P91	F	General-purpose I/O port	—	○
	DA1		8-bit D/A converter ch.1 analog output pin	—	—
50	V <sub>SS</sub>	—	GND pin	—	—
51	V <sub>CC</sub>	—	Power pin	—	—
52	P92	C	General-purpose I/O port	—	○
53	PA0	C	General-purpose I/O port	—	○
	INT16_1		External interrupt request 16 input pin (Port 1)	—	○
54	PA1	C	General-purpose I/O port	—	○
	INT17_1		External interrupt request 17 input pin (Port 1)	—	○
55	PA2	C	General-purpose I/O port	—	○
	TMO0_1		16-bit reload timer ch.0 output pin (Port 1)	—	—
	INT18_1		External interrupt request 18 input pin (Port 1)	—	○
56	PA3	C	General-purpose I/O port	—	○
	TMO1_1		16-bit reload timer ch.1 output pin (Port 1)	—	—
	INT19_1		External interrupt request 19 input pin (Port 1)	—	○
57	PA4	C	General-purpose I/O port	—	○
	TMO2_1		16-bit reload timer ch.2 output pin (Port 1)	—	—
	INT20_1		External interrupt request 20 input pin (Port 1)	—	○
58	PA5	C	General-purpose I/O port	—	○
	TMI0_1		16-bit reload timer ch.0 input pin (Port 1)	—	○
	INT21_1		External interrupt request 21 input pin (Port 1)	—	○
59	PA6	C	General-purpose I/O port	—	○
	TMI1_1		16-bit reload timer ch.1 input pin (Port 1)	—	○
	INT22_1		External interrupt request 22 input pin (Port 1)	—	○
60	PA7	C	General-purpose I/O port	—	○
	TMI2_1		16-bit reload timer ch.2 input pin (Port 1)	—	○
	INT23_1		External interrupt request 23 input pin (Port 1)	—	○

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Pin no.	Pin name	I/O circuit type*1	Function	CMOS level input	CMOS level hysteresis input
LQFP-100					
61	P50	C	General-purpose I/O port	—	○
	SOUT10 (SDA10)		Multifunction serial interface ch.10 output pin. This pin operates as SOUT10 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA10 when it is used in an I <sup>2</sup> C (operation mode 4).	—	○
	AIN0_1		Up/Down counter ch.0 AIN input pin (Port 1)	—	○
62	P51	C	General-purpose I/O port	—	○
	SIN10		Multifunction serial interface ch.10 input pin	—	○
	BIN0_1		Up/Down counter ch.0 BIN input pin (Port 1)	—	○
63	P52	C	General-purpose I/O port	—	○
	SCK10 (SCL10)		Multifunction serial interface ch.10 clock I/O pin. This pin operates as SCK10 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL10 when it is used in an I <sup>2</sup> C (operation mode 4).	—	○
	ZIN0_1		Up/Down counter ch.0 ZIN input pin (Port 1)	—	○
64	P53	C	General-purpose I/O port	—	○
	FRCK1		32-bit free-run timer ch.1 external clock input pin	—	○
	INT21_2		External interrupt request 21 input pin (Port 2)	—	○
65	P54	C	General-purpose I/O port	—	○
	SOUT11 (SDA11)		Multifunction serial interface ch.11 output pin. This pin operates as SOUT11 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA11 when it is used in an I <sup>2</sup> C (operation mode 4).	—	○
	AIN1_1		Up/Down counter ch.1 AIN input pin (Port 1)	—	○
66	P55	C	General-purpose I/O port	—	○
	SIN11		Multifunction serial interface ch.11 input pin	—	○
	BIN1_1		Up/Down counter ch.1 BIN input pin (Port 1)	—	○
	ADTRG0		10-bit A/D converter external trigger input pin	—	○

(Continued)

# MB91625 Series

Pin no.	Pin name	I/O circuit type*1	Function	CMOS level input	CMOS level hysteresis input
LQFP-100					
67	P56	C	General-purpose I/O port	—	○
	SCK11 (SCL11)		Multifunction serial interface ch.11 clock I/O pin. This pin operates as SCK11 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL11 when it is used in an I <sup>2</sup> C (operation mode 4).	—	○
	ZIN1_1		Up/Down counter ch.1 ZIN input pin (Port 1)	—	○
	FRCK0		32-bit free-run timer ch.0 external clock input pin	—	○
68	P57	C	General-purpose I/O port	—	○
69	P60	C	General-purpose I/O port	—	○
	AIN2_1		Up/Down counter ch.2 AIN input pin (Port 1)	—	○
70	P61	C	General-purpose I/O port	—	○
	BIN2_1		Up/Down counter ch.2 BIN input pin (Port 1)	—	○
71	P62	C	General-purpose I/O port	—	○
	ZIN2_1		Up/Down counter ch.2 ZIN input pin (Port 1)	—	○
72	P63	C	General-purpose I/O port	—	○
	FRCK1_1		32-bit free-run timer ch.1 external clock input pin (Port 1)	—	○
	INT22_2		External interrupt request 22 input pin (Port 2)	—	○
73	P64	C	General-purpose I/O port	—	○
	AIN3_1		Up/Down counter ch.3 AIN input pin (Port 1)	—	○
74	P65	C	General-purpose I/O port	—	○
	BIN3_1		Up/Down counter ch.3 BIN input pin (Port 1)	—	○
	ADTRG0_1		10-bit A/D converter external trigger input pin (Port 1)	—	○
75	P66	C	General-purpose I/O port	—	○
	ZIN3_1		Up/Down counter ch.3 ZIN input pin (Port 1)	—	○
	FRCK0_1		32-bit free-run timer ch.0 external clock input pin (Port 1)	—	○
76	P67	C	General-purpose I/O port	—	○
	INT23_2		External interrupt request 23 input pin (Port 2)	—	○

(Continued)

# MB91625 Series

Pin no.	Pin name	I/O circuit type*1	Function	CMOS level input	CMOS level hysteresis input
LQFP-100					
77	P00	C	General-purpose I/O port	—	○
	TIOA0		Base timer ch.0 TIOA pin	—	—
	SOUT0_1		Multifunction serial interface ch.0 output pin (Port 1). This pin operates as SOUT0_1 when it is used in a UART/CSIO (operation modes 0 to 2).	—	—
	IN0		32-bit input capture ch.0 input pin	—	○
78	P01	C	General-purpose I/O port	—	○
	TIOB0		Base timer ch.0 TIOB pin	—	○
	SIN0_1		Multifunction serial interface ch.0 input pin (Port 1)	—	○
	IN1		32-bit input capture ch.1 input pin	—	○
79	P02	C	General-purpose I/O port	—	○
	TIOA1		Base timer ch.1 TIOA pin	—	○
	SCK0_1		Multifunction serial interface ch.0 clock I/O pin (Port 1). This pin operates as SCK0_1 when it is used in a UART/CSIO (operation modes 0 to 2).	—	○
	IN2		32-bit input capture ch.2 input pin	—	○
80	P03	C	General-purpose I/O port	—	○
	TIOB1		Base timer ch.1 TIOB pin	—	○
	IN3		32-bit input capture ch.3 input pin	—	○
81	P04	C	General-purpose I/O port	—	○
	TIOA2		Base timer ch.2 TIOA pin	—	—
	SOUT1 (SDA1)		Multifunction serial interface ch.1 output pin. This pin operates as SOUT1 when the product is used in a UART/CSIO (operation modes 0 to 2) and as SDA1 when it is used in an I <sup>2</sup> C (operation mode 4).	—	○
	IN4		32-bit input capture ch.4 input pin	—	○
82	P05	C	General-purpose I/O port	—	○
	TIOB2		Base timer ch.2 TIOB pin	—	○
	SIN1		Multifunction serial interface ch.1 input pin	—	○
	IN5		32-bit input capture ch.5 input pin	—	○

(Continued)

# MB91625 Series

Pin no.	Pin name	I/O circuit type*1	Function	CMOS level input	CMOS level hysteresis input
LQFP-100					
83	P06	C	General-purpose I/O port	—	○
	TIOA3		Base timer ch.3 TIOA pin	—	○
	SCK1 (SCL1)		Multifunction serial interface ch.1 clock I/O pin. This pin operates as SCK1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL1 when it is used in an I <sup>2</sup> C (operation mode 4).	—	○
	IN6		32-bit input capture ch.6 input pin	—	○
84	P07	C	General-purpose I/O port	—	○
	TIOB3		Base timer ch.3 TIOB pin	—	○
	IN7		32-bit input capture ch.7 input pin	—	○
85	P10	C	General-purpose I/O port	—	○
	TIOA4		Base timer ch.4 TIOA pin	—	—
	SOUT2 (SDA2)		Multifunction serial interface ch.2 output pin. This pin operates as SOUT2 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA2 when it is used in an I <sup>2</sup> C (operation mode 4).	—	○
	AIN0		Up/Down counter ch.0 AIN input pin	—	○
	INT0		External interrupt request 0 input pin	—	○
86	P11	C	General-purpose I/O port	—	○
	TIOB4		Base timer ch.4 TIOB pin	—	○
	SIN2		Multifunction serial interface ch.2 input pin	—	○
	BIN0		Up/Down counter ch.0 BIN input pin	—	○
	INT1		External interrupt request 1 input pin	—	○
87	P12	C	General-purpose I/O port	—	○
	TIOA5		Base timer ch.5 TIOA pin	—	○
	SCK2 (SCL2)		Multifunction serial interface ch.2 clock I/O pin. This pin operates as SCK2 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL2 when it is used in an I <sup>2</sup> C (operation mode 4).	—	○
	ZIN0		Up/Down counter ch.0 ZIN input pin	—	○
	INT2		External interrupt request 2 input pin	—	○
88	P13	C	General-purpose I/O port	—	○
	TIOB5		Base timer ch.5 TIOB pin	—	○
	INT3		External interrupt request 3 input pin	—	○

(Continued)

# MB91625 Series

Pin no.	Pin name	I/O circuit type*1	Function	CMOS level input	CMOS level hysteresis input
LQFP-100					
89	P14	C	General-purpose I/O port	—	○
	TIOA6		Base timer ch.6 TIOA pin	—	—
	SOUT3 (SDA3)		Multifunction serial interface ch.3 output pin. This pin operates as SOUT3 when the product is used in a UART/CSIO (operation modes 0 to 2) and as SDA3 when it is used in an I <sup>2</sup> C (operation mode 4).	—	○
	AIN1		Up/Down counter ch.1 AIN input pin	—	○
	INT4		External interrupt request 4 input pin	—	○
90	P15	C	General-purpose I/O port	—	○
	TIOB6		Base timer ch.6 TIOB pin	—	○
	SIN3		Multifunction serial interface ch.3 input pin	—	○
	BIN1		Up/Down counter ch.1 BIN input pin	—	○
	INT5		External interrupt request 5 input pin	—	○
91	P16	C	General-purpose I/O port	—	○
	TIOA7		Base timer ch.7 TIOA pin	—	○
	SCK3 (SCL3)		Multifunction serial interface ch.3 clock I/O pin. This pin operates as SCK3 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL3 when it is used in an I <sup>2</sup> C (operation mode 4).	—	○
	ZIN1		Up/Down counter ch.1 ZIN input pin	—	○
	INT6		External interrupt request 6 input pin	—	○
92	P17	C	General-purpose I/O port	—	○
	TIOB7		Base timer ch.7 TIOB pin	—	○
	INT7		External interrupt request 7 input pin	—	○
93	P20	D*2	General-purpose I/O port	—	○
	TIOA8		Base timer ch.8 TIOA pin	—	—
	SOUT4 (SDA4)		Multifunction serial interface ch.4 output pin. This pin operates as SOUT4 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA4 when it is used in an I <sup>2</sup> C (operation mode 4).	—	○
	AIN2		Up/Down counter ch.2 AIN input pin	—	○
94	P21	D*2	General-purpose I/O port	—	○
	TIOB8		Base timer ch.8 TIOB pin	—	○
	SIN4		Multifunction serial interface ch.4 input pin	—	○
	BIN2		Up/Down counter ch.2 BIN input pin	—	○

(Continued)

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Pin no. LQFP-100	Pin name	I/O circuit type*1	Function	CMOS level input	CMOS level hysteresis input
95	P22	D*2	General-purpose I/O port	—	○
	TIOA9		Base timer ch.9 TIOA pin	—	○
	SCK4 (SCL4)		Multifunction serial interface ch.4 clock I/O pin. This pin operates as SCK4 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL4 when it is used in an I <sup>2</sup> C (operation mode 4).	—	○
	ZIN2		Up/Down counter ch.2 ZIN input pin	—	○
96	P23	D*2	General-purpose I/O port	—	○
	TIOB9		Base timer ch.9 TIOB pin	—	○
97	P24	D*2	General-purpose I/O port	—	○
	TIOA10		Base timer ch.10 TIOA pin	—	—
	SOUT5 (SDA5)		Multifunction serial interface ch.5 output pin. This pin operates as SOUT5 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA5 when it is used in an I <sup>2</sup> C (operation mode 4).	—	○
	AIN3		Up/Down counter ch.3 AIN input pin	—	○
	OUT0		32-bit output compare ch.0 output pin	—	—
98	P25	D*2	General-purpose I/O port	—	○
	TIOB10		Base timer ch.10 TIOB pin	—	○
	SIN5		Multifunction serial interface ch.5 input pin	—	○
	BIN3		Up/Down counter ch.3 BIN input pin	—	○
	OUT1		32-bit output compare ch.1 output pin	—	—
99	P26	D*2	General-purpose I/O port	—	○
	TIOA11		Base timer ch.11 TIOA pin	—	○
	SCK5 (SCL5)		Multifunction serial interface ch.5 clock I/O pin. This pin operates as SCK5 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL5 when it is used in an I <sup>2</sup> C (operation mode 4).	—	○
	ZIN3		Up/Down counter ch.3 ZIN input pin	—	○
	OUT2		32-bit output compare ch.2 output pin	—	—
100	V <sub>CC</sub>	—	Power pin	—	—

\*1: Refer to “■ I/O CIRCUIT TYPE” for details on the I/O circuit types.

\*2: 5 V tolerant pin

# MB91625 Series

## ■ I/O CIRCUIT TYPE

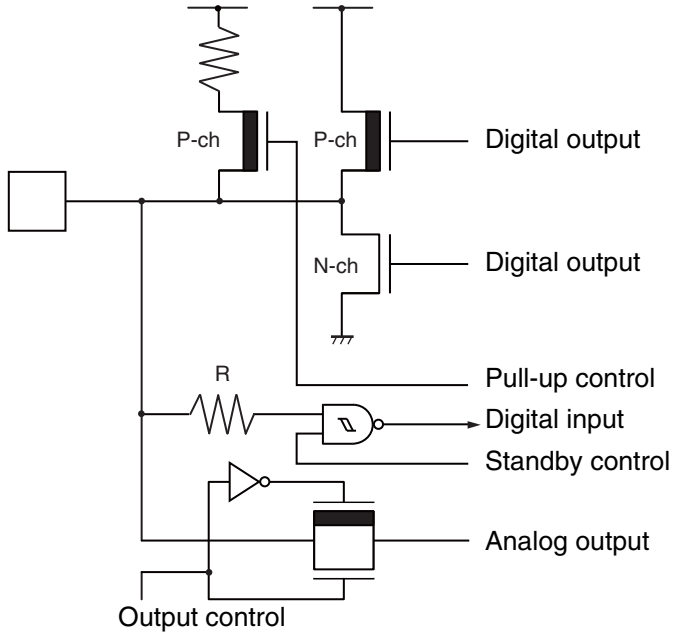
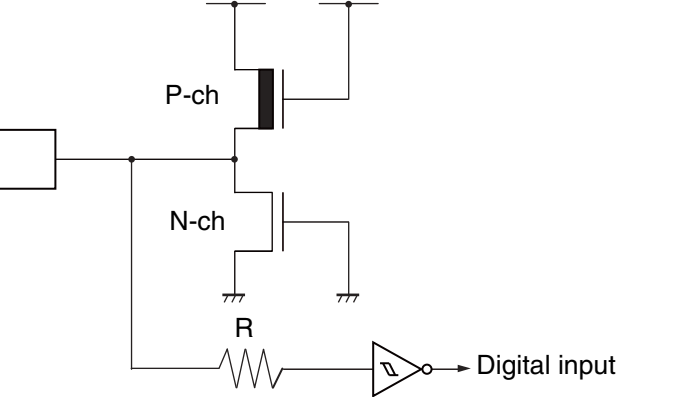
Type	Circuit	Remarks
A		<ul style="list-style-type: none"> <li>• Oscillation feedback resistance approx. 1 MΩ</li> <li>• With standby control</li> </ul>
C		<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• With pull-up control</li> <li>• With standby control</li> </ul> <p>Note: When this pin is used as an I<sup>2</sup>C pin, the digital output P-ch transistor is always off.</p>

(Continued)

Type	Circuit	Remarks
D	<p>The diagram shows a digital input pin connected to a pull-up resistor R. The input signal is also connected to a P-channel MOSFET (P-ch) and an N-channel MOSFET (N-ch). The P-ch MOSFET's source is connected to VDD and its gate is connected to the input. The N-ch MOSFET's source is connected to ground and its gate is connected to the input. The P-ch MOSFET's drain is labeled 'Digital output'. The N-ch MOSFET's drain is also labeled 'Digital output'. A separate input labeled 'Digital input Standby control' is connected to a NAND gate, which has one input connected to the input pin and the other input connected to ground.</p>	<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• 5 V tolerant input</li> <li>• With standby control</li> </ul> <p>Note: When this pin is used as an I<sup>2</sup>C pin, the digital output P-ch transistor is always off.</p>
E	<p>The diagram shows a digital input pin connected to a pull-up resistor R. The input signal is also connected to a P-channel MOSFET (P-ch) and an N-channel MOSFET (N-ch). The P-ch MOSFET's source is connected to VDD and its gate is connected to the input. The N-ch MOSFET's source is connected to ground and its gate is connected to the input. The P-ch MOSFET's drain is labeled 'Digital output'. The N-ch MOSFET's drain is also labeled 'Digital output'. A separate input labeled 'Pull-up control' is connected to the gate of the P-ch MOSFET. A separate input labeled 'Digital input Standby control' is connected to a NAND gate, which has one input connected to the input pin and the other input connected to ground. A separate input labeled 'Analog input' is connected to an analog input terminal. A separate input labeled 'Input control' is connected to a control terminal.</p>	<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• With input control</li> <li>• Analog input</li> <li>• With pull-up control</li> <li>• With standby control</li> </ul>

(Continued)

# MB91625 Series

Type	Circuit	Remarks
F	 <p>The diagram for Type F shows a CMOS output stage. It includes a pull-up resistor connected to a supply rail. The output node is driven by a P-channel MOSFET (P-ch) and an N-channel MOSFET (N-ch). The N-ch MOSFET is grounded. A digital input signal is connected to the gates of both MOSFETs through a resistor R. The output node is also connected to an analog output stage, which consists of a resistor R and an output control signal. The output control signal is connected to the gates of the P-ch and N-ch MOSFETs. The output node is connected to a digital output terminal and a pull-up control terminal. The output control signal is also connected to a standby control terminal.</p>	<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• With input control</li> <li>• Analog output</li> <li>• With pull-up control</li> <li>• With standby control</li> </ul>
H	 <p>The diagram for Type H shows a CMOS output stage. It includes a pull-up resistor connected to a supply rail. The output node is driven by a P-channel MOSFET (P-ch) and an N-channel MOSFET (N-ch). The N-ch MOSFET is grounded. A digital input signal is connected to the gates of both MOSFETs through a resistor R.</p>	<p>CMOS level hysteresis input</p>

(Continued)

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Type	Circuit	Remarks
I	<p>The diagram for Type I shows two input pins, X1A and X0A. X1A is connected to a P-channel MOSFET (Digital output), an N-channel MOSFET (Digital output), a resistor R (Digital input), a NAND gate (Standby control), and an inverter (Clock input). X0A is connected to a P-channel MOSFET (Digital output), an N-channel MOSFET (Digital output), a resistor R (Digital input), and a NAND gate (Standby control). The circuit also includes a NAND gate and an inverter.</p>	<ul style="list-style-type: none"> <li>• Oscillation feedback resistance approx. 10 MΩ</li> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• With standby control</li> </ul>
P	<p>The diagram for Type P shows an input pin connected to a stack of four N-channel MOSFETs. The top two are connected to a Control pin, and the bottom two are connected to a Mode input through a resistor R.</p>	<ul style="list-style-type: none"> <li>• Flash memory product only</li> <li>• CMOS level hysteresis input</li> <li>• High voltage control for testing Flash memory</li> </ul>

## ■ PRECAUTIONS FOR HANDLING THE DEVICES

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your FUJITSU SEMICONDUCTOR semiconductor devices.

### 1. Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

- Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

- Recommended Operating Conditions

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

- Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

- (1) Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

- (2) Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device. Therefore, avoid this type of connection.

- (3) Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

- Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNP junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

Note: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

- (a) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
- (b) Be sure that abnormal current flows do not occur during the power-on sequence.

- Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

- Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

- Precautions Related to Usage of Devices

FUJITSU SEMICONDUCTOR semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with FUJITSU SEMICONDUCTOR sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

## 2. Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under FUJITSU SEMICONDUCTOR's recommended conditions. For detailed information about mount conditions, contact your sales representative.

- Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder.

In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

- Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. FUJITSU SEMICONDUCTOR recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with FUJITSU SEMICONDUCTOR ranking of recommended conditions.

- Lead-Free Packaging

Note: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

- Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

- (a) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
- (b) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between + 5 °C and + 30 °C. When you open Dry Package that recommends humidity 40% to 70% relative humidity.
- (c) When necessary, FUJITSU SEMICONDUCTOR packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
- (d) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

- Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the FUJITSU SEMICONDUCTOR recommended conditions for baking.

Condition: + 125 °C / 24 h

- Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

- (a) Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
- (b) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
- (c) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ). Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
- (d) Ground all fixtures and instruments, or protect with anti-static measures.
- (e) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

### 3. Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above. For reliable performance, do the following:

- (1) Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

- (2) Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

- (3) Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

- (4) Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

- (5) Smoke, Flame

Note: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of FUJITSU SEMICONDUCTOR products in other special environmental conditions should consult with sales representatives.

# MB91625 Series

## ■ HANDLING DEVICES

### • Power supply pins

In products with multiple  $V_{CC}$  and  $V_{SS}$  pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating. Moreover, connect the current supply source with the  $V_{CC}$  and  $V_{SS}$  pins of this device at low impedance.

It is also advisable that a ceramic capacitor of approximately  $0.1 \mu\text{F}$  be connected as a bypass capacitor between  $V_{CC}$  and  $V_{SS}$  pins near this device.

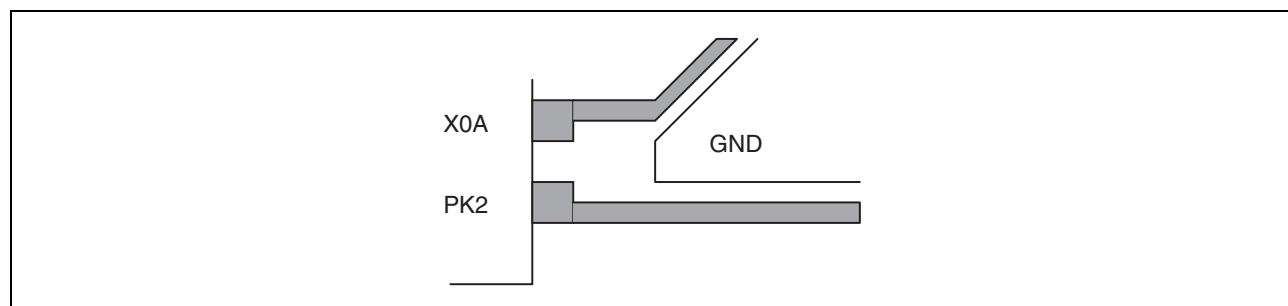
### • Crystal oscillator circuit

Noise near the X0 and X1 pins may cause the device to malfunction. Design the printed circuit board so that X0, X1, the crystal oscillator (or ceramic oscillator), and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended that the PC board artwork be designed such that the X0 and X1 pins are surrounded by ground plane as this is expected to produce stable operation.

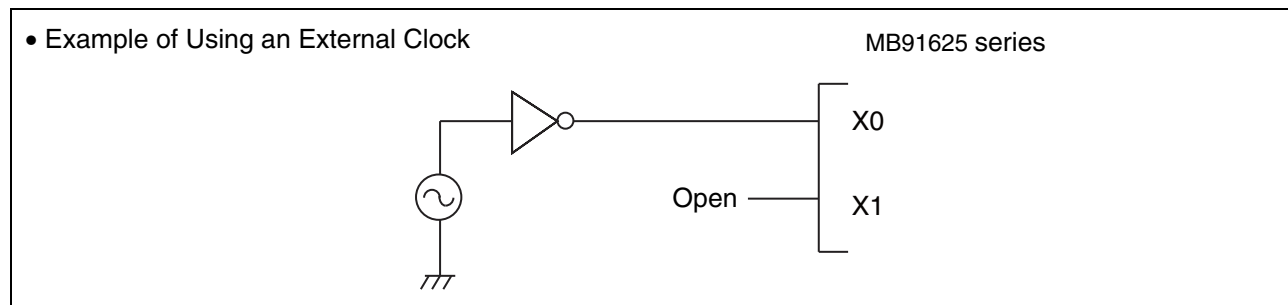
If a 32 kHz oscillator is used (X0A, X1A), use the PK2 pin for an input that changes as infrequently as possible. Furthermore, take steps such as shown in the following figure to prevent the X0A and PK2 wiring from running parallel to each other.

If 32 kHz oscillation is not used, there are no limitations.



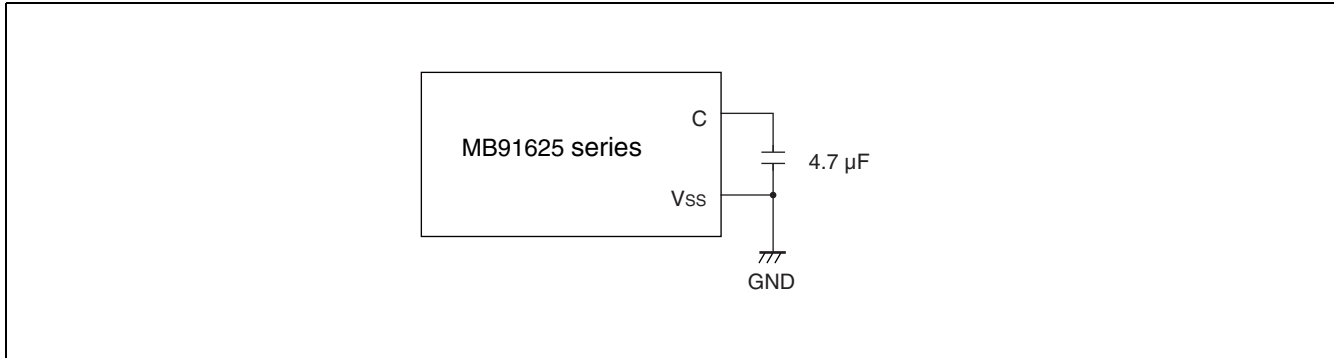
### • Using an external clock

When using an external clock, the clock signal should be input to the X0 pin only and the X1 should be kept open.



- C Pin

As MB91625 series includes an internal regulator, always connect a bypass capacitor of approximately 4.7  $\mu\text{F}$  to the C pin for use by the regulator.



- Mode pins (MD0, MD1)

Connect the MD pin (MD0, MD1) directly to  $V_{CC}$  or  $V_{SS}$  pins. Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and  $V_{CC}$  pins or  $V_{SS}$  pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

- Notes on power-on

- To ensure that the internal regulator and the oscillator have stabilized immediately after the power is turned on, keep an “L” level input connected to the  $\overline{\text{INIT}}$  pin for the duration of the regulator voltage stabilization wait time + the oscillator start time of the oscillator + the main oscillator stabilization wait time.
- Turn power on/off in the following order  
Turning on :  $V_{CC} \rightarrow AV_{CC} \rightarrow AVRH$   
Turning off :  $AVRH \rightarrow AV_{CC} \rightarrow V_{CC}$

Release the reset ( $\overline{\text{INIT}}$  pin “L” level to “H” level) after the power supply has stabilized.

- Caution on Operations during PLL Clock Mode

On this microcontroller, if in case the crystal oscillator breaks off or an external reference clock input stops while the PLL clock mode is selected, a self-oscillator circuit contained in the PLL may continue its operation at its self-running frequency.

However, FUJITSU SEMICONDUCTOR will not guarantee results of operations if such failure occurs.

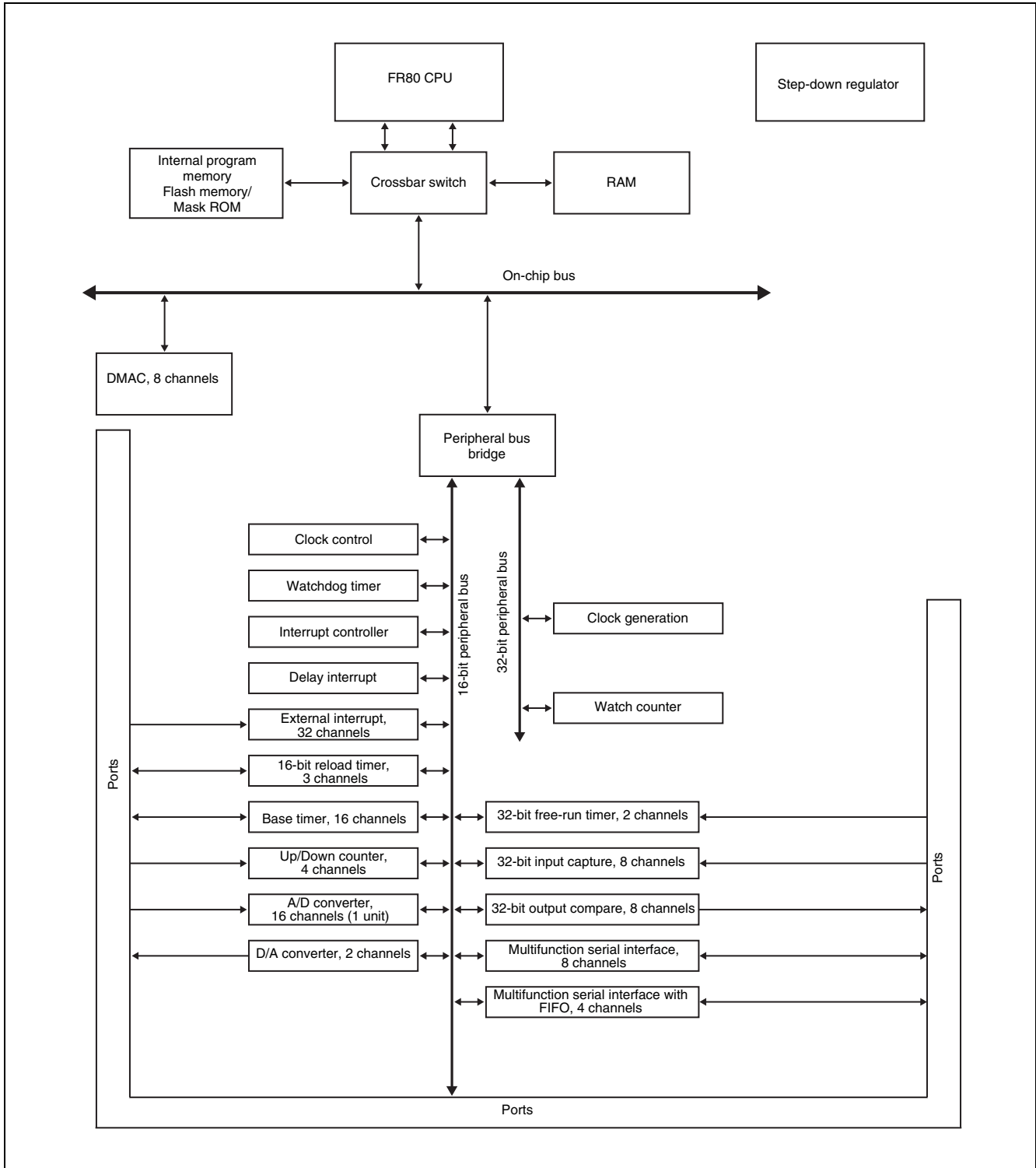
- Differences in features among the products with different memory sizes and between Flash products and MASK products

The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between Flash products and MASK products are different because chip layout and memory structures are different.

If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

# MB91625 Series

## ■ BLOCK DIAGRAM



## ■ MEMORY SPACE

### 1. Memory Space

The FR family has 4 Gbytes of logical address space ( $2^{32}$  addresses) available to the CPU by linear access.

- Direct Addressing Areas

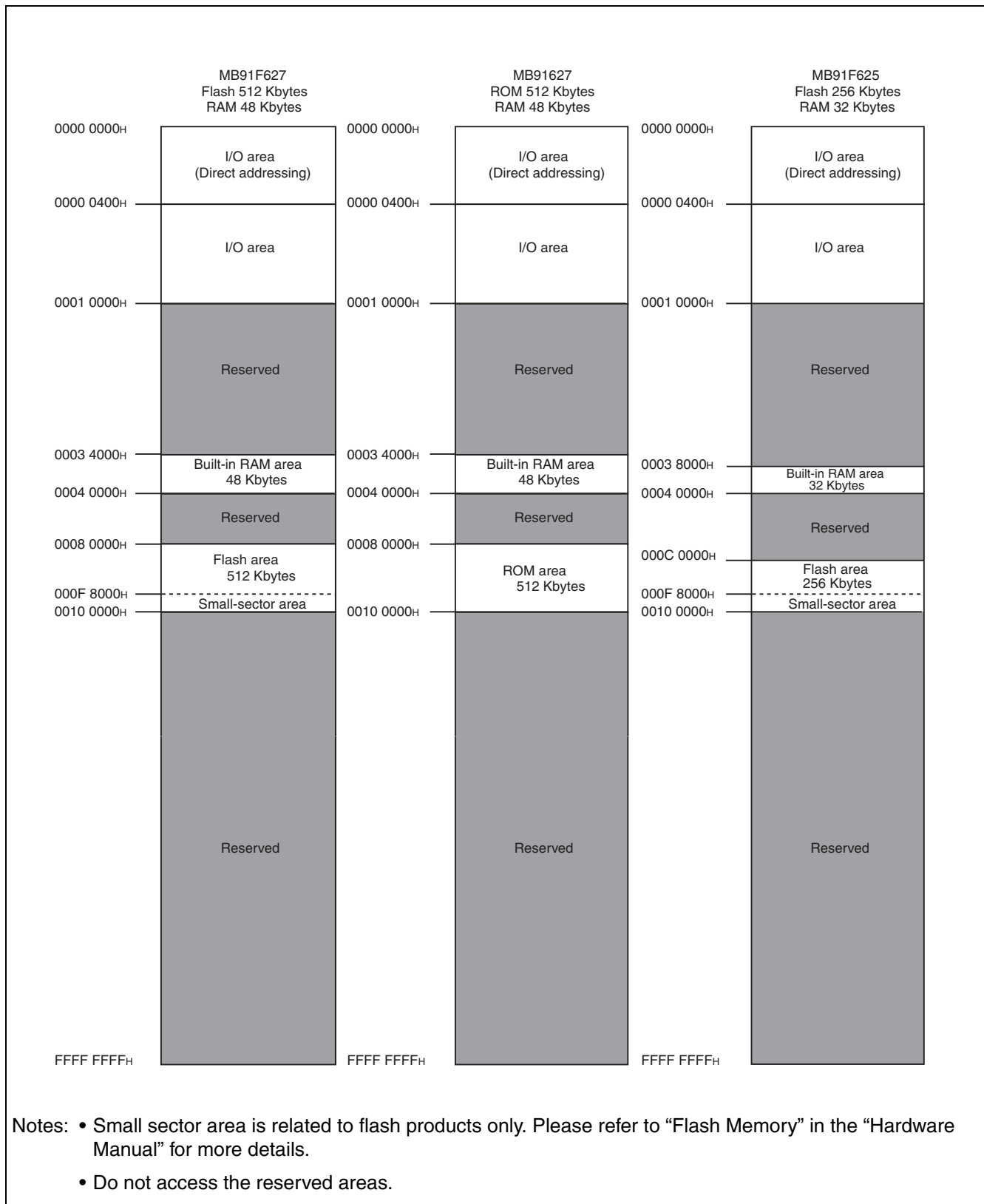
The following areas in the address space are used as I/O areas.

These areas are called direct addressing areas, and the address of an operand in these areas can be specified directly within an instruction. The size of the directly addressable area depends on the length of the data being accessed as follows.

- Byte data access : 0000 0000<sub>H</sub> to 0000 00FF<sub>H</sub>
- Half word data access : 0000 0000<sub>H</sub> to 0000 01FF<sub>H</sub>
- Word data access : 0000 0000<sub>H</sub> to 0000 03FF<sub>H</sub>

# MB91625 Series

## 2. Memory Map



## ■ I/O MAP

[How to read the table]

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 0000 <sub>H</sub>	PDR0 [R/W] B, H XXXXXXXX	PDR1 [R/W] B, H XXXXXXXX	PDR2 [R/W] B, H XXXXXXXXXXXX	PDR3 [R/W] B, H XXXXXXXX	Port data register
0000 003C <sub>H</sub>	WDCR0 [R/W] B, H -0--0000	WDTCP0 [R/W] B, H 00000000	—		Watchdog timer
0000 0040 <sub>H</sub>	EIRR0 [R/W] B, H, W 00000000	ENIR0 [R/W] B, H, W 00000000	ELVR0 [R/W] B, H, W 00000000 00000000		External interrupt 0 to 7

Initial value after reset  
 "1" : Initial value "1"  
 "0" : Initial value "0"  
 "X" : Initial value undefined  
 "-" : Reserved bit or undefined bit

Access unit  
 (B : byte, H : half word, W : word)

Read/write attribute  
 "R" : Indicates that there is a read only bit.  
 "R/W" : Indicates that there is a read/write bit.  
 "W" : Indicates that there is a write only bit.

Register name (column 1 of the register is at address 4n, column 2 is at address 4 n + 2...)

Leftmost register address (For word-length access, column 1 of the register is the MSB of the data.)

- Notes:
- When performing a data access, the addresses should be as below.
    - Word access : Address should be multiples of 4 (least significant 2 bits should be "00<sub>B</sub>")
    - Half word access : Address should be multiples of 2 (least significant bit should be "0<sub>B</sub>")
    - Byte access : —
  - Do not access the reserved areas.

# MB91625 Series

Address	Register				Block
	+0	+1	+2	+3	
0000 0000 <sub>H</sub>	PDR0 [R/W] B,H XXXXXXXX	PDR1 [R/W] B,H XXXXXXXX	PDR2 [R/W] B,H XXXXXXXX	PDR3 [R/W] B,H XXXXXXXX	Port data register
0000 0004 <sub>H</sub>	PDR4 [R/W] B,H XXXXXXXX	PDR5 [R/W] B,H XXXXXXXX	PDR6 [R/W] B,H XXXXXXXX	PDR7 [R/W] B,H XXXXXXXX	
0000 0008 <sub>H</sub>	PDR8 [R/W] B,H XXXXXXXX	PDR9 [R/W] B,H ----XXX	PDRA [R/W] B,H XXXXXXXX	—	
0000 000C <sub>H</sub> to 0000 0010 <sub>H</sub>	—				
0000 0014 <sub>H</sub>	PDRK [R/W] B ----XXX	—			
0000 0018 <sub>H</sub> to 0000 001C <sub>H</sub>	—				
0000 0020 <sub>H</sub> to 0000 0038 <sub>H</sub>	—				Reserved
0000 003C <sub>H</sub>	WDCR0 [R/W] B,H -0--0000	WDCPR0 [R/W] B,H 00000000	—		Watchdog timer
0000 0040 <sub>H</sub>	EIRR0 [R/W] B,H,W 00000000	ENIR0 [R/W] B,H,W 00000000	ELVR0 [R/W] B,H,W 00000000 00000000		External interrupt 0 to 7
0000 0044 <sub>H</sub>	DICR [R/W] B -----0	—			Delay interrupt
0000 0048 <sub>H</sub>	TMRLRA0 [R/W] H XXXXXXXX XXXXXXXX		TMR0 [R] H XXXXXXXX XXXXXXXX		16-bit reload timer ch.0
0000 004C <sub>H</sub>	—		TMCSR0 [R/W] H --000000 --000000		
0000 0050 <sub>H</sub>	TMRLRA1 [R/W] H XXXXXXXX XXXXXXXX		TMR1 [R] H XXXXXXXX XXXXXXXX		16-bit reload timer ch.1
0000 0054 <sub>H</sub>	—		TMCSR1 [R/W] H --000000 --000000		
0000 0058 <sub>H</sub>	TMRLRA2 [R/W] H XXXXXXXX XXXXXXXX		TMR2 [R] H XXXXXXXX XXXXXXXX		16-bit reload timer ch.2
0000 005C <sub>H</sub>	—		TMCSR2 [R/W] H --000000 --000000		

(Continued)

# MB91625 Series

Address	Register				Block
	+0	+1	+2	+3	
0000 0060 <sub>H</sub>	SCR0 [R/W] B,H,W 0--00000	SMR0 [R/W] B,H,W 000-0000	SSR0 [R,R/W] B,H,W 0-000011	ESCR0 [R/W] B,H,W -0000000	Multi-function serial interface ch.0
0000 0064 <sub>H</sub>	RDR0[R] / TDR0 [W] B,H,W*1 -----0 00000000		BGR10 [R/W] H,W 00000000	BGR00 [R/W] H,W 00000000	
0000 0068 <sub>H</sub>	SCR1 [R/W] / IBCR1 [R,R/W] B,H,W*2 0--00000	SMR1 [R/W] B,H,W 000-0000	SSR1 [R,R/W] B,H,W 0-000011	ESCR1 [R/W] / IBSR1 [R,R/W] B,H,W*2 -0000000	Multi-function serial interface ch.1
0000 006C <sub>H</sub>	RDR1 [R] / TDR1[W] B,H,W*1 -----0 00000000		BGR11 [R/W] H,W 00000000	BGR01 [R/W] H,W 00000000	
0000 0070 <sub>H</sub>	ISMK1 [R/W] B,H*2 -----	ISBA1 [R/W] B,H*2 -----	—		
0000 0074 <sub>H</sub>	SCR2 [R/W] / IBCR2 [R,R/W] B,H,W*2 0--00000	SMR2 [R/W] B,H,W 000-0000	SSR2 [R,R/W] B,H,W 0-000011	ESCR2 [R/W] / IBSR2 [R,R/W] B,H,W*2 -0000000	Multi-function serial interface ch.2
0000 0078 <sub>H</sub>	RDR2 [R] / TDR2 [W] B,H,W*1 -----0 00000000		BGR12 [R/W] H,W 00000000	BGR02 [R/W] H,W 00000000	
0000 007C <sub>H</sub>	ISMK2 [R/W] B,H*2 -----	ISBA2 [R/W] B,H*2 -----	—		
0000 0080 <sub>H</sub>	SCR3 [R/W] / IBCR3 [R,R/W] B,H,W*2 0--00000	SMR3 [R/W] B,H,W 000-0000	SSR3 [R,R/W] B,H,W 0-000011	ESCR3 [R/W] / IBSR3 [R,R/W] B,H,W*2 -0000000	Multi-function serial interface ch.3
0000 0084 <sub>H</sub>	RDR3 [R] / TDR3 [W] B,H,W*1 -----0 00000000		BGR13 [R/W] H,W 00000000	BGR03 [R/W] H,W 00000000	
0000 0088 <sub>H</sub>	ISMK3 [R/W] B,H*2 -----	ISBA3 [R/W] B,H*2 -----	—		

(Continued)

# MB91625 Series

Address	Register				Block
	+0	+1	+2	+3	
0000 008C <sub>H</sub>	SCR4 [R/W] / IBCR4 [R,R/W] B,H,W*2 0--00000	SMR4 [R/W] B,H,W 000-0000	SSR4 [R,R/W] B,H,W 0-000011	ESCR4 [R/W] / IBSR4 [R,R/W] B,H,W*2 -0000000	Multi-function serial interface ch.4
0000 0090 <sub>H</sub>	RDR4 [R] / TDR4 [W] B,H,W*1 -----0 00000000		BGR14 [R/W] H,W 00000000	BGR04 [R/W] H,W 00000000	
0000 0094 <sub>H</sub>	ISMK4 [R/W] B,H*2 -----	ISBA4 [R/W] B,H*2 -----	—		
0000 0098 <sub>H</sub>	SCR5 [R/W] / IBCR5 [R,R/W] B,H,W*2 0--00000	SMR5 [R/W] B,H,W 000-0000	SSR5 [R,R/W] B,H,W 0-000011	ESCR5 [R/W] / IBSR5 [R,R/W] B,H,W*2 -0000000	Multi-function serial interface ch.5
0000 009C <sub>H</sub>	RDR5 [R] / TDR5 [W] B,H,W*1 -----0 00000000		BGR15 [R/W] H,W 00000000	BGR05 [R/W] H,W 00000000	
0000 00A0 <sub>H</sub>	ISMK5 [R/W] B,H*2 -----	ISBA5 [R/W] B,H*2 -----	—		
0000 00A4 <sub>H</sub>	SCR6 [R/W] / IBCR6 [R,R/W] B,H,W*2 0--00000	SMR6 [R/W] B,H,W 000-0000	SSR6 [R,R/W] B,H,W 0-000011	ESCR6 [R/W] / IBSR6 [R,R/W] B,H,W*2 -0000000	Multi-function serial interface ch.6
0000 00A8 <sub>H</sub>	RDR6 [R] / TDR6 [W] B,H,W*1 -----0 00000000		BGR16 [R/W] H,W 00000000	BGR06 [R/W] H,W 00000000	
0000 00AC <sub>H</sub>	ISMK6 [R/W] B,H*2 -----	ISBA6 [R/W] B,H*2 -----	—		
0000 00B0 <sub>H</sub>	SCR7 [R/W] / IBCR7 [R,R/W] B,H,W*2 0--00000	SMR7 [R/W] B,H,W 000-0000	SSR7 [R,R/W] B,H,W 0-000011	ESCR7 [R/W] / IBSR7 [R,R/W] B,H,W*2 -0000000	Multi-function serial interface ch.7
0000 00B4 <sub>H</sub>	RDR7 [R] / TDR7 [W] B,H,W*1 -----0 00000000		BGR17 [R/W] H,W 00000000	BGR07 [R/W] H,W 00000000	
0000 00B8 <sub>H</sub>	ISMK7 [R/W] B,H*2 -----	ISBA7 [R/W] B,H*2 -----	—		
0000 00BC <sub>H</sub>	—				Reserved

(Continued)

# MB91625 Series

Address	Register				Block
	+0	+1	+2	+3	
0000 00C0 <sub>H</sub>	RDRM0 [R] / TDRM0 [W] B,H,W 00000000	RDRM1 [R] / TDRM1 [W] B,H,W 00000000	RDRM2 [R] / TDRM2 [W] B,H,W 00000000	RDRM3 [R] / TDRM3 [W] B,H,W 00000000	Multi-function serial interface data register (mirror)
0000 00C4 <sub>H</sub>	RDRM4 [R] / TDRM4 [W] B,H,W 00000000	RDRM5 [R] / TDRM5 [W] B,H,W 00000000	RDRM6 [R] / TDRM6 [W] B,H,W 00000000	RDRM7 [R] / TDRM7 [W] B,H,W 00000000	
0000 00C8 <sub>H</sub>	SSEL0123 [R/W] B -----00	—	SSEL4567 [R/W] B -----00	—	Multi-function serial interface serial clock selection
0000 00CC <sub>H</sub>	—				Reserved
0000 00D0 <sub>H</sub>	SCR8 [R/W] / IBCR8 [R,R/W] B,H,W*2 0--00000	SMR8 [R/W] B,H,W 000-0000	SSR8 [R,R/W] B,H,W 0-000011	ESCR8 [R/W] / IBSR8 [R,R/W] B,H,W*2 -0000000	Multi-function serial interface ch.8 (FIFO)
0000 00D4 <sub>H</sub>	RDR8 [R] / TDR8 [W] B,H,W*1 -----0 00000000		BGR18 [R/W] H,W 00000000	BGR08 [R/W] H,W 00000000	
0000 00D8 <sub>H</sub>	ISMK8 [R/W] B,H*2 -----	ISBA8 [R/W] B,H*2 -----	—		
0000 00DC <sub>H</sub>	FCR18 [R/W] B,H,W ---00100	FCR08 [R,R/W] B,H,W -0000000	FBYTE28 [R/W] B,H,W 00000000	FBYTE18 [R/W] B,H,W 00000000	
0000 00E0 <sub>H</sub>	SCR9 [R/W] / IBCR9 [R,R/W] B,H,W*2 0--00000	SMR9 [R/W] B,H,W 000-0000	SSR9 [R,R/W] B,H,W 0-000011	ESCR9 [R/W] / IBSR9 [R,R/W] B,H,W*2 -0000000	Multi-function serial interface ch.9 (FIFO)
0000 00E4 <sub>H</sub>	RDR9 [R] / TDR9 [W] B,H,W*1 -----0 00000000		BGR19 [R/W] H,W 00000000	BGR09 [R/W] H,W 00000000	
0000 00E8 <sub>H</sub>	ISMK9 [R/W] B,H*2 -----	ISBA9 [R/W] B,H*2 -----	—		
0000 00EC <sub>H</sub>	FCR19 [R/W] B,H,W ---00100	FCR09 [R,R/W] B,H,W -0000000	FBYTE29 [R/W] B,H,W 00000000	FBYTE19 [R/W] B,H,W 00000000	

(Continued)

# MB91625 Series

Address	Register				Block
	+0	+1	+2	+3	
0000 00F0 <sub>H</sub>	SCR10 [R/W] / IBCR10 [R,R/W] B,H,W*2 0--00000	SMR10 [R/W] B,H,W 000-0000	SSR10 [R,R/W] B,H,W 0-000011	ESCR10 [R/W] / IBSR10 [R,R/W] B,H,W*2 -0000000	Multi-function serial interface ch.10 (FIFO)
0000 00F4 <sub>H</sub>	RDR10 [R] / TDR10 [W] B,H,W*1 -----0 00000000		BGR110 [R/W] H,W 00000000	BGR010 [R/W] H,W 00000000	
0000 00F8 <sub>H</sub>	ISMK10 [R/W] B,H*2 -----	ISBA10 [R/W] B,H*2 -----	—		
0000 00FC <sub>H</sub>	FCR110 [R/W] B,H,W ---00100	FCR010 [R,R/W] B,H,W -0000000	FBYTE210 [R/W] B,H,W 00000000	FBYTE110 [R/W] B,H,W 00000000	
0000 0100 <sub>H</sub>	SCR11 [R/W] / IBCR11 [R,R/W] B,H,W*2 0--00000	SMR11 [R/W] B,H,W 000-0000	SSR11 [R,R/W] B,H,W 0-000011	ESCR11 [R/W] / IBSR11 [R,R/W] B,H,W*2 -0000000	Multi-function serial interface ch.11 (FIFO)
0000 0104 <sub>H</sub>	RDR11[R] / TDR11[W] B,H,W*1 -----0 00000000		BGR111 [R/W] H,W 00000000	BGR011 [R/W] H,W 00000000	
0000 0108 <sub>H</sub>	ISMK11 [R/W] B,H*2 -----	ISBA11 [R/W] B,H*2 -----	—		
0000 010C <sub>H</sub>	FCR111 [R/W] B,H,W ---00100	FCR011 [R,R/W] B,H,W -0000000	FBYTE211 [R/W] B,H,W 00000000	FBYTE111 [R/W] B,H,W 00000000	
0000 0110 <sub>H</sub>	EIRR1 [R/W] B,H,W 00000000	ENIR1 [R/W] B,H,W 00000000	ELVR1 [R/W] B,H,W 00000000 00000000		External interrupt 8 to 15
0000 0114 <sub>H</sub>	EIRR2 [R/W] B,H,W 00000000	ENIR2 [R/W] B,H,W 00000000	ELVR2 [R/W] B,H,W 00000000 00000000		External interrupt 16 to 23
0000 0118 <sub>H</sub>	EIRR3 [R/W] B,H,W 00000000	ENIR3 [R/W] B,H,W 00000000	ELVR3 [R/W] B,H,W 00000000 00000000		External interrupt 24 to 31
0000 011C <sub>H</sub>	—				Reserved

(Continued)

# MB91625 Series

Address	Register				Block
	+0	+1	+2	+3	
0000 0120 <sub>H</sub>	ADCR0 [R/W] B,H 000-0000	ADSR0 [R,R/W] B,H 00---000	—		A/D converter
0000 0124 <sub>H</sub>	SCCR0 [R,R/W] B,H 1000-000	SFNS0 [R/W] B,H ----0000	SCFD0 [R] B,H XXXXXXXX XX-XXXXX		
0000 0128 <sub>H</sub>	—		SCIS10 [R/W] B,H 00000000	SCIS00 [R/W] B,H 00000000	
0000 012C <sub>H</sub>	PCCR0 [R,R/W] B,H 1000-000	PFNS0[R/W] B,H -----00	PCFD0[R] B,H XXXXXXXX XXXXXXXX		
0000 0130 <sub>H</sub>	PCIS0 [R/W] B 00000000	—	CMPD0 [R/W] B,H 00000000	CMPCR0 [R/W] B,H 00000000	
0000 0134 <sub>H</sub>	—		ADSS10 [R/W] B,H 00000000	ADSS00 [R/W] B,H 00000000	
0000 0138 <sub>H</sub>	ADST00 [R/W] B,H 00100000	ADST10 [R/W] B,H 00100000	ADCT0 [R/W] B ----111	—	
0000 013C <sub>H</sub>	—				Reserved
0000 0140 <sub>H</sub>	BT0TMR [R] H 00000000 00000000		BT0TMCR [R/W] B,H -0000000 00000000		Base timer ch.0
0000 0144 <sub>H</sub>	—	BT0STC [R/W] B 0000-000	—		
0000 0148 <sub>H</sub>	BT0PCSR / BT0PRLL [R/W] H XXXXXXXX XXXXXXXX		BT0PDUT / BT0PRLH / BT0DTBF [R/W] H XXXXXXXX XXXXXXXX		
0000 014C <sub>H</sub>	—				
0000 0150 <sub>H</sub>	BT1TMR [R] H 00000000 00000000		BT1TMCR [R/W] B,H -0000000 00000000		Base timer ch.1
0000 0154 <sub>H</sub>	—	BT1STC [R/W] B 0000-000	—		
0000 0158 <sub>H</sub>	BT1PCSR / BT1PRLL [R/W] H XXXXXXXX XXXXXXXX		BT1PDUT / BT1PRLH / BT1DTBF [R/W] H XXXXXXXX XXXXXXXX		
0000 015C <sub>H</sub>	—				

(Continued)

# MB91625 Series

Address	Register				Block
	+0	+1	+2	+3	
0000 0160 <sub>H</sub>	BT2TMR [R] H 00000000 00000000		BT2TMCR [R/W] B,H -0000000 00000000		Base timer ch.2
0000 0164 <sub>H</sub>	—	BT2STC [R/W] B 0000-000	—		
0000 0168 <sub>H</sub>	BT2PCSR / BT2PRLL [R/W] H XXXXXXXX XXXXXXXX		BT2PDUT / BT2PRLH / BT2DTBF [R/W] H XXXXXXXX XXXXXXXX		
0000 016C <sub>H</sub>	—				
0000 0170 <sub>H</sub>	BT3TMR [R] H 00000000 00000000		BT3TMCR [R/W] B,H -0000000 00000000		Base timer ch.3
0000 0174 <sub>H</sub>	—	BT3STC [R/W] B 0000-000	—		
0000 0178 <sub>H</sub>	BT3PCSR / BT3PRLL [R/W] H XXXXXXXX XXXXXXXX		BT3PDUT / BT3PRLH / BT3DTBF [R/W] H XXXXXXXX XXXXXXXX		
0000 017C <sub>H</sub>	BTSEL0123 [R/W] B 00000000	—			
0000 0180 <sub>H</sub>	DACR0 [R/W] B,H,W -----0	DADR0 [R/W] B,H,W XXXXXXXX	DACR1 [R/W] B,H,W -----0	DADR1 [R/W] B,H,W XXXXXXXX	D/A converter
0000 0184 <sub>H</sub> to 0000 018C <sub>H</sub>	—				
0000 0190 <sub>H</sub> to 0000 01A8 <sub>H</sub>	—				Reserved
0000 01AC <sub>H</sub>	ADCHE [R/W] B,H,W -11111111 11111111 11111111 11111111				A/D channel enable
0000 01B0 <sub>H</sub>	IRPR0H [R] B 000----	—	IRPR1H [R] B,H 000-000-	IRPR1L [R] B,H 000-000-	Interrupt request batch read function
0000 01B4 <sub>H</sub>	IRPR2H [R] B,H,W 0000----	IRPR2L [R] B,H,W 000----	IRPR3H [R] B,H,W 0000----	IRPR3L [R] B,H,W 00000---	
0000 01B8 <sub>H</sub>	IRPR4H [R] B,H,W 0000----	IRPR4L [R] B,H,W 000000--	IRPR5H [R] B,H,W 0000----	IRPR5L [R] B,H,W 0000----	
0000 01BC <sub>H</sub>	IRPR6H [R] B,H,W 0000----	IRPR6L [R] B,H,W 0000----	IRPR7H [R] B,H,W 0000----	IRPR7L [R] B,H,W 0000----	

(Continued)

# MB91625 Series

Address	Register				Block
	+0	+1	+2	+3	
0000 01C0 <sub>H</sub>	RCRH0 [W] H,W 00000000	RCRL0 [W] B,H,W 00000000	UDCRH0 [R] H,W 00000000	UDCRL0 [R] B,H,W 00000000	Up/down counter ch.0
0000 01C4 <sub>H</sub>	CCR0 [R,R/W] B,H 00000000 -0001000		—	CSR0 [R,R/W] B 00000000	
0000 01C8 <sub>H</sub>	—				
0000 01CC <sub>H</sub>	—				Reserved
0000 01D0 <sub>H</sub>	RCRH1 [W] H,W 00000000	RCRL1 [W] B,H,W 00000000	UDCRH1 [R] H,W 00000000	UDCRL1 [R] B,H,W 00000000	Up/down counter ch.1
0000 01D4 <sub>H</sub>	CCR1 [R,R/W] B,H 00000000 -0001000		—	CSR1 [R,R/W] B 00000000	
0000 01D8 <sub>H</sub>	—				
0000 01DC <sub>H</sub>	—				Reserved
0000 01E0 <sub>H</sub>	RCRH2 [W] H,W 00000000	RCRL2 [W] B,H,W 00000000	UDCRH2 [R] H,W 00000000	UDCRL2 [R] B,H,W 00000000	Up/down counter ch.2
0000 01E4 <sub>H</sub>	CCR2 [R,R/W] B,H 00000000 -0001000		—	CSR2 [R,R/W] B 00000000	
0000 01E8 <sub>H</sub>	—				
0000 01EC <sub>H</sub>	—				Reserved
0000 01F0 <sub>H</sub>	RCRH3 [W] H,W 00000000	RCRL3 [W] B,H,W 00000000	UDCRH3 [R] H,W 00000000	UDCRL3 [R] B,H,W 00000000	Up/down counter ch.3
0000 01F4 <sub>H</sub>	CCR3 [R,R/W] B,H 00000000 -0001000		—	CSR3 [R,R/W] B 00000000	
0000 01F8 <sub>H</sub>	—				
0000 01FC <sub>H</sub>	—				Reserved
0000 0200 <sub>H</sub>	CPCLR0 [R/W] W 11111111 11111111 11111111 11111111				32-bit Free-run timer ch.0
0000 0204 <sub>H</sub>	TCDT0 [R/W] W 00000000 00000000 00000000 00000000				
0000 0208 <sub>H</sub>	TCCSH0 [R/W] B,H 0----00	TCCSL0 [R/W] B,H -1-00000	—		

(Continued)

# MB91625 Series

Address	Register				Block
	+0	+1	+2	+3	
0000 020CH	IPCP0 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				32-bit Input capture ch.0 to ch.3
0000 0210H	IPCP1 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0214H	IPCP2 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0218H	IPCP3 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 021CH	—	ICS01 [R/W] B 00000000	—	ICS23 [R/W] B 00000000	
0000 0220H	IPCP4 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				32-bit Input capture ch.4 to ch.7
0000 0224H	IPCP5 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0228H	IPCP6 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 022CH	IPCP7 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0230H	—	ICS45 [R/W] B 00000000	—	ICS67 [R/W] B 00000000	
0000 0234H	OCCP0 [R/W] W 00000000 00000000 00000000 00000000				32-bit Output compare ch.0 to ch.3
0000 0238H	OCCP1 [R/W] W 00000000 00000000 00000000 00000000				
0000 023CH	OCCP2 [R/W] W 00000000 00000000 00000000 00000000				
0000 0240H	OCCP3 [R/W] W 00000000 00000000 00000000 00000000				
0000 0244H	OCSH1 [R/W] B,H,W ---0--00	OCSL0 [R/W] B,H,W 0000--00	OCSH3 [R/W] B,H,W ---0--00	OCSL2 [R/W] B,H,W 0000--00	

(Continued)

# MB91625 Series

Address	Register				Block
	+0	+1	+2	+3	
0000 0248 <sub>H</sub>	OCCP4 [R/W] W 00000000 00000000 00000000 00000000				32-bit Output compare ch.4 to ch.7
0000 024C <sub>H</sub>	OCCP5 [R/W] W 00000000 00000000 00000000 00000000				
0000 0250 <sub>H</sub>	OCCP6 [R/W] W 00000000 00000000 00000000 00000000				
0000 0254 <sub>H</sub>	OCCP7 [R/W] W 00000000 00000000 00000000 00000000				
0000 0258 <sub>H</sub>	OCSH5 [R/W] B,H,W ---0--00	OCSL4 [R/W] B,H,W 0000--00	OCSH7 [R/W] B,H,W ---0--00	OCSL6 [R/W] B,H,W 0000--00	
0000 025C <sub>H</sub>	FRTSEL [R/W] B -----00	—			Free-run timer selector
0000 0260 <sub>H</sub>	CPCLR1 [R/W] W 11111111 11111111 11111111 11111111				32-bit Free-run timer ch.1
0000 0264 <sub>H</sub>	TCDT1 [R/W] W 00000000 00000000 00000000 00000000				
0000 0268 <sub>H</sub>	TCCSH1 [R/W] B,H 0-----00	TCCSL1 [R/W] B,H -1-00000	—		
0000 026C <sub>H</sub> to 0000 031C <sub>H</sub>	—				Reserved
0000 0320 <sub>H</sub>	FCTLR [R/W] H -0--1011 -----		—	FSTR [R] B -----1	Flash memory control
0000 0324 <sub>H</sub> to 0000 0334 <sub>H</sub>	—				Reserved
0000 0338 <sub>H</sub>	—		WREN [R/W] B,H 00000000 00000000		Wild register
0000 033C <sub>H</sub>	—				
0000 0340 <sub>H</sub> to 0000 037C <sub>H</sub>	—				Reserved

(Continued)

# MB91625 Series

Address	Register				Block
	+0	+1	+2	+3	
0000 0380 <sub>H</sub>	WRAR00 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				Wild register
0000 0384 <sub>H</sub>	WRDR00 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0388 <sub>H</sub>	WRAR01 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0000 038C <sub>H</sub>	WRDR01 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0390 <sub>H</sub>	WRAR02 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0000 0394 <sub>H</sub>	WRDR02 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0398 <sub>H</sub>	WRAR03 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0000 039C <sub>H</sub>	WRDR03 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03A0 <sub>H</sub>	WRAR04 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0000 03A4 <sub>H</sub>	WRDR04 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03A8 <sub>H</sub>	WRAR05 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0000 03AC <sub>H</sub>	WRDR05 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03B0 <sub>H</sub>	WRAR06 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				

(Continued)

# MB91625 Series

Address	Register				Block
	+0	+1	+2	+3	
0000 03B4 <sub>H</sub>	WRDR06 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Wild register
0000 03B8 <sub>H</sub>	WRAR07 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0000 03BC <sub>H</sub>	WRDR07 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03C0 <sub>H</sub>	WRAR08 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0000 03C4 <sub>H</sub>	WRDR08 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03C8 <sub>H</sub>	WRAR09 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0000 03CC <sub>H</sub>	WRDR09 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03D0 <sub>H</sub>	WRAR10 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0000 03D4 <sub>H</sub>	WRDR10 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03D8 <sub>H</sub>	WRAR11 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0000 03DC <sub>H</sub>	WRDR11 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03E0 <sub>H</sub>	WRAR12 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0000 03E4 <sub>H</sub>	WRDR12 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03E8 <sub>H</sub>	WRAR13 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0000 03EC <sub>H</sub>	WRDR13 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03F0 <sub>H</sub>	WRAR14 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0000 03F4 <sub>H</sub>	WRDR14 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03F8 <sub>H</sub>	WRAR15 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0000 03FC <sub>H</sub>	WRDR15 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

(Continued)

# MB91625 Series

Address	Register				Block
	+0	+1	+2	+3	
0000 0400 <sub>H</sub>	DDR0 [R/W] B,H 00000000	DDR1 [R/W] B,H 00000000	DDR2 [R/W] B,H 00000000	DDR3 [R/W] B,H 00000000	Data direction register
0000 0404 <sub>H</sub>	DDR4 [R/W] B,H 00000000	DDR5 [R/W] B,H 00000000	DDR6 [R/W] B,H 00000000	DDR7[R/W] B,H 00000000	
0000 0408 <sub>H</sub>	DDR8 [R/W] B,H 00000000	DDR9 [R/W] B,H -----000	DDRA [R/W] B 00000000	—	
0000 040C <sub>H</sub> to 0000 0410 <sub>H</sub>	—				
0000 0414 <sub>H</sub>	DDRK [R/W] B -----000	—			
0000 0418 <sub>H</sub> to 0000 041C <sub>H</sub>	—				
0000 0420 <sub>H</sub>	PCR0 [R/W] B,H 00000000	PCR1 [R/W] B,H 00000000	—		Pull-up control register
0000 0424 <sub>H</sub>	—	PCR5 [R/W] B 00000000	PCR6 [R/W] B,H 00000000	PCR7[R/W] B,H 00000000	
0000 0428 <sub>H</sub>	PCR8 [R/W] B,H 00000000	PCR9 [R/W] B,H -----000	PCRA [R/W] B 00000000	—	
0000 042C <sub>H</sub> to 0000 0430 <sub>H</sub>	—				
0000 0434 <sub>H</sub>	PCRK [R/W] B -----0--	—			
0000 0438 <sub>H</sub> to 0000 043C <sub>H</sub>	—				

(Continued)

Address	Register				Block	
	+0	+1	+2	+3		
0000 0440 <sub>H</sub>	ICR00 [R,R/W] B,H,W ---11111	ICR01 [R,R/W] B,H,W ---11111	ICR02 [R,R/W] B,H,W ---11111	ICR03 [R,R/W] B,H,W ---11111	Interrupt control	
0000 0444 <sub>H</sub>	ICR04 [R,R/W] B,H,W ---11111	ICR05 [R,R/W] B,H,W ---11111	ICR06 [R,R/W] B,H,W ---11111	ICR07 [R,R/W] B,H,W ---11111		
0000 0448 <sub>H</sub>	ICR08 [R,R/W] B,H,W ---11111	ICR09 [R,R/W] B,H,W ---11111	ICR10 [R,R/W] B,H,W ---11111	ICR11 [R,R/W] B,H,W ---11111		
0000 044C <sub>H</sub>	ICR12 [R,R/W] B,H,W ---11111	ICR13 [R,R/W] B,H,W ---11111	ICR14 [R,R/W] B,H,W ---11111	ICR15 [R,R/W] B,H,W ---11111		
0000 0450 <sub>H</sub>	ICR16 [R,R/W] B,H,W ---11111	ICR17 [R,R/W] B,H,W ---11111	ICR18 [R,R/W] B,H,W ---11111	ICR19 [R,R/W] B,H,W ---11111		
0000 0454 <sub>H</sub>	ICR20 [R,R/W] B,H,W ---11111	ICR21 [R,R/W] B,H,W ---11111	ICR22 [R,R/W] B,H,W ---11111	ICR23 [R,R/W] B,H,W ---11111		
0000 0458 <sub>H</sub>	ICR24 [R,R/W] B,H,W ---11111	ICR25 [R,R/W] B,H,W ---11111	ICR26 [R,R/W] B,H,W ---11111	ICR27 [R,R/W] B,H,W ---11111		
0000 045C <sub>H</sub>	ICR28 [R,R/W] B,H,W ---11111	ICR29 [R,R/W] B,H,W ---11111	ICR30 [R,R/W] B,H,W ---11111	ICR31 [R,R/W] B,H,W ---11111		
0000 0460 <sub>H</sub>	ICR32 [R,R/W] B,H,W ---11111	ICR33 [R,R/W] B,H,W ---11111	ICR34 [R,R/W] B,H,W ---11111	ICR35 [R,R/W] B,H,W ---11111		
0000 0464 <sub>H</sub>	ICR36 [R,R/W] B,H,W ---11111	ICR37 [R,R/W] B,H,W ---11111	ICR38 [R,R/W] B,H,W ---11111	ICR39 [R,R/W] B,H,W ---11111		
0000 0468 <sub>H</sub>	ICR40 [R,R/W] B,H,W ---11111	ICR41 [R,R/W] B,H,W ---11111	ICR42 [R,R/W] B,H,W ---11111	ICR43 [R,R/W] B,H,W ---11111		
0000 046C <sub>H</sub>	ICR44 [R,R/W] B,H,W ---11111	ICR45 [R,R/W] B,H,W ---11111	ICR46 [R,R/W] B,H,W ---11111	ICR47 [R,R/W] B,H,W ---11111		
0000 0470 <sub>H</sub> to 0000 047C <sub>H</sub>	—					Reserved

(Continued)

# MB91625 Series

Address	Register				Block
	+0	+1	+2	+3	
0000 0480 <sub>H</sub>	RSTRR [R] B,H,W 11-X--X*3	RSTCR [R/W] B,H,W 000----0	STBCR [R/W] B,H,W 0000--11	SLPRR [R/W] B,H,W 00000000	Reset control/ Power consumption control
0000 0484 <sub>H</sub>	—				
0000 0488 <sub>H</sub>	DIVR0 [R/W] B,H 000-----	—	DIVR2 [R/W] B 0011----	—	Clock division control
0000 048C <sub>H</sub>	—				
0000 0490 <sub>H</sub>	IORR0 [R/W] B,H,W -0000000	IORR1 [R/W] B,H,W -0000000	IORR2 [R/W] B,H,W -0000000	IORR3 [R/W] B,H,W -0000000	Peripheral DMA transmission re- quest control
0000 0494 <sub>H</sub>	IORR4 [R/W] B,H,W -0000000	IORR5 [R/W] B,H,W -0000000	IORR6 [R/W] B,H,W -0000000	IORR7 [R/W] B,H,W -0000000	
0000 0498 <sub>H</sub> to 0000 049C <sub>H</sub>	—				Reserved
0000 04A0 <sub>H</sub>	PFR0 [R/W] B,H 00000000	PFR1 [R/W] B,H 00000000	PFR2 [R/W] B,H 00000000	PFR3 [R/W] B,H 00000000	Port function register
0000 04A4 <sub>H</sub>	PFR4 [R/W] B,H 00000000	PFR5 [R/W] B,H 00000000	PFR6 [R/W] B,H 00-00-0-	PFR7[R/W] B,H 00000000	
0000 04A8 <sub>H</sub>	PFR8 [R/W] B 00000000	—	PFRA [R/W] B 00-00000	—	
0000 04AC <sub>H</sub> to 0000 04B4 <sub>H</sub>	—				

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# MB91625 Series

Address	Register				Block
	+0	+1	+2	+3	
0000 04B8 <sub>H</sub>	EPFR0 [R/W] B,H --000000	EPFR1 [R/W] B,H --000000	EPFR2 [R/W] B,H --000000	EPFR3 [R/W] B,H --000000	Extended port function register
0000 04BC <sub>H</sub>	EPFR4 [R/W] B,H 00000000	EPFR5 [R/W] B,H 00000000	EPFR6 [R/W] B,H 00000000	EPFR7 [R/W] B,H ---00000	
0000 04C0 <sub>H</sub>	EPFR8 [R/W] B,H ---00000	EPFR9 [R/W] B,H ---00000	EPFR10 [R/W] B,H ---00000	EPFR11 [R/W] B,H ---00000	
0000 04C4 <sub>H</sub>	EPFR12 [R/W] B,H ---00000	EPFR13 [R/W] B,H ---00000	EPFR14 [R/W] B,H ---00000	EPFR15 [R/W] B,H ---00000	
0000 04C8 <sub>H</sub>	EPFR16 [R/W] B,H ---00000	EPFR17 [R/W] B,H ---00000	EPFR18 [R/W] B,H 00000000	EPFR19 [R/W] B,H -0000001	
0000 04CC <sub>H</sub>	EPFR20 [R/W] B,H --000000	EPFR21 [R/W] B,H --000000	EPFR22 [R/W] B,H --000000	EPFR23 [R/W] B,H --000000	
0000 04D0 <sub>H</sub>	EPFR24 [R/W] B,H --000000	EPFR25 [R/W] B,H --000000	EPFR26 [R/W] B,H --000000	EPFR27 [R/W] B,H --000000	
0000 04D4 <sub>H</sub>	EPFR28 [R/W] B,H 00000000	EPFR29 [R/W] B,H 00000000	EPFR30 [R/W] B,H ----0000	EPFR31 [R/W] B,H -0000000	
0000 04D8 <sub>H</sub>	EPFR32 [R/W] B,H 00000000	EPFR33 [R/W] B,H --000000	EPFR34 [R/W] B -0000000	—	
0000 04DC <sub>H</sub>	—				
0000 04E0 <sub>H</sub> to 0000 04EC <sub>H</sub>	—				Reserved
0000 04F0 <sub>H</sub>	ICSEL0 [R/W] B,H,W ----000	ICSEL1 [R/W] B,H,W ----000	ICSEL2 [R/W] B,H,W ----000	ICSEL3 [R/W] B,H,W ----000	DMA start request clear select function
0000 04F4 <sub>H</sub>	ICSEL4 [R/W] B,H,W -----00	ICSEL5 [R/W] B,H,W ----000	ICSEL6 [R/W] B,H,W ----00	ICSEL7 [R/W] B,H,W -----0	
0000 04F8 <sub>H</sub>	ICSEL8 [R/W] B,H,W -----00	ICSEL9 [R/W] B,H,W ----000	ICSEL10 [R/W] B,H,W ----0000	ICSEL11 [R/W] B,H,W ----0000	
0000 04FC <sub>H</sub>	ICSEL12 [R/W] B,H ----0000	ICSEL13 [R/W] B,H -----0-0	ICSEL14 [R/W] B -----00	—	

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# MB91625 Series

Address	Register				Block
	+0	+1	+2	+3	
0000 0500 <sub>H</sub> to 0000 050C <sub>H</sub>	—				Reserved
0000 0510 <sub>H</sub>	CSELR [R/W] B,H,W 001---00	CMONR [R] B,H,W 001---00	MTMCR [R/W] B,H,W 00001111	STMCR [R/W] B,H,W 0000-111	Clock generation/ Main timer/ Sub timer
0000 0514 <sub>H</sub>	PLLCR [R/W] B,H --000000 11110000		CSTBR [R/W] B -0000000	—	
0000 0518 <sub>H</sub>	WCRD [R] B,H --000000	WCRL [R/W] B,H --000000	WCCR [R,R/W] B 00--0000	—	Clock counter
0000 051C <sub>H</sub> to 0000 0BFC <sub>H</sub>	—				Reserved
0000 0C00 <sub>H</sub>	DCCR0 [R/W] W 0----000 --00--00 00000000 0-000000				DMAC
0000 0C04 <sub>H</sub>	DCSR0 [R,R/W] H 0----- -----000		DTCR0 [R/W] H 00000000 00000000		
0000 0C08 <sub>H</sub>	DSAR0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C0C <sub>H</sub>	DDAR0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C10 <sub>H</sub>	DCCR1 [R/W] W 0----000 --00--00 00000000 0-000000				
0000 0C14 <sub>H</sub>	DCSR1 [R,R/W] H 0----- -----000		DTCR1 [R/W] H 00000000 00000000		
0000 0C18 <sub>H</sub>	DSAR1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C1C <sub>H</sub>	DDAR1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C20 <sub>H</sub>	DCCR2 [R/W] W 0----000 --00--00 00000000 0-000000				
0000 0C24 <sub>H</sub>	DCSR2 [R,R/W] H 0----- -----000		DTCR2 [R/W] H 00000000 00000000		
0000 0C28 <sub>H</sub>	DSAR2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C2C <sub>H</sub>	DDAR2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C30 <sub>H</sub>	DCCR3 [R/W] W 0----000 --00--00 00000000 0-000000				
0000 0C34 <sub>H</sub>	DCSR3 [R,R/W] H 0----- -----000		DTCR3 [R/W] H 00000000 00000000		

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# MB91625 Series

Address	Register				Block
	+0	+1	+2	+3	
0000 0C38H	DSAR3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
0000 0C3CH	DDAR3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C40H	DCCR4 [R/W] W 0----000 --00--00 00000000 0-000000				
0000 0C44H	DCSR4 [R,R/W] H 0-----000		DTCR4 [R/W] H 00000000 00000000		
0000 0C48H	DSAR4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C4CH	DDAR4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C50H	DCCR5 [R/W] W 0----000 --00--00 00000000 0-000000				
0000 0C54H	DCSR5 [R,R/W] H 0-----000		DTCR5 [R/W] H 00000000 00000000		
0000 0C58H	DSAR5 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C5CH	DDAR5 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C60H	DCCR6 [R/W] W 0----000 --00--00 00000000 0-000000				
0000 0C64H	DCSR6 [R,R/W] H 0-----000		DTCR6 [R/W] H 00000000 00000000		
0000 0C68H	DSAR6 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C6CH	DDAR6 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C70H	DCCR7 [R/W] W 0----000 --00--00 00000000 0-000000				
0000 0C74H	DCSR7 [R,R/W] H 0-----000		DTCR7 [R/W] H 00000000 00000000		
0000 0C78H	DSAR7 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C7CH	DDAR7 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C80H to 0000 0DF0H	—				
0000 0DF4H	—		DILVR [R,R/W] B ---11111		

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# MB91625 Series

Address	Register				Block
	+0	+1	+2	+3	
0000 0DF8 <sub>H</sub>	DMACR [R/W] W 0-----0-----				DMAC
0000 0DFC <sub>H</sub> to 0000 0F3C <sub>H</sub>	—				Reserved
0000 0F40 <sub>H</sub>	BT4TMR [R] H 00000000 00000000		BT4TMCR [R/W] B,H -0000000 00000000		Base timer ch.4
0000 0F44 <sub>H</sub>	—	BT4STC [R/W] B 0000-000	—		
0000 0F48 <sub>H</sub>	BT4PCSR / BT4PRLL [R/W] H XXXXXXXX XXXXXXXX		BT4PDUT / BT4PRLH / BT4DTBF [R/W] H XXXXXXXX XXXXXXXX		
0000 0F4C <sub>H</sub>	—				
0000 0F50 <sub>H</sub>	BT5TMR [R] H 00000000 00000000		BT5TMCR [R/W] B,H -0000000 00000000		Base timer ch.5
0000 0F54 <sub>H</sub>	—	BT5STC [R/W] B 0000-000	—		
0000 0F58 <sub>H</sub>	BT5PCSR / BT5PRLL [R/W] H XXXXXXXX XXXXXXXX		BT5PDUT / BT5PRLH / BT5DTBF [R/W] H XXXXXXXX XXXXXXXX		
0000 0F5C <sub>H</sub>	—				
0000 0F60 <sub>H</sub>	BT6TMR [R] H 00000000 00000000		BT6TMCR [R/W] B,H -0000000 00000000		Base timer ch.6
0000 0F64 <sub>H</sub>	—	BT6STC [R/W] B 0000-000	—		
0000 0F68 <sub>H</sub>	BT6PCSR / BT6PRLL [R/W] H XXXXXXXX XXXXXXXX		BT6PDUT / BT6PRLH / BT6DTBF [R/W] H XXXXXXXX XXXXXXXX		
0000 0F6C <sub>H</sub>	—				
0000 0F70 <sub>H</sub>	BT7TMR [R] H 00000000 00000000		BT7TMCR [R/W] B,H -0000000 00000000		Base timer ch.7
0000 0F74 <sub>H</sub>	—	BT7STC [R/W] B 0000-000	—		
0000 0F78 <sub>H</sub>	BT7PCSR / BT7PRLL [R/W] H XXXXXXXX XXXXXXXX		BT7PDUT / BT7PRLH / BT7DTBF [R/W] H XXXXXXXX XXXXXXXX		
0000 0F7C <sub>H</sub>	BTSEL4567 [R/W] B 00000000	—			

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# MB91625 Series

Address	Register				Block
	+0	+1	+2	+3	
0000 0F80 <sub>H</sub>	BT8TMR [R] H 00000000 00000000		BT8TMCR [R/W] B,H -0000000 00000000		Base timer ch.8
0000 0F84 <sub>H</sub>	—	BT8STC [R/W] B 0000-000	—		
0000 0F88 <sub>H</sub>	BT8PCSR / BT8PRLL [R/W] H XXXXXXXX XXXXXXXX		BT8PDUT / BT8PRLH / BT8DTBF [R/W] H XXXXXXXX XXXXXXXX		
0000 0F8C <sub>H</sub>	—				
0000 0F90 <sub>H</sub>	BT9TMR [R] H 00000000 00000000		BT9TMCR [R/W] B,H -0000000 00000000		Base timer ch.9
0000 0F94 <sub>H</sub>	—	BT9STC [R/W] B 0000-000	—		
0000 0F98 <sub>H</sub>	BT9PCSR / BT9PRLL [R/W] H XXXXXXXX XXXXXXXX		BT9PDUT / BT9PRLH / BT9DTBF [R/W] H XXXXXXXX XXXXXXXX		
0000 0F9C <sub>H</sub>	—				
0000 0FA0 <sub>H</sub>	BTATMR [R] H 00000000 00000000		BTATMCR [R/W] B,H -0000000 00000000		Base timer ch.10
0000 0FA4 <sub>H</sub>	—	BTASTC [R/W] B 0000-000	—		
0000 0FA8 <sub>H</sub>	BTAPCSR / BTAPRLL [R/W] H XXXXXXXX XXXXXXXX		BTAPDUT / BTAPRLH / BTADTBF [R/W] H XXXXXXXX XXXXXXXX		
0000 0FAC <sub>H</sub>	—				
0000 0FB0 <sub>H</sub>	BTBTMR [R] H 00000000 00000000		BTBTMCR [R/W] B,H -0000000 00000000		Base timer ch.11
0000 0FB4 <sub>H</sub>	—	BTBSTC [R/W] B 0000-000	—		
0000 0FB8 <sub>H</sub>	BTBPCSR / BTBPRLL [R/W] H XXXXXXXX XXXXXXXX		BTBPDUT / BTBPRLH / BTBDTBF [R/W] H XXXXXXXX XXXXXXXX		
0000 0FBC <sub>H</sub>	BTSEL89AB [R/W] B 00000000	—			

(Continued)

# MB91625 Series

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
0000 0FC0 <sub>H</sub>	BTCTMR [R] H 00000000 00000000		BTCTMCR [R/W] B,H -00000000 00000000		Base timer ch.12
0000 0FC4 <sub>H</sub>	—	BTCSTC [R/W] B 0000-000	—		
0000 0FC8 <sub>H</sub>	BTCPCSR / BTCPRLL [R/W] H XXXXXXXX XXXXXXXX		BTCPDUT / BTCPR LH / BTCDTBF [R/W] H XXXXXXXX XXXXXXXX		
0000 0FCC <sub>H</sub>	—				
0000 0FD0 <sub>H</sub>	BDTMR [R] H 00000000 00000000		BDTMCR [R/W] B,H -00000000 00000000		Base timer ch.13
0000 0FD4 <sub>H</sub>	—	BDSTC [R/W] B 0000-000	—		
0000 0FD8 <sub>H</sub>	BDPCSR / BDPRLL [R/W] H XXXXXXXX XXXXXXXX		BDPDUT / BDPR LH / BDDBTF [R/W] H XXXXXXXX XXXXXXXX		
0000 0FDC <sub>H</sub>	—				
0000 0FE0 <sub>H</sub>	BETMR [R] H 00000000 00000000		BETMCR [R/W] B,H -00000000 00000000		Base timer ch.14
0000 0FE4 <sub>H</sub>	—	BESTC [R/W] B 0000-000	—		
0000 0FE8 <sub>H</sub>	BTEPCSR / BTEPRLL [R/W] H XXXXXXXX XXXXXXXX		BTEPDUT / BTEPR LH / BTEDTBF [R/W] H XXXXXXXX XXXXXXXX		
0000 0FEC <sub>H</sub>	—				
0000 0FF0 <sub>H</sub>	BTFTMR [R] H 00000000 00000000		BTFTMCR [R/W] B,H -00000000 00000000		Base timer ch.15
0000 0FF4 <sub>H</sub>	—	BTFSTC [R/W] B 0000-000	—		
0000 0FF8 <sub>H</sub>	BTFPCSR / BTFPRLL [R/W] H XXXXXXXX XXXXXXXX		BTFPDUT / BTFPR LH / BTFDTBF [R/W] H XXXXXXXX XXXXXXXX		
0000 0FFC <sub>H</sub>	BTSELCDEF [R/W] B 00000000	—	BTSSSR [W] H XXXXXXXX XXXXXXXX		
0000 1000 <sub>H</sub> to 0000 FFFC <sub>H</sub>	—				

\*1 : Byte access is available only when accessing the lower 8 bits within 9 bits.

\*2 : The register of I<sup>2</sup>C can not be read immediate after reset.

\*3 : Value just after reset by  $\overline{\text{INIT}}$  pin.

Do not access the reserved areas.

## ■ VECTOR TABLE

Interrupt source (Peripheral resource)	Interrupt number		Interrupt level setting register	Offset	Address of TBR default
	Decimal	Hexa-decimal			
Reset	0	00	—	3FC <sub>H</sub>	000F FFFC <sub>H</sub>
System reserved	1	01	—	3F8 <sub>H</sub>	000F FFF8 <sub>H</sub>
System reserved	2	02	—	3F4 <sub>H</sub>	000F FFF4 <sub>H</sub>
System reserved	3	03	—	3F0 <sub>H</sub>	000F FFF0 <sub>H</sub>
System reserved	4	04	—	3EC <sub>H</sub>	000F FFEC <sub>H</sub>
System reserved	5	05	—	3E8 <sub>H</sub>	000F FFE8 <sub>H</sub>
System reserved	6	06	—	3E4 <sub>H</sub>	000F FFE4 <sub>H</sub>
System reserved	7	07	—	3E0 <sub>H</sub>	000F FFE0 <sub>H</sub>
System reserved	8	08	—	3DC <sub>H</sub>	000F FFDC <sub>H</sub>
INTE instruction	9	09	—	3D8 <sub>H</sub>	000F FFD8 <sub>H</sub>
System reserved	10	0A	—	3D4 <sub>H</sub>	000F FFD4 <sub>H</sub>
System reserved	11	0B	—	3D0 <sub>H</sub>	000F FFD0 <sub>H</sub>
Step trace trap	12	0C	—	3CC <sub>H</sub>	000F FFCC <sub>H</sub>
System reserved	13	0D	—	3C8 <sub>H</sub>	000F FFC8 <sub>H</sub>
Undefined instruction exception	14	0E	—	3C4 <sub>H</sub>	000F FFC4 <sub>H</sub>
—	15	0F	15(F <sub>H</sub> ) fixed	3C0 <sub>H</sub>	000F FFC0 <sub>H</sub>
External interrupt request ch.0 to ch.7	16	10	ICR00	3BC <sub>H</sub>	000F FFBC <sub>H</sub>
External interrupt request ch.8 to ch.15	17	11	ICR01	3B8 <sub>H</sub>	000F FFB8 <sub>H</sub>
External interrupt request ch.16 to ch.23	18	12	ICR02	3B4 <sub>H</sub>	000F FFB4 <sub>H</sub>
External interrupt request ch.24 to ch.31	19	13	ICR03	3B0 <sub>H</sub>	000F FFBO <sub>H</sub>
16-bit reload timer ch.0 to ch.2	20	14	ICR04	3AC <sub>H</sub>	000F FFAC <sub>H</sub>
Reception interrupt request of UART/CSIO ch.0	21	15	ICR05	3A8 <sub>H</sub>	000F FFA8 <sub>H</sub>
Transmission interrupt request of UART/CSIO ch.0 Transmission bus idle interrupt request of UART/CSIO ch.0	22	16	ICR06	3A4 <sub>H</sub>	000F FFA4 <sub>H</sub>
Reception interrupt request of UART/CSIO/ I <sup>2</sup> C ch.1	23	17	ICR07	3A0 <sub>H</sub>	000F FFA0 <sub>H</sub>
Transmission interrupt request of UART/CSIO/ I <sup>2</sup> C ch.1 Transmission bus idle interrupt request of UART/CSIO ch.1	24	18	ICR08	39C <sub>H</sub>	000F FF9C <sub>H</sub>
Status interrupt request of I <sup>2</sup> C ch.1	25	19	ICR09	398 <sub>H</sub>	000F FF98 <sub>H</sub>
Reception interrupt request of UART/CSIO/I <sup>2</sup> C ch.2	26	1A	ICR10	394 <sub>H</sub>	000F FF94 <sub>H</sub>
Transmission interrupt request of UART/CSIO/I <sup>2</sup> C ch.2 Transmission bus idle interrupt request of UART/CSIO ch.2	27	1B	ICR11	390 <sub>H</sub>	000F FF90 <sub>H</sub>

(Continued)

# MB91625 Series

Interrupt source (Peripheral resource)	Interrupt number		Interrupt level setting register	Offset	Address of TBR default
	Decimal	Hexa-decimal			
Status interrupt request of I <sup>2</sup> C ch.2	28	1C	ICR12	38C <sub>H</sub>	000F FF8C <sub>H</sub>
Reception interrupt request of UART/CSIO/I <sup>2</sup> C ch.3	29	1D	ICR13	388 <sub>H</sub>	000F FF88 <sub>H</sub>
Transmission interrupt request of UART/CSIO/I <sup>2</sup> C ch.3 Transmission bus idle interrupt request of UART/CSIO ch.3 Status interrupt request of I <sup>2</sup> C ch.3	30	1E	ICR14	384 <sub>H</sub>	000F FF84 <sub>H</sub>
Reception interrupt request of UART/CSIO/I <sup>2</sup> C ch.4	31	1F	ICR15	380 <sub>H</sub>	000F FF80 <sub>H</sub>
Transmission interrupt request of UART/CSIO/I <sup>2</sup> C ch.4 Transmission bus idle interrupt request of UART/CSIO ch.4 Status interrupt request of I <sup>2</sup> C ch.4	32	20	ICR16	37C <sub>H</sub>	000F FF7C <sub>H</sub>
Reception interrupt request of UART/CSIO/I <sup>2</sup> C ch.5	33	21	ICR17	378 <sub>H</sub>	000F FF78 <sub>H</sub>
Transmission interrupt request of UART/CSIO/I <sup>2</sup> C ch.5 Transmission bus idle interrupt request of UART/CSIO ch.5 Status interrupt request of I <sup>2</sup> C ch.5	34	22	ICR18	374 <sub>H</sub>	000F FF74 <sub>H</sub>
Reception interrupt request of UART/CSIO/ I <sup>2</sup> C ch.6	35	23	ICR19	370 <sub>H</sub>	000F FF70 <sub>H</sub>
Transmission interrupt request of UART/CSIO/I <sup>2</sup> C ch.6 Transmission bus idle interrupt request of UART/CSIO ch.6 Status interrupt request of I <sup>2</sup> C ch.6	36	24	ICR20	36C <sub>H</sub>	000F FF6C <sub>H</sub>
Reception interrupt request of UART/CSIO/I <sup>2</sup> C ch.7 32-bit input capture ch.4 to ch.7	37	25	ICR21	368 <sub>H</sub>	000F FF68 <sub>H</sub>
Transmission interrupt request of UART/CSIO/I <sup>2</sup> C ch.7 Transmission bus idle interrupt request of UART/CSIO ch.7 Status interrupt request of I <sup>2</sup> C ch.7 32-bit output compare ch.4 to ch.7	38	26	ICR22	364 <sub>H</sub>	000F FF64 <sub>H</sub>
Reception interrupt request of UART/CSIO/I <sup>2</sup> C ch.8 to ch.11 Transmission interrupt request of UART/CSIO/I <sup>2</sup> C ch.8 to ch.11 Transmission bus idle interrupt request of UART/CSIO ch.8 to ch.11 Transmission FIFO interrupt request UART/CSIO/I <sup>2</sup> C ch.8 to ch.11 Status interrupt request of I <sup>2</sup> C ch.8 to ch.11	39	27	ICR23	360 <sub>H</sub>	000F FF60 <sub>H</sub>
16-bit up/down counter ch.0 to ch.3	40	28	ICR24	35C <sub>H</sub>	000F FF5C <sub>H</sub>
Main timer/Sub timer/Watch counter	41	29	ICR25	358 <sub>H</sub>	000F FF58 <sub>H</sub>
10-bit A/D converter <ul style="list-style-type: none"> <li>• Scan conversion interrupt request</li> <li>• Priority conversion interrupt request</li> <li>• FIFO overrun interrupt request</li> <li>• Conversion result compare interrupt request</li> </ul>	42	2A	ICR26	354 <sub>H</sub>	000F FF54 <sub>H</sub>
32-bit free run timer ch.0, ch.1	43	2B	ICR27	350 <sub>H</sub>	000F FF50 <sub>H</sub>
32-bit input capture ch.0 to ch.3	44	2C	ICR28	34C <sub>H</sub>	000F FF4C <sub>H</sub>
32-bit output compare ch.0 to ch.3	45	2D	ICR29	348 <sub>H</sub>	000F FF48 <sub>H</sub>

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Interrupt source (Peripheral resource)	Interrupt number		Interrupt level setting register	Offset	Address of TBR default
	Decimal	Hexa-decimal			
Base timer ch.0	46	2E	ICR30	344 <sub>H</sub>	000F FF44 <sub>H</sub>
Base timer ch.1	47	2F	ICR31	340 <sub>H</sub>	000F FF40 <sub>H</sub>
Base timer ch.2	48	30	ICR32	33C <sub>H</sub>	000F FF3C <sub>H</sub>
Base timer ch.3	49	31	ICR33	338 <sub>H</sub>	000F FF38 <sub>H</sub>
Base timer ch.4, ch.5	50	32	ICR34	334 <sub>H</sub>	000F FF34 <sub>H</sub>
Base timer ch.6, ch.7	51	33	ICR35	330 <sub>H</sub>	000F FF30 <sub>H</sub>
Base timer ch.8, ch.9	52	34	ICR36	32C <sub>H</sub>	000F FF2C <sub>H</sub>
Base timer ch.10, ch.11	53	35	ICR37	328 <sub>H</sub>	000F FF28 <sub>H</sub>
Base timer ch.12	54	36	ICR38	324 <sub>H</sub>	000F FF24 <sub>H</sub>
Base timer ch.13	55	37	ICR39	320 <sub>H</sub>	000F FF20 <sub>H</sub>
Base timer ch.14, ch.15	56	38	ICR40	31C <sub>H</sub>	000F FF1C <sub>H</sub>
DMA controller (DMAC) ch.0	57	39	ICR41	318 <sub>H</sub>	000F FF18 <sub>H</sub>
DMA controller (DMAC) ch.1	58	3A	ICR42	314 <sub>H</sub>	000F FF14 <sub>H</sub>
DMA controller (DMAC) ch.2	59	3B	ICR43	310 <sub>H</sub>	000F FF10 <sub>H</sub>
DMA controller (DMAC) ch.3	60	3C	ICR44	30C <sub>H</sub>	000F FF0C <sub>H</sub>
DMA controller (DMAC) ch.4 to ch.7	61	3D	ICR45	308 <sub>H</sub>	000F FF08 <sub>H</sub>
System reserved	62	3E	ICR46	304 <sub>H</sub>	000F FF04 <sub>H</sub>
Delay interrupt	63	3F	ICR47	300 <sub>H</sub>	000F FF00 <sub>H</sub>
System reserved (Used by REALOS)	64	40	—	2FC <sub>H</sub>	000F FEF C <sub>H</sub>
System reserved (Used by REALOS)	65	41	—	2F8 <sub>H</sub>	000F FEF 8 <sub>H</sub>
Used by INT instruction	66 to 255	42 to FF	—	2F4 <sub>H</sub> to 000 <sub>H</sub>	000F FEF 4 <sub>H</sub> to 000F FC00 <sub>H</sub>

## ■ PIN STATUS IN EACH CPU STATE

The terms used for pin status have the following meanings.

- When  $\overline{\text{INIT}}$  = "L"

This is the period when the  $\overline{\text{INIT}}$  pin is the "L" level.

- When  $\overline{\text{INIT}}$  = "H"

The status immediately after the  $\overline{\text{INIT}}$  pin changes from the "L" level to the "H" level.

- SLVL1

This bit is a standby level setting bit in the standby mode control register (STBCR).

- Input enabled

Indicates that the input function can be used.

- Input disabled

Indicates that the input function cannot be used.

- Output Hi-Z

Indicates that the output drive transistor is disabled and the pin is put in the Hi-Z state.

- Maintain previous state

Maintains the state that was being output immediately prior to entering the current mode.

If a built-in peripheral function is operating, the output follows the peripheral function.

If the pin is being used as a port, that output is maintained.

- Internal input fixed at "0"

The input gate connected to the pin is disconnected from the external input and internally connected to "0".

- Input enabled when interrupt function selected and enabled

Inputs are allowed only when the pin is configured as an external interrupt request input pin and the external interrupt request is enabled.

• List of pin status

Pin name	Function name	Initial Value		Sleep Mode	Standby Mode	
		$\overline{\text{INIT}}$ = "L" Period	$\overline{\text{INIT}}$ = "H" Period		SLVL1 = 0	SLVL1 = 1
$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	—	—	Input enabled	Input enabled	Input enabled
X0	X0	Input enabled	Input enabled		Hi-Z or Input enabled	Hi-Z or Input enabled
X1	X1	Input enabled	Input enabled		"H" output or Input enabled	"H" output or Input enabled
X0A	X0A (When $\overline{\text{INIT}}$ input, see PK1. When port selected, input disabled)	Input disabled	Input disabled		Hi-Z or Input enabled	Hi-Z or Input enabled
X1A	X1A (When $\overline{\text{INIT}}$ input, see PK0. When port selected, input disabled)	Input disabled	Input disabled		"H" output or Input enabled	"H" output or Input enabled
MD0	MD0	Input enabled	Input enabled		Input enabled	Input enabled
MD1	MD1	Input enabled	Input enabled			
P00	P00/TIOA0/SOUT0_1/IN0	Output Hi-Z	Output Hi-Z/Input enabled	Last state maintained	Last state maintained	Output Hi-Z/Internal input "0" fixed
P01	P01/TIOB0/SIN0_1/IN1					
P02	P02/TIOA1/SCK0_1/IN2					
P03	P03/TIOB1/IN3					
P04	P04/TIOA2/SOUT1/IN4					
P05	P05/TIOB2/SIN1/IN5					
P06	P06/TIOA3/SCK1/IN6					
P07	P07/TIOB3/IN7					
P10	P10/TIOA4/SOUT2/AIN0/INT0	Output Hi-Z	Output Hi-Z/Input enabled	Last state maintained	Last state maintained	Output Hi-Z/Internal input "0" fixed Input enabled when the selection of interrupt function is enabled
P11	P11/TIOB4/SIN2/BIN0/INT1					
P12	P12/TIOA5/SCK2/ZIN0/INT2					
P13	P13/TIOB5/INT3					
P14	P14/TIOA6/SOUT3/AIN1/INT4					
P15	P15/TIOB6/SIN3/BIN1/INT5					
P16	P16/TIOA7/SCK3/ZIN1/INT6					
P17	P17/TIOB7/INT7					

(Continued)

# MB91625 Series

Pin name	Function name	Initial Value		Sleep Mode	Standby Mode	
		$\overline{\text{INIT}} = \text{"L"}$ Period	$\overline{\text{INIT}} = \text{"H"}$ Period		SLVL1 = 0	SLVL1 = 1
P20	P20/TIOA8/SOUT4/AIN2	Output Hi-Z	Output Hi-Z/Input enabled	Last state maintained	Last state maintained	Output Hi-Z/Internal in- put "0" fixed
P21	P21/TIOB8/SIN4/BIN2					
P22	P22/TIOA9/SCK4/ZIN2					
P23	P23/TIOB9					
P24	P24/TIOA10/SOUT5/AIN3/OUT0					
P25	P25/TIOB10/SIN5/BIN3/OUT1					
P26	P26/TIOA11/SCK5/ZIN3/OUT2					
P27	P27/TIOB11/OUT3					
P30	P30/TIOA12/SOUT6/INT8	Output Hi-Z	Output Hi-Z/Input enabled	Last state maintained	Last state maintained	Output Hi-Z/Internal in- put "0" fixed  Input enabled when the selection of interrupt func- tion is enabled
P31	P31/TIOB12/SIN6/INT9					
P32	P32/TIOA13/SCK6/INT10					
P33	P33/TIOB13/INT11					
P34	P34/TIOA14/SOUT7/OUT4/ INT12					
P35	P35/TIOB14/SIN7/OUT5/INT13					
P36	P36/TIOA15/SCK7/OUT6/INT14					
P37	P37/TIOB15/OUT7/INT15					
P40	P40/SOUT8	Output Hi-Z	Output Hi-Z/Input enabled	Last state maintained	Last state maintained	Output Hi-Z/Internal in- put "0" fixed
P41	P41/SIN8					
P42	P42/SCK8					
P43	P43					
P44	P44/SOUT9					
P45	P45/SIN9					
P46	P46/SCK9					
P47	P47					

(Continued)

Pin name	Function name	Initial Value		Sleep Mode	Standby Mode		
		$\overline{\text{INIT}} = \text{"L"}$ Period	$\overline{\text{INIT}} = \text{"H"}$ Period		SLVL1 = 0	SLVL1 = 1	
P50	P50/SOUT10/AIN0_1	Output Hi-Z	Output Hi-Z/Input enabled	Last state maintained	Last state maintained	Output Hi-Z/Internal input "0" fixed	
P51	P51/SIN10/BIN0_1						
P52	P52/SCK10/ZIN0_1						
P53	P53/FRCK1/INT21_2					Input enabled when the selec- tion of interrupt function is enabled	
P54	P54/SOUT11/AIN1_1						Output Hi-Z/Internal input "0" fixed
P55	P55/SIN11/BIN1_1/ADTRG0						Output Hi-Z/Internal input "0" fixed
P56	P56/SCK11/ZIN1_1/FRCK0						
P57	P57						

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# MB91625 Series

Pin name	Function name	Initial Value		Sleep Mode	Standby Mode	
		INIT = "L" Period	INIT = "H" Period		SLVL1 = 0	SLVL1 = 1
P60	P60/AIN2_1	Output Hi-Z	Output Hi-Z/ Input enabled	Last state maintained or Input enabled	Last state maintained	Output Hi-Z/ Internal input "0" fixed
P61	P61/BIN2_1					
P62	P62/ZIN2_1					
P63	P63/FRCK1_1/INT22_2					Input enabled when the selection of interrupt function is enabled
P64	P64/AIN3_1					
P65	P65/BIN3_1/ADTRG0_1					
P66	P66/ZIN3_1/FRCK0_1					
P67	P67/INT23_2	Output Hi-Z/ Internal input "0" fixed	Input enabled when the selection of interrupt function is enabled			
P70	P70/AN0/OUT0_1/INT16					
P71	P71/AN1/OUT1_1/INT17	Output Hi-Z	Output Hi-Z/ Input disabled	Last state maintained	Last state maintained	Output Hi-Z/ Internal input "0" fixed
P72	P72/AN2/TMO0/OUT2_1/INT18					
P73	P73/AN3/TMO1/OUT3_1/INT19					
P74	P74/AN4/TMO2/OUT4_1/INT20					
P75	P75/AN5/SOUT0/TMI0/OUT5_1/ INT21					
P76	P76/AN6/SIN0/TMI1/OUT6_1/ INT22					
P77	P77/AN7/SCK0/TMI2/OUT7_1/ INT23					

(Continued)

(Continued)

Pin name	Function name	Initial Value		Sleep Mode	Standby Mode	
		$\overline{\text{INIT}} = \text{"L"}$ Period	$\overline{\text{INIT}} = \text{"H"}$ Period		SLVL1 = 0	SLVL1 = 1
P80	P80/AN8/IN0_1/INT24	Output Hi-Z	Output Hi-Z/Input disabled	Last state maintained	Last state maintained	Output Hi-Z/ Internal input "0" fixed  Input enabled when the selection of interrupt function is enabled
P81	P81/AN9/IN1_1/INT25					
P82	P82/AN10/IN2_1/INT26					
P83	P83/AN11/IN3_1/INT27					
P84	P84/AN12/IN4_1/INT28					
P85	P85/AN13/IN5_1/INT29					
P86	P86/AN14/IN6_1/INT30					
P87	P87/AN15/IN7_1/INT31					
P90	P90/DA0	Output Hi-Z	Output Hi-Z/Input enabled	Last state maintained	Last state maintained	Output Hi-Z/ Internal input "0" fixed
P91	P91/DA1					
P92	P92					
PA0	PA0/INT16_1	Output Hi-Z	Output Hi-Z/Input disabled	Last state maintained	Last state maintained	Output Hi-Z/ Internal input "0" fixed  Input enabled when the selection of interrupt function is enabled
PA1	PA1/INT17_1					
PA2	PA2/TMO0_1/INT18_1					
PA3	PA3/TMO1_1/INT19_1					
PA4	PA4/TMO2_1/INT20_1					
PA5	PA5/TMI0_1/INT21_1					
PA6	PA6/TMI1_1/INT22_1					
PA7	PA7/TMI2_1/INT23_1					
PK0	PK0	Output Hi-Z	Internal input "0" fixed	Last state maintained	Last state maintained	Output Hi-Z/ Internal input "0" fixed
PK1	PK1		Output Hi-Z/Input enabled			
PK2	PK2/ADTRG0_2					

# MB91625 Series

- List of pin status (serial write mode)

Pin name	Function name	During initialization	During asynchronous write operation	During synchronous write operation
		$\overline{\text{INIT}} = \text{"L"}$	$\overline{\text{INIT}} = \text{"H"}$	
$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	—	—	—
X0	X0	Input enabled	Input enabled	Input enabled
X1	X1	Input enabled	Input enabled	Input enabled
X0A	X0A (When $\overline{\text{INIT}}$ input, see PK1. When port selected, input disabled)	Input disabled	Input disabled	Input disabled
X1A	X1A (When $\overline{\text{INIT}}$ input, see PK0. When port selected, input disabled)	Input disabled	Input disabled	Input disabled
MD0	MD0	Input enabled	Input enabled	Input enabled
MD1	MD1	Input enabled	Input enabled	Input enabled
P00	P00/TIOA0/SOUT0_1/IN0	Output Hi-Z	Output Hi-Z/Input enabled	Output Hi-Z/Input enabled
P01	P01/TIOB0/SIN0_1/IN1			
P02	P02/TIOA1/SCK0_1/IN2			
P03	P03/TIOB1/IN3			
P04	P04/TIOA2/SOUT1/IN4			
P05	P05/TIOB2/SIN1/IN5			
P06	P06/TIOA3/SCK1/IN6			
P07	P07/TIOB3/IN7			
P10	P10/TIOA4/SOUT2/AIN0/INT0	Output Hi-Z	Output Hi-Z/Input enabled	Output Hi-Z/Input enabled
P11	P11/TIOB4/SIN2/BIN0/INT1			
P12	P12/TIOA5/SCK2/ZIN0/INT2			
P13	P13/TIOB5/INT3			
P14	P14/TIOA6/SOUT3/AIN1/INT4			
P15	P15/TIOB6/SIN3/BIN1/INT5			
P16	P16/TIOA7/SCK3/ZIN1/INT6			
P17	P17/TIOB7/INT7			

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# MB91625 Series

Pin name	Function name	During initialization	During asynchronous write operation	During synchronous write operation
		$\overline{\text{INIT}} = \text{"L"}$	$\overline{\text{INIT}} = \text{"H"}$	
P20	P20/TIOA8/SOUT4/AIN2	Output Hi-Z	Output Hi-Z/Input enabled	Output Hi-Z/Input enabled
P21	P21/TIOB8/SIN4/BIN2			
P22	P22/TIOA9/SCK4/ZIN2			
P23	P23/TIOB9			
P24	P24/TIOA10/SOUT5/AIN3/OUT0			
P25	P25/TIOB10/SIN5/BIN3/OUT1			
P26	P26/TIOA11/SCK5/ZIN3/OUT2			
P27	P27/TIOB11/OUT3			
P30	P30/TIOA12/SOUT6/INT8	Output Hi-Z	Output Hi-Z/Input enabled	Output Hi-Z/Input enabled
P31	P31/TIOB12/SIN6/INT9			
P32	P32/TIOA13/SCK6/INT10			
P33	P33/TIOB13/INT11			
P34	P34/TIOA14/SOUT7/OUT4/ INT12			
P35	P35/TIOB14/SIN7/OUT5/INT13			
P36	P36/TIOA15/SCK7/OUT6/INT14			
P37	P37/TIOB15/OUT7/INT15			
P40	P40/SOUT8	Output Hi-Z	Output Hi-Z/Input enabled	Output Hi-Z/Input enabled
P41	P41/SIN8			
P42	P42/SCK8			
P43	P43			
P44	P44/SOUT9			
P45	P45/SIN9			
P46	P46/SCK9			
P47	P47			
P50	P50/SOUT10/AIN0_1	Output Hi-Z	Output Hi-Z/Input enabled	Output Hi-Z/Input enabled
P51	P51/SIN10/BIN0_1			
P52	P52/SCK10/ZIN0_1			
P53	P53/FRCK1/INT21_2			
P54	P54/SOUT11/AIN1_1			
P55	P55/SIN11/BIN1_1/ADTRG0			
P56	P56/SCK11/ZIN1_1/FRCK0			
P57	P57			

(Continued)

# MB91625 Series

Pin name	Function name	During initialization	During asynchronous write operation	During synchronous write operation
		$\overline{\text{INIT}} = \text{"L"}$	$\overline{\text{INIT}} = \text{"H"}$	
P60	P60/AIN2_1	Output Hi-Z	Output Hi-Z/Input enabled	Output Hi-Z/Input enabled
P61	P61/BIN2_1			
P62	P62/ZIN2_1			
P63	P63/FRCK1_1/INT22_2			
P64	P64/AIN3_1			
P65	P65/BIN3_1/ADTRG0_1			
P66	P66/ZIN3_1/FRCK0_1			
P67	P67/INT23_2	Output Hi-Z	Output Hi-Z/Input disabled	Output Hi-Z/Input disabled
P70	P70/AN0/OUT0_1/INT16			
P71	P71/AN1/OUT1_1/INT17			
P72	P72/AN2/TMO0/OUT2_1/INT18			
P73	P73/AN3/TMO1/OUT3_1/INT19			
P74	P74/AN4/TMO2/OUT4_1/INT20			
P75	P75/AN5/SOUT0/TMI0/OUT5_1/ INT21			
P76	P76/AN6/SIN0/TMI1/OUT6_1/ INT22	Output Hi-Z	Output Hi-Z/ Input enabled	Output Hi-Z/ Input enabled
P77	P77/AN7/SCK0/TMI2/OUT7_1/ INT23		Output Hi-Z/ Input disabled	Output Hi-Z/ Input disabled
P80	P80/AN8/IN0_1/INT24	Output Hi-Z	Output Hi-Z/Input disabled	Output Hi-Z/Input disabled
P81	P81/AN9/IN1_1/INT25			
P82	P82/AN10/IN2_1/INT26			
P83	P83/AN11/IN3_1/INT27			
P84	P84/AN12/IN4_1/INT28			
P85	P85/AN13/IN5_1/INT29			
P86	P86/AN14/IN6_1/INT30			
P87	P87/AN15/IN7_1/INT31	Output Hi-Z	Output Hi-Z/Input enabled	Output Hi-Z/Input enabled
P90	P90/DA0			
P91	P91/DA1			
P92	P92			

(Continued)

(Continued)

Pin name	Function name	During initialization	During asynchronous write operation	During synchronous write operation
		$\overline{\text{INIT}} = \text{"L"}$	$\overline{\text{INIT}} = \text{"H"}$	
PA0	PA0/INT16_1	Output Hi-Z	Output Hi-Z/Input disabled	Output Hi-Z/Input disabled
PA1	PA1/INT17_1			
PA2	PA2/TMO0_1/INT18_1			
PA3	PA3/TMO1_1/INT19_1			
PA4	PA4/TMO2_1/INT20_1			
PA5	PA5/TMI0_1/INT21_1			
PA6	PA6/TMI1_1/INT22_1			
PA7	PA7/TMI2_1/INT23_1			
PK0	PK0	Output Hi-Z	Output Hi-Z/Input disabled	Output Hi-Z/Input disabled
PK1	PK1			
PK2	PK2/ADTRG0_2		Output Hi-Z/Input enabled	Output Hi-Z/Input enabled

# MB91625 Series

## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1, *2	V <sub>CC</sub>	V <sub>SS</sub> – 0.3	V <sub>SS</sub> + 4.0	V	
Analog power supply voltage*1, *3	AV <sub>CC</sub>	V <sub>SS</sub> – 0.3	V <sub>SS</sub> + 4.0	V	
Analog reference voltage*1, *3	AVRH	V <sub>SS</sub> – 0.3	V <sub>SS</sub> + 4.0	V	
Input voltage*1	V <sub>I</sub>	V <sub>SS</sub> – 0.3	V <sub>CC</sub> + 0.3 (≤ 4.0)	V	*7
		V <sub>SS</sub> – 0.3	V <sub>SS</sub> + 6.0	V	5 V tolerant
Analog pin input voltage*1	V <sub>IA</sub>	V <sub>SS</sub> – 0.3	V <sub>SS</sub> + 4.0	V	
Output voltage*1	V <sub>O</sub>	V <sub>SS</sub> – 0.3	V <sub>CC</sub> + 0.3	V	
Maximum clamp current	I <sub>CLAMP</sub>	– 4	+ 4	mA	*8
Total maximum clamp current	Σ I <sub>CLAMP</sub>	—	40	mA	*8
“L” level maximum output current*4	I <sub>OL</sub>	—	10	mA	
“L” level average output current*5	I <sub>OLAV</sub>	—	4	mA	
“L” level total maximum output current	ΣI <sub>OL</sub>	—	100	mA	
“L” level total average output current*6	ΣI <sub>OLAV</sub>	—	50	mA	
“H” level maximum output current*4	I <sub>OH</sub>	—	– 10	mA	
“H” level average output current*5	I <sub>OHAV</sub>	—	– 4	mA	
“H” level total maximum output current	ΣI <sub>OH</sub>	—	– 100	mA	
“H” level total average output current*6	ΣI <sub>OHAV</sub>	—	– 50	mA	
Power consumption (Flash product)	P <sub>D</sub>	—	500	mW	
Power consumption (MASK product)	P <sub>D</sub>	—	350	mW	
Operating temperature	T <sub>a</sub>	– 40	+ 85	°C	
Storage temperature	T <sub>STG</sub>	– 55	+ 125	°C	

\*1 : The parameter is based on V<sub>SS</sub> = AV<sub>SS</sub> = 0.0 V.

\*2 : V<sub>CC</sub> must not drop below V<sub>SS</sub> – 0.3 V.

\*3 : Be careful not to exceed V<sub>CC</sub> + 0.3 V, for example, when the power is turned on.

\*4 : The maximum output current is the peak value for a single pin.

\*5 : The average output is the average current for a single pin over a period of 100 ms.

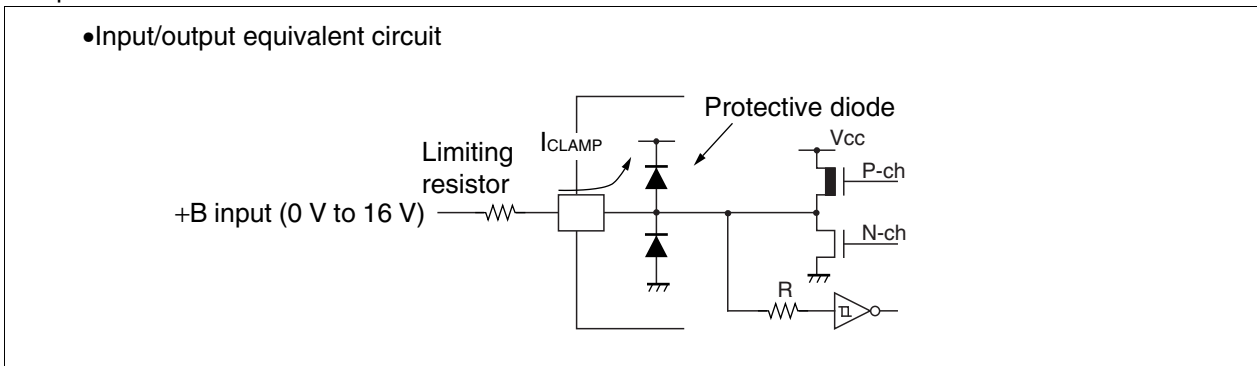
\*6 : The total average output current is the average current for all pins over a period of 100 ms.

\*7 : If the input current or the maximum input current are limited by some means with external components, the I<sub>CLAMP</sub> rating supersedes the V<sub>I</sub> rating.

(Continued)

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- \*8 :
- Corresponding pins:P14 to P17,P50 to P57, P60 to P62, P67, PK2
  - Use within recommended operating conditions.
  - Use at DC voltage (current).
  - The +B signal should always be applied by connecting a limiting resistor between the +B signal and the microcontroller.
  - The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed rated values at any time regardless of instantaneously or constantly when the +B signal is input.
  - Note that when the microcontroller drive current is low, such as in the low power consumption modes, the +B input potential can increase the potential at the  $V_{CC}$  pin via a protective diode, possibly affecting other devices.
  - Note that if the +B signal is input when the microcontroller is off (not fixed at 0V), since the power is supplied through the pin, the microcontroller may operate incompletely.
  - Do not leave +B input pins open.
  - Sample recommended circuit



**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

# MB91625 Series

## 2. Recommended Operating Conditions

( $V_{SS} = AV_{SS} = 0.0\text{ V}$ )

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	$V_{CC}$	2.7	3.6	V	
Analog power supply voltage	$AV_{CC}$	2.7	3.6	V	$AV_{CC} \leq V_{CC}$
Analog reference voltage	$AV_{RH}$	$AV_{SS}$	$AV_{CC}$	V	
Operating temperature	$T_a$	- 40	+ 85	°C	

**WARNING:** The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

## 3. DC Characteristics

( $V_{CC} = AV_{CC} = 2.7\text{ V}$  to  $3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_a = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Powersupply current (Flash product)	I <sub>CC</sub>	V <sub>CC</sub>	Normal operation	—	65	75	mA	CPU: 60MHz Peripheral: 30 MHz*1,*3
	I <sub>CCS</sub>		SLEEP mode	—	30	40	mA	Peripheral: 30 MHz*1,*3
	I <sub>CCL</sub>		Sub operation	—	200	650	μA	CPU: 32 kHz Peripheral: 32 kHz *1,*2,*4
	I <sub>CC<sub>T</sub></sub>		Watch mode	—	100	550	μA	*1,*2,*4
	I <sub>CC<sub>H</sub></sub>		STOP mode	—	70	500	μA	*1,*2
Powersupply current (MASK product)	I <sub>CC</sub>	V <sub>CC</sub>	Normal operation	—	45	55	mA	CPU: 60MHz Peripheral: 30 MHz*1,*3
	I <sub>CCS</sub>		SLEEP mode	—	30	40	mA	Peripheral: 30 MHz*1,*3
	I <sub>CCL</sub>		Sub operation	—	200	650	μA	CPU: 32 kHz Peripheral: 32 kHz *1,*2,*4
	I <sub>CC<sub>T</sub></sub>		Watch mode	—	100	550	μA	*1,*2,*4
	I <sub>CC<sub>H</sub></sub>		STOP mode	—	70	500	μA	*1,*2
“H” level input voltage (hysteresis input)	V <sub>IHS</sub>	P00 to P07, P10 to P17, P50 to P57, P60, P61 to P67, P70 to P77, P80 to P87, P90 to P92, PA0 to PA7, PK0 to PK2, $\overline{\text{INIT}}$ , MD0, MD1	—	$V_{CC} \times 0.8$	—	$V_{CC} + 0.3$	V	
		P20 to P27, P30 to P37, P40 to P47	—	$V_{CC} \times 0.8$	—	$V_{SS} + 5.5$	V	5 V tolerant
“L” level input voltage (hysteresis input)	V <sub>ILS</sub>	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60, P61 to P67, P70 to P77, P80 to P87, P90 to P92, PA0 to PA7, PK0 to PK2, $\overline{\text{INIT}}$ , MD0, MD1	—	$V_{SS} - 0.3$	—	$V_{CC} \times 0.2$	V	

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# MB91625 Series

(Continued)

( $V_{CC} = AV_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$ ,  $V_{SS} = AV_{SS} = 0 \text{ V}$ ,  $T_a = -40 \text{ }^\circ\text{C to } +85 \text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	$V_{OH}$	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87,	$V_{CC} = 2.7 \text{ V}$ $I_{OH} = -4 \text{ mA}$	$V_{CC} - 0.5$	—	$V_{CC}$	V	
"L" level output voltage	$V_{OL}$	P90 to P92, PA0 to PA7, PK0 to PK2	$V_{CC} = 2.7 \text{ V}$ $I_{OL} = 4 \text{ mA}$	$V_{SS}$	—	0.4	V	
Input leak current	$I_{IL}$	—	—	-5	—	+5	$\mu\text{A}$	Digital pin
				-10	—	+10	$\mu\text{A}$	Analog pin
Pull-up resistance value	$R_{PU}$	Pull-up pin	—	16.6	33	66	$\text{k}\Omega$	
Input capacitance	$C_{IN}$	Other than $V_{CC}$ , $V_{SS}$ , $AV_{CC}$ , $AV_{SS}$ , $AVRH$	—	—	10	15	pF	

\*1 : When opened, all ports are fixed to output

\*2 :  $T_a = +25 \text{ }^\circ\text{C}$  and  $V_{CC} = 3.3 \text{ V}$

\*3 :  $X0 = 15 \text{ MHz}$ , CPU clock = 60 MHz and X0A = when stopped

\*4 :  $X0 = \text{STOP}$  and X0A = 32 kHz

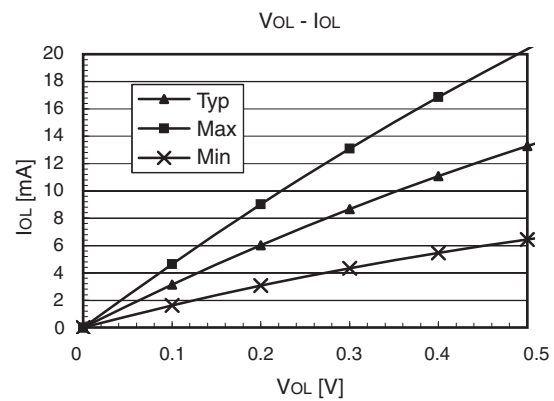
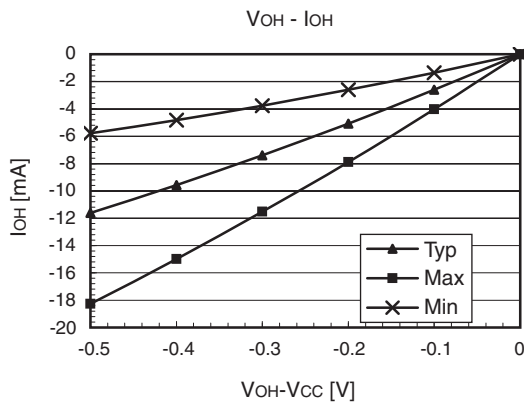
## •V-I characteristics

Conditions

Min : Process = Slow,  $T_a = +85 \text{ }^\circ\text{C}$ ,  $V_{CC} = 2.7 \text{ V}$

Typ : Process = Typical,  $T_a = +25 \text{ }^\circ\text{C}$ ,  $V_{CC} = 3.3 \text{ V}$

Max : Process = Fast,  $T_a = -40 \text{ }^\circ\text{C}$ ,  $V_{CC} = 3.6 \text{ V}$



## 4. AC Characteristics

### (1) Main Clock (MCLK) Input Standard

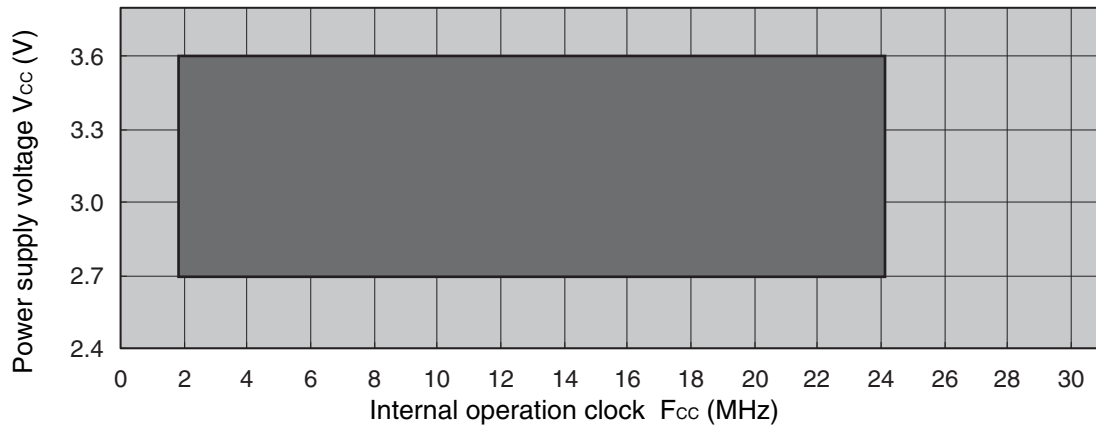
( $V_{CC} = AV_{CC} = 2.7\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	$F_{CH}$	X0, X1	—	4	48	MHz	When crystal oscillator is connected
			—	4	48	MHz	When using external clock
Input clock cycle	$t_{CYLH}$		—	20.83	250	ns	When using external clock
Input clock pulse width	—		$P_{WH}/t_{CYLH}$ $P_{WL}/t_{CYLH}$	45	55	%	When using external clock
Input clock rise time and fall time	$t_{CF}$ , $t_{CR}$		—	—	5	ns	When using external clock
Internal operating clock frequency	$F_{CS}$	—	—	—	60	MHz	Source clock
	$F_{CC}$	—	—	—	60	MHz	CPU clock
	$F_{CP}$	—	—	—	40	MHz	Peripheral bus clock
Internal operating clock cycle time	$t_{CYCS}$	—	—	16.7	—	ns	Source clock
	$t_{CYCC}$	—	—	16.7	—	ns	CPU clock
	$t_{CYCP}$	—	—	25	—	ns	Peripheral bus clock

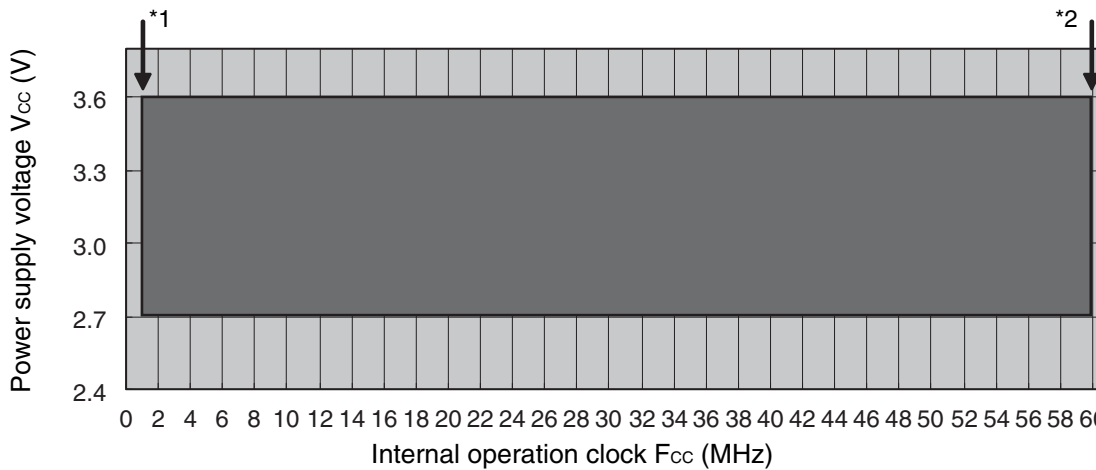
# MB91625 Series

- Operation guaranteed range

- When the main clock is selected (DIVB = 000)



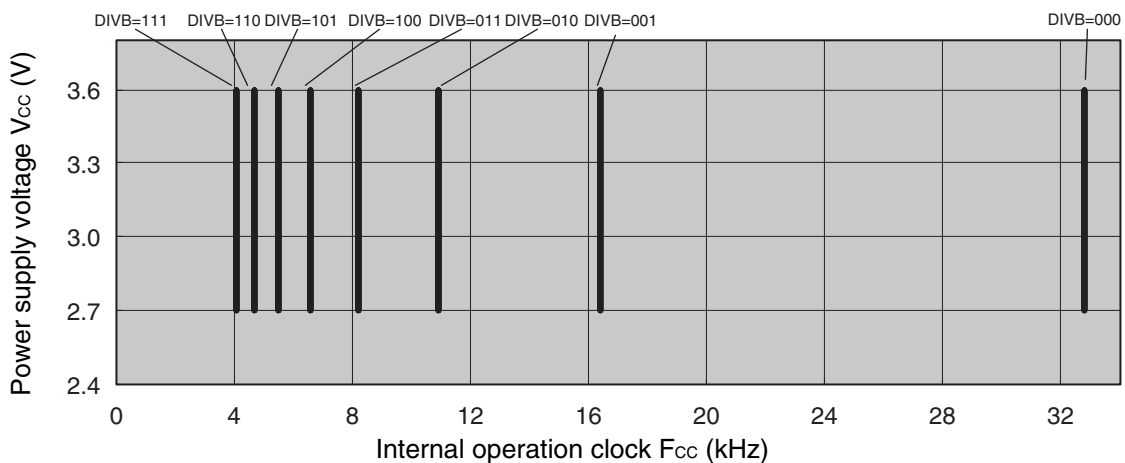
- When the PLL clock is selected



\*1 : DIVB = 111, ODS = 11, and PLL macro oscillation frequency = 30 MHz

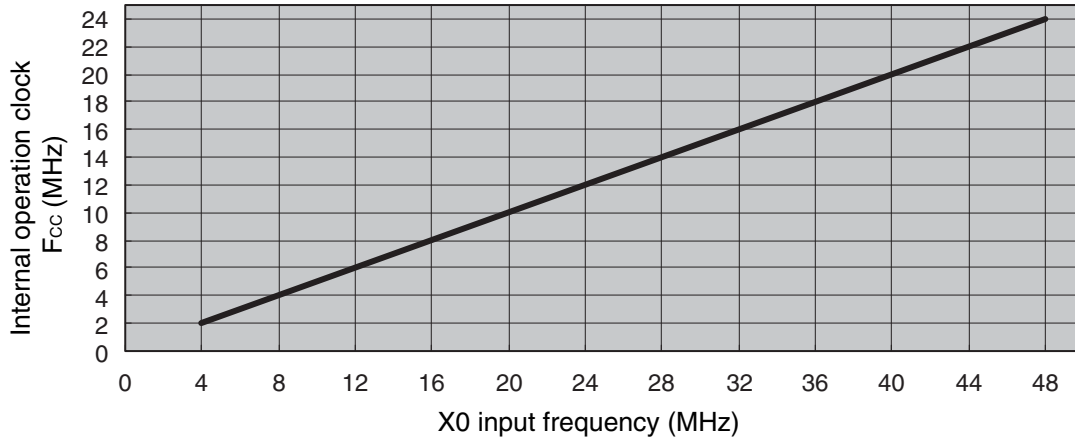
\*2 : DIVB = 000, ODS = 01, and PLL macro oscillation frequency = 60 MHz

- When the sub clock is selected ( $F_{CL} = 32.768$  kHz)

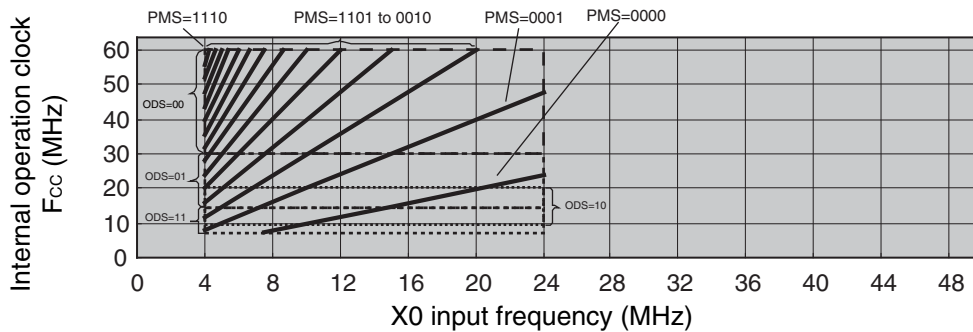


- Example of configuration

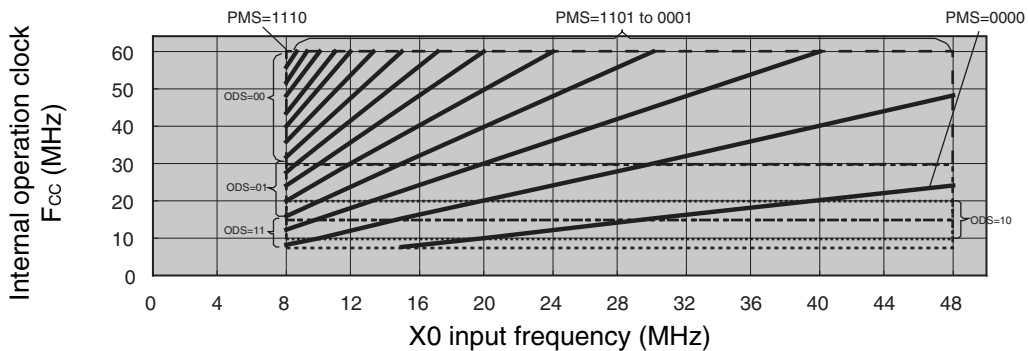
- When the main clock is selected (DIVB = 000\*1)



- When the PLL clock is selected (DIVB = 000\*1, PDS = 0000\*2)



- When the PLL clock is selected (DIVB = 000\*1, PDS = 0001\*2)



\*1 : The values other than DIVB = 000 are omitted.

\*2 : The values other than PDS = 0000 and 0001 are omitted.

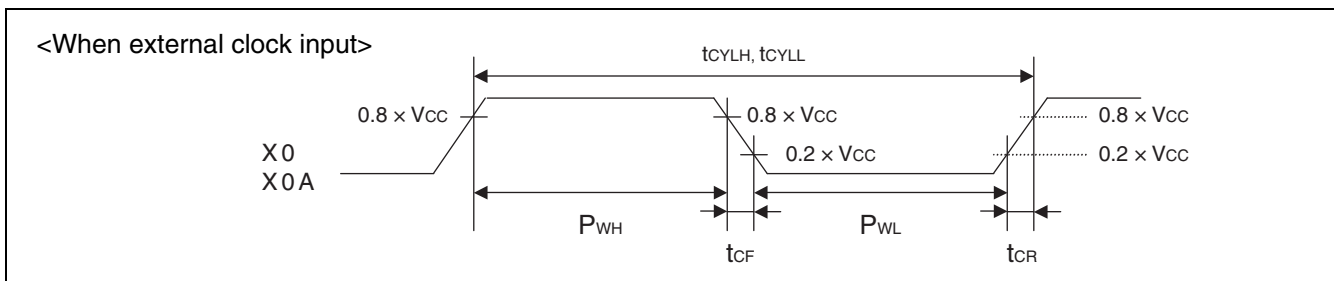
Note: DIVB : Base clock division configuration bit  
 ODS : PLL macro oscillation clock division rate select bit  
 PDS : PLL input clock division select bit  
 PMS : PLL clock multiple rate select bit

# MB91625 Series

## (2) Sub Clock (SBCLK) Input Standard

( $V_{CC} = AV_{CC} = 2.7\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	$F_{CL}$	X0A, X1A	—	—	32.768	—	kHz	When crystal oscillator is connected
			—	—	32.768	—	kHz	When using external clock
Input clock cycle	$t_{CYLL}$		—	—	30.518	—	$\mu\text{s}$	When using external clock
Input clock pulse width	—		$P_{WH}/t_{CYLL}$ $P_{WL}/t_{CYLL}$	45	—	55	%	When using external clock
Input clock rise time and fall time	$t_{CF}$ , $t_{CR}$		—	—	—	200	ns	When using external clock



## (3) Conditions of PLL

( $V_{CC} = AV_{CC} = 2.7\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
PLL oscillation stabilization wait time (LOCK UP time)	$t_{LOCK}$	—	600	—	—	$\mu\text{s}$	Time from when the PLL starts operating until the oscillation stabilizes
PLL input clock frequency	$f_{PLLI}$	—	4	—	24	MHz	
PLL multiple rate	—	—	2	—	15	Multiplied by	
PLL macro oscillation clock frequency	$f_{PLLO}$	—	30	—	60	MHz	

## (4) Regulator Voltage Stabilization Wait Time

( $V_{CC} = AV_{CC} = 2.7\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Regulator voltage stabilization wait time	$t_{REG}$	—	50	—	$\mu\text{s}$	Time taken for the regulator voltage to stabilize

Note : This is the time from when the external power supply stabilizes (after reaching 2.7 V).

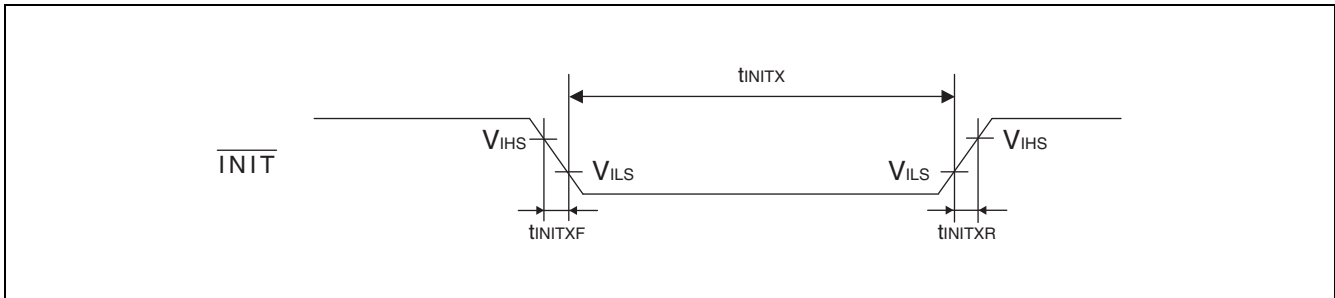
## (5) Reset Input Standards

( $V_{CC} = AV_{CC} = 2.7\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condi- tions	Value		Unit	Remarks
				Min	Max		
Reset input time (At power-on, main oscillation stop mode)	$t_{INITX}$	$\overline{INIT}$	—	Oscillation time of oscillator + 10 $t_{CYLH}$	—	ns	*
Reset input time (At other times)				10 $t_{CYLH}$	—	ns	
Reset input rise time and fall time	$t_{INITXF}$ , $t_{INITXR}$			—	10	ms	

\* : After the supply voltage has stabilized, it takes a further 50  $\mu\text{s}$  until the internal supply stabilizes. Hold the input to the  $\overline{INIT}$  pin during that period.

- At power-on
- When in stop mode
- When in sub mode and sub watch mode when the main oscillation is stopped.



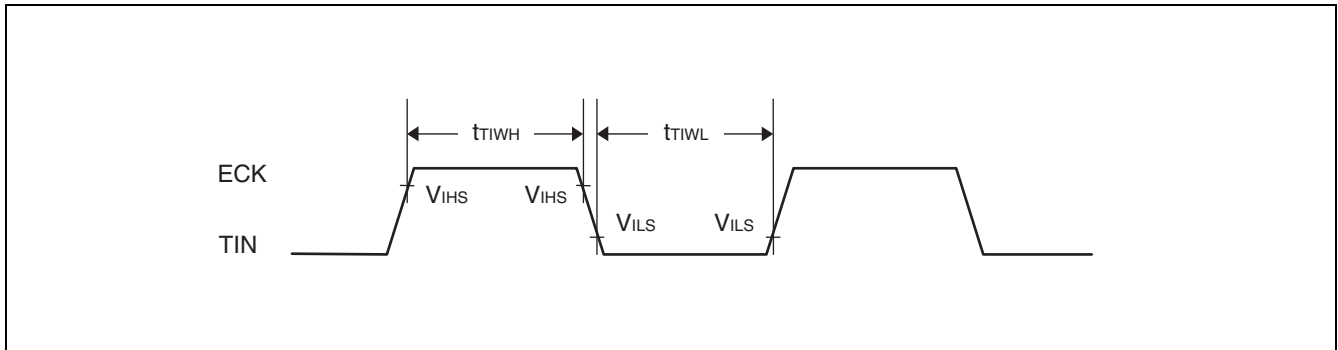
# MB91625 Series

## (6) Base Timer Input Timing

- Timer input timing

( $V_{CC} = AV_{CC} = 2.7\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

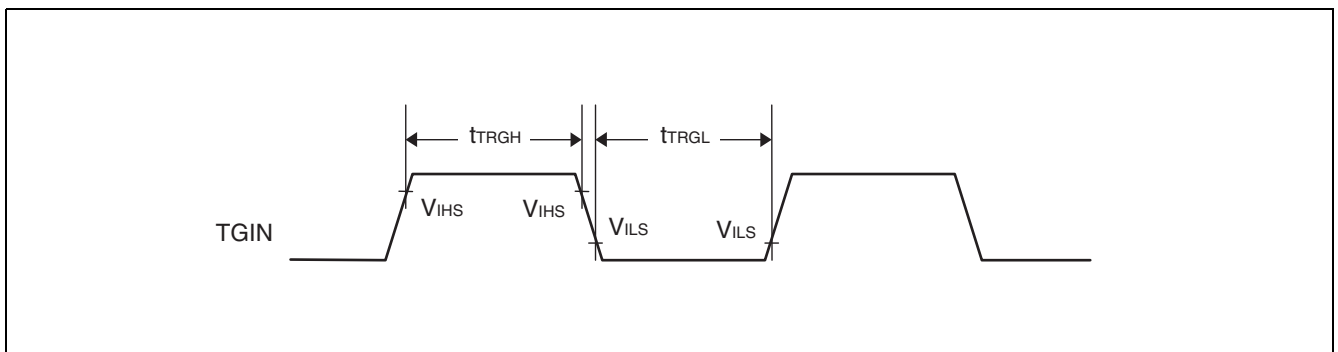
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Input pulse width	$t_{TIWH}$ , $t_{TIWL}$	TIOAn / TIOBn (When used as ECK, TIN)	—	$2 t_{CYCP}$	—	ns



- Trigger Input Timing

( $V_{CC} = AV_{CC} = 2.7\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Input pulse width	$t_{TRGH}$ , $t_{TRGL}$	TIOAn / TIOBn (When used as TGIN)	—	$2 t_{CYCP}$	—	ns



## (7) Synchronous serial (CSIO) timing

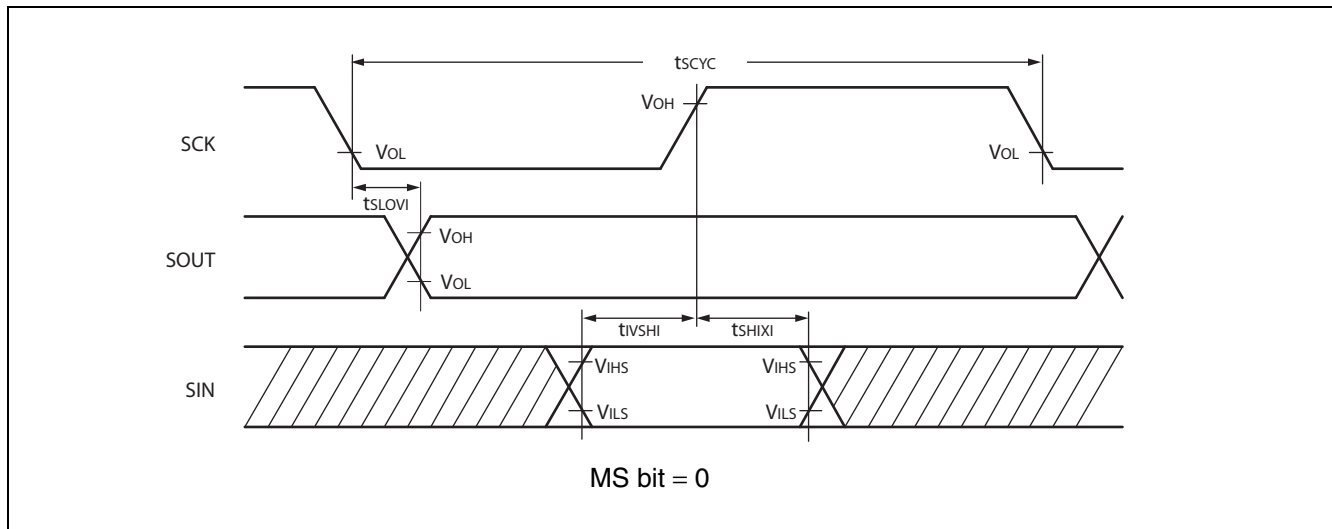
( $V_{CC} = AV_{CC} = 2.7\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

- Synchronous serial (SPI = 0, SCINV = 0)

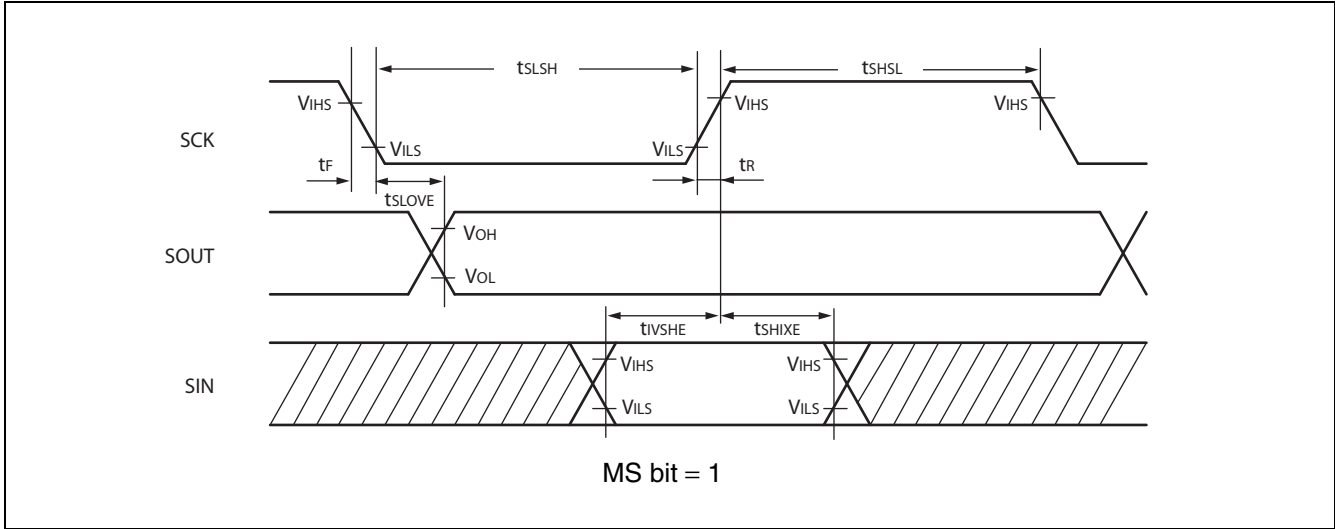
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	$t_{SCYC}$	SCKn	Internal shift clock operation	$4t_{CYCP}$	—	ns
SCK ↓ → SOUT delay time	$t_{SLOVI}$	SCKn, SOUTn		- 30	+ 30	ns
SIN → SCK ↑ setup time	$t_{IVSHI}$	SCKn, SINn		45	—	ns
SCK ↑ → SIN hold time	$t_{SHIXI}$	SCKn, SINn		0	—	ns
Serial clock "L" pulse width	$t_{LSH}$	SCKn	External shift clock operation	$2t_{CYCP} - 10$	—	ns
Serial clock "H" pulse width	$t_{HSL}$	SCKn		$t_{CYCP} + 10$	—	ns
SCK ↓ → SOUT delay time	$t_{SLOVE}$	SCKn, SOUTn		—	40	ns
SIN → SCK ↑ setup time	$t_{IVSHE}$	SCKn, SINn		15	—	ns
SCK ↑ → SIN hold time	$t_{SHIXE}$	SCKn, SINn		20	—	ns
SCK fall time	$t_F$	SCKn		—	—	5
SCK rise time	$t_R$	SCKn	—	—	5	ns

Notes: • The above standards apply to CLK synchronous mode.

- $t_{CYCP}$  indicates the peripheral clock cycle time.
- When the external load capacitance  $C = 50\text{ pF}$ .



# MB91625 Series

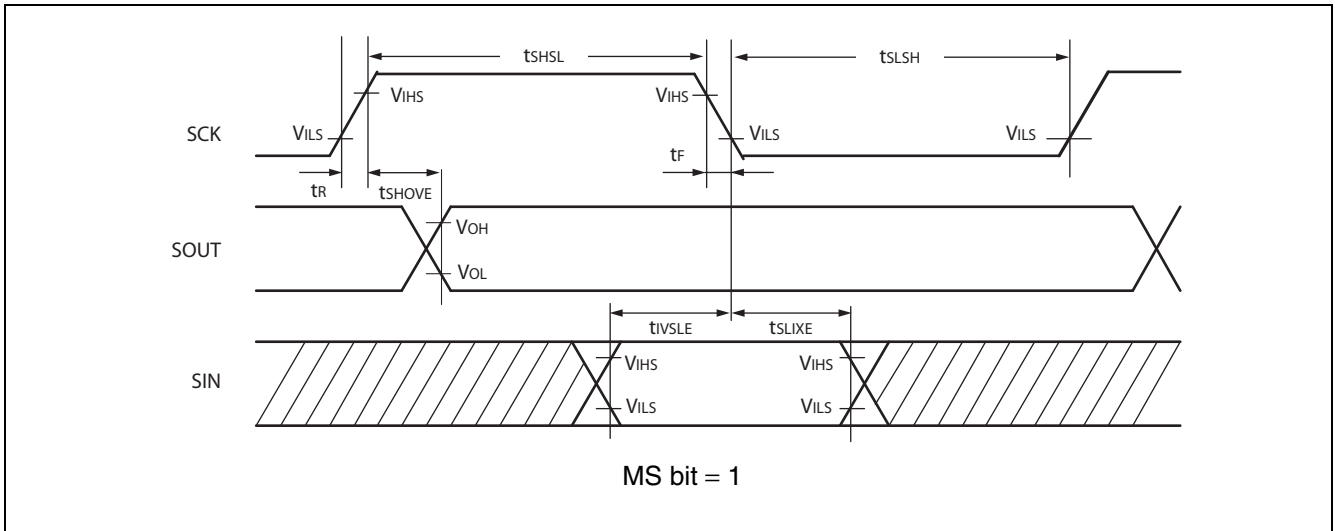
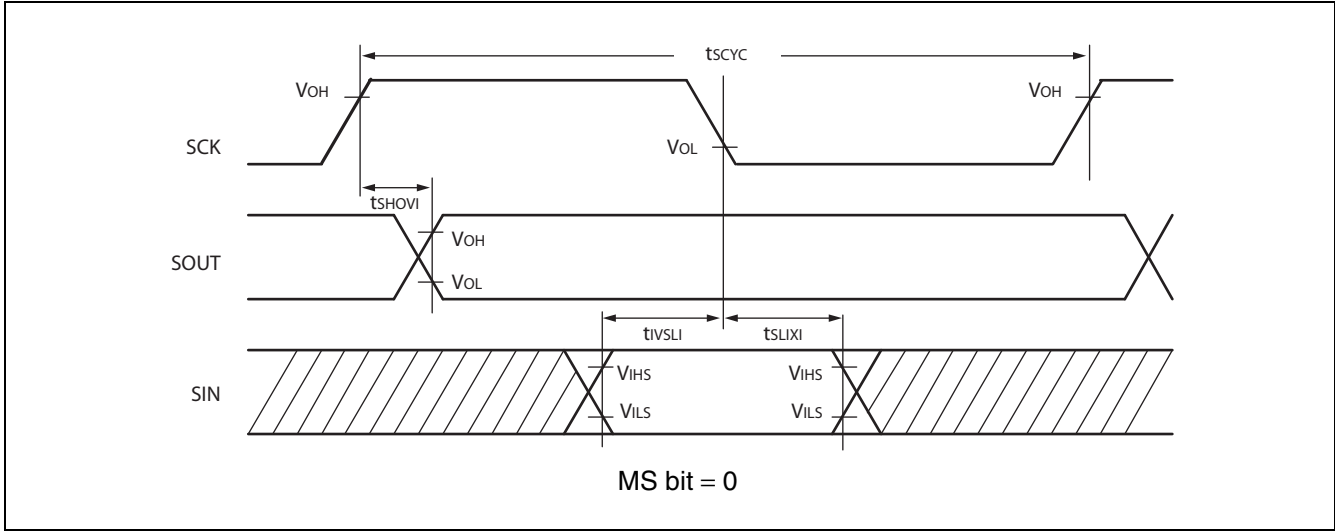


- Synchronous serial (SPI = 0, SCINV = 1)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	$t_{SCYC}$	SCKn	Internal shift clock operation	$4t_{CYCP}$	—	ns
SCK $\uparrow$ $\rightarrow$ SOUT delay time	$t_{SHOVI}$	SCKn, SOUTn		- 30	+ 30	ns
SIN $\rightarrow$ SCK $\downarrow$ setup time	$t_{VSLI}$	SCKn, SINn		45	—	ns
SCK $\downarrow$ $\rightarrow$ SIN hold time	$t_{SLIXI}$	SCKn, SINn		0	—	ns
Serial clock "L" pulse width	$t_{SLSH}$	SCKn	External shift clock operation	$2t_{CYCP} - 10$	—	ns
Serial clock "H" pulse width	$t_{SHSL}$	SCKn		$t_{CYCP} + 10$	—	ns
SCK $\uparrow$ $\rightarrow$ SOUT delay time	$t_{SHOVE}$	SCKn, SOUTn		—	40	ns
SIN $\rightarrow$ SCK $\downarrow$ setup time	$t_{VSLI}$	SCKn, SINn		15	—	ns
SCK $\downarrow$ $\rightarrow$ SIN hold time	$t_{SLIXI}$	SCKn, SINn		20	—	ns
SCK fall time	$t_F$	SCKn		—	5	ns
SCK rise time	$t_R$	SCKn		—	5	ns

Notes: • The above standards apply to CLK synchronous mode.

- $t_{CYCP}$  indicates the peripheral clock cycle time.
- When the external load capacitance  $C = 50\text{pF}$ .



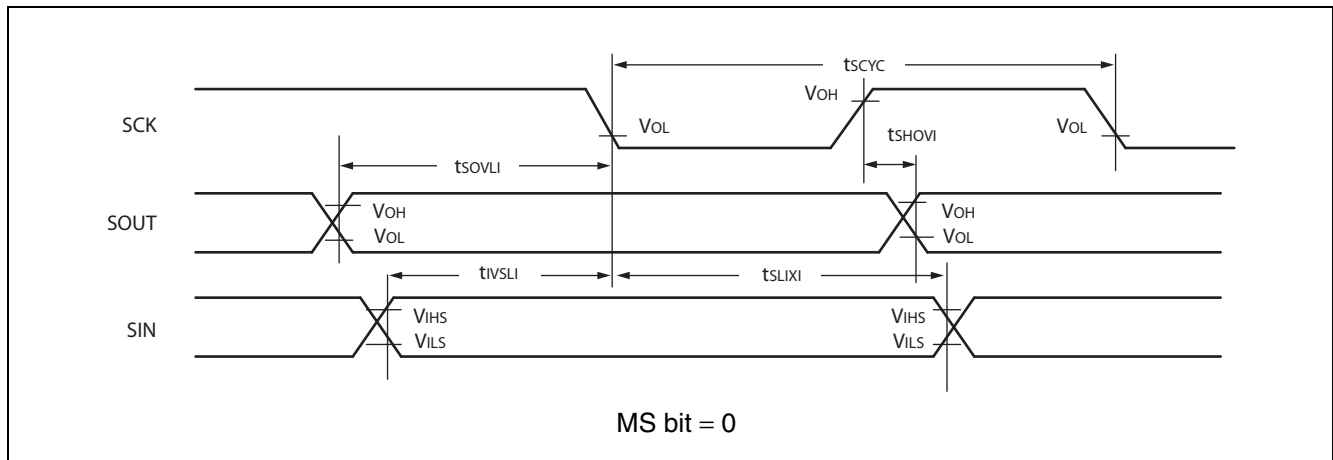
# MB91625 Series

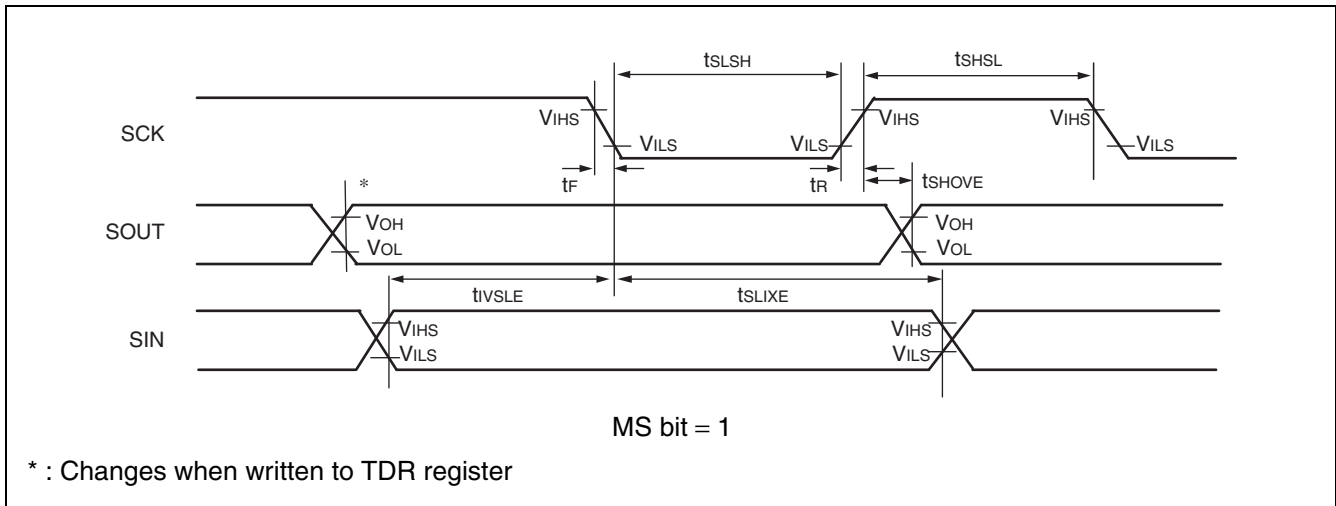
- Synchronous serial (SPI = 1, SCINV = 0)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	$t_{SCYC}$	SCKn	Internal shift clock operation	$4t_{CYCP}$	—	ns
SCK $\uparrow$ $\rightarrow$ SOUT delay time	$t_{SHOVI}$	SCKn, SOUTn		- 30	+ 30	ns
SIN $\rightarrow$ SCK $\downarrow$ setup time	$t_{IVSLI}$	SCKn, SINn		45	—	ns
SCK $\downarrow$ $\rightarrow$ SIN hold time	$t_{SLIXI}$	SCKn, SINn		0	—	ns
SOUT $\rightarrow$ SCK $\downarrow$ delay time	$t_{SOVLI}$	SCKn, SOUTn		$2t_{CYCP} - 30$	—	ns
Serial clock "L" pulse width	$t_{SLSH}$	SCKn	External shift clock operation	$2t_{CYCP} - 10$	—	ns
Serial clock "H" pulse width	$t_{SHSL}$	SCKn		$t_{CYCP} + 10$	—	ns
SCK $\uparrow$ $\rightarrow$ SOUT delay time	$t_{SHOVE}$	SCKn, SOUTn		—	40	ns
SIN $\rightarrow$ SCK $\downarrow$ setup time	$t_{IVSLE}$	SCKn, SINn		15	—	ns
SCK $\downarrow$ $\rightarrow$ SIN hold time	$t_{SLIXE}$	SCKn, SINn		20	—	ns
SCK fall time	$t_F$	SCKn	—	5	ns	
SCK rise time	$t_R$	SCKn	—	5	ns	

Notes: • The above standards apply to CLK synchronous mode.

- $t_{CYCP}$  indicates the peripheral clock cycle time.
- When the external load capacitance  $C = 50\text{pF}$ .





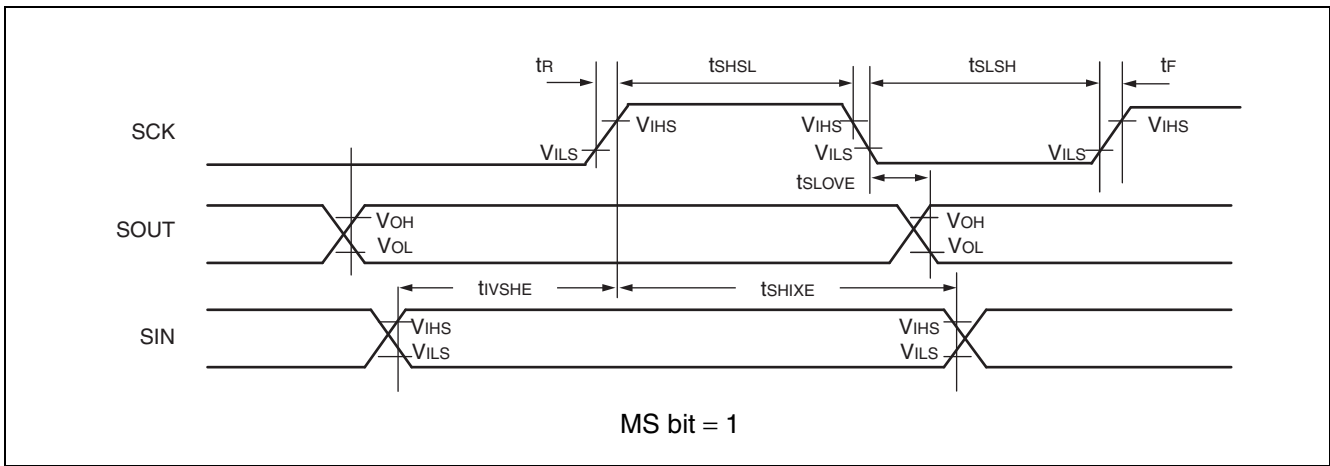
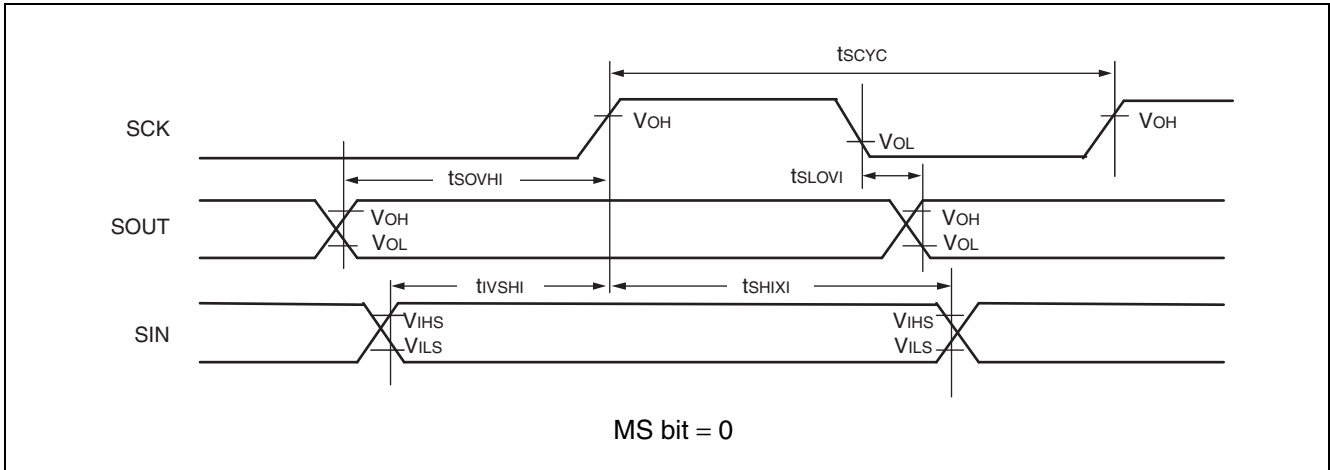
- Synchronous serial (SPI = 1, SCINV = 1)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	$t_{SCYC}$	SCKn	Internal shift clock operation	$4t_{CYCP}$	—	ns
SCK ↓ → SOUT delay time	$t_{SLOVI}$	SCKn, SOUTn		- 30	+ 30	ns
SIN → SCK ↑ setup time	$t_{IVSHI}$	SCKn, SINn		45	—	ns
SCK ↑ → SIN hold time	$t_{SHIXI}$	SCKn, SINn		0	—	ns
SOUT → SCK ↑ delay time	$t_{SOVHI}$	SCKn, SOUTn		$2t_{CYCP} - 30$	—	ns
Serial clock “L” pulse width	$t_{SLSH}$	SCKn		$2t_{CYCP} - 10$	—	ns
Serial clock “H” pulse width	$t_{SHSL}$	SCKn	External shift clock operation	$t_{CYCP} + 10$	—	ns
SCK ↓ → SOUT delay time	$t_{SLOVE}$	SCKn, SOUTn		—	40	ns
SIN → SCK ↑ setup time	$t_{IVSHE}$	SCKn, SINn		15	—	ns
SCK ↑ → SIN hold time	$t_{SHIXE}$	SCKn, SINn		20	—	ns
SCK fall time	$t_F$	SCKn		—	5	ns
SCK rise time	$t_R$	SCKn		—	5	ns

Notes: • The above standards apply to CLK synchronous mode.

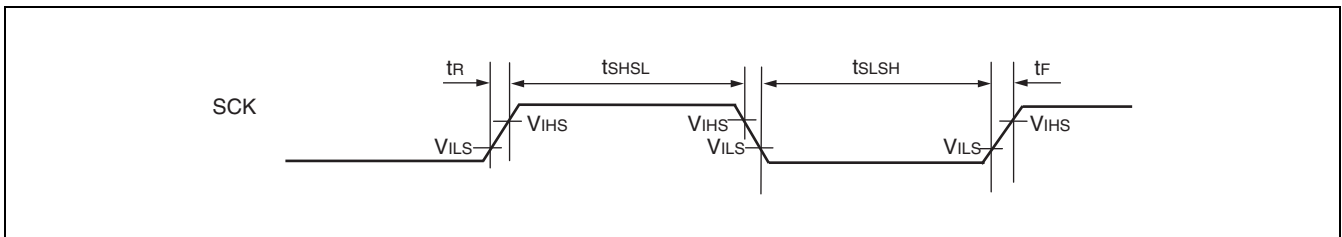
- $t_{CYCP}$  indicates the peripheral clock cycle time.
- When the external load capacitance  $C = 50\text{pF}$ .

# MB91625 Series



• External clock (EXT = 1) : asynchronous only

Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
Serial clock "L" pulse width	$t_{SLSH}$	$C_L = 50 \text{ pF}$	$t_{CYCP} + 10$	—	ns
Serial clock "H" pulse width	$t_{SHSL}$		$t_{CYCP} + 10$	—	ns
SCK fall time	$t_F$		—	5	ns
SCK rise time	$t_R$		—	5	ns



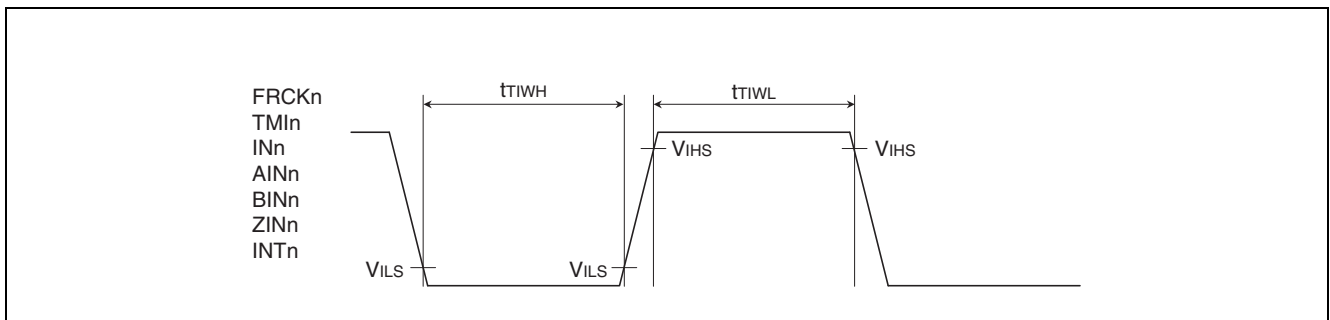
## (8) Free-run Timer Clock, Reload Timer Event Input, Up/down Counter Input, Input Capture Input, Interrupt Input Timing

( $V_{CC} = AV_{CC} = 2.7\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condi- tions	Value		Unit	Remarks
				Min	Max		
Input pulse width	$t_{TIWH}$ , $t_{TIWL}$	FRCKn, TMIn, INn, AINn, BINn, ZINn	—	$2 t_{CYCP}$	—	ns	*1
		INTn	—	$3 t_{CYCP}$	—	ns	*1
			—	1.0	—	$\mu\text{s}$	*2

\*1 :  $t_{CYCP}$  indicates peripheral clock cycle time, except when in stop mode, in main timer mode and in watch mode.

\*2 : When in stop mode, in main timer mode, or in watch mode.

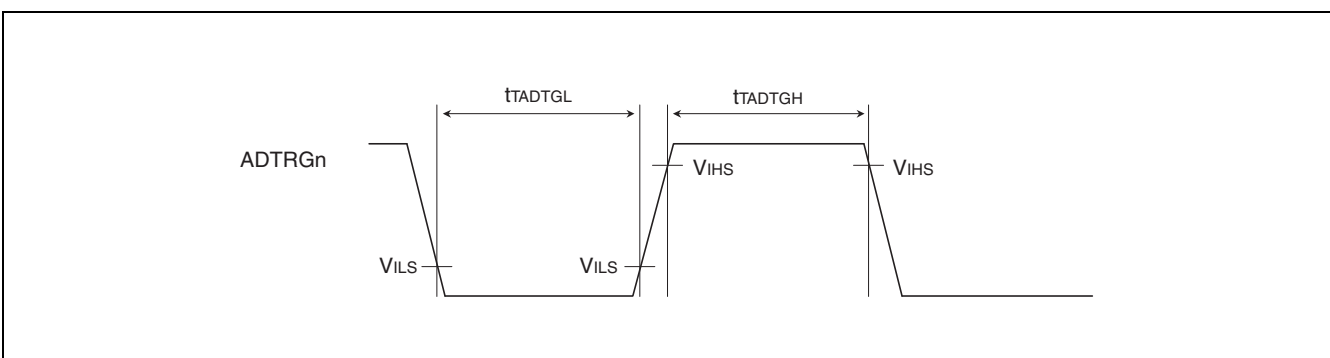


## (9) A/D Converter Trigger Input Timing

( $V_{CC} = AV_{CC} = 2.7\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condi- tions	Value		Unit	Remarks
				Min	Max		
A/D converter trigger input	$t_{TADTGL}$ , $t_{TADTGH}$	ADTRGn	—	$2 t_{CYCP}$	—	ns	*

\* :  $t_{CYCP}$  indicates peripheral clock cycle time.



# MB91625 Series

## (10) I<sup>2</sup>C Timing

(V<sub>CC</sub> = AV<sub>CC</sub> = 2.7 V to 3.6 V, V<sub>SS</sub> = AV<sub>SS</sub> = 0 V, Ta = -40 °C to +85 °C)

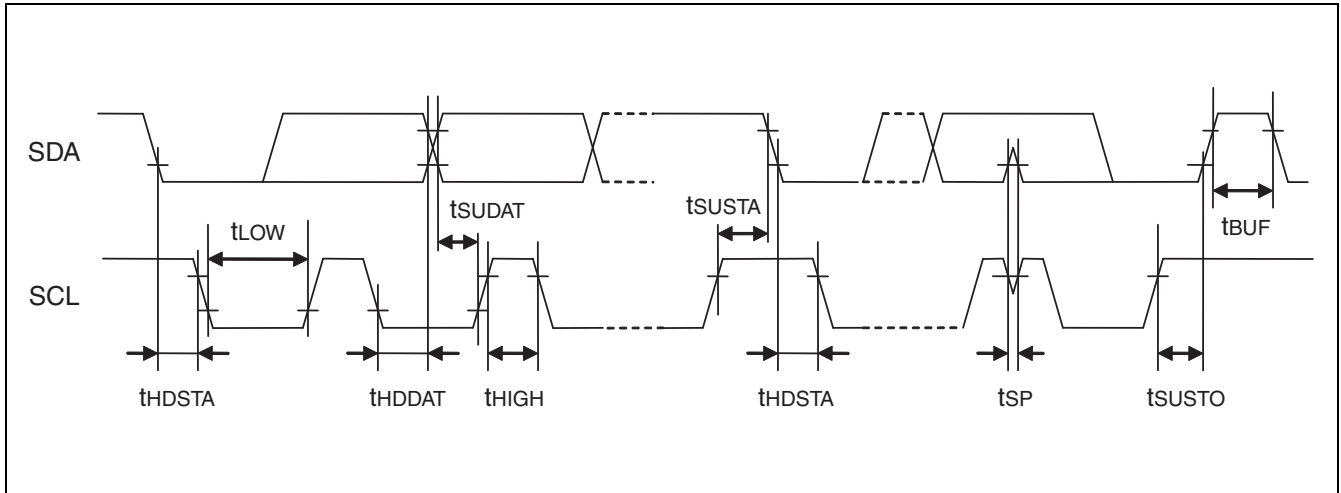
Parameter	Symbol	Pin name	Condition	Typical mode		High-speed mode		Unit
				Min	Max	Min	Max	
SCL clock frequency	f <sub>SCL</sub>	SCKn (SCLn)	C <sub>L</sub> = 50 pF R = (V <sub>p</sub> /I <sub>OL</sub> )* <sup>1</sup>	0	100	0	400	kHz
“(Repeated) START condition” hold time SDA ↓ → SCL ↓	t <sub>HDSTA</sub>	SOUTn (SDAn), SCKn (SCLn)		4.0	—	0.6	—	μs
SCL clock “L” width	t <sub>LOW</sub>	SCKn (SCLn)		4.7	—	1.3	—	μs
SCL clock “H” width	t <sub>HIGH</sub>	SCKn (SCLn)		4.0	—	0.6	—	μs
“(Repeated START condition)” setup time SCL ↑ → SDA ↓	t <sub>SUSTA</sub>	SCKn (SCLn)		4.7	—	0.6	—	μs
Data hold time SCL ↓ → SDA ↓ ↑	t <sub>HDDAT</sub>	SOUTn (SDAn), SCKn (SCLn)		0	3.45* <sup>2</sup>	0	0.9* <sup>3</sup>	μs
Data setup time SDA ↓ ↑ → SCL ↑	t <sub>SUDAT</sub>	SOUTn (SDAn), SCKn (SCLn)		250	—	100	—	ns
“(STOP condition)” setup time SCL ↑ → SDA ↑	t <sub>SUSTO</sub>	SOUTn (SDAn), SCKn (SCLn)		4.0	—	0.6	—	μs
Bus free time between “STOP condition” and “START condition”	t <sub>BUF</sub>	—		4.7	—	1.3	—	μs
Noise filter	t <sub>SP</sub>	—	—	2t <sub>CYCP</sub> * <sup>4</sup>	—	2t <sub>CYCP</sub> * <sup>4</sup>	—	ns

\*1 : R and C represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. V<sub>p</sub> indicates the power supply voltage of the pull-up resistance and I<sub>OL</sub> indicates V<sub>OL</sub> guaranteed current.

\*2 : The maximum t<sub>HDDAT</sub> must satisfy that it doesn't extend at least “L” period (t<sub>LOW</sub>) of device's SCL signal.

\*3 : A high-speed mode I<sup>2</sup>C bus device can be used on a standard mode I<sup>2</sup>C bus system as long as the device satisfies the requirement of “t<sub>SUDAT</sub> ≥ 250 ns”.

\*4 : t<sub>CYCP</sub> is the peripheral clock cycle time. To use I<sup>2</sup>C, set the peripheral bus clock at 8 MHz or more.



# MB91625 Series

## 5. Electrical Characteristics for the A/D Converter

( $V_{CC} = AV_{CC} = 2.7\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_a = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ )

Parameter	Pin name	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	10	bit	
Total error	—	- 5.0	—	+ 5.0	LSB	AV <sub>CC</sub> = 3.3 V, AV <sub>RH</sub> = 3.3 V
Linearity error	—	- 3.5	—	+ 3.5	LSB	
Differential linearity error	—	- 3	—	+ 3	LSB	
Zero transition voltage	AN0 to AN15	- 1.5	+ 0.5	+ 4	LSB	
Full transition voltage	AN0 to AN15	AV <sub>RH</sub> - 4	AV <sub>RH</sub> - 1.5	AV <sub>RH</sub> + 0.5	LSB	
Compare time	—	0.72* <sup>3</sup>	—	—	μs	PCLK = 33 MHz
Conversion time	—	1.2* <sup>1</sup>	—	—	μs	PCLK = 33 MHz
Power supply current (analog + digital)	AV <sub>CC</sub>	—	—	3.5	mA	When operating A/D (with D/A stopped)
		—	—	11	μA	At power-down* <sup>2</sup>
Reference power supply current (between AV <sub>RH</sub> and AV <sub>SS</sub> )	AV <sub>RH</sub>	—	—	0.6	mA	When operating A/D AV <sub>RH</sub> = 3.0 V
		—	—	5	μA	At power-down* <sup>2</sup>
Analog input capacitance	—	—	—	8.5	pF	
Interchannel disparity	—	—	—	4	LSB	
Analog port input current	AN0 to AN15	—	—	10	μA	
Analog input voltage	AN0 to AN15	AV <sub>SS</sub>	—	AV <sub>RH</sub>	V	
Reference voltage	AV <sub>RH</sub>	AV <sub>SS</sub>	—	AV <sub>CC</sub>	V	

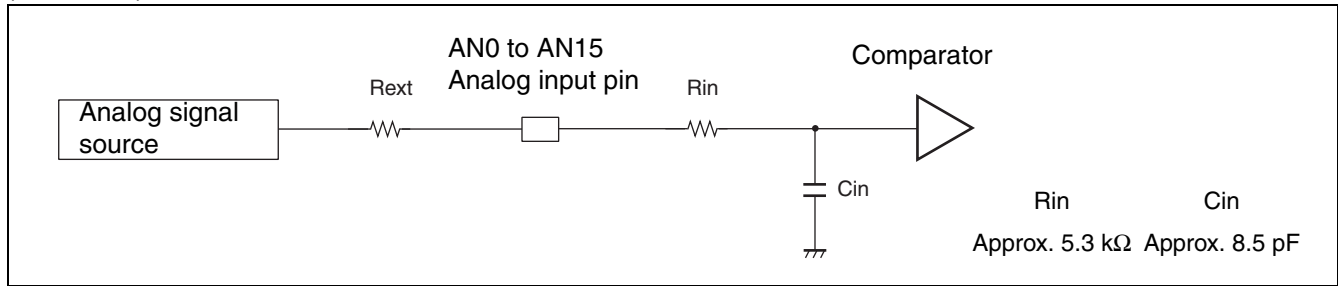
\*1 : It depends on the actual external load and the clock cycle supplied to peripheral resources. Make sure to satisfy PCLK cycle × 4 or over + below (Equation 1). The condition of minimum conversion time is the value when PCLK = 33 MHz, sampling time: 0.424 μs, external impedance: 1.4k Ω or below, compare time: 0.72 μs.

\*2 : The current when the CPU is in stop mode and the A/D converter is not operating.

\*3 : Compare time = {(CT + 1) × 10 + 4} × peripheral clock (PCLK) period. (CT indicates compare time setting bits.)  
The condition of the minimum compare time is when CT = 1 and PCLK = 33 MHz.

(Continued)

(Continued)



The output impedance of the external circuit connected to the analog input affects the sampling time of the A/D converter. Design the output impedance of the output circuit such that the required sampling time is less than the value of  $T_s$  calculated from the following equation.

(Equation1)  $T_s = (R_{in} + R_{ext}) \times C_{in} \times 8$   
 $T_s$  : Sampling time  
 $R_{in}$  : Input resistance of A/D =  $5.3\text{ k}\Omega$   
 $C_{in}$  : Input capacitance of A/D =  $8.5\text{ pF}$   
 $R_{ext}$  : Output impedance of external circuit

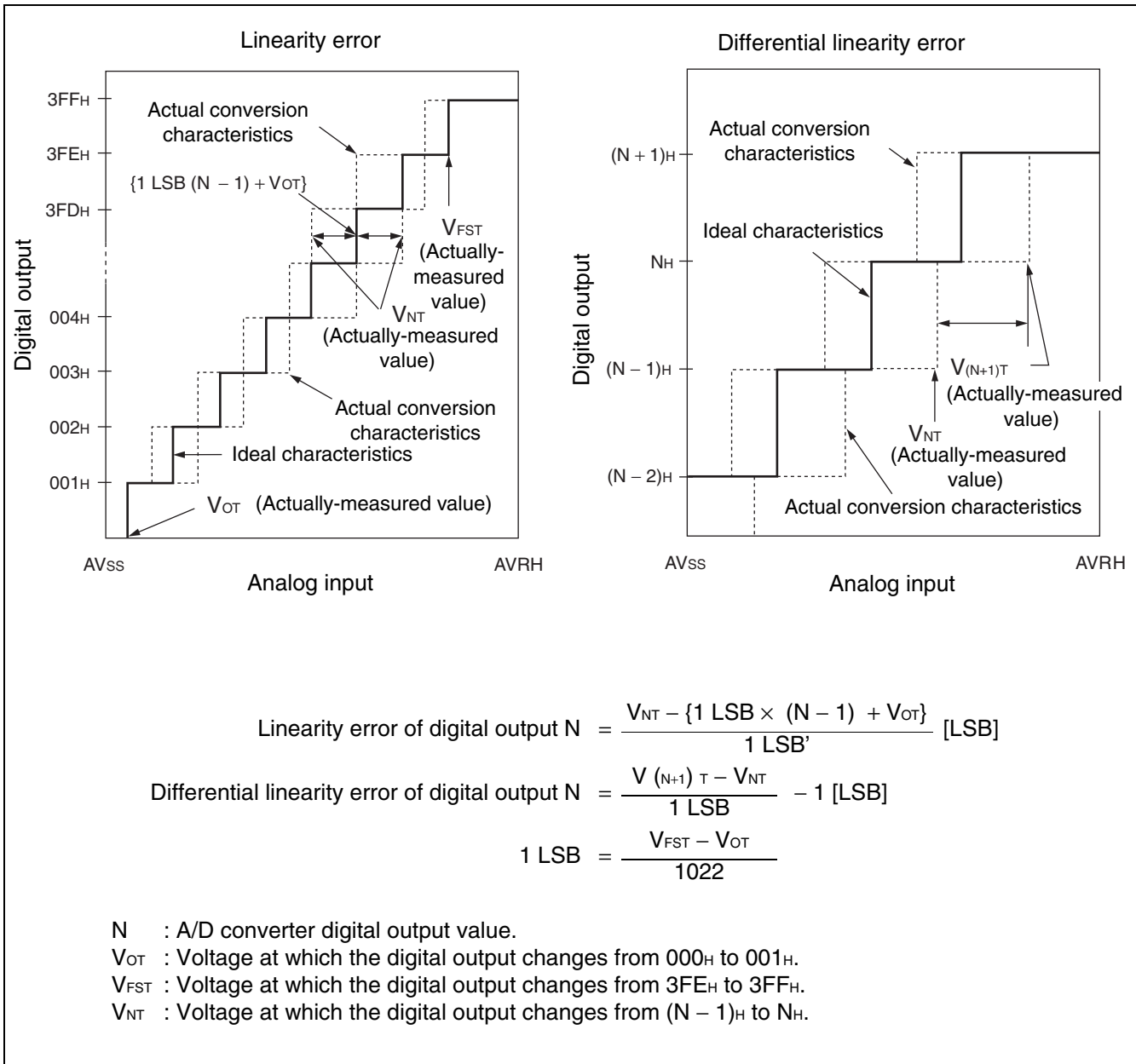
If the sampling time is set as  $600\text{ ns}$ ,  
 $600\text{ ns} \geq (5.3\text{ k}\Omega + R_{ext}) \times 8.5\text{ pF} \times 8$   
 $\therefore R_{ext} \leq 3.5\text{ k}\Omega$

And the impedance of the external circuit therefore needs to be  $3.5\text{ k}\Omega$  or less.

# MB91625 Series

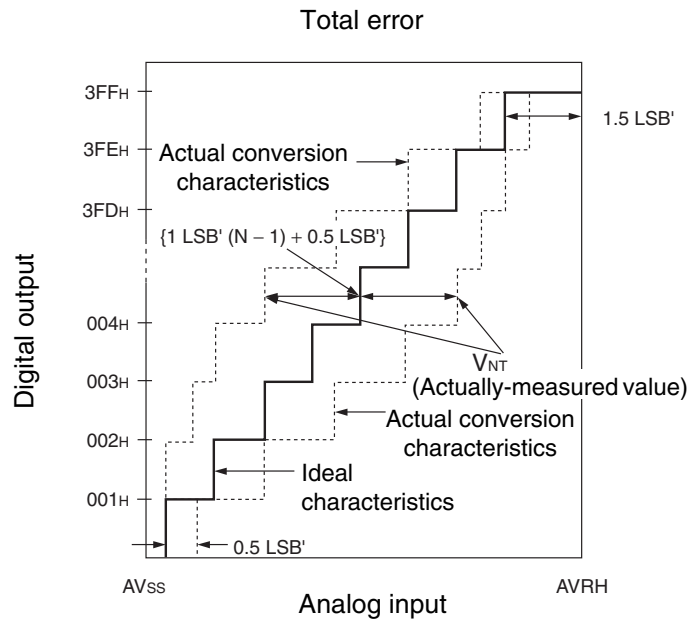
## •Definition of 10-bit A/D Converter Terms

- Resolution : Analog variation that is recognized by an A/D converter.
- Linearity error : Deviation of the line between the zero-transition point (0000000000←→0000000001) and the full-scale transition point (1111111110←→1111111111) from the actual conversion characteristics.
- Differential linearity error : Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.
- Total error : Difference between the actual value and the theoretical value. The total error includes zero transition error, full-scale transition error, and linear error.



(Continued)

(Continued)



$$1 \text{ LSB}' (\text{Ideal value}) = \frac{\text{AVRH} - \text{AVSS}}{1024} [\text{V}]$$

$$\text{Total error of digital output } N = \frac{V_{\text{NT}} - \{1 \text{ LSB}' \times (N - 1) + 0.5 \text{ LSB}'\}}{1 \text{ LSB}'}$$

N : A/D converter digital output value.

$V_{\text{NT}}$  : Voltage at which the digital output changes from  $(N + 1)_H$  to  $N_H$ .

$V_{\text{OT}}'$  (Ideal value) =  $\text{AVSS} + 0.5 \text{ LSB}'$  [V]

$V_{\text{FST}}'$  (Ideal value) =  $\text{AVRH} - 1.5 \text{ LSB}'$  [V]

# MB91625 Series

## 6. Electrical Characteristics for the D/A Converter

( $V_{CC} = AV_{CC} = 2.7\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

Parameter	Pin name	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	8	bit	
Linearity error	—	- 2.0	—	+ 2.0	LSB	When the output is unloaded
Differential linearity error	—	- 1.0	—	+ 1.0	LSB	When the output is unloaded
Conversion time	—	—	0.6	—	$\mu\text{s}$	When load capacitance ( $C_L$ ) = 20 pF
	—	—	3.0	—	$\mu\text{s}$	When load capacitance ( $C_L$ ) = 100 pF
Analog output impedance	DA0, DA1	3.19	3.51	5.85	k $\Omega$	
Analog current	$AV_{CC}$	—	300	—	$\mu\text{A}$	10 $\mu\text{s}$ conversion, when the output is unloaded (When 2 channels operating, A/D stopped)
		—	—	3600*	$\mu\text{A}$	When the input digital code is fixed at 7A <sub>H</sub> or 85 <sub>H</sub> (When 2 channels operating, A/D stopped)
		—	—	11	$\mu\text{A}$	At power-down (When A/D stopped)

\* : The current consumption of the D/A converter varies with input digital code. The standard value indicates the current consumed when the digital code that maximizes the current consumption is input.

## 7. Flash Memory Write/Erase Characteristics

(V<sub>CC</sub> = 3.3 V, Ta = + 25 °C)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	—	0.9	3.6	s	Excludes write time prior to internal erase
Half word (16 bits) write time	—	23	370	μs	Not including system-level overhead time.
Chip erase time*1	—	7.2	28.8	s	Excludes write time prior to internal erase (When equipped with 512 Kbytes)
Erase/write cycles	10000	—	—	cycle	Average Ta ≤ + 85 °C
Flash memory data hold time	10*2	—	—	year	Average Ta ≤ + 85 °C

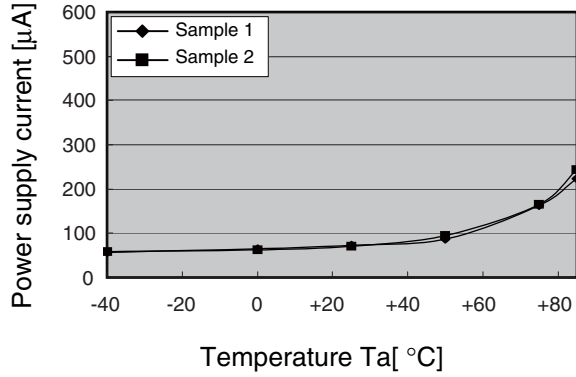
\*1 : The chip erase time is the sector erase time multiplied across all sectors.

\*2 : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85 °C) .

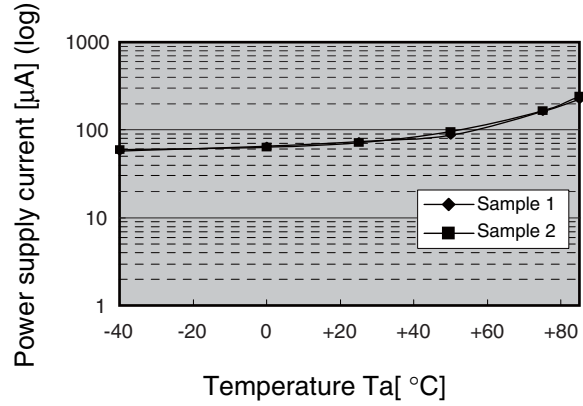
## CHARACTERISTICS

- Characteristics of MB91F625

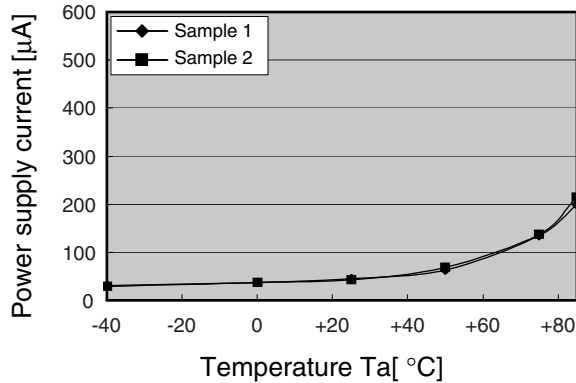
Power supply current (sub operation)  
 $I_{CCCL}$  temperature characteristics  
 $V_{CC} = 3.3\text{ V}$



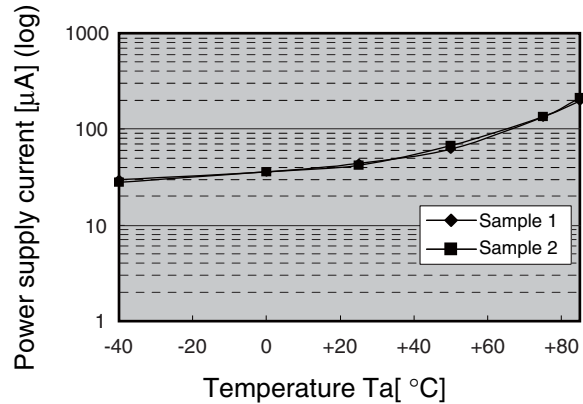
$I_{CCCL}$  temperature characteristics (semi-log)  
 $V_{CC} = 3.3\text{ V}$



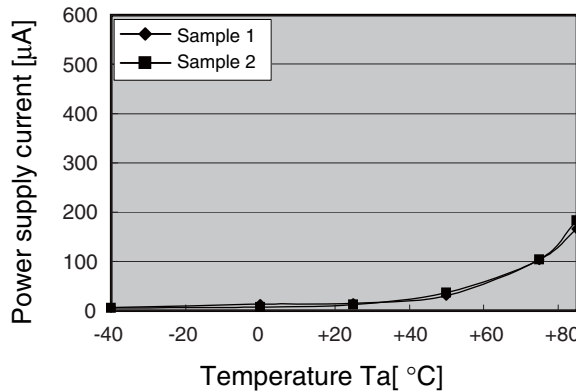
Power supply current (watch mode)  
 $I_{CCCT}$  temperature characteristics  
 $V_{CC} = 3.3\text{ V}$



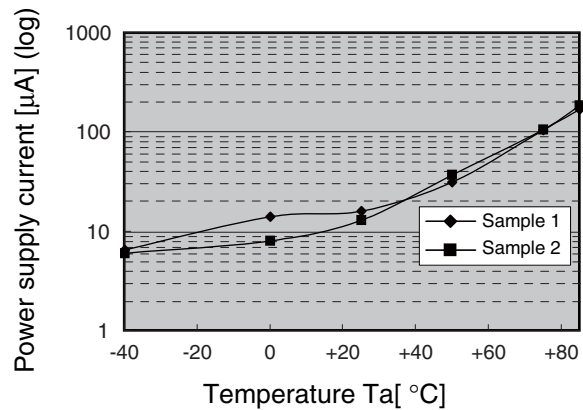
$I_{CCCT}$  temperature characteristics (semi-log)  
 $V_{CC} = 3.3\text{ V}$



Power supply current (stop mode)  
 $I_{CCH}$  temperature characteristics  
 $V_{CC} = 3.3\text{ V}$



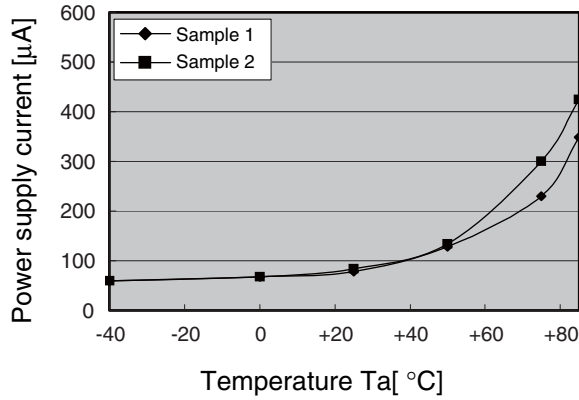
$I_{CCH}$  temperature characteristics (semi-log)  
 $V_{CC} = 3.3\text{ V}$



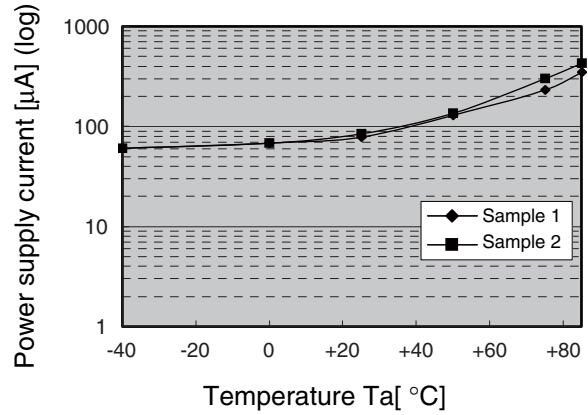
• Characteristics of MB91F627

Power supply current (sub operation)

$I_{CCCL}$  temperature characteristics  
 $V_{CC} = 3.3\text{ V}$

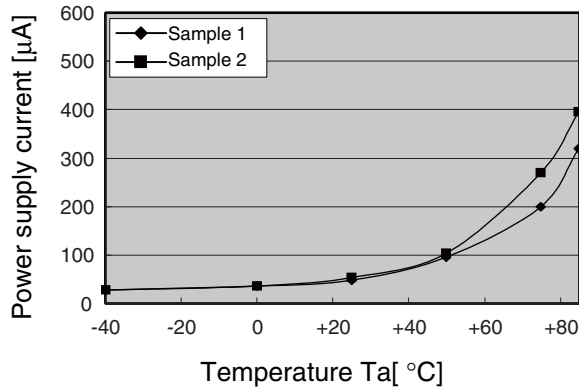


$I_{CCCL}$  temperature characteristics (semi-log)  
 $V_{CC} = 3.3\text{ V}$

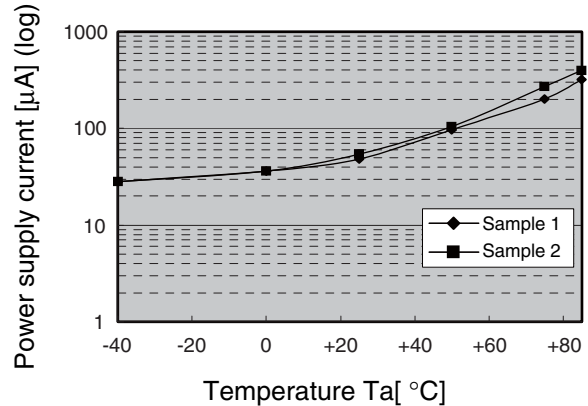


Power supply current (watch mode)

$I_{CCW}$  temperature characteristics  
 $V_{CC} = 3.3\text{ V}$

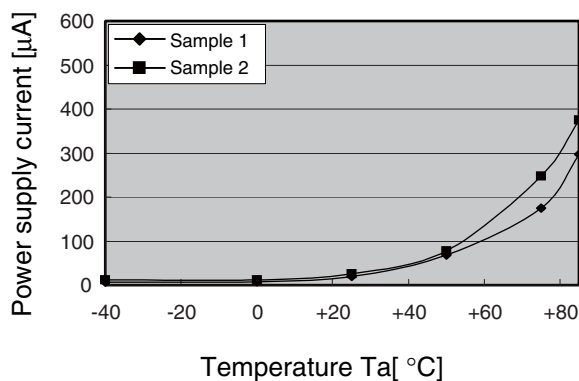


$I_{CCW}$  temperature characteristics (semi-log)  
 $V_{CC} = 3.3\text{ V}$

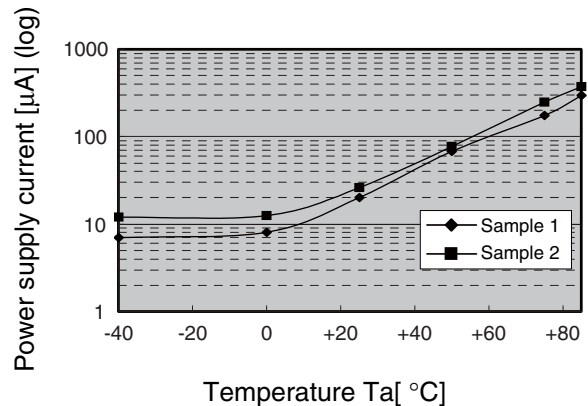


Power supply current (stop mode)

$I_{CCS}$  temperature characteristics  
 $V_{CC} = 3.3\text{ V}$



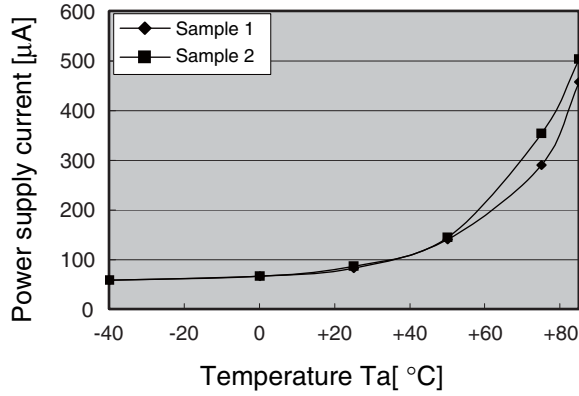
$I_{CCS}$  temperature characteristics (semi-log)  
 $V_{CC} = 3.3\text{ V}$



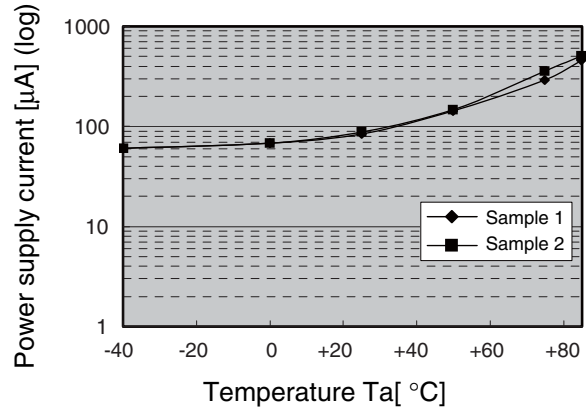
# MB91625 Series

- Characteristics of MB91627

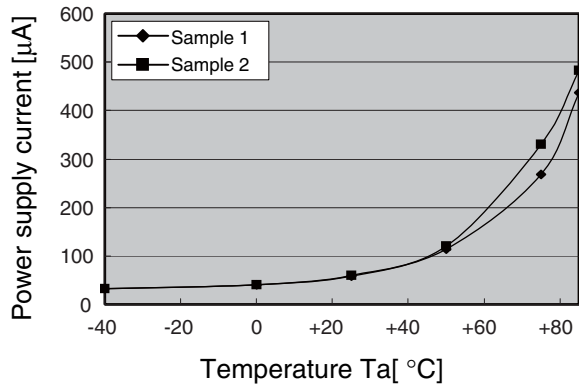
Power supply current (sub operation)  
 $I_{CCL}$  temperature characteristics  
 $V_{CC} = 3.3\text{ V}$



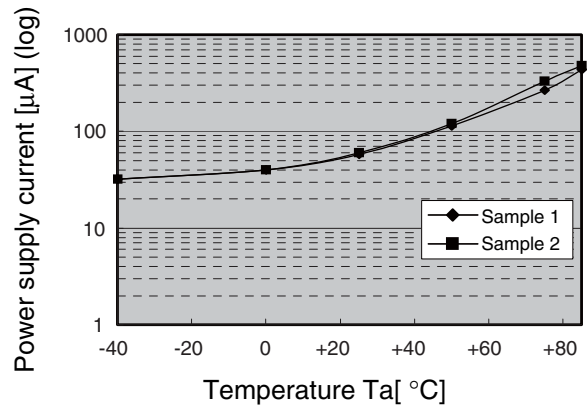
$I_{CCL}$  temperature characteristics (semi-log)  
 $V_{CC} = 3.3\text{ V}$



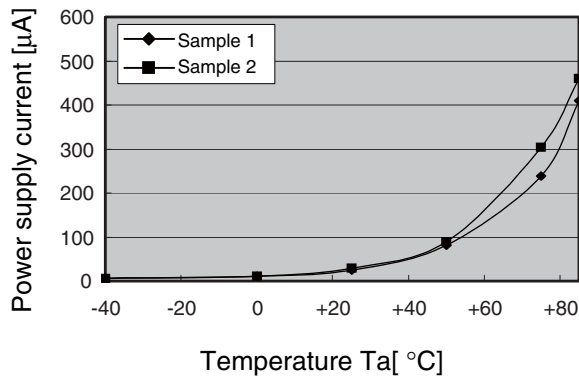
Power supply current (watch mode)  
 $I_{CCT}$  temperature characteristics  
 $V_{CC} = 3.3\text{ V}$



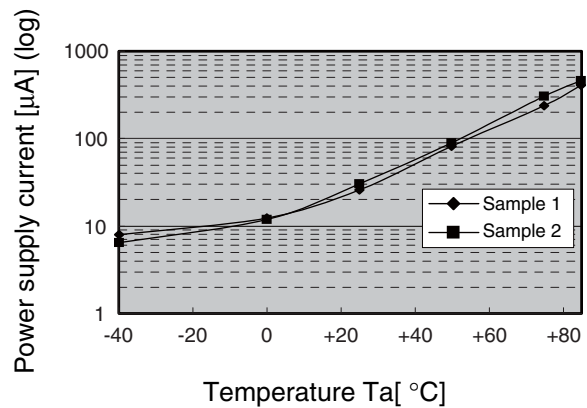
$I_{CCT}$  temperature characteristics (semi-log)  
 $V_{CC} = 3.3\text{ V}$



Power supply current (stop mode)  
 $I_{CCH}$  temperature characteristics  
 $V_{CC} = 3.3\text{ V}$



$I_{CCH}$  temperature characteristics (semi-log)  
 $V_{CC} = 3.3\text{ V}$



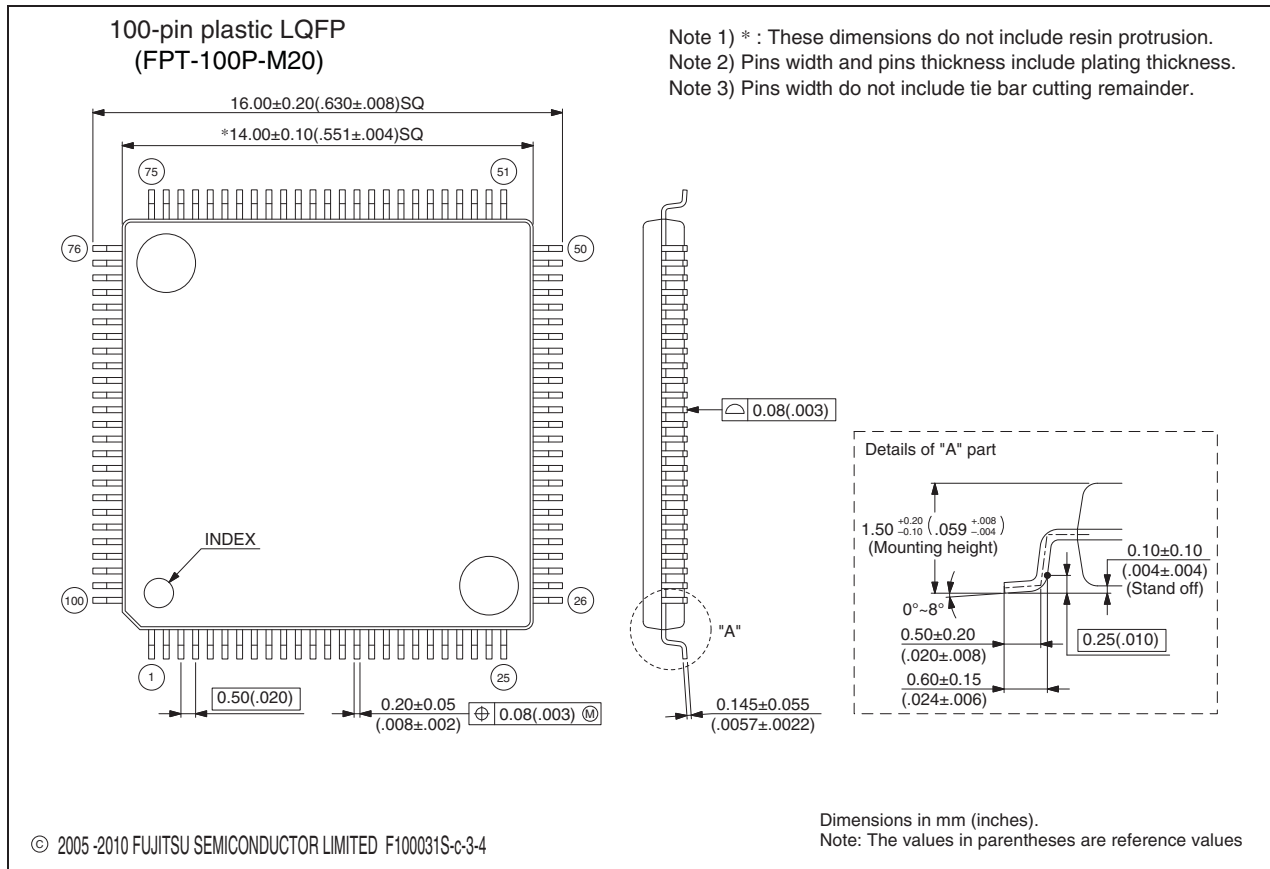
## ■ ORDERING INFORMATION

Part number	Package
MB91F627PMC	100-pin plastic LQFP (FPT-100P-M20)
MB91627PMC	
MB91F625PMC	

# MB91625 Series

## PACKAGE DIMENSION

<p>100-pin plastic LQFP</p> <p>(FPT-100P-M20)</p>	Lead pitch	0.50 mm
	Package width × package length	14.0 mm × 14.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm Max
	Weight	0.65 g
	Code (Reference)	P-LFQFP100-14×14-0.50



Please check the latest package dimension at the following URL.  
<http://edevice.fujitsu.com/package/en-search/>

## ■ MAIN CHANGES IN THIS EDITION (Changes from the first edition.)

Page	Section	Change Results
—	—	Added MB91627 and MB91F625.
9	■ PIN DESCRIPTION	Corrected “I/O circuit type” of the pins number 20, 21 and 22. (P → H, P)
22	■ I/O CIRCUIT TYPE	Added the type H.
29	■ HANDLING DEVICES	Added “ • Differences in features among the products with different memory sizes and between Flash products and MASK products”.
30	■ BLOCK DIAGRAM	Added “/Mask ROM” to “Internal program memory Flash memory”.
32	■ MEMORY SPACE 2. Memory Map	Corrected the table. (000F 0000 <sub>H</sub> → 000F 8000 <sub>H</sub> )
68	■ ELECTRICAL CHARACTERISTICS 1. Absolute Maximum Ratings	Changed from “Power consumption” to “Power consumption (Flash product)”. Added “Power consumption (MASK product)”.
71	3. DC Characteristics	Added “Power supply current (MASK product)”.
94 to 96	■ CHARACTERISTICS	Added a new section.

The vertical lines marked in the left side of the page show the changes.

# MB91625 Series

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