

## 32-bit Microcontrollers

CMOS

# FR80 MB91610 Series

## MB91F610A/613

### ■ DESCRIPTION

The MB91610 series is a line of Fujitsu Semiconductor microcontrollers based on a 32-bit RISC CPU core that feature a variety of peripheral functions for embedded applications that demand high-performance and high-speed CPU processing.

This series is based on the FR80\* family CPU and is implemented as a single chip.

\* : FR, the abbreviation of FUJITSU RISC controller, is a line of products of Fujitsu Semiconductor Limited.

### ■ FEATURES

- FR80 CPU
  - 32-bit RISC, load/store architecture, five-stage pipeline
  - General-purpose registers : 32-bit × 16
  - 16-bit fixed-length instructions (basic instructions) : 1 instruction per cycle
  - Instructions suitable for embedded applications
    - Memory-to-memory transfer, bit processing, barrel shift instructions, etc.
    - Instruction support for high level languages  
Function entry and exit instructions, instructions for register multi-load and multi-store
    - Bit search instruction  
"1" detection, "0" detection, transition point detection
    - Branch instructions with delay slots  
Reduced overhead when processing branches
    - Register interlock functions  
Facilitate coding in assembly language

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For the information for microcontroller supports, see the following web site.

This web site includes the "**Customer Design Review Supplement**" which provides the latest cautions on system development and the minimal requirements to be checked to prevent problems before the system development.

<http://edevice.fujitsu.com/micom/en-support/>

# MB91610 Series

- Built-in multiplier/instruction-level support
  - Signed 32-bit multiplication : 5 cycles
  - Signed 16-bit multiplication : 3 cycles
- Interrupts (save PC and PS) : 6 cycles, 16 priority levels
- Harvard architecture allowing program access and data access to be executed simultaneously
- Instruction prefetch function has been added with 4 word instruction queue of CPU
  
- Instruction compatible with FR family CPU
  - Additional bit search instructions
  - No resource instructions and coprocessor instructions
  
- Maximum operating frequency
  - CPU : 33 MHz
  - Resources : 33 MHz
  
- DMA controller (DMAC)
  - 8 channels
  - Address space : 32 bits (4 Gbytes)
  - Transfer modes : Block transfer/burst transfer/demand transfer
  - Address update : Increment/decrement/fix (increment/decrement step size of 1, 2, or 4)
  - Transfer data length : Selectable from 8-bit, 16-bit, 32-bit
  - Block size : 1 to 16
  - Number of transfers : 1 to 65535
  - Transfer requests
    - Requests from software
    - Interrupt requests from peripheral resources (interrupt requests are shared, including external interrupts)
  - Reload functions : Reload can be specified on all channels
  - Priority order : Fixed (ch.0 > ch.1 > ch.2 > ch.3 > ...) or round-robin
  - Interrupt requests : Interrupts can be generated for transfer complete, transfer error, and transfer interrupted.
  
- Multifunction serial interface
  - 4 channels with 16-byte FIFO, 4 channels without FIFO
  - Operation mode is selectable from UART/CSIO/I<sup>2</sup>C for each channel (For ch.0, I<sup>2</sup>C is not available.)
    - UART
      - Full-duplex double buffer
      - Selectable parity on/off
      - Built-in dedicated baud rate generator
      - External clock can be used as a serial clock
      - Error detection function for parity, frame and overrun errors
    - CSIO
      - Full-duplex double buffer
      - Built-in dedicated baud rate generator
      - Overrun error detection function
    - I<sup>2</sup>C
      - Supports both standard mode (Max 100 kbps) and Fast mode (Max 400 kbps)
      - Some channels are 5 V tolerant

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- Interrupts
  - Total of 16 external interrupts (some pins are 5 V tolerant)
  - Interrupts from peripheral resources
  - Programmable interrupt levels (16 levels)
  - Can be used to return from stop mode, sleep mode
- A/D converter
  - 8 channels, 1 unit
  - 10-bit resolution
  - Conversion time : approx. 1.2  $\mu$ s (PCLK = 33 MHz)
  - Priority conversion (2 levels)
  - Conversion modes : Single-shot conversion mode, scan conversion mode
  - Activation sources : Software, external trigger, base timer
  - Built-in FIFO for storing conversion data (for scan conversion:16, for priority conversion:4)
- Base timer
  - 8 channels
  - Operation mode is selectable from the followings for each channel
    - 16/32-bit reload timer
    - 16-bit PWM timer
    - 16/32-bit PWC timer
    - 16-bit PPG timer
  - Cascading connection between 2 channels allows them to be used as one 32-bit timer
  - Multiple channels can be started simultaneously
  - Input/output select function
- 16-bit reload timer
  - 3 channels (including 1 channel for REALOS)
  - Interval timer function
  - Count clock select function (peripheral clock (PCLK) divided by 2 to 64)
- Compare timer
  - 32-bit input capture : 4 channels
  - 32-bit output compare : 4 channels
  - 32-bit free-run timer : 1 channel
- Other interval timers
  - Watch counter : 1 channel
  - Watchdog timer : 2 channels
    - Watchdog timer 0
      - After resetting this device, the watchdog timer becomes active when an arbitrary value is written to the WDTCPRO register.
      - The cycle of the watchdog timer 0 can be selected from the peripheral clock (PCLK)  $\times$  ( $2^9$  to  $2^{24}$ ).
    - Watchdog timer 1
      - After releasing the reset of this device, it counts with the CPU clock (CCLK).
      - Disable/ enable of the counter operation can be controlled by HWDE pin.
      - The cycle of the watchdog timer 1 is CCLK  $\times$   $2^{23}$  cycle fixed.

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# MB91610 Series

- USB function / HOST
  - 1 channel
  - Supports Full-Speed only
  - The USB function and USB HOST are the switch types (USB I/O multiplexed)
  - Support of DMA transfer
  - USB Function
    - Support of up to six endpoints
      - Endpoint 0 is provided for the fixed use of control transfers
      - Bulk or interrupt transfer can be selected for endpoint 1 to 5
    - Double buffer structure for endpoint 1 to 5
  - USB HOST
    - Support control transfer, bulk transfer, interrupt transfer, and isochronous transfer
    - Automatic detection of connection/disconnection of USB devices
    - Automatic processing of a handshake packet for IN/OUT token processing
    - Support of a maximum packet length of up to 256 bytes
    - Support for a wakeup function
- HDMI-CEC/Remote Control Reception
  - 1 channel
  - HDMI-CEC reception function (with automatic ACK response function)
  - Remote control reception function (built-in 4-byte receive buffer)
- OSD function
  - 16 bits RGB (256 colors available among 65536 colors)
  - Analog RGB output : Max 50 MHz
  - Digital RGB output : Max 75 MHz
  - A font in 32 × 32 dots can be displayed up to 60 × 32
  - Two-layered display of MAIN/SUB
  - 16384 characters at the maximum
  - Equipped with one PLL for dot clock generation
- Main timer
  - 1 channel
  - Counts the oscillation stabilization wait time of the main clock (MCLK)
  - Counts the oscillation stabilization wait time of the PLL clock (PLLCLK)
  - Can be used as an interval timer while the main clock (MCLK) oscillations is stable
- Sub timer
  - 1 channel
  - Counts the oscillation stabilization wait time of the sub clock (SBCLK)
  - Can be used as an interval timer while the sub clock (SBCLK) oscillations is stable
- Clock generation
  - Main clock (MCLK) oscillator
  - Sub clock (SBCLK) oscillator
  - PLL clock (PLLCLK) oscillator

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- Low-power dissipation mode
  - Stop mode
  - Watch mode
  - Sleep mode
  - Doze mode
  - Clock division function
  
- Other features
  - I/O port
  - $\overline{\text{INIT}}$  pin is provided as a reset pin
  - Watchdog timer reset, software reset
  - Delay interrupt
  - Power supply
    - Single power supply (3.0 V to 3.6 V)

# MB91610 Series

## ■ PRODUCT LINEUP

Items \ Product Name	MB91F610A	MB91613
Product type	Flash memory product	MASK ROM product
Built-in program memory capacity	512 Kbytes (Flash)	512 Kbytes (ROM)
Built-in RAM capacity	32 Kbytes	
DMA controller (DMAC)	8 channels	
Base timer	8 channels	
Multifunction serial interface	Without FIFO : 4 channels (ch.0 to ch.3) With FIFO : 4 channels (ch.8 to ch.11)	
External interrupt	16 channels	
10-bit A/D converter	8 channels (1 unit)	
16-bit reload timer	3 channels	
Compare timer	32-bit input capture : 4 channels 32-bit output compare : 4 channels 32-bit free-run timer : 1 channel	
Watch counter	1 channel	
I/O port	50 (Max)	
USB function / HOST	1 channel	
HDMI-CEC/Remote control reception	1 channel	
OSDC	Font FLASH : 16384 characters	Font ROM : 7168 characters
Main timer	1 channel	
Sub timer	1 channel	
Wild register	16 channels	
Debug function	DSU4	—

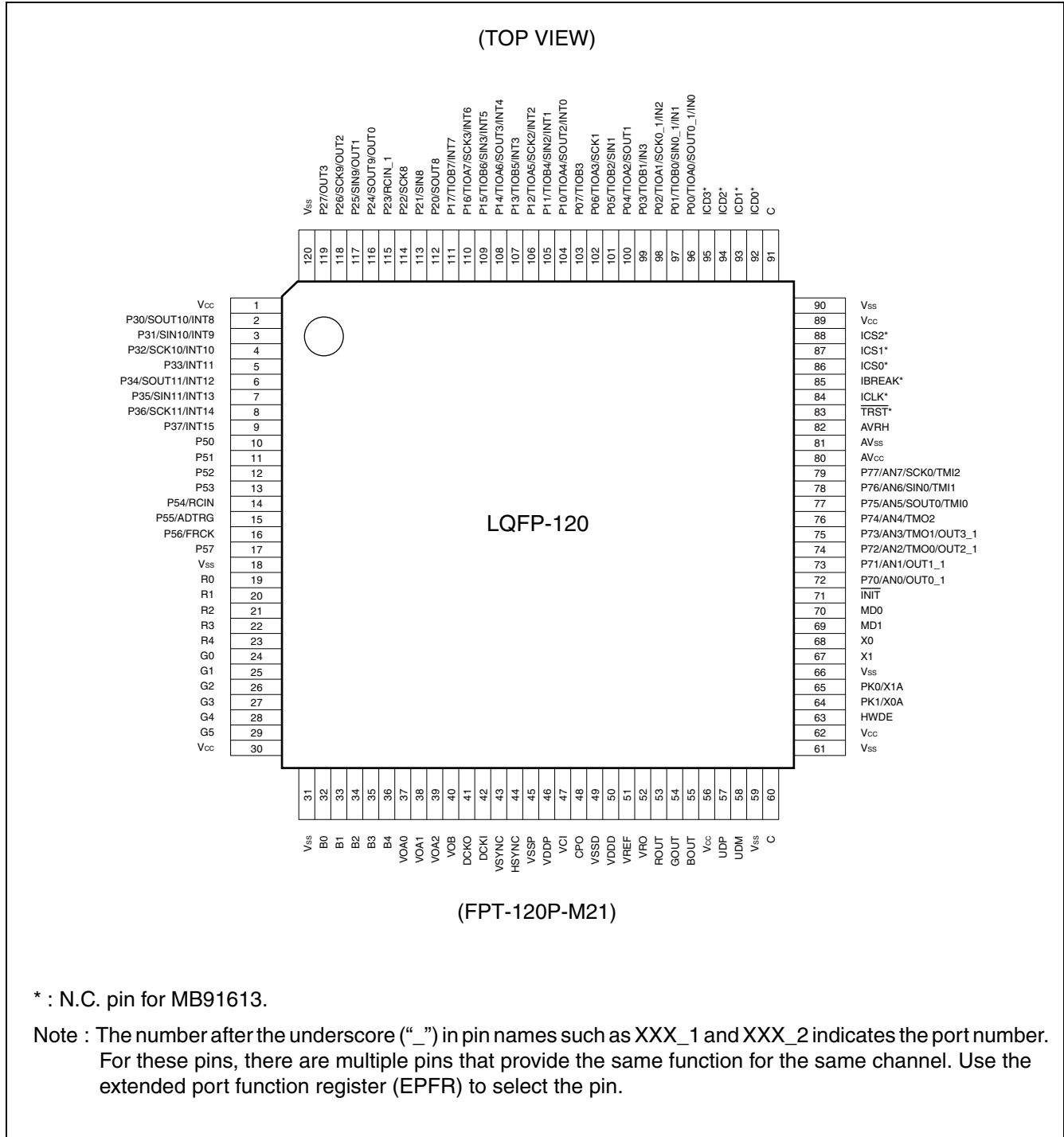
## ■ PACKAGES

Product name \ Package	MB91F610A	MB91613
FPT-120P-M21	○	○

○ : Supported

Note: Refer to "■ PACKAGE DIMENSIONS" for detailed information on each package.

## PIN ASSIGNMENT



# MB91610 Series

## ■ PIN DESCRIPTION

The number after the underscore (“\_”) in pin names such as XXX\_1 and XXX\_2 indicates the port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin no.	Pin name	I/O circuit type*	Function
1	V <sub>cc</sub>	—	3.3 V power supply
2	P30	C	General-purpose I/O port
	SOUT10 (SDA10)		Multifunction serial ch.10 output [operation modes 0 to 2] I <sup>2</sup> C ch.10 serial data line [operation mode 4]
	INT8		External interrupt 8 input
3	P31	C	General-purpose I/O port
	SIN10		Multifunction serial ch.10 input
	INT9		External interrupt 9 input
4	P32	C	General-purpose I/O port
	SCK10 (SCL10)		Multifunction serial ch.10 clock [operation modes 0 to 2] I <sup>2</sup> C ch.10 serial clock line [operation mode 4]
	INT10		External interrupt 10 input
5	P33	C	General-purpose I/O port
	INT11		External interrupt 11 input
6	P34	C	General-purpose I/O port
	SOUT11 (SDA11)		Multifunction serial ch.11 output [operation modes 0 to 2] I <sup>2</sup> C ch.11 serial data line [operation mode 4]
	INT12		External interrupt 12 input
7	P35	C	General-purpose I/O port
	SIN11		Multifunction serial ch.11 input
	INT13		External interrupt 13 input
8	P36	C	General-purpose I/O port
	SCK11 (SCL11)		Multifunction serial ch.11 clock [operation modes 0 to 2] I <sup>2</sup> C ch.11 serial clock line [operation mode 4]
	INT14		External interrupt 14 input
9	P37	C	General-purpose I/O port
	INT15		External interrupt 15 input
10	P50	B	General-purpose I/O port
11	P51	B	General-purpose I/O port

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Pin no.	Pin name	I/O circuit type*	Function
12	P52	B	General-purpose I/O port
13	P53	B	General-purpose I/O port
14	P54	B	General-purpose I/O port
	RCIN		Remote control I/O
15	P55	B	General-purpose I/O port
	ADTRG		A/D converter external trigger input
16	P56	B	General-purpose I/O port
	FRCK		Free-run timer clock input
17	P57	B	General-purpose I/O port
18	V <sub>SS</sub>	—	GND
19	R0	H	RGB digital output
20	R1	H	RGB digital output
21	R2	H	RGB digital output
22	R3	H	RGB digital output
23	R4	H	RGB digital output
24	G0	H	RGB digital output
25	G1	H	RGB digital output
26	G2	H	RGB digital output
27	G3	H	RGB digital output
28	G4	H	RGB digital output
29	G5	H	RGB digital output
30	V <sub>CC</sub>	—	3.3V power supply
31	V <sub>SS</sub>	—	GND
32	B0	H	RGB digital output
33	B1	H	RGB digital output
34	B2	H	RGB digital output
35	B3	H	RGB digital output
36	B4	H	RGB digital output
37	VOA0	H	Alpha blend output
38	VOA1	H	Alpha blend output
39	VOA2	H	Alpha blend output

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Pin no.	Pin name	I/O circuit type*	Function
40	VOB	H	OSD display period output
41	DCKO	H	Dot clock output
42	DCKI	F	Dot clock input
43	VSYNC	F	Vertical synchronous input
44	HSYNC	F	Horizontal synchronous input
45	VSSP	—	Dot clock PLL ground
46	VDDP	—	Dot clock PLL power supply
47	VCI	—	VCO control voltage input
48	CPO	M	Charge pump output
49	VSSD	—	RGB analog output GND
50	VDDD	—	RGB analog output power supply
51	VREF	M	RGB analog output reference power supply
52	VRO	M	RGB analog output resistance connected pin
53	ROUT	M	R output (analog)
54	GOUT	M	G output (analog)
55	BOUT	M	B output (analog)
56	V <sub>cc</sub>	—	3.3 V power supply
57	UDP	USB	USB pin
58	UDM	USB	USB pin
59	V <sub>ss</sub>	—	GND
60	C	—	C pin for a regulator
61	V <sub>ss</sub>	—	GND
62	V <sub>cc</sub>	—	3.3 V power supply
63	HWDE	F	Hardware watchdog enable input
64	PK1	G	General-purpose I/O port
	X0A		32kHz oscillation pin
65	PK0	G	General-purpose I/O port
	X1A		32 kHz oscillation pin
66	V <sub>ss</sub>	—	GND
67	X1	A	Main oscillation pin
68	X0	A	Main oscillation pin

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Pin no.	Pin name	I/O circuit type*	Function
69	MD1	F, L	Mode pin
70	MD0	F, L	Mode pin
71	$\overline{\text{INIT}}$	F, L	Initial (reset) pin
72	P70	D	General-purpose I/O port
	AN0		A/D converter ch.0 analog input
	OUT0_1		Output compare ch.0 output (Port 1)
73	P71	D	General-purpose I/O port
	AN1		A/D converter ch.1 analog input
	OUT1_1		Output compare ch.1 output (Port 1)
74	P72	D	General-purpose I/O port
	AN2		A/D converter ch.2 analog input
	TMO0		Reload timer ch.0 output
	OUT2_1		Output compare ch.2 output (Port 1)
75	P73	D	General-purpose I/O port
	AN3		A/D converter ch.3 analog input
	TMO1		Reload timer ch.1 output
	OUT3_1		Output compare ch.3 output (Port 1)
76	P74	D	General-purpose I/O port
	AN4		A/D converter ch.4 analog input
	TMO2		Reload timer ch.2 output
77	P75	D	General-purpose I/O port
	AN5		A/D converter ch.5 analog input
	SOUT0		Multifunction serial ch.0 output [operation modes 0 to 2]
	TMI0		Reload timer ch.0 input
78	P76	D	General-purpose I/O port
	AN6		A/D converter ch.6 analog input
	SIN0		Multifunction serial ch.0 input
	TMI1		Reload timer ch.1 input

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# MB91610 Series

Pin no.	Pin name	I/O circuit type*	Function
79	P77	D	General-purpose I/O port
	AN7		A/D converter ch.7 analog input
	SCK0		Multifunction serial ch.0 clock [operation modes 0 to 2]
	TMI2		Reload timer ch.2 input
80	AV <sub>cc</sub>	—	A/D converter analog power supply
81	AV <sub>ss</sub>	—	A/D converter GND
82	AVRH	—	A/D converter analog reference power supply
83	$\overline{\text{TRST}}$	E	Tool reset input for DSU4 N.C. pin for MASK products.
84	ICLK	K	Clock pin for DSU4 N.C. pin for MASK products.
85	IBREAK	I	Break pin for DSU4 N.C. pin for MASK products.
86	ICS0	H	DSU4 status N.C. pin for MASK products.
87	ICS1	H	DSU4 status N.C. pin for MASK products.
88	ICS2	H	DSU4 status N.C. pin for MASK products.
89	V <sub>cc</sub>	—	3.3 V power supply
90	V <sub>ss</sub>	—	GND
91	C	—	C pin for a regulator
92	ICD0	J	DSU4 data N.C. pin for MASK products.
93	ICD1	J	DSU4 data N.C. pin for MASK products.
94	ICD2	J	DSU4 data N.C. pin for MASK products.
95	ICD3	J	DSU4 data N.C. pin for MASK products.
96	P00	B	General-purpose I/O port
	TIOA0		Base timer ch.0 TIOA
	SOUT0_1		Multifunction serial ch.0 output (Port 1) [operation modes 0 to 2]
	IN0		Input capture ch.0 input

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Pin no.	Pin name	I/O circuit type*	Function
97	P01	B	General-purpose I/O port
	TIOB0		Base timer ch.0 TIOB
	SIN0_1		Multifunction serial ch.0 input (Port 1)
	IN1		Input capture ch.1 input
98	P02	B	General-purpose I/O port
	TIOA1		Base timer ch.1 TIOA
	SCK0_1		Multifunction serial ch.0 clock (Port 1) [operation modes 0 to 2]
	IN2		Input capture ch.2 input
99	P03	B	General-purpose I/O port
	TIOB1		Base timer ch.1 TIOB
	IN3		Input capture ch.3 input
100	P04	B	General-purpose I/O port
	TIOA2		Base timer ch.2 TIOA
	SOUT1 (SDA1)		Multifunction serial ch.1 output [operation modes 0 to 2] I <sup>2</sup> C ch.1 serial data line [operation mode 4]
101	P05	B	General-purpose I/O port
	TIOB2		Base timer ch.2 TIOB
	SIN1		Multifunction serial ch.1 input
102	P06	B	General-purpose I/O port
	TIOA3		Base timer ch.3 TIOA
	SCK1 (SCL1)		Multifunction serial ch.1 clock [operation modes 0 to 2] I <sup>2</sup> C ch.1 serial clock line [operation mode 4]
103	P07	B	General-purpose I/O port
	TIOB3		Base timer ch.3 TIOB
104	P10	B	General-purpose I/O port
	TIOA4		Base timer ch.4 TIOA
	SOUT2 (SDA2)		Multifunction serial ch.2 output [operation modes 0 to 2] I <sup>2</sup> C ch.2 serial data line [operation mode 4]
	INT0		External interrupt 0 input

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# MB91610 Series

Pin no.	Pin name	I/O circuit type*	Function
105	P11	B	General-purpose I/O port
	TIOB4		Base timer ch.4 TIOB
	SIN2		Multifunction serial ch.2 input
	INT1		External interrupt 1 input
106	P12	B	General-purpose I/O port
	TIOA5		Base timer ch.5 TIOA
	SCK2 (SCL2)		Multifunction serial ch.2 clock [operation modes 0 to 2]
			I <sup>2</sup> C ch.2 serial clock line [operation mode 4]
	INT2		External interrupt 2 input
107	P13	B	General-purpose I/O port
	TIOB5		Base timer ch.5 TIOB
	INT3		External interrupt 3 input
108	P14	B	General-purpose I/O port
	TIOA6		Base timer ch.6 TIOA
	SOUT3 (SDA3)		Multifunction serial ch.3 output [operation modes 0 to 2]
			I <sup>2</sup> C ch.3 serial data line [operation mode 4]
	INT4		External interrupt 4 input
109	P15	B	General-purpose I/O port
	TIOB6		Base timer ch.6 TIOB
	SIN3		Multifunction serial ch.3 input
	INT5		External interrupt 5 input
110	P16	B	General-purpose I/O port
	TIOA7		Base timer ch.7 TIOA
	SCK3 (SCL3)		Multifunction serial ch.3 clock [operation modes 0 to 2]
			I <sup>2</sup> C ch.3 serial clock line [operation mode 4]
	INT6		External interrupt 6 input
111	P17	B	General-purpose I/O port
	TIOB7		Base timer ch.7 TIOB
	INT7		External interrupt 7 input
112	P20	C	General-purpose I/O port
	SOUT8 (SDA8)		Multifunction serial ch.8 output [operation modes 0 to 2]
			I <sup>2</sup> C ch.8 serial data line [operation mode 4]

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Pin no.	Pin name	I/O circuit type*	Function
113	P21	C	General-purpose I/O port
	SIN8		Multifunction serial ch.8 input
114	P22	C	General-purpose I/O port
	SCK8 (SCL8)		Multifunction serial ch.8 clock [operation modes 0 to 2]
			I <sup>2</sup> C ch.8 serial clock line [operation mode 4]
115	P23	C	General-purpose I/O port
	RCIN_1		Remote control I/O (1)
116	P24	C	General-purpose I/O port
	SOUT9 (SDA9)		Multifunction serial ch.9 output [operation modes 0 to 2]
			I <sup>2</sup> C ch.9 serial data line [operation mode 4]
OUT0	Output compare ch.0 output		
117	P25	C	General-purpose I/O port
	SIN9		Multifunction serial ch.9 input
	OUT1		Output compare ch.1 output
118	P26	C	General-purpose I/O port
	SCK9 (SCL9)		Multifunction serial ch.9 clock [operation modes 0 to 2]
			I <sup>2</sup> C ch.9 serial clock line [operation mode 4]
OUT2	Output compare ch.2 output		
119	P27	C	General-purpose I/O port
	OUT3		Output compare ch.3 output
120	V <sub>SS</sub>	—	GND

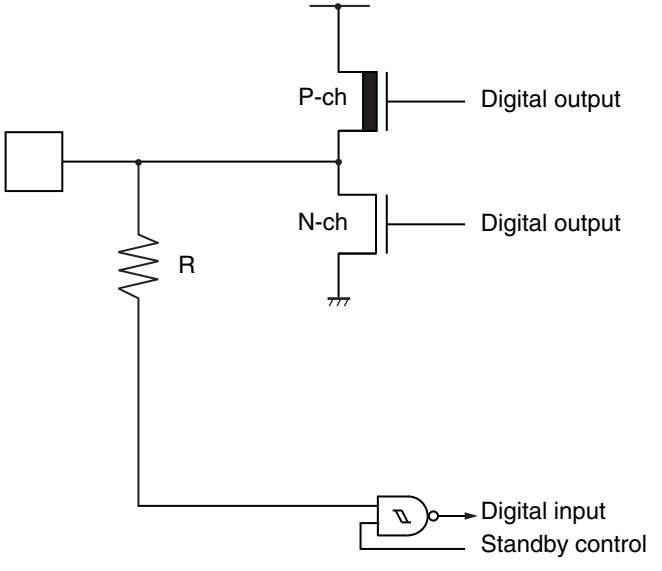
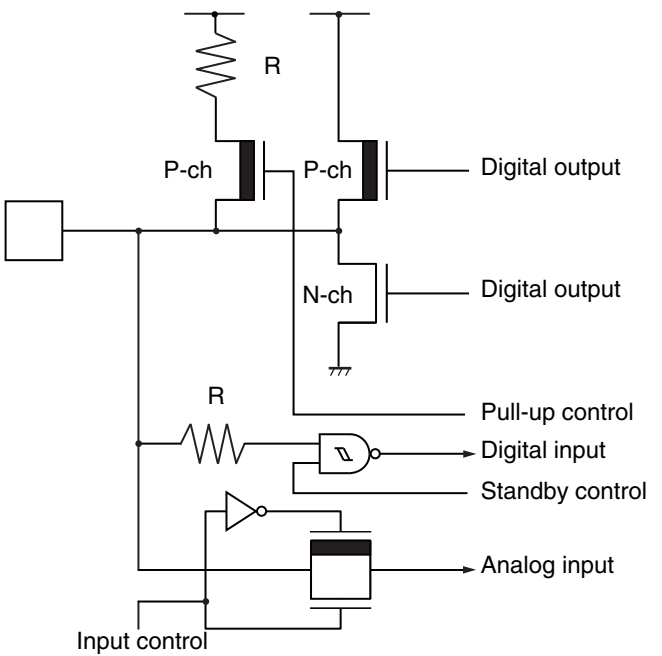
\* : Refer to “■ I/O CIRCUIT TYPE” for details on the I/O circuit types.

# MB91610 Series

## ■ I/O CIRCUIT TYPE

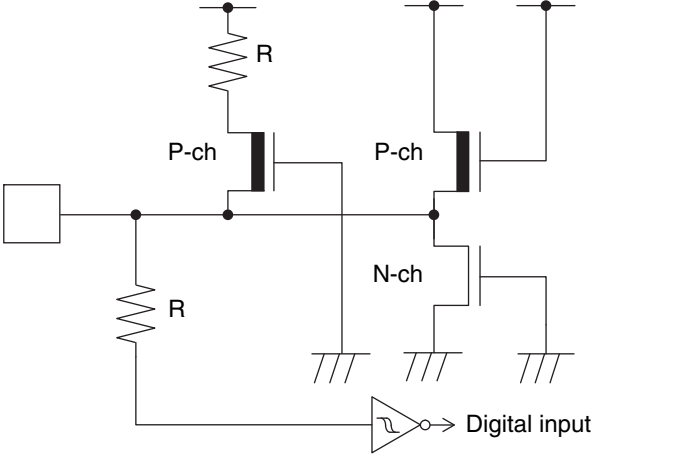
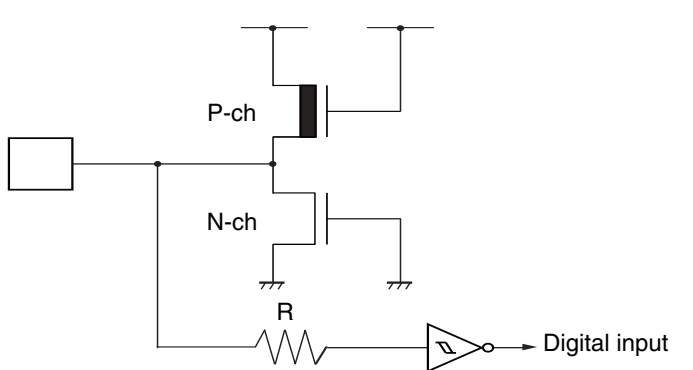
Type	Circuit	Remarks
A		<ul style="list-style-type: none"> <li>• Oscillation feedback resistance approx. 1 MΩ</li> <li>• With standby control</li> </ul>
B		<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• With pull-up control</li> <li>• With standby control</li> </ul> <p>Note: When this pin is used as an I<sup>2</sup>C pin, the digital output P-ch transistor is always off.</p>

(Continued)

Type	Circuit	Remarks
C	 <p>The diagram shows a CMOS output stage. A pull-up resistor labeled 'R' is connected to the output node. The output node is connected to the gate of a P-channel MOSFET (P-ch) and the gate of an N-channel MOSFET (N-ch). The P-ch transistor's source is connected to VDD, and its drain is connected to the output node. The N-ch transistor's source is connected to ground, and its drain is connected to the output node. The output node is also connected to a digital input terminal. A standby control input is connected to the gates of both transistors through an inverter.</p>	<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• 5 V tolerant input</li> <li>• With standby control</li> </ul> <p>Note: When this pin is used as an I<sup>2</sup>C pin, the digital output P-ch transistor is always off.</p>
D	 <p>The diagram shows a more complex CMOS output stage. It includes a pull-up resistor 'R' connected to the output node. The output node is connected to the gates of a P-channel MOSFET (P-ch) and an N-channel MOSFET (N-ch). The P-ch transistor's source is connected to VDD, and its drain is connected to the output node. The N-ch transistor's source is connected to ground, and its drain is connected to the output node. The output node is also connected to a digital input terminal. A pull-up control input is connected to the gates of both transistors through an inverter. A standby control input is connected to the gates of both transistors through an inverter. An analog input is connected to the gates of both transistors through an inverter. An input control input is connected to the gates of both transistors through an inverter.</p>	<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• With input control</li> <li>• Analog input</li> <li>• With pull-up control</li> <li>• With standby control</li> </ul> <p>Note: When this pin is used as an I<sup>2</sup>C pin, the digital output P-ch transistor is always off.</p>

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# MB91610 Series

Type	Circuit	Remarks
E		<ul style="list-style-type: none"> <li>• CMOS level hysteresis input</li> <li>• With pull-up</li> </ul>
F		CMOS level hysteresis input

(Continued)

Type	Circuit	Remarks
G	<p>The diagram for Type G shows two input pins, X1A and X0A. X1A is connected to a P-channel MOSFET (Digital output), an N-channel MOSFET (Digital output), a resistor R, a NAND gate (Digital input, Standby control), and a clock input. X0A is connected to a P-channel MOSFET (Digital output), an N-channel MOSFET (Digital output), a resistor R, and a NAND gate (Digital input, Standby control). A standby control circuit is also shown.</p>	<ul style="list-style-type: none"> <li>• Oscillation feedback resistance approx. 10MΩ</li> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• With standby control</li> </ul>
H	<p>The diagram for Type H shows a single input pin connected to a P-channel MOSFET (Digital output) and an N-channel MOSFET (Digital output).</p>	<p>CMOS level output</p>

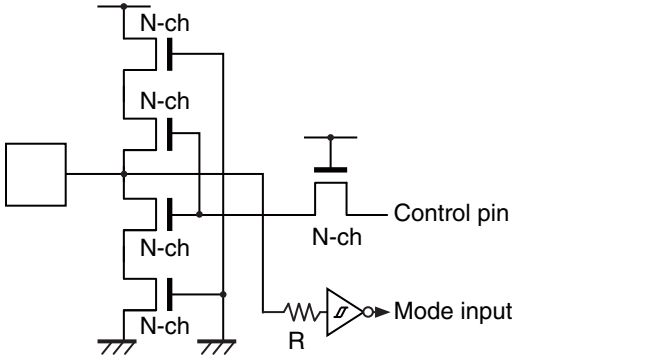
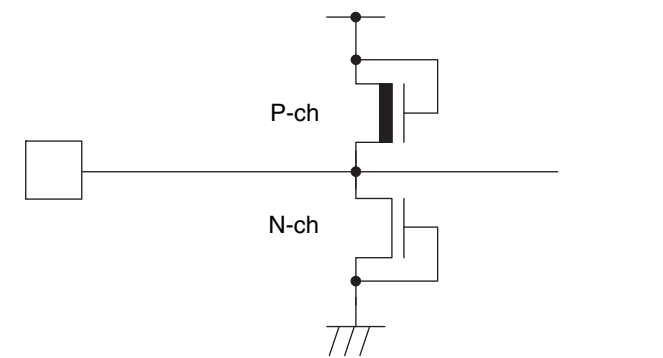
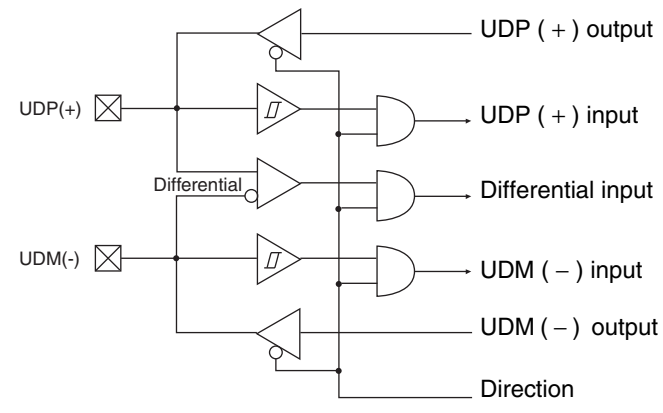
(Continued)

# MB91610 Series

Type	Circuit	Remarks
I		<ul style="list-style-type: none"> <li>• CMOS level hysteresis input</li> <li>• With Pull-down control</li> </ul>
J		<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level input</li> <li>• With Pull-down control</li> </ul>
K		CMOS level output (8 mA)

(Continued)

(Continued)

Type	Circuit	Remarks
L		<ul style="list-style-type: none"> <li>Flash memory product only</li> <li>CMOS level hysteresis input</li> <li>High voltage control for testing Flash memory</li> </ul>
M		Analog pin
USB		USB I/O pin

## ■ PRECAUTIONS FOR HANDLING THE DEVICES

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your FUJITSU SEMICONDUCTOR semiconductor devices.

### 1. Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

#### • Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

#### • Recommended Operating Conditions

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

#### • Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

##### (1) Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

##### (2) Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device. Therefore, avoid this type of connection.

##### (3) Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

##### - PLL pin for OSD (recommended pin handling when PLL for OSD is not in use)

Pin no.	Pin name	Recommended handling of unused pin
45	VSSP	V <sub>SS</sub> (PLL macro GND)
46	VDDP	V <sub>SS</sub> (PLL macro power supply)
47	VCI	V <sub>SS</sub>
48	CPO	V <sub>SS</sub>

##### - Analog OSD (recommended pin handling when analog OSD is not in use)

Pin no.	Pin name	Recommended handling of unused pin
49	VSSD	V <sub>SS</sub> (DAC macro GND)

50	VDDD	V <sub>SS</sub> (DAC macro power supply)
51	VREF	V <sub>SS</sub>
52	VRO	V <sub>SS</sub>
53	ROUT	V <sub>SS</sub>
54	GOUT	V <sub>SS</sub>
55	BOUT	V <sub>SS</sub>

- Digital OSD (recommended pin handling when digital OSD is not in use)

Pin no.	Pin name	Recommended handling of unused pin
19	R0	OPEN
20	R1	OPEN
21	R2	OPEN
22	R3	OPEN
23	R4	OPEN
24	G0	OPEN
25	G1	OPEN
26	G2	OPEN
27	G3	OPEN
28	G4	OPEN
29	G5	OPEN
32	B0	OPEN
33	B1	OPEN
34	B2	OPEN
35	B3	OPEN
36	B4	OPEN

- Other OSD pins

Pin no.	Pin name	Recommended handling of unused pin
37	VOA0	OPEN
38	VOA1	OPEN
39	VOA2	OPEN
40	VOB	OPEN
41	DCKO	OPEN
42	DCKI	pull-down
43	VSYNC	pull-down
44	HSYNC	pull-down

- USB (example of pin handling when USB is not in use)

Pin no.	Pin name	Recommended handling of unused pin
57	UDP	pull-down
58	UDM	pull-down

- DSU pin

Pin no.	Pin name	Recommended handling of unused pin
83	$\overline{\text{TRST}}$	Reset signal input from user board
84	ICLK	OPEN
85	IBREAK	OPEN
86	ICS0	OPEN
87	ICS1	OPEN
88	ICS2	OPEN
92	ICD0	OPEN
93	ICD1	OPEN
94	ICD2	OPEN
95	ICD3	OPEN

# MB91610 Series

- Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

- Note: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:
- (a) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
  - (b) Be sure that abnormal current flows do not occur during the power-on sequence.

- Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

- Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

- Precautions Related to Usage of Devices

FUJITSU SEMICONDUCTOR semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with FUJITSU Semiconductor sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

## 2. Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under FUJITSU SEMICONDUCTOR's recommended conditions. For detailed information about mount conditions, contact your sales representative.

### • Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder.

In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

### • Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. FUJITSU SEMICONDUCTOR recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with FUJITSU SEMICONDUCTOR ranking of recommended conditions.

### • Lead-Free Packaging

Note: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

### • Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

- (a) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
- (b) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5 °C and 30 °C. When you open Dry Package that recommends humidity 40% to 70% relative humidity.
- (c) When necessary, FUJITSU SEMICONDUCTOR packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
- (d) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

# MB91610 Series

- Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the FUJITSU SEMICONDUCTOR recommended conditions for baking.

Condition: + 125 °C/24 h

- Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

- (a) Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
- (b) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
- (c) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ). Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
- (d) Ground all fixtures and instruments, or protect with anti-static measures.
- (e) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

- Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

- (1) Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

- (2) Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

- (3) Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

- (4) Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

- (5) Smoke, Flame

Note : Plastic molded devices are flammable, and therefore should not be used near combustible substances.

If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of FUJITSU SEMICONDUCTOR products in other special environmental conditions should consult with sales representatives.

## ■ HANDLING DEVICES

### • Power supply pins

In products with multiple  $V_{CC}$  and  $V_{SS}$  pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating. Moreover, connect the current supply source with the  $V_{CC}$  and  $V_{SS}$  pins of this device at low impedance.

It is also advisable that a ceramic capacitor of approximately  $0.1 \mu\text{F}$  be connected as a bypass capacitor between  $V_{CC}$  and  $V_{SS}$  near this device.

### • Crystal oscillator circuit

Noise near the X0 and X1 pins may cause the device to malfunction. Design the printed circuit board so that X0, X1, the crystal oscillator (or ceramic oscillator), and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended that the PC board artwork be designed such that the X0 and X1 pins are surrounded by ground plane as this is expected to produce stable operation.

### • OSDC output pin

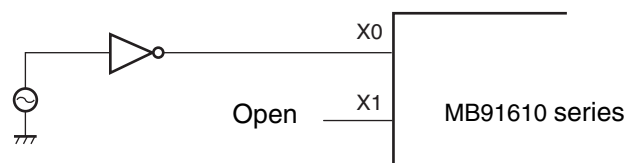
The OSDC output pins (R0 to R4, G0 to G5, B0 to B4, VOA0 to VOA2, VOB, DCKO) are high-speed corresponded output pin.

Adjust the signal waveform such as by inserting damping resistor on the board as needed.

### • Using an external clock

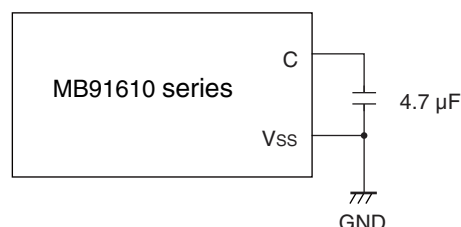
When using an external clock, the clock signal should be input to the X0 pin only and the X1 pin should be kept open.

#### • Example of Using an External Clock



### • C Pin

As MB91610 series includes an internal regulator, always connect a bypass capacitor of approximately  $4.7 \mu\text{F}$  to the C pin for use by the regulator.



# MB91610 Series

- Mode pins (MD0, MD1)

Connect the MD pin (MD0, MD1) directly to  $V_{CC}$  or  $V_{SS}$  pins. Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and  $V_{CC}$  pins or  $V_{SS}$  pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

- Notes on power-on

- To ensure that the internal regulator and the oscillator have stabilized immediately after the power is turned on, keep an “L” level input connected to the  $\overline{INIT}$  pin for the duration of the regulator voltage stabilization wait time + the oscillator start time of the oscillator + the main oscillator stabilization wait time.

- Turn power on/off in the following order

Turning on :  $V_{CC} \rightarrow AV_{CC} \rightarrow AVRH$

Turning off :  $AVRH \rightarrow AV_{CC} \rightarrow V_{CC}$

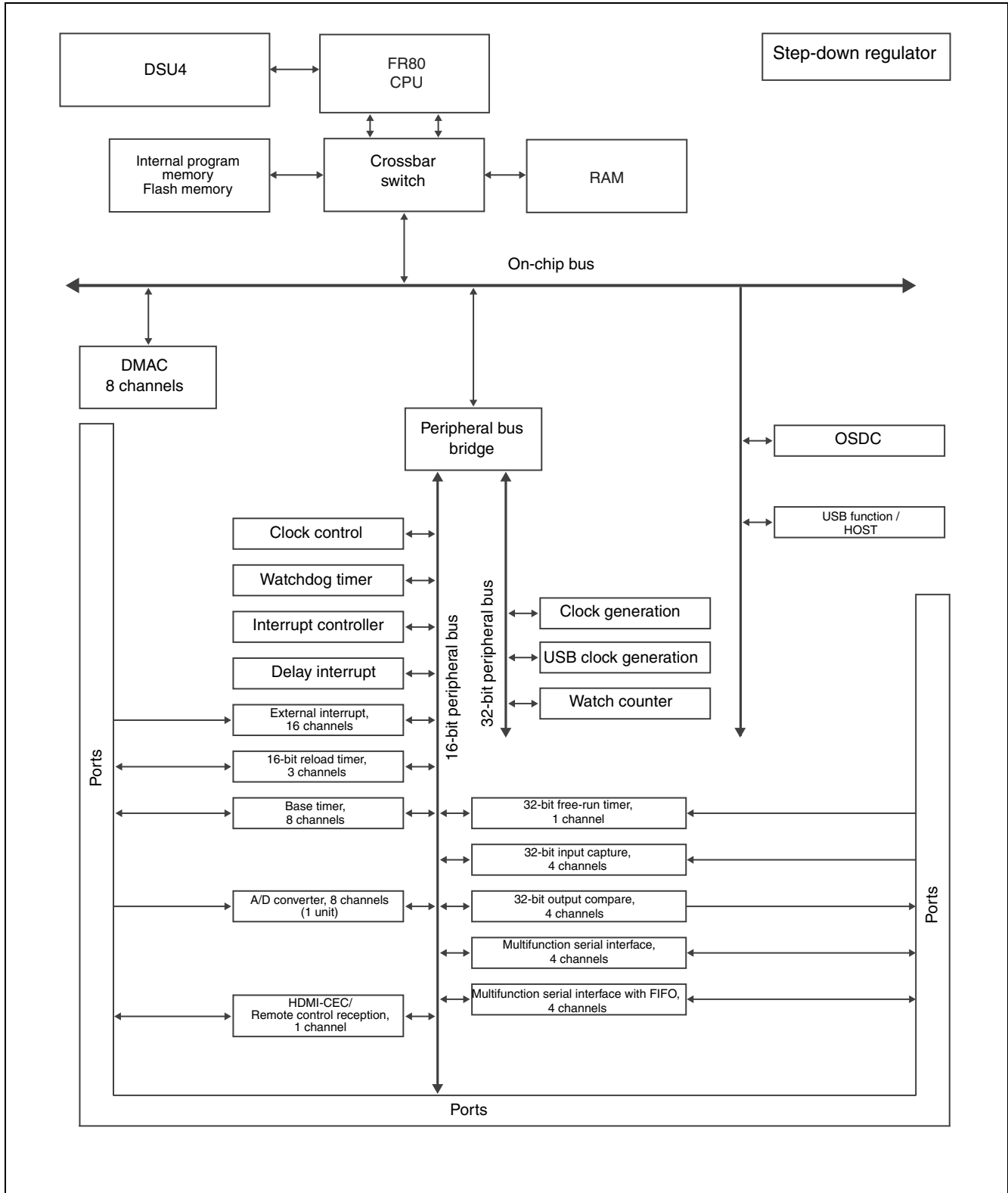
- Release the reset ( $\overline{INIT}$  pin “L” level to “H” level) after the power supply has stabilized.

- Caution on operations during PLL clock mode

On this microcontroller, if in case the crystal oscillator breaks off or an external reference clock input stops while the PLL clock mode is selected, a self-oscillator circuit contained in the PLL may continue its operation at its self-running frequency.

However, Fujitsu Semiconductor will not guarantee results of operations if such failure occurs.

## ■ BLOCK DIAGRAM



## ■ MEMORY SPACE

### 1. Memory Space

The FR family has 4 Gbytes of logical address space ( $2^{32}$  addresses) available to the CPU by linear access.

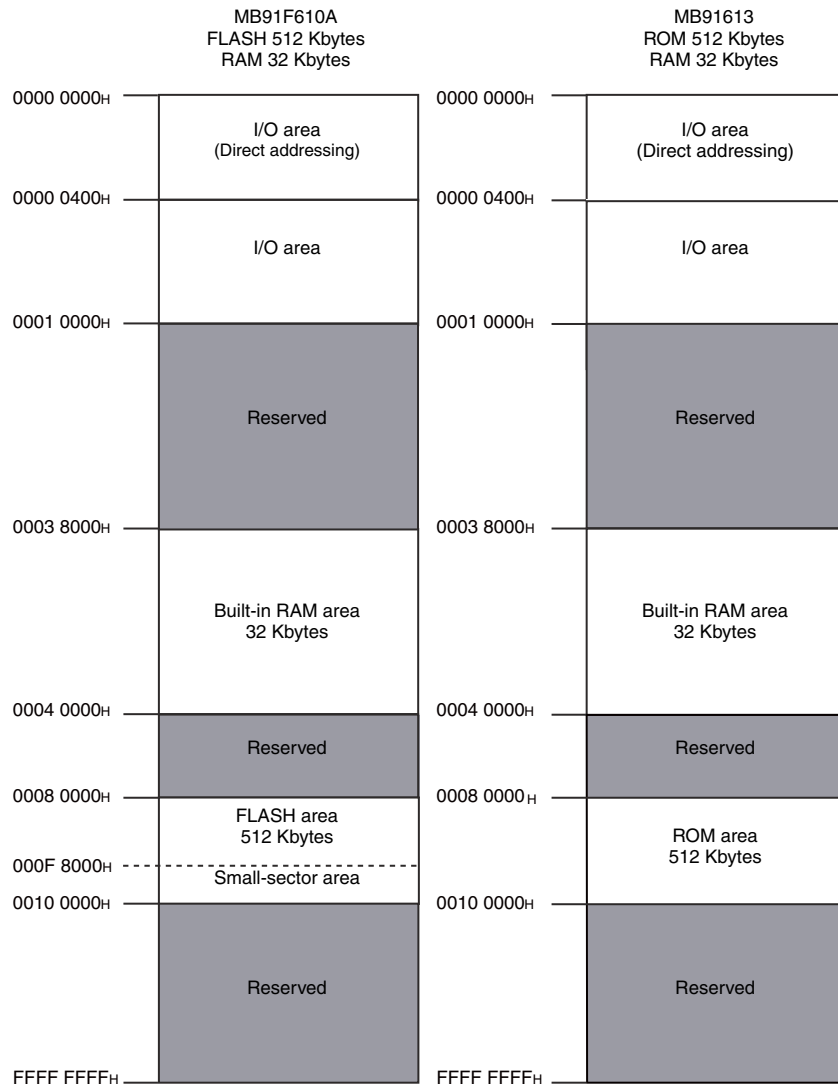
#### • Direct Addressing Areas

The following areas in the address space are used as I/O areas.

These areas are called direct addressing areas, and the address of an operand in these areas can be specified directly within an instruction. The size of the directly addressable area depends on the length of the data being accessed as follows.

- Byte data access : 0000 0000<sub>H</sub> to 0000 00FF<sub>H</sub>
- Half word data access : 0000 0000<sub>H</sub> to 0000 01FF<sub>H</sub>
- Word data access : 0000 0000<sub>H</sub> to 0000 03FF<sub>H</sub>

## 2. Memory Map



- Notes:
- Small sector area is related to flash products only. Please refer to the Flash Memory section of the Hardware Manual for more details.
  - Do not access the reserved areas.

# MB91610 Series

## ■ I/O MAP

[How to read the table]

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 0000 <sub>H</sub>	PDR0 [R/W] B, H XXXXXXXX	PDR1 [R/W] B, H XXXXXXXX	PDR2 [R/W] B, H XXXXXXXXXXXX	PDR3 [R/W] B, H XXXXXXXX	Port data register
0000 003C <sub>H</sub>	WDTCR0 [R/W] B, H -0--0000	WDTCPR0 [R/W] B, H 00000000	—		Watchdog timer
0000 0040 <sub>H</sub>	EIRRO [R/W] B, H, W 000 0000	ENIRO [R/W] B, H, W 00000000	ELVRO [R/W] B, H, W 00000000 00000000		External interrupt 0 to 7

Initial value after reset — : Reserved area

“1” : Initial value“1”

“0” : Initial value“0”

“X” : Initial value undefined

“ - ” : Reserved bit or undefined bit

Access unit

(B : byte, H : half word, W : word)

Read/write attribute

“R” : Indicates that there is a read only bit.

“R/W” : Indicates that there is a read/write bit.

“W” : Indicates that there is a write only bit.

Register name (column 1 of the register is at address 4n, column 2 is at address 4 n + 2...)

Leftmost register address (For word-length access, column 1 of the register is the MSB of the data.)

Notes : • When performing a data access, the addresses should be as below.

- Word access : Address should be multiples of 4 (least significant 2 bits should be “00<sub>B</sub>”)

- Half word access : Address should be multiples of 2 (least significant bit should be “0<sub>B</sub>”)

- Byte access : —

• Do not access the reserved areas.

# MB91610 Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 0000 <sub>H</sub>	PDR0 [R/W] B,H XXXXXXXX	PDR1 [R/W] B,H XXXXXXXX	PDR2 [R/W] B,H XXXXXXXX	PDR3 [R/W] B,H XXXXXXXX	Port data register
0000 0004 <sub>H</sub>	—	PDR5 [R/W] B,H XXXXXXXX	—	PDR7[R/W] B,H XXXXXXXX	
0000 0008 <sub>H</sub> to 0000 0010 <sub>H</sub>	—				
0000 0014 <sub>H</sub>	PDRK [R/W] B -----XX	—			
0000 0018 <sub>H</sub> to 0000 001C <sub>H</sub>	—				
0000 0020 <sub>H</sub>	RCCR [R/W] B 0---0000	RCST [R/W] B 00000000	RCSHW [R/W] B 00000000	RCDAHW [R/W] B 00000000	HDMI-CEC/ Remote controller
0000 0024 <sub>H</sub>	RCDBHW [R/W] B 00000000	—	RCADR1 [R/W] B ---00000	RCADR2 [R/W] B ---00000	
0000 0028 <sub>H</sub>	RCDTHH [R] B,H,W 00000000	RCDTHL [R] B,H,W 00000000	RCDTLH [R] B,H,W 00000000	RCDTLL [R] B,H,W 00000000	
0000 002C <sub>H</sub>	RCCKD [R/W] H ---00000 00000000		—		
0000 0030 <sub>H</sub> to 0000 0038 <sub>H</sub>	—				Reserved
0000 003C <sub>H</sub>	WDCR0[R/W] B,H 00000000	WDCPR0[R/W] B,H 00000000	WDCR1[R] B,H XXXX0000	WDCPR1[R/W] B,H 00000000	Watchdog timer
0000 0040 <sub>H</sub>	EIRR0[R/W] B,H,W 00000000	ENIR0[R/W] B,H,W 00000000	ELVR0[R/W] B,H,W 00000000 00000000		External interrupt 0 to 7
0000 0044 <sub>H</sub>	DICR [R/W] B -----0	—			Delay interrupt
0000 0048 <sub>H</sub>	TMRLRA0 [R/W] H XXXXXXXX XXXXXXXX		TMR0 [R] H XXXXXXXX XXXXXXXX		16-bit reload timer ch.0
0000 004C <sub>H</sub>	—		TMCSR0 [R/W] H --000000 --000000		
0000 0050 <sub>H</sub>	TMRLRA1 [R/W] H XXXXXXXX XXXXXXXX		TMR1 [R] H XXXXXXXX XXXXXXXX		16-bit reload timer ch.1
0000 0054 <sub>H</sub>	—		TMCSR1 [R/W] H --000000 --000000		

(Continued)

# MB91610 Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 0058 <sub>H</sub>	TMRLRA2 [R/W] H XXXXXXXX XXXXXXXX		TMR2 [R] H XXXXXXXX XXXXXXXX		16-bit reload timer ch.2
0000 005C <sub>H</sub>	—		TMCSR2 [R/W] H --000000 --000000		
0000 0060 <sub>H</sub>	SCR0 [R/W] B,H,W 0--00000	SMR0 [R/W] B,H,W 000-0000	SSR0 [R,R/W] B,H,W 0-000011	ESCR0 [R/W] B,H,W -0000000	Multi-function serial interface ch.0
0000 0064 <sub>H</sub>	RDR0[R]/TDR0[W] B,H,W*1 -----0 00000000		BGR10[R/W]H,W 00000000	BGR00[R/W] H,W 00000000	
0000 0068 <sub>H</sub>	SCR1[R/W] IBCR1[R,R/W] B,H,W*2 0--00000	SMR1 [R/W] B,H,W 000-0000	SSR1 [R,R/W] B,H,W 0-000011	ESCR1[R/W] IBSR1[R,R/W] B,H,W*2 -0000000	Multi-function serial interface ch.1
0000 006C <sub>H</sub>	RDR1[R]/TDR1[W] B,H,W*1 -----0 00000000		BGR11[R/W] H,W 00000000	BGR01[R/W] H,W 00000000	
0000 0070 <sub>H</sub>	ISMK1 [R/W] B,H*2 -----	ISBA1 [R/W] B,H*2 -----	—		
0000 0074 <sub>H</sub>	SCR2[R/W] IBCR2[R,R/W] B,H,W*2 0--00000	SMR2 [R/W] B,H,W 000-0000	SSR2 [R,R/W] B,H,W 0-000011	ESCR2[R/W] IBSR2 [R,R/W] B,H,W*2 -0000000	Multi-function serial interface ch.2
0000 0078 <sub>H</sub>	RDR2[R]/TDR2[W] B,H,W*1 -----0 00000000		BGR12[R/W] H,W 00000000	BGR02[R/W] H,W 00000000	
0000 007C <sub>H</sub>	ISMK2 [R/W] B,H*2 -----	ISBA2 [R/W] B,H*2 -----	—		
0000 0080 <sub>H</sub>	SCR3[R/W] IBCR3[R,R/W] B,H,W*2 0--00000	SMR3 [R/W] B,H,W 000-0000	SSR3 [R,R/W] B,H,W 0-000011	ESCR3[R/W] IBSR3[R,R/W] B,H,W*2 -0000000	Multi-function serial interface ch.3
0000 0084 <sub>H</sub>	RDR3[R]/TDR3[W] B,H,W*1 -----0 00000000		BGR13[R/W] H,W 00000000	BGR03[R/W] H,W 00000000	
0000 0088 <sub>H</sub>	ISMK3 [R/W] B,H*2 -----	ISBA3 [R/W] B,H*2 -----	—		
0000 008C <sub>H</sub> to 0000 00BC <sub>H</sub>	—				Reserved

(Continued)

# MB91610 Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 00C0 <sub>H</sub>	RDRM0 [R]/ TDRM0[W] B,H,W 00000000	RDRM1 [R]/ TDRM1[W] B,H,W 00000000	RDRM2 [R]/ TDRM2[W] B,H,W 00000000	RDRM3 [R]/ TDRM3[W] B,H,W 00000000	Multi-function serial interface data register (mirror)
0000 00C4 <sub>H</sub>	—				
0000 00C8 <sub>H</sub>	SSEL0123 [R/W] B -----00	—			Multi-function serial interface serial clock selection
0000 00CC <sub>H</sub>	—				Reserved
0000 00D0 <sub>H</sub>	SCR8 [R/W] IBCR8 [R,R/W] B,H,W*2 0--00000	SMR8 [R/W] B,H,W 000-0000	SSR8 [R,R/W] B,H,W 0-000011	ESCR8 [R/W] IBSR8 [R,R/W] B,H,W*2 -0000000	Multi-function serial interface ch. 8 (FIFO)
0000 00D4 <sub>H</sub>	RDR8[R]/TDR8[W] B,H,W*1 -----0 00000000		BGR18 [R/W] H,W 00000000	BGR08 [R,R/W] H,W 00000000	
0000 00D8 <sub>H</sub>	ISMK8 [R/W] B,H*2 -----	ISBA8 [R/W] B,H*2 -----	—		
0000 00DC <sub>H</sub>	FCR18 [R/W] B,H,W ---00100	FCR08 [R,R/W] B,H,W -0000000	FBYTE28 [R/W] B,H,W 00000000	FBYTE18 [R/W] B,H,W 00000000	
0000 00E0 <sub>H</sub>	SCR9 [R/W] IBCR9 [R,R/W] B,H,W*2 0--00000	SMR9 [R/W] B,H,W 000-0000	SSR9 [R,R/W] B,H,W 0-000011	ESCR9 [R/W] IBSR9[R,R/W] B,H,W*2 -0000000	
0000 00E4 <sub>H</sub>	RDR9[R]/TDR9[W] B,H,W*1 -----0 00000000		BGR19 [R/W] H,W 00000000	BGR09 [R/W] H,W 00000000	Multi-function serial interface ch. 9 (FIFO)
0000 00E8 <sub>H</sub>	ISMK9 [R/W] B,H*2 -----	ISBA9 [R/W] B,H*2 -----	—		
0000 00EC <sub>H</sub>	FCR19 [R/W] B,H,W ---00100	FCR09 [R,R/W] B,H,W -0000000	FBYTE29 [R/W] B,H,W 00000000	FBYTE19 [R/W] B,H,W 00000000	

(Continued)

# MB91610 Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 00F0 <sub>H</sub>	SCR10 [R/W] IBCR10 [R,R/W] B,H,W*2 0--00000	SMR10 [R/W] B,H,W 000-0000	SSR10 [R,R/W] B,H,W 0-000011	ESCR10 [R/W] IBSR10 [R,R/W] B,H,W*2 -0000000	Multi-function serial interface ch.10 (FIFO)
0000 00F4 <sub>H</sub>	RDR10[R]/TDR10[W] B,H,W*1 -----0 00000000		BGR110 [R/W] H,W 00000000	BGR010 [R/W] H,W 00000000	
0000 00F8 <sub>H</sub>	ISMK10 [R/W] B,H*2 -----	ISBA10 [R/W] B,H*2 -----	—		
0000 00FC <sub>H</sub>	FCR110 [R/W] B,H,W ---00100	FCR010 [R,R/W] B,H,W -0000000	FBYTE210 [R/W] B,H,W 00000000	FBYTE110 [R/W] B,H,W 00000000	
0000 0100 <sub>H</sub>	SCR11 [R/W] IBCR11 [R,R/W] B,H,W*2 0--00000	SMR11 [R/W] B,H,W 000-0000	SSR11 [R,R/W] B,H,W 0-000011	ESCR11 [R/W] IBSR11 [R,R/W] B,H,W*2 -0000000	Multi-function serial interface ch.11 (FIFO)
0000 0104 <sub>H</sub>	RDR11[R]/TDR11[W] B,H,W*1 -----0 00000000		BGR111 [R/W] H,W 00000000	BGR011 [R/W] H,W 00000000	
0000 0108 <sub>H</sub>	ISMK11 [R/W] B,H*2 -----	ISBA11 [R/W] B,H*2 -----	—		
0000 010C <sub>H</sub>	FCR111 [R/W] B,H,W ---00100	FCR011 [R,R/W] B,H,W -0000000	FBYTE211 [R/W] B,H,W 00000000	FBYTE111 [R/W] B,H,W 00000000	
0000 0110 <sub>H</sub>	EIRR1[R/W] B,H,W 00000000	ENIR1[R/W] B,H,W 00000000	ELVR1[R/W] B,H,W 00000000 00000000		External interrupt 8 to 15
0000 0114 <sub>H</sub> to 0000 011C <sub>H</sub>	—				Reserved

(Continued)

# MB91610 Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 0120 <sub>H</sub>	ADCR0[R/W] B,H 000-0000	ADSR0[R,R/W] B,H 00---000	—		A/D converter
0000 0124 <sub>H</sub>	SCCR0[R,R/W] B,H 1000-000	SFNS0[R/W] B,H ----0000	SCFD0[R] B,H XXXXXXXX XX-XXXXX		
0000 0128 <sub>H</sub>	—			SCIS00[R/W] B 00000000	
0000 012C <sub>H</sub>	PCCR0[R,R/W] B,H 1000-000	PFNS0[R/W] B,H -----00	PCFD0[R] B,H XXXXXXXX XXXXXXXX		
0000 0130 <sub>H</sub>	PCIS0[R/W] B 00000000	—	CMPD0[R/W] B,H 00000000	CMPCR0[R/W] B,H 00000000	
0000 0134 <sub>H</sub>	—			ADSS00[R/W] B 00000000	
0000 0138 <sub>H</sub>	ADST00[R/W] B,H 00100000	ADST10[R/W] B,H 00100000	ADCT0[R/W] B -----111	—	
0000 013C <sub>H</sub>	—				Reserved
0000 0140 <sub>H</sub>	BT0TMR[R]H 00000000 00000000		BT0TMCR[R/W] B,H -0000000 00000000		Base timer ch.0
0000 0144 <sub>H</sub>	—	BT0STC[R/W]B 0000-000	—		
0000 0148 <sub>H</sub>	BT0PCSR/BT0PRL[R/W]H XXXXXXXX XXXXXXXX		BT0PDUT/BT0PRLH/BT0DTBF [R/W]H XXXXXXXX XXXXXXXX		
0000 014C <sub>H</sub>	—				
0000 0150 <sub>H</sub>	BT1TMR[R]H 00000000 00000000		BT1TMCR[R/W] B,H -0000000 00000000		Base timer ch.1
0000 0154 <sub>H</sub>	—	BT1STC[R/W]B 0000-000	—		
0000 0158 <sub>H</sub>	BT1PCSR/BT1PRL[R/W]H XXXXXXXX XXXXXXXX		BT1PDUT/BT1PRLH/BT1DTBF [R/W]H XXXXXXXX XXXXXXXX		
0000 015C <sub>H</sub>	—				

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# MB91610 Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 0160 <sub>H</sub>	BT2TMR[R]H 00000000 00000000		BT2TMCR [R/W] B,H -0000000 00000000		Base timer ch.2
0000 0164 <sub>H</sub>	—	BT2STC[R/W]B 0000-000	—		
0000 0168 <sub>H</sub>	BT2PCSR/BT2PRL[R/W]H XXXXXXXX XXXXXXXX		BT2PDUT/BT2PRLH/BT2DTBF [R/W]H XXXXXXXX XXXXXXXX		
0000 016C <sub>H</sub>	—				
0000 0170 <sub>H</sub>	BT3TMR[R]H 00000000 00000000		BT3TMCR[R/W] B,H -0000000 00000000		Base timer ch.3
0000 0174 <sub>H</sub>	—	BT3STC[R/W]B 0000-000	—		
0000 0178 <sub>H</sub>	BT3PCSR/BT3PRL[R/W]H XXXXXXXX XXXXXXXX		BT3PDUT/BT3PRLH/BT3DTBF [R/W]H XXXXXXXX XXXXXXXX		
0000 017C <sub>H</sub>	BTSEL0123 [R/W] B 00000000	—			
0000 0180 <sub>H</sub> to 0000 01A8 <sub>H</sub>	—				Reserved
0000 01AC <sub>H</sub>	ADCHE [R/W] B,H,W ----- 11111111				A/D channel enable
0000 01B0 <sub>H</sub>	IRPR0H [R] B 000----	—	IRPR1H [R] B,H 000-000-	IRPR1L [R] B,H 000-000-	Interrupt request batch read function
0000 01B4 <sub>H</sub>	—	IRPR2L [R] B,H,W 000----	IRPR3H [R] B,H,W 0000----	—	
0000 01B8 <sub>H</sub>	IRPR4H [R] B,H,W 0000----	—	IRPR5H [R] B,H,W 0000----	IRPR5L [R] B,H,W 0000----	
0000 01BC <sub>H</sub>	—			IRPR7L [R] B,H,W 0000----	
0000 01C0 <sub>H</sub> to 0000 01FC <sub>H</sub>	—				Reserved
0000 0200 <sub>H</sub>	CPCLR0 [R/W] W 11111111 11111111 11111111 11111111				32-bit Free-run timer ch.0
0000 0204 <sub>H</sub>	TCDT0 [R/W] W 00000000 00000000 00000000 00000000				
0000 0208 <sub>H</sub>	TCCSH0 [R/W] B,H 0-----00	TCCSL0 [R/W] B,H -1-00000	—		

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# MB91610 Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 020C <sub>H</sub>	IPCP0 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				32-bit Input capture ch.0 to ch.3
0000 0210 <sub>H</sub>	IPCP1 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0214 <sub>H</sub>	IPCP2 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0218 <sub>H</sub>	IPCP3 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 021C <sub>H</sub>	—	ICS01 [R/W] B 00000000	—	ICS23 [R/W] B 00000000	
0000 0220 <sub>H</sub> to 0000 0230 <sub>H</sub>	—				Reserved
0000 0234 <sub>H</sub>	OCCP0 [R/W] W 00000000 00000000 00000000 00000000				32-bit Output compare ch.0 to ch.3
0000 0238 <sub>H</sub>	OCCP1 [R/W] W 00000000 00000000 00000000 00000000				
0000 023C <sub>H</sub>	OCCP2 [R/W] W 00000000 00000000 00000000 00000000				
0000 0240 <sub>H</sub>	OCCP3 [R/W] W 00000000 00000000 00000000 00000000				
0000 0244 <sub>H</sub>	OCSH1 [R/W] B,H,W ---0--00	OCSL0 [R/W] B,H,W 0000--00	OCSH3 [R/W] B,H,W ---0--00	OCSL2 [R/W] B,H,W 0000--00	
0000 0248 <sub>H</sub> to 0000 031C <sub>H</sub>	—				Reserved
0000 0320 <sub>H</sub>	FCTLR[R/W] H -0--1011 -----		—	FSTR[R] B -----1	Flash memory control
0000 0324 <sub>H</sub> to 0000 0334 <sub>H</sub>	—				Reserved
0000 0338 <sub>H</sub>	—		WREN[R/W] B,H 00000000 00000000		Wild register
0000 033C <sub>H</sub>	—				
0000 0340 <sub>H</sub> to 0000 037C <sub>H</sub>	—				Reserved

(Continued)

# MB91610 Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 0380 <sub>H</sub>	WRAR00[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				Wild register
0000 0384 <sub>H</sub>	WRDR00[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0388 <sub>H</sub>	WRAR01[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0000 038C <sub>H</sub>	WRDR01[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0390 <sub>H</sub>	WRAR02[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0000 0394 <sub>H</sub>	WRDR02[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0398 <sub>H</sub>	WRAR03[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0000 039C <sub>H</sub>	WRDR03[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03A0 <sub>H</sub>	WRAR04[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0000 03A4 <sub>H</sub>	WRDR04[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03A8 <sub>H</sub>	WRAR05[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0000 03AC <sub>H</sub>	WRDR05[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03B0 <sub>H</sub>	WRAR06[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0000 03B4 <sub>H</sub>	WRDR06[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03B8 <sub>H</sub>	WRAR07[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0000 03BC <sub>H</sub>	WRDR07[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03C0 <sub>H</sub>	WRAR08[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0000 03C4 <sub>H</sub>	WRDR08[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03C8 <sub>H</sub>	WRAR09[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0000 03CC <sub>H</sub>	WRDR09[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

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# MB91610 Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 03D0 <sub>H</sub>	WRAR10[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				Wild register
0000 03D4 <sub>H</sub>	WRDR10[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03D8 <sub>H</sub>	WRAR11[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0000 03DC <sub>H</sub>	WRDR11[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03E0 <sub>H</sub>	WRAR12[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0000 03E4 <sub>H</sub>	WRDR12[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03E8 <sub>H</sub>	WRAR13[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0000 03EC <sub>H</sub>	WRDR13[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03F0 <sub>H</sub>	WRAR14[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0000 03F4 <sub>H</sub>	WRDR14[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 03F8 <sub>H</sub>	WRAR15[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0000 03FC <sub>H</sub>	WRDR15[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0400 <sub>H</sub>	DDR0 [R/W] B,H 00000000	DDR1 [R/W] B,H 00000000	DDR2 [R/W] B,H 00000000	DDR3 [R/W] B,H 00000000	Data direction register
0000 0404 <sub>H</sub>	—	DDR5 [R/W] B,H 00000000	—	DDR7[R/W] B,H 00000000	
0000 0408 <sub>H</sub> to 0000 0410 <sub>H</sub>	—				
0000 0414 <sub>H</sub>	DDRK [R/W] B -----00	—			
0000 0418 <sub>H</sub> to 0000 041C <sub>H</sub>	—				
0000 0420 <sub>H</sub>	PCR0 [R/W] B,H 00000000	PCR1 [R/W] B,H 00000000	—		Pull-up control register
0000 0424 <sub>H</sub>	—	PCR5 [R/W] B 00000000	—	PCR7[R/W] B,H 00000000	
0000 0428 <sub>H</sub> to 0000 043C <sub>H</sub>	—				

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# MB91610 Series

Address	Register				Block	
	+ 0	+ 1	+ 2	+ 3		
0000 0440 <sub>H</sub>	ICR00 [R,R/W] B,H,W ---11111	ICR01 [R,R/W] B,H,W ---11111	ICR02 [R,R/W] B,H,W ---11111	ICR03 [R,R/W] B,H,W ---11111	Interrupt control	
0000 0444 <sub>H</sub>	ICR04 [R,R/W] B,H,W ---11111	ICR05 [R,R/W] B,H,W ---11111	ICR06 [R,R/W] B,H,W ---11111	ICR07 [R,R/W] B,H,W ---11111		
0000 0448 <sub>H</sub>	ICR08 [R,R/W] B,H,W ---11111	ICR09 [R,R/W] B,H,W ---11111	ICR10 [R,R/W] B,H,W ---11111	ICR11 [R,R/W] B,H,W ---11111		
0000 044C <sub>H</sub>	ICR12 [R,R/W] B,H,W ---11111	ICR13 [R,R/W] B,H,W ---11111	ICR14 [R,R/W] B,H,W ---11111	ICR15 [R,R/W] B,H,W ---11111		
0000 0450 <sub>H</sub>	ICR16 [R,R/W] B,H,W ---11111	ICR17 [R,R/W] B,H,W ---11111	ICR18 [R,R/W] B,H,W ---11111	ICR19 [R,R/W] B,H,W ---11111		
0000 0454 <sub>H</sub>	ICR20 [R,R/W] B,H,W ---11111	ICR21 [R,R/W] B,H,W ---11111	ICR22 [R,R/W] B,H,W ---11111	ICR23 [R,R/W] B,H,W ---11111		
0000 0458 <sub>H</sub>	ICR24 [R,R/W] B,H,W ---11111	ICR25 [R,R/W] B,H,W ---11111	ICR26 [R,R/W] B,H,W ---11111	ICR27 [R,R/W] B,H,W ---11111		
0000 045C <sub>H</sub>	ICR28 [R,R/W] B,H,W ---11111	ICR29 [R,R/W] B,H,W ---11111	ICR30 [R,R/W] B,H,W ---11111	ICR31 [R,R/W] B,H,W ---11111		
0000 0460 <sub>H</sub>	ICR32 [R,R/W] B,H,W ---11111	ICR33 [R,R/W] B,H,W ---11111	ICR34 [R,R/W] B,H,W ---11111	ICR35 [R,R/W] B,H,W ---11111		
0000 0464 <sub>H</sub>	ICR36 [R,R/W] B,H,W ---11111	ICR37 [R,R/W] B,H,W ---11111	ICR38 [R,R/W] B,H,W ---11111	ICR39 [R,R/W] B,H,W ---11111		
0000 0468 <sub>H</sub>	ICR40 [R,R/W] B,H,W ---11111	ICR41 [R,R/W] B,H,W ---11111	ICR42 [R,R/W] B,H,W ---11111	ICR43 [R,R/W] B,H,W ---11111		
0000 046C <sub>H</sub>	ICR44 [R,R/W] B,H,W ---11111	ICR45 [R,R/W] B,H,W ---11111	ICR46 [R,R/W] B,H,W ---11111	ICR47 [R,R/W] B,H,W ---11111		
0000 0470 <sub>H</sub> to 0000 047C <sub>H</sub>	—					Reserved
0000 0480 <sub>H</sub>	RSTRR [R] B,H,W 11XX---X*3	RSTCR [R/W] B,H,W 000----0	STBCR [R/W] B,H,W 0000--11	SLPRR [R/W] B,H,W 00000000		Reset control/ Power consumption control
0000 0484 <sub>H</sub>	—					

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# MB91610 Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 0488 <sub>H</sub>	DIVR0 [R/W] B,H 000--011	—	DIVR2 [R/W] B 0011----	—	Clock division control
0000 048C <sub>H</sub>	—				
0000 0490 <sub>H</sub>	IORR0 [R/W] B,H,W -0000000	IORR1 [R/W] B,H,W -0000000	IORR2 [R/W] B,H,W -0000000	IORR3 [R/W] B,H,W -0000000	Peripheral DMA transmission request control
0000 0494 <sub>H</sub>	IORR4 [R/W] B,H,W -0000000	IORR5 [R/W] B,H,W -0000000	IORR6 [R/W] B,H,W -0000000	IORR7 [R/W] B,H,W -0000000	
0000 0498 <sub>H</sub> to 0000 049C <sub>H</sub>	—				Reserved
0000 04A0 <sub>H</sub>	PFR0 [R/W] B,H 00000000	PFR1 [R/W] B,H 00000000	PFR2 [R/W] B,H 00000000	PFR3 [R/W] B,H 00000000	Port function register
0000 04A4 <sub>H</sub>	—	PFR5 [R/W] B,H 00000000	—	PFR7[R/W] B,H 00000000	
0000 04A8 <sub>H</sub> to 0000 04B0 <sub>H</sub>	—				
0000 04B4 <sub>H</sub>	PFRK [R/W] B,H ----0000	—			
0000 04B8 <sub>H</sub>	EPFR0 [R/W] B,H ---00-00	EPFR1 [R/W] B,H ---00-00	—		Extended port function register
0000 04BC <sub>H</sub>	—		EPFR6 [R/W] B,H -00-00-0	EPFR7 [R/W] B,H ----0-0-	
0000 04C0 <sub>H</sub>	EPFR8 [R/W] B,H ----0-0-	EPFR9 [R/W] B,H ----00-0	EPFR10 [R/W] B,H ----0---	—	
0000 04C4 <sub>H</sub>	—		EPFR14 [R/W] B,H ----0-0-	EPFR15 [R/W] B,H ----0-0-	
0000 04C8 <sub>H</sub>	EPFR16 [R/W] B,H ----0-0-	EPFR17 [R/W] B,H ----0-0-	—	EPFR19 [R/W] B,H -----1	
0000 04CC <sub>H</sub>	EPFR20 [R/W] B,H ---0--0-	EPFR21 [R/W] B,H ---0--0-	EPFR22 [R/W] B,H ---0--0-	EPFR23 [R/W] B,H ---0--0-	
0000 04D0 <sub>H</sub> , 0000 04D4 <sub>H</sub>	—				
0000 04D8 <sub>H</sub>	—	EPFR33 [R/W] B,H ---0--0-	EPFR34 [R/W] B,H --0-----	—	
0000 04DC <sub>H</sub>	—				

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# MB91610 Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 04E0 <sub>H</sub> to 0000 04EC <sub>H</sub>	—				Reserved
0000 04F0 <sub>H</sub>	ICSEL0[R/W] B,H,W ----000	ICSEL1[R/W] B,H,W ----000	—		DMA start request clear select function
0000 04F4 <sub>H</sub>	ICSEL4[R/W] B,H,W ----00	—	ICSEL6[R/W] B,H,W ----00	ICSEL7[R/W] B,H,W ----0	
0000 04F8 <sub>H</sub>	ICSEL8[R/W] B,H,W ----00	—	ICSEL10[R/W] B,H,W ----0000	ICSEL11[R/W] B,H,W ----0000	
0000 04FC <sub>H</sub>	—				Reserved
0000 0500 <sub>H</sub> to 0000 050C <sub>H</sub>	—				
0000 0510 <sub>H</sub>	CSELR [R/W] B,H,W 001---00	CMONR [R] B,H,W 001---00	MTMCR [R/W] B,H,W 00001111	STMCR [R/W] B,H,W 0000-111	Clock generation/ Main timer/ Sub timer
0000 0514 <sub>H</sub>	PLLCR [R/W] B,H --000000 11110000		CSTBR [R/W] B -0000000	—	
0000 0518 <sub>H</sub>	WCRD [R] B,H --000000	WCRL [R/W] B,H --000000	WCCR [R,R/W] B 00--0000	—	Clock counter
0000 051C <sub>H</sub>	UCCR [R/W] B ----001	—			USB clock generation
0000 0520 <sub>H</sub> to 0000 0BFC <sub>H</sub>	—				Reserved
0000 0C00 <sub>H</sub>	DCCR0 [R/W] W 0----000 --00--00 00000000 0-000000				DMAC
0000 0C04 <sub>H</sub>	DCSR0 [R,R/W] H 0-----0000		DTCR0 [R/W] H 00000000 00000000		
0000 0C08 <sub>H</sub>	DSAR0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C0C <sub>H</sub>	DDAR0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C10 <sub>H</sub>	DCCR1 [R/W] W 0----000 --00--00 00000000 0-000000				
0000 0C14 <sub>H</sub>	DCSR1 [R,R/W] H 0-----0000		DTCR1 [R/W] H 00000000 00000000		
0000 0C18 <sub>H</sub>	DSAR1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C1C <sub>H</sub>	DDAR1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

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# MB91610 Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 0C20 <sub>H</sub>	DCCR2 [R/W] W 0----000 --00--00 00000000 0-000000				DMAC
0000 0C24 <sub>H</sub>	DCSR2 [R,R/W] H 0-----000		DTCR2 [R/W] H 00000000 00000000		
0000 0C28 <sub>H</sub>	DSAR2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C2C <sub>H</sub>	DDAR2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C30 <sub>H</sub>	DCCR3 [R/W] W 0----000 --00--00 00000000 0-000000				
0000 0C34 <sub>H</sub>	DCSR3 [R,R/W] H 0-----000		DTCR3 [R/W] H 00000000 00000000		
0000 0C38 <sub>H</sub>	DSAR3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C3C <sub>H</sub>	DDAR3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C40 <sub>H</sub>	DCCR4 [R/W] W 0----000 --00--00 00000000 0-000000				
0000 0C44 <sub>H</sub>	DCSR4 [R,R/W] H 0-----000		DTCR4 [R/W] H 00000000 00000000		
0000 0C48 <sub>H</sub>	DSAR4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C4C <sub>H</sub>	DDAR4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C50 <sub>H</sub>	DCCR5 [R/W] W 0----000 --00--00 00000000 0-000000				
0000 0C54 <sub>H</sub>	DCSR5 [R,R/W] H 0-----000		DTCR5 [R/W] H 00000000 00000000		
0000 0C58 <sub>H</sub>	DSAR5 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C5C <sub>H</sub>	DDAR5 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C60 <sub>H</sub>	DCCR6 [R/W] W 0----000 --00--00 00000000 0-000000				
0000 0C64 <sub>H</sub>	DCSR6 [R,R/W] H 0-----000		DTCR6 [R/W] H 00000000 00000000		
0000 0C68 <sub>H</sub>	DSAR6 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C6C <sub>H</sub>	DDAR6 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C70 <sub>H</sub>	DCCR7 [R/W] W 0----000 --00--00 00000000 0-000000				
0000 0C74 <sub>H</sub>	DCSR7 [R,R/W] H 0-----000		DTCR7 [R/W] H 00000000 00000000		

(Continued)

# MB91610 Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 0C78 <sub>H</sub>	DSAR7 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
0000 0C7C <sub>H</sub>	DDAR7 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0000 0C80 <sub>H</sub> to 0000 0DF0 <sub>H</sub>	—				
0000 0DF4 <sub>H</sub>	—			DILVR [R,R/W] B ---1111	
0000 0DF8 <sub>H</sub>	DMACR [R/W] W 0----- 0-----				
0000 0DFC <sub>H</sub> to 0000 0F3C <sub>H</sub>	—				Reserved
0000 0F40 <sub>H</sub>	BT4TMR[R]H 00000000 00000000		BT4TMCR[R/W] B,H -0000000 00000000		Base timer ch.4
0000 0F44 <sub>H</sub>	—	BT4STC[R/W]B 0000-000	—		
0000 0F48 <sub>H</sub>	BT4PCSR/BT4PRLL[R/W]H XXXXXXXX XXXXXXXX		BT4PDUT/BT4PRLH/BT4DTBF [R/W]H XXXXXXXX XXXXXXXX		
0000 0F4C <sub>H</sub>	—				
0000 0F50 <sub>H</sub>	BT5TMR[R]H 00000000 00000000		BT5TMCR[R/W] B,H -0000000 00000000		Base timer ch.5
0000 0F54 <sub>H</sub>	—	BT5STC[R/W]B 0000-000	—		
0000 0F58 <sub>H</sub>	BT5PCSR/BT5PRLL[R/W]H XXXXXXXX XXXXXXXX		BT5PDUT/BT5PRLH/BT5DTBF [R/W]H XXXXXXXX XXXXXXXX		
0000 0F5C <sub>H</sub>	—				
0000 0F60 <sub>H</sub>	BT6TMR[R]H 00000000 00000000		BT6TMCR[R/W] B,H -0000000 00000000		Base timer ch.6
0000 0F64 <sub>H</sub>	—	BT6STC[R/W]B 0000-000	—		
0000 0F68 <sub>H</sub>	BT6PCSR/BT6PRLL[R/W]H XXXXXXXX XXXXXXXX		BT6PDUT/BT6PRLH/BT6DTBF [R/W]H XXXXXXXX XXXXXXXX		
0000 0F6C <sub>H</sub>	—				

(Continued)

# MB91610 Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 0F70 <sub>H</sub>	BT7TMR[R]H 00000000 00000000		BT7TMCR[R/W] B,H -0000000 00000000		Base timer ch.7
0000 0F74 <sub>H</sub>	—	BT7STC[R/W]B 0000-000	—		
0000 0F78 <sub>H</sub>	BT7PCSR/BT7PRLL[R/W]H XXXXXXXX XXXXXXXX		BT7PDUT/BT7PRLH/BT7DTBF [R/W]H XXXXXXXX XXXXXXXX		
0000 0F7C <sub>H</sub>	BTSEL4567 [R/W] B 00000000	—			
0000 0F80 <sub>H</sub> to 0000 0FF8 <sub>H</sub>	—				Reserved
0000 0FFC <sub>H</sub>	—		BTSSSR[W] H XXXXXXXX XXXXXXXX		Base Timer I/O Select Function
0000 1000 <sub>H</sub> to 0000 20FC <sub>H</sub>	—				Reserved
0000 2100 <sub>H</sub>	HCNT1[R/W] B,H ----001	HCNT0[R/W] B,H 00000000	—		USB function / HOST
0000 2104 <sub>H</sub>	HERR[R/W] B,H 00000011	HIRQ[R/W] B,H 0-000000	—		
0000 2108 <sub>H</sub>	HFCOMP[R/W] B,H 00000000	HSTATE[R,W] B,H ---10010	—		
0000 210C <sub>H</sub>	HRTIMER1[R/W] B,H 00000000	HRTIMER0[R/W] B,H 00000000	—		
0000 2110 <sub>H</sub>	HADR[R/W] B,H -0000000	HRTIMER2[R/W] B,H -----00	—		
0000 2114 <sub>H</sub>	HEOF1[R/W] B,H --000000	HEOF0[R/W] B,H 00000000	—		
0000 2118 <sub>H</sub>	HFRAME1[R/W] B,H -----000	HFRAME0[R/W] B,H 00000000	—		
0000 211C <sub>H</sub>	—	HTOKEN[R/W] B 00000000	—		
0000 2120 <sub>H</sub>	—	UDCC[R/W] B 1010--00	—		

(Continued)

# MB91610 Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 2124 <sub>H</sub>	EP0C[R/W] H -----0- -1000000			—	USB function / HOST
0000 2128 <sub>H</sub>	EP1C[R/W] H 01100001 00000000			—	
0000 212C <sub>H</sub>	EP2C[R/W] H 0110000- -1000000			—	
0000 2130 <sub>H</sub>	EP3C[R/W] H 0110000- -1000000			—	
0000 2134 <sub>H</sub>	EP4C[R/W] H 0110000- -1000000			—	
0000 2138 <sub>H</sub>	EP5C[R/W] H 0110000- -1000000			—	
0000 213C <sub>H</sub>	TMSP[R] H -----000 00000000			—	
0000 2140 <sub>H</sub>	UDCIE[R,R/W] B,H --000000	UDCS[R/W] B,H --000000		—	
0000 2144 <sub>H</sub>	EP0IS[R/W] H 10---1-- -----			—	
0000 2148 <sub>H</sub>	EP00S[R,R/W] H 100--00- -XXXXXXXX			—	
0000 214C <sub>H</sub>	EP1S[R,R/W] H 100-000X XXXXXXXXX			—	
0000 2150 <sub>H</sub>	EP2S[R,R/W] H 100-000- -XXXXXXXX			—	
0000 2154 <sub>H</sub>	EP3S[R,R/W] H 100-000- -XXXXXXXX			—	
0000 2158 <sub>H</sub>	EP4S[R,R/W] H 100-000- -XXXXXXXX			—	
0000 215C <sub>H</sub>	EP5S[R,R/W] H 100-000- -XXXXXXXX			—	
0000 2160 <sub>H</sub>	EP0DTH [R/W] B,H XXXXXXXXX	EP0DTL [R/W] B,H XXXXXXXXX		—	
0000 2164 <sub>H</sub>	EP1DTH [R/W] B,H XXXXXXXXX	EP1DTL [R/W] B,H XXXXXXXXX		—	
0000 2168 <sub>H</sub>	EP2DTH [R/W] B,H XXXXXXXXX	EP2DTL [R/W] B,H XXXXXXXXX		—	
0000 216C <sub>H</sub>	EP3DTH [R/W] B,H XXXXXXXXX	EP3DTL [R/W] B,H XXXXXXXXX		—	

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 2170 <sub>H</sub>	EP4DTH [R/W] B,H XXXXXXXX	EP4DTL [R/W] B,H XXXXXXXX	—		USB function / HOST
0000 2174 <sub>H</sub>	EP5DTH [R/W] B,H XXXXXXXX	EP5DTL [R/W] B,H XXXXXXXX	—		
0000 2178 <sub>H</sub> to 0000 217C <sub>H</sub>	—				
0000 2180 <sub>H</sub> to 0000 21A0 <sub>H</sub>	—				Reserved
0000 21A4 <sub>H</sub>	DREQSEL [R/W] B,H 00111011	USBSEL [R/W] B,H -----0	USBEN [R/W] B -----0	—	DMA transfer request selector/ USB enable
0000 21A8 <sub>H</sub> to 0000 3FFC <sub>H</sub>	—				Reserved
0000 4000 <sub>H</sub>	MOSD_VADR [W] W -----0 ---00000 --000000				OSDC (MAIN)
0000 4004 <sub>H</sub>	MOSD_CDS1 [W] W 00000000 ---00000 00000000 00000000				
0000 4008 <sub>H</sub>	MOSD_CDS2 [W] W ----- 0000-000 --000000 00000000				
0000 400C <sub>H</sub>	MOSD_LDS1 [W] W 0000-000 00000000 ----0000 00000000				
0000 4010 <sub>H</sub>	MOSD_LDS2 [W] W ----- ---00000 --000000 00000000				
0000 4014 <sub>H</sub>	MOSD_SCOC [W] W -----00 0000---- ---0---0 XXXX----				
0000 4018 <sub>H</sub>	MOSD_HVDP [W] W ----000 00000000 ----000 00000000				
0000 401C <sub>H</sub>	MOSD_TSBC [W] W -----00000000 -----0 00000000				
0000 4020 <sub>H</sub>	MOSD_GRCC [W] W -----0 00000000 -----0 00000000				
0000 4024 <sub>H</sub>	MOSD_SBCC [W] W ----000 -----00 --000000 00000000				
0000 4028 <sub>H</sub>	MOSD_SCBC [W] W ----- --00--00 ---0-000 00000000				
0000 402C <sub>H</sub>	MOSD_WPC1 [W] W ----000 00000000 ----000 00000000				

(Continued)

# MB91610 Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 4030 <sub>H</sub>	MOSD_WPC2 [W] W ----0000 00000000 ----0000 00000000				OSDC (MAIN)
0000 4034 <sub>H</sub>	MOSD_SPC1 [W] W ---0-000 -----00 --000000 00000000				
0000 4038 <sub>H</sub>	MOSD_SPC2 [W] W ----0000 00000000 ----000 00000000				
0000 403C <sub>H</sub>	MOSD_SYNC [W] W ----- --000000 ----- -0-0----				
0000 4040 <sub>H</sub>	MOSD_CBC0 [W] W --000000 00000000 --000000 00000000				
0000 4044 <sub>H</sub>	MOSD_CBC1 [W] W --000000 00000000 --000000 00000000				
0000 4048 <sub>H</sub>	MOSD_CBC2 [W] W --000000 00000000 --000000 00000000				
0000 404C <sub>H</sub>	MOSD_CBC3 [W] W --000000 00000000 --000000 00000000				
0000 4050 <sub>H</sub>	MOSD_CBC4 [W] W --000000 00000000 --000000 00000000				
0000 4054 <sub>H</sub>	MOSD_CBC5 [W] W --000000 00000000 --000000 00000000				
0000 4058 <sub>H</sub>	MOSD_CBC6 [W] W --000000 00000000 --000000 00000000				
0000 405C <sub>H</sub>	MOSD_CBC7 [W] W --000000 00000000 --000000 00000000				
0000 4060 <sub>H</sub>	MOSD_IOTC [W] W -----0 0----00- ----- ----XXX				
0000 4064 <sub>H</sub>	MOSD_CDP1 [W] W ----000 00000000 ----000 00000000				
0000 4068 <sub>H</sub>	MOSD_CDP2 [W] W ----0000 00000000 ----0000 00000000				
0000 406C <sub>H</sub>	MOSD_INTC [R/W] W ----- ----- ----XXX ----XXX				
0000 4070 <sub>H</sub>	MOSD_SBC0 [W] W 00000000 00000000 00000000 00000000				
0000 4074 <sub>H</sub>	MOSD_SBC1 [W] W 00000000 00000000 00000000 00000000				
0000 4078 <sub>H</sub>	MOSD_SBC2 [W] W 00000000 00000000 00000000 00000000				
0000 407C <sub>H</sub>	MOSD_SBC3 [W] W 00000000 00000000 00000000 00000000				

(Continued)

# MB91610 Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 4080 <sub>H</sub> to 0000 40FC <sub>H</sub>	—				Reserved
0000 4100 <sub>H</sub>	SOSD_VADR [W] W -----0 ---00000 --000000				OSDC (SUB)
0000 4104 <sub>H</sub>	SOSD_CDS1 [W] W 00000000 ---00000 00000000 00000000				
0000 4108 <sub>H</sub>	SOSD_CDS2 [W] W ----- 0000-000 --000000 00000000				
0000 410C <sub>H</sub>	SOSD_LDS1 [W] W 0000-000 00000000 ----0000 00000000				
0000 4110 <sub>H</sub>	SOSD_LDS2 [W] W ----- --000000 --000000 00000000				
0000 4114 <sub>H</sub>	SOSD_SCOC [W] W -----00 0000---- --0---0 XX-X---X				
0000 4118 <sub>H</sub>	SOSD_HVDP [W] W ----000 00000000 ----000 00000000				
0000 411C <sub>H</sub>	SOSD_TSBC [W] W -----000000000 00000000				
0000 4120 <sub>H</sub>	SOSD_GRCC [W] W -----0 00000000 -----0 00000000				
0000 4124 <sub>H</sub>	—				
0000 4128 <sub>H</sub>	SOSD_SCBC [W] W ----- --00-00 ---0-000 00000000				
0000 412C <sub>H</sub>	SOSD_WPC1 [W] W ----000 00000000 ----000 00000000				
0000 4130 <sub>H</sub>	SOSD_WPC2 [W] W ----0000 00000000 ----0000 00000000				
0000 4134 <sub>H</sub>	SOSD_SPC1 [W] W --0-000 -----00 --000000 00000000				
0000 4138 <sub>H</sub>	SOSD_SPC2 [W] W ----0000 00000000 ----000 00000000				
0000 413C <sub>H</sub> to 0000 4168 <sub>H</sub>	—				
0000 416C <sub>H</sub>	SOSD_INTC [R/W] W -----000000000 ---XXX ---XXX				
0000 4170 <sub>H</sub>	SOSD_SBC0 [W] W 00000000 00000000 00000000 00000000				
0000 4174 <sub>H</sub>	SOSD_SBC1 [W] W 00000000 00000000 00000000 00000000				
0000 4178 <sub>H</sub>	SOSD_SBC2 [W] W 00000000 00000000 00000000 00000000				
0000 417C <sub>H</sub>	SOSD_SBC3 [W] W 00000000 00000000 00000000 00000000				

(Continued)

# MB91610 Series

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000 4180 <sub>H</sub> to 0000 41FC <sub>H</sub>	—				Reserved
0000 4200 <sub>H</sub> to 0000 43FC <sub>H</sub>	MOSD_PLn [W] W (n: 0 to 127) 00000000 00000000 00000000 00000000				OSDC (MAIN)
0000 4400 <sub>H</sub>	MOSD_OSDC [W] W ----- --XX--XX -----XX ---X---X				
0000 4404 <sub>H</sub>	MOSD_PLLC [W] W --000000 00000000 00000000 ---00000				
0000 4408 <sub>H</sub> to 0000 FFFC <sub>H</sub>	—				Reserved

\*1 : Byte access is available only when accessing the lower 8 bits within 9 bits.

\*2 : The register of I<sup>2</sup>C can not be read immediate after reset.

\*3 : Value just after reset by  $\overline{\text{INIT}}$  pin.

Do not access the reserved areas.

## ■ VECTOR TABLE

Interrupt source (Peripheral resource)	Interrupt number		Interrupt level setting register	Offset	Address of TBR default
	Decimal	Hexadecimal			
Reset	0	00	—	3FC <sub>H</sub>	000F FFFC <sub>H</sub>
System reserved	1	01	—	3F8 <sub>H</sub>	000F FFF8 <sub>H</sub>
System reserved	2	02	—	3F4 <sub>H</sub>	000F FFF4 <sub>H</sub>
System reserved	3	03	—	3F0 <sub>H</sub>	000F FFF0 <sub>H</sub>
System reserved	4	04	—	3EC <sub>H</sub>	000F FFEC <sub>H</sub>
System reserved	5	05	—	3E8 <sub>H</sub>	000F FFE8 <sub>H</sub>
System reserved	6	06	—	3E4 <sub>H</sub>	000F FFE4 <sub>H</sub>
System reserved	7	07	—	3E0 <sub>H</sub>	000F FFE0 <sub>H</sub>
System reserved	8	08	—	3DC <sub>H</sub>	000F FFDC <sub>H</sub>
INTE instruction	9	09	—	3D8 <sub>H</sub>	000F FFD8 <sub>H</sub>
Instruction break exception	10	0A	—	3D4 <sub>H</sub>	000F FFD4 <sub>H</sub>
Operand break	11	0B	—	3D0 <sub>H</sub>	000F FFD0 <sub>H</sub>
Step trace trap	12	0C	—	3CC <sub>H</sub>	000F FFCC <sub>H</sub>
System reserved	13	0D	—	3C8 <sub>H</sub>	000F FFC8 <sub>H</sub>
Undefined instruction exception	14	0E	—	3C4 <sub>H</sub>	000F FFC4 <sub>H</sub>
—	15	0F	15 (F <sub>H</sub> ) fixed	3C0 <sub>H</sub>	000F FFC0 <sub>H</sub>
External interrupt request ch.0 to ch.7	16	10	ICR00	3BC <sub>H</sub>	000F FFBC <sub>H</sub>
External interrupt request ch.8 to ch.15	17	11	ICR01	3B8 <sub>H</sub>	000F FFB8 <sub>H</sub>
Reserved	18	12	ICR02	3B4 <sub>H</sub>	000F FFB4 <sub>H</sub>
Reserved	19	13	ICR03	3B0 <sub>H</sub>	000F FFB0 <sub>H</sub>
16-bit reload timer ch.0 to ch.2	20	14	ICR04	3AC <sub>H</sub>	000F FFAC <sub>H</sub>
Reception interrupt request of UART/CSIO ch.0	21	15	ICR05	3A8 <sub>H</sub>	000F FFA8 <sub>H</sub>
Transmission interrupt request of UART/CSIO ch.0 Transmission bus idle interrupt request of UART/CSIO ch.0	22	16	ICR06	3A4 <sub>H</sub>	000F FFA4 <sub>H</sub>
Reception interrupt request of UART/CSIO/ I <sup>2</sup> C ch.1	23	17	ICR07	3A0 <sub>H</sub>	000F FFA0 <sub>H</sub>
Transmission interrupt request of UART/CSIO/ I <sup>2</sup> C ch.1 Transmission bus idle interrupt request of UART/CSIO ch.1	24	18	ICR08	39C <sub>H</sub>	000F FF9C <sub>H</sub>
Status interrupt request of I <sup>2</sup> C ch.1	25	19	ICR09	398 <sub>H</sub>	000F FF98 <sub>H</sub>

(Continued)

# MB91610 Series

Interrupt source (Peripheral resource)	Interrupt number		Interrupt level setting register	Offset	Address of TBR default
	Decimal	Hexadecimal			
Reception interrupt request of UART/CSIO/I <sup>2</sup> C ch.2	26	1A	ICR10	394 <sub>H</sub>	000F FF94 <sub>H</sub>
Transmission interrupt request of UART/CSIO/I <sup>2</sup> C ch.2 Transmission bus idle interrupt request of UART/CSIO ch.2	27	1B	ICR11	390 <sub>H</sub>	000F FF90 <sub>H</sub>
Status interrupt request of I <sup>2</sup> C ch.2	28	1C	ICR12	38C <sub>H</sub>	000F FF8C <sub>H</sub>
Reception interrupt request of UART/CSIO/I <sup>2</sup> C ch.3	29	1D	ICR13	388 <sub>H</sub>	000F FF88 <sub>H</sub>
Transmission interrupt request of UART/CSIO/I <sup>2</sup> C ch.3 Transmission bus idle interrupt request of UART/CSIO ch.3 Status interrupt request of I <sup>2</sup> C ch.3	30	1E	ICR14	384 <sub>H</sub>	000F FF84 <sub>H</sub>
Reserved	31	1F	ICR15	380 <sub>H</sub>	000F FF80 <sub>H</sub>
Reserved	32	20	ICR16	37C <sub>H</sub>	000F FF7C <sub>H</sub>
Reserved	33	21	ICR17	378 <sub>H</sub>	000F FF78 <sub>H</sub>
Reserved	34	22	ICR18	374 <sub>H</sub>	000F FF74 <sub>H</sub>
Reserved	35	23	ICR19	370 <sub>H</sub>	000F FF70 <sub>H</sub>
Reserved	36	24	ICR20	36C <sub>H</sub>	000F FF6C <sub>H</sub>
Reserved	37	25	ICR21	368 <sub>H</sub>	000F FF68 <sub>H</sub>
Reserved	38	26	ICR22	364 <sub>H</sub>	000F FF64 <sub>H</sub>
Reception interrupt request of UART/CSIO/I <sup>2</sup> C ch.8 to ch.11 Transmission interrupt request of UART/CSIO/I <sup>2</sup> C ch.8 to ch.11 Transmission bus idle interrupt request of UART/CSIO ch.8 to ch.11 Transmission FIFO interrupt request UART/CSIO/I <sup>2</sup> C ch.8 to ch.11 Status interrupt request of I <sup>2</sup> C ch.8 to ch.11	39	27	ICR23	360 <sub>H</sub>	000F FF60 <sub>H</sub>
HDMI-CEC/Remote control reception	40	28	ICR24	35C <sub>H</sub>	000F FF5C <sub>H</sub>
Main timer/Sub timer/Watch counter	41	29	ICR25	358 <sub>H</sub>	000F FF58 <sub>H</sub>
10-bit A/D converter <ul style="list-style-type: none"> <li>• Scan conversion interrupt request</li> <li>• Priority conversion interrupt request</li> <li>• FIFO overrun interrupt request</li> <li>• Conversion result compare interrupt request</li> </ul>	42	2A	ICR26	354 <sub>H</sub>	000F FF54 <sub>H</sub>

(Continued)

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Interrupt source (Peripheral resource)	Interrupt number		Interrupt level setting register	Offset	Address of TBR default
	Decimal	Hexadecimal			
32-bit free run timer ch.0	43	2B	ICR27	350 <sub>H</sub>	000F FF50 <sub>H</sub>
32-bit input capture ch.0 to ch.3	44	2C	ICR28	34C <sub>H</sub>	000F FF4C <sub>H</sub>
32-bit output compare ch.0 to ch.3	45	2D	ICR29	348 <sub>H</sub>	000F FF48 <sub>H</sub>
Base timer ch.0	46	2E	ICR30	344 <sub>H</sub>	000F FF44 <sub>H</sub>
Base timer ch.1	47	2F	ICR31	340 <sub>H</sub>	000F FF40 <sub>H</sub>
Base timer ch.2	48	30	ICR32	33C <sub>H</sub>	000F FF3C <sub>H</sub>
Base timer ch.3	49	31	ICR33	338 <sub>H</sub>	000F FF38 <sub>H</sub>
Base timer ch.4, ch.5	50	32	ICR34	334 <sub>H</sub>	000F FF34 <sub>H</sub>
Base timer ch.6, ch.7	51	33	ICR35	330 <sub>H</sub>	000F FF30 <sub>H</sub>
Reserved	52	34	ICR36	32C <sub>H</sub>	000F FF2C <sub>H</sub>
OSDC (MAIN)	53	35	ICR37	328 <sub>H</sub>	000F FF28 <sub>H</sub>
USB function (DRQ of End Point 1 to 5)	54	36	ICR38	324 <sub>H</sub>	000F FF24 <sub>H</sub>
USB function (DRQI of End Point 0, DRQO and each status/ USB HOST (each status))	55	37	ICR39	320 <sub>H</sub>	000F FF20 <sub>H</sub>
OSDC (SUB)	56	38	ICR40	31C <sub>H</sub>	000F FF1C <sub>H</sub>
DMA controller (DMAC) ch.0	57	39	ICR41	318 <sub>H</sub>	000F FF18 <sub>H</sub>
DMA controller (DMAC) ch.1	58	3A	ICR42	314 <sub>H</sub>	000F FF14 <sub>H</sub>
DMA controller (DMAC) ch.2	59	3B	ICR43	310 <sub>H</sub>	000F FF10 <sub>H</sub>
DMA controller (DMAC) ch.3	60	3C	ICR44	30C <sub>H</sub>	000F FF0C <sub>H</sub>
DMA controller (DMAC) ch.4 to ch.7	61	3D	ICR45	308 <sub>H</sub>	000F FF08 <sub>H</sub>
System reserved	62	3E	ICR46	304 <sub>H</sub>	000F FF04 <sub>H</sub>
Delay interrupt	63	3F	ICR47	300 <sub>H</sub>	000F FF00 <sub>H</sub>
System reserved (Used by REALOS)	64	40	—	2FC <sub>H</sub>	000F FEFC <sub>H</sub>
System reserved (Used by REALOS)	65	41	—	2F8 <sub>H</sub>	000F FEF8 <sub>H</sub>
Used by INT instruction	66 to 255	42 to FF	—	2F4 <sub>H</sub> to 000 <sub>H</sub>	000F FEF4 <sub>H</sub> to 000F FC00 <sub>H</sub>

# MB91610 Series

\* : USB interrupt source

Interrupt Number		USB interrupt source	Details
Decimal	Hexadecimal		
54	36	USB function (DRQ of End Point 1 to 5)	DRQ (End Point1 to 5)
55	37	USB function (DRQI, DRQO of End Point 0 and each status)	DRQI, DRQO, SPK, SUSP, SOF, BRST, CONF, WKUP
		USB HOST (Each status)	DIRQ, URIRQ, RWKIRQ, CNNIRQ, SOFIRQ, CMPIRQ

## ■ PIN STATUS IN EACH CPU STATE

- When  $\overline{\text{INIT}} = \text{“L”}$

This is the period when the  $\overline{\text{INIT}}$  pin is the “L” level.

- When  $\overline{\text{INIT}} = \text{“H”}$

The status immediately after the  $\overline{\text{INIT}}$  pin changes from the “L” level to the “H” level.

- SLVL1

This bit is a standby level setting bit in the standby mode control register (STBCR) .

- Input enabled

Indicates that the input function can be used.

- Input disabled

Indicates that the input function cannot be used.

- Output Hi-Z

Indicates that the output drive transistor is disabled and the pin is put in the Hi-Z state.

- Maintain previous state

Maintains the state that was being output immediately prior to entering the current mode.  
If a built-in peripheral function is operating, the output follows the peripheral function.  
If the pin is being used as a port, that output is maintained.

- Internal input fixed at “0”

The input gate connected to the pin is disconnected from the external input and internally connected to “0”.

- Input enabled when interrupt function selected and enabled

Inputs are allowed only when the pin is configured as an external interrupt request input pin and the external interrupt request is enabled.

# MB91610 Series

• List of pin status

Pin name	Function	During initialization		Sleep Mode	Standby Mode	
		$\overline{\text{INIT}} = \text{"L"}$	$\overline{\text{INIT}} = \text{"H"}$		SLVL1 = 0	SLVL1 = 1
$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	—	—	Input enabled	Input enabled	Input enabled
X0	X0	Input enabled	Input enabled		Hi-Z/ Input enabled	Hi-Z/ Input enabled
X1	X1	Input enabled	Input enabled		"H" output/ Input enabled	"H" output/ Input enabled
X0A	X0A (When $\overline{\text{INIT}}$ input, see PK1. When port selected, input disabled)	Input disabled	Input disabled		Hi-Z/ Input enabled	Hi-Z/ Input enabled
X1A	X1A (When $\overline{\text{INIT}}$ input, see PK0. When port selected, input disabled)	Input disabled	Input disabled		"H" output/ Input enabled	"H" output/ Input enabled
MD0	MD0	Input enabled	Input enabled		Input enabled	Input enabled
MD1	MD1	Input enabled	Input enabled			
P00	P00/TIOA0/SOUT0_1/IN0	Output Hi-Z	Output Hi-Z Input enabled		Maintain previous state	Maintain previous state
P01	P01/TIOB0/SIN0_1/IN1					
P02	P02/TIOA1/SCK0_1/IN2					
P03	P03/TIOB1/IN3					
P04	P04/TIOA2/SOUT1					
P05	P05/TIOB2/SIN1					
P06	P06/TIOA3/SCK1					
P07	P07/TIOB3					
P10	P10/TIOA4/SOUT2/INT0	Output Hi-Z	Output Hi-Z Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0"  Input enabled when interrupt function selected and enabled
P11	P11/TIOB4/SIN2/INT1					
P12	P12/TIOA5/SCK2/INT2					
P13	P13/TIOB5/INT3					
P14	P14/TIOA6/SOUT3/INT4					
P15	P15/TIOB6/SIN3/INT5					
P16	P16/TIOA7/SCK3/INT6					
P17	P17/TIOB7/INT7					

(Continued)

# MB91610 Series

Pin name	Function	During initialization		Sleep Mode	Standby Mode	
		$\overline{\text{INIT}} = \text{"L"}$	$\overline{\text{INIT}} = \text{"H"}$		SLVL1 = 0	SLVL1 = 1
P20	P20/SOUT8	Output Hi-Z	Output Hi-Z Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0"
P21	P21/SIN8					
P22	P22/SCK8					
P23	P23/RCIN_1					
P24	P24/SOUT9/OUT0					
P25	P25/SIN9/OUT1					
P26	P26/SCK9/OUT2					
P27	P27/OUT3					
P30	P30/SOUT10/INT8	Output Hi-Z	Output Hi-Z Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0"  Input enabled when interrupt function selected and enabled
P31	P31/SIN10/INT9					
P32	P32/SCK10/INT10					
P33	P33/INT11					
P34	P34/SOUT11/INT12					
P35	P35/SIN11/INT13					
P36	P36/SCK11/INT14					
P37	P37/INT15					
P50	P50	Output Hi-Z	Output Hi-Z Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0"
P51	P51					
P52	P52					
P53	P53					
P54	P54/RCIN					
P55	P55/ADTRG					
P56	P56/FRCK					
P57	P57					
P70	P70/AN0/OUT0_1	Output Hi-Z	Output Hi-Z Input enabled*	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0"
P71	P71/AN1/OUT1_1					
P72	P72/AN2/TMO0/OUT2_1					
P73	P73/AN3/TMO1/OUT3_1					
P74	P74/AN4/TMO2					
P75	P75/AN5/SOUT0/TMI0					
P76	P76/AN6/SIN0/TMI1					
P77	P77/AN7/SCK0/TMI2					
PK0	PK0	Output Hi-Z	Output Hi-Z Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0"
PK1	PK1					

\* : Analog input has a priority (digital input is disconnected)

(Continued)

# MB91610 Series

(Continued)

Pin name	Function	During initialization		Sleep Mode	Standby Mode	
		$\overline{\text{INIT}} = \text{"L"}$	$\overline{\text{INIT}} = \text{"H"}$		SLVL1 = 0	SLVL1 = 1
UDP	UDP(USB)	Output Hi-Z	Output Hi-Z	Maintain previous state/ Input enabled	Maintain previous state	Output Hi-Z/ Internal input fixed at "0"
UDM	UDM(USB)		Input enabled			
DCKI	DCKI	Input state	Input enabled	Input enabled	Input state	Input state
DCKO	DCKO	L output	L output/ DCK output	L output/ DCK output	L output (OSDC stop)	L output (OSDC stop)
VSYNC	VSYNC	Input state	Input enabled	Input enabled	Input state	Input state
HSYNC	HSYNC					
R4 to R0	R4 to R0	L output	L output/ R output	L output/ R output	L output (OSDC stop)	L output (OSDC stop)
G5 to G0	G5 to G0		L output/ G output	L output/ G output		
B4 to B0	B4 to B0		L output/ B output	L output/ B output		
VOA2 to VOA0	VOA2 to VOA0		L output/ VOA output	L output/ VOA output		
VOB	VOB		L output/ VOB output	L output/ VOB output		
ROUT	ROUT		L output/ ROUT output	L output/ ROUT output		
GOUT	GOUT		L output/ GOUT output	L output/ GOUT output		
BOUT	BOUT		L output/ BOUT output	L output/ BOUT output		
HWDE	HWDE	Input state	Input enabled	Input enabled	Input state	Input state

# MB91610 Series

- List of pin status (serial write mode)

Pin name	Function	During initialization	During asynchronous write operation	During synchronous write operation
		$\overline{\text{INIT}} = \text{"L"}$	$\overline{\text{INIT}} = \text{"H"}$	
$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	—	—	—
X0	X0	Input enabled	Input enabled	Input enabled
X1	X1	Input enabled	Input enabled	Input enabled
X0A	X0A (When $\overline{\text{INIT}}$ input, see PK1. When port selected, input disabled)	Input disabled	Input disabled	Input disabled
X1A	X1A (When $\overline{\text{INIT}}$ input, see PK0. When port selected, input disabled)	Input disabled	Input disabled	Input disabled
MD0	MD0	Input enabled	Input enabled	Input enabled
MD1	MD1	Input enabled	Input enabled	Input enabled
P00	P00/TIOA0/SOUT0_1/IN0	Output Hi-Z	Output Hi-Z Input enabled	Output Hi-Z Input enabled
P01	P01/TIOB0/SIN0_1/IN1			
P02	P02/TIOA1/SCK0_1/IN2			
P03	P03/TIOB1/IN3			
P04	P04/TIOA2/SOUT1			
P05	P05/TIOB2/SIN1			
P06	P06/TIOA3/SCK1			
P07	P07/TIOB3			
P10	P10/TIOA4/SOUT2/INT0	Output Hi-Z	Output Hi-Z Input enabled	Output Hi-Z Input enabled
P11	P11/TIOB4/SIN2/INT1			
P12	P12/TIOA5/SCK2/INT2			
P13	P13/TIOB5/INT3			
P14	P14/TIOA6/SOUT3/INT4			
P15	P15/TIOB6/SIN3/INT5			
P16	P16/TIOA7/SCK3/INT6			
P17	P17/TIOB7/INT7			
P20	P20/SOUT8	Output Hi-Z	Output Hi-Z Input enabled	Output Hi-Z Input enabled
P21	P21/SIN8			
P22	P22/SCK8			
P23	P23/RCIN_1			
P24	P24/SOUT9/OUT0			
P25	P25/SIN9/OUT1			
P26	P26/SCK9/OUT2			
P27	P27/OUT3			

(Continued)

# MB91610 Series

Pin name	Function	During initialization	During asynchronous write operation	During synchronous write operation
		$\overline{\text{INIT}} = \text{"L"}$	$\overline{\text{INIT}} = \text{"H"}$	
P30	P30/SOUT10/INT8	Output Hi-Z	Output Hi-Z Input enabled	Output Hi-Z Input enabled
P31	P31/SIN10/INT9			
P32	P32/SCK10/INT10			
P33	P33/INT11			
P34	P34/SOUT11/INT12			
P35	P35/SIN11/INT13			
P36	P36/SCK11/INT14			
P37	P37/INT15			
P50	P50	Output Hi-Z	Output Hi-Z Input enabled	Output Hi-Z Input enabled
P51	P51			
P52	P52			
P53	P53			
P54	P54/RCIN			
P55	P55/ADTRG			
P56	P56/FRCK			
P57	P57			
P70	P70/AN0/OUT0_1	Output Hi-Z	Output Hi-Z Input enabled	Output Hi-Z Input enabled
P71	P71/AN1/OUT1_1			
P72	P72/AN2/TMO0/OUT2_1			
P73	P73/AN3/TMO1/OUT3_1			
P74	P74/AN4/TMO2		Output	Output
P75	P75/AN5/SOUT0/TMI0			
P76	P76/AN6/SIN0/TMI1			
P77	P77/AN7/SCK0/TMI2			
PK0	PK0	Output Hi-Z	Output Hi-Z Input enabled	Output Hi-Z Input enabled
PK1	PK1			
UDP	UDP (USB)	Output Hi-Z	Output Hi-Z Input enabled	Output Hi-Z Input enabled
UDM	UDM (USB)			
DCKI	DCKI	Input state	Input enabled	Input enabled
DCKO	DCKO	L output	L output	L output
VSYNC	VSYNC	Input state	Input enabled	Input enabled
HSYNC	HSYNC			

(Continued)

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Pin name	Function	During initialization	During asynchronous write operation	During synchronous write operation
		$\overline{\text{INIT}} = \text{“L”}$	$\overline{\text{INIT}} = \text{“H”}$	
R4 to R0	R4 to R0	L output	L output	L output
G5 to G0	G5 to G0			
B4 to B0	B4 to B0			
VOA2 to VOA0	VOA2 to VOA0			
VOB	VOB			
ROUT	ROUT	L output	L output	L output
GOUT	GOUT			
BOUT	BOUT			
HWDE	HWDE	Input state	Input enabled	Input enabled

# MB91610 Series

## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1, *2	$V_{CC}$	$V_{SS} - 0.3$	$V_{SS} + 4.0$	V	
Analog power supply voltage*1, *3	$AV_{CC}$	$V_{SS} - 0.3$	$V_{SS} + 4.0$	V	
Analog reference voltage*1, *3	$AV_{RH}$	$V_{SS} - 0.3$	$V_{SS} + 4.0$	V	
Input voltage*1	$V_I$	$V_{SS} - 0.3$	$V_{CC} + 0.3$ ( $\leq 4.0$ )	V	*7
		$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	5 V tolerant
		$V_{SS} - 0.5$	$V_{CC} + 0.5$ ( $\leq 4.0$ )	V	USB I/O
Analog pin input voltage*1	$V_{IA}$	$V_{SS} - 0.3$	$V_{SS} + 4.0$	V	
Output voltage*1	$V_O$	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	
		$V_{SS} - 0.5$	$V_{CC} + 0.5$ ( $\leq 4.0$ )	V	USB I/O
Maximum clamp current	$I_{CLAMP}$	- 4	+ 4	mA	*8
Total maximum clamp current	$\Sigma I_{CLAMP} $	—	40	mA	*8
“L” level maximum output current*4	$I_{OL}$	—	10	mA	
		—	43	mA	USB I/O
“L” level average output current*5	$I_{OLAV}$	—	4	mA	
		—	15	mA	USB I/O
“L” level total maximum output current	$\Sigma I_{OL}$	—	100	mA	
“L” level total average output current*6	$\Sigma I_{OLAV}$	—	50	mA	
“H” level maximum output current*4	$I_{OH}$	—	- 10	mA	
		—	- 43	mA	USB I/O
“H” level average output current*5	$I_{OHAV}$	—	- 4	mA	
		—	- 15	mA	USB I/O
“H” level total maximum output current*6	$\Sigma I_{OH}$	—	- 100	mA	
“H” level total average output current	$\Sigma I_{OHAV}$	—	- 50	mA	
Power consumption (Flash product)	$P_D$	—	850	mW	
Power consumption (MASK product)		—	600	mW	
Operating temperature	$T_a$	- 40	+ 85	°C	
Storage temperature	$T_{STG}$	- 55	+ 125	°C	

\*1 : The parameter is based on  $V_{SS} = AV_{SS} = 0.0$  V.

\*2 :  $V_{CC}$  must not drop below  $V_{SS} - 0.3$  V.

\*3 : Be careful not to exceed  $V_{CC} + 0.3$  V, for example, when the power is turned on.

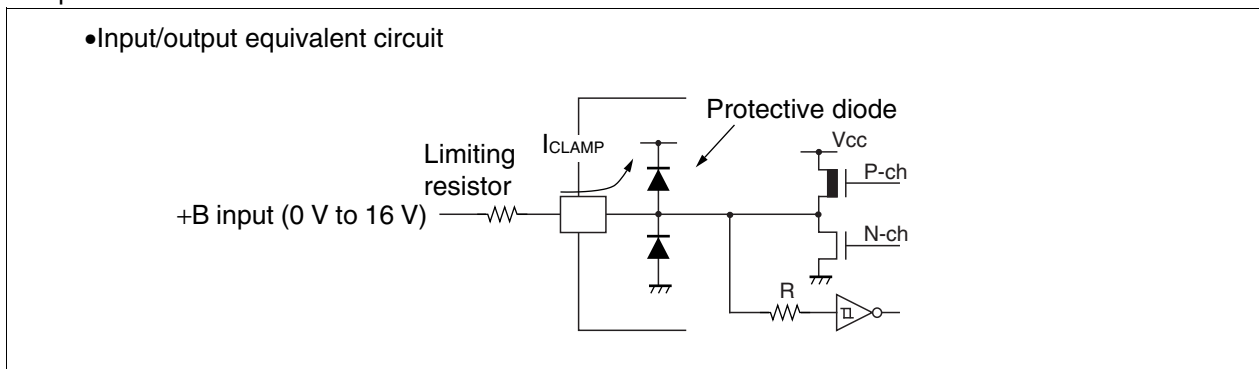
\*4 : The maximum output current is the peak value for a single pin.

\*5 : The average output is the average current for a single pin over a period of 100 ms.

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- \*6 : The total average output current is the average current for all pins over a period of 100 ms.
- \*7 : If the input current or the maximum input current are limited by some means with external components, the  $I_{CLAMP}$  rating supersedes the  $V_I$  rating.
- \*8 :
  - Corresponding pins:P14 to P17,P20 to P27,P30 to P37,P50 to P57
  - Use within recommended operating conditions.
  - Use at DC voltage (current).
  - The +B signal should always be applied by connecting a limiting resistor between the +B signal and the microcontroller.
  - The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed rated values at any time regardless of instantaneously or constantly when the +B signal is input.
  - Note that when the microcontroller drive current is low, such as in the low power consumption modes, the +B input potential can increase the potential at the  $V_{CC}$  pin via a protective diode, possibly affecting other devices.
  - Note that if the +B signal is input when the microcontroller is off (not fixed at 0V), since the power is supplied through the pin, the microcontroller may operate incompletely.
  - Do not leave +B input pins open.
  - Sample recommended circuit



**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

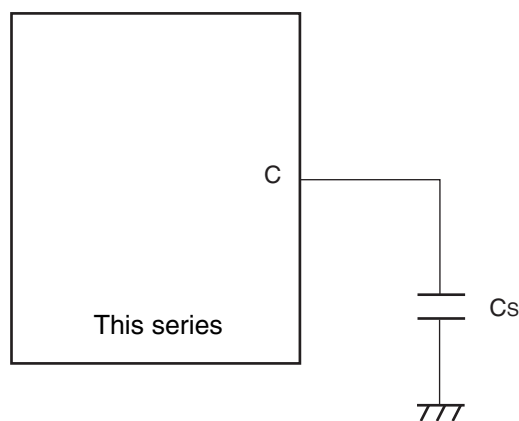
# MB91610 Series

## 2. Recommended Operating Conditions

( $V_{SS} = AV_{SS} = 0.0\text{ V}$ )

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	$V_{CC}$	3.0	—	3.6	V	
Analog power supply voltage	$AV_{CC}$	3.0	—	3.6	V	$AV_{CC} \leq V_{CC}$
Analog reference voltage	$AV_{RH}$	$AV_{SS}$	—	$AV_{CC}$	V	
Smoothing capacitor	$C_s$	—	4.7	—	$\mu\text{F}$	
Operating temperature	$T_a$	-40	—	+85	$^{\circ}\text{C}$	

• C Pin Connection Diagram



**WARNING:** The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

## 3. DC Characteristics

### (1) DC Characteristics

( $V_{CC} = AV_{CC} = 3.0\text{ V to } 3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_a = -40\text{ }^\circ\text{C to } +85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current (Flash product)	I <sub>CC</sub>	V <sub>CC</sub>	Normal operation	—	45	60	mA	OSDC stopped Not using USB CPU : 33 MHz, Peripheral : 33 MHz
				—	55	75	mA	OSDC stopped Using USB CPU : 32 MHz, Peripheral : 32 MHz
	—			100	130	mA	Dot clock 50 MHz (PLL) Dot clock PLL is used Analog RGB DAC is used Digital RGB is not used CPU : 33 MHz, Peripheral : 33 MHz	
	—			105	150	mA	Dot clock 75 MHz (PLL) Dot clock PLL is used Analog RGB DAC is not used Digital RGB is used CPU : 33 MHz, Peripheral:33 MHz	
	—			15	25	mA	OSDC stopped Not using USB Peripheral : 33 MHz	
	—			25	40	mA	OSDC stopped Using USB Peripheral : 32 MHz	
	I <sub>CCO</sub>		Sub operation*	—	150	550	μA	CPU : 32 kHz Peripheral : 32 kHz
	I <sub>CCS</sub>		Watch mode*	—	120	450	μA	
	I <sub>CCCL</sub>		STOP mode*	—	65	320	μA	
	I <sub>CCCT</sub>							
I <sub>CCCH</sub>								

\* :  $T_a = +25\text{ }^\circ\text{C}$  and  $V_{CC} = 3.3\text{ V}$

(Continued)

# MB91610 Series

( $V_{CC} = AV_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_a = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ )

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current (MASK product)	I <sub>CC</sub>	V <sub>CC</sub>	Normal operation	—	35	45	mA	OSDC stopped Not using USB CPU : 33 MHz, Peripheral : 33 MHz
				—	50	60	mA	OSDC stopped Using USB CPU : 32 MHz, Peripheral : 32 MHz
	—			80	100	mA	Dot clock 50 MHz (PLL) Dot clock PLL is used Analog RGB DAC is used Digital RGB is not used CPU : 33 MHz, Peripheral : 33 MHz	
	—			80	110	mA	Dot clock 75 MHz (PLL) Dot clock PLL is used Analog RGB DAC is not used Digital RGB is used CPU : 33 MHz, Peripheral:33 MHz	
	I <sub>CCS</sub>		SLEEP mode	—	15	25	mA	OSDC stopped Not using USB Peripheral : 33 MHz
			SLEEP mode	—	25	40	mA	OSDC stopped Using USB Peripheral : 32 MHz
	I <sub>CCCL</sub>		Sub operation*	—	150	550	μA	CPU : 32 kHz Peripheral : 32 kHz
	I <sub>CCCT</sub>		Watch mode*	—	120	450	μA	
	I <sub>CCCH</sub>		STOP mode*	—	65	320	μA	

\* :  $T_a = +25\text{ }^{\circ}\text{C}$  and  $V_{CC} = 3.3\text{ V}$

(Continued)

# MB91610 Series

( $V_{CC} = AV_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
“H” level input voltage (hysteresis input)	$V_{IHS}$	P00 to P07, P10 to P17, P50 to P57, P70 to P77, PK0, PK1, DCKI, VSYNC, HSYNC, $\overline{\text{INIT}}$ , MD0, MD1	—	$V_{CC} \times 0.8$	—	$V_{CC} + 0.3$	V	
		P20 to P27, P30 to P37	—	$V_{CC} \times 0.8$	—	$V_{SS} + 5.5$	V	5 V tolerant
“L” level input voltage (hysteresis input)	$V_{ILS}$	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P50 to P57, P70 to P77, PK0, PK1, DCKI, VSYNC, HSYNC, $\overline{\text{INIT}}$ , MD0, MD1	—	$V_{SS} - 0.3$	—	$V_{CC} \times 0.2$	V	
“H” level output voltage	$V_{OH}$	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P50 to P57, P70 to P77, PK0, PK1,	$V_{CC} = 3.0\text{ V}$ $I_{OH} = -4\text{ mA}$	$V_{CC} - 0.5$	—	$V_{CC}$	V	
“L” level output voltage	$V_{OL}$	R0 to R4, G0 to G5, B0 to B4, VOA0 to VOA2, VOB, DCKO	$V_{CC} = 3.0\text{ V}$ $I_{OL} = 4\text{ mA}$	$V_{SS}$	—	0.4	V	
Input leak current	$I_{IL}$	—	—	- 5	—	+ 5	$\mu\text{A}$	Digital pin
				- 10	—	+ 10	$\mu\text{A}$	Analog pin
Pull-up resistance value	$R_{PU}$	Pull-up pin	—	16.6	33	66	k $\Omega$	
Pull-down resistance value	$R_{PD}$	IBREAK, ICD0 to ICD3	—	16.6	33	66	k $\Omega$	MB91F610A only
Input capacitance	$C_{IN}$	Other than $V_{CC}$ , $V_{SS}$ , $AV_{CC}$ , $AV_{SS}$ , AVRH	—	—	10	15	pF	

(Continued)

# MB91610 Series

(Continued)

( $V_{CC} = AV_{CC} = 3.0\text{ V to } 3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_a = -40\text{ }^\circ\text{C to } +85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Analog RGB reference voltage	$V_{REF}$	VREF	—	1.05	1.10	1.15	V	
Analog RGB reference resistance	$R_{REF}$	VRO-VSSD	—	2.4	2.7	—	k $\Omega$	
Analog RGB external load resistance	$R_L$	ROUT, GOUT, BOUT	—	—	150	160	$\Omega$	

## 4. AC Characteristics

### (1) Main Clock (MCLK) Input Standard

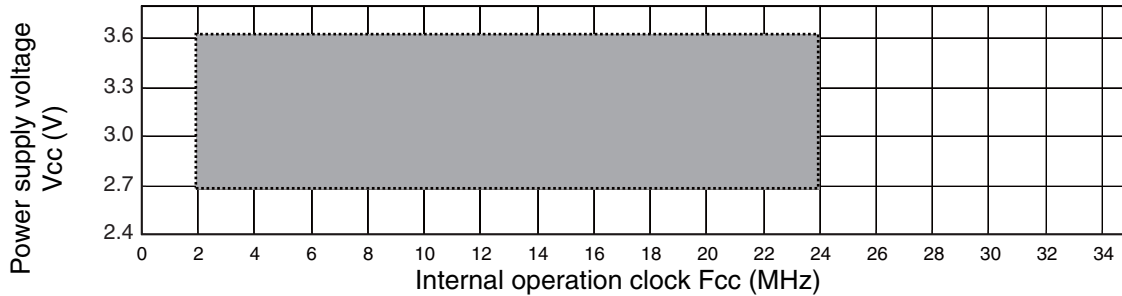
( $V_{CC} = AV_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	$F_{CH}$	X0, X1	—	4	48	MHz	When crystal oscillator is connected
			—	4	48	MHz	When using external clock
Input clock cycle	$t_{CYLH}$		—	20.83	250	ns	When using external clock
Input clock pulse width	—		$P_{WH}/t_{CYLH}$ $P_{WL}/t_{CYLH}$	45	55	%	When using external clock
Input clock rise time and fall time	$t_{CF}$ $t_{CR}$		—	—	5	ns	When using external clock
Internal operating clock frequency	$F_{CS}$	—	—	—	33	MHz	Source clock
	$F_{CC}$	—	—	—	33	MHz	CPU clock
	$F_{CP}$	—	—	—	33	MHz	Peripheral bus clock
Internal operating clock cycle time	$t_{CYCS}$	—	—	30	—	ns	Source clock
	$t_{CYCC}$	—	—	30	—	ns	CPU clock
	$t_{CYCP}$	—	—	30	—	ns	Peripheral bus clock

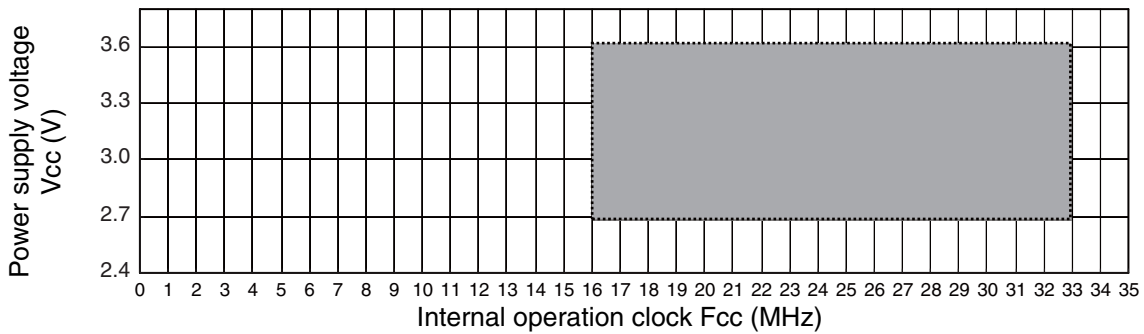
# MB91610 Series

- Operating guaranteed range (Not using USB)

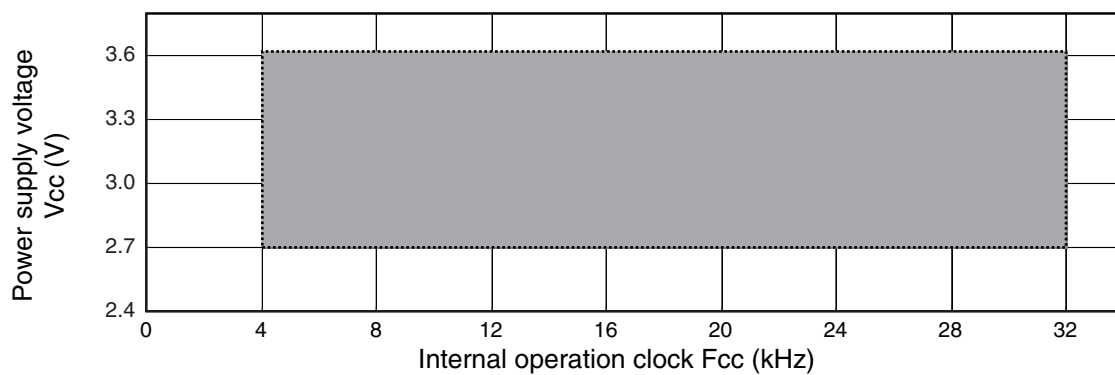
- When the main clock is selected (DIVB=000)



- When the PLL clock is selected (DIVB=000)

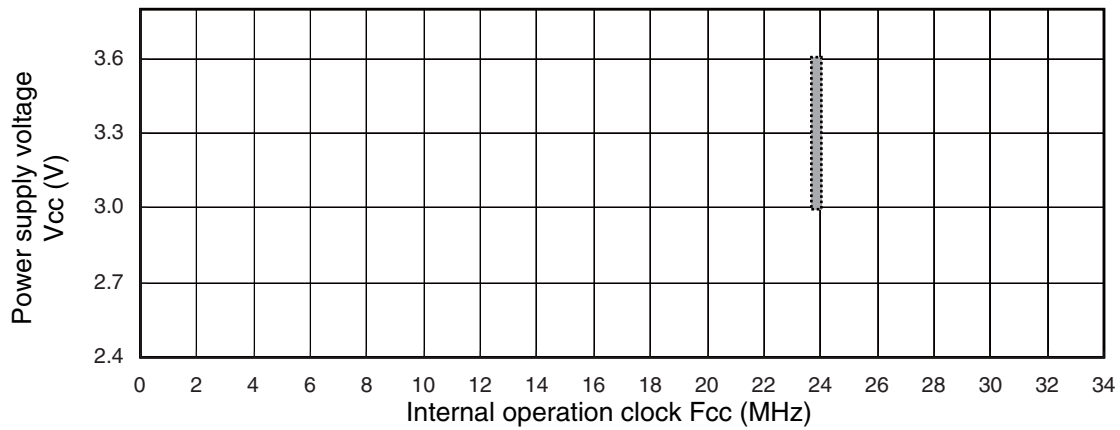


- When the sub clock is selected

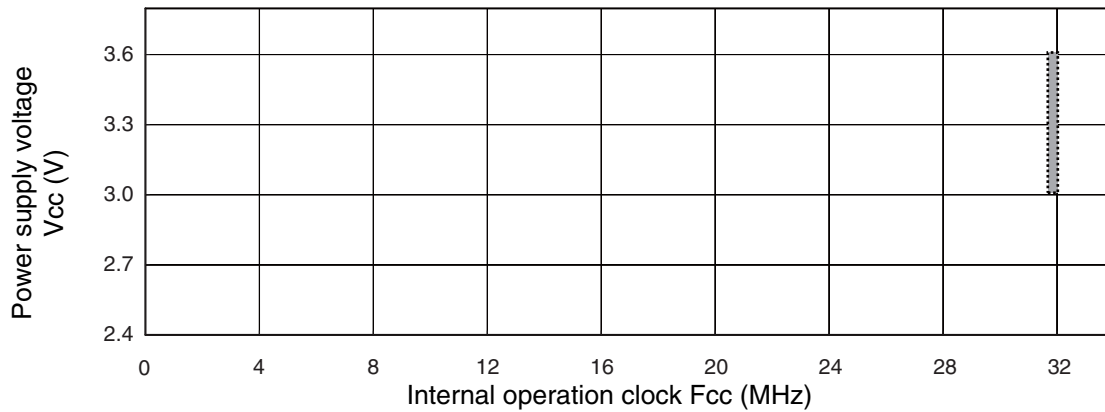


- Operating guaranteed range (at using USB)

- When the main clock is selected (DIVB=000\*1)



- When the PLL clock is selected (DIVB=000\*1, ODS=10\*3, PMS=0111\*4, PDS=0000\*2, X0=4 MHz or DIVB=000\*1, ODS=10\*3, PMS=0001\*4, PDS=0010\*2, X0=48 MHz)



\*1 : The values other than DIVB = 000 are omitted.

\*2 : The values other than PDS = 0000, 0001, 0010 are omitted.

\*3 : The values other than ODS = 10 are omitted.

\*4 : The values other than PMS = 0001, 0111 are omitted.

Note: DIVB : Base clock division configuration bit  
 ODS : PLL macro oscillation clock division rate select bit  
 PDS : PLL input clock division select bit  
 PMS : PLL clock multiple rate select bit

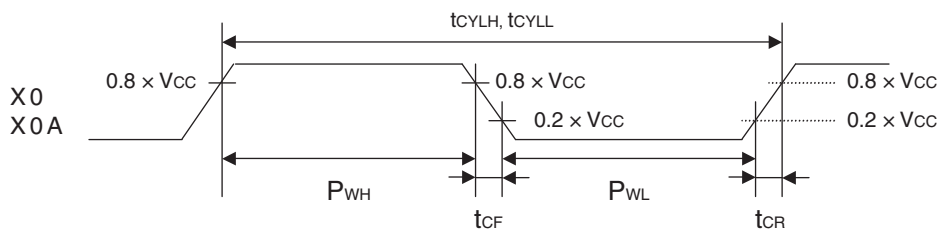
# MB91610 Series

## (2) Sub Clock (SBCLK) Input Standard

( $V_{CC} = AV_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_a = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ )

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	$F_{CL}$	X0A, X1A	—	—	32.768	—	kHz	When crystal oscillator is connected
			—	—	32.768	—	kHz	When using external clock
Input clock cycle	$t_{CYLL}$		—	—	30.518	—	$\mu\text{s}$	When using external clock
Input clock pulse width	—		$P_{WH} / t_{CYLL}$ $P_{WL} / t_{CYLL}$	45	—	55	%	When using external clock
Input clock rise time and fall time	$t_{CF}$ , $t_{CR}$		—	—	—	200	ns	When using external clock

<When external clock input>



### (3) Conditions of PLL

( $V_{CC} = AV_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time (LOCK UP time)	$t_{LOCK}$	600	—	—	$\mu\text{s}$	Time from when the PLL starts operating until the oscillation stabilizes
PLL oscillation stabilization wait time for OSDC (LOCK UP time)	$t_L$	10	—	—	ms	
PLL input clock frequency	$f_{PLLI}$	4	—	24	MHz	
PLL multiple rate	—	4	—	24	multiplied by	ODS $\times$ PMS
PLL macro oscillation clock frequency	$f_{PLLO}$	96	—	100	MHz	

### (4) Regulator Voltage Stabilization Wait Time

( $V_{CC} = AV_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Regulator voltage stabilization wait time	$t_{REG}$	50	—	$\mu\text{s}$	Time taken for the regulator voltage to stabilize

Note : This is the time from when the external power supply stabilizes (after reaching 3.0 V).

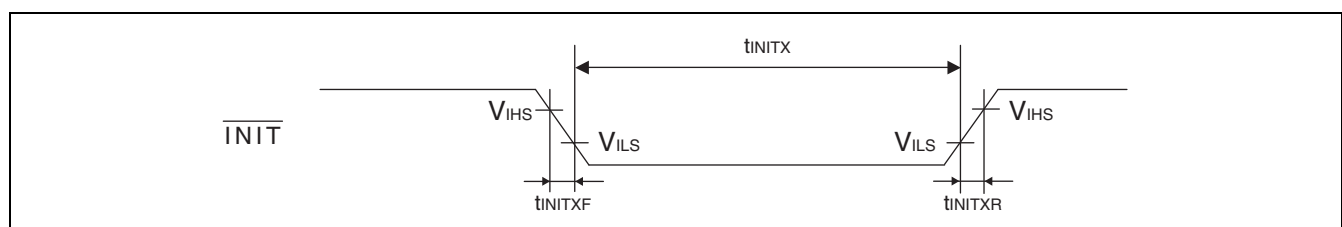
### (5) Reset Input Standards

( $V_{CC} = AV_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time (At power-on, main oscillation stop mode)	$t_{INITX}$	$\overline{INIT}$	—	Oscillation time of oscillator + $10 t_{CYLH}$	—	ns	*
Reset input time (At other times)				$10 t_{CYLH}$	—	ns	
Reset input rise time and fall time	$t_{INITXF}$ $t_{INITXR}$			—	10	ms	

\* : After the supply voltage has stabilized, it takes a further 50  $\mu\text{s}$  until the internal supply stabilizes. Hold the input to the  $\overline{INIT}$  pin during that period.

- At power-on
- When in stop mode
- When in sub mode and sub watch mode when the main oscillation is stopped.



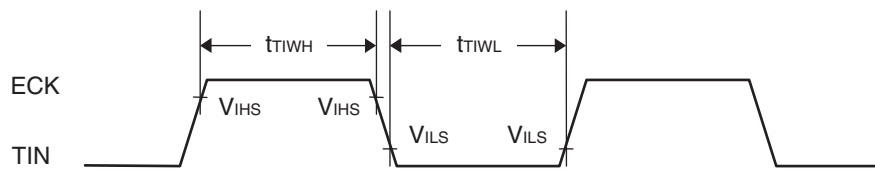
# MB91610 Series

## (6) Base Timer Input Timing

- Timer input timing

( $V_{CC} = AV_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

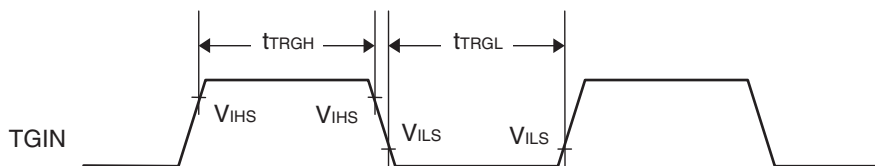
Parameter	Symbol	Pin name	Condi- tions	Value		Unit
				Min	Max	
Input pulse width	$t_{TIWH}$ , $t_{TIWL}$	TIOAn/TIOBn (When used as ECK, TIN)	—	$2 t_{CYCP}$	—	ns



- Trigger Input Timing

( $V_{CC} = AV_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condi- tions	Value		Unit
				Min	Max	
Input pulse width	$t_{TRGH}$ , $t_{TRGL}$	TIOAn/TIOBn (When used as TGIN)	—	$2 t_{CYCP}$	—	ns



## (7) Synchronous serial (CSIO) timing

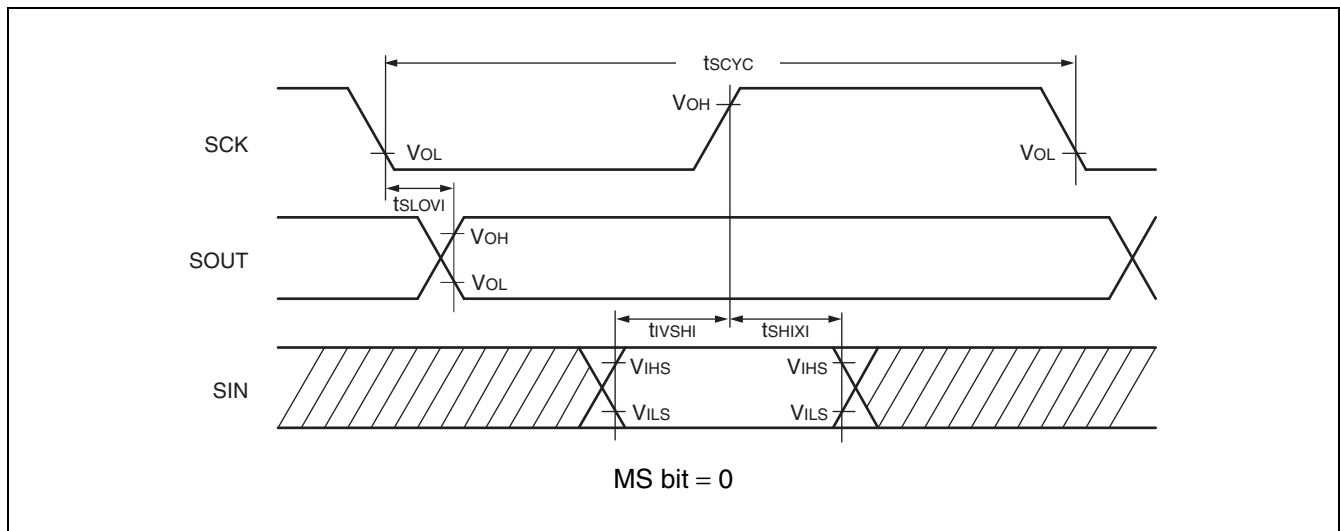
( $V_{CC} = AV_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_a = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ )

- Synchronous serial (SPI = 0, SCINV = 0)

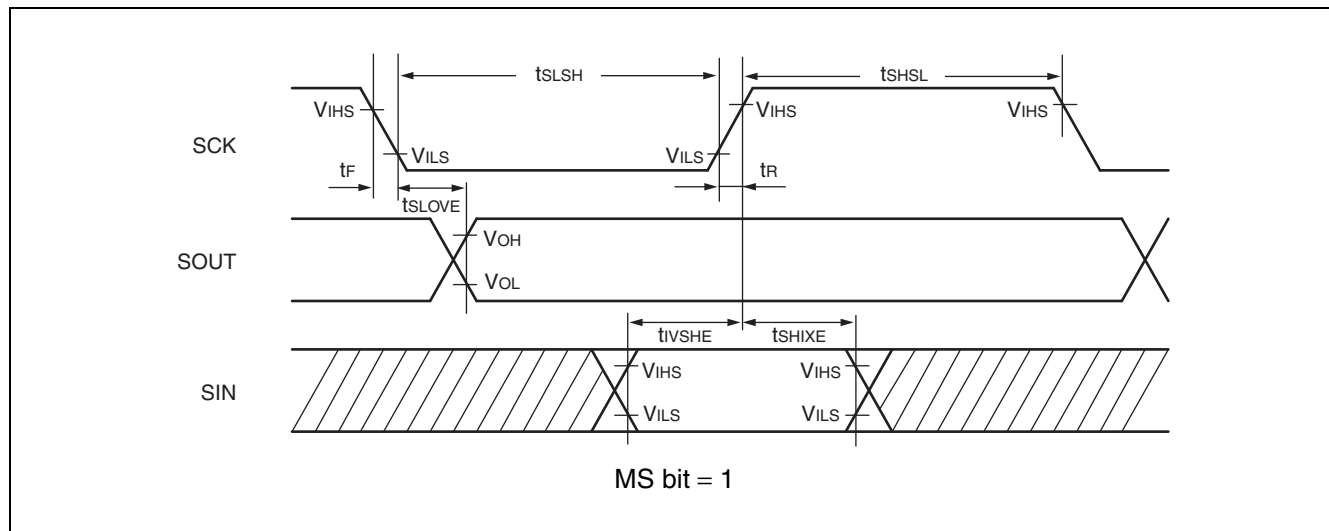
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	$t_{SCYC}$	SCKn	Internal shift clock operation	$4t_{CYCP}$	—	ns
SCK ↓ → SOUT delay time	$t_{SLOVI}$	SCKn, SOUTn		- 30	+ 30	ns
SIN → SCK ↑ setup time	$t_{VSHI}$	SCKn, SINn		57	—	ns
SCK ↑ → SIN hold time	$t_{SHIXI}$	SCKn, SINn		0	—	ns
Serial clock “L” pulse width	$t_{LSLH}$	SCKn	External shift clock operation	$2t_{CYCP} - 10$	—	ns
Serial clock “H” pulse width	$t_{HSLH}$	SCKn		$t_{CYCP} + 10$	—	ns
SCK ↓ → SOUT delay time	$t_{SLOVE}$	SCKn, SOUTn		—	48	ns
SIN → SCK ↑ setup time	$t_{VSHI}$	SCKn, SINn		25	—	ns
SCK ↑ → SIN hold time	$t_{SHIXE}$	SCKn, SINn		20	—	ns
SCK fall time	$t_F$	SCKn		—	5	ns
SCK rise time	$t_R$	SCKn		—	5	ns

Notes: • The above standards apply to CLK synchronous mode.

- $t_{CYCP}$  indicates the peripheral clock cycle time.
- When the external load capacitance  $C = 50\text{ pF}$ .



# MB91610 Series

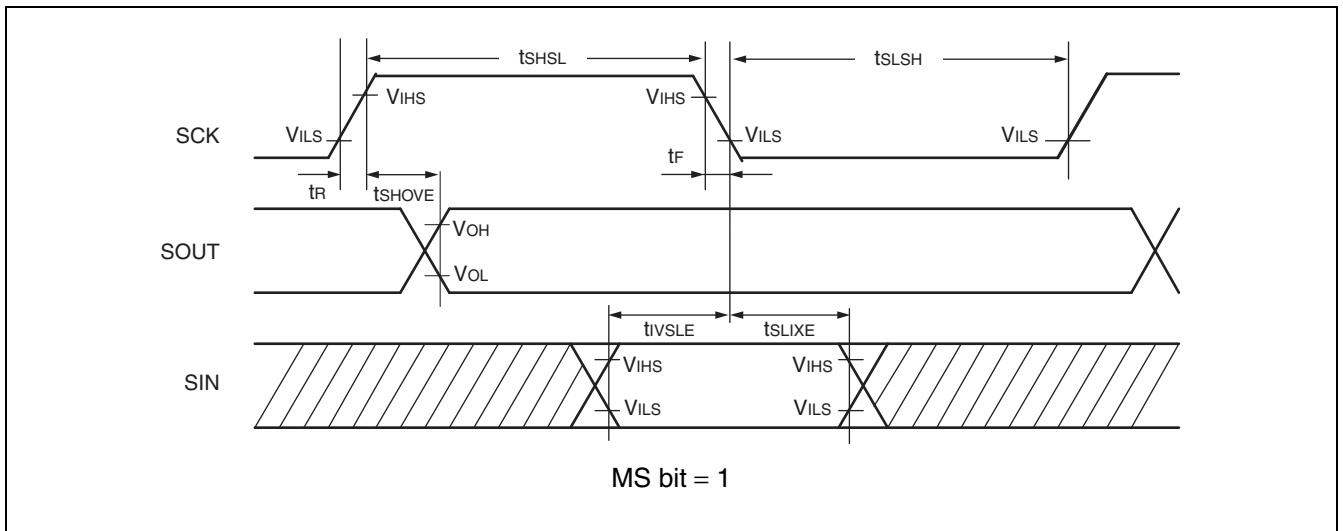
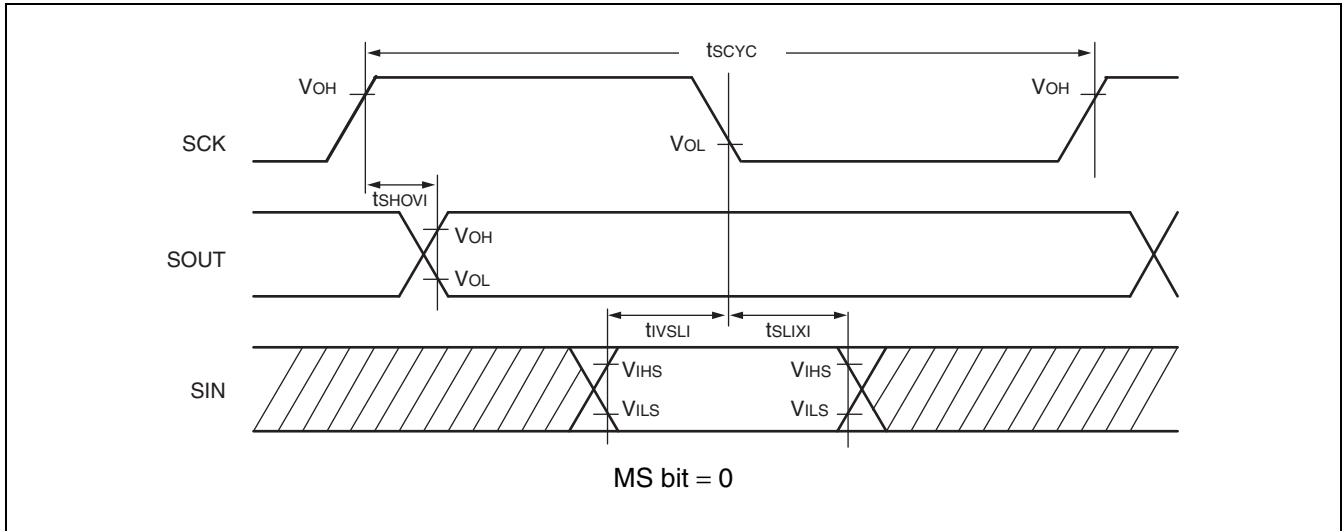


• Synchronous serial (SPI = 0, SCINV = 1)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	$t_{SCYC}$	SCKn	Internal shift clock operation	$4t_{CYCP}$	—	ns
SCK $\uparrow$ $\rightarrow$ SOUT delay time	$t_{SHOVI}$	SCKn, SOUTn		- 30	+ 30	ns
SIN $\rightarrow$ SCK $\downarrow$ setup time	$t_{IVSLI}$	SCKn, SINn		57	—	ns
SCK $\downarrow$ $\rightarrow$ SIN hold time	$t_{SLIXI}$	SCKn, SINn		0	—	ns
Serial clock "L" pulse width	$t_{SLSH}$	SCKn	External shift clock operation	$2t_{CYCP} - 10$	—	ns
Serial clock "H" pulse width	$t_{SHSL}$	SCKn		$t_{CYCP} + 10$	—	ns
SCK $\uparrow$ $\rightarrow$ SOUT delay time	$t_{SHOVE}$	SCKn, SOUTn		—	48	ns
SIN $\rightarrow$ SCK $\downarrow$ setup time	$t_{IVSLE}$	SCKn, SINn		25	—	ns
SCK $\downarrow$ $\rightarrow$ SIN hold time	$t_{SLIXE}$	SCKn, SINn		20	—	ns
SCK fall time	$t_F$	SCKn		—	5	ns
SCK rise time	$t_R$	SCKn		—	5	ns

Notes: • The above standards apply to CLK synchronous mode.

- $t_{CYCP}$  indicates the peripheral clock cycle time.
- When the external load capacitance  $C = 50$  pF.



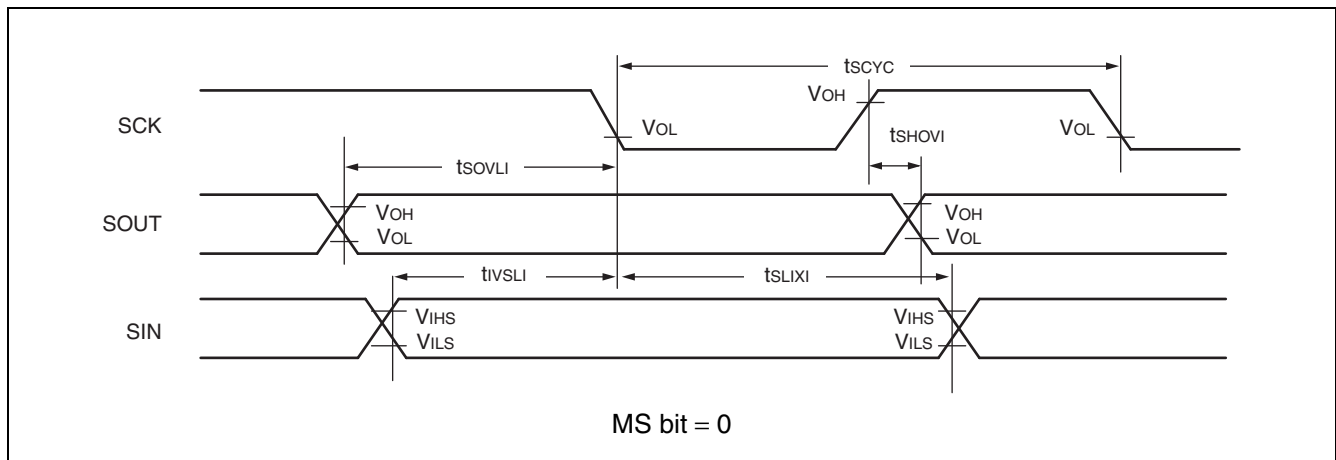
# MB91610 Series

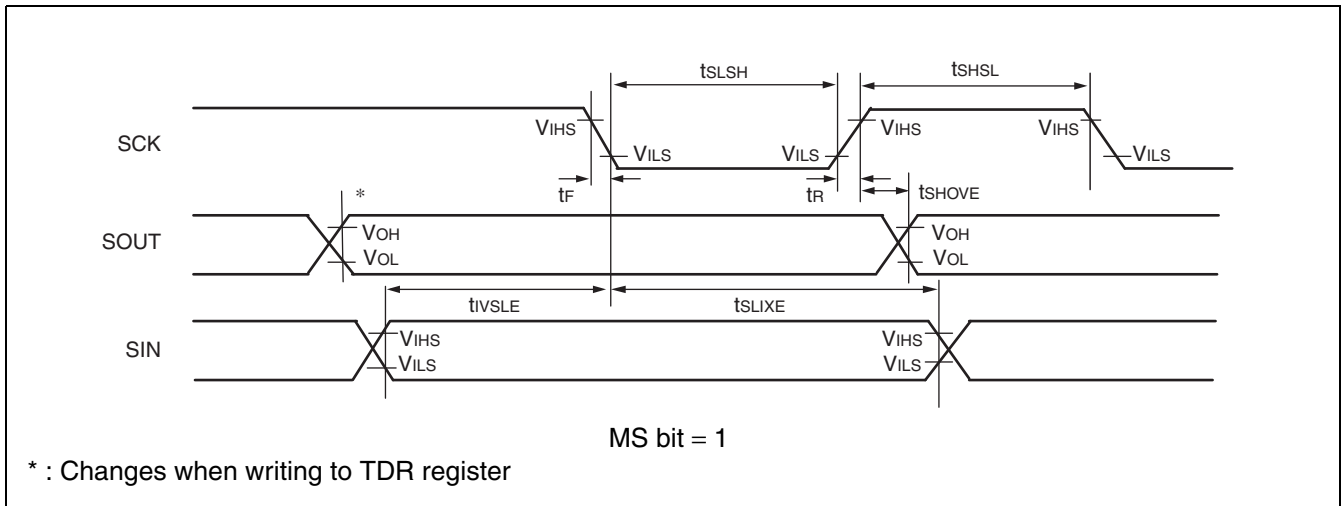
- Synchronous serial (SPI = 1, SCINV = 0)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	$t_{SCYC}$	SCKn	Internal shift clock operation	$4t_{CYCP}$	—	ns
SCK $\uparrow$ $\rightarrow$ SOUT delay time	$t_{SHOVI}$	SCKn, SOUTn		- 30	+ 30	ns
SIN $\rightarrow$ SCK $\downarrow$ setup time	$t_{IVSLI}$	SCKn, SINn		57	—	ns
SCK $\downarrow$ $\rightarrow$ SIN hold time	$t_{SLIXI}$	SCKn, SINn		0	—	ns
SOUT $\rightarrow$ SCK $\downarrow$ delay time	$t_{SOVLI}$	SCKn, SOUTn		$2t_{CYCP} - 30$	—	ns
Serial clock "L" pulse width	$t_{LSLH}$	SCKn	External shift clock operation	$2t_{CYCP} - 10$	—	ns
Serial clock "H" pulse width	$t_{HSL}$	SCKn		$t_{CYCP} + 10$	—	ns
SCK $\uparrow$ $\rightarrow$ SOUT delay time	$t_{SHOVE}$	SCKn, SOUTn		—	48	ns
SIN $\rightarrow$ SCK $\downarrow$ setup time	$t_{IVSLE}$	SCKn, SINn		25	—	ns
SCK $\downarrow$ $\rightarrow$ SIN hold time	$t_{SLIXE}$	SCKn, SINn		20	—	ns
SCK fall time	$t_F$	SCKn		—	5	ns
SCK rise time	$t_R$	SCKn		—	5	ns

Notes: • The above standards apply to CLK synchronous mode.

- $t_{CYCP}$  indicates the peripheral clock cycle time.
- When the external load capacitance  $C = 50$  pF.





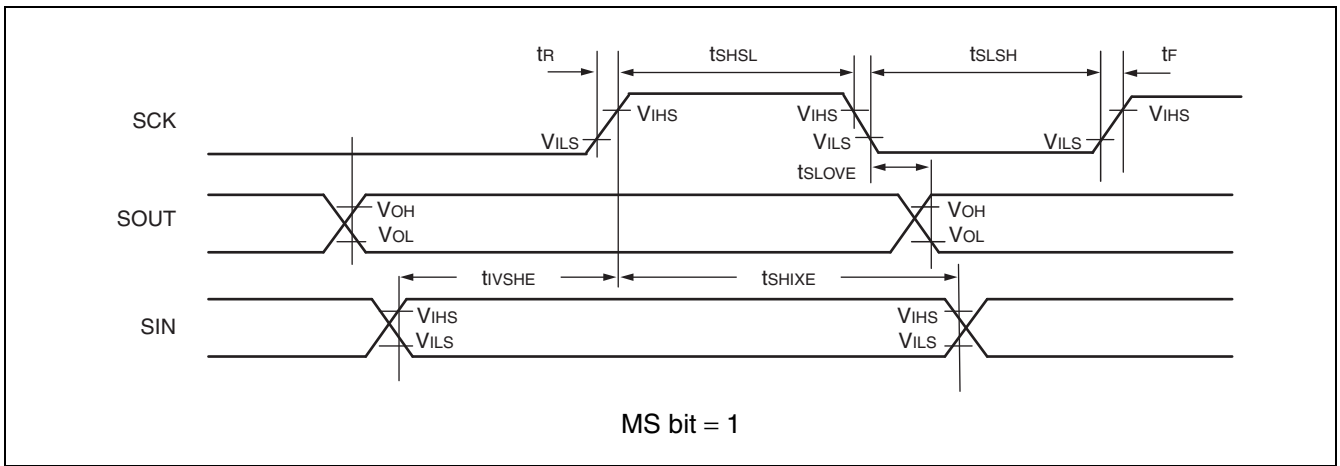
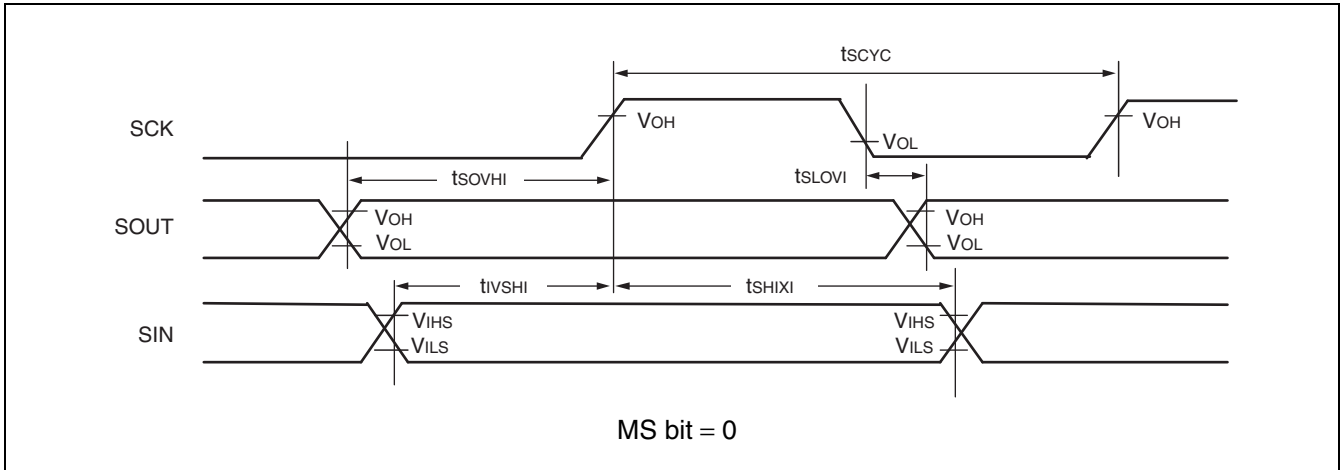
• Synchronous serial (SPI = 1, SCINV = 1)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	$t_{SCYC}$	SCKn	Internal shift clock operation	$4t_{CYCP}$	—	ns
SCK ↓ → SOUT delay time	$t_{SLOVI}$	SCKn, SOUTn		- 30	+ 30	ns
SIN → SCK ↑ setup time	$t_{IVSHI}$	SCKn, SINn		57	—	ns
SCK ↑ → SIN hold time	$t_{SHIXI}$	SCKn, SINn		0	—	ns
SOUT → SCK ↑ delay time	$t_{SOVHI}$	SCKn, SOUTn		$2t_{CYCP} - 30$	—	ns
Serial clock “L” pulse width	$t_{SLSH}$	SCKn		$2t_{CYCP} - 10$	—	ns
Serial clock “H” pulse width	$t_{SHSL}$	SCKn	External shift clock operation	$t_{CYCP} + 10$	—	ns
SCK ↓ → SOUT delay time	$t_{SLOVE}$	SCKn, SOUTn		—	48	ns
SIN → SCK ↑ setup time	$t_{IVSHE}$	SCKn, SINn		25	—	ns
SCK ↑ → SIN hold time	$t_{SHIXE}$	SCKn, SINn		20	—	ns
SCK fall time	$t_F$	SCKn		—	5	ns
SCK rise time	$t_R$	SCKn		—	5	ns

Notes: • The above standards apply to CLK synchronous mode.

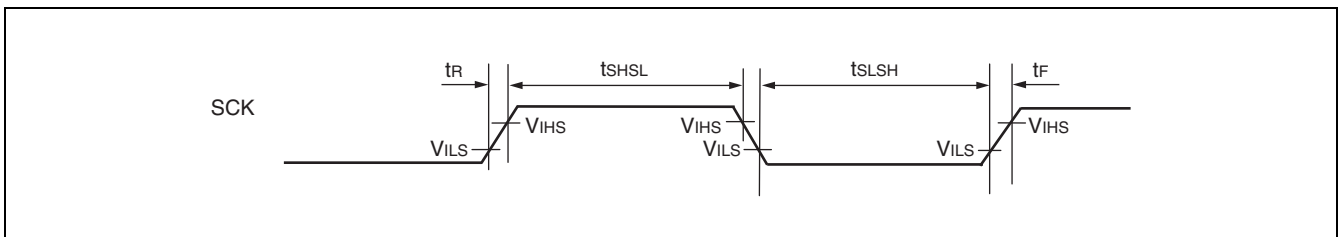
- $t_{CYCP}$  indicates the peripheral clock cycle time.
- When the external load capacitance  $C = 50$  pF.

# MB91610 Series



- External clock (EXT = 1) : asynchronous only

Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
Serial clock "L" pulse width	$t_{SLSH}$	$C_L = 50 \text{ pF}$	$t_{CYCP} + 10$	—	ns
Serial clock "H" pulse width	$t_{SHSL}$		$t_{CYCP} + 10$	—	ns
SCK fall time	$t_f$		—	5	ns
SCK rise time	$t_r$		—	5	ns



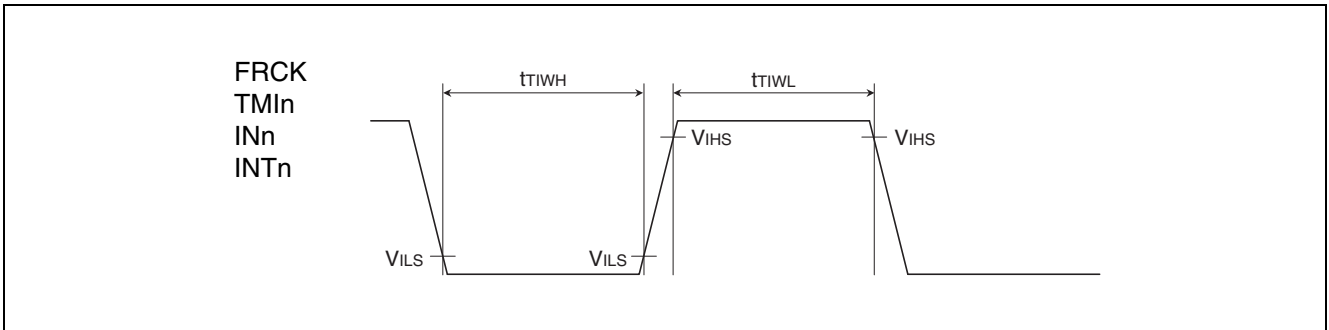
## (8) Free-run Timer Clock, Reload Timer Event Input, Input Capture Input, Interrupt Input Timing

( $V_{CC} = AV_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condi- tions	Value		Unit	Remarks
				Min	Max		
Input pulse width	$t_{TIWH}$ , $t_{TIWL}$	FRCK, TMIn, INn	—	$2 t_{CYCP}$	—	ns	*1
		INTn	—	$3 t_{CYCP}$	—	ns	*1
			—	1.0	—	$\mu\text{s}$	*2

\*1 :  $t_{CYCP}$  indicates peripheral clock cycle time, except when in stop mode, in main timer mode and in watch mode.

\*2 : When in stop mode, in main timer mode, or in watch mode.

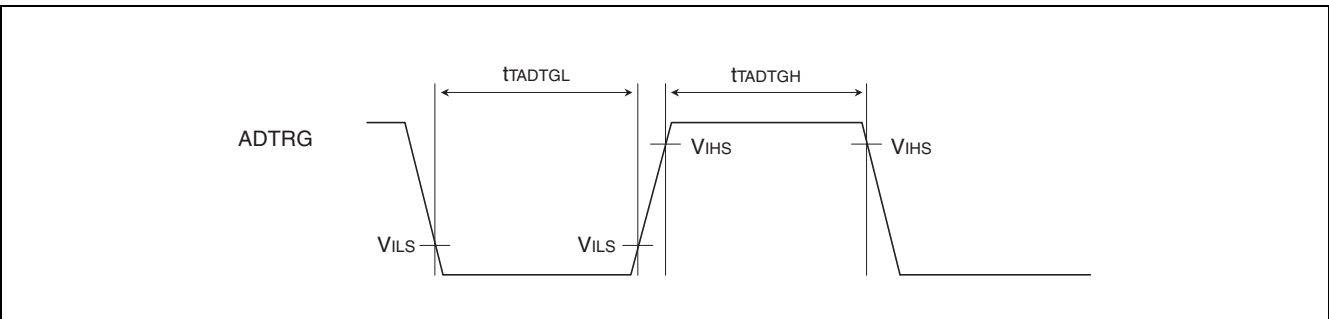


## (9) A/D Converter Trigger Input Timing

( $V_{CC} = AV_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condi- tions	Value		Unit	Remarks
				Min	Max		
A/D converter trigger input	$t_{TADTGL}$ , $t_{TADTGH}$	ADTRG	—	$2 t_{CYCP}$	—	ns	*

\* :  $t_{CYCP}$  indicates peripheral clock cycle time.



# MB91610 Series

## (10) I<sup>2</sup>C Timing

(V<sub>CC</sub> = AV<sub>CC</sub> = 3.0 V to 3.6 V, V<sub>SS</sub> = AV<sub>SS</sub> = 0 V, Ta = -40 °C to +85 °C)

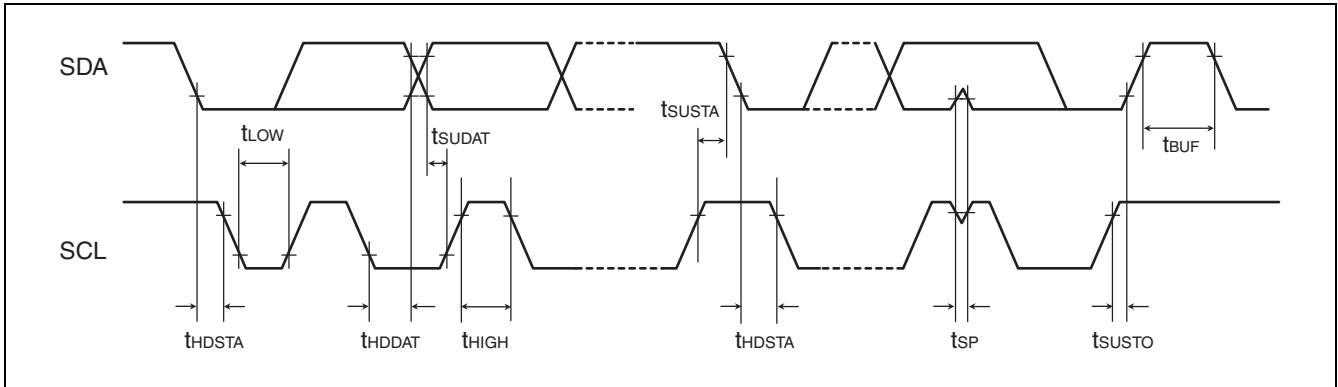
Parameter	Symbol	Pin name	Condi- tions	Typical mode		High-speed mode*3		Unit
				Min	Max	Min	Max	
SCL clock frequency	f <sub>SCL</sub>	SCKn (SCLn)	C <sub>L</sub> = 50 pF, R = (V <sub>p</sub> /I <sub>oL</sub> ) *1	0	100	0	400	kHz
“(Repeated) START condition” hold time SDA ↓ → SCL ↓	t <sub>HDSTA</sub>	SOUTn (SDAn), SCKn (SCLn)		4.0	—	0.6	—	μs
SCL clock “L” width	t <sub>LOW</sub>	SCKn (SCLn)		4.7	—	1.3	—	μs
SCL clock “H” width	t <sub>HIGH</sub>	SCKn (SCLn)		4.0	—	0.6	—	μs
“(Repeated) START condition” setup time SCL ↑ → SDA ↓	t <sub>SUSTA</sub>	SCKn (SCLn)		4.7	—	0.6	—	μs
Data hold time SCL ↓ → SDA ↓ ↑	t <sub>HDDAT</sub>	SOUTn (SDAn), SCKn (SCLn)		0	3.45*2	0	0.9*3	μs
Data setup time SDA ↓ ↑ → SCL ↑	t <sub>SUDAT</sub>	SOUTn (SDAn), SCKn (SCLn)		250	—	100	—	ns
“(STOP condition) setup time SCL ↑ → SDA ↑	t <sub>SUSTO</sub>	SOUTn (SDAn), SCKn (SCLn)		4.0	—	0.6	—	μs
Bus free time between “(STOP condition)” and “(START condition)”	t <sub>BUF</sub>	—		4.7	—	1.3	—	μs
Noise filter	t <sub>SP</sub>	—	—	2 t <sub>CYCP</sub> *4	—	2 t <sub>CYCP</sub> *4	—	ns

\*1 : R and C represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. V<sub>p</sub> indicates the power supply voltage of the pull-up resistance and I<sub>oL</sub> indicates V<sub>oL</sub> guaranteed current.

\*2 : The maximum t<sub>HDDAT</sub> must satisfy that it doesn't extend at least “L” period (t<sub>LOW</sub>) of device's SCL signal.

\*3 : A high-speed mode I<sup>2</sup>C bus device can be used on a standard mode I<sup>2</sup>C bus system as long as the device satisfies the requirement of “t<sub>SUDAT</sub> ≥ 250 ns”.

\*4 : t<sub>CYCP</sub> is the peripheral clock cycle time. To use I<sup>2</sup>C, set the peripheral bus clock at 8 MHz or more.

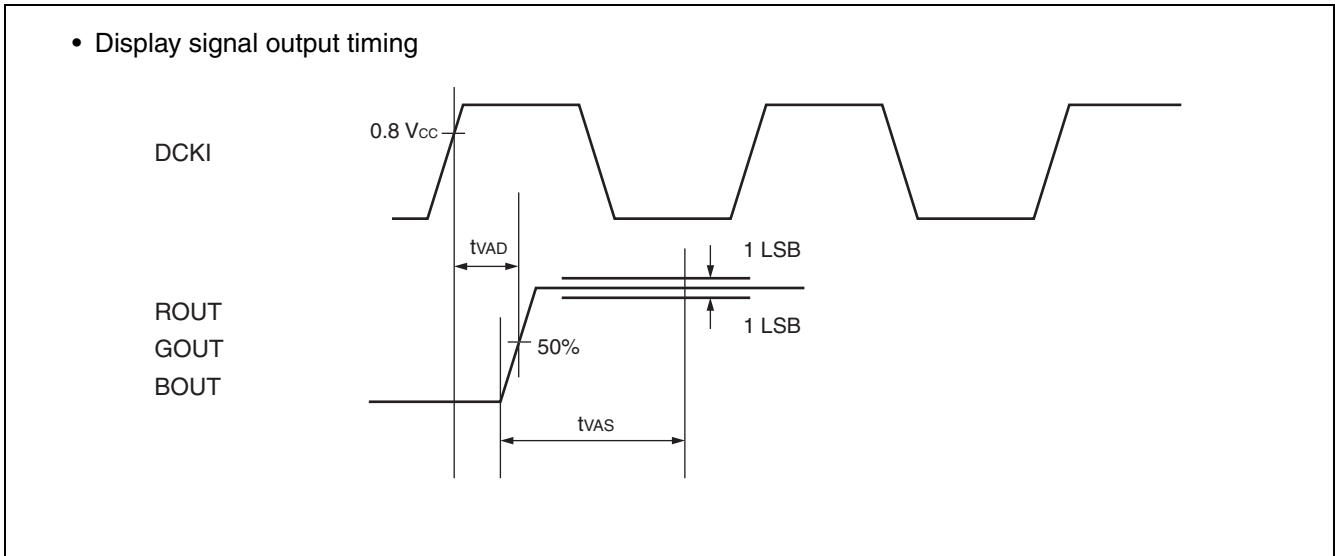


## (11) Analog RGB

( $V_{CC} = AV_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_a = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ )

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Analog RGB output delay	$t_{VAD}$	ROUT, GOUT, BOUT	$V_{REF} = 1.1\text{ V}$ , $V_{DDD} = 3.3\text{ V}$ , $V_{RO}^* = 2.7\text{ k}\Omega$	—	12	—	ns	50 MHz (Max)
Analog RGB output settling time	$t_{VAS}$			—	—	20	ns	

\* :  $V_{RO}$  is an external resistance for DAC.



# MB91610 Series

## (12) Digital RGB

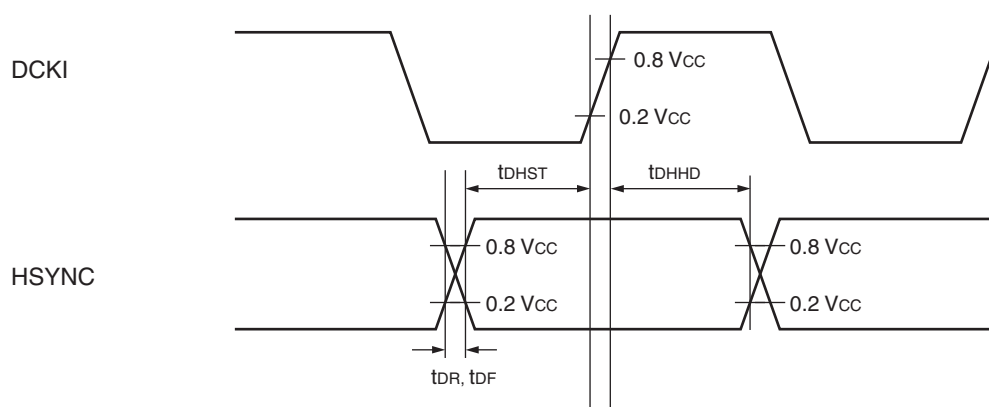
Vertical synchronous/ horizontal synchronous/ display output control signal input timing

( $V_{CC} = AV_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_a = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ )

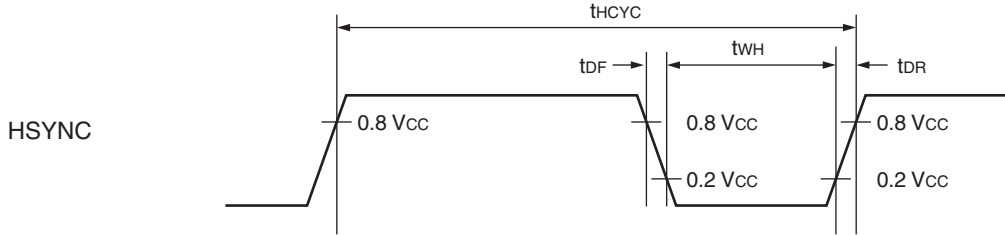
Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Horizontal synchronous signal cycle time	$t_{HCYC}$	HSYNC	$100 + t_{WH}$	—	Dot clock	
Horizontal synchronous signal pulse width	$t_{WH}$	HSYNC	20	—	Dot clock	
			—	6	$\mu\text{s}$	
Horizontal synchronous signal setup time	$t_{DHST}$	HSYNC	4	—	ns	
Horizontal synchronous signal hold time	$t_{DHHD}$		0	—	ns	
Vertical synchronous signal setup time	$t_{HVST}$	VSYNC	5	—	Dot clock	
Vertical synchronous signal hold time	$t_{HVHD}$		1H – 5	—	Dot clock	
Input synchronous signal rising/falling time	$t_{DR}$ , $t_{DF}$	HSYNC, VSYNC	—	2	ns	

\* : H stands for the horizontal synchronous signal. 1 synchronous is 1 unit.

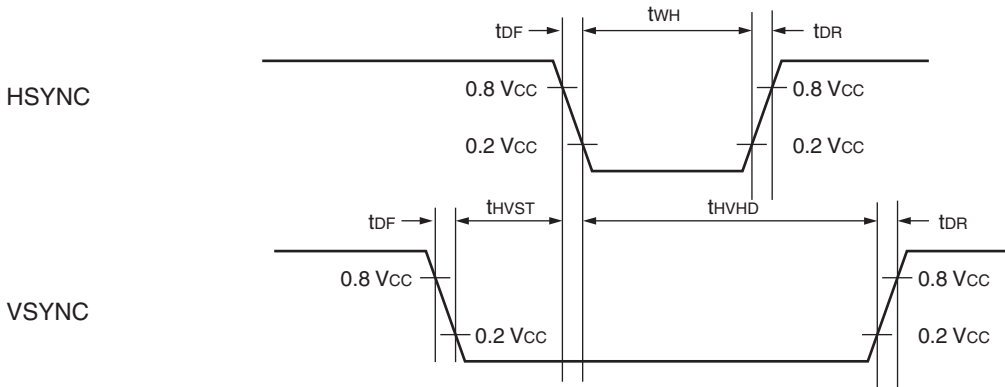
### • Horizontal synchronous signal and display output control signal input timing



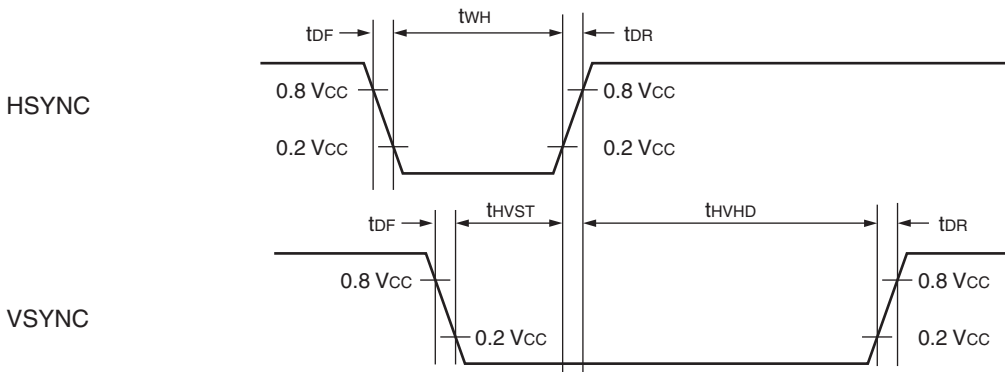
- Horizontal synchronous signal input



- Vertical synchronous signal input timing
  - Detect VSYNC at HSYNC leading edge



- Detect VSYNC at HSYNC trailing edge



# MB91610 Series

## (13) Display signal timing

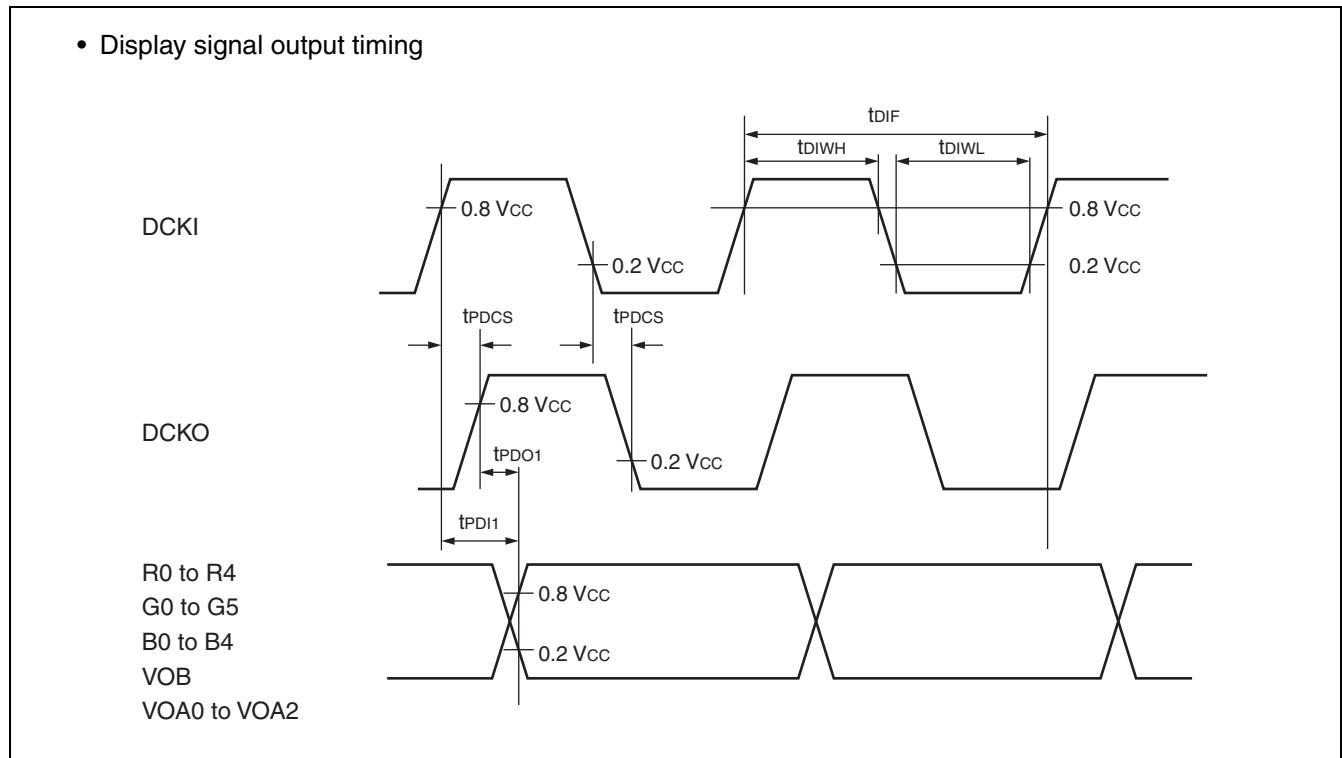
( $V_{CC} = AV_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_a = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ )

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Dot clock input cycle time	$t_{DIF}$	DCKI	8	75	MHz	*1
Dot clock input pulse width	$t_{DIWH}$	DCKI	5	—	ns	*1
	$t_{DIWL}$		5	—	ns	
Dot clock output delay time1	$t_{PDCS}$	DCKO	2.2	8	ns	*2
Display signal output delay time I1	$t_{PDI1}$	R0 to R4, G0 to G5, B0 to B4, VOB, VOA0 to VOA2	2	8.3	ns	*2
Display signal output delay time O1	$t_{PDO1}$		-4	+5	ns	*2

\*1 : Input continuous signal to the dot clock.

\*2 : Output load 16 pF

Note: Actual display output varies depending on what is controlled, such as display output control and display location control in each display layer.



## 5. Electrical Characteristics for the A/D Converter

( $V_{CC} = AV_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_a = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ )

Parameter	Pin name	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	10	bit	
Total error	—	-5	—	+5	LSB	$AV_{CC} = 3.3\text{ V}$ , $AV_{RH} = 3.3\text{ V}$
Linearity error	—	-3.5	—	+3.5	LSB	
Differential linearity error	—	-3	—	+3	LSB	
Zero transition voltage	AN0 to AN7	-1.5	+0.5	+4	LSB	
Full transition voltage	AN0 to AN7	$AV_{RH} - 4$	$AV_{RH} - 1.5$	$AV_{RH} + 0.5$	LSB	
Compare time	—	$0.72^{*3}$	—	—	$\mu\text{s}$	PCLK = 33 MHz
Conversion time	—	$1.2^{*1}$	—	—	$\mu\text{s}$	PCLK = 33 MHz
Power supply current (analog + digital)	$AV_{CC}$	—	—	3.5	mA	D/A stopped
		—	—	11	$\mu\text{A}$	At power-down <sup>*2</sup>
Reference power supply current (between $AV_{RH}$ and $AV_{SS}$ )	$AV_{RH}$	—	—	0.6	mA	$AV_{RH} = 3.0\text{ V}$
		—	—	5	$\mu\text{A}$	At power-down <sup>*2</sup>
Analog input capacity	—	—	—	8.5	pF	
Interchannel disparity	—	—	—	4	LSB	
Analog port input current	AN0 to AN7	—	—	10	$\mu\text{A}$	
Analog input voltage	AN0 to AN7	$AV_{SS}$	—	$AV_{RH}$	V	
Standard voltage	$AV_{RH}$	$AV_{SS}$	—	$AV_{CC}$	V	

\*1 : Depending on the clock cycle supplied to peripheral resources.

Ensure that it satisfies the value; PCLK cycle  $\times$  more than 4 + the value calculated from (Equation 1).

The condition of the minimum conversion time is when PCLK = 33 MHz, the value of sampling time: 0.424  $\mu\text{s}$ , external impedance: 1.4 k $\Omega$  or less and compare time: 0.72  $\mu\text{s}$ .

\*2 : The current when the CPU is in stop mode and the A/D converter is not operating.

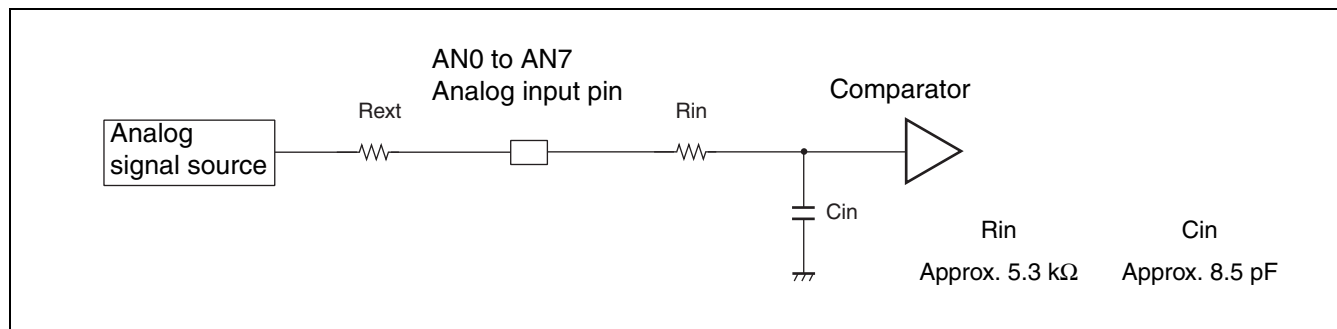
\*3 : Compare time =  $\{(CT + 1) \times 10 + 4\} \times$  peripheral clock (PCLK) period. (CT indicates compare time setting bits.)

The condition of the minimum compare time is when CT = 1 and PCLK = 33 MHz.

(Continued)

# MB91610 Series

(Continued)



The output impedance of the external circuit connected to the analog input affects the sampling time of the A/D converter. Design the output impedance of the output circuit such that the required sampling time is less than the value of  $T_s$  calculated from the following equation.

(Equation 1)  $T_s = (R_{in} + R_{ext}) \times C_{in} \times 8$

- $T_s$  : Sampling time
- $R_{in}$  : Input resistance of A/D = 5.3 kΩ
- $C_{in}$  : Input capacitance of A/D = 8.5 pF
- $R_{ext}$  : Output impedance of external circuit

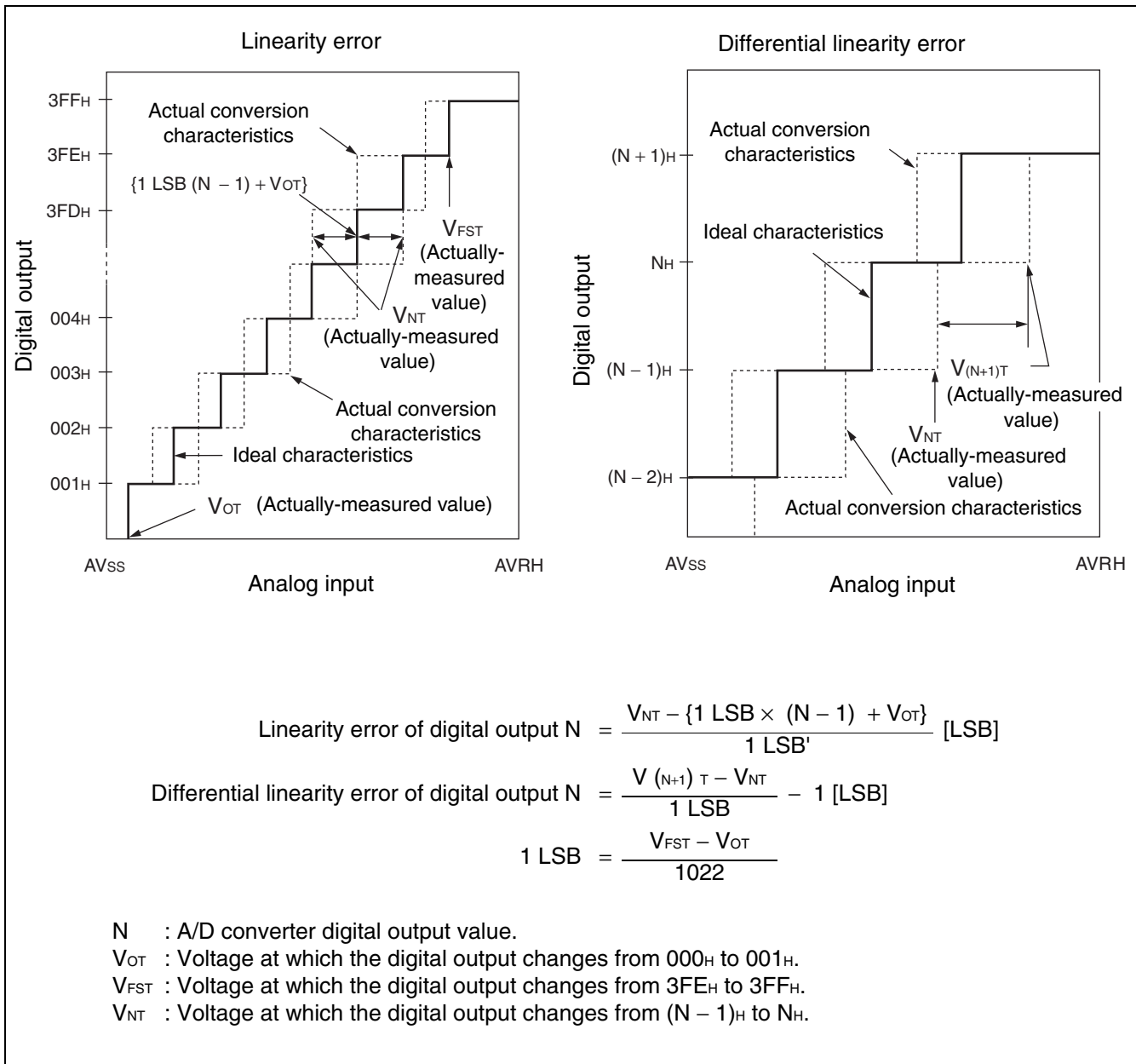
If the sampling time is set as 600 ns,

$$600 \text{ ns} \geq (5.3 \text{ k}\Omega + R_{ext}) \times 8.5 \text{ pF} \times 8$$
$$\therefore R_{ext} \leq 3.5 \text{ k}\Omega$$

And the impedance of the external circuit therefore needs to be 3.5 kΩ or less.

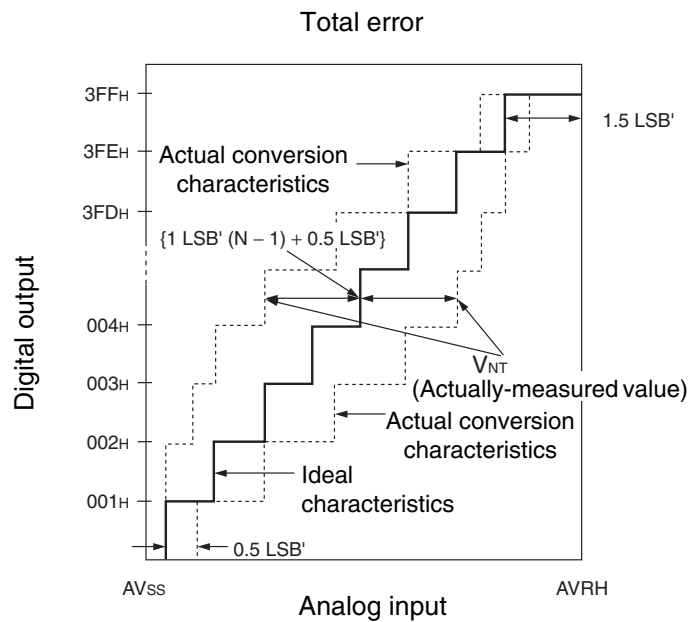
• Definition of 10-bit A/D Converter Terms

- Resolution : Analog variation that is recognized by an A/D converter.
- Linearity error : Deviation of the line between the zero-transition point (0000000000 $\leftarrow$ →0000000001) and the full-scale transition point (1111111110 $\leftarrow$ →1111111111) from the actual conversion characteristics.
- Differential linearity error : Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.
- Total error : Difference between the actual value and the theoretical value. The total error includes zero transition error, full-scale transition error, and linear error.



(Continued)

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$$1 \text{ LSB}' (\text{Ideal value}) = \frac{AVRH - AVSS}{1024} \text{ [V]}$$

$$\text{Total error of digital output } N = \frac{V_{NT} - \{1 \text{ LSB}' \times (N - 1) + 0.5 \text{ LSB}'\}}{1 \text{ LSB}'}$$

N : A/D converter digital output value.

$V_{NT}$  : Voltage at which the digital output changes from  $(N + 1)_H$  to  $N_H$ .

$V_{OT}'$  (Ideal value) =  $AVSS + 0.5 \text{ LSB}$  [V]

$V_{FST}'$  (Ideal value) =  $AVRH - 1.5 \text{ LSB}$  [V]

## 6. Electrical Characteristics for the Analog RGB D/A Converter

( $V_{CC} = AV_{CC} = 3.0\text{ V to } 3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_a = -40\text{ °C to } +85\text{ °C}$ )

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Resolution	—	—	5	bit	ROUT, BOUT
	—	—	6	bit	GOUT
Linearity error	- 2.0	—	+ 2.0	LSB	When the output is unloaded
Differential linearity error	- 1.0	—	+ 1.0	LSB	When the output is unloaded
Analog output impedance	—	250	—	k $\Omega$	Analog output < 1.0 V
Analog current (R/G/BOUT)	4.5	5.2	5.8	mA	Full-scale*
	0	2	20	$\mu$ A	Zero-scale
Power supply current (VDDD)	—	25	27	mA	VREF = 1.1 V

\*: The calculating formula of analog current (R/G/BOUT) in full-scale is as follows.

$$R/G/BOUT = (V_{REF} / R_{REF}) \times 12.75$$

Typical value is defined in case of  $V_{REF} = 1.1\text{ V}$ ,  $R_{REF} = 2.7\text{ k}\Omega$ .

# MB91610 Series

## 7. USB Characteristics

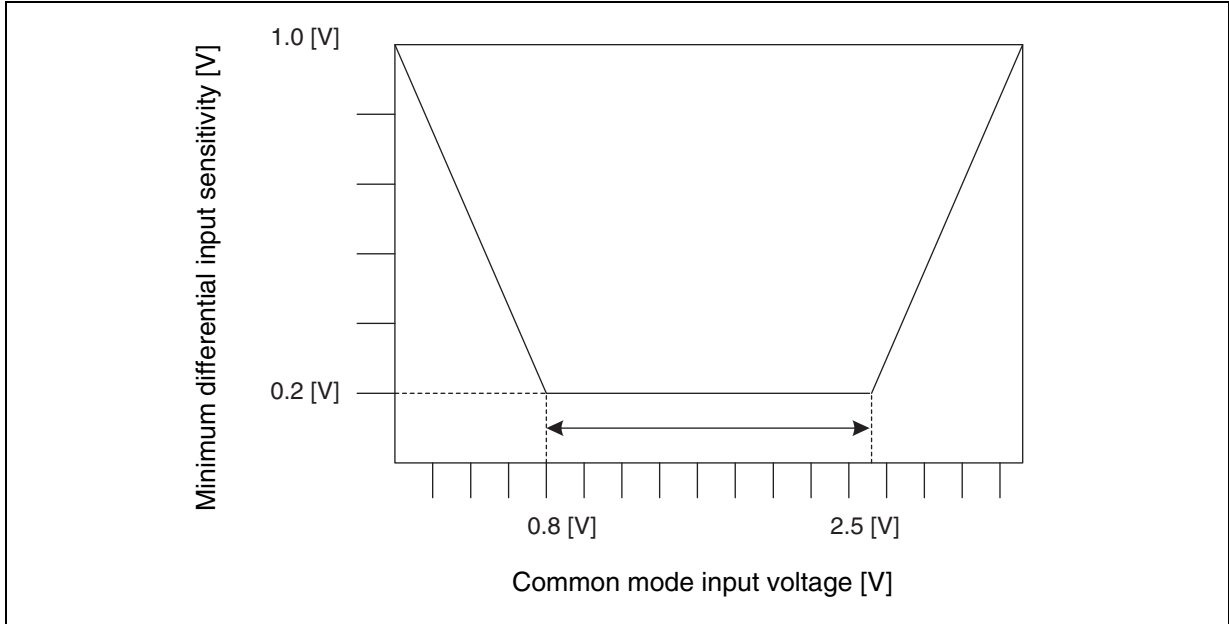
( $V_{CC} = AV_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

Parameter		Symbol	Pin name	Conditions	Value		Unit	Remarks
					Min	Max		
Input characteristics	Input High level voltage	$V_{IH}$	UDP, UDM	—	2.0	$V_{CC} + 0.3$	V	*1
	Input Low level voltage	$V_{IL}$		—	$V_{SS} - 0.3$	0.8	V	*1
	Differential input sensitivity	$V_{DI}$		—	0.2	—	V	*2
	Differential common mode input voltage	$V_{CM}$		—	0.8	2.5	V	*2
Output characteristics	Output High level voltage	$V_{OH}$		External pull-down resistance = 15 k $\Omega$	2.8	3.6	V	*3
	Output Low level voltage	$V_{OL}$		External pull-up resistance = 1.5 k $\Omega$	0.0	0.3	V	*3
	Crossover voltage	$V_{CRS}$		—	1.3	2.0	V	*4
	Rise time	$t_{FR}$		—	4	20	nS	*5
	Fall time	$t_{FF}$	—	4	20	nS	*5	
	Rise/fall time matching	$t_{RFM}$	—	90	111.11	%	*5	
	Output impedance	$Z_{DRV}$	—	28	44	$\Omega$	Including $R_s = 27\ \Omega$	
Input capacitance	Transceiver edge rate control capacitance	$C_{EDGE}$	—	—	75	pF	*6	
Series resistance		$R_s$	—	25	30	$\Omega$	Recommended value: 27 $\Omega$	

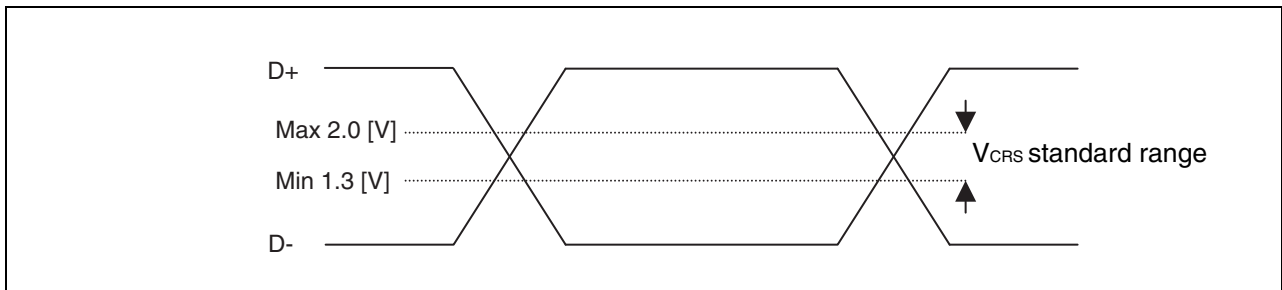
\*1 : The switching threshold voltage of Single-End-Receiver of USB I/O buffer is set as within  $V_{IL}$  (Max) = 0.8 [V],  $V_{IH}$  (Min) = 2.0 [V] (TTL input standard).  
There are some hystereses to lower noise sensitivity.

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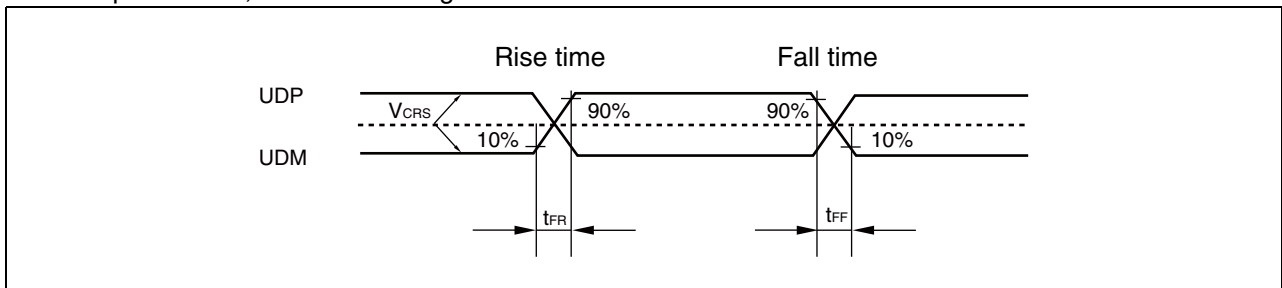
- \*2 : Use differential-Receiver to receive USB differential data signal.  
 Differential-Receiver has 200 [mV] of differential input sensitivity when the differential data input is within 0.8 [V] to 2.5 [V] to the local ground reference level.  
 Above voltage range is the common mode input voltage range.



- \*3 : The output drive capability of the driver is below 0.3 [V] at Low-State ( $V_{OL}$ ) (to 3.6 [V] and 1.5 k $\Omega$  load), and 2.8 [V] or above (to the  $V_{SS}$  and 15 k $\Omega$  load) at High-State ( $V_{OH}$ ).  
 \*4 : The cross voltage of the external differential output signal ( $D+ / D-$ ) of USB I/O buffer is within 1.3 [V] to 2.0 [V].



- \*5 : Regarding  $t_{FR}$ ,  $t_{FF}$ ,  $t_{RFM}$   
 They indicate rise time ( $T_{rise}$ ) and fall time ( $T_{fall}$ ) of the differential data signal.  
 They are defined by the time between 10% to 90% of the output signal voltage.  
 For full-speed buffer,  $t_{FR}/t_{FF}$  ratio is regulated as within  $\pm 10\%$  to minimize RFI emission.



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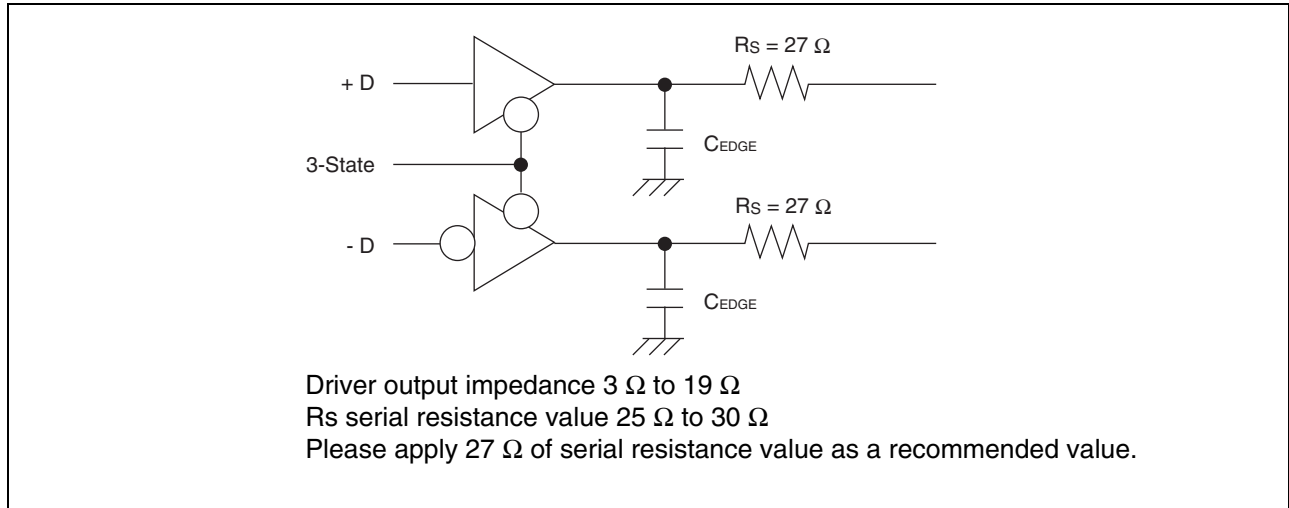
# MB91610 Series

(Continued)

\*6 : The place to connect transceiver edge rate control capacitance  $C_{EDGE}$

For this USB I/O, it is recommended to use  $C_{EDGE}$  control capacitor.

For USB Max standard as 75 pF, please control the edge characteristic of output waveform by connecting 30 [pF] to 50 [pF] (recommended value : 47 [pF]  $\pm$  50[pF]) to D + and D - lines when implementing on the board.



## 8. Flash Memory Write/Erase Characteristics

( $V_{CC} = 3.3\text{ V}$ ,  $T_a = +25\text{ °C}$ )

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	—	0.9	3.6	s	Excludes write time prior to internal erase
Half word (16bits) write time	—	23	370	μs	Not including system-level overhead time.
Chip erase time*1	—	10.8	43.2	s	Excludes write time prior to internal erase
Erase/write cycles	10000	—	—	cycle	Average $T_a \leq +85\text{ °C}$
Flash memory data hold time	$10^{*2}$	—	—	year	Average $T_a \leq +85\text{ °C}$

\*1 : The chip erase time is the sector erase time multiplied across all sectors.

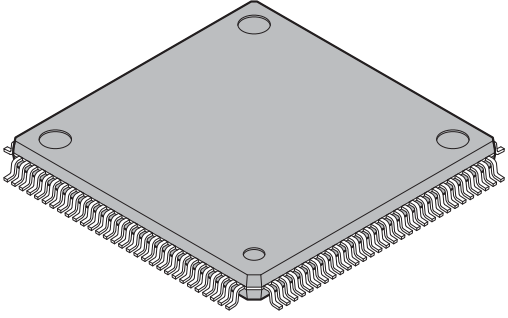
\*2 : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at  $+85\text{ °C}$ ).

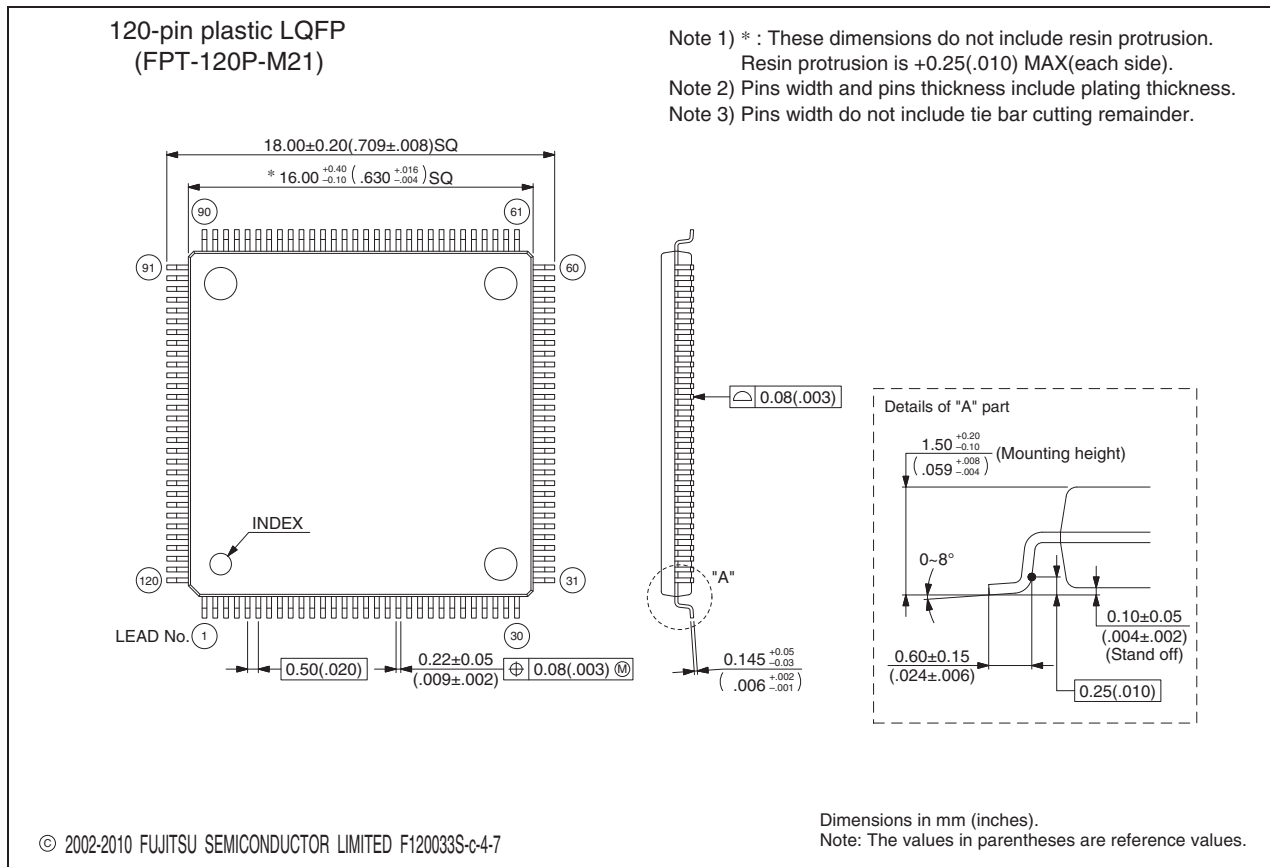
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## ■ ORDERING INFORMATION

Part number	Package
MB91F610APMC	120-pin plastic LQFP (FPT-120P-M21)
MB91613PMC	

## ■ PACKAGE DIMENSION

<p style="text-align: center;">120-pin plastic LQFP</p>  <p style="text-align: center;">(FPT-120P-M21)</p>	Lead pitch	0.50 mm
	Package width package length	16.0 16.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.88 g
	Code (Reference)	P-LFQFP120-16 16-0.50



Please check the latest package dimension at the following URL.  
<http://edevic.fujitsu.com/package/en-search/>

## ■ MAJOR CHANGES IN THIS EDITION

A change on a page is indicated by a vertical line drawn on the left side of that page.

Page	Section	Change Results
—	—	Changed the Company name. Fujitsu Microelectronics Limited → Fujitsu Semiconductor Limited
93	<b>■ ELECTRICAL CHARACTERISTICS</b> 6. Electrical Characteristics for the Analog RGB D/A Converter	Changed the parameter. “Analog current (R/B/GOUT)” → “Analog current (R/G/BOUT)” Added the following footnote. “*”: The calculating formula of analog current (R/G/BOUT) in full-scale is as follows. $R/G/BOUT = (V_{REF} / R_{REF}) \times 12.75$ Typical value is defined in case of $V_{REF} = 1.1 \text{ V}$ , $R_{REF} = 2.7 \text{ k}\Omega$ .”

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# MB91610 Series

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