FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-16903-4E

32-bit Microcontroller

CMOS

FR80 MB91605A Series

MB91605A

■ DESCRIPTION

The FR family* is a line of microcontrollers based on a 32-bit RISC CPU that contains a variety of built-in I/O resources for embedded control applications which require high-performance, high-speed CPU processing.

The MB91605A series of microcontrollers are based on the FR80 family and offer enhanced bus access that is optimal for embedded applications for controlling DVD players, printers, TVs, and PDPs.

* : FR, the abbreviation of FUJITSU RISC controller, is a line of products of Fujitsu Semiconductor Limited.

■ FEATURES

1. FR CPU

- 32-bit RISC load/store architecture with a five-stage pipeline
- Operating frequency 80 MHz (With PLL : 16 MHz base frequency × 5)
- 16-bit fixed length instructions (basic instructions), 1 instruction per cycle
- Instructions including memory-to-memory transfer, bit manipulation, barrel shift instructions : Instruction suitable for embedded applications
- Function entry/exit instructions and register data multi-read store instructions : Instructions supporting C language
- Register interlock function : Facilitates assembly-language coding

(Continued)

For the information for microcontroller supports, see the following web site.
This web site includes the **"Customer Design Review Supplement"** which provides the latest cautions on system development and the minimal requirements to be checked to prevent problems before the system development.

http://edevice.fujitsu.com/micom/en-support/

2010.4

- Built-in multiplier supported at the instruction level
  - Signed 32-bit multiplication : 5 cycles
  - Signed 16-bit multiplication : 3 cycles
- Interrupts (save PC and PS) : 6 cycles, 16 priority levels
- Harvard architecture enabling program access and data access to be executed simultaneously
- Instruction prefetch feature implemented using a 4-word queue in the CPU
- Instruction compatible with the FR family

2. Bus interface

- Operating frequency : Configurable from 1/1 to 1/4 of the on-chip frequency
- Basic bus cycle
  Read : 1 cycle
  Write : 3 cycles
- Supports multiplexed address/data bus
- Unused address pins can be used as general-purpose I/O ports
- Configurable as read-only (other than read-only areas, SDRAM areas)
- Automatic wait cycle generation function programmable for each area (Max 15 cycles)
- Areas configurable in the minimum unit of 1 Mbyte.
- Capable of chip select output for 8 completely independent areas

3. Built-in Memory

RAM : 128 Kbytes
Instruction cache : 8 Kbytes
Data cache : 8 Kbytes

4. DMAC (DMA Controller)

- 4 channels
- Two transfer sources : Internal peripheral/software
- Addressing mode : Specified as full 32-bit addresses (increment/decrement/fixed)
- Transfer modes : Burst transfer/block transfer
- Transfer data size : Selectable from 1, 2, 4, or 32 bytes

5. 16-bit Reload Timer (Including 1 Channel for REALOS)

- 3 channels
- Internal clock: Frequency division selectable from 2, 4, 8, 16, 32, and 64

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6. Multi-function Serial Interface

- 8 channels with 16-byte FIFO, 4 channels without FIFO
- Selectable from the following 3 operation modes by channels

  < UART >
  - Full duplex double buffer
  - Parity on/off selectable
  - Built-in dedicated baud rate generator
  - External clock can be used as a serial clock
  - Error detection function for parity, frame and overrun errors

  < CSIO >
  - Transfer mode : Clock synchronous (Max 10 Mbps)
  - Full-duplex double buffer
  - Built-in dedicated baud rate generator
  - Error detection function for overrun error

  < I^2C >

  Supports both typical mode (Max 100 kbps) and high-speed mode (Max 400 kbps)

7. Interrupt Controller

- External interrupt lines: Total of 25 lines (external interrupt pins : 24 pins + $\overline{NMI}$ pin : 1 pin)
- Interrupts from internal peripherals
- Can be set priority levels as programmable (16 levels) for all pins other than $\overline{NMI}$ pin
- Can be used to wakeup from STOP mode

8. A/D Converter

- 12 channels
- 10-bit resolution
- Successive approximation type : Conversion time : About 8.1 µs
- Conversion mode : Single-shot conversion mode, scan conversion mode
- Activation sources : Software/external trigger

9. Base Timer

- 12 channels
- Operation mode is selectable from the followings by a channel
  - 16/32-bit reload timer (32-bit timer is used in 2 channels.)
  - 16-bit PWM timer
  - 16/32-bit PWC timer (32-bit timer is used in 2 channels.)
  - 16-bit PPG timer
- 4-channel synchronized start mode

10. HDMI-CEC/Remote Control Reception

- 1 channel
- HDMI-CEC receiver function (with automatic ACK response function)
- Remote control reception function (built-in 4-byte receive buffer)

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11. Other Interval Timers

Watchdog timer : built-in 1 channel

12. I/O Ports

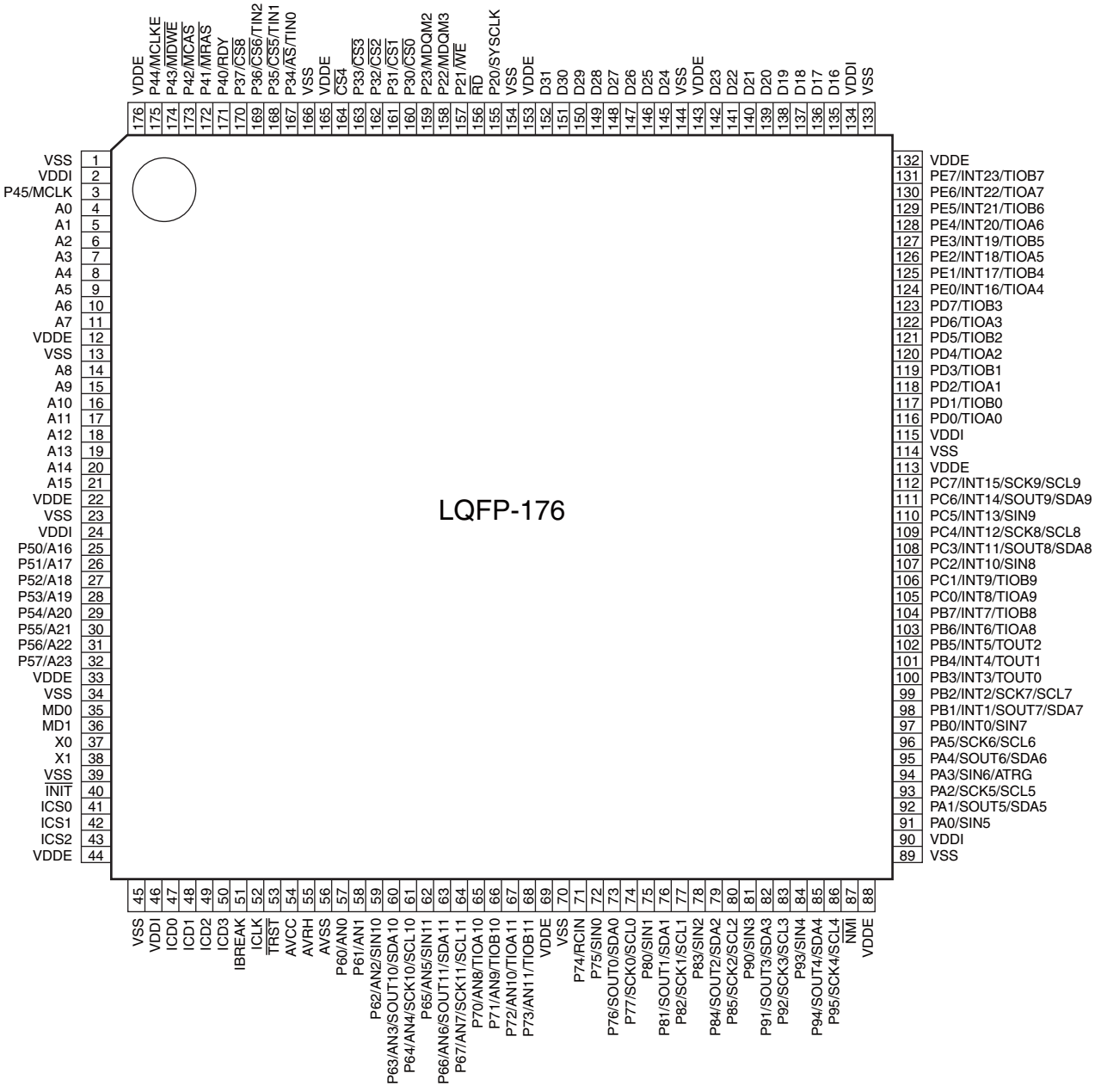
Max 92 ports

13. Other Features

- Internal oscillator circuit as a clock source
- $\overline{\text{INIT}}$ provided as a reset pin
- Watchdog timer reset and software reset are available
- Stop and sleep modes supported as low-power consumption modes
- Gear function
  - Built-in time-base timer
- Package LQFP-176, 0.50 mm pitch, 24.0 mm × 24.0 mm
- Power supply voltage 3.3 V ± 0.3 V, 1.8 V ± 0.15 V dual power supply

■ PIN ASSIGNMENT

(TOP VIEW)



(FPT-176P-M07)

■ PIN DESCRIPTION

Pin no.	Pin name	I/O circuit type*	Description
3	P45	A	General-purpose I/O port
	MCLK		Clock output pin for external bus interface
4 to 11	A0 to A7	B	Address bus output pins for external bus interface (bit0 to bit7)
14 to 21	A8 to A15	B	Address bus output pins for external bus interface (bit8 to bit15)
25 to 32	P50 to P57	A	General-purpose I/O ports
	A16 to A23		Address bus output pins for external bus interface (bit16 to bit23)
35, 36	MD0, MD1	C	Mode setting pins
37	X0	D	Clock (oscillator) input pin
38	X1	D	Clock (oscillator) I/O pin
40	$\overline{\text{INIT}}$	E	External reset input pin
41 to 43	ICS0 to ICS2	B	Development tool status output pins
47 to 50	ICD0 to ICD3	F	Development tool data I/O pins
51	IBREAK	G	Development tool break input pin
52	ICLK	B	Development tool clock output pin
53	$\overline{\text{TRST}}$	E	Development tool reset input pin
57	P60	H	General-purpose I/O port
	AN0		A/D converter ch.0 analog input pin
58	P61	H	General-purpose I/O port
	AN1		A/D converter ch.1 analog input pin
59	P62	H	General-purpose I/O port
	AN2		A/D converter ch.2 analog input pin
	SIN10		Multi-function serial interface ch.10 serial data input pin
60	P63	H	General-purpose I/O port
	AN3		A/D converter ch.3 analog input pin
	SOUT10		Multi-function serial interface ch.10 serial data output pin
	SDA10		Multi-function serial interface ch.10 I^2C data I/O pin
61	P64	H	General-purpose I/O port
	AN4		A/D converter ch.4 analog input pin
	SCK10		Multi-function serial interface ch.10 serial clock I/O pin
	SCL10		Multi-function serial interface ch.10 I^2C clock I/O pin
62	P65	H	General-purpose I/O port
	AN5		A/D converter ch.5 analog input pin
	SIN11		Multi-function serial interface ch.11 serial data input pin

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Pin no.	Pin name	I/O circuit type*	Description
63	P66	H	General-purpose I/O port
	AN6		A/D converter ch.6 analog input pin
	SOUT11		Multi-function serial interface ch.11 serial data output pin
	SDA11		Multi-function serial interface ch.11 I²C data I/O pin
64	P67	H	General-purpose I/O port
	AN7		A/D converter ch.7 analog input pin
	SCK11		Multi-function serial interface ch.11 serial clock I/O pin
	SCL11		Multi-function serial interface ch.11 I²C clock I/O pin
65	P70	H	General-purpose I/O port
	AN8		A/D converter ch.8 analog input pin
	TIOA10		Base timer ch.10 timer I/O pin
66	P71	H	General-purpose I/O port
	AN9		A/D converter ch.9 analog input pin
	TIOB10		Base timer ch.10 timer input pin
67	P72	H	General-purpose I/O port
	AN10		A/D converter ch.10 analog input pin
	TIOA11		Base timer ch.11 timer I/O pin
68	P73	H	General-purpose I/O port
	AN11		A/D converter ch.11 analog input pin
	TIOB11		Base timer ch.11 timer input pin
71	P74	A	General-purpose I/O port
	RCIN		HDMI-CEC/Remote control I/O pin
72	P75	A	General-purpose I/O port
	SIN0		Multi-function serial interface ch.0 serial data input pin
73	P76	A	General-purpose I/O port
	SOUT0		Multi-function serial interface ch.0 serial data output pin
	SDA0		Multi-function serial interface ch.0 I²C data I/O pin
74	P77	A	General-purpose I/O port
	SCK0		Multi-function serial interface ch.0 serial clock I/O pin
	SCL0		Multi-function serial interface ch.0 I²C clock I/O pin
75	P80	A	General-purpose I/O port
	SIN1		Multi-function serial interface ch.1 serial data input pin

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Pin no.	Pin name	I/O circuit type*	Description
76	P81	A	General-purpose I/O port
	SOUT1		Multi-function serial interface ch.1 serial data output pin
	SDA1		Multi-function serial interface ch.1 I²C data I/O pin
77	P82	A	General-purpose I/O port
	SCK1		Multi-function serial interface ch.1 serial clock I/O pin
	SCL1		Multi-function serial interface ch.1 I²C clock I/O pin
78	P83	A	General-purpose I/O port
	SIN2		Multi-function serial interface ch.2 serial data input pin
79	P84	A	General-purpose I/O port
	SOUT2		Multi-function serial interface ch.2 serial data output pin
	SDA2		Multi-function serial interface ch.2 I²C data I/O pin
80	P85	A	General-purpose I/O port
	SCK2		Multi-function serial interface ch.2 serial clock I/O pin
	SCL2		Multi-function serial interface ch.2 I²C clock I/O pin
81	P90	A	General-purpose I/O port
	SIN3		Multi-function serial interface ch.3 serial data input pin
82	P91	A	General-purpose I/O port
	SOUT3		Multi-function serial interface ch.3 serial data output pin
	SDA3		Multi-function serial interface ch.3 I²C data I/O pin
83	P92	A	General-purpose I/O port
	SCK3		Multi-function serial interface ch.3 serial clock I/O pin
	SCL3		Multi-function serial interface ch.3 I²C clock I/O pin
84	P93	A	General-purpose I/O port
	SIN4		Multi-function serial interface ch.4 serial data input pin
85	P94	A	General-purpose I/O port
	SOUT4		Multi-function serial interface ch.4 serial data output pin
	SDA4		Multi-function serial interface ch.4 I²C data I/O pin
86	P95	A	General-purpose I/O port
	SCK4		Multi-function serial interface ch.4 serial clock I/O pin
	SCL4		Multi-function serial interface ch.4 I²C clock I/O pin
87	$\overline{\text{NMI}}$	E	NMI input pin

(Continued)

Pin no.	Pin name	I/O circuit type*	Description
91	PA0	A	General-purpose I/O port
	SIN5		Multi-function serial interface ch.5 serial data input pin
92	PA1	A	General-purpose I/O port
	SOUT5		Multi-function serial interface ch.5 serial data output pin
	SDA5		Multi-function serial interface ch.5 I²C data I/O pin
93	PA2	A	General-purpose I/O port
	SCK5		Multi-function serial interface ch.5 serial clock I/O pin
	SCL5		Multi-function serial interface ch.5 I²C clock I/O pin
94	PA3	A	General-purpose I/O port
	SIN6		Multi-function serial interface ch.6 serial data input pin
	ATRG		A/D converter external trigger input pin
95	PA4	A	General-purpose I/O port
	SOUT6		Multi-function serial interface ch.6 serial data output pin
	SDA6		Multi-function serial interface ch.6 I²C data I/O pin
96	PA5	A	General-purpose I/O port
	SCK6		Multi-function serial interface ch.6 serial clock I/O pin
	SCL6		Multi-function serial interface ch.6 I²C clock I/O pin
97	PB0	I	General-purpose I/O port
	INT0		External interrupt input pin
	SIN7		Multi-function serial interface ch.7 serial data input pin
98	PB1	I	General-purpose I/O port
	INT1		External interrupt input pin
	SOUT7		Multi-function serial interface ch.7 serial data output pin
	SDA7		Multi-function serial interface ch.7 I²C data I/O pin
99	PB2	I	General-purpose I/O port
	INT2		External interrupt input pin
	SCK7		Multi-function serial interface ch.7 serial clock I/O pin
	SCL7		Multi-function serial interface ch.7 I²C clock I/O pin
100 to 102	PB3 to PB5	I	General-purpose I/O ports
	INT3 to INT5		External interrupt input pins
	TOUT0 to TOUT2		16-bit reload timer ch.0 to ch.2 output pins

(Continued)

Pin no.	Pin name	I/O circuit type*	Description
103	PB6	I	General-purpose I/O port
	INT6		External interrupt input pin
	TIOA8		Base timer ch.8 timer output pin
104	PB7	I	General-purpose I/O port
	INT7		External interrupt input pin
	TIOB8		Base timer ch.8 timer input pin
105	PC0	I	General-purpose I/O port
	INT8		External interrupt input pin
	TIOA9		Base timer ch.9 timer I/O pin
106	PC1	I	General-purpose I/O port
	INT9		External interrupt input pin
	TIOB9		Base timer ch.9 timer input pin
107	PC2	I	General-purpose I/O port
	INT10		External interrupt input pin
	SIN8		Multi-function serial interface ch.8 serial data input pin
108	PC3	I	General-purpose I/O port
	INT11		External interrupt input pin
	SOUT8		Multi-function serial interface ch.8 serial data output pin
	SDA8		Multi-function serial interface ch.8 I^2C data I/O pin
109	PC4	I	General-purpose I/O port
	INT12		External interrupt input pin
	SCK8		Multi-function serial interface ch.8 serial clock I/O pin
	SCL8		Multi-function serial interface ch.8 I^2C clock I/O pin
110	PC5	I	General-purpose I/O port
	INT13		External interrupt input pin
	SIN9		Multi-function serial interface ch.9 serial data input pin
111	PC6	I	General-purpose I/O port
	INT14		External interrupt input pin
	SOUT9		Multi-function serial interface ch.9 serial data output pin
	SDA9		Multi-function serial interface ch.9 I^2C data I/O pin

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Pin no.	Pin name	I/O circuit type*	Description
112	PC7	I	General-purpose I/O port
	INT15		External interrupt input pin
	SCK9		Multi-function serial interface ch.9 serial clock I/O pin
	SCL9		Multi-function serial interface ch.9 I^2C clock I/O pin
116	PD0	A	General-purpose I/O port
	TIOA0		Base timer ch.0 timer output pin
117	PD1	A	General-purpose I/O port
	TIOB0		Base timer ch.0 timer input pin
118	PD2	A	General-purpose I/O port
	TIOA1		Base timer ch.1 timer I/O pin
119	PD3	A	General-purpose I/O port
	TIOB1		Base timer ch.1 timer input pin
120	PD4	A	General-purpose I/O port
	TIOA2		Base timer ch.2 timer output pin
121	PD5	A	General-purpose I/O port
	TIOB2		Base timer ch.2 timer input pin
122	PD6	A	General-purpose I/O port
	TIOA3		Base timer ch.3 timer I/O pin
123	PD7	A	General-purpose I/O port
	TIOB3		Base timer ch.3 timer input pin
124	PE0	I	General-purpose I/O port
	INT16		External interrupt input pin
	TIOA4		Base timer ch.4 timer output pin
125	PE1	I	General-purpose I/O port
	INT17		External interrupt input pin
	TIOB4		Base timer ch.4 timer input pin
126	PE2	I	General-purpose I/O port
	INT18		External interrupt input pin
	TIOA5		Base timer ch.5 timer I/O pin
127	PE3	I	General-purpose I/O port
	INT19		External interrupt input pin
	TIOB5		Base timer ch.5 timer input pin

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Pin no.	Pin name	I/O circuit type*	Description
128	PE4	I	General-purpose I/O port
	INT20		External interrupt input pin
	TIOA6		Base timer ch.6 timer output pin
129	PE5	I	General-purpose I/O port
	INT21		External interrupt input pin
	TIOB6		Base timer ch.6 timer input pin
130	PE6	I	General-purpose I/O port
	INT22		External interrupt input pin
	TIOA7		Base timer ch.7 timer I/O pin
131	PE7	I	General-purpose I/O port
	INT23		External interrupt input pin
	TIOB7		Base timer ch.7 timer input pin
135 to 142	D16 to D23	J	Data bus I/O pins for external bus interface (bit16 to bit23)
145 to 152	D24 to D31	J	Data bus I/O pins for external bus interface (bit24 to bit31)
155	P20	A	General-purpose I/O port
	SYSCLK		System clock output pin
156	$\overline{RD}$	B	External bus interface read strobe output pin
157	P21	A	General-purpose I/O port
	$\overline{WE}$		External bus interface write strobe output pin
158, 159	P22, P23	A	General-purpose I/O ports
	MDQM3, MDQM2		External bus interface byte enable output pins MDQM3:D[31:24], MDQM2:D[23:16]
160 to 163	P30 to P33	A	General-purpose I/O ports
	$\overline{CS0}$ to $\overline{CS3}$		External bus interface chip select output pins
164	$\overline{CS4}$	B	External bus interface chip select output pin
167	P34	A	General-purpose I/O port
	$\overline{AS}$		External bus interface address strobe output pin
	TIN0		16-bit reload timer ch.0 input pin
168, 169	P35, P36	A	General-purpose I/O ports
	$\overline{CS5}$, $\overline{CS6}$		External bus interface chip select output pins
	TIN1, TIN2		16-bit reload timer ch.1, ch.2 input pins
170	P37	A	General-purpose I/O port
	$\overline{CS8}$		SDRAM interface chip select output pin

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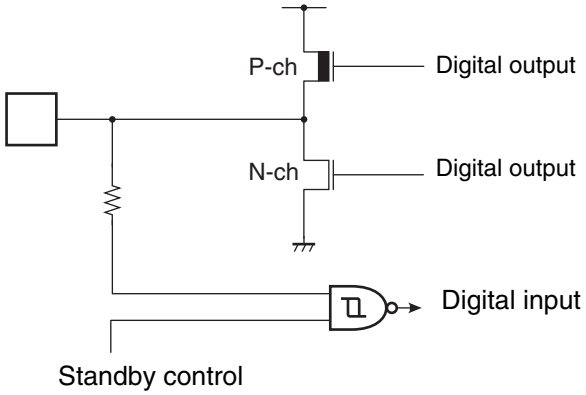
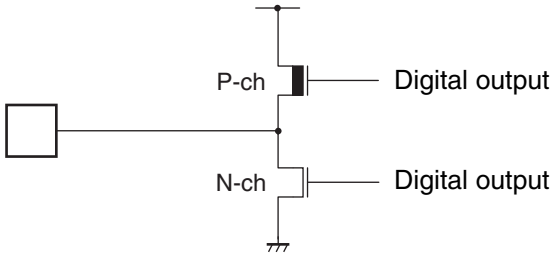
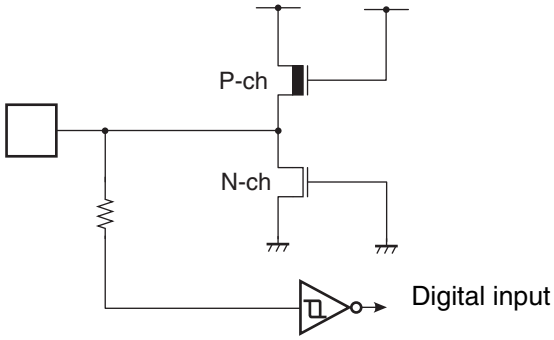
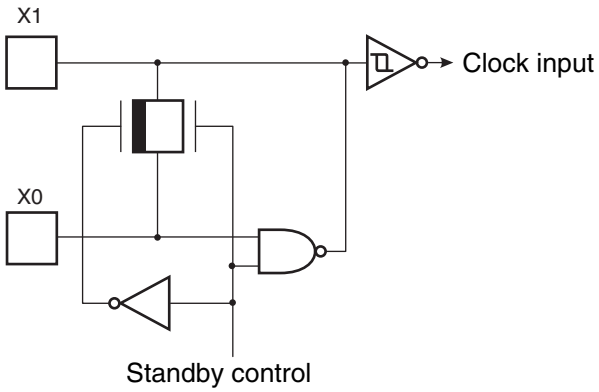
Pin no.	Pin name	I/O circuit type*	Description
171	P40	A	General-purpose I/O port
	RDY		External bus interface ready input pin
172	P41	A	General-purpose I/O port
	$\overline{\text{MRAS}}$		RAS strobe output pin for SDRAM interface
173	P42	A	General-purpose I/O port
	$\overline{\text{MCAS}}$		CAS strobe output pin for SDRAM interface
174	P43	A	General-purpose I/O port
	$\overline{\text{MDWE}}$		Write strobe output pin for SDRAM interface
175	P44	A	General-purpose I/O port
	MCLKE		Clock enable output pin for SDRAM interface

* : Refer to “■ I/O CIRCUIT TYPE” for details on the I/O circuit types.

[Power supply/GND pins]

Pin no.	Pin name	I/O circuit type	Description
12, 22, 33, 44, 69, 88, 113, 132, 143, 153, 165, 176	VDDE	—	3.3 V power supply pins
2, 24, 46, 90, 115, 134	VDDI	—	1.8 V power supply pins
1, 13, 23, 34, 39, 45, 70, 89, 114, 133, 144, 154, 166	VSS	—	GND pins
54	AVCC	—	A/D converter power supply pin
56	AVSS	—	A/D converter analog GND pin
55	AVRH	—	A/D converter reference voltage pin

■ I/O CIRCUIT TYPE

Type	Circuit type	Remarks
A		• CMOS level output • CMOS level hysteresis input With standby control
B		CMOS level output
C		CMOS level hysteresis input
D		Oscillation feedback resistor : approx. 1 MΩ (built-in)

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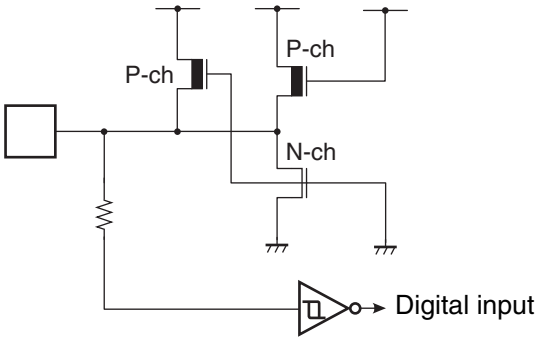
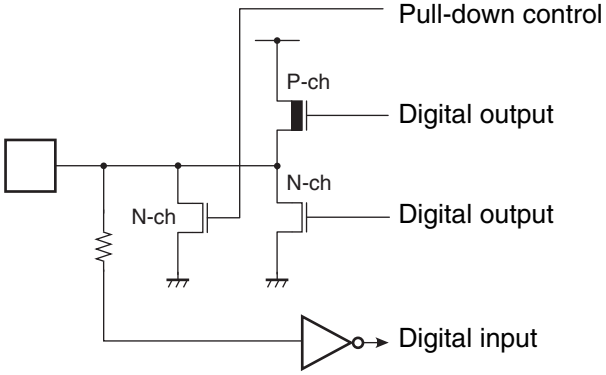
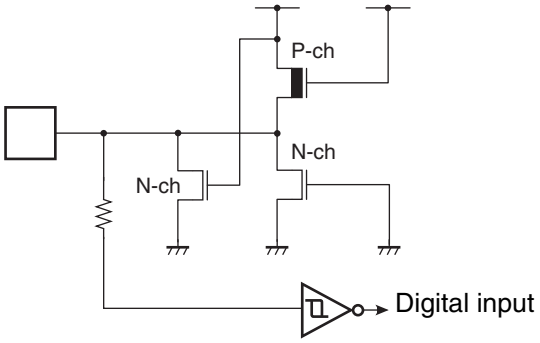
Type	Circuit type	Remarks
E		• With pull-up resistor CMOS hysteresis input Pull-up resistor value = approx. 33 kΩ (Typ)
F		• CMOS input/output • With pull-down control
G		• CMOS hysteresis input With pull-down resistor

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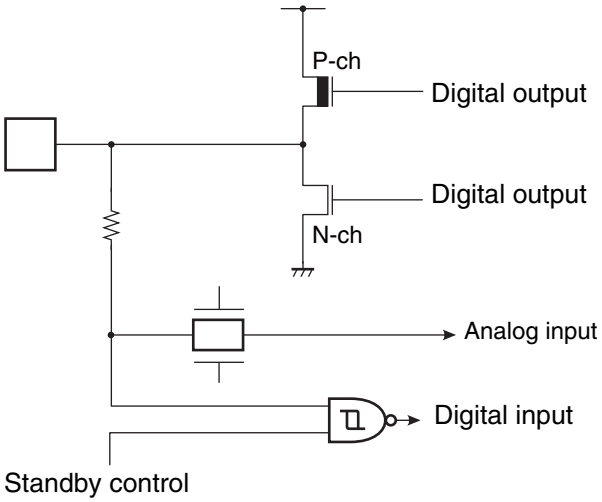
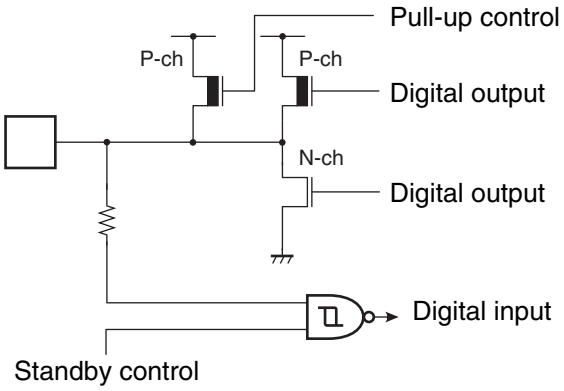
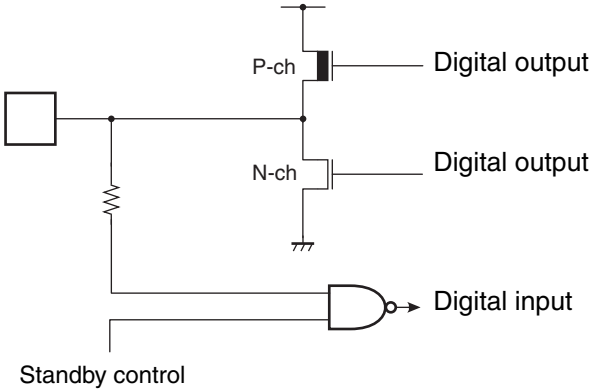
Type	Circuit type	Remarks
H		• CMOS level output • CMOS level hysteresis input With standby control • With analog input
I		• With pull-up control • Pull-up resistor value = approx. 33 kΩ (Typ) • CMOS level output • CMOS level hysteresis input • With standby control
J		• CMOS level input/output • With standby control

■ HANDLING DEVICES

• Preventing latch-up

Latch-up may occur in a CMOS IC if a voltage higher than V_{DDE} or V_{DDI}, or less than V_{SS} is applied to an input or output pin or if a voltage exceeding the rated value is applied between VDDE and VSS, or VDDI and VSS. If latch-up occurs, the power supply current increases rapidly, sometimes resulting in thermal breakdown of the device. Therefore, be very careful not to apply voltages in excess of the absolute maximum ratings.

• Handling of unused pins

Leaving unused input pins unconnected can cause misoperation or permanent damage to the device due to latchup. Always pull-up or pull-down unused pins using a 2 kΩ or larger resistor.
If some I/O pins are unused, either set as outputs and leave open circuit or set as inputs and treat in the same way as input pins.

• Power supply pins

The MB91605A series has multiple VDDE, VDDI, and VSS pins. respective pins at the same potential are interconnected in order to prevent latch-up and other malfunctions. However, you must connect the pins externally to the power supply and ground lines to reduce the electro-magnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating. Furthermore, the VDDE pins, VDDI pins and VSS pins of the MB91605A series must be connected to the current supply source at a low impedance.
It is also recommended to connect a ceramic capacitor of approximately 0.1 μF as a bypass capacitor between the VDDE, VDDI and VSS pins near the device.

• Crystal oscillator circuit

Noise in proximity to the X0 and X1 pins can cause the device to malfunction. Printed circuit boards should be designed so that the X0 and X1 pins, crystal oscillator, and bypass capacitors connected to ground are located near the device and ground.

It is recommended that the printed circuit board artwork be designed such that the X0 and X1 pins are surrounded by ground plane for the stable operation.

Please request the oscillator manufacturer to evaluate the oscillational characteristics of the crystal and this device.

• Mode pins (MD0, MD1)

Connect them directly to power supply pins or GND pins. To prevent the device from entering test mode accidentally due to noise, minimize the lengths of the patterns between each mode pin and power supply pin or GND pin on the printed circuit board as much as possible and connect them at a low impedance.

• Operation at power-on

Ensure that a settings initialization reset (INIT) is performed using the $\overline{\text{INIT}}$ pin immediately after the power is turned on.
Maintain the “L” level input to the $\overline{\text{INIT}}$ pin for the duration of the stabilization wait time immediately after the power on to ensure the stabilization wait time as required by the oscillator circuit (the stabilization wait time is reset to the minimum value when INIT is asserted using the $\overline{\text{INIT}}$ pin).

• Note on oscillator input at power-on

At power-on, ensure that the clock is input until the oscillator stabilization wait time has elapsed.

- Notes on the turning on and off the power to the VDDI pin (1.8 V internal power supply) and VDDE pin (3.3 V external pin power supply).
  Turn on/off the power in the following procedure.

Power on	VDDI pin (internal power supply) → VDDE pin (external power supply) → Analog→ Signal
Power off	Signal → Analog→ VDDE pin (external power supply) → VDDI pin (internal power supply)

  Do not continuously (more than one minute) apply power to the VDDE pin (external power supply) while the VDDI pin (internal power supply) is disconnected as this will adversely affect the reliability of the LSI.

  When the VDDE pin (external power supply) returns from the off state to the on state, the internal state of the circuit might not be able to be maintained due to power supply noise and other effects.

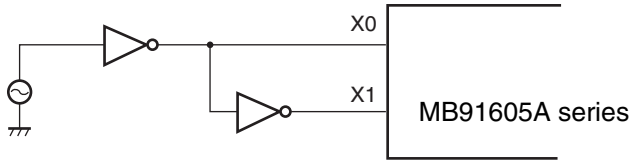
  When the power is turned on, the states of the output pins may remain undefined until the internal power supply becomes stable.

  There is no problem for turning on and off the power (VDDI/VDDE/analog) simultaneously.

- Notes on using an external clock

  When using an external clock, in principal, the clock signal should be supplied simultaneously to the X0 and X1 pins, with the phase-inverted clock signal of X0 supplied to the X1 pin. However, the external clock must not be used while the microcontroller is in stop mode (oscillator stop mode). (This is because the X1 pin stops at “H” output in STOP mode.)

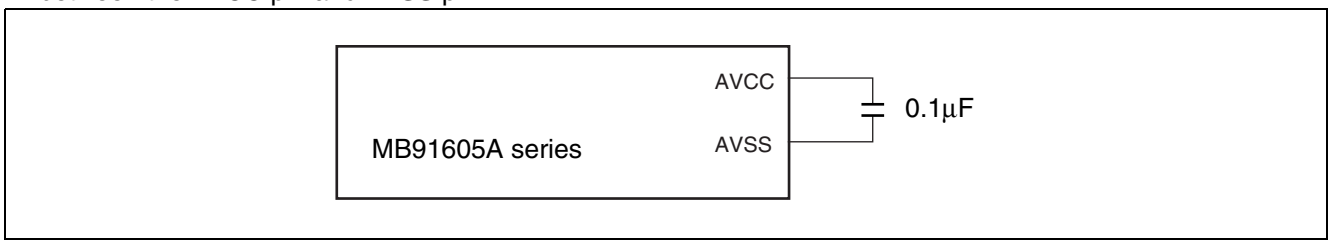
Using an External Clock



Cannot be used in STOP mode (oscillation stop mode).

• AVCC pin

The MB91605A series has a built-in A/D converter. A capacitor of approximately 0.1μF must be connected between the AVCC pin and AVSS pin.



• Notes when not using the emulator

To operate the evaluation MCU on the user system without connecting the emulator, each of the input pins on the evaluation MCU connected to the emulator interface on the user system as shown below.

Note that switching circuits or other measures may be needed on the user system.

Emulator Interface Pin Treatment

Evaluation MCU Pin Name	Pin Connection
$\overline{\text{TRST}}$	Connect to the reset output circuit on the user system.
$\overline{\text{INIT}}$	Connect to the reset output circuit on the user system.
Other Pins	Open

• Precautions when the PLL clock is selected

If the crystal oscillator is disconnected or the clock input stops while the PLL clock is selected, the microcontroller may continue to operate at the free-running frequency of the self-oscillator within the PLL. However, this operation is not guaranteed.

■ RESTRICTIONS

1) Notes on the PS register

Some instructions write to the PS register in advance before executing. When a debugger is being used, execution may break within an interrupt handler routine, or the values of the flags within the PS register may be updated due to exception processing. However, the microcontroller is designed to reprocess correctly after returning from the EIT, and to execute before and after the EIT proceeds according to the specifications.

- If any of the following situations occur in the instruction immediately before a DIV0U or DIV0S instruction, the processing in (1) to (3) will be performed.

  - A user interrupt or NMI is accepted
  - Step execution is performed
  - A break occurs due to a data event or by being selected from the emulator menu

  (1) The D0 and D1 flags are updated in advance.

  (2) The EIT handling routine (user interrupt/NMI or emulator) is executed.

  (3) Upon returning from the EIT, the DIV0U or DIV0S instruction is executed and the D0/D1 flags are updated back to the same value as in step (1).

- If any of the OR CCR, ST ILM, or MOV Ri, PS instructions are executed to enable a user interrupt or NMI interrupt source when that interrupt has occurred, the following operation will be performed.

  (1) The PS register is updated in advance.

  (2) The EIT handling routine (user interrupt/NMI or emulator) is executed.

  (3) Upon returning from the EIT, the above instructions are executed and the PS registers are updated back to the same value as in step (1).

2) Watchdog timer

The watchdog timer is a function that monitors the program to check that it delays a reset within a certain period of time, and resets the CPU if the program runs out of control and fails to delay the reset. Once the watchdog timer has been enabled, it keeps running until reset. As an exception, the reset is automatically delayed in conditions where the execution of the CPU program stops. It is possible that the watchdog timer will not be triggered if these conditions arise as a result of the system running out of control. In that case, please reset (INIT) using the external $\overline{\text{INIT}}$ pin.

3) Notes on debugger

- Step execution of RETI instruction
  If stepped execution is used in an environment where interrupts occur frequently, the interrupt processing routines corresponding to those interrupts are executed repeatedly, and the programs for the main routine and low-level interrupt routines are not able to execute as a result. (For example, if a reload timer is enabled, execution will always break at the beginning of the reload timer interrupt routine when the RETI instruction is step-executed.) Disable the corresponding interrupts when the interrupt processing routines no longer need to be debugged.

- Break function

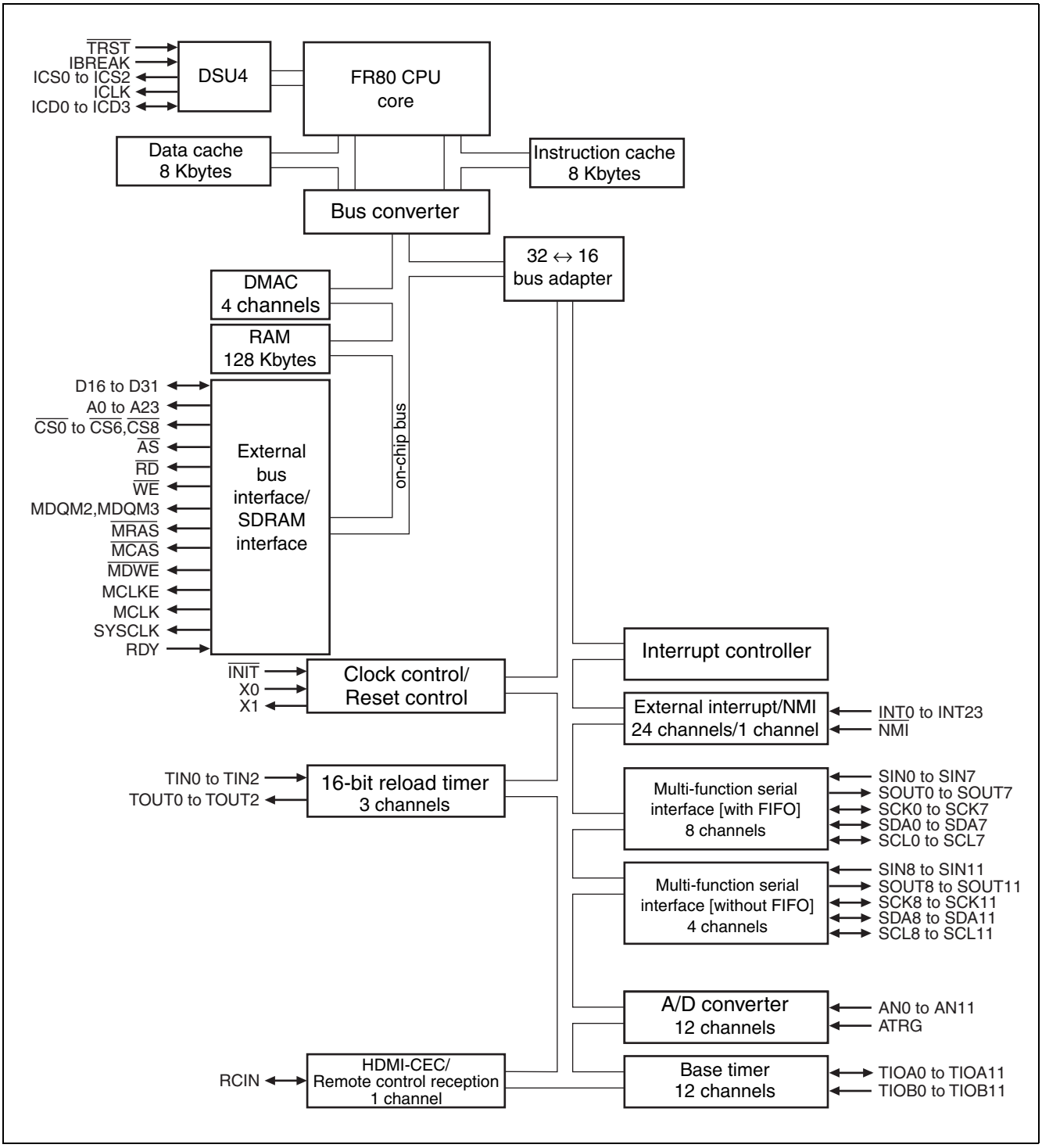
  If the target address of a hardware break (including event breaks) is set to the address of the current system stack pointer or to an area that contains the stack pointer, execution will break after each instruction regardless of whether the user program actually contains data access instructions.

  To prevent this, do not set (word) access to the area containing the address of the system stack pointer as the target of a hardware break (including an event break).

- Operand break

  Malfunctions may occur if the stack pointer is within an area which is set as the DSU operand break. Do not set the access to the areas containing the address of system stack pointer as a target of data event break.

■ BLOCK DIAGRAM



■ MEMORY SPACE

1. Memory space

The FR family has 4 Gbytes of logical address space (2^{32} addresses) linearly accessible to the CPU.

Direct Addressing Areas

The following areas in the address space are used as I/O areas.

These areas are called direct addressing areas. The addresses of operands in these areas can be specified directly within some instructions.

The direct addressing area varies depending on the size of data to be accessed as follows :

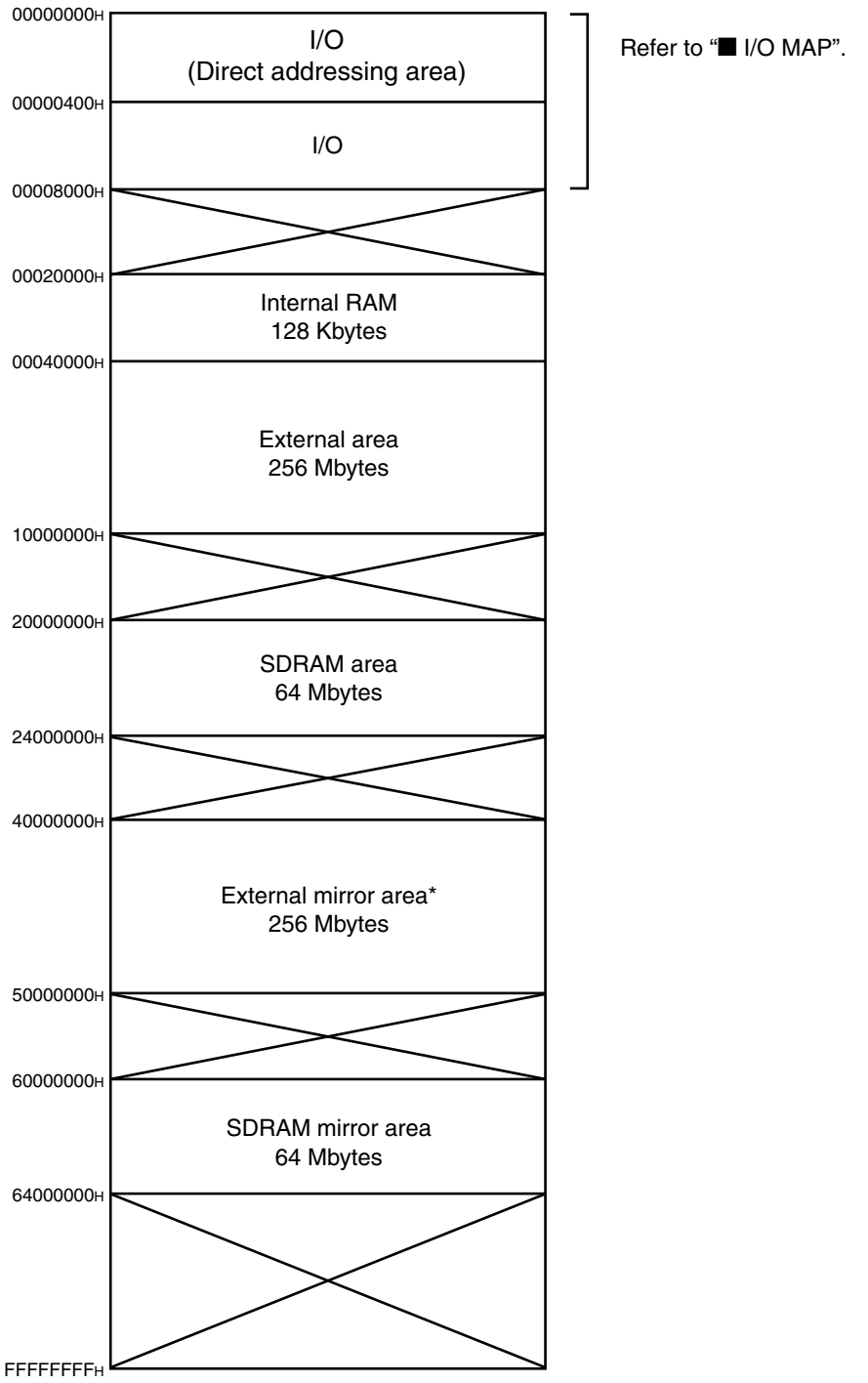
→ Byte data access : 000_H to $0FF_H$

→ Half word data access : 000_H to $1FF_H$

→ Word data access : 000_H to $3FF_H$

2. Memory Map

MB91605A
External ROM external bus mode



* : The mirror of external bus interface register can be found at 40002000H to 40002FFFH .

■ I/O MAP

The following table shows the correspondence between the memory space area and each of the peripheral resource registers.

[How to read the table]

Address	Register				Block
	+0	+1	+2	+3	
000000H	PDR0 [R/W] XXXXXXXX	PDR1 [R/W] XXXXXXXX	PDR2 [R/W] XXXXXXXX	PDR3 [R/W] XXXXXXXX	T-unit Port data register

Read/Write attribute

Initial value after a reset

Register name (First-column register at address 4n; second-column register at address 4n + 1)

Location of left-most register (When using word access, the register in column 1 is in the MSB side of the data.)

Notes: • The bit values in the register represent the following initial values :
- "1" : Initial value "1"
- "0" : Initial value "0"
- "X" : Initial value "Undefined"
- "-" : No physical register at this location
- "*" : Uninitialized bit

• Read/write attribute is as follows.
- "R" : Indicates that there is a read only bit.
- "R/W" : Indicates that there is a read/write bit.
- "W" : Indicates that there is a write only bit.

• Access is prohibited for data access attributes that are not listed.

Address	Register				Block
	+0	+1	+2	+3	
000000H	Reserved		PDR2 [R/W] ----XXXX	PDR3 [R/W] XXXXXXXX	Port data register
000004H	PDR4 [R/W] --XXXXXX	PDR5 [R/W] XXXXXXXX	PDR6 [R/W] XXXXXXXX	PDR7[R/W] XXXXXXXX	
000008H	PDR8 [R/W] --XXXXXX	PDR9 [R/W] --XXXXXX	PDRA [R/W] --XXXXXX	PDRB[R/W] XXXXXXXX	
00000CH	PDRC [R/W] XXXXXXXX	PDRD [R/W] XXXXXXXX	PDRE [R/W] XXXXXXXX	Reserved	
000010H to 00001CH	Reserved				
000020H	ADCTH [R/W] 00000000	ADCTL [R/W] 00000000	ADCH [R/W] 00000000 00000000		10-bit A/D converter
000024H	ADAT0 [R] 00000000 00000000		ADAT1 [R] 00000000 00000000		
000028H	ADAT2 [R] 00000000 00000000		ADAT3 [R] 00000000 00000000		
00002CH	ADAT4 [R] 00000000 00000000		ADAT5 [R] 00000000 00000000		
000030H	ADAT6 [R] 00000000 00000000		ADAT7 [R] 00000000 00000000		
000034H	ADAT8 [R] 00000000 00000000		ADAT9 [R] 00000000 00000000		
000038H	ADAT10 [R] 00000000 00000000		ADAT11 [R] 00000000 00000000		
00003CH	WDTCR0 [R/W] 00000000	WDTCPR0 [R/W] 00000000	Reserved		Watchdog timer
000040H	EIRR0 [R/W] 00000000	ENIR0 [R/W] 00000000	ELVR0 [R/W] 00000000 00000000		External interrupt 0 to 7
000044H	DICR [R/W] 11111110	Reserved			Delay interrupt
000048H	TMRLRA0 [R/W] XXXXXXXX XXXXXXXX		TMR0 [R] XXXXXXXX XXXXXXXX		16-bit reload timer ch.0
00004CH	Reserved		TMCSR0 [R/W] 00000000 XX000000		
000050H	TMRLRA1 [R/W] XXXXXXXX XXXXXXXX		TMR1 [R] XXXXXXXX XXXXXXXX		16-bit reload timer ch.1
000054H	Reserved		TMCSR1 [R/W] 00000000 XX000000		

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000058H	TMRLRA2 [R/W] XXXXXXXX XXXXXXXX		TMR2 [R] XXXXXXXX XXXXXXXX		16-bit reload timer ch.2
00005CH	Reserved		TMCSR2 [R/W] 00000000 XX000000		
000060H	SCR0/IBCR0 [R, R/W] 0--00000	SMR0 [R/W] 00000000	SSR0 [R, R/W] 0-000011	ESCR0 [R/W], IBSR0 [R,R/W] -0000000	Multi-function serial interface (with FIFO) ch.0
000064H	RDR0[R]/TDR0[W] -------0 00000000		BGR10 [R/W] 00000000	BGR00 [R/W] 00000000	
000068H	ISMK0 [R/W] 01111111	ISBA0 [R/W] 00000000	Reserved		
00006CH	FCR10 [R/W] 00-00100	FCR00 [R, R/W] 00000000	FBYTE20 [R/W] 00000000	FBYTE10 [R/W] 00000000	
000070H	SCR1/IBCR1 [R, R/W] 0--00000	SMR1 [R/W] 00000000	SSR1 [R, R/W] 0-000011	ESCR1 [R/W], IBSR1 [R,R/W] -0000000	Multi-function serial interface (with FIFO) ch.1
000074H	RDR1[R]/TDR1[W] -------0 00000000		BGR11 [R/W] 00000000	BGR01 [R/W] 00000000	
000078H	ISMK1 [R/W] 01111111	ISBA1 [R/W] 00000000	Reserved		
00007CH	FCR11 [R/W] 00-00100	FCR01 [R, R/W] 00000000	FBYTE21 [R/W] 00000000	FBYTE11 [R/W] 00000000	
000080H	SCR2/IBCR2 [R, R/W] 0--00000	SMR2 [R/W] 00000000	SSR2 [R, R/W] 0-000011	ESCR2 [R/W], IBSR2 [R,R/W] -0000000	Multi-function serial interface (with FIFO) ch.2
000084H	RDR2[R]/TDR2[W] -------0 00000000		BGR12 [R/W] 00000000	BGR02 [R/W] 00000000	
000088H	ISMK2 [R/W] 01111111	ISBA2 [R/W] 00000000	Reserved		
00008CH	FCR12 [R/W] 00-00100	FCR02 [R, R/W] 00000000	FBYTE22 [R/W] 00000000	FBYTE12 [R/W] 00000000	
000090H	SCR3/IBCR3 [R, R/W] 0--00000	SMR3 [R/W] 00000000	SSR3 [R, R/W] 0-000011	ESCR3 [R/W], IBSR3 [R,R/W] -0000000	Multi-function serial interface (with FIFO) ch.3
000094H	RDR3[R]/TDR3[W] -------0 00000000		BGR13 [R/W] 00000000	BGR03 [R/W] 00000000	
000098H	ISMK3 [R/W] 01111111	ISBA3 [R/W] 00000000	Reserved		
00009CH	FCR13 [R/W] 00-00100	FCR03 [R, R/W] 00000000	FBYTE23 [R/W] 00000000	FBYTE13 [R/W] 00000000	

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
0000A0H	SCR4/IBCR4 [R, R/W] 0--00000	SMR4 [R/W] 00000000	SSR4 [R, R/W] 0-000011	ESCR4 [R/W], IBSR4 [R,R/W] -0000000	Multi-function serial interface (with FIFO) ch.4
0000A4H	RDR4[R]/TDR4[W] -------0 00000000		BGR14 [R/W] 00000000	BGR04 [R/W] 00000000	
0000A8H	ISMK4 [R/W] 01111111	ISBA4 [R/W] 00000000	Reserved		
0000ACH	FCR14 [R/W] 00-00100	FCR04 [R, R/W] 00000000	FBYTE24 [R/W] 00000000	FBYTE14 [R/W] 00000000	
0000B0H	SCR5/IBCR5 [R, R/W] 0--00000	SMR5 [R/W] 00000000	SSR5 [R, R/W] 0-000011	ESCR5 [R/W], IBSR5 [R,R/W] -0000000	Multi-function serial interface (with FIFO) ch.5
0000B4H	RDR5[R]/TDR5[W] -------0 00000000		BGR15 [R/W] 00000000	BGR05 [R/W] 00000000	
0000B8H	ISMK5 [R/W] 01111111	ISBA5 [R/W] 00000000	Reserved		
0000BCH	FCR15 [R/W] 00-00100	FCR05 [R, R/W] 00000000	FBYTE25 [R/W] 00000000	FBYTE15 [R/W] 00000000	
0000C0H	SCR6/IBCR6 [R, R/W] 0--00000	SMR6 [R/W] 00000000	SSR6 [R, R/W] 0-000011	ESCR6 [R/W], IBSR6 [R,R/W] -0000000	Multi-function serial interface (with FIFO) ch.6
0000C4H	RDR6[R]/TDR6[W] -------0 00000000		BGR16 [R/W] 00000000	BGR06 [R/W] 00000000	
0000C8H	ISMK6 [R/W] 01111111	ISBA6 [R/W] 00000000	Reserved		
0000CCH	FCR16 [R/W] 00-00100	FCR06 [R, R/W] 00000000	FBYTE26 [R/W] 00000000	FBYTE16 [R/W] 00000000	
0000D0H	SCR7/IBCR7 [R, R/W] 0--00000	SMR7 [R/W] 00000000	SSR7 [R, R/W] 0-000011	ESCR7 [R/W], IBSR7 [R,R/W] -0000000	Multi-function serial interface (with FIFO) ch.7
0000D4H	RDR7[R]/TDR7[W] -------0 00000000		BGR17 [R/W] 00000000	BGR07 [R/W] 00000000	
0000D8H	ISMK7 [R/W] 01111111	ISBA7 [R/W] 00000000	Reserved		
0000DCH	FCR17 [R/W] 00-00100	FCR07 [R, R/W] 00000000	FBYTE27 [R/W] 00000000	FBYTE17 [R/W] 00000000	
0000E0H	EIRR1 [R/W] 00000000	ENIR1 [R/W] 00000000	ELVR1 [R/W] 00000000 00000000		External interrupt 8 to 15
0000E4H	EIRR2 [R/W] 00000000	ENIR2 [R/W] 00000000	ELVR2 [R/W] 00000000 00000000		External interrupt 16 to 23

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
0000E8H	IRPR0H [R] 00000000	Reserved			Interrupt request batch read function
0000ECH	Reserved				Reserved
0000F0H	RCCR [R/W] 0---0000	RCST [R/W] 00000000	RCSHW [R/W] 00000000	RCDAHW [R/W] 00000000	Remote control
0000F4H	RCDBHW [R/W] 00000000	Reserved	RCADR1 [R/W] ---00000	RCADR2 [R/W] ---00000	
0000F8H	RCDTHH [R] 00000000	RCDTHL [R] 00000000	RCDTLH [R] 00000000	RCDTLL[R] 00000000	
0000FCH	RCCKD [R/W] ---00000 00000000		Reserved		
000100H to 0001FCH	Reserved				Reserved
000200H	SCR8/IBCR8 [R, R/W] 0--00000	SMR8 [R/W] 00000000	SSR8 [R, R/W] 0-000011	ESCR8 [R/W], IBSR8 [R,R/W] -0000000	Multi-function serial interface (without FIFO) ch.8
000204H	RDR8[R]/TDR8[W] -------0 00000000		BGR18 [R/W] 00000000	BGR08 [R/W] 00000000	
000208H	ISMK8 [R/W] 01111111	ISBA8 [R/W] 00000000	Reserved		
00020CH	Reserved				
000210H	SCR9/IBCR9 [R, R/W] 0--00000	SMR9 [R/W] 00000000	SSR9 [R, R/W] 0-000011	ESCR9 [R/W], IBSR9 [R,R/W] -0000000	Multi-function serial interface (without FIFO) ch.9
000214H	RDR9[R]/TDR9[W] -------0 00000000		BGR19 [R/W] 00000000	BGR09 [R/W] 00000000	
000218H	ISMK9 [R/W] 01111111	ISBA9 [R/W] 00000000	Reserved		
00021CH	Reserved				
000220H	SCRA/IBCRA [R, R/W] 0--00000	SMRA [R/W] 00000000	SSRA [R, R/W] 0-000011	ESCRA [R/W], IBSRA [R,R/W] -0000000	Multi-function serial interface (without FIFO) ch.10
000224H	RDRA[R]/TDRA[W] -------0 00000000		BGR1A [R/W] 00000000	BGR0A [R/W] 00000000	
000228H	ISMKA [R/W] 01111111	ISBAA [R/W] 00000000	Reserved		
00022CH	Reserved				

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000230H	SCRB/IBCRB [R, R/W] 0--00000	SMRB [R/W] 00000000	SSRB [R, R/W] 0-000011	ESCRB [R/W], IBSRB [R,R/W] -0000000	Multi-function serial interface (without FIFO) ch.11
000234H	RDRB[R]/TDRB[W] -------0 00000000		BGR1B [R/W] 00000000	BGR0B [R/W] 00000000	
000238H	ISMKB [R/W] 01111111	ISBAB [R/W] 00000000	Reserved		
00023CH	Reserved				
000240H	RDRM8/TDRM8 [R/W] 00000000	RDRM9/TDRM9 [R/W] 00000000	RDRMA/TDRMA [R/W] 00000000	RDRMB/TDRMB [R/W] 00000000	Multi-function serial interface data register (mirror)
000244H	SSEL89AB [R/W] ------00	Reserved			Multi-function serial interface serial clock selection
000248H to 00027CH	Reserved				Reserved
000280H	BT0TMR [R] 00000000 00000000		BT0TMCR [R/W] 00000000 00000000		Base timer ch.0
000284H	Reserved	BT0STC [R/W] 00000000	Reserved		
000288H	BT0PCSR/BT0PRLL [R/W] XXXXXXXX XXXXXXXX		BT0PDUT/BT0PRLH [R/W], BT0DTBF [R] XXXXXXXX XXXXXXXX		
00028CH	Reserved				
000290H	BT1TMR [R] 00000000 00000000		BT1TMCR [R/W] 00000000 00000000		Base timer ch.1
000294H	Reserved	BT1STC [R/W] 00000000	Reserved		
000298H	BT1PCSR/BT1PRLL [R/W] XXXXXXXX XXXXXXXX		BT1PDUT/BT1PRLH [R/W], BT1DTBF [R] XXXXXXXX XXXXXXXX		
00029CH	Reserved				
0002A0H	BT2TMR [R] 00000000 00000000		BT2TMCR [R/W] 00000000 00000000		Base timer ch.2
0002A4H	Reserved	BT2STC [R/W] 00000000	Reserved		
0002A8H	BT2PCSR/BT2PRLL [R/W] XXXXXXXX XXXXXXXX		BT2PDUT/BT2PRLH [R/W], BT2DTBF [R] XXXXXXXX XXXXXXXX		
0002ACH	Reserved				

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
0002B0H	BT3TMR [R] 00000000 00000000		BT3TMCR [R/W] 00000000 00000000		Base timer ch.3
0002B4H	Reserved	BT3STC [R/W] 00000000	Reserved		
0002B8H	BT3PCSR/BT3PRLL [R/W] XXXXXXXX XXXXXXXX		BT3PDUT/BT3PRLH [R/W], BT3DTBF [R] XXXXXXXX XXXXXXXX		
0002BCH	BTSEL0123 [R/W] 00000000	Reserved			
0002C0H	BT4TMR [R] 00000000 00000000		BT4TMCR [R/W] 00000000 00000000		Base timer ch.4
0002C4H	Reserved	BT4STC [R/W] 00000000	Reserved		
0002C8H	BT4PCSR/BT4PRLL [R/W] XXXXXXXX XXXXXXXX		BT4PDUT/BT4PRLH [R/W], BT4DTBF [R] XXXXXXXX XXXXXXXX		
0002CCH	Reserved				
0002D0H	BT5TMR [R] 00000000 00000000		BT5TMCR [R/W] 00000000 00000000		Base timer ch.5
0002D4H	Reserved	BT5STC [R/W] 00000000	Reserved		
0002D8H	BT5PCSR/BT5PRLL [R/W] XXXXXXXX XXXXXXXX		BT5PDUT/BT5PRLH [R/W], BT5DTBF [R] XXXXXXXX XXXXXXXX		
00028DH	Reserved				
0002E0H	BT6TMR [R] 00000000 00000000		BT6TMCR [R/W] 00000000 00000000		Base timer ch.6
0002E4H	Reserved	BT6STC [R/W] 00000000	Reserved		
0002E8H	BT6PCSR/BT6PRLL [R/W] XXXXXXXX XXXXXXXX		BT6PDUT/BT6PRLH [R/W], BT6DTBF [R] XXXXXXXX XXXXXXXX		
0002ECH	Reserved				
0002F0H	BT7TMR [R] 00000000 00000000		BT7TMCR [R/W] 00000000 00000000		Base timer ch.7
0002F4H	Reserved	BT7STC [R/W] 00000000	Reserved		
0002F8H	BT7PCSR/BT7PRLL [R/W] XXXXXXXX XXXXXXXX		BT7PDUT/BT7PRLH [R/W], BT7DTBF [R] XXXXXXXX XXXXXXXX		
0002FCH	BTSEL4567 [R/W] 00000000	Reserved			

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000300H to 0003CCH	Reserved				Reserved
0003D0H to 0003DCH	Reserved				Instruction/data cache
0003E0H	CARR [R/W] 00000000	Reserved		DCHCR [R/W] XXXXXX00	
0003E4H	Reserved			ICHCR [R/W] XXXX0000	
0003E8H	DSIZE [R] 00100000 00000000		DFUNC [R] 00000001 01010010		
0003ECH	ISIZE [R] 00100000 00000000		IFUNC [R] 00000000 00010110		
0003F0H to 0003FCH	Reserved				Reserved
000400H	Reserved		DDR2 [R/W] ----0000	DDR3 [R/W] 00000000	Data direction register
000404H	DDR4 [R/W] --000000	DDR5 [R/W] 00000000	DDR6 [R/W] 00000000	DDR7[R/W] 00000000	
000408H	DDR8 [R/W] --000000	DDR9 [R/W] --000000	DDRA [R/W] --000000	DDRB[R/W] 00000000	
00040CH	DDRC [R/W] 00000000	DDRD [R/W] 00000000	DDRE [R/W] 00000000	Reserved	
000410H to 00041CH	Reserved				
000420H, 000424H	Reserved				Port pull-up control register
000428H	Reserved			PCRB [R/W] 00000000	
00042CH	PCRC [R/W] 00000000	Reserved	PCRE [R/W] 00000000	Reserved	
000430H to 00043CH	Reserved				

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000440H	ICR00 [R/W] 11111111	ICR01 [R/W] 11111111	ICR02 [R/W] 11111111	ICR03 [R/W] 11111111	Interrupt controller
000444H	ICR04 [R/W] 11111111	ICR05 [R/W] 11111111	ICR06 [R/W] 11111111	ICR07 [R/W] 11111111	
000448H	ICR08 [R/W] 11111111	ICR09 [R/W] 11111111	ICR10 [R/W] 11111111	ICR11 [R/W] 11111111	
00044CH	ICR12 [R/W] 11111111	ICR13 [R/W] 11111111	ICR14 [R/W] 11111111	ICR15 [R/W] 11111111	
000450H	ICR16 [R/W] 11111111	ICR17 [R/W] 11111111	ICR18 [R/W] 11111111	ICR19 [R/W] 11111111	
000454H	ICR20 [R/W] 11111111	ICR21 [R/W] 11111111	ICR22 [R/W] 11111111	ICR23 [R/W] 11111111	
000458H	ICR24 [R/W] 11111111	ICR25 [R/W] 11111111	ICR26 [R/W] 11111111	ICR27 [R/W] 11111111	
00045CH	ICR28 [R/W] 11111111	ICR29 [R/W] 11111111	ICR30 [R/W] 11111111	ICR31 [R/W] 11111111	
000460H	ICR32 [R/W] 11111111	ICR33 [R/W] 11111111	ICR34 [R/W] 11111111	ICR35 [R/W] 11111111	
000464H	ICR36 [R/W] 11111111	ICR37 [R/W] 11111111	ICR38 [R/W] 11111111	ICR39 [R/W] 11111111	
000468H	ICR40 [R/W] 11111111	ICR41 [R/W] 11111111	ICR42 [R/W] 11111111	ICR43 [R/W] 11111111	
00046CH	ICR44 [R/W] 11111111	ICR45 [R/W] 11111111	ICR46 [R/W] 11111111	ICR47 [R/W] 11111111	
000470H to 00047CH	Reserved				
000480H	RSTRR [R] XXXXXXXX	RSTCR [R/W] 00000000	STBCR [R/W] 00000011	SLPRR [R/W] 00000000	Clock control unit
000484H	Reserved				
000488H	DIVR0 [R/W] 00000000	DIVR1 [R/W] 00010000	DIVR2 [R/W] 00110000	Reserved	
00048CH	Reserved				
000490H	IORR0 [R/W] 00000000	IORR1 [R/W] 00000000	IORR2 [R/W] 00000000	IORR3 [R/W] 00000000	Peripheral DMA transfer request
000494H to 00049CH	Reserved				Reserved

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
0004A0H	Reserved		PFR2 [R/W] ----1110	PFR3 [R/W] 10001111	Port function register
0004A4H	PFR4 [R/W] --110000	PFR5 [R/W] 11111111	PFR6 [R/W] 00000000	PFR7 [R/W] 00000000	
0004A8H	PFR8 [R/W] --000000	PFR9 [R/W] --000000	PFRA [R/W] --000000	PFRB [R/W] 00000000	
0004ACH	PFRC [R/W] 00000000	PFRD [R/W] 00000000	PFRE [R/W] 00000000	Reserved	
0004B0H to 0004DCH	Reserved				
0004E0H	ADER [R/W] 00001111 11111111		Reserved		A/D input enable
0004E4H to 0004ECH	Reserved				Reserved
0004F0H	ICSEL0[R/W] 00000000	ICSEL1[R/W] 00000000	ICSEL2[R/W] 00000000	ICSEL3[R/W] 00000000	DMA start request clear select function
0004F4H to 00050CH	Reserved				Reserved
000510H	CSELR [R/W] -01---00 (at INIT) -**---** (at RST)	CMONR [R] -01---00 (at INIT) -**---** (at RST)	MTMCR [R/W] 00001111	Reserved	Clock generation
000514H	PLLCR [R/W] --000000 11110000 (at INIT) --****** ******** (at RST)		CSTBR [R/W] ---- 0000 ($\overline{\text{INIT}}$ pin = “L” level) ---- **** (at INIT) 0*** **** (at RST)	Reserved	
000518H to 0007DCH	Reserved				Reserved
0007E0H to 0007E8H	Reserved				DMAC
0007ECH	Reserved		DNMIR [R/W] 00000000	DILVR [R/W] 00011111	
0007F0H to 0007F8H	Reserved				Reserved

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
0007FC$_H$	BMODR [R] XXXXXXXX (Varied by operation modes)	MODR [R] 000XXXXX (Varied by operation modes)	Reserved		Operation mode control
000800$_H$ to 000BFC$_H$	Reserved				Reserved
000C00$_H$	GCFR [R/W] 00000000 00000000 00000000 00000000				DMAC
000C04$_H$ to 000CFC$_H$	Reserved				Reserved
000D00$_H$	CCFR0 [R/W] 00000000 00000000		CSTR0 [R/W] 00000000 00000000		DMAC
000D04$_H$	CCTR0 [R/W] 00000000 00000000		Reserved		
000D08$_H$	SBA0 [R/W] 00000000 00000000 00000000 00000000				
000D0C$_H$	DBA0 [R/W] 00000000 00000000 00000000 00000000				
000D10$_H$	PIX0 [R/W] 00000000 00000000 00000000 00000000				
000D14$_H$	SIX0 [R/W] 00000000 00000000 00000000 00000000				
000D18$_H$	BCL0 [R/W] 00000000 00000000 00000000 00000000				
000D1C$_H$	APR0 [R/W] 00000000 00000000 00000000 00000000				
000D20$_H$	CCFR1 [R/W] 00000000 00000000		CSTR1 [R/W] 00000000 00000000		
000D24$_H$	CCTR1 [R/W] 00000000 00000000		Reserved		
000D28$_H$	SBA1 [R/W] 00000000 00000000 00000000 00000000				
000D2C$_H$	DBA1 [R/W] 00000000 00000000 00000000 00000000				
000D30$_H$	PIX1 [R/W] 00000000 00000000 00000000 00000000				
000D34$_H$	SIX1 [R/W] 00000000 00000000 00000000 00000000				

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000D38H	BCL1 [R/W] 00000000 00000000 00000000 00000000				DMAC
000D3CH	APR1 [R/W] 00000000 00000000 00000000 00000000				
000D40H	CCFR2 [R/W] 00000000 00000000		CSTR2 [R/W] 00000000 00000000		
000D44H	CCTR2 [R/W] 00000000 00000000		Reserved		
000D48H	SBA2 [R/W] 00000000 00000000 00000000 00000000				
000D4CH	DBA2 [R/W] 00000000 00000000 00000000 00000000				
000D50H	PIX2 [R/W] 00000000 00000000 00000000 00000000				
000D54H	SIX2 [R/W] 00000000 00000000 00000000 00000000				
000D58H	BCL2 [R/W] 00000000 00000000 00000000 00000000				
000D5CH	APR2 [R/W] 00000000 00000000 00000000 00000000				
000D60H	CCFR3 [R/W] 00000000 00000000		CSTR3 [R/W] 00000000 00000000		
000D64H	CCTR3 [R/W] 00000000 00000000		Reserved		
000D68H	SBA3 [R/W] 00000000 00000000 00000000 00000000				
000D6CH	DBA3 [R/W] 00000000 00000000 00000000 00000000				
000D70H	PIX3 [R/W] 00000000 00000000 00000000 00000000				
000D74H	SIX3 [R/W] 00000000 00000000 00000000 00000000				
000D78H	BCL3 [R/W] 00000000 00000000 00000000 00000000				
000D7CH	APR3 [R/W] 00000000 00000000 00000000 00000000				
000D80H to 000EFCH	Reserved				Reserved

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000F00H	BT8TMR [R] 00000000 00000000		BT8TMCR [R/W] 00000000 00000000		Base timer ch.8
000F04H	Reserved	BT8STC [R/W] 00000000	Reserved		
000F08H	BT8PCSR/BT8PRLL [R/W] XXXXXXXX XXXXXXXX		BT8PDUT/BT8PRLH [R/W], BT8DTBF [R] XXXXXXXX XXXXXXXX		
000F0CH	Reserved				
000F10H	BT9TMR [R] 00000000 00000000		BT9TMCR [R/W] 00000000 00000000		Base timer ch.9
000F14H	Reserved	BT9STC [R/W] 00000000	Reserved		
000F18H	BT9PCSR/BT9PRLL [R/W] XXXXXXXX XXXXXXXX		BT9PDUT/BT9PRLH [R/W], BT9DTBF [R] XXXXXXXX XXXXXXXX		
000F1CH	Reserved				
000F20H	BTATMR [R] 00000000 00000000		BTATMCR [R/W] 00000000 00000000		Base timer ch.10
000F24H	Reserved	BTASTC [R/W] 00000000	Reserved		
000F28H	BTAPCSR/BTAPRLL [R/W] XXXXXXXX XXXXXXXX		BTAPDUT/BTAPRLH [R/W], BTADTBF [R] XXXXXXXX XXXXXXXX		
000F2CH	Reserved				
000F30H	BTBTMR [R] 00000000 00000000		BTBTMCR [R/W] 00000000 00000000		Base timer ch.11
000F34H	Reserved	BTBSTC [R/W] 00000000	Reserved		
000F38H	BTBPCSR/BTBPRLL [R/W] XXXXXXXX XXXXXXXX		BTBPDUT/BTBPRLH [R/W], BTBDTBF [R] XXXXXXXX XXXXXXXX		
000F3CH	BTSEL89AB [R/W] 00000000	Reserved	BTSSSR [W] -------- --------		
000F40H to 001FFCH	Reserved				Reserved

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
002000H	MCMR0 [R/W] -------- -------- -------- -0000000				External bus interface
002004H	MCMR1 [R/W] -------- -------- -------- -0000000				
002008H	MCMR2 [R/W] -------- -------- -------- -0000000				
00200CH	MCMR3 [R/W] -------- -------- -------- -0000000				
002010H	MCMR4 [R/W] -------- -------- -------- -0000001				
002014H	MCMR5 [R/W] -------- -------- -------- -0000000				
002018H	MCMR6 [R/W] -------- -------- -------- -0000000				
00201CH	MCMR7 [R/W] -------- -------- -------- -0000000				
002020H	MCTR0 [R/W] 00000101 01011111 11110000 00001111				
002024H	MCTR1 [R/W] 00000101 01011111 11110000 00001111				
002028H	MCTR2 [R/W] 00000101 01011111 11110000 00001111				
00202CH	MCTR3 [R/W] 00000101 01011111 11110000 00001111				
002030H	MCTR4 [R/W] 00000101 01011111 11110000 00001111				
002034H	MCTR5 [R/W] 00000101 01011111 11110000 00001111				
002038H	MCTR6 [R/W] 00000101 01011111 11110000 00001111				
00203CH	MCTR7 [R/W] 00000101 01011111 11110000 00001111				
002040H	MCAR0 [R/W] -------- -0001111 -------- 01000000				
002044H	MCAR1 [R/W] -------- -0001111 -------- 00010000				
002048H	MCAR2 [R/W] -------- -0001111 -------- 00100000				
00204CH	MCAR3 [R/W] -------- -0001111 -------- 00110000				

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Address	Register				Block
	+0	+1	+2	+3	
002050H	MCAR4 [R/W] -------- -0001111 -------- 00000000				External bus interface
002054H	MCAR5 [R/W] -------- -0001111 -------- 01010000				
002058H	MCAR6 [R/W] -------- -0001111 -------- 01100000				
00205CH	MCAR7 [R/W] -------- -0001111 -------- 01110000				
002000H to 0020FCH	Reserved				Reserved
002100H	SDMR [R/W] -------- -------- 00010011 --00-000				SDRAM interface
002104H	SDRTR [R/W] -------0 00000000 00000000 00101000				
002108H	SDPDR [R/W] -------- -------- 00000000 00000000				
00210CH	SDTR [R/W] ------00 01000010 00010001 0100--01				
002110H	SDCMR [R/W] 0------- ---00000 00000000 00000000				
002114H to 0022FCH	Reserved				Reserved
002300H	CLKCTL [R/W] ------00	Reserved			External bus interface
002304H to 007FFCH	Reserved				Reserved

■ VECTOR TABLE

Interrupt source	Interrupt number		Interrupt level	Offset	TBR default address	DMA transfer request
	Decimal	Hexa-decimal				
Reset	0	00	—	3FC$_H$	000FFFFC$_H$	—
System reserved	1	01	—	3F8$_H$	000FFFF8$_H$	—
System reserved	2	02	—	3F4$_H$	000FFFF4$_H$	—
System reserved	3	03	—	3F0$_H$	000FFFF0$_H$	—
System reserved	4	04	—	3EC$_H$	000FFFEC$_H$	—
System reserved	5	05	—	3E8$_H$	000FFFE8$_H$	—
System reserved	6	06	—	3E4$_H$	000FFFE4$_H$	—
System reserved	7	07	—	3E0$_H$	000FFFE0$_H$	—
System reserved	8	08	—	3DC$_H$	000FFFDC$_H$	—
INTE instruction	9	09	—	3D8$_H$	000FFFD8$_H$	—
Instruction break exception	10	0A	—	3D4$_H$	000FFFD4$_H$	—
Operand break	11	0B	—	3D0$_H$	000FFFD0$_H$	—
Step trace trap	12	0C	—	3CC$_H$	000FFFCC$_H$	—
NMI request (tool)	13	0D	—	3C8$_H$	000FFFC8$_H$	—
Undefined instruction exception	14	0E	—	3C4$_H$	000FFFC4$_H$	—
NMI request	15	0F	15 (F$_H$) fixed	3C0$_H$	000FFFC0$_H$	—
External interrupt ch.0	16	10	ICR00	3BC$_H$	000FFFBC$_H$	○
External interrupt ch.1	17	11	ICR01	3B8$_H$	000FFFB8$_H$	○
External interrupt ch.2	18	12	ICR02	3B4$_H$	000FFFB4$_H$	○
External interrupt ch.3	19	13	ICR03	3B0$_H$	000FFFB0$_H$	○
External interrupt ch.4	20	14	ICR04	3AC$_H$	000FFFAC$_H$	○
External interrupt ch.5	21	15	ICR05	3A8$_H$	000FFFA8$_H$	○
External interrupt ch.6	22	16	ICR06	3A4$_H$	000FFFA4$_H$	○
External interrupt ch.7	23	17	ICR07	3A0$_H$	000FFFA0$_H$	○
16-bit reload timer ch.0	24	18	ICR08	39C$_H$	000FFF9C$_H$	○
16-bit reload timer ch.1	25	19	ICR09	398$_H$	000FFF98$_H$	○
16-bit reload timer ch.2	26	1A	ICR10	394$_H$	000FFF94$_H$	○
Multi-function serial interface ch.0 RX	27	1B	ICR11	390$_H$	000FFF90$_H$	○
Multi-function serial interface ch.0 TX	28	1C	ICR12	38C$_H$	000FFF8C$_H$	○
Multi-function serial interface ch.0 I^{2}C status	29	1D	ICR13	388$_H$	000FFF88$_H$	—
Multi-function serial interface ch.1 RX	30	1E	ICR14	384$_H$	000FFF84$_H$	○
Multi-function serial interface ch.1 TX	31	1F	ICR15	380$_H$	000FFF80$_H$	○
Multi-function serial interface ch.1 I^{2}C status	32	20	ICR16	37C$_H$	000FFF7C$_H$	—
Multi-function serial interface ch.2 RX	33	21	ICR17	378$_H$	000FFF78$_H$	○

(Continued)

Interrupt source	Interrupt number		Interrupt level	Offset	TBR default address	DMA transfer request
	Decimal	Hexa-decimal				
Multi-function serial interface ch.2 TX	34	22	ICR18	374H	000FFF74H	○
Multi-function serial interface ch.2 I²C status	35	23	ICR19	370H	000FFF70H	—
Multi-function serial interface ch.3 RX/TX/I²C status	36	24	ICR20	36CH	000FFF6CH	○*
Multi-function serial interface ch.4 RX/TX/I²C status	37	25	ICR21	368H	000FFF68H	○*
Multi-function serial interface ch.5 RX/TX/I²C status	38	26	ICR22	364H	000FFF64H	○*
A/D converter	39	27	ICR23	360H	000FFF60H	○
HDMI-CEC/Remote control	40	28	ICR24	35CH	000FFF5CH	—
External interrupt 8-15	41	29	ICR25	358H	000FFF58H	○
External interrupt 16-23	42	2A	ICR26	354H	000FFF54H	○
Multi-function serial interface ch.6 RX/TX/I²C status	43	2B	ICR27	350H	000FFF50H	○*
Multi-function serial interface ch.7 RX/TX/I²C status	44	2C	ICR28	34CH	000FFF4CH	○*
Multi-function serial interface ch.8 RX/TX/I²C status	45	2D	ICR29	348H	000FFF48H	○*
Multi-function serial interface ch.9 RX/TX/I²C status	46	2E	ICR30	344H	000FFF44H	○*
Multi-function serial interface ch.10 RX/TX/I²C status	47	2F	ICR31	340H	000FFF40H	○*
Multi-function serial interface ch.11 RX/TX/I²C status	48	30	ICR32	33CH	000FFF3CH	○*
Base timer ch.0	49	31	ICR33	338H	000FFF38H	○
Base timer ch.1	50	32	ICR34	334H	000FFF34H	○
Base timer ch.2	51	33	ICR35	330H	000FFF30H	○
Base timer ch.3	52	34	ICR36	32CH	000FFF2CH	○
Base timer ch.4	53	35	ICR37	328H	000FFF28H	○
Base timer ch.5	54	36	ICR38	324H	000FFF24H	○
Base timer ch.6	55	37	ICR39	320H	000FFF20H	○
Base timer ch.7	56	38	ICR40	31CH	000FFF1CH	○
Base timer ch.8/ch.9/ch.10/ch.11	57	39	ICR41	318H	000FFF18H	○
DMAC ch.0	58	3A	ICR42	314H	000FFF14H	—
DMAC ch.1	59	3B	ICR43	310H	000FFF10H	—
DMAC ch.2	60	3C	ICR44	30CH	000FFF0CH	—
DMAC ch.3	61	3D	ICR45	308H	000FFF08H	—
Timebase timer	62	3E	ICR46	304H	000FFF04H	—

(Continued)

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Interrupt source	Interrupt number		Interrupt level	Offset	TBR default address	DMA transfer request
	Decimal	Hexa-decimal				
Delay interrupt	63	3F	ICR47	300_H	$000FFF00_H$	—
System reserved (Used by REALOS)	64	40	—	$2FC_H$	$000FFEFC_H$	—
System reserved (Used by REALOS)	65	41	—	$2F8_H$	$000FFEF8_H$	—
Used by INT instruction	66 to 255	42 to FF	—	$2F4_H$ to 000_H	$000FFEF4_H$ to $000FFC00_H$	—

* : The I^2C status interrupt cannot be used for DMAC transfer requests.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{DDE}	Vss − 0.3	Vss + 4.0	V	
	V_{DDI}	Vss − 0.3	Vss + 2.2	V	
Analog power supply voltage*1	AV_{CC}	Vss − 0.3	Vss + 4.0	V	*2
Analog reference power voltage*1	AVRH	Vss − 0.3	Vss + 4.0	V	*2
Input voltage*1	V_I	Vss − 0.3	V_{DDE} + 0.5	V	
Analog pin input voltage*1	V_{IA}	Vss − 0.3	AVcc + 0.5	V	
Output voltage*1	V_O	Vss − 0.3	V_{DDE} + 0.5	V	
“L” level maximum output current	I_{OL}	—	10	mA	*3
“L” level average output current	I_{OLAV}	—	4	mA	*4
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current	ΣI_{OLAV}	—	50	mA	*5
“H” level maximum output current	I_{OH}	—	−10	mA	*3
“H” level average output current	I_{OHAV}	—	−4	mA	*4
“H” level total maximum output current	ΣI_{OH}	—	−100	mA	
“H” level total average output current	ΣI_{OHAV}	—	−50	mA	*5
Power consumption	P_D	—	—	mW	
Operating temperature	T_a	−10	+70	°C	
Storage temperature	T_{STG}	−55	+125	°C	

*1 : The parameter is based on $AV_{SS} = V_{SS} = 0.0$ V.

*2 : Must not exceed V_{DDE} + 0.3 V during transitions such as when the power is turned on.

*3 : The maximum output current is the peak value for a single pin.

*4 : The average output current is the average current for a single pin over a period of 100 ms.

*5 : The total average output current is the average current for all pins over a period of 100 ms.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(Vss = AVss = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{DDE}	3.0	3.6	V	
	V_{DDI}	1.65	1.95	V	
Analog power supply voltage	AV_{CC}	3.0	3.6	V	Avcc ≤ V_{DDE}
Analog reference voltage	AVRH	AV_{SS}	AV_{CC}	V	
Operating temperature	T_a	− 10	+ 70	°C	

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

3. DC Characteristics

(V_{DDE} = AVcc = 3.0 V to 3.6 V, V_{DDI} = 1.65 V to 1.95 V, Vss = AVss = 0 V, Ta = –10 °C to + 70 °C)

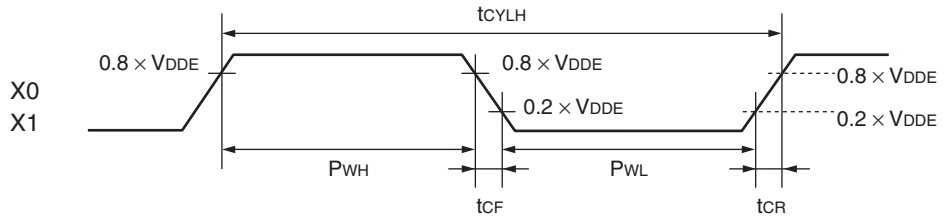
Parameter	Sym-bol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CC}	Upper : VDDE, Lower : VDDI	During normal operation	—	—	100	mA	CPU : 80 MHz, Peripheral : 40 MHz, External bus : 80 MHz
				—	—	180		
	I_{CCS}		Sleep mode	—	—	50	mA	CPU : 80 MHz, Peripheral : 40 MHz, External bus : 80 MHz
				—	—	90		
	I_{CCH}		Stop mode	—	—	100	µA	Ta = + 25 °C, V_{DDE} = 3.3 V, V_{DDI} = 1.8 V
				—	—	1000		
“H” level input voltage	V_{IH}	—	—	V_{DDE} × 0.7	—	V_{DDE} + 0.3	V	
“L” level input voltage	V_{IL}	—	—	Vss – 0.3	—	V_{DDE} × 0.3	V	
“H” level input voltage (hysteresis input)	V_{IHS}	—	—	V_{DDE} × 0.8	—	V_{DDE} + 0.3	V	
“L” level input voltage (hysteresis input)	V_{ILS}	—	—	Vss – 0.3	—	V_{DDE} × 0.2	V	
“H” level output voltage	V_{OH}	—	V_{DDE} = 3.0 V I_{OH} = –4 mA	V_{DDE} – 0.5	—	V_{DDE}	V	
“L” level output voltage	V_{OL}	—	V_{DDE} = 3.0 V I_{OL} = 4 mA	Vss	—	0.4	V	
Input leak current	I_{IL}	—	—	– 5	—	+ 5	µA	(Digital pins)
			—	– 10	—	+ 10	µA	(Analog-shared pins)
Pull-up resistor value/pull-down resistor value	R_{PU}	Pull-up pin Pull-down pin	—	16.6	33	66	kΩ	
Input capacitance	C_{IN}	Other than VDDE, VDDI, VSS, AVCC, AVSS, AVRH	—	—	10	—	pF	

4. AC Characteristics

(1) Main Clock Input Standard

(V_{DDE} = AVcc = 3.0 V to 3.6 V, V_{DDI} = 1.65 V to 1.95 V, Vss = AVss = 0 V, Ta = –10 °C to + 70 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Input frequency	F_{CH}	X0 X1	—	10	20	MHz	When using PLL
			—	4	20	MHz	When using external clock
Input clock cycle	t_{CYLH}		—	50	250	ns	When using external clock
Input clock pulse width	—		P_{WH}/t_{CYLH} P_{WL}/t_{CYLH}	45	55	%	When using external clock
Input clock rise time and fall time	T_{CF} t_{CR}		—	—	5	ns	When using external clock
Internal operating clock frequency	F_{CC}	—	—	—	80	MHz	CPU clock
	F_{CP}	—	—	—	40	MHz	Peripheral clock
	F_{CT}	—	—	—	80	MHz	External bus clock
Internal operating clock cycle time	t_{CYCC}	—	—	12.5	—	ns	CPU clock
	t_{CYCP}	—	—	25	—	ns	Peripheral clock
	t_{CYCT}	—	—	12.5	—	ns	External bus clock



(2) PLL Oscillation Stabilization Time (LOCK UP Time)

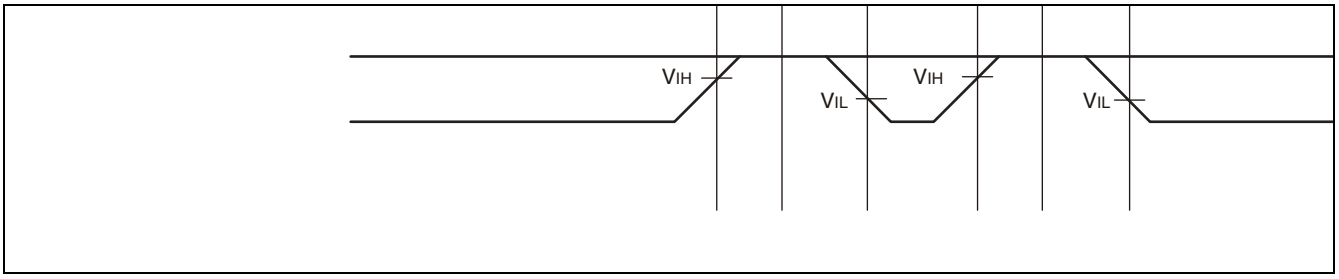
(V_{DDE} = AVcc = 3.0 V to 3.6 V, V_{DDI} = 1.65 V to 1.95 V, Vss = AVss = 0 V, Ta = –10 °C to + 70 °C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
PLL oscillation stabilization time (LOCK UP time)	t_{LOCK}	—	600	—	µs	Time from when the PLL starts operating until the oscillation stabilizes

(3) Reset Input Standards

(V_{DDE} = AVcc = 3.0 V to 3.6 V, V_{DDI} = 1.65 V to 1.95 V, Vss = AVss = 0 V, Ta = –10 °C to + 70 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Reset input time (At power-on, main oscillation stop mode)	t_{INITX}	$\overline{INIT}$	—	Oscillation time of oscillator + 10 t_{CYLH}	—	ns
Reset input time (At other times)				10 t_{CYLH}	—	ns
Reset input rise time and fall time	t_{INITXF} t_{INITXR}			—	10	ms



(4) Clock Output Timing

t_{CHCL} : t_{CLCH} = 1 : 1 (divided by 1, 2, 4)

(V_{DDE} = AVcc = 3.0 V to 3.6 V, V_{DDI} = 1.65 V to 1.95 V, Vss = AVss = 0 V, Ta = –10 °C to + 70 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Cycle time	t_{CYC}*	MCLK	$F_{CT} = F_{CC}$ $F_{CT} = F_{CC} / 2$	t_{CYCT}	—	ns
MCLK ↑ → MCLK ↓	t_{CHCL}			$t_{CYC} / 2 - 2.25$	$t_{CYC} / 2 + 2.25$	ns
MCLK ↓ → MCLK ↑	t_{CLCH}			$t_{CYC} / 2 - 2.25$	$t_{CYC} / 2 + 2.25$	ns

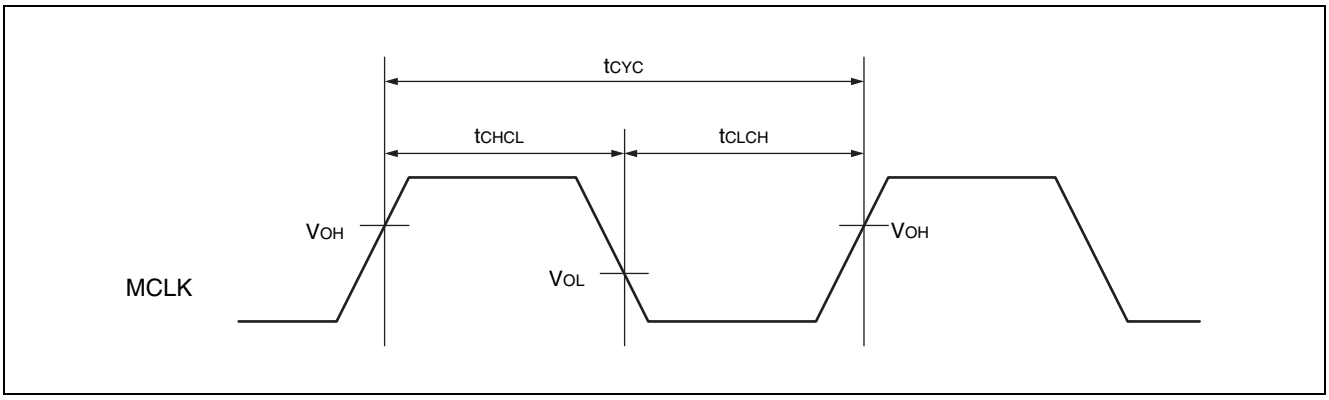
* : t_{CYC} is the period of 1 clock cycle including the gear cycle.

t_{CHCL} : t_{CLCH} = 1 : 2 (divided by 3)

(V_{DDE} = AVcc = 3.0 V to 3.6 V, V_{DDI} = 1.65 V to 1.95 V, Vss = AVss = 0 V, Ta = –10 °C to + 70 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Cycle time	t_{CYC}*	MCLK	$F_{CT} = F_{CC}$ $F_{CT} = F_{CC} / 2$	t_{CYCT}	—	ns
MCLK ↑ → MCLK ↓	t_{CHCL}			1/3 t_{CYC} – 2.25	1/3 t_{CYC} + 2.25	ns
MCLK ↓ → MCLK ↑	t_{CLCH}			2/3 t_{CYC} – 2.25	2/3 t_{CYC} + 2.25	ns

* : t_{CYC} is the period of 1 clock cycle including the gear cycle.



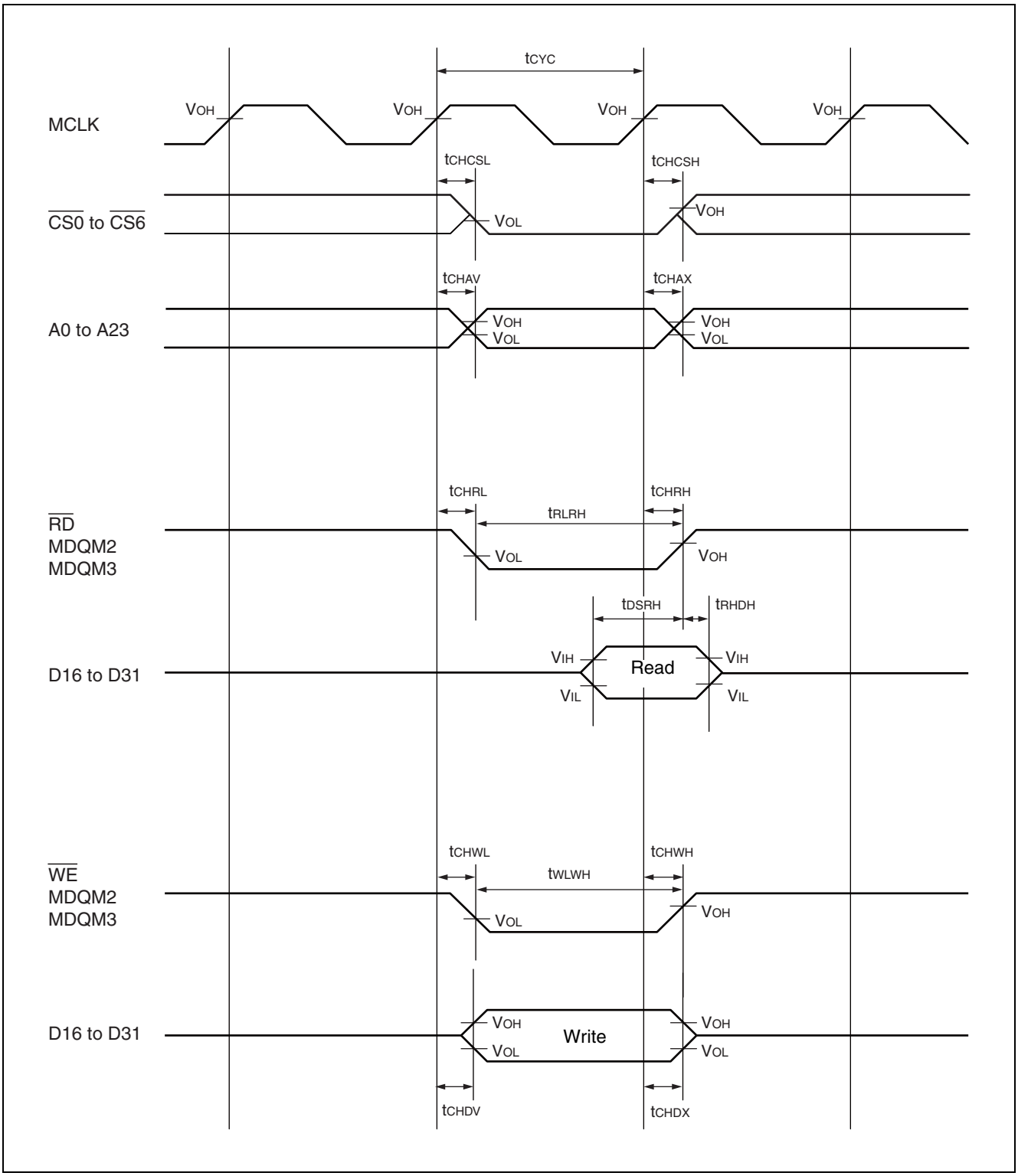
(5) External Bus Access Read/Write Operation

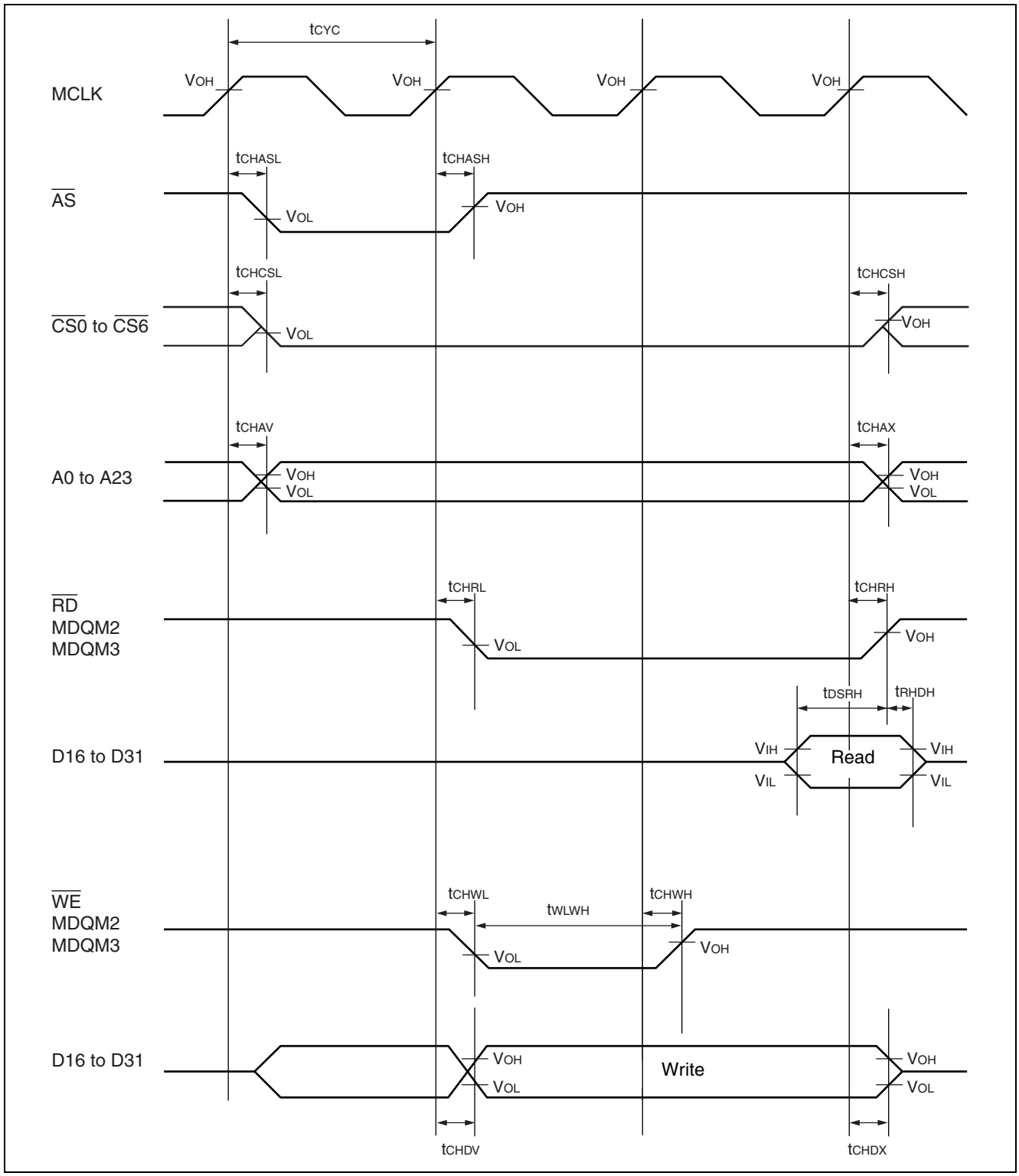
(V_{DDE} = AVcc = 3.0 V to 3.6 V, V_{DDI} = 1.65 V to 1.95 V, Vss = AVss = 0 V, Ta = –10 °C to + 70 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
$\overline{AS}$ delay time	t_{CHASL}	MCLK $\overline{AS}$	—	0.8	6	ns	
	t_{CHASH}						
$\overline{CS}$ delay time	t_{CHCSL}	MCLK $\overline{CS0}$ to $\overline{CS6}$		0.8	6	ns	
	t_{CHCSH}						
Address delay time	t_{CHAV}	MCLK A0 to A23		0.8	6	ns	
	t_{CHAX}						
$\overline{RD}$ delay time	t_{CHRL}	MCLK $\overline{RD}$		0.8	6	ns	
	t_{CHRH}						
$\overline{RD}$ minimum pulse width	t_{RLRH}	$\overline{RD}$		t_{CYC} – 6	—	ns	*
Data setup → $\overline{RD}$ ↑ time	t_{DSRH}	$\overline{RD}$ D16 to D31		10	—	ns	
$\overline{RD}$ ↑ → data hold time	t_{RHDH}			0	—	ns	
$\overline{WE}$, MDQM2, MDQM3 delay time	t_{CHWL}	MCLK $\overline{WE}$ MDQM2, MDQM3		0.8	6	ns	
	t_{CHWH}						
$\overline{WE}$, MDQM2, MDQM3 minimum pulse width	t_{WLWH}	$\overline{WE}$ MDQM2, MDQM3		t_{CYC} – 6	—	ns	*
MCLK ↑ → data output time	t_{CHDV}	MCLK D16 to D31		0.8	6	ns	
MCLK ↑ → data hold time	t_{CHDX}			0.8	6	ns	

* : When the bus timing is delayed by automatic wait insertion or RDY input, add the time (t_{CYC} × the number of cycles added for the delay) to this rating.

Note: When the external load capacitance C = 30 pF.


tCYC
MCLK
VOH
VOH
VOH
VOH
tCHCSL
tCHCSH
CS0 to CS6
VOL
VOH
tCHAV
tCHAX
A0 to A23
VOH
VOL
VOH
VOL
tCHRL
tCHRH
tRLRH
RD
MDQM2
MDQM3
VOL
VOH
tDSRH
tRHDH
VIH
Read
VIH
D16 to D31
VIL
VIL
tCHWL
tCHWH
tWLWH
WE
MDQM2
MDQM3
VOL
VOH
VOH
Write
VOH
D16 to D31
VOL
VOL
tCHDV
tCHDX


tCYC
MCLK
VOH
VOH
VOH
VOH
tCHASL
tCHASH
AS
VOL
VOH
tCHCSL
tCHCSH
CS0 to CS6
VOL
VOH
tCHAV
tCHAX
A0 to A23
VOH
VOL
VOH
VOL
tCHRL
tCHRH
RD
MDQM2
MDQM3
VOL
VOH
tDSRH
tRHDH
D16 to D31
VIH
VIL
Read
VIH
VIL
tCHWL
tWLWH
tCHWH
WE
MDQM2
MDQM3
VOL
VOH
D16 to D31
VOH
VOL
Write
VOH
VOL
tCHDV
tCHDX

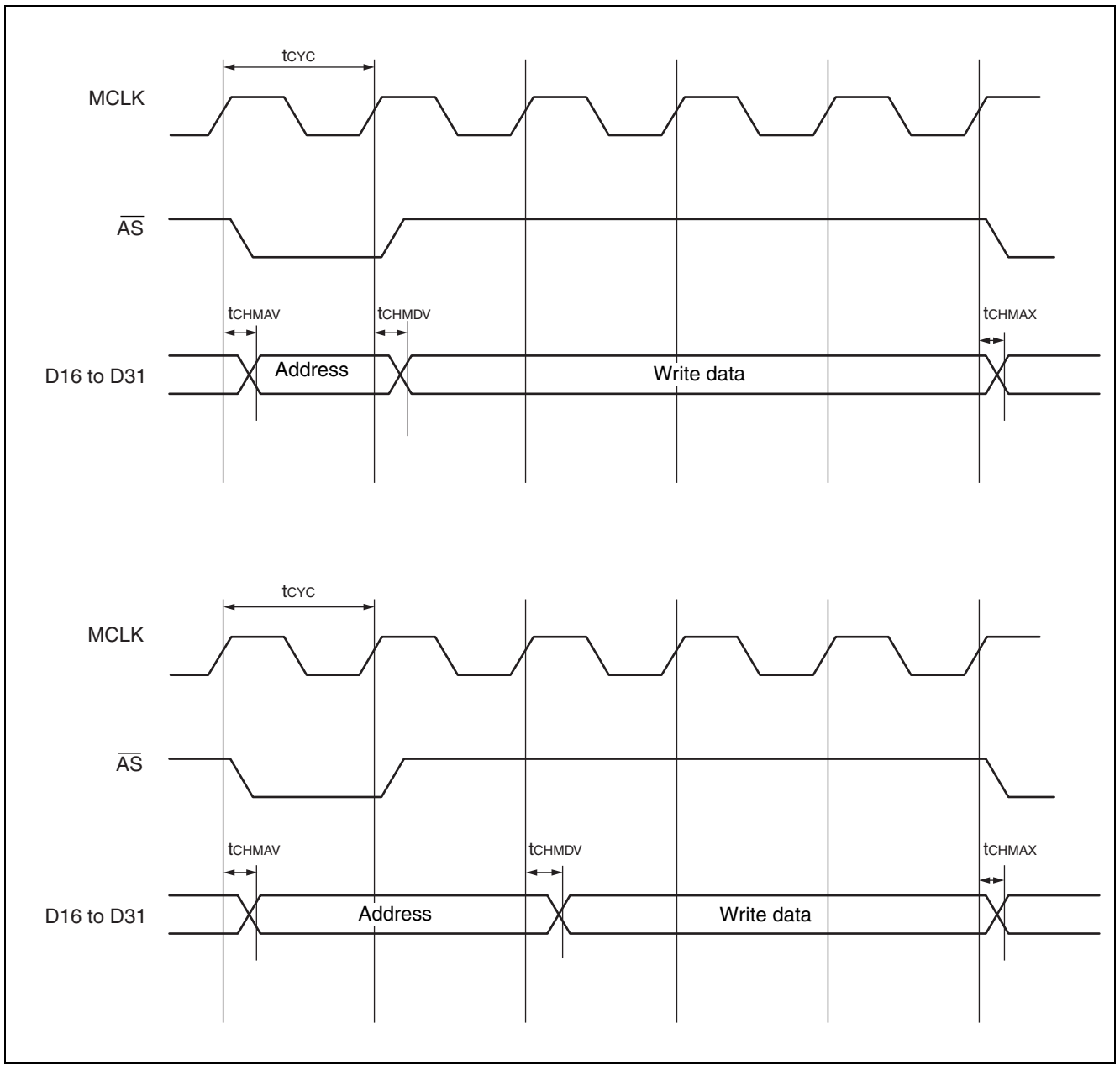
(6) Multiplexed Bus Access Read/Write Operation

(V_{DDE} = AVcc = 3.0 V to 3.6 V, V_{DDI} = 1.65 V to 1.95 V, Vss = AVss = 0 V, Ta = –10 °C to + 70 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
MCLK ↑ → D16 to D31 address delay time	t_{CHMAV} t_{CHMAX}	MCLK D16 to D31 (address)	—	0.8	10	ns
MCLK ↑ → D16 to D31 data delay time	t_{CHMDV}			0.8	10	ns

Notes: • Ratings other than those listed here are the same as the standard bus interface ratings.

• When the external load capacitance C = 30 pF.

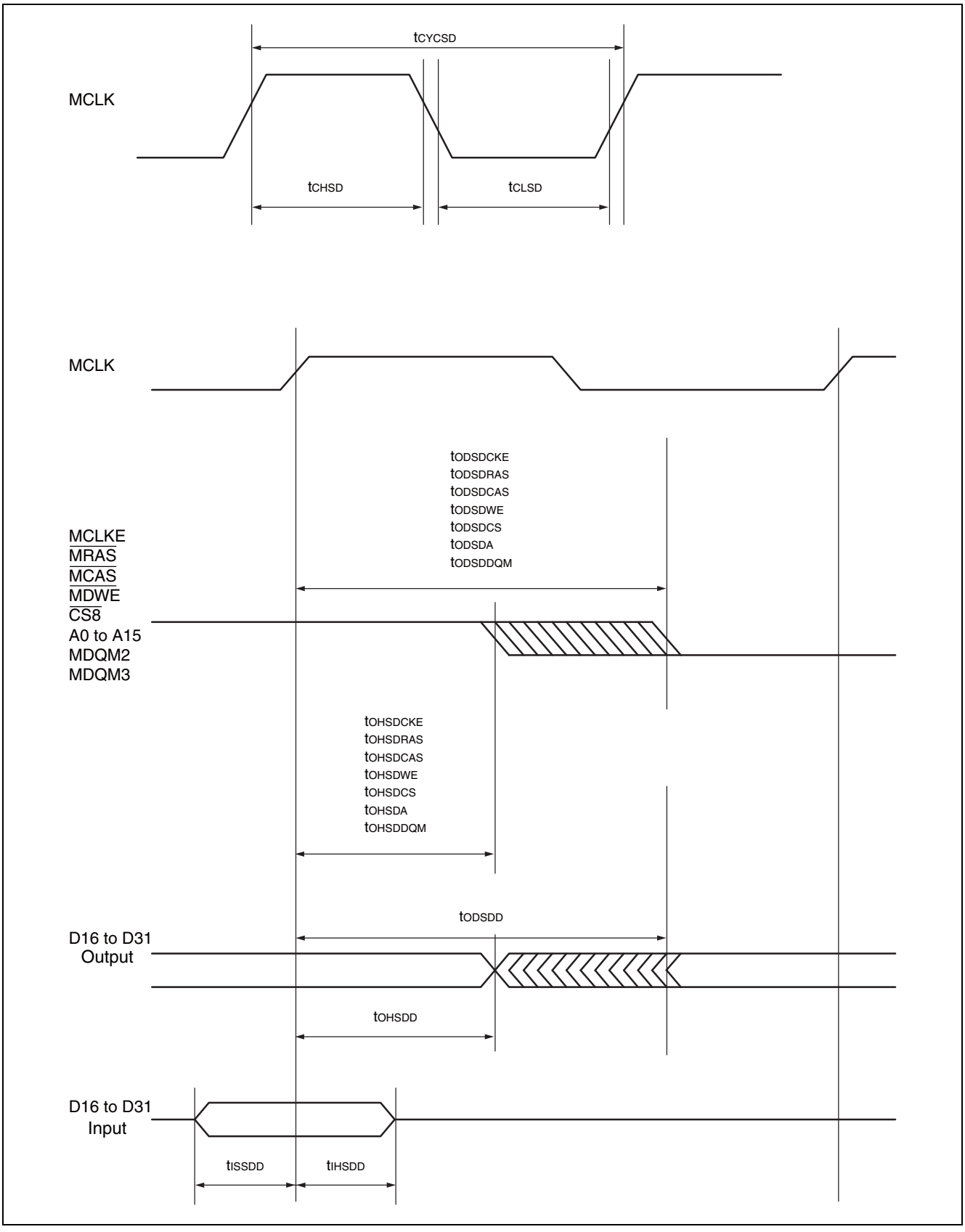


(7) SDRAM Timing

(V_{DDE} = AVcc = 3.0 V to 3.6 V, V_{DDI} = 1.65 V to 1.95 V, Vss = AVss = 0 V, Ta = –10 °C to + 70 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Output clock cycle time	t_{CYCSD}	MCLK	—	—	80	MHz
"H" level clock pulse width	t_{CHSD}			4	—	ns
"L" level clock pulse width	t_{CLSD}			4	—	ns
MCLK ↑ → output delay time	$t_{ODSDCKE}$	MCLKE	—	—	6	ns
Output hold time	$t_{OHSDCKE}$			0.8	—	ns
MCLK ↑ → output delay time	$t_{ODSDRAS}$	$\overline{MRAS}$		—	6	ns
Output hold time	$t_{OHSDRAS}$			0.8	—	ns
MCLK ↑ → output delay time	$t_{ODSDCAS}$	$\overline{MCAS}$		—	6	ns
Output hold time	$t_{OHSDCAS}$			0.8	—	ns
MCLK ↑ → output delay time	t_{ODSDWE}	$\overline{MDWE}$		—	6	ns
Output hold time	t_{OHSDWE}			0.8	—	ns
MCLK ↑ → output delay time	t_{ODSDCS}	$\overline{CS8}$		—	6	ns
Output hold time	t_{OHSDCS}			0.8	—	ns
MCLK ↑ → output delay time	t_{ODSDA}	A0 to A15		—	6	ns
Output hold time	t_{OHSDA}			0.8	—	ns
MCLK ↑ → output delay time	$t_{ODSDDQM}$	MDQM2 MDQM3		—	6	ns
Output hold time	$t_{OHSDDQM}$			0.8	—	ns
MCLK ↑ → output delay time	t_{ODSDD}	D16 to D31		—	6	ns
Output hold time	t_{OHSDD}			0.8	—	ns
Data input setup time	t_{ISSDD}	D16 to D31	—	6	—	ns
Data input hold time	t_{IHSDD}			0.8	—	ns

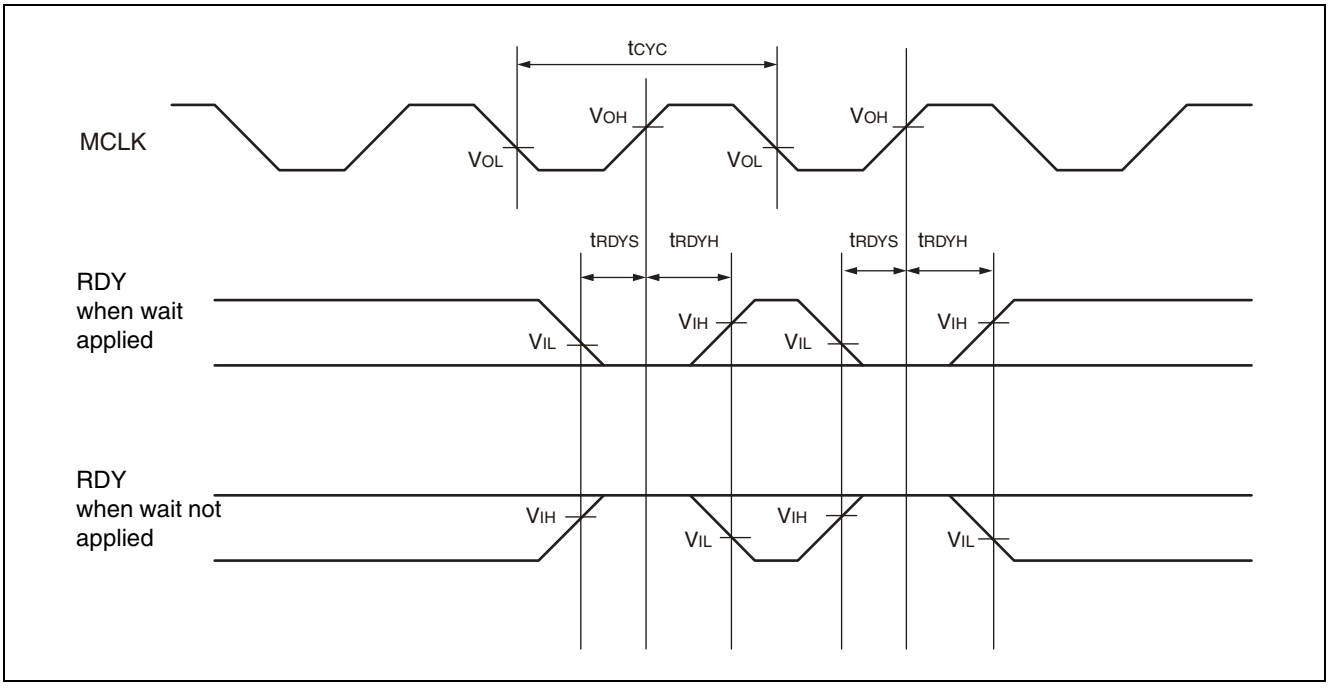
Note: When the external load capacitance C = 30 pF.


tCYCSD
MCLK
tCHSD
tCLSD
MCLK
tODSDCKE
tODSDRAS
tODSDCAS
tODSDWE
tODSDCS
tODSDA
tODSDDQM
MCLKE
MRAS
MCAS
MDWE
CS8
A0 to A15
MDQM2
MDQM3
tOHSDCKE
tOHSDRAS
tOHSDCAS
tOHSDWE
tOHSDCS
tOHSDA
tOHSDDQM
tODSDD
D16 to D31
Output
tOHSDD
D16 to D31
Input
tISSDD
tIHSDD

(8) Ready Input Timings

(V_{DDE} = AVcc = 3.0 V to 3.6 V, V_{DDI} = 1.65 V to 1.95 V, Vss = AVss = 0 V, Ta = –10 °C to + 70 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
RDY setup time → MCLK ↑	t_{RDYS}	MCLK RDY	—	6	—	ns
MCLK ↑ → RDY hold time	t_{RDYH}			0	—	ns



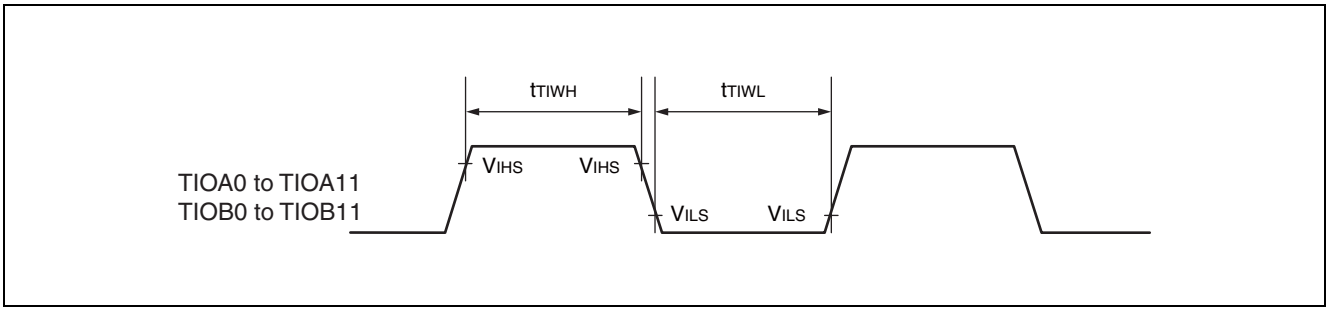
(9) Base Timer Input Timing

• Timer input timing

(V_{DDE} = AVcc = 3.0 V to 3.6 V, V_{DDI} = 1.65 V to 1.95 V, Vss = AVss = 0 V, Ta = –10 °C to + 70 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	TIOA0 to TIOA11 TIOB0 to TIOB11	—	2 t_{CYCP}*	—	ns

* : t_{CYCP} represents the peripheral clock cycle time.



(10) UART Timing

(V_{DDE} = AVcc = 3.0 V to 3.6 V, V_{DDI} = 1.65 V to 1.95 V, Vss = AVss = 0 V, Ta = –10 °C to + 70 °C)

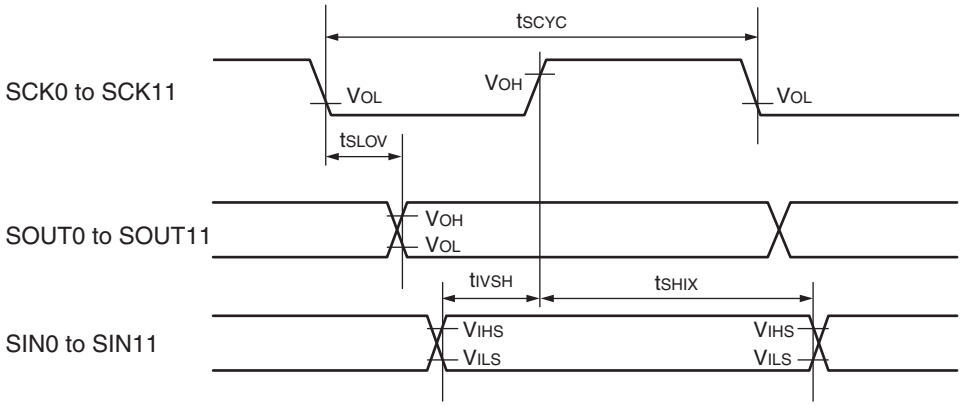
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK11	Internal shift clock operation	4 t_{CYCP}*	—	ns
SCK ↓ → SOUT delay time	t_{SLOV}	SCK0 to SCK11 SOUT0 to SOUT11		– 20	+ 20	ns
Valid SIN → SCK ↑	t_{IVSH}	SCK0 to SCK11 SIN0 to SIN11		30	—	ns
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK0 to SCK11 SIN0 to SIN11		20	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK0 to SCK11	External shift clock operation	2 t_{CYCP}*	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK0 to SCK11		2 t_{CYCP}*	—	ns
SCK ↓ → SOUT delay time	t_{SLOV}	SCK0 to SCK11 SOUT0 to SOUT11		—	30	ns
Valid SIN → SCK ↑	t_{IVSH}	SCK0 to SCK11 SIN0 to SIN11		20	—	ns
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK0 to SCK11 SIN0 to SIN11		20	—	ns

* : t_{CYCP} represents the peripheral clock cycle time.

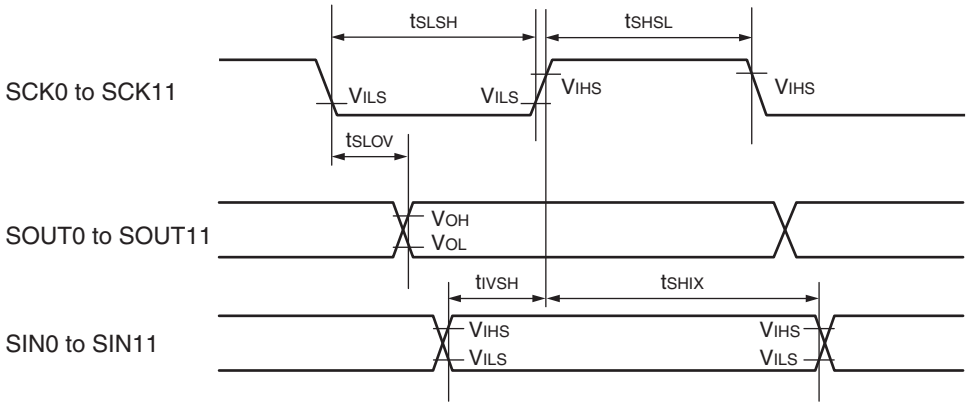
Notes: • The above standards are the AC ratings for CLK synchronous mode.

• When the external load capacitance C = 50 pF.

• Internal shift clock mode



• External shift clock mode



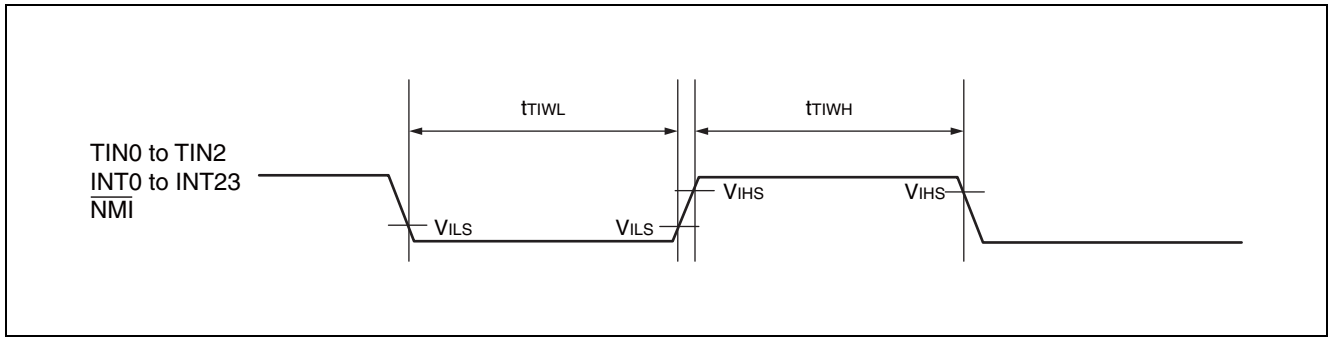
(11) Reload Timer Event Input, Interrupt Input Timing

(V_{DDE} = AVcc = 3.0 V to 3.6 V, V_{DDI} = 1.65 V to 1.95 V, Vss = AVss = 0 V, Ta = –10 °C to + 70 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH} t_{TIWL}	TIN0 to TIN2	—	2 t_{CYCP}	—	ns	*1
		INT0 to INT23 $\overline{NMI}$		3 t_{CYCP}	—	ns	*1
				1.0	—	µs	*2

*1 : t_{CYCP} represents the peripheral clock cycle time, except when in stop mode.

*2 : When in stop mode.

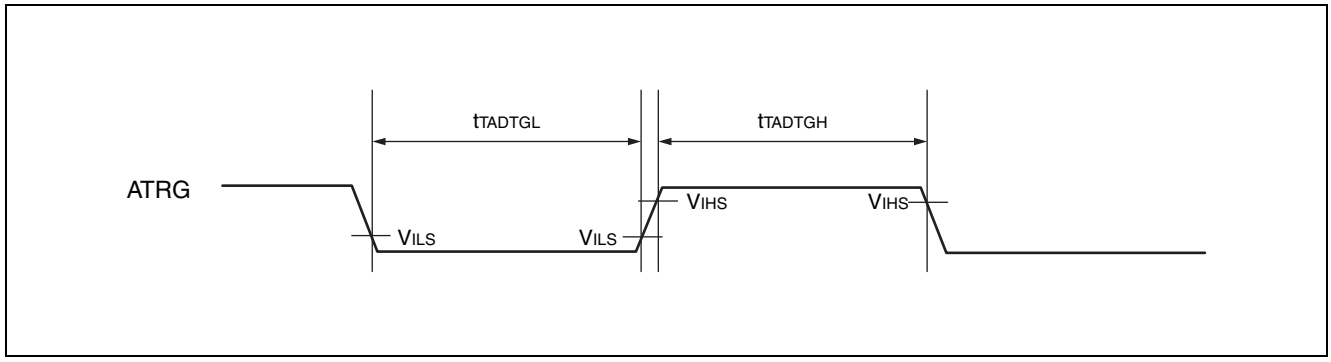


(12) A/D Converter Trigger Input Timing

(V_{DDE} = AVcc = 3.0 V to 3.6 V, V_{DDI} = 1.65 V to 1.95 V, Vss = AVss = 0 V, Ta = –10 °C to + 70 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
A/D converter trigger input	t_{TADTGL} t_{TADTGH}	ATRG	—	2 t_{CYCP}	—	ns	*

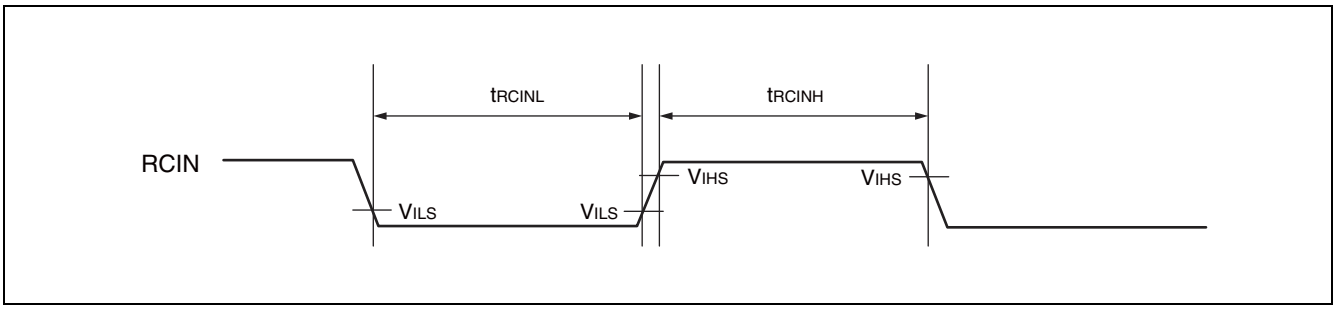
* : t_{CYCP} represents the peripheral clock cycle time.



(13) Remote Control and HDMI-CEC Input Timing

(V_{DDE} = AVcc = 3.0 V to 3.6 V, V_{DDI} = 1.65 V to 1.95 V, Vss = AVss = 0 V, Ta = –10 °C to + 70 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Remote receiver	t_{RCINH} t_{RCINL}	RCIN	—	62	—	µs	2 clocks or more of the count clock



(14) I²C Timing

• When operating in master mode

(V_{DDE} = AVcc = 3.0 V to 3.6 V, V_{DDI} = 1.65 V to 1.95 V, Vss = AVss = 0 V, Ta = –10 °C to + 70 °C)

Parameter	Symbol	Pin name	Condition	Typical mode		High-speed mode*3		Unit	Remarks
				Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	SDA0 to SDA11, SCL0 to SCL11	R = 1 kΩ, C = 50 pF*4	0	100	0	400	kHz	
"L" period of SCL clock	t_{LOW}			4.7	—	1.3	—	µs	
"H" period of SCL clock	t_{HIGH}			4.0	—	0.6	—	µs	
Bus free time between "STOP condition" and "START condition"	t_{BUS}			4.7	—	1.3	—	µs	
SCL ↓ → SDA output delay time	t_{DLDAT}			—	5 t_{CYCP}*1	—	5 t_{CYCP}*1	ns	
"Repeated START condition" setup time SCL ↑ → SDA ↓	t_{SUSTA}			4.7	—	0.6	—	µs	
"Repeated START condition" hold time SDA ↓ → SCL ↓	t_{HDSTA}			4.0	—	0.6	—	µs	The first clock pulse is generated after this.
"STOP condition" set-up time SCL ↑ → SDA ↑	t_{SUSTO}			4.0	—	0.6	—	µs	
SDA data input hold time (vs. SCL ↓)	t_{HDDAT}			2 t_{CYCP}*1	—	2 t_{CYCP}*1	—	µs	
SDA data input setup time (vs. SCL ↑)	t_{SUDAT}			250	—	100*2	—	ns	

*1 : t_{CYCP} is peripheral clock cycle time.

*2 : A high-speed mode I²C bus device can be used on a standard mode I²C bus system. In this case, the device must satisfy the requirement of "$t_{SUDAT} \geq 250$ ns".
When a device does not extend the "L" period of the SCL signal, the next data must be output to the SDA line within 1250 ns (maximum SDA/SCL rise time + t_{SUDAT}) from when the SCL line is released.

*3 : For use at over 100 kHz, set the resource clock to 6 MHz or higher.

*4 : R and C represent the pull-up resistance and load capacitance of the SCL and SDA output lines, respectively.

• When operating in slave mode

(V_{DDE} = AVcc = 3.0 V to 3.6 V, V_{DDI} = 1.65 V to 1.95 V, Vss = AVss = 0 V, Ta = –10 °C to + 70 °C)

Parameter	Symbol	Pin name	Condition	Typical mode		High-speed mode*3		Unit	Remarks
				Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	SDA0 to SDA11, SCL0 to SCL11	R = 1 kΩ, C = 50 pF*4	0	100	0	400	kHz	
"L" period of SCL clock	t_{LOW}			4.7	—	1.3	—	µs	
"H" period of SCL clock	t_{HIGH}			4.0	—	0.6	—	µs	
SCL ↓ → SDA output delay time	t_{DLDAT}			—	5 t_{CYCP}*1	—	5 t_{CYCP}*1	ns	
Bus free time between "STOP condition" and "START condition"	t_{BUS}			4.7	—	1.3	—	µs	
SDA data input hold time (vs. SCL ↓)	t_{HDDAT}			2 t_{CYCP}*1	—	2 t_{CYCP}*1	—	µs	
SDA data input setup time (vs. SCL ↑)	t_{SUDAT}			250	—	100*2	—	ns	
"Repeated START condition" setup time SCL ↑ → SDA ↓	t_{SUSTA}			4.7	—	0.6	—	µs	
"Repeated START condition" hold time SDA ↓ → SCL ↓	t_{HDSTA}			4.0	—	0.6	—	µs	The first clock pulse is generated after this.
"STOP condition" set-up time SCL ↑ → SDA ↑	t_{SUSTO}			4.0	—	0.6	—	µs	

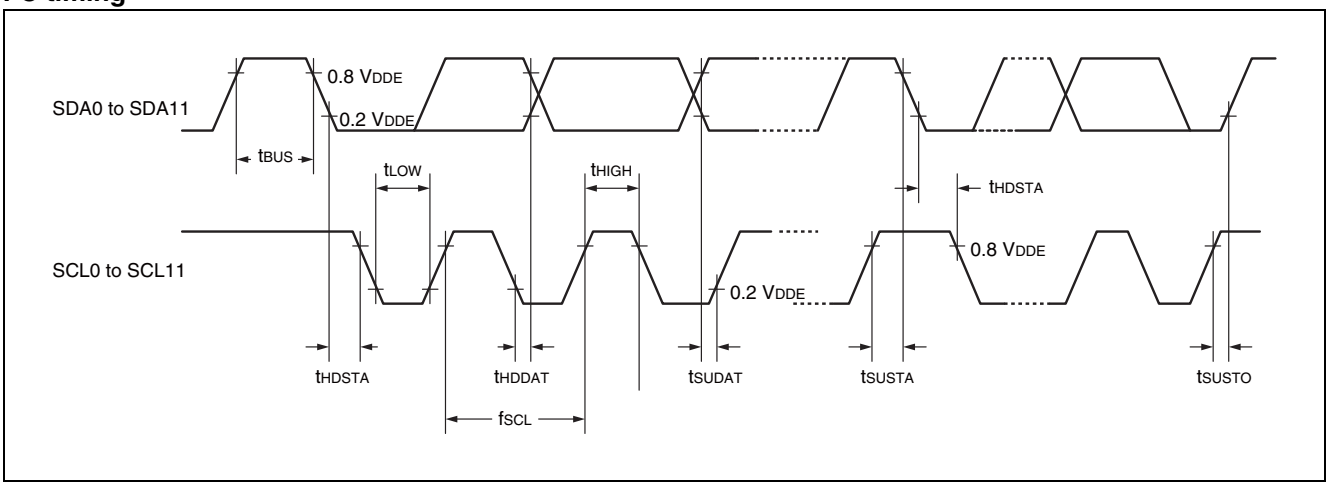
*1 : t_{CYCP} is peripheral clock cycle time.

*2 : A high-speed mode I^2C bus device can be used on a standard mode I^2C bus system. In this case, the device must satisfy the requirement of "$t_{SUDAT} \geq 250$ ns".
When a device does not extend the "L" period of the SCL signal, the next data must be output to the SDA line within 1250 ns (maximum SDA/SCL rise time + t_{SUDAT}) from when the SCL line is released.

*3 : For use at over 100 kHz, set the resource clock to 6 MHz or higher.

*4 : R and C represent the pull-up resistance and load capacitance of the SCL and SDA output lines, respectively.

I²C timing


SDA0 to SDA11
SCL0 to SCL11
0.8 VDDE
0.2 VDDE
tBUS
tLOW
tHIGH
tHDSTA
tHDSTA
tHDDAT
tSUDAT
tSUSTA
tSUSTO
fSCL

5. Electrical Characteristics for the A/D Converter

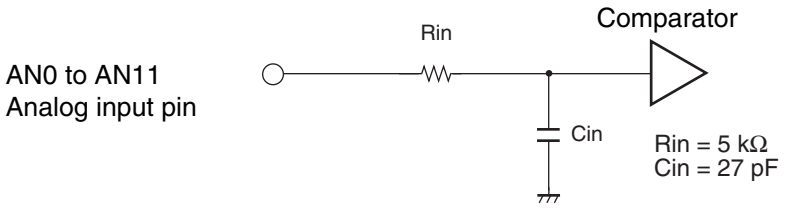
(V_{DDE} = AVcc = 3.0 V to 3.6 V, V_{DDI} = 1.65 V to 1.95 V, Vss = AVss = 0 V Ta = –10 °C to + 70 °C)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Resolution	—	—	10	bit	
Total error*1	—	—	± 5.5	LSB	When AVcc = 3.3 V, AVRH = 3.3 V
Linearity error*1	—	—	± 3.5	LSB	
Differential linear error*1	—	—	± 2.0	LSB	
Zero transition voltage*1	—	—	± 6.0	LSB	
Full transition voltage*1	AVRH – 5.5	—	AVRH + 3.0	LSB	
Conversion time	8.1*2	—	—	µs	When PCLK (peripheral clock) = 40 MHz
Power supply current (analog + digital)	—	3.6	—	mA	
	—	—	5	µA	At power-down*3
Reference power supply current (between AVRH and AV_{SS})	—	470	—	mA	When AVRH = 3.0 V, AVss = 0.0 V
	—	—	10	µA	At power-down*3
Analog input capacitance	—	—	27	pF	
Interchannel disparity	—	—	4	LSB	

*1 : Measured in the CPU sleep state

*2 : Depending on the clock cycle supplied to peripheral resources.

*3 : The current when the CPU is in stop mode and the A/D converter is not operating.



The output impedance of the external circuit connected to the analog input affects the sampling time of the A/D converter. Design the output impedance of the output circuit such that the required sampling time is less than the value of T_S calculated from the following equation.

$$Ts = (Rin + Rext) \times Cin \times 8$$

Ts : Sampling time

Rin : Input resistance of A/D = 5 kΩ

Cin : Input capacitance of A/D = 27 pF

Rext : Output impedance of external circuit

If the sampling time is taken to be 5.9 µs:

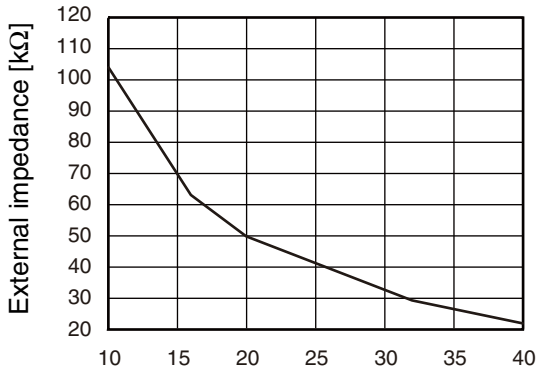
$$5.9\ \mu s = (5\ k\Omega + Rext) \times 27\ pF \times 8$$

$$\therefore Rext = 22.3\ k\Omega$$

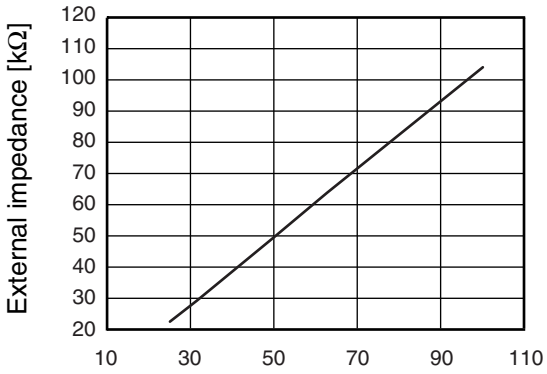
And the impedance of the external circuit therefore needs to be 22 kΩ or less.

- The relationship between peripheral clock and external impedance

Peripheral clock frequency and external impedance

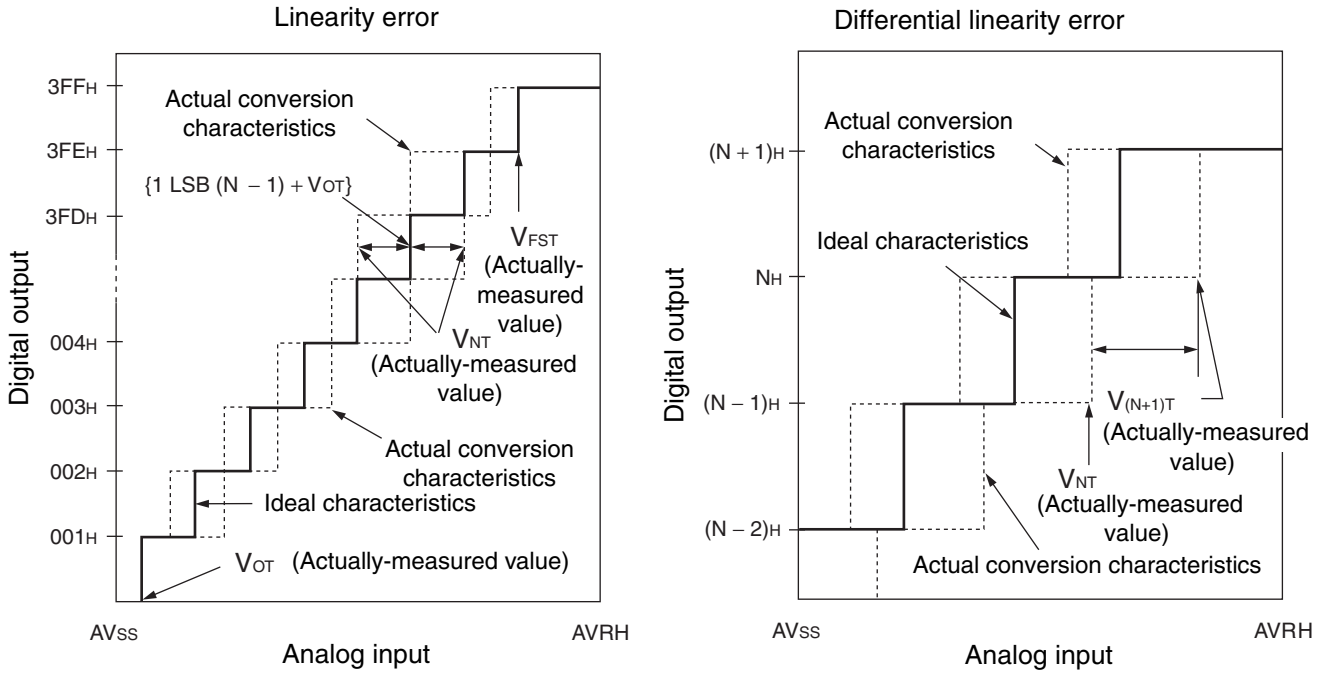


Peripheral clock cycle and external impedance



•Definition of 10-bit A/D Converter Terms

- Resolution : Analog variation that is recognized by an A/D converter.
- Linearity error : Deviation of the line between the zero-transition point (0000000000←→0000000001) and the full-scale transition point (1111111110←→1111111111) from the actual conversion characteristics.
- Differential linearity error : Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.
- Total error : Difference between the actual value and the theoretical value. The total error includes zero transition error, full-scale transition error, and linear error.



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB'}}\ [\text{LSB}]$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ [\text{LSB}]$$

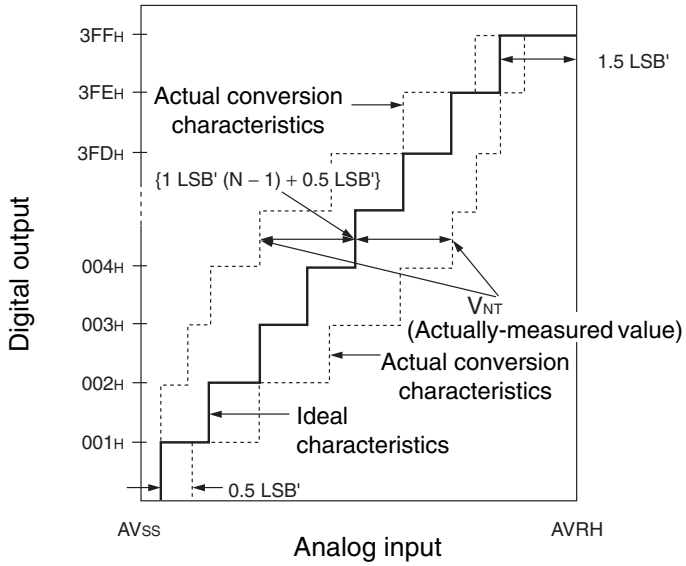
$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}$$

N : A/D converter digital output value.
V_{OT} : Voltage at which the digital output changes from 000_H to 001_H.
V_{FST} : Voltage at which the digital output changes from $3FE_H$ to $3FF_H$.
V_{NT} : Voltage at which the digital output changes from $(N - 1)_H$ to N_H.

(Continued)

(Continued)

Total error



$$1\ \text{LSB'}\ (\text{Ideal value}) = \frac{\text{AVRH} - \text{AV}_{SS}}{1024}\ [\text{V}]$$

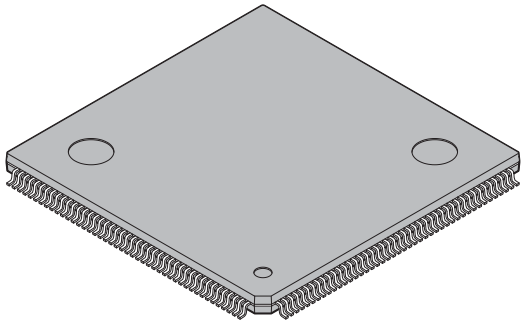
$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB'} \times (\text{N} - 1) + 0.5\ \text{LSB'}\}}{1\ \text{LSB'}}$$

N : A/D converter digital output value.
V_{NT} : Voltage at which the digital output changes from $(N + 1)_H$ to N_H.
V_{OT}' (Ideal value) = AV_{SS} + 0.5 LSB [V]
V_{FST}' (Ideal value) = AVRH – 1.5 LSB [V]

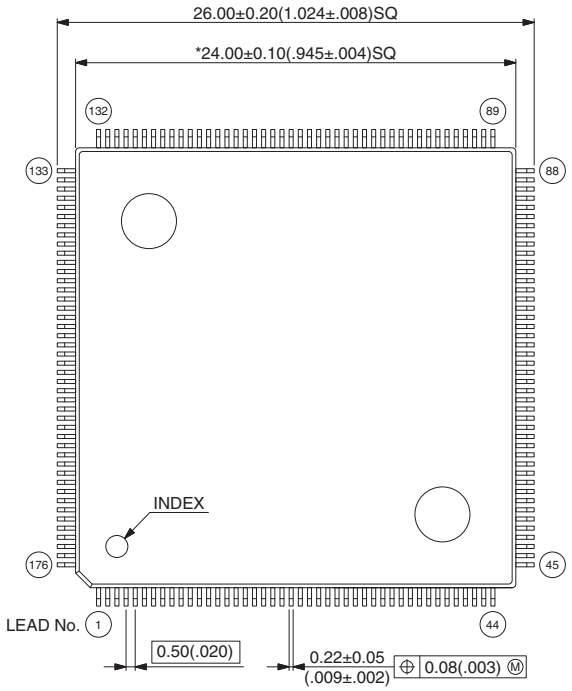
■ ORDERING INFORMATION

Part number	Package
MB91605APMC	176-pin plastic LQFP (FPT-176P-M07)

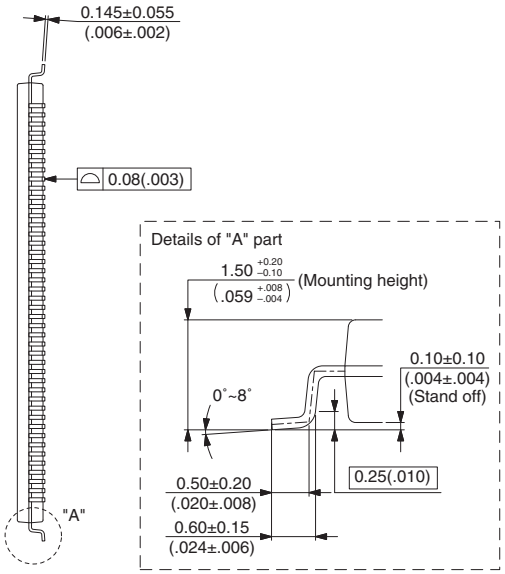
■ PACKAGE DIMENSION

176-pin plastic LQFP		
 (FPT-176P-M07)	Lead pitch	0.50 mm
	Package width × package length	24.0 × 24.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Code (Reference)	P-LQFP-0176-2424-0.50

176-pin plastic LQFP
(FPT-176P-M07)



Note 1) * : Values do not include resin protrusion.
Resin protrusion is +0.25(.010)Max(each side).
Note 2) Pins width and pins thickness include plating thickness
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

■ MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
24	■ MEMORY SPACE 2. Memory Map	Changed the following address. $10040000_H \rightarrow 10000000_H$
		Added below note to “External mirror area”. *: The mirror of external bus interface register can be found at 40002000_H to $40002FFF_H$.
46	■ ELECTRICAL CHARACTERISTICS 4. AC Characteristics (1) Main Clock Input Standard	Added “When using external clock” to the remarks for “Input clock cycle” and “Input clock pulse width”.
50, 51	(5) External Bus Access Read/Write Operation	Replaced the Timing chart.

The vertical lines marked in the left side of the page show the changes.

MEMO

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