FUJITSU MICROELECTRONICS
DATA SHEET

DS07-16801-3E

32-bit Microcontroller

CMOS

FR60Lite MB91270 Series

MB91F273(S)/MB91V280

■ DESCRIPTION

The MB91270 series is single chip microcontroller that builds various I/O resources and the bus control mechanisms into by using 32-bit efficient RISC CPU for the built-in control being demanded for CPU processing high performance/high-speed. RAM (for reading data) is included in order to support CPU to access to the vast address space and to speed up the execution of CPU instructions. This series is optimized to the embedded applications; automotive applications such as car audio or car air-conditioning equipment that require high-performance CPU processing power.
It is designed based on the FR-family* CPU.

* : FR, the abbreviation of FUJITSU RISC controller, is a line of products of Fujitsu Microelectronics Limited.

■ FEATURES

- FR CPU characteristics
  - 32-bit RISC, load/store architecture with a five-stage pipeline
  - Maximum operating frequency: 32 MHz (using the PLL at an oscillation frequency of 4 MHz)
  - 16-bit fixed length instructions (basic instructions), 1 instruction per cycle
  - Function entry/exit instructions, multiple - register load/store instructions :
    Instructions adapted for high - level languages
  - Memory-to-memory transfer, bit manipulation, barrel shift instruction etc.:
    Instruction optimized for embedded applications

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For the information for microcontroller supports, see the following web site.

http://edevice.fujitsu.com/micom/en-support/

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- Register interlock functions:
  Easier assembler coding enabled
- Built-in multiplier supported at the instruction level
  Signed 32-bit multiplication: 5 cycles
  Signed 16-bit multiplication: 3 cycles
- Interrupt (PC, PS save): 6 cycles, 16 priority levels
- Harvard architecture allowing program access and data access to be executed simultaneously
- Instruction compatible with FR family

• External bus interface
- Maximum operating frequency: 16 MHz
- Can output full 24-bit address range (16 Mbyte space)
- 8,16-bit data output
- Unused data/address pin can be used as general-purpose I/O ports.
- Capable of chip select output for completely independent four areas settable in 64 Kbytes minimum.
- Supports the following memory interfaces
  SRAM, ROM/Flash
- Basic bus cycle: 2 cycles
- Programmable automatic wait cycle generation function capable of inserting wait cycles for each area
- RDY input for external wait cycles

• Built-in memory

	MB91V280	MB91F273 (S)
ROM/Flash	External SRAM	Flash 512 Kbytes
F-bus RAM	48 Kbytes	24 Kbytes

The peripheral circuits are described below.

Refer to “■PRODUCT LINEUP” for the number of available channels on each model.

• DMAC (DMA Controller)
- Capable of simultaneous operation of up to five channels
- Two forwarding factors (internal peripheral/software)

• Bit search module (for REALOS)

Search for the first position of the bit “1”/ “0” changed in one word from the MSB

• LIN UARTs (LIN-UART) : Up to 7 channels
- Asynchronous (start-stop synchronous) communications, clock synchronous communications
- Synch-Break detection
- Built-in baud rate generator on each channel
- Supports SPI (mode 2: Clock synchronous communication mode)

• CAN CONTROLLERS : 3 channels (Max)
- High-speed transfer : 1 Mbps
- 32 message buffer (128 message buffer on the MB91V280)

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- Various timers
  - 16-bit reload timer : 3 channels (including one channel for REALOS)
    The internal clock can be divided by 2, 8, or 32
  - 16-bit free-running timer: 4 channels
    Output compare module: 8 channels
    Input capture module: 8 channels
  - 8/16-bit PPG timer: 8-bit x 16 channels or 16-bit x 8 channels

- Interrupt controller
  - Interrupt from internal peripheral
  - Software-selectable priority level (16 levels)

- D/A converter : 2 channels
  8-bit or 10-bit resolution, R-2R type

- A/D converter: 24 channels (MB91V280 has an additional module with eight more channels)
  - 10-bit resolution
  - Successive approximation conversion type
    Conversion time : 3 μs
  - Conversion mode (single conversion mode, continuous conversion mode)
  - Activation source (software, external trigger, peripheral interrupt)

- Other interval timer/counter
  - 8/16-bit up down counter :
    8 bits × 4 channels or 16 bits × 2 channels
  - 16-bit timebase timer / watchdog timer

- I^2C bus interface (400 kbps): 3 channels
  - Master/slave sending and receiving
  - Arbitration and clock synchronization

- Hardware watchdog
  Interval time: 569 ms (Min), 771 ms (Max)
  (Use of self-oscillation circuit with timing (100 kHz))

- I/O port
  - Pull-up/pull-down can be controlled independently for each pin.
  - The input level for each pin can be set to either CMOS Schmitt trigger levels or CMOS automotive Schmitt trigger levels.
  - The pin level can be read directly.
  - Max 82 ports

- Other features
  - Internal oscillator circuit as clock source, allowing PLL multiplication to be selected
  - $\overline{\text{INIT}}$ is prepared as a reset pin.
  - Watchdog timer reset, software reset
  - Available low-power consumption modes are stop mode, sleep mode, and real time clock mode.
    Supports low-power consumption operation with CPU operating at 32 kHz (“s” without only product).
  - Gear function
  - Built-in timebase timer
  - Wild register

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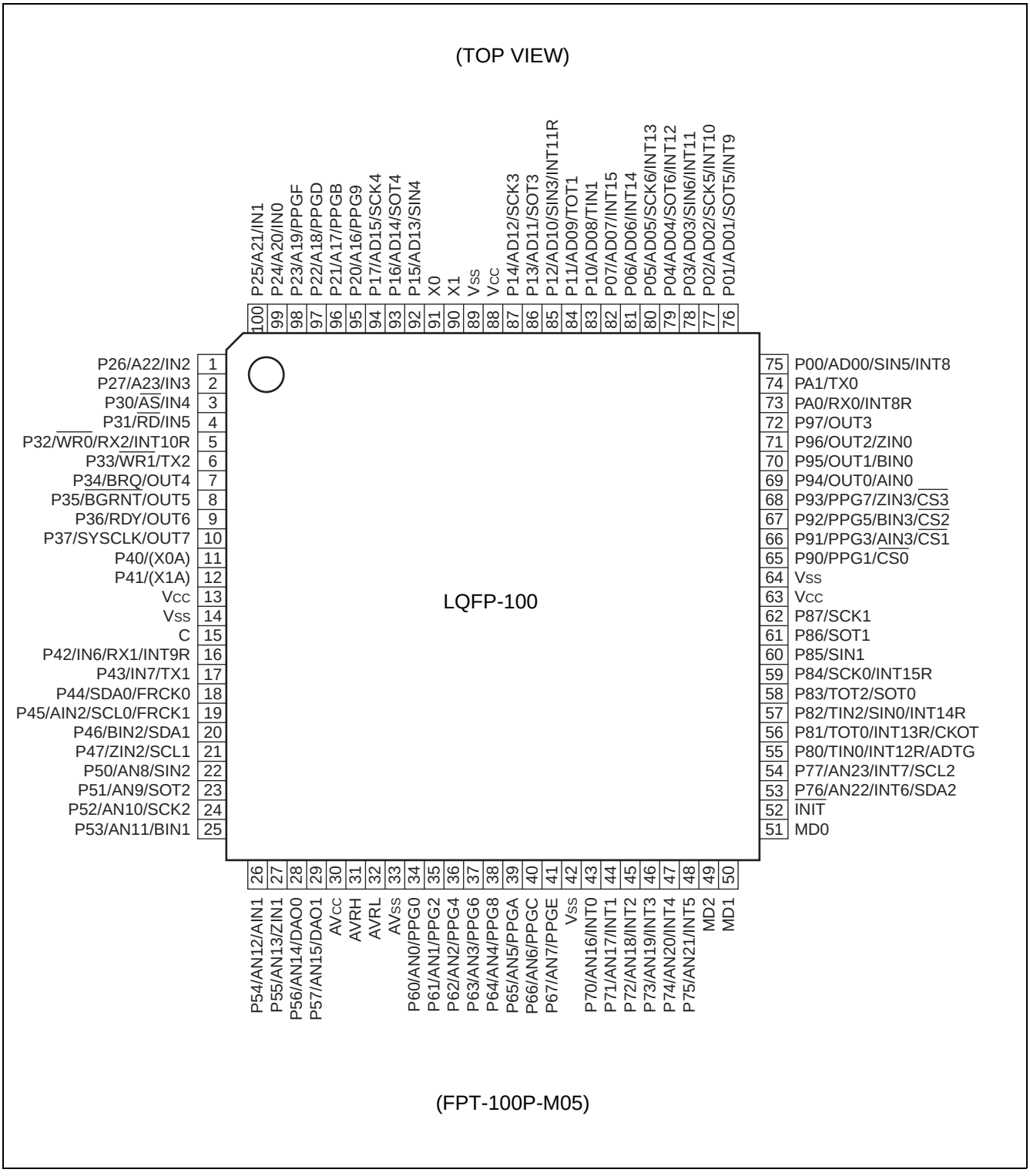
- Output clock (clock monitor)
- Clock Modulator
- Package PGA-401, LQFP-100
- CMOS technology (0.35 µm)
- Power supply voltage: 3.5 V to 5.5 V
  The 3.3 V supply to internal circuits is generated by an internal step-down circuit.

■ PRODUCT LINEUP

Kind / Parameter	MB91F273 (S)	MB91V280
Package	LQFP-100	PGA-401
Built-in ROM/ Flash	Flash 512 Kbytes	External SRAM
RAM	24 Kbytes	48 Kbytes
External bus	Address : 24 bits Data : 16 bits (Multiplex only)	Address : 24 bits Data : 16 bits
External interrupt	16 channels	40 channels
DMAC (DMA Controller)	5 channels	
Clock modulator	Yes	
Clock supervisor	No	Yes
Clock monitor	Yes	
32 kHz sub-clock	Option (Models without S-suffix part number only)	Yes
Real time clock	Yes	
CAN controllers	1 channel (32 message buffer)	3 channels (128 message buffer)
LIN UARTs (LIN-UART)	7 channels	
I^2C interface	3 channels	
16-bit reload timer	3 channels	
8/16-bit up down counter	2 channels	
16-bit free-run timer	4 channels	
Input capture	8 channels	
Output compare	8 channels	
8/16-bit PPG	16-bit × 8 channels 8-bit × 16 channels	
10-bit A/D converter	24 channels	24 channels + 8 channels
8/10-bit D/A converter	No	2 channels
Pin pull-up/down	Refer to “■ PIN FUNCTION”	All pins
Input level selector	Refer to “■ PIN FUNCTION”	All pins
Debugging support	Wild register	DSU4

■ PIN ASSIGNMENT



■ PIN FUNCTION

Pin No.	Pin name	Function name	I/O circuit type*	Function
90	X1	X1	OB	Oscillator output pin
91	X0	X0	OA	Oscillator input pin
52	$\overline{INIT}$	$\overline{INIT}$	N	Reset input pin (“L” active)
49 to 51	MD2 to MD0	MD2 to MD0	J	Operation mode select input pins. Connect to V_{CC} or V_{SS} directly.
Port 0				
75	P00/AD00/ SIN5/INT8	P00	T	General-purpose I/O port. This function is enabled in single-chip mode.
		AD00		External address/data bus I/O pin bit 0 This function is enabled when the external bus is enabled.
		INT8		External interrupt request 8 input pin
		SIN5		Serial data input pin for LIN-UART5
76	P01/AD01/ SOT5/INT9	P01	T	General-purpose I/O port. This function is enabled in single-chip mode.
		AD01		External address/data bus I/O pin bit 1 This function is enabled when the external bus is enabled.
		INT9		External interrupt request 9 input pin
		SOT5		Serial data output pin for LIN-UART5
77	P02/AD02/ SCK5/INT10	P02	T	General-purpose I/O port. This function is enabled in single-chip mode.
		AD02		External address/data bus I/O pin bit 2 This function is enabled when the external bus is enabled.
		INT10		External interrupt request 10 input pin
		SCK5		Clock I/O pin for LIN-UART5
78	P03/AD03/ SIN6/INT11	P03	T	General-purpose I/O port. This function is enabled in single-chip mode.
		AD03		External address/data bus I/O pin bit 3 This function is enabled when the external bus is enabled.
		INT11		External interrupt request 11 input pin
		SIN6		Serial data input pin for LIN-UART6
79	P04/AD04/ SOT6/INT12	P04	T	General-purpose I/O port. This function is enabled in single-chip mode.
		AD04		External address/data bus I/O pin bit 4 This function is enabled when the external bus is enabled.
		INT12		External interrupt request 12 input pin
		SOT6		Serial data output pin for LIN-UART6

* : Refer to “■ I/O CIRCUIT TYPE” for the I/O circuit type.

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Pin No.	Pin name	Function name	I/O circuit type*	Function
80	P05/AD05/ SCK6/INT13	P05	T	General-purpose I/O port. This function is enabled in single-chip mode.
		AD05		External address/data bus I/O pin bit 5 This function is enabled when the external bus is enabled.
		INT13		External interrupt request 13 input pin
		SCK6		Clock I/O pin for LIN-UART6
81	P06/AD06/ INT14	P06	T	General-purpose I/O port. This function is enabled in single-chip mode.
		AD06		External address/data bus I/O pin bit 6 This function is enabled when the external bus is enabled.
		INT14		External interrupt request 14 input pin
82	P07/AD07/ INT15	P07	T	General-purpose I/O port. This function is enabled in single-chip mode.
		AD07		External address/data bus I/O pin bit 7 This function is enabled when the external bus is enabled.
		INT15		External interrupt request 15 input pin
Port 1				
83	P10/AD08/ TIN1	P10	T	General-purpose I/O port. This function is enabled in single-chip mode.
		AD08		External address/data bus I/O pin bit 8 This function is enabled when the external bus is enabled.
		TIN1		Event input pin for reload timer 1
84	P11/AD09/ TOT1	P11	T	General-purpose I/O port. This function is enabled in single-chip mode.
		AD09		External address/data bus I/O pin bit 9 This function is enabled when the external bus is enabled.
		TOT1		Output pin for reload timer 1
85	P12/AD10/ SIN3/ INT11R	P12	T	General-purpose I/O port. This function is enabled in single-chip mode.
		AD10		External address/data bus I/O pin bit 10 This function is enabled when the external bus is enabled.
		SIN3		Serial data input pin for LIN-UART3
		INT11R		External interrupt request 11 input pin (Set by EISSR)
86	P13/AD11/ SOT3	P13	T	General-purpose I/O port. This function is enabled in single-chip mode.
		AD11		External address/data bus I/O pin bit 11 This function is enabled when the external bus is enabled.
		SOT3		Serial data output pin for LIN-UART3

* : Refer to “■ I/O CIRCUIT TYPE” for the I/O circuit type.

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Pin No.	Pin name	Function name	I/O circuit type*	Function
87	P14/AD12/ SCK3	P14	T	General-purpose I/O port. This function is enabled in single-chip mode.
		AD12		External address/data bus I/O pin bit 12 This function is enabled when the external bus is enabled.
		SCK3		Clock I/O pin for LIN-UART3
92	P15/AD13/ SIN4	P15	T	General-purpose I/O port. This function is enabled in single-chip mode.
		AD13		External address/data bus I/O pin bit 13 This function is enabled when the external bus is enabled.
		SIN4		Serial data input pin for LIN-UART4
93	P16/AD14/ SOT4	P16	T	General-purpose I/O port. This function is enabled in single-chip mode.
		AD14		External address/data bus I/O pin bit 14 This function is enabled when the external bus is enabled.
		SOT4		Serial data output pin for LIN-UART4
94	P17/AD15/ SCK4	P17	T	General-purpose I/O port. This function is enabled in single-chip mode.
		AD15		External address/data bus I/O pin bit 15 This function is enabled when the external bus is enabled.
		SCK4		Clock I/O pin for LIN-UART4
Port 2				
95	P20/A16/ PPG9	P20	A	General-purpose I/O port. This function is enabled in single-chip mode.
		A16		External address bus output pin bit 16 This function is enabled when the external bus is enabled.
		PPG9		Output pin for PPG9
96	P21/A17/ PPGB	P21	A	General-purpose I/O port. This function is enabled in single-chip mode.
		A17		External address bus output pin bit 17 This function is enabled when the external bus is enabled.
		PPGB		Output pin for PPGB
97	P22/A18/ PPGD	P22	A	General-purpose I/O port. This function is enabled in single-chip mode.
		A18		External address bus output pin bit 18 This function is enabled when the external bus is enabled.
		PPGD		Output pin for PPGD

* : Refer to “■ I/O CIRCUIT TYPE” for the I/O circuit type.

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Pin No.	Pin name	Function name	I/O circuit type*	Function
98	P23/A19/ PPGF	P23	A	General-purpose I/O port. This function is enabled in single-chip mode.
		A19		External address bus output pin bit 19 This function is enabled when the external bus is enabled.
		PPGF		Output pin for PPGF
99, 100, 1, 2	P24/A20/IN0 to P27/A23/IN3	P24 to P27	A	General-purpose I/O port. This function is enabled in single-chip mode.
		A20 to A23		External address bus output pins bits 20 to 23 This function is enabled when the external bus is enabled.
		IN0 to IN3		Data sample input pins for input capture ICU0 to ICU3
Port 3				
3	P30/$\overline{AS}$/IN4	P30	A	General-purpose I/O port. This function is enabled in single-chip mode.
		$\overline{AS}$		External address strobe output pin This function is enabled when the external bus is enabled.
		IN4		Data sample input pin for input capture ICU4
4	P31/$\overline{RD}$/IN5	P31	A	General-purpose I/O port. This function is enabled in single-chip mode.
		$\overline{RD}$		External read strobe output pin This function is enabled when the external bus is enabled.
		IN5		Data sample input pin for input capture ICU5
5	P32/$\overline{WR0}$/ RX2/ INT10R	P32	A	General-purpose I/O port. This function is enabled in single-chip mode.
		$\overline{WR0}$		External data bus write strobe output pin. Enabled when the external bus is enabled. $\overline{WR0}$ is used as the data write strobe for 8-bit access and as the upper 8 bits of the data in 16-bit access.
		RX2		CAN2 RX input pin (MB91V280 only)
		INT10R		External interrupt request 10 input pin (Set by EISSR)
6	P33/$\overline{WR1}$/ TX2	P33	A	General-purpose I/O port. This function is enabled in single-chip mode.
		$\overline{WR1}$		Write strobe output pin for lower 8 bits in external data bus Enabled when the external bus is enabled and external bus 16-bit mode is selected.
		TX2		CAN2 TX output pin (MB91V280 only)

* : Refer to “■ I/O CIRCUIT TYPE” for the I/O circuit type.

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Pin No.	Pin name	Function name	I/O circuit type*	Function
7	P34/BRQ/ OUT4	P34	T (A)	General-purpose I/O port. This function is enabled in single-chip mode.
		BRQ		External bus request input pin Enabled when the external bus and the bus request functions are enabled. (MB91V280 only)
		OUT4		Waveform output pin for output compare OCU4.
8	P35/ $\overline{\text{BGRNT}}$/ OUT5	P35	A	General-purpose I/O port. This function is enabled in single-chip mode.
		$\overline{\text{BGRNT}}$		External bus acknowledge output pin Enabled when the external bus and the bus request functions are enabled. (MB91V280 only)
		OUT5		Waveform output pin for output compare OCU5.
9	P36/RDY/ OUT6	P36	T	General-purpose I/O port. This function is enabled in single-chip mode.
		RDY		External ready input pin Enabled when the external bus and the bus request functions are enabled.
		OUT6		Waveform output pin for output compare OCU6.
10	P37/ SYSCLK/ OUT7	P37	A	General-purpose I/O port. This function is enabled in single-chip mode.
		SYSCLK		External clock output pin This function is enabled when the external bus is enabled.
		OUT7		Waveform output pin for output compare OCU7.
Port 4				
11, 12	P40/ (X0A) , P41/ (X1A)	P40, P41	A	General-purpose I/O port (S-suffix models)
		X0A, X1A	WA WB	sub-clock oscillator input pin (without S-suffix models)
16	P42/IN6/ RX1/INT9R	P42	A	General-purpose I/O port
		IN6		Data sample input pin for input capture ICU6
		RX1		CAN1 RX input pin (MB91V280 only)
		INT9R		External interrupt request 9 input pin (Set by EISSR)
17	P43/IN7/ TX1	P43	A	General-purpose I/O port
		IN7		Data sample input pin for input capture ICU7
		TX1		CAN1 TX output pin (MB91V280 only)
18	P44/SDA0/ FRCK0	P44	C	General-purpose I/O port
		SDA0		Serial data I/O pin for I^2C0
		FRCK0		16-bit input/output timer 0 input pin

* : Refer to "■ I/O CIRCUIT TYPE" for the I/O circuit type.

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Pin No.	Pin name	Function name	I/O circuit type*	Function
19	P45/AIN2/ SCL0/ FRCK1	P45	C	General-purpose I/O port
		SCL0		Serial clock I/O pin for I²C0
		FRCK1		16-bit input/output timer 1 input pin
		AIN2		8/16-bit up-count input pin for up down counter 2/3
20	P46/BIN2/ SDA1	P46	C	General-purpose I/O port
		SDA1		Serial clock I/O pin for I²C1
		BIN2		8/16-bit down-count input pin for up down counter 2/3
21	P47/ZIN2/ SCL1	P47	C	General-purpose I/O port
		SCL1		Serial clock I/O pin for I²C1
		ZIN2		8/16-bit reset input pin for up down counter 2/3
				Port 5
22	P50/AN8/ SIN2	P50	D	General-purpose I/O port
		AN8		Analog input pin of A/D converter
		SIN2		Serial data input pin for LIN-UART2
23	P51/AN9/ SOT2	P51	D	General-purpose I/O port
		AN9		Analog input pin of A/D converter
		SOT2		Serial data output pin for LIN-UART2
24	P52/AN10/ SCK2	P52	D	General-purpose I/O port
		AN10		Analog input pin of A/D converter
		SCK2		Clock I/O pin for LIN-UART2
25	P53/AN11/ BIN1	P53	D	General-purpose I/O port
		AN11		Analog input pin of A/D converter
		BIN1		8-bit down-count input pin for 16-bit up down counter 1
26	P54/AN12/ AIN1	P54	D	General-purpose I/O port
		AN12		Analog input pin of A/D converter
		AIN1		8-bit up-count input pin for 16-bit up down counter 1
27	P55/AN13/ ZIN1	P55	D	General-purpose I/O port
		AN13		Analog input pin of A/D converter
		ZIN1		8-bit reset input pin for 16-bit up down counter 1
28	P56/AN14/ DAO0	P56	E	General-purpose I/O port
		AN14		Analog input pin of A/D converter
		DAO0		Analog output pin 0 for D/A converter (MB91V280 only)
29	P57/AN15/ DAO1	P57	E	General-purpose I/O port
		AN15		Analog input pin of A/D converter
		DAO1		Analog output pin 1 for D/A converter (MB91V280 only)

* : Refer to “■ I/O CIRCUIT TYPE” for the I/O circuit type.

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Pin No.	Pin name	Function name	I/O circuit type*	Function
				Port 6
34 to 41	P60/AN0/ PPG0 to P67/AN7/ PPGE	P60 to P67	D	General-purpose I/O port
		AN0 to AN7		Analog input pins of A/D converter
		PPG0 PPG2 PPG4 PPG6 PPG8 PPGA PPGC PPGE		Output pins for PPG
				Port 7
43 to 48	P70/AN16/ INT0 to P75/AN21/ INT5	P70 to P75	D	General-purpose I/O port
		AN16 to AN21		Analog input pins of A/D converter
		INT0 to INT5		External interrupt request 0 to 5 input pin
53	P76/AN22/ INT6/SDA2	P76	CA	General-purpose I/O port
		AN22		Analog input pin of A/D converter
		INT6		External interrupt request 6 input pin
		SDA2		Serial clock I/O pin for I^2C2
54	P77/AN23/ INT7/SCL2	P77	CA	General-purpose I/O port
		AN23		Analog input pin of A/D converter
		INT7		External interrupt request 7 input pin
		SCL2		Serial clock I/O pin for I^2C2
				Port 8
55	P80/TIN0/ INT12R/ ADTG	P80	A	General-purpose I/O port
		TIN0		Event input pin for reload timer 0
		ADTG		Trigger input pin for A/D converter
		INT12R		External interrupt request 12 input pin (Set by EISSR)
56	P81/TOT0/ INT13R/ CKOT	P81	A	General-purpose I/O port
		TOT0		Output pin for reload timer 0
		CKOT		Output pin for clock monitor
		INT13R		External interrupt request 13 input pin (Set by EISSR)
57	P82/TIN2/ SIN0/INT14R	P82	A	General-purpose I/O port
		SIN0		Serial data input pin for LIN-UART0
		TIN2		Event input pin for reload timer 2
		INT14R		External interrupt request 14 input pin (Set by EISSR)

* : Refer to "■ I/O CIRCUIT TYPE" for the I/O circuit type.

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Pin No.	Pin name	Function name	I/O circuit type*	Function
58	P83/TOT2/ SOT0	P83	A	General-purpose I/O port
		SOT0		Serial data output pin for LIN-UART0
		TOT2		Output pin for reload timer 2
59	P84/SCK0/ INT15R	P84	A	General-purpose I/O port
		SCK0		Clock I/O pin for LIN-UART0
		INT15R		External interrupt request 15 input pin (Set by EISSR)
60	P85/SIN1	P85	A	General-purpose I/O port
		SIN1		Serial data input pin for LIN-UART1
61	P86/SOT1	P86	A	General-purpose I/O port
		SOT1		Serial data output pin for LIN-UART1
62	P87/SCK1	P87	A	General-purpose I/O port
		SCK1		Clock I/O pin for LIN-UART1
				Port 9
65	P90/PPG1/ $\overline{CS0}$	P90	A	General-purpose I/O port
		$\overline{CS0}$		External chip select 0 This function is enabled when the external bus is enabled.
		PPG1		Output pin for PPG1
66	P91/PPG3/ AIN3/$\overline{CS1}$	P91	A	General-purpose I/O port
		$\overline{CS1}$		External chip select 1 This function is enabled when the external bus is enabled.
		PPG3		Output pin for PPG3
		AIN3		8-bit up-count input pin for up down counter 3
67	P92/PPG5/ BIN3/$\overline{CS2}$	P92	A	General-purpose I/O port
		$\overline{CS2}$		External chip select 2 This function is enabled when the external bus is enabled.
		PPG5		Output pin for PPG5
		BIN3		8-bit down-count input pin for up down counter 3
68	P93/PPG7/ ZIN3/$\overline{CS3}$	P93	A	General-purpose I/O port
		$\overline{CS3}$		External chip select 3 This function is enabled when the external bus is enabled.
		PPG7		Output pin for PPG7
		ZIN3		8-bit reset input pin for up down counter 3
69	P94/OUT0/ AIN0	P94	A	General-purpose I/O port
		OUT0		Waveform output pin for output compare OCU0
		AIN0		16/8-bit up-count input pin for up down counter 0/1

* : Refer to "■ I/O CIRCUIT TYPE" for the I/O circuit type.

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Pin No.	Pin name	Function name	I/O circuit type*	Function
70	P95/OUT1/ BIN0	P95	A	General-purpose I/O port
		OUT1		Waveform output pin for output compare OCU1
		BIN0		8/16-bit down-count input pin for up down counter 0/1
71	P96/OUT2/ ZIN0	P96	A	General-purpose I/O port
		OUT2		Waveform output pin for output compare OCU2
		ZIN0		8/16-bit reset input pin for up down counter 0/1
72	P97/OUT3	P97	A	General-purpose I/O port
		OUT3		Waveform output pin for output compare OCU3
Port A				
73	PA0/RX0/ INT8R	PA0	A	General-purpose I/O port
		RX0		RX input pin for CAN0
		INT8R		External interrupt request 8 input pin (Set by EISSR)
74	PA1/TX0	PA1	A	General-purpose I/O port
		TX0		TX output pin for CAN0
Port B (MB91V280 only)				
—	PB0	PB0	A	General-purpose I/O port
		INT8-2		External interrupt request 8 input pin (Set by EPFRB)
		SIN5-2		Serial data input pin for LIN-UART5 (Set by PFRB)
—	PB1	PB1	A	General-purpose I/O port
		INT9-2		External interrupt request 9 input pin (Set by EPFRB)
		SOT5-2		Serial data output pin for LIN-UART5
—	PB2	PB2	A	General-purpose I/O port
		INT10-2		External interrupt request 10 input pin (Set by EPFRB)
		SCK5-2		Clock I/O pin for LIN-UART5 (set by PFRB)
—	PB3	PB3	A	General-purpose I/O port
		INT11-2		External interrupt request 11 input pin (Set by EPFEB)
		SIN6-2		Serial data input pin for LIN-UART6 (Set by PFRB)
—	PB4	PB4	A	General-purpose I/O port
		INT12-2		External interrupt request 12 input pin (Set by EPFRB)
		SOT6-2		Serial data output pin for LIN-UART6
—	PB5	PB5	A	General-purpose I/O port
		INT13-2		External interrupt request 13 input pin (Set by EPFRB)
		SCK6-2		Clock I/O pin for LIN-UART6 (set by PFRB)
Port C (MB91V280 only)				

* : Refer to “■ I/O CIRCUIT TYPE” for the I/O circuit type.

(Continued)

Pin No.	Pin name	Function name	I/O circuit type*	Function
—	PC0	PC0	A	General-purpose I/O port
		OUT4-2		Output pin for output compare 4
		INT0R		External interrupt request 0 input pin (Set by EISSR)
—	PC1	PC1	A	General-purpose I/O port
		OUT5-2		Output pin for output compare 5
		INT1R		External interrupt request 1 input pin (Set by EISSR)
—	PC2	PC2	A	General-purpose I/O port
		SIN3-2		Serial data input pin for LIN-UART3 (Set by PFRC)
		INT2R		External interrupt request 2 input pin (Set by EISSR)
—	PC3	PC3	A	General-purpose I/O port
		SOT3-2		Serial data output pin for LIN-UART3
		INT3R		External interrupt request 3 input pin (Set by EISSR)
—	PC4	PC4	A	General-purpose I/O port
		SCK3-2		Clock I/O pin for LIN-UART3 (set by PFRC)
		INT4R		External interrupt request 4 input pin (Set by EISSR)
—	PC5	PC5	A	General-purpose I/O port
		SIN4-2		Serial data input pin for LIN-UART4 (Set by PFRC)
		INT5R		External interrupt request 5 input pin (Set by EISSR)
—	PC6	PC6	A	General-purpose I/O port
		SOT4-2		Serial data output pin for LIN-UART4
		INT6R		External interrupt request 6 input pin (Set by EISSR)
—	PC7	PC7	A	General-purpose I/O port
		SCK4-2		Clock I/O pin for LIN-UART4 (set by PFRC)
		INT7R		External interrupt request 7 input pin (Set by EISSR)
Port D (MB91V280 only)				
—	PD0	PD0	A	General-purpose I/O port
		INT16		External interrupt request 16 input pin
		PPG9-2		Output pin for PPG9 (8)
—	PD1	PD1	A	General-purpose I/O port
		INT17		External interrupt request 17 input pin
		PPGB-2		Output pin for PPGB (A)
—	PD2	PD2	A	General-purpose I/O port
		INT18		External interrupt request 18 input pin
		PPGD-2		Output pin for PPGD (C)

* : Refer to “■ I/O CIRCUIT TYPE” for the I/O circuit type.

(Continued)

Pin No.	Pin name	Function name	I/O circuit type*	Function
—	PD3	PD3	A	General-purpose I/O port
		INT19		External interrupt request 19 input pin
		PPGF-2		Output pin for PPGF (E)
—	PD4	PD4	A	General-purpose I/O port
		INT20		External interrupt request 20 input pin
		IN0-2		Input pin for input capture ICU0 (set by PFRD)
—	PD5	PD5	A	General-purpose I/O port
		INT21		External interrupt request 21 input pin
		IN1-2		Input pin for input capture ICU1 (set by PFRD)
—	PD6	PD6	A	General-purpose I/O port
		INT22		External interrupt request 22 input pin
		IN2-2		Input pin for input capture ICU2 (set by PFRD)
—	PD7	PD7	A	General-purpose I/O port
		INT23		External interrupt request 23 input pin
		IN3-2		Input pin for input capture ICU3 (set by PFRD)
Port E (MB91V280 only)				
—	PE0	PE0	A	General-purpose I/O port
		A00		External address bus output pin bit 0 This function is enabled when the external bus is enabled.
		INT24		External interrupt request 24 input pin
—	PE1	PE1	A	General-purpose I/O port
		A01		External address bus output pin bit 1 This function is enabled when the external bus is enabled.
		INT25		External interrupt request 25 input pin
—	PE2	PE2	A	General-purpose I/O port
		A02		External address bus output pin bit 2 This function is enabled when the external bus is enabled.
		INT26		External interrupt request 26 input pin
—	PE3	PE3	A	General-purpose I/O port
		A03		External address bus output pin bit 3 This function is enabled when the external bus is enabled.
		INT27		External interrupt request 27 input pin
—	PE4	PE4	A	General-purpose I/O port
		A04		External address bus output pin bit 4 This function is enabled when the external bus is enabled.
		INT28		External interrupt request 28 input pin

* : Refer to "■ I/O CIRCUIT TYPE" for the I/O circuit type.

(Continued)

Pin No.	Pin name	Function name	I/O circuit type*	Function
—	PE5	PE5	A	General-purpose I/O port
		A05		External address bus output pin bit 5 This function is enabled when the external bus is enabled.
		INT29		External interrupt request 29 input pin
—	PE6	PE6	A	General-purpose I/O port
		A06		External address bus output pin bit 6 This function is enabled when the external bus is enabled.
		INT30		External interrupt request 30 input pin
—	PE7	PE7	A	General-purpose I/O port
		A07		External address bus output pin bit 7 This function is enabled when the external bus is enabled.
		INT31		External interrupt request 31 input pin
Port F (MB91V280 only)				
—	PF0	PF0	A	General-purpose I/O port
		A08		External address bus output pin bit 8 This function is enabled when the external bus is enabled.
		INT32		External interrupt request 32 input pin
—	PF1	PF1	A	General-purpose I/O port
		A09		External address bus output pin bit 9 This function is enabled when the external bus is enabled.
		INT33		External interrupt request 33 input pin
—	PF2	PF2	A	General-purpose I/O port
		A10		External address bus output pin bit 10 This function is enabled when the external bus is enabled.
		INT34		External interrupt request 34 input pin
—	PF3	PF3	A	General-purpose I/O port
		A11		External address bus output pin bit 11 This function is enabled when the external bus is enabled.
		INT35		External interrupt request 35 input pin
—	PF4	PF4	A	General-purpose I/O port
		A12		External address bus output pin bit 12 This function is enabled when the external bus is enabled.
		INT36		External interrupt request 36 input pin
—	PF5	PF5	A	General-purpose I/O port
		A13		External address bus output pin bit 13 This function is enabled when the external bus is enabled.
		INT37		External interrupt request 37 input pin

* : Refer to “■ I/O CIRCUIT TYPE” for the I/O circuit type.

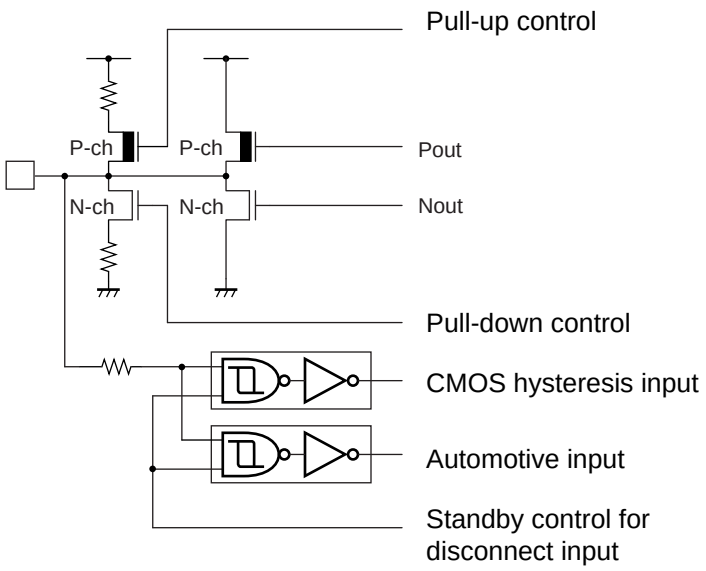
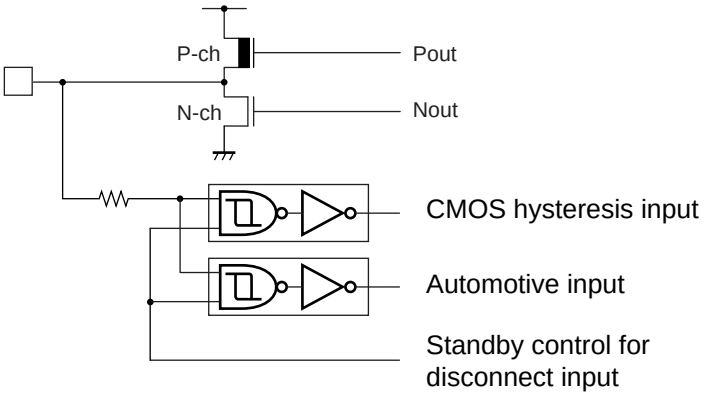
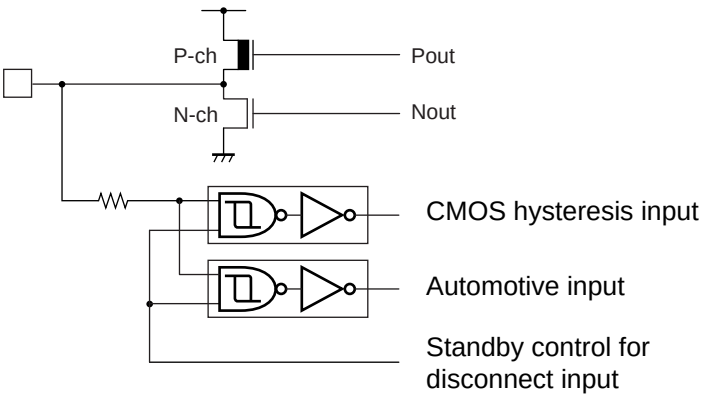
(Continued)

(Continued)

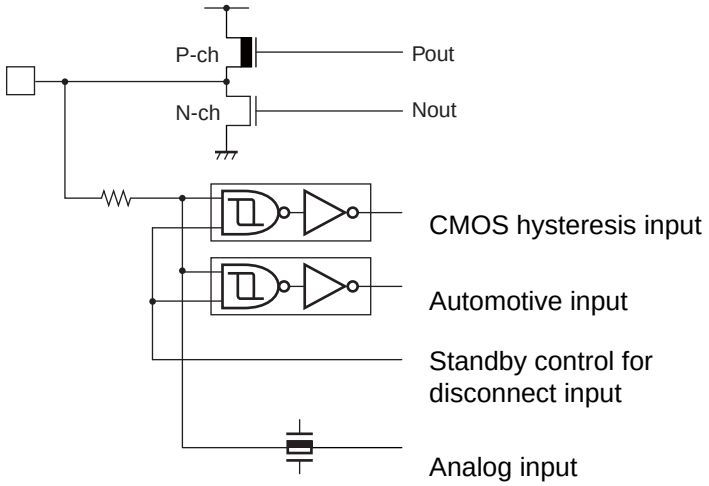
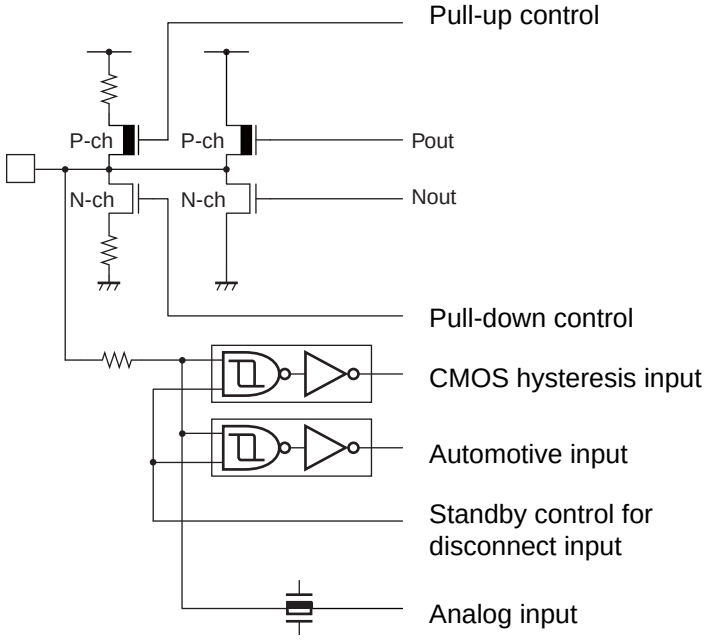
Pin No.	Pin name	Function name	I/O circuit type*	Function
—	PF6	PF6	A	General-purpose I/O port
		A14		External address bus output pin bit 14 This function is enabled when the external bus is enabled.
		INT38		External interrupt request 38 input pin
—	PF7	PF7	A	General-purpose I/O port
		A15		External address bus output pin bit 15 This function is enabled when the external bus is enabled.
		INT39		External interrupt request 39 input pin
Port G (MB91V280 only)				
—	PG0	PG0	D	General-purpose I/O port
		AN24		Analog input pin of A/D converter
—	PG1	PG1	D	General-purpose I/O port
		AN25		Analog input pin of A/D converter
—	PG2	PG2	D	General-purpose I/O port
		AN26		Analog input pin of A/D converter
—	PG3	PG3	D	General-purpose I/O port
		AN27		Analog input pin of A/D converter
—	PG4	PG4	D	General-purpose I/O port
		AN28		Analog input pin of A/D converter
—	PG5	PG5	D	General-purpose I/O port
		AN29		Analog input pin of A/D converter
—	PG6	PG6	D	General-purpose I/O port
		AN30		Analog input pin of A/D converter
—	PG7	PG7	D	General-purpose I/O port
		AN31		Analog input pin of A/D converter
Power supply pin				
13, 63, 88	V_{CC}	—	—	Power supply (5 V) input pin
14, 42, 64, 89	V_{SS}	—	—	Power supply (0 V) input pin
15	C	—	—	Power stabilization capacitance pin
30	AV_{CC}	—	—	Analog power supply input pin
31	AVRH	—	—	Reference voltage input pin for the A/D converter Ensure that a voltage greater than AVRH is applied to AV_{CC} when turning this power supply on or off.
32	AVRL	—	—	Low reference voltage input pin for the A/D converter
33	AV_{SS}	—	—	Analog V_{SS} input pin

* : Refer to “■ I/O CIRCUIT TYPE” for the I/O circuit type.

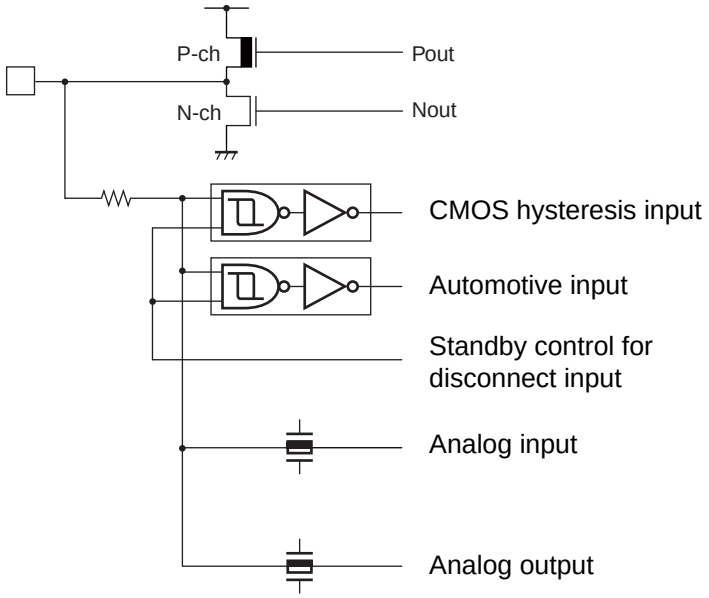
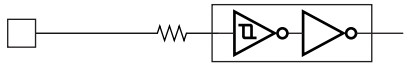
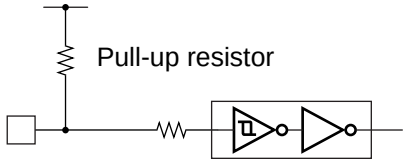
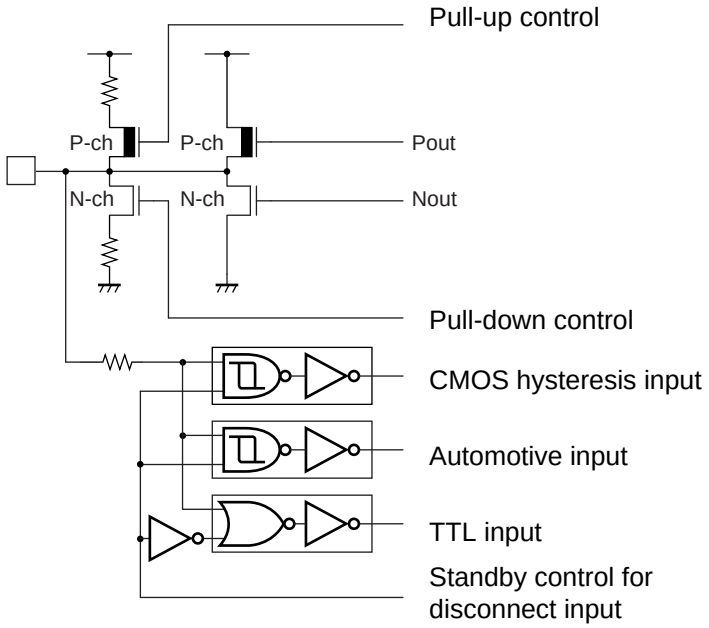
■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) • CMOS hysteresis input (With function to disconnect input during standby mode.) • Automotive input (With function to disconnect input during standby mode.) • Resistor that can be set pull-up resistor : Approx. 50 Ω
B		• CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) • CMOS hysteresis input (With function to disconnect input during standby mode.) • Automotive input (With function to disconnect input during standby mode.)
C		• CMOS level output (I_{OL} = 3 mA, I_{OH} = –3 mA) • CMOS hysteresis input (With function to disconnect input during standby mode.) • Automotive input (With function to disconnect input during standby mode.)

(Continued)

Type	Circuit	Remarks
CA		• CMOS level output (I_{OL} = 3 mA, I_{OH} = –3 mA) • CMOS hysteresis input (With function to disconnect input during standby mode.) • Automotive input (With function to disconnect input during standby mode.) • A/D analog input
D		• CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) • CMOS hysteresis input (With function to disconnect input during standby mode.) • Automotive input (With function to disconnect input during standby mode.) • Resistor that can be set pull-up resistor : Approx. 50 Ω • A/D analog input

(Continued)

Type	Circuit	Remarks
E		• CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) • CMOS hysteresis input (With function to disconnect input during standby mode.) • Automotive input (With function to disconnect input during standby mode.) • A/D analog input • D/A analog output
J		CMOS hysteresis input
N		• CMOS hysteresis input • Pull-up resistor value : Approx. 50 kΩ
T		• CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) • CMOS hysteresis input (With function to disconnect input during standby mode.) • Automotive input (With function to disconnect input during standby mode.) • TTL (With function to disconnect input during standby mode.) • Resistor that can be set pull-up resistor : Approx. 50 kΩ

(Continued)

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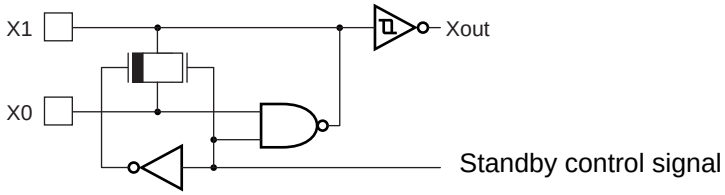
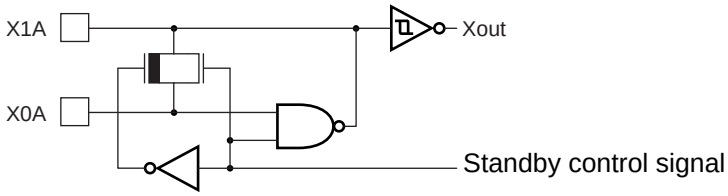
Type	Circuit	Remarks
OA OB		Oscillation circuit High speed oscillation feedback resistance = Approx. 1 MΩ
WA WB		Oscillation circuit Low speed oscillation feedback resistance = Approx. 10 MΩ

■ I/O CELL LIST

Type	Input			Analog Line	Output Driver	Remarks
	Pull Up/Down (50 kΩ)	CMOS (C) CMOS Schmitt (CS) Automotive (A)	Input Stop			
A	Up/Down switch	CS/A switch	Stop	—	4 mA	
B	—	CS/A switch	Stop	—	4 mA	
C*	—	CS/A switch	Stop	—	3 mA	I^2C
CA*	—	CS/A switch	Stop	Input	3 mA	I^2C + A/DC
D	Up/Down switch	CS/A switch	Stop	Input	4 mA	A/DC
E	—	CS/A switch	Stop	I/O	4 mA	A/DC + D/AC
J	—	C	—	—	—	MD[2 : 0]
N	Up	CS (initx)	—	—	—	$\overline{INIT}$
T	Up/Down switch	CS/A/TTL switch	Stop	—	4 mA	Has TTL input
OA OB	—	—	Stop	—	—	4 MHz Oscillator
WA WB	—	—	Stop	—	—	32 kHz Oscillator

* : When the C and CA ports are set for the use of an I^2C interface, the outputs are Nch open drain outputs. Otherwise, functions as a CMOS output.

■ PIN INPUT VOLTAGE

Form	Type	V_{IL}	V_{IH}
C	CMOS input	V_{SS} + 0.3 V	V_{CC} – 0.3 V
CS (initx)	CMOS Schmitt trigger input (for $\overline{INIT}$ pin)	0.2 × V_{CC}	0.8 × V_{CC}
CS	CMOS Schmitt trigger input	0.3 × V_{CC}	0.7 × V_{CC}
A	CMOS automotive Schmitt trigger input	0.5 × V_{CC}	0.8 × V_{CC}
T	TTL input	0.8 V	2.1 V

■ HANDLING DEVICES

• Preventing Latch-up

Latch-up may occur in a CMOS IC if a voltage greater than V_{CC} or less than V_{SS} is applied to an input or output pin or if an above-rating voltage is applied between V_{CC} pin and V_{SS} pin. A latch-up, if it occurs, significantly increases the power supply current and may cause thermal destruction of an element. When you use a CMOS IC, do not exceed the maximum rating.

• Treatment of Unused Pins

Do not leave an unused input pin open, since it may cause a malfunction. Handle by, for example, using a pull-up or pull-down resistor.

• Power Supply Pins

In products with multiple V_{CC} or V_{SS} pins, the pins of the same potential are internally connected in the device to avoid abnormal operations such as latch-up. However, you must connect the pins to external power supply and a ground line to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with the V_{CC} and V_{SS} pins of this device at the low impedance.

It is also advisable to connect a ceramic bypass capacitor of approximately 0.1 µF between V_{CC} and V_{SS} near this device.

• Crystal Oscillator Circuit

Noise near the X0, X1, X0A and X1A pins may cause the device to malfunction. Design the printed circuit board so that X0, X1, X0A and X1A pins the crystal oscillator (or ceramic oscillator), and the bypass capacitor to ground are located as close to the device as possible.

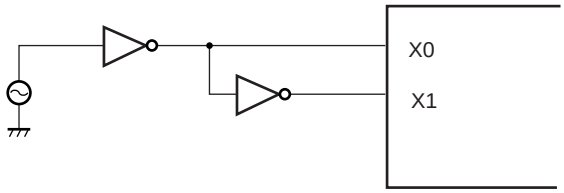
It is strongly recommended to design the PC board artwork with the X0, X1, X0A and X1A pins surrounded by ground plane because stable operation can be expected with such a layout.

Please ask the crystal maker to evaluate the oscillational characteristics of the crystal and this device.

• Notes on Using External Clock

When external clock is selected, supply it to X0 pin generally, and simultaneously the opposite phase clock to X0 must be supplied to X1 pin. However, in this case the stop mode (oscillation stop mode) must not be used. (This is because the X1 pin stops at High level output in STOP mode.)

Using an external clock (normal)



Note : The STOP mode (oscillation stop mode) cannot be used.

- Serial Communication

  There is a possibility to receive wrong data due to the noise or other causes on the serial communication. Therefore, design a printed circuit board so as to avoid noise.
  Retransmit the data if an error occurs because of applying the checksum to the last data in consideration of receiving wrong data due to the noise.

- Notes when using no sub-clock

  Use a single-clock model if not using the sub-clock.

  Always connect a resonator of 100 kHz or less on dual clock models.

- Treatment of NC or OPEN pins

  Pins marked as NC and OPEN must be left open - circuit.

- Mode pins (MD0 to MD2)

  These pins should be connected directly to V_{CC} or V_{SS}. To prevent the device erroneously switching to test mode due to noise, design the printed circuit board such that the distance between the mode pins and V_{CC} or V_{SS} is as short as possible and the connection impedance is low.

- Operation at start-up

  The $\overline{INIT}$ pin must be held at the “L”level when turning on the power.

- Source oscillation input at power on

  When turning the power on, maintain clock input until the device is released from the oscillation stabilization wait state.

- Caution on operations during PLL Clock Mode

  On this microcontroller, if in case the crystal oscillator breaks off or an external reference clock input stops while the PLL clock mode is selected, a self-oscillator circuit contained in the PLL may continue its operation at its self-running frequency. However, Fujitsu will not guarantee results of operations if such failure occurs.

- External bus setting

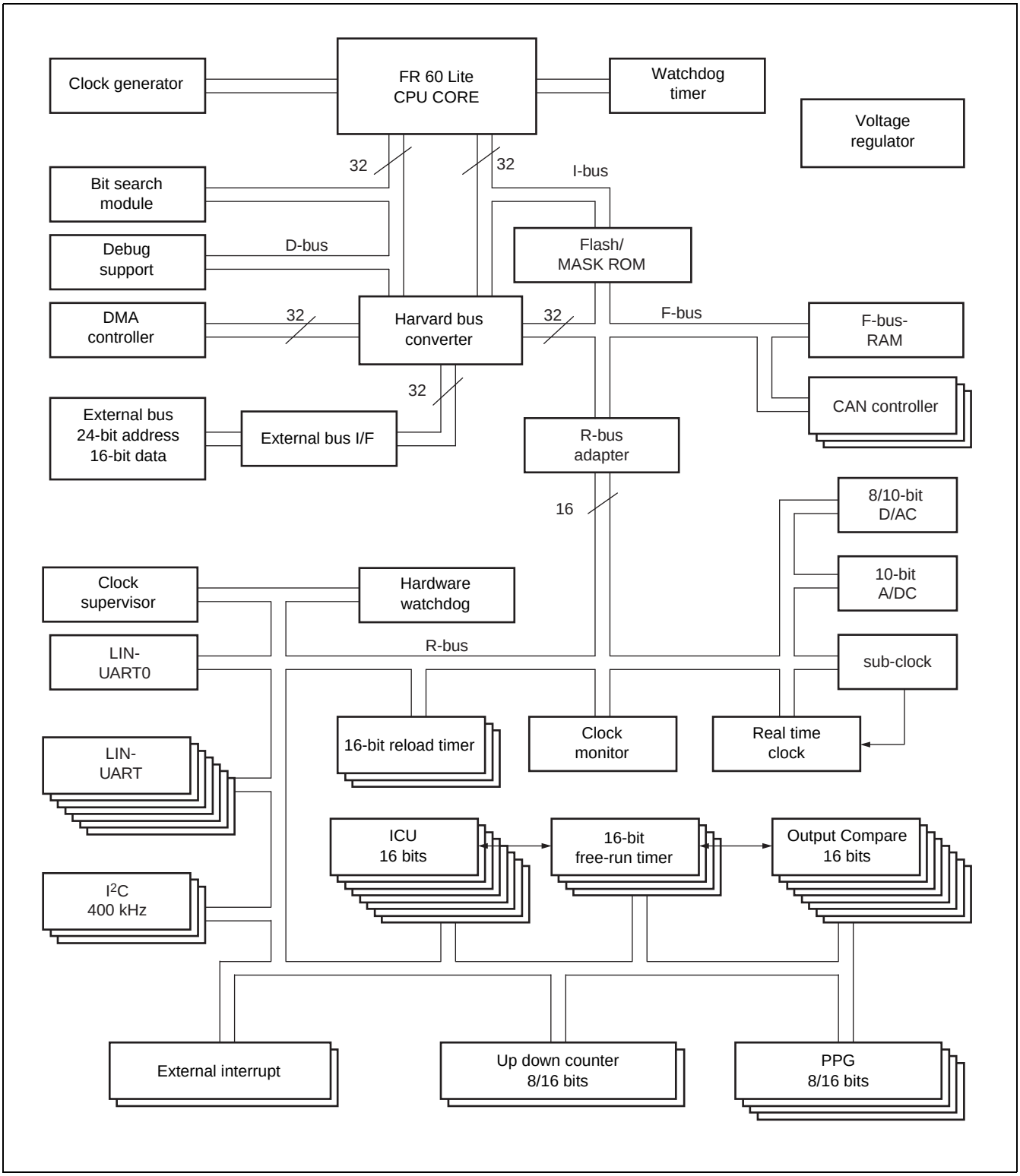
  This device is guaranteed for use with a 16 MHz external bus.

  If the base clock is set to 32 MHz with DIVR1 (external bus base clock division setting register) set to its initial value, the external bus also operates at 32 MHz. When changing the base clock, set the external bus so that it will not exceed 16 MHz.

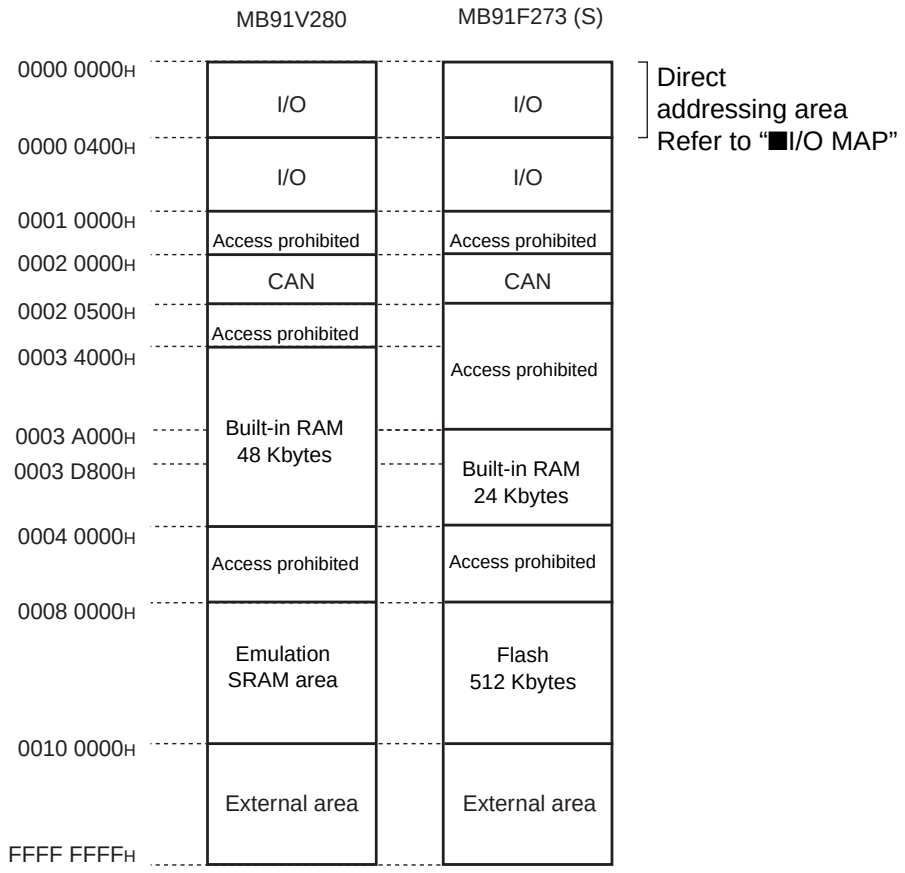
- Pull-up control

  The AC characteristics cannot be guaranteed if pull-up resistors are used for the pins used as external bus pins.

■ BLOCK DIAGRAM



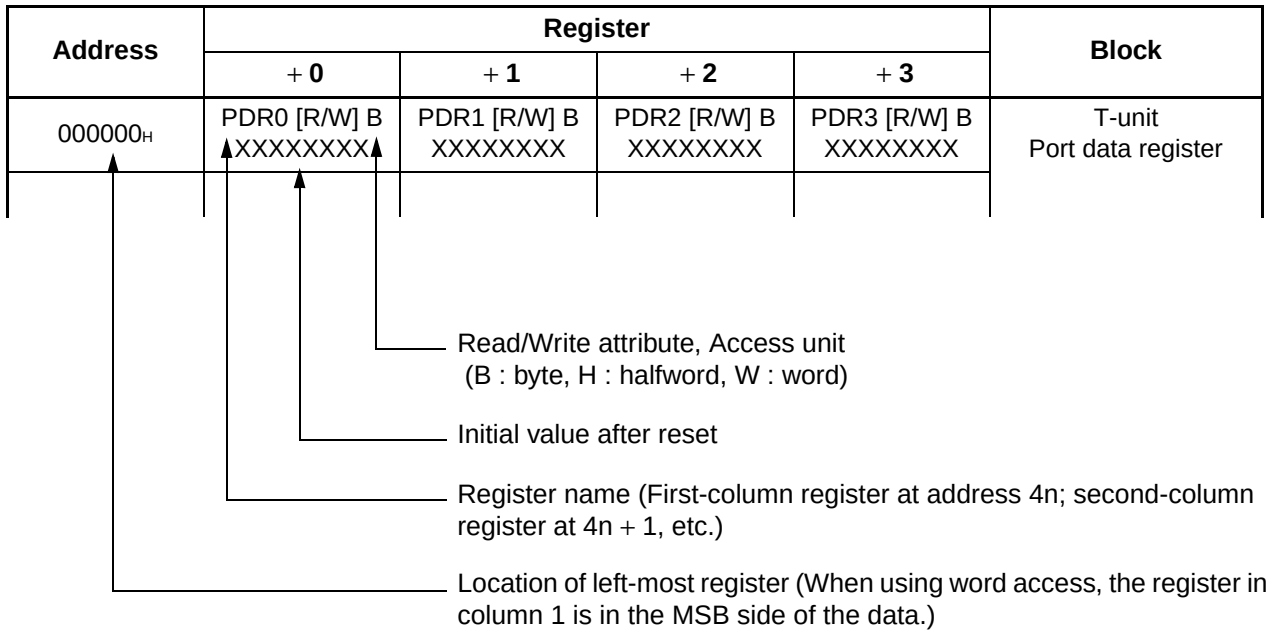
■ MEMORY MAP



Note : The initial value for the emulation SRAM area on the MB91V280 is 512 Kbytes (0000080000H to 0000100000H) .
An SRAM area is supported up to 1024 Kbytes (0000050000H to 0000150000H)

■ I/O MAP

How to read I/O map



Note :

Initial values of register bits are represented as follows :

“ 1 ” : Initial value “1”

“ 0 ” : Initial value “0”

“ X ” : Initial value “undefined”

“ - ” : No physical register present at this location

Access by any undescribed data access attribute is prohibited.

Address	Register				Block
	+0	+1	+2	+3	
000000H	PDR0 [R/W] B, H XXXXXXXX	PDR1 [R/W] B, H XXXXXXXX	PDR2 [R/W] B, H XXXXXXXX	PDR3 [R/W] B, H XXXXXXXX	Port Data Registers (PDRB to PDRG are only available on the MB91V280.)
000004H	PDR4 [R/W] B, H XXXXXXXX	PDR5 [R/W] B, H XXXXXXXX	PDR6 [R/W] B, H XXXXXXXX	PDR7 [R/W] B, H XXXXXXXX	
000008H	PDR8 [R/W] B, H XXXXXXXX	PDR9 [R/W] B, H XXXXXXXX	PDRA [R/W] B, H ------XX	PDRB [R/W] B, H --XXXXXX	
00000CH	PDRC [R/W] B, H XXXXXXXX	PDRD [R/W] B, H XXXXXXXX	PDRE [R/W] B, H XXXXXXXX	PDRF [R/W] B, H XXXXXXXX	
000010H	PDRG [R/W] B, H XXXXXXXX	—			
000014H to 00003CH	—				System Reserved
000040H	EIRR0 [R/W] 00000000	ENIR [R/W] 00000000	ELVR0 [R/W] 00000000 00000000		Ext. INT 0-7
000044H	DICR [R/W] -------0	HRCL [R, R/W] 0--11111	—		DLY / I-Unit
000048H	TMRLR0 [W] XXXXXXXX XXXXXXXX		TMR0 [R] XXXXXXXX XXXXXXXX		Reload Timer 0
00004CH	—		TMCSR0 [R, RW] 00000000 00000000		
000050H	TMRLR1 [W] XXXXXXXX XXXXXXXX		TMR1 [R] XXXXXXXX XXXXXXXX		Reload Timer 1
000054H	—		TMCSR1 [R, RW] 00000000 00000000		
000058H	TMRLR2 [W] XXXXXXXX XXXXXXXX		TMR2 [R] XXXXXXXX XXXXXXXX		Reload Timer 2
00005CH	—	—	TMCSR2 [R, RW] 00000000 00000000		
000060H	SCR0 [R, R/W] 00000000	SMR0 [W, R/W] 00000000	SSR0 [R, R/W] 00001000	RDR0/TRD0 [R/W] 00000000	LIN-UART 0
000064H	ESCR0 [R/W] 00000100	ECCR0 [R, W, R/W] 000000XX	BGR10 [R/W] 00000000	BGR00 [R/W] 00000000	
000068H	SCR5 [R, R/W] 00000000	SMR5 [W, R/W] 00000000	SSR5 [R, R/W] 00001000	RDR5/TRD5 [R/W] 00000000	LIN-UART 5
00006CH	ESCR5 [R/W] 00000100	ECCR5 [R, W, R/W] 000000XX	BGR15 [R/W] 00000000	BGR05 [R/W] 00000000	

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000070H	SCR6 [R, R/W] 00000000	SMR6 [W, R/W] 00000000	SSR6 [R, R/W] 00001000	RDR6/TRD6 [R/W] 00000000	LIN-UART 6
000074H	ESCR6 [R/W] 00000100	ECCR6 [R, W, R/W] 000000XX	BGR16 [R/W] 00000000	BGR06 [R/W] 00000000	
000078H to 0000ACH	—				System Reserved
0000B0H	SCR1 [R, R/W] 00000000	SMR1 [W, R/W] 00000000	SSR1 [R, R/W] 00001000	RDR1/TRD1 [R/W] 00000000	LIN-UART 1
0000B4H	ESCR1 [R/W] 00000100	ECCR1 [R, W, R/W] 000000XX	BGR11 [R/W] 00000000	BGR01 [R/W] 00000000	
0000B8H	SCR2 [R, R/W] 00000000	SMR2 [W, R/W] 00000000	SSR2 [R, R/W] 00001000	RDR2/TRD2 [R/W] 00000000	LIN-UART 2
0000BCH	ESCR2 [R/W] 00000100	ECCR2 [R, W, R/W] 000000XX	BGR12 [R/W] 00000000	BGR02 [R/W] 00000000	
0000C0H	SCR3 [R, R/W] 00000000	SMR3 [W, R/W] 00000000	SSR3 [R, R/W] 00001000	RDR3/TRD3 [R/W] 00000000	LIN-UART 3
0000C4H	ESCR3 [R/W] 00000100	ECCR3 [R, W, R/W] 000000XX	BGR13 [R/W] 00000000	BGR03 [R/W] 00000000	
0000C8H	SCR4 [R, R/W] 00000000	SMR4 [W, R/W] 00000000	SSR4 [R, R/W] 00001000	RDR4/TRD4 [R/W] 00000000	LIN-UART 4
0000CCH	ESCR4 [R/W] 00000100	ECCR4 [R, W, R/W] 000000XX	BGR14 [R/W] 00000000	BGR04 [R/W] 00000000	
0000D0H	EIRR1 [R/W] 00000000	ENIR1 [R/W] 00000000	ELVR1 [R/W] 00000000 00000000		Ext. INT 8 to 15
0000D4H	TCTDT0 [R/W] H 00000000 00000000		—	TCCS0 [R/W] B 00000000	Free-run Timer 0
0000D8H	TCTDT1 [R/W] H 00000000 00000000		—	TCCS1 [R/W] B 00000000	Free-run Timer 1
0000DCH	TCTDT2 [R/W] H 00000000 00000000		—	TCCS2 [R/W] B 00000000	Free-run Timer 2
0000E0H	TCTDT3 [R/W] H 00000000 00000000		—	TCCS3 [R/W] B 00000000	Free Run Timer 3

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
0000E4H	IPCP1 [R] XXXXXXXX XXXXXXXX		IPCP0 [R] XXXXXXXX XXXXXXXX		Input Capture Unit 0, 1
0000E8H	—			ICS01 [R/W] 00000000	
0000ECH	IPCP3 [R] XXXXXXXX XXXXXXXX		IPCP2 [R] XXXXXXXX XXXXXXXX		Input Capture Unit 2, 3
0000F0H	—			ICS23 [R/W] 00000000	
0000F4H	IPCP5 [R] XXXXXXXX XXXXXXXX		IPCP4 [R] XXXXXXXX XXXXXXXX		Input Capture Unit 4, 5
0000F8H	—			ICS45 [R/W] 00000000	
0000FCH	IPCP7 [R] XXXXXXXX XXXXXXXX		IPCP6 [R] XXXXXXXX XXXXXXXX		Input Capture Unit 6, 7
000100H	—			ICS67 [R/W] 00000000	
000104H	—				System Reserved
000108H	OCCP1 [R/W] XXXXXXXX XXXXXXXX		OCCP0 [R/W] XXXXXXXX XXXXXXXX		Output Compare 1/0
00010CH	OCCP3 [R/W] XXXXXXXX XXXXXXXX		OCCP2 [R/W] XXXXXXXX XXXXXXXX		Output Compare 3/2
000110H	OCS23 [R/W] 11101100 00001100		OCS01 [R/W] 11101100 00001100		Output Compare 3 to 0 Ctrl.
000114H	OCCP5 [R/W] XXXXXXXX XXXXXXXX		OCCP4 [R/W] XXXXXXXX XXXXXXXX		Output Compare 5/4
000118H	OCCP7 [R/W] XXXXXXXX XXXXXXXX		OCCP6 [R/W] XXXXXXXX XXXXXXXX		Output Compare 7/6
00011CH	OCS67 [R/W] 11101100 00001100		OCS45 [R/W] 11101100 00001100		Output Compare 7 to 4 Ctrl.
000120H to 00012CH	—				System Reserved
000130H	EIRR2 [R/W] 00000000	ENIR2 [R/W] 00000000	ELVR2 [R/W] 00000000 00000000		Ext. INT 16 to 23
000134H	EIRR3 [R/W] 00000000	ENIR3 [R/W] 00000000	ELVR3 [R/W] 00000000 00000000		Ext. INT 24 to 31 (MB91V280 only)
000138H	EIRR4 [R/W] 00000000	ENIR4 [R/W] 00000000	ELVR4 [R/W] 00000000 00000000		Ext. INT 32 to 39 (MB91V280 only)
00013CH	—	DACR [R/W] -----000	DADR0 [R/W] ------00 00000000		D/A Converter (MB91V280 only)
000140H	DADR1 [R/W] ------00 00000000		—	DADBL [R/W] -------0	

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000144H	—	WTDBL [R/W] B ------00	WTCR [R/W] B, H 00000000 000-00-X		Real Time Clock
000148H	—	WTBR [R/W] B ---XXXXX XXXXXXXX XXXXXXXX			
00014CH	WTHR [R/W] B, H XXXXXXXX	WTMR [R/W] B, H XXXXXXXX	WTSR [R/W] B --XXXXXX	—	
000150H	ADERH [R/W] 00000000 00000000		ADERL [R/W] 00000000 00000000		A/D Converter
000154H	ADCS1 [R/W] 00000000	ADCS0 [R, R/W] 00000000	ADCR1 [R] ------XX	ADCR0 [R] XXXXXXXX	
000158H	ADCT1 [R/W] 00010000	ADCT0 [R/W] 00101100	ADSCH [R/W] ---00000	ADECH [R/W] ---00000	
00015CH	CUCR [R/W] B, H, W -------- ---00000		CUTD [R/W] B, H, W 10000000 00000000		Clock Calibration (MB91V280 and without S-suffix models only)
000160H	CUTR1 [R] B, H, W -------- 00000000		CUTR2 [R] B, H, W 00000000 00000000		
000164H to 00016CH	—				System Reserved
000170H	UDRC1 [W] B, H 00000000	UDRC0 [W] B, H 00000000	UDCR1 [R] B, H 00000000	UDCR0 [R] B, H 00000000	Up Down Counter 0/1
000174H	UDCCH0 [R/W] B, H 00000000	UDCCL0 [R/W] B, H -0000000	—	UDCS0 [R/W] B 00000000	
000178H	UDCCH1 [R/W] B, H -0000000	UDCCL1 [R/W] B, H -0000000	—	UDCS1 [R/W] B 00000000	
00017CH	—				System Reserved
000180H	UDRC3 [W] B, H 00000000	UDRC2 [W] B, H 00000000	UDCR3 [R] B, H 00000000	UDCR2 [R] B, H 00000000	Up Down Counter 2/3
000184H	UDCCH2 [R/W] B, H 00000000	UDCCL2 [R/W] B, H -0000000	—	UDCS2 [R/W] B 00000000	
000188H	UDCCH3 [R/W] B, H -0000000	UDCCL3 [R/W] B, H -0000000	—	UDCS2 [R/W] B 00000000	
00018CH	—				System Reserved
000190H	AD2ERH [R/W] 00000000 00000000		AD2ERL [R/W] 00000000 00000000		A/D Converter 2 (MB91V280 only)
000194H	AD2CS1 [R/W] 00000000	AD2CS0 [R, R/W] 00000000	AD2CR1 [R] ------XX	AD2CR0 [R] XXXXXXXX	
000198H	AD2CT1 [R/W] 00010000	AD2CT0 [R/W] 00101100	AD2SCH [R/W] ---00000	AD2ECH [R/W] ---00000	

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
00019CH	—				System Reserved
0001A0H	CMPR [R/W] B, H --000010 11111101		—	CMCR [R/W] B, H -0010000	Clock Modulator
0001A4H	CMT1 [R/W] B, H, W 00000000 10000000		CMT2 [R/W] B, H, W 00000000 00000000		
0001A8H	CANPRE [R, R/W] 00000000	—	EISSR [R/W] B, H 00000000 00000000		CAN Clock Presc / Ext. Int. Source Sel.
0001ACH	—				System Reserved
0001B0H	PRLH0 [R/W] B, H, W XXXXXXXX	PRLL0 [R/W] B, H, W XXXXXXXX	PRLH1 [R/W] B, H, W XXXXXXXX	PRLL1 [R/W] B, H, W XXXXXXXX	PPG0 to PPG3
0001B4H	PRLH2 [R/W] B, H, W XXXXXXXX	PRLL2 [R/W] B, H, W XXXXXXXX	PRLH3 [R/W] B, H, W XXXXXXXX	PRLL3 [R/W] B, H, W XXXXXXXX	
0001B8H	PPGC0 [R/W] B, H, W 0000000X	PPGC1 [R/W] B, H, W 0000000X	PPGC2 [R/W] B, H, W 0000000X	PPGC3 [R/W] B, H, W 0000000X	
0001BCH	—				System Reserved
0001C0H	PRLH4 [R/W] B, H, W XXXXXXXX	PRLL4 [R/W] B, H, W XXXXXXXX	PRLH5 [R/W] B, H, W XXXXXXXX	PRLL5 [R/W] B, H, W XXXXXXXX	PPG4 to PPG7
0001C4H	PRLH6 [R/W] B, H, W XXXXXXXX	PRLL6 [R/W] B, H, W XXXXXXXX	PRLH7 [R/W] B, H, W XXXXXXXX	PRLL7 [R/W] B, H, W XXXXXXXX	
0001C8H	PPGC4 [R/W] B, H, W 0000000X	PPGC5 [R/W] B, H, W 0000000X	PPGC6 [R/W] B, H, W 0000000X	PPGC7 [R/W] B, H, W 0000000X	
0001CCH	—				System Reserved
0001D0H	PRLH8 [R/W] B, H, W XXXXXXXX	PRLL8 [R/W] B, H, W XXXXXXXX	PRLH9 [R/W] B, H, W XXXXXXXX	PRLL9 [R/W] B, H, W XXXXXXXX	PPG8 to PPGB
0001D4H	PRLHA [R/W] B, H, W XXXXXXXX	PRLLA [R/W] B, H, W XXXXXXXX	PRLHB [R/W] B, H, W XXXXXXXX	PRLLB [R/W] B, H, W XXXXXXXX	
0001D8H	PPGC8 [R/W] B, H, W 0000000X	PPGC9 [R/W] B, H, W 0000000X	PPGCA [R/W] B, H, W 0000000X	PPGCB [R/W] B, H, W 0000000X	
0001DCH	—				System Reserved

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
0001E0H	PRLHC [R/W] B, H, W XXXXXXXX	PRLLC [R/W] B, H, W XXXXXXXX	PRLHD [R/W] B, H, W XXXXXXXX	PRLLD [R/W] B, H, W XXXXXXXX	PPGC to PPGF
0001E4H	PRLHE [R/W] B, H, W XXXXXXXX	PRLLE [R/W] B, H, W XXXXXXXX	PRLHF [R/W] B, H, W XXXXXXXX	PRLLF [R/W] B, H, W XXXXXXXX	
0001E8H	PPGCC [R/W] B, H, W 0000000X	PPGCD [R/W] B, H, W 0000000X	PPGCE [R/W] B, H, W 0000000X	PPGCF [R/W] B, H, W 0000000X	
0001ECH	—				System Reserved
0001F0H	PPGTRG [R/W] B, H, W 00000000 00000000		PPGREVC [R/W] B, H, W 00000000 00000000		PPG0 to PPGF Enable / Reverse
0001F4H	PPGSWAP [R/W] B 00000000	—			PPG0 to PPGF Output Swap
0001F8H	CMCLKR [R/W] B ----0000	—			Clock Monitor
0001FCH	—				System Reserved
000200H	DMACA0 [R/W] 00000000 00000000 00000000 00000000				DMAC
000204H	DMACB0 [R/W] 00000000 00000000 00000000 00000000				
000208H	DMACA1 [R/W] 00000000 00000000 00000000 00000000				
00020CH	DMACB1 [R/W] 00000000 00000000 00000000 00000000				DMAC
000210H	DMACA2 [R/W] 00000000 00000000 00000000 00000000				
000214H	DMACB2 [R/W] 00000000 00000000 00000000 00000000				
000218H	DMACA3 [R/W] 00000000 00000000 00000000 00000000				
00021CH	DMACB3 [R/W] 00000000 00000000 00000000 00000000				
000220H	DMACA4 [R/W] 00000000 00000000 00000000 00000000				
000224H	DMACB4 [R/W] 00000000 00000000 00000000 00000000				
000228H to 00023CH	—				System Reserved

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000240H	DMACR [R/W] 0XX00000 XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
000244H to 0003ECH	—				System Reserved
0003F0H	BSD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit Search
0003F4H	BSD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003F8H	BSDC [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003FCH	BSRR [R] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000400H	DDR0 [R/W] B, H 00000000	DDR1 [R/W] B, H 00000000	DDR2 [R/W] B, H 00000000	DDR3 [R/W] B, H 00000000	Data Direction Registers (DDRB to DDRG are only available on the MB91V280)
000404H	DDR4 [R/W] B, H 00000000	DDR5 [R/W] B, H 00000000	DDR6 [R/W] B, H 00000000	DDR7 [R/W] B, H 00000000	
000408H	DDR8 [R/W] B, H 00000000	DDR9 [R/W] B, H 00000000	DDRA [R/W] B, H ------00	DDRB [R/W] B, H --000000	
00040CH	DDRC [R/W] B, H 00000000	DDRD [R/W] B, H 00000000	DDRE [R/W] B, H 00000000	DDRF [R/W] B, H 00000000	
000410H	DDRG [R/W] B, H 00000000	—			
000414H to 00041CH	—				System Reserved
000420H	PFR0 [R/W] B, H 00000000	PFR1 [R/W] B, H 00000000	PFR2 [R/W] B, H 00000000	PFR3 [R/W] B, H 00000000	Port Function Registers (PFRB to PFRG are only available on the MB91V280)
000424H	PFR4 [R/W] B, H 00000000	PFR5 [R/W] B, H 00000000	PFR6 [R/W] B, H 00000000	PFR7 [R/W] B, H 00000000	
000428H	PFR8 [R/W] B, H 00000000	PFR9 [R/W] B, H 00000000	PFRA [R/W] B, H ------00	PFRB [R/W] B, H --000000	
00042CH	PFRC [R/W] B, H 00000000	PFRD [R/W] B, H 00000000	PFRE [R/W] B, H 00000000	PFRF [R/W] B, H 00000000	
000430H	PFRG [R/W] B, H 00000000	—			

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000434H to 00043CH	—				System Reserved
000440H	ICR00 [R, R/W] ---11111	ICR01 [R, R/W] ---11111	ICR02 [R, R/W] ---11111	ICR03 [R, R/W] ---11111	Interrupt Control Unit
000444H	ICR04 [R, R/W] ---11111	ICR05 [R, R/W] ---11111	ICR06 [R, R/W] ---11111	ICR07 [R, R/W] ---11111	
000448H	ICR08 [R, R/W] ---11111	ICR09 [R, R/W] ---11111	ICR10 [R, R/W] ---11111	ICR11 [R, R/W] ---11111	
00044CH	ICR12 [R, R/W] ---11111	ICR13 [R, R/W] ---11111	ICR14 [R, R/W] ---11111	ICR15 [R, R/W] ---11111	
000450H	ICR16 [R, R/W] ---11111	ICR17 [R, R/W] ---11111	ICR18 [R, R/W] ---11111	ICR19 [R, R/W] ---11111	
000454H	ICR20 [R, R/W] ---11111	ICR21 [R, R/W] ---11111	ICR22 [R, R/W] ---11111	ICR23 [R, R/W] ---11111	
000458H	ICR24 [R, R/W] ---11111	ICR25 [R, R/W] ---11111	ICR26 [R, R/W] ---11111	ICR27 [R, R/W] ---11111	
00045CH	ICR28 [R, R/W] ---11111	ICR29 [R, R/W] ---11111	ICR30 [R, R/W] ---11111	ICR31 [R, R/W] ---11111	
000460H	ICR32 [R, R/W] ---11111	ICR33 [R, R/W] ---11111	ICR34 [R, R/W] ---11111	ICR35 [R, R/W] ---11111	
000464H	ICR36 [R, R/W] ---11111	ICR37 [R, R/W] ---11111	ICR38 [R, R/W] ---11111	ICR39 [R, R/W] ---11111	
000468H	ICR40 [R, R/W] ---11111	ICR41 [R, R/W] ---11111	ICR42 [R, R/W] ---11111	ICR43 [R, R/W] ---11111	
00046CH	ICR44 [R, R/W] ---11111	ICR45 [R, R/W] ---11111	ICR46 [R, R/W] ---11111	ICR47 [R, R/W] ---11111	
000470H to 00047CH	—				System Reserved
000480H	RSRR [R, R/W] 10000000	STCR [R/W] 00110011	TBCR [R/W] 00XXXX00	CTBR [W] XXXXXXXX	Clock Control Unit
000484H	CLKR [R/W] 00000000	WPR [W] XXXXXXXX	DIVR0 [R/W] 00000011	DIVR1 [R/W] 00000000	
000488H	—		OSCCR [R/W] XXXXXXX0	—	
00048CH	—				System Reserved
000490H	OSCR [W, R/W] 00000000	—			Stb. Wait Timer

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000494H to 0004A8H	—				System Reserved
0004ACH	—	CSVCR [R/W] 0001XX00	—		Clock Supervisor
0004B0H to 0004FCH	—				System Reserved
000500H	PPER0 [R/W] B, H 00000000	PPER1 [R/W] B, H 00000000	PPER2 [R/W] B, H 00000000	PPER3 [R/W] B, H 00000000	Port Pull-up/down Enable Registers (PPERB to PPERG are only available on the MB91V280)
000504H	PPER4 [R/W] B, H 00000000	PPER5 [R/W] B, H 00000000	PPER6 [R/W] B, H 00000000	PPER7 [R/W] B, H 00000000	
000508H	PPER8 [R/W] B, H 00000000	PPER9 [R/W] B, H 00000000	PPERA [R/W] B, H ------00	PPERB [R/W] B, H --000000	
00050CH	PPERC [R/W] B, H 00000000	PPERD [R/W] B, H 00000000	PPERE [R/W] B, H 00000000	PPERF [R/W] B, H 00000000	
000510H	PPERG [R/W] B, H 00000000	—			
000514H to 00051CH	—				System Reserved
000520H	PPCR0 [R/W] B, H 00000000	PPCR1 [R/W] B, H 00000000	PPCR2 [R/W] B, H 00000000	PPCR3 [R/W] B, H 00000000	Port Pull-up/down Control Registers (PPCRB to PPCRG are only available on the MB91V280)
000524H	PPCR4 [R/W] B, H 00000000	PPCR5 [R/W] B, H 00000000	PPCR6 [R/W] B, H 00000000	PPCR7 [R/W] B, H 00000000	
000528H	PPCR8 [R/W] B, H 00000000	PPCR9 [R/W] B, H 00000000	PPCRA [R/W] B, H ------00	PPCRB [R/W] B, H --000000	
00052CH	PPCRC [R/W] B, H 00000000	PPCRD [R/W] B, H 00000000	PPCRE [R/W] B, H 00000000	PPCRF [R/W] B, H 00000000	
000530H	PPCRG [R/W] B, H 00000000	—			
000534H to 00053CH	—				System Reserved

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000540H	PILR0 [R/W] B, H 00000000	PILR1 [R/W] B, H 00000000	PILR2 [R/W] B, H 00000000	PILR3 [R/W] B, H 00000000	Port Input Level select Registers (PILRB to PILRG are only available on the MB91V280)
000544H	PILR4 [R/W] B, H 00000000	PILR5 [R/W] B, H 00000000	PILR6 [R/W] B, H 00000000	PILR7 [R/W] B, H 00000000	
000548H	PILR8 [R/W] B, H 00000000	PILR9 [R/W] B, H 00000000	PILRA [R/W] B, H ------00	PILRB [R/W] B, H --000000	
00054CH	PILRC [R/W] B, H 00000000	PILRD [R/W] B, H 00000000	PILRE [R/W] B, H 00000000	PILRF [R/W] B, H 00000000	
000550H	PILRG [R/W] 00000000	—			
000554H to 00055CH	—				System Reserved
000560H	IBCR0 [R/W] 00000000	IBSR0 [R] 00000000	ITBAH0 [R/W] ------00	ITBAL0 [R/W] 00000000	I²C 0
000564H	ITMKH0 [R/W, R] 00----11	ITMKL0 [R/W] 11111111	ISMK0 [R/W] 01111111	ISBA0 [R/W] -0000000	
000568H	—	IDAR0 [R/W] 00000000	ICCR0 [R/W] -0011111	—	
00056CH	—				System Reserved
000570H	IBCR1 [R/W] 00000000	IBSR1 [R] 00000000	ITBAH1 [R/W] ------00	ITBAL1 [R/W] 00000000	I²C 1
000574H	ITMKH1 [R/W, R] 00----11	ITMKL1 [R/W] 11111111	ISMK1 [R/W] 01111111	ISBA1 [R/W] -0000000	
000578H	—	IDAR1 [R/W] 00000000	ICCR1 [R/W] -0011111	—	
00057CH	—				System Reserved
000580H	IBCR2 [R/W] 00000000	IBSR2 [R] 00000000	ITBAH2 [R/W] ------00	ITBAL2 [R/W] 00000000	I²C 2
000584H	ITMKH2 [R/W, R] 00----11	ITMKL2 [R/W] 11111111	ISMK2 [R/W] 01111111	ISBA2 [R/W] -0000000	
000588H	—	IDAR2 [R/W] 00000000	ICCR2 [R/W] -0011111	—	
00058CH	—				System Reserved
000590H to 0005F8H	—				System Reserved
0005FCH	—	HWDCS [R/W] B, H 00011000	—		Hardware Watchdog

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000600H	EPFR0 [R/W] B, H 00000000	EPFR1 [R/W] B, H 00000000	EPFR2 [R/W] B, H 00000000	EPFR3 [R/W] B, H 00000000	Extra Port Function Register (EPFRB to EPFRG are only available on the MB91V280)
000604H	EPFR4 [R/W] B, H 00000000	EPFR5 [R/W] B, H 00000000	EPFR6 [R/W] B, H 00000000	EPFR7 [R/W] B, H 00000000	
000608H	EPFR8 [R/W] B, H 00000000	EPFR9 [R/W] B, H 00000000	EPFRA [R/W] B, H ------00	EPFRB [R/W] B, H --000000	
00060CH	EPFRC [R/W] B, H 00000000	EPFRD [R/W] B, H 00000000	EPFRE [R/W] B, H 00000000	EPFRF [R/W] B, H 00000000	
000610H	EPFRG [R/W] B, H 00000000	—			
000614H to 00061CH	—				System Reserved
000620H	PIDR0 [R] B, H XXXXXXXX	PIDR1 [R] B, H XXXXXXXX	PIDR2 [R] B, H XXXXXXXX	PIDR3 [R] B, H XXXXXXXX	Input Data Direct Read Data Register (PIDRB to PDIRG are only available on the MB91V280)
000624H	PIDR4 [R] B, H XXXXXXXX	PIDR5 [R] B, H XXXXXXXX	PIDR6 [R] B, H XXXXXXXX	PIDR7 [R] B, H XXXXXXXX	
000628H	PIDR8 [R] B, H XXXXXXXX	PIDR9 [R] B, H XXXXXXXX	PIDRA [R] B, H ------XX	PIDRB [R] B, H --XXXXXX	
00062CH	PIDRC [R] B, H XXXXXXXX	PIDRD [R] B, H XXXXXXXX	PIDRE [R] B, H XXXXXXXX	PIDRF [R] B, H XXXXXXXX	
000630H	PIDRG [R] B, H XXXXXXXX	—			
000634H to 00063CH	—				System Reserved
000640H	ASR0 [R/W] 00000000 00000000		ACR0 [R/W] 00110*00 00000000		T-Unit
000644H	ASR1 [R/W] XXXXXXXX XXXXXXXX		ACR1 [R/W] XXXX0X00 00X0XXXX		
000648H	ASR2 [R/W] XXXXXXXX XXXXXXXX		ACR2 [R/W] XXXX0X00 00X0XXXX		
00064CH	ASR3 [R/W] XXXXXXXX XXXXXXXX		ACR3 [R/W] 01XX0X00 00X0XXXX		

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Address	Register				Block
	+0	+1	+2	+3	
000650H to 00065CH	—				T-Unit
000660H	AWR0 [R/W] 01110000 01011011		AWR1 [R/W] XXXX0000 XX0X1XXX		
000664H	AWR2 [R/W] 0XXX0000 XX0X1XXX		AWR3 [R/W] 0XXX0000 0X0X1XXX		
000668H to 00067CH	—				
000680H	CSER [R/W] ----0001	—			
000684H to 0007F8H	—				System Reserved
0007FCH	—	MODR [W] XXXXXXXX	—		Mode Register
000800H to 000FFCH	—				System Reserved
001000H	—	DMASA0 [R/W] ----0000 00000000 00000000			DMAC
001004H	—	DMADA0 [R/W] ----0000 00000000 00000000			
001008H	—	DMASA1 [R/W] ----0000 00000000 00000000			
00100CH	—	DMADA1 [R/W] ----0000 00000000 00000000			
001010H	—	DMASA2 [R/W] ----0000 00000000 00000000			
001014H	—	DMADA2 [R/W] ----0000 00000000 00000000			
001018H	—	DMASA3 [R/W] ----0000 00000000 00000000			
00101CH	—	DMADA30 [R/W] ----0000 00000000 00000000			
001020H	—	DMASA4 [R/W] 00000000 00000000 00000000			
001024H	—	DMADA4 [R/W] 00000000 00000000 00000000			
00102BH to 006FFCH	—				System Reserved

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
007000H	FLCR [R/W] 0110X000	—			Flash I/F
007004H	FLWC [R/W] 00000011	—			
007008H to 01FFFCH	—				System Reserved
020000H	CTRLR0 [R, R/W] 00000000 00000001		STATR0 [R, R/W] 00000000 00000000		CAN 0
020004H	ERRCNT0 [R] 00000000 00000000		BTR0 [R, R/W] 00100011 00000001		
020008H	INTR0 [R] 00000000 00000000		TESTR0 [R, R/W] 00000000 00000000		CAN 0
02000CH	BRPER0 [R, R/W] 00000000 00000000		—		
020010H	IF1CREQ0 [R, R/W] 00000000 00000001		IF1CMSK0 [R, R/W] 00000000 00000000		
020014H	IF1MSK20 [R, R/W] 11111111 11111111		IF1MSK10 [R, R/W] 11111111 11111111		
020018H	IF1ARB20 [R/W] 00000000 00000000		IF1ARB10 [R/W] 00000000 00000000		
02001CH	IF1MCTR0 [R, R/W] 00000000 00000000		—		
020020H	IF1DTA10 [R/W] XXXXXXXX XXXXXXXX		IF1DTA20 [R/W] XXXXXXXX XXXXXXXX		
020024H	IF1DTB10 [R/W] XXXXXXXX XXXXXXXX		IF1DTB20 [R/W] XXXXXXXX XXXXXXXX		
020030H to 02003CH	System Reserved (IF1 data mirror, little endian byte ordering)				
020040H	IF2CREQ0 [R, R/W] 00000000 00000001		IF2CMSK0 [R, R/W] 00000000 00000000		
020044H	IF2MSK20 [R, R/W] 11111111 11111111		IF2MSK10 [R, R/W] 11111111 11111111		
020048H	IF2ARB20 [R/W] 00000000 00000000		IF2ARB10 [R/W] 00000000 00000000		
02004CH	IF2MCTR0 [R, R/W] 00000000 00000000		—		
020050H	IF2DTA10 [R/W] XXXXXXXX XXXXXXXX		IF2DTA20 [R/W] XXXXXXXX XXXXXXXX		
020054H	IF2DTB10 [R/W] XXXXXXXX XXXXXXXX		IF2DTB20 [R/W] XXXXXXXX XXXXXXXX		

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
020060H to 02007CH	System Reserved (IF2 data mirror, little endian byte ordering)				CAN 0
020080H	TREQR20 [R] 00000000 00000000		TREQR10 [R] 00000000 00000000		
020090H	NEWDT20 [R] 00000000 00000000		NEWDT10 [R] 00000000 00000000		
0200A0H	INTPND20 [R] 00000000 00000000		INTPND10 [R] 00000000 00000000		
0200B0H	MSGVAL20 [R] 00000000 00000000		MSGVAL10 [R] 00000000 00000000		
0200B4H to 0200FCH	—				System Reserved
020100H	CTRLR1 [R, R/W] 00000000 00000001		STATR1 [R, R/W] 00000000 00000000		CAN 1 (MB91V280 only)
020104H	ERRCNT1 [R] 00000000 00000000		BTR1 [R, R/W] 00100011 00000001		
020108H	INTR1 [R] 00000000 00000000		TESTR1 [R, R/W] 00000000 00000000		
02010CH	BRPER1 [R, R/W] 00000000 00000000		—		
020110H	IF1CREQ1 [R, R/W] 00000000 00000001		IF1CMSK1 [R, R/W] 00000000 00000000		
020114H	IF1MSK21 [R, R/W] 11111111 11111111		IF1MSK11 [R, R/W] 11111111 11111111		
020118H	IF1ARB21 [R/W] 00000000 00000000		IF1ARB11 [R/W] 00000000 00000000		
02011CH	IF1MCTR1 [R, R/W] 00000000 00000000		—		
020120H	IF1DTA11 [R/W] XXXXXXXX XXXXXXXX		IF1DTA21 [R/W] XXXXXXXX XXXXXXXX		
020124H	IF1DTB11 [R/W] XXXXXXXX XXXXXXXX		IF1DTB21 [R/W] XXXXXXXX XXXXXXXX		
020130H to 02013CH	System Reserved (IF1 data mirror, little endian byte ordering)				
020140H	IF2CREQ1 [R, R/W] 00000000 00000001		IF2CMSK1 [R, R/W] 00000000 00000000		
020144H	IF2MSK21 [R, R/W] 11111111 11111111		IF2MSK11 [R, R/W] 11111111 11111111		
020148H	IF2ARB21 [R/W] 00000000 00000000		IF2ARB11 [R/W] 00000000 00000000		

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
02014CH	IF2MCTR1 [R, R/W] 00000000 00000000		—		CAN 1 (MB91V280 only)
020150H	IF2DTA11 [R/W] XXXXXXXX XXXXXXXX		IF2DTA21 [R/W] XXXXXXXX XXXXXXXX		
020154H	IF2DTB11 [R/W] XXXXXXXX XXXXXXXX		IF2DTB21 [R/W] XXXXXXXX XXXXXXXX		
020160H to 02017CH	System Reserved (IF2 data mirror, little endian byte ordering)				
020180H	TREQR21 [R] 00000000 00000000		TREQR11 [R] 00000000 00000000		
020190H	NEWDT21 [R] 00000000 00000000		NEWDT11 [R] 00000000 00000000		
0201A0H	INTPND21 [R] 00000000 00000000		INTPND11 [R] 00000000 00000000		
0201B0H	MSGVAL21 [R] 00000000 00000000		MSGVAL11 [R] 00000000 00000000		
020200H	CTRLR2 [R, R/W] 00000000 00000001		STATR2 [R, R/W] 00000000 00000000		CAN 2 (MB91V280 only)
020204H	ERRCNT2 [R] 00000000 00000000		BTR2 [R, R/W] 00100011 00000001		
020208H	INTR2 [R] 00000000 00000000		TESTR2 [R, R/W] 00000000 00000000		
02020CH	BRPER2 [R, R/W] 00000000 00000000		—		
020210H	IF1CREQ2 [R, R/W] 00000000 00000001		IF1CMSK2 [R, R/W] 00000000 00000000		
020214H	IF1MSK22 [R, R/W] 11111111 11111111		IF1MSK12 [R, R/W] 11111111 11111111		
020218H	IF1ARB22 [R/W] 00000000 00000000		IF1ARB12 [R/W] 00000000 00000000		
02021CH	IF1MCTR2 [R, R/W] 00000000 00000000		—		
020220H	IF1DTA12 [R/W] XXXXXXXX XXXXXXXX		IF1DTA22 [R/W] XXXXXXXX XXXXXXXX		
020224H	IF1DTB12 [R/W] XXXXXXXX XXXXXXXX		IF1DTB22 [R/W] XXXXXXXX XXXXXXXX		
020230H to 02023CH	System Reserved (IF1 data mirror, little endian byte ordering)				
020240H	IF2CREQ2 [R, R/W] 00000000 00000001		IF2CMSK2 [R, R/W] 00000000 00000000		

(Continued)

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
020244H	IF2MSK22 [R, R/W] 11111111 11111111		IF2MSK12 [R, R/W] 11111111 11111111		CAN 2 (MB91V280 only)
020248H	IF2ARB22 [R/W] 00000000 00000000		IF2ARB12 [R/W] 00000000 00000000		
02024CH	IF2MCTR2 [R, R/W] 00000000 00000000		—		
020250H	IF2DTA12 [R/W] XXXXXXXX XXXXXXXX		IF2DTA22 [R/W] XXXXXXXX XXXXXXXX		
020254H	IF2DTB12 [R/W] XXXXXXXX XXXXXXXX		IF2DTB22 [R/W] XXXXXXXX XXXXXXXX		
020260H to 02027CH	System Reserved (IF2 data mirror, little endian byte ordering)				
020280H	TREQR22 [R] 00000000 00000000		TREQR12 [R] 00000000 00000000		
020290H	NEWDT22 [R] 00000000 00000000		NEWDT12 [R] 00000000 00000000		
0202A0H	INTPND22 [R] 00000000 00000000		INTPND12 [R] 00000000 00000000		
0202B0H	MSGVAL22 [R] 00000000 00000000		MSGVAL12 [R] 00000000 00000000		
034000H to 03FFFCH	—				F-bus RAM (MB91V280)
03A000H to 03FFFCH	—				F-bus RAM (MB91F273 (S))
080000H to 0FFFFCH	—				Flash memory (MB91F273 (S))

■ INTERRUPT VECTOR

Interrupt source	Interrupt number		Interrupt level		Interrupt vector		DMA	
	Decimal	Hexa-decimal	Register	Address	Offset	TBR default address	RN	Stop
Reset	0	00	—	—	3FC$_H$	000FFFFC$_H$	—	—
Mode vector	1	01	—	—	3F8$_H$	000FFFF8$_H$	—	—
System reserved	2	02	—	—	3F4$_H$	000FFFF4$_H$	—	—
System reserved	3	03	—	—	3F0$_H$	000FFFF0$_H$	—	—
System reserved	4	04	—	—	3EC$_H$	000FFFEC$_H$	—	—
System reserved	5	05	—	—	3E8$_H$	000FFFE8$_H$	—	—
System reserved	6	06	—	—	3E4$_H$	000FFFE4$_H$	—	—
Coprocessor absent trap	7	07	—	—	3E0$_H$	000FFFE0$_H$	—	—
Coprocessor error trap	8	08	—	—	3DC$_H$	000FFFDC$_H$	—	—
INTE instruction	9	09	—	—	3D8$_H$	000FFFD8$_H$	—	—
System reserved	10	0A	—	—	3D4$_H$	00FFFD4C$_H$	—	—
System reserved	11	0B	—	—	3D0$_H$	000FFFD0$_H$	—	—
Step trace trap	12	0C	—	—	3CC$_H$	000FFFCC$_H$	—	—
NMI request (tool)	13	0D	—	—	3C8$_H$	000FFFC8$_H$	—	—
Undefined instruction exception	14	0E	—	—	3C4$_H$	000FFFC4$_H$	—	—
NMI request	15	0F	15 (F$_H$) fixed	—	3C0$_H$	000FFFC0$_H$	—	—
External interrupt 0	16	10	ICR00	0x440	3BC$_H$	000FFFBC$_H$	6	—
External interrupt 1	17	11	ICR01	0x441	3B8$_H$	000FFFB8$_H$	7	—
External interrupt 2	18	12	ICR02	0x442	3B4$_H$	000FFFB4$_H$	—	—
External interrupt 3	19	13	ICR03	0x443	3B0$_H$	000FFFB0$_H$	—	—
External interrupt 4	20	14	ICR04	0x444	3AC$_H$	000FFFAC$_H$	—	—
External interrupt 5	21	15	ICR05	0x445	3A8$_H$	000FFFA8$_H$	—	—
External interrupt 6	22	16	ICR06	0x446	3A4$_H$	000FFFA4$_H$	—	—
External interrupt 7	23	17	ICR07	0x447	3A0$_H$	000FFFA0$_H$	—	—
Reload timer 0	24	18	ICR08	0x448	39C$_H$	000FFF9C$_H$	8	—
Reload timer 1	25	19	ICR09	0x449	398$_H$	000FFF98$_H$	9	—
Reload timer 2	26	1A	ICR10	0x44A	394$_H$	000FFF94$_H$	10	—
LIN-UART 0 reception	27	1B	ICR11	0x44B	390$_H$	000FFF90$_H$	0	Stop
LIN-UART 0 transmission	28	1C	ICR12	0x44C	38C$_H$	000FFF8C$_H$	3	—
LIN-UART 1 reception	29	1D	ICR13	0x44D	388$_H$	000FFF88$_H$	1	Stop
LIN-UART 1 transmission	30	1E	ICR14	0x44E	384$_H$	000FFF84$_H$	4	—

(Continued)

Interrupt source	Interrupt number		Interrupt level		Interrupt vector		DMA	
	Decimal	Hexa-decimal	Register	Address	Offset	TBR default address	RN	Stop
LIN-UART 2 reception	31	1F	ICR15	0x44F	380_H	$000FFF80_H$	2	Stop
LIN-UART 2 transmission	32	20	ICR16	0x450	$37C_H$	$000FFF7C_H$	5	—
CAN 0	33	21	ICR17	0x451	378_H	$000FFF78_H$	—	—
CAN 1/ICU 6/7*	34	22	ICR18	0x452	374_H	$000FFF74_H$	—	—
CAN 2*	35	23	ICR19	0x453	370_H	$000FFF70_H$	—	—
LIN-UART 3/5 reception	36	24	ICR20	0x454	$36C_H$	$000FFF6C_H$	—	—
LIN-UART 3/5 transmission	37	25	ICR21	0x455	368_H	$000FFF68_H$	—	—
LIN-UART 4/6 reception	38	26	ICR22	0x456	364_H	$000FFF64_H$	—	—
LIN-UART 4/6 transmission	39	27	ICR23	0x457	360_H	$000FFF60_H$	—	—
I^2C 0	40	28	ICR24	0x458	$35C_H$	$000FFF5C_H$	—	—
I^2C 1/UDC 2	41	29	ICR25	0x459	358_H	$000FFF58_H$	—	—
I^2C 2	42	2A	ICR26	0x45A	354_H	$000FFF54_H$	—	—
A/D converter	43	2B	ICR27	0x45B	350_H	$000FFF50_H$	14	—
RTC	44	2C	ICR28	0x45C	$34C_H$	$000FFF4C_H$	—	—
UDC 1	45	2D	ICR29	0x45D	348_H	$000FFF48_H$	—	—
Main oscillation stabilization wait timer	46	2E	ICR30	0x45E	344_H	$000FFF44_H$	—	—
TBT overflow	47	2F	ICR31	0x45F	340_H	$000FFF40_H$	—	—
PPG 0/1/4/5	48	30	ICR32	0x460	$33C_H$	$000FFF3C_H$	—	—
PPG 2/3/6/7	49	31	ICR33	0x461	338_H	$000FFF38_H$	—	—
PPG 8/9/C/D	50	32	ICR34	0x462	334_H	$000FFF34_H$	—	—
PPG A/B/E/F	51	33	ICR35	0x463	330_H	$000FFF30_H$	—	—
FRT 0/1	52	34	ICR36	0x464	$32C_H$	$000FFF2C_H$	—	—
FRT 2/3	53	35	ICR37	0x465	328_H	$000FFF28_H$	—	—
ICU 0/1/2/3	54	36	ICR38	0x466	324_H	$000FFF24_H$	—	—
ICU 4/5	55	37	ICR39	0x467	320_H	$000FFF20_H$	—	—
OCU 0/1/2/3 UDC 3	56	38	ICR40	0x468	$31C_H$	$000FFF1C_H$	—	—
OCU 4/5/6/7	57	39	ICR41	0x469	318_H	$000FFF18_H$	—	—
UDC 0	58	3A	ICR42	0x46A	314_H	$000FFF14_H$	—	—
External interrupt 8/9/10/11	59	3B	ICR43	0x46B	310_H	$000FFF10_H$	—	—
External interrupt 12 to 39*	60	3C	ICR44	0x46C	$30C_H$	$000FFF0C_H$	—	—
ROM correction interrupt	61	3D	ICR45	0x46D	308_H	$000FFF08_H$	—	—
DMA	62	3E	ICR46	0x46E	304_H	$000FFF04_H$	—	—
Delay interrupt	63	3F	ICR47	0x46F	300_H	$000FFF00_H$	—	—

(Continued)

(Continued)

Interrupt source	Interrupt number		Interrupt level		Interrupt vector		DMA	
	Decimal	Hexa-decimal	Register	Address	Offset	TBR default address	RN	Stop
System reserved (REALOS)	64	40	—	—	2FC$_H$	000FFEFC$_H$	—	—
System reserved (REALOS)	65	41	—	—	2F8$_H$	000FFEF8$_H$	—	—
System reserved	66	42	—	—	2F4$_H$	000FFEF4$_H$	—	—
System reserved	67	43	—	—	2F0$_H$	000FFEF0$_H$	—	—
System reserved	68	44	—	—	2EC$_H$	000FFEEC$_H$	—	—
System reserved	69	45	—	—	2E8$_H$	000FFEE8$_H$	—	—
System reserved	70	46	—	—	2E4$_H$	000FFEE4$_H$	—	—
System reserved	71	47	—	—	2E0$_H$	000FFEE0$_H$	—	—
System reserved	72	48	—	—	2DC$_H$	000FFEDC$_H$	—	—
System reserved	73	49	—	—	2D8$_H$	000FFED8$_H$	—	—
System reserved	74	4A	—	—	2D4$_H$	000FFED4$_H$	—	—
System reserved	75	4B	—	—	2D0$_H$	000FFED0$_H$	—	—
System reserved	76	4C	—	—	2CC$_H$	000FFECC$_H$	—	—
System reserved	77	4D	—	—	2C8$_H$	000FFEC8$_H$	—	—
System reserved	78	4E	—	—	2C4$_H$	000FFEC4$_H$	—	—
System reserved	79	4F	—	—	2C0$_H$	000FFEC0$_H$	—	—
Used by INT instruction	80 to 255	50 to FF	—	—	2BC$_H$ to 000$_H$	000FFEBC$_H$ to 000FFC00$_H$	—	—

* : CAN1, CAN2, and external interrupts 16 to 39 are only available on the MB91V280.

■ PIN STATES IN EACH CPU STATE

• Pin states in single-chip mode

Port name	Specified function name	At initialization			Sleep Sub sleep	In stop mode In RTC mode		Remarks
		Function name	Internal ROM mode vector (MD2-0 = 000)			HIZ = 0	HIZ = 1	
			INIT	RST				
P00	INT8 SIN5	P00	Output Hi-Z Input enabled	Output Hi-Z Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z Input disconnect	*1
P01	INT9 SOT5	P01						
P02	INT10 SCK5	P02						
P03	INT11 SIN6	P03						
P04	INT12 SOT6	P04						
P05	INT13 SCK6	P05						
P06	INT14	P06						
P07	INT15	P07						
P10	TIN1	P10	Output Hi-Z Input enabled	Output Hi-Z Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z Input disconnect	
P11	TOT1	P11						
P12	SIN3 INT11R	P12						*1
P13	SOT3	P13						
P14	SCK3	P14						
P15	SIN4	P15						
P16	SOT4	P16						
P17	SCK4	P17						
P20	PPG9	P20	Output Hi-Z Input enabled	Output Hi-Z Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z Input disconnect	
P21	PPGB	P21						
P22	PPGD	P22						
P23	PPGF	P23						
P24	IN0	P24						
P25	IN1	P25						
P26	IN2	P26						
P27	IN3	P27						

(Continued)

Port name	Specified function name	At initialization			Sleep Sub sleep	In stop mode In RTC mode		Remarks
		Function name	Internal ROM mode vector (MD2-0 = 000)			HIZ = 0	HIZ = 1	
			INIT	RST				
P30	IN4	P30	Output Hi-Z Input enabled	Output Hi-Z Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z Input disconnect	
P31	IN5	P31						
P32	RX2 INT10R	P32						*1
P33	TX2	P33						
P34	OUT4	P34						
P35	OUT5	P35						
P36	OUT6	P36						
P37	OUT7	P37						
P40	—	P40	Output Hi-Z Input enabled	Output Hi-Z Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z Input disconnect	
P41	—	P41						
P42	IN6 INT9R	P42	Output Hi-Z Input enabled	Output Hi-Z Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z Input disconnect	*1
P43	IN7	P43						
P44	SDA0 FRCK0	P44						
P45	SCL0 FRCK1 AIN2	P45						
P46	SDA1 BIN2	P46						
P47	SCL1 ZIN2	P47						
P50	AN8 SIN2	P50	Output Hi-Z Input enabled	Output Hi-Z Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z Input disconnect	
P51	AN9 SOT2	P51						
P52	AN10 SCK2	P52						
P53	AN11 BIN1	P53						
P54	AN12 AIN1	P54						

(Continued)

Port name	Specified function name	At initialization			Sleep Sub sleep	In stop mode In RTC mode		Remarks
		Function name	Internal ROM mode vector (MD2-0 = 000)			HIZ = 0	HIZ = 1	
			INIT	RST				
P55	AN13 ZIN1	P55	Output Hi-Z Input enabled	Output Hi-Z Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z Input disconnect	
P56	AN14 DAO0	P56						
P57	AN15 DAO1	P57						
P60	AN0 PPG0	P60	Output Hi-Z Input enabled	Output Hi-Z Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z Input disconnect	
P61	AN1 PPG2	P61						
P62	AN2 PPG4	P62						
P63	AN3 PPG6	P63						
P64	AN4 PPG8	P64						
P65	AN5 PPGA	P65						
P66	AN6 PPGC	P66						
P67	AN7 PPGE	P67						
P70	AN16 INT0	P70	Output Hi-Z Input enabled	Output Hi-Z Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z Input disconnect	*1
P71	AN17 INT1	P71						
P72	AN18 INT2	P72	Output Hi-Z Input enabled	Output Hi-Z Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z Input disconnect	
P73	AN19 INT3	P73						
P74	AN20 INT4	P74						
P75	AN21 INT5	P75						
P76	AN22 INT6 SDA2	P76						
P77	AN23 INT7 SCL2	P77						

(Continued)

Port name	Specified function name	At initialization			Sleep Sub sleep	In stop mode In RTC mode		Remarks
		Function name	Internal ROM mode vector (MD2-0 = 000)			HIZ = 0	HIZ = 1	
			INIT	RST				
P80	TIN0 ADTG INT12R	P80	Output Hi-Z Input enabled	Output Hi-Z Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z Input disconnect	*1
P81	TOT0 CKOT INT13R	P81						
P82	SIN0 TIN2 INT14R	P82						
P83	SOT0 TOT2	P83						
P84	SCK0 INT15R	P84						*1
P85	SIN1	P85						
P86	SOT1	P86						
P87	SCK1	P87						
P90	PPG1	P90	Output Hi-Z Input enabled	Output Hi-Z Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z Input disconnect	
P91	PPG3 AIN3	P91						
P92	PPG5 BIN3	P92						
P93	PPG7 ZIN3	P93						
P94	OUT0 AIN0	P94						
P95	OUT1 BIN0	P95						
P96	OUT2 ZIN0	P96						
P97	OUT3	P97						
PA0	RX0 INT8R	PA0	Output Hi-Z Input enabled	Output Hi-Z Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z Input disconnect	*1
PA1	TX0	PA1						
PB0	INT8-2 SIN5-2	PB0	Output Hi-Z Input enabled	Output Hi-Z Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z Input disconnect	*2

(Continued)

Port name	Specified function name	At initialization			Sleep Sub sleep	In stop mode In RTC mode		Remarks
		Function name	Internal ROM mode vector (MD2-0 = 000)			HIZ = 0	HIZ = 1	
			INIT	RST				
PB1	INT9-2 SOT5-2	PB1	Output Hi-Z Input enabled	Output Hi-Z Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z Input disconnect	*2
PB2	INT10-2 SCK5-2	PB2						
PB3	INT11-2 SIN6-2	PB3						
PB4	INT12-2 SOT6-2	PB4						
PB5	INT13-2 SCK6-2	PB5						
PC0	OUT4-2 INT0R	PC0	Output Hi-Z Input enabled	Output Hi-Z Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z Input disconnect	*1
PC1	OUT5-2 INT1R	PC1						
PC2	SIN3-2 INT2R	PC2						
PC3	SOT3-2 INT3R	PC3						
PC4	SCK3-2 INT4R	PC4						
PC5	SIN4-2 INT5R	PC5						
PC6	SOT4-2 INT6R	PC6	Output Hi-Z Input enabled	Output Hi-Z Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z Input disconnect	
PC7	SCK4-2 INT7R	PC7						

(Continued)

Port name	Specified function name	At initialization			Sleep Sub sleep	In stop mode In RTC mode		Remarks
		Function name	Internal ROM mode vector (MD2-0 = 000)			HIZ = 0	HIZ = 1	
			INIT	RST				
PD0	PPG9-2 INT16	PD0	Output Hi-Z Input enabled	Output Hi-Z Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z Input disconnect	*1
PD1	PPGB-2 INT17	PD1						
PD2	PPGD-2 INT18	PD2						
PD3	PPGF-2 INT19	PD3						
PD4	IN0-2 INT20	PD4						
PD5	IN1-2 INT21	PD5						
PD6	IN2-2 INT22	PD6						
PD7	IN3-2 INT23	PD7						
PE0	INT24	PE0	Output Hi-Z Input enabled	Output Hi-Z Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z Input disconnect	
PE1	INT25	PE1						
PE2	INT26	PE2						
PE3	INT27	PE3						
PE4	INT28	PE4						
PE5	INT29	PE5						
PE6	INT30	PE6						
PE7	INT31	PE7						
PF0	INT32	PF0	Output Hi-Z Input enabled	Output Hi-Z Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z Input disconnect	
PF1	INT33	PF1						
PF2	INT34	PF2						
PF3	INT35	PF3						
PF4	INT36	PF4						
PF5	INT37	PF5						
PF6	INT38	PF6						
PF7	INT39	PF7						

(Continued)

(Continued)

Port name	Specified function name	At initialization			Sleep Sub sleep	In stop mode In RTC mode		Remarks
		Function name	Internal ROM mode vector (MD2-0 = 000)			HIZ = 0	HIZ = 1	
			INIT	RST				
PG0	AN24	PG0	Output Hi-Z Input enabled	Output Hi-Z Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z Input disconnect	*1
PG1	AN25	PG1						
PG2	AN26	PG2						
PG3	AN27	PG3						
PG4	AN28	PG4						
PG5	AN29	PG5						
PG6	AN30	PG6						
PG7	AN31	PG7						

*1 : Pins become inputs and can be used to wakeup from STOP mode when the corresponding external interrupt is enabled in ENIR and the pin is selected as an external interrupt input pin in EISSR.

*2 : Pins will be available to input and can be used to restore from the STOP mode when the corresponding external interrupt is enabled in ENIR and the pin is selected as an external interrupt input pin in EPFR.

Input enabled : This indicates that the input function is available in this state.
Input disconnect : Disconnects the external input at the input gate immediately adjacent to the pin . An "L" level is passed to internal circuits.
Output Hi-Z : Turns the pin to high-impedance by preventing the pin drive transistor from driving.
Output maintained : Indicates that pins maintain the output level they had prior to changing to this mode. In other words, the pin outputs the value in accordance with the peripheral operation if the internal peripheral that uses the output is operating, and the pin maintains its output level if the pin is set as a port.
Maintain previous state : Indicates that output pins maintain the output level they had prior to this mode, or input pins continue to operate.

• Pin states in external bus mode

- The external bus interface pins will be in an output mode while the device is in the settings initialization (INIT) state. The pins is in the Hi-Z state while the $\overline{INIT}$ pin is at the “L” level. The value listed in the table is output when the $\overline{INIT}$ pin goes to the “H” level.
- The external bus interface output functions for ports 2, 3, 9, E, and F can be disabled by setting EPFR. The symbols in the table indicate :
  B : External bus interface function mode (EPFR = 0)
  P : General-purpose port or peripheral function mode (EPFR = 1)

Port name	Specified function name	At a initial/reset			Sleep Sub sleep	In stop mode In RTC mode		Remarks
		Function name	Initial Value			HIZ = 0	HIZ = 1	
			External ROM mode vector (MD2-0 = 001)	Internal ROM mode vector (MD2-0 = 000)				
P00	AD00 INT8 SIN5	AD00	Output Hi-Z Input enabled	Output Hi-Z Input enabled	Address output (MPX) Output Hi-Z Input enabled (Data)		Output Hi-Z Input discon-nect	*1
P01	AD01 INT9 SOT5	AD01						
P02	AD02 INT10 SCK5	AD02						
P03	AD03 INT11 SIN6	AD03						
P04	AD04 INT12 SOT6	AD04						
P05	AD05 INT13 SCK6	AD05						
P06	AD06 INT14	AD06						
P07	AD07 INT15	AD07						

(Continued)

Port name	Specified function name	At a initial/reset			Sleep Sub sleep	In stop mode In RTC mode		Remarks
		Function name	Initial Value			HIZ = 0	HIZ = 1	
			External ROM mode vector (MD2-0 = 001)	Internal ROM mode vector (MD2-0 = 000)				
P10	AD08 TIN1	AD08	Output Hi-Z Input enabled	Output Hi-Z Input enabled	Address output (MPX) Output Hi-Z Input enabled (Data)		Output Hi-Z Input disconnect	
P11	AD09 TOT1	AD09						
P12	AD10 SIN3 INT11R	AD10						*1
P13	AD11 SOT3	AD11						
P14	AD12 SCK3	AD12						
P15	AD13 SIN4	AD13						
P16	AD14 SOT4	AD14	Output Hi-Z Input enabled	Output Hi-Z Input enabled	Address output (MPX) Output Hi-Z Input enabled (Data)		Output Hi-Z Input disconnect	
P17	AD15 SCK4	AD15						
P20	A16 PPG9	A16	Output 0xFF	Output Hi-Z Input enabled	B : Address output P : Maintain previous state		Output Hi-Z Input disconnect	*2
P21	A17 PPGB	A17						
P22	A18 PPGD	A18						
P23	A19 PPGF	A19						
P24	A20 IN0	A20						
P25	A21 IN1	A21						
P26	A22 IN2	A22						
P27	A23 IN3	A23						

(Continued)

<table>
<tr><th rowspan="3">Port name</th><th rowspan="3">Specified function name</th><th colspan="3">At a initial/reset</th><th rowspan="2">Sleep

Sub sleep</th><th colspan="2">In stop mode
In RTC mode</th><th rowspan="3">Remarks</th></tr>
<tr><th rowspan="2">Function name</th><th colspan="2">Initial Value</th><th rowspan="2">HIZ = 0</th><th rowspan="2">HIZ = 1</th></tr>
<tr><th>External ROM mode vector (MD2-0 = 001)</th><th>Internal ROM mode vector (MD2-0 = 000)</th></tr>
<tr><td>P30</td><td>$\overline{AS}$
IN4</td><td>$\overline{AS}$</td><td rowspan="4">“H” level output</td><td rowspan="8">Output Hi-Z
Input enabled</td><td colspan="2" rowspan="4">B : “H” level output

P : Maintain previous state</td><td rowspan="8">Output
Hi-Z
Input
disconnect</td><td rowspan="2">*2</td></tr>
<tr><td>P31</td><td>$\overline{RD}$
IN5</td><td>$\overline{RD}$</td></tr>
<tr><td>P32</td><td>$\overline{WR0}$
RX2
INT10R</td><td>$\overline{WR0}$</td><td>*1
*2</td></tr>
<tr><td>P33</td><td>$\overline{WR1}$
TX2</td><td>$\overline{WR1}$</td><td>*2</td></tr>
<tr><td>P34</td><td>OUT4</td><td>P34</td><td rowspan="3">Output Hi-Z
Input enabled</td><td colspan="2" rowspan="2">Maintain previous state</td><td rowspan="3"></td></tr>
<tr><td>P35</td><td>OUT5</td><td>P35</td></tr>
<tr><td>P36</td><td>RDY
OUT6</td><td>RDY</td><td colspan="2">B : Output Hi-Z
P : Maintain previous state</td></tr>
<tr><td>P37</td><td>SYSCLK
OUT7</td><td>P37</td><td>Clock output</td><td>B :
Clock output

P :
Maintain previous state</td><td>B :
“H” level output

P :
Maintain previous state</td><td>*2</td></tr>
<tr><td>P40</td><td>—</td><td>P40</td><td colspan="6" rowspan="5">Same as single-chip mode</td></tr>
<tr><td>P41</td><td>—</td><td>P41</td></tr>
<tr><td>P42</td><td>IN6
INT9R</td><td>P42</td></tr>
<tr><td>P43</td><td>IN7</td><td>P43</td></tr>
<tr><td>P44</td><td>SDA0
FRCK0</td><td>P44</td></tr>
</table>

(Continued)

Port name	Specified function name	At a initial/reset			Sleep Sub sleep	In stop mode In RTC mode		Remarks
		Function name	Initial Value			HIZ = 0	HIZ = 1	
			External ROM mode vector (MD2-0 = 001)	Internal ROM mode vector (MD2-0 = 000)				
P45	SCL0 AIN2 FRCK1	P45	Same as single-chip mode					
P46	SDA1 BIN2	P46						
P47	SCL1 ZIN2	P47						
P50	AN8 SIN2	P50	Same as single-chip mode					
P51	AN9 SOT2	P51						
P52	AN10 SCK2	P52						
P53	AN11 BIN1	P53						
P54	AN12 AIN1	P54						
P55	AN13 ZIN1	P55						
P56	AN14 DAO0	P56						
P57	AN15 DAO1	P57						
P60	AN0 PPG0	P60	Same as single-chip mode					
P61	AN1 PPG2	P61						
P62	AN2 PPG4	P62						
P63	AN3 PPG6	P63						
P64	AN4 PPG8	P64						
P65	AN5 PPGA	P65						
P66	AN6 PPGC	P66						
P67	AN7 PPGE	P67						

(Continued)

Port name	Specified function name	At a initial/reset			Sleep Sub sleep	In stop mode In RTC mode		Remarks
		Function name	Initial Value			HIZ = 0	HIZ = 1	
			External ROM mode vector (MD2-0 = 001)	Internal ROM mode vector (MD2-0 = 000)				
P70	AN16 INT0	P70	Same as single-chip mode					
P71	AN17 INT1	P71						
P72	AN18 INT2	P72						
P73	AN19 INT3	P73						
P74	AN20 INT4	P74						
P75	AN21 INT5	P75						
P76	AN22 INT6 SDA2	P76						
P77	AN23 INT7 SCL2	P77						
P80	TIN0 ADTG INT12R	P80	Same as single-chip mode					
P81	TOT0 CKOT INT13R	P81						
P82	SIN0 TIN2 INT14R	P82						
P83	SOT0 TOT2	P83						
P84	SCK0 INT15R	P84						
P85	SIN1	P85						
P86	SOT1	P86						
P87	SCK1	P87						

(Continued)

Port name	Specified function name	At a initial/reset			Sleep	In stop mode In RTC mode		Remarks
		Function name	Initial Value		Sub sleep	HIZ = 0	HIZ = 1	
			External ROM mode vector (MD2-0 = 001)	Internal ROM mode vector (MD2-0 = 000)				
P90	$\overline{CS0}$ PPG1	$\overline{CS0}$	"H" level output	Output Hi-Z Input enabled	B : "H" level output P : Maintain previous state	Output Hi-Z Input disconnect	*2	
P91	$\overline{CS1}$ PPG3 AIN3	$\overline{CS1}$						
P92	$\overline{CS2}$ PPG5 BIN3	$\overline{CS2}$						
P93	$\overline{CS3}$ PPG7 ZIN3	$\overline{CS3}$						
P94	OUT0 AIN0	P94	Same as single-chip mode					
P95	OUT1 BIN0	P95						
P96	OUT2 ZIN0	P96						
P97	OUT3	P97						
PA0	RX0 INT8R	PA0	Same as single-chip mode					
PA1	TX0	PA1						
PB0	INT8-2 SIN5-2	PB0	Same as single-chip mode					
PB1	INT9-2 SOT5-2	PB1						
PB2	INT10-2 SCK5-2	PB2						
PB3	INT11-2 SIN6-2	PB3						
PB4	INT12-2 SOT6-2	PB4						
PB5	INT13-2 SCK6-2	PB5						

(Continued)

Port name	Specified function name	At a initial/reset			Sleep Sub sleep	In stop mode In RTC mode		Remarks
		Function name	Initial Value			HIZ = 0	HIZ = 1	
			External ROM mode vector (MD2-0 = 001)	Internal ROM mode vector (MD2-0 = 000)				
PC0	OUT4-2 INT0R	PC0	Same as single-chip mode					
PC1	OUT5-2 INT1R	PC1						
PC2	SIN3-2 INT2R	PC2						
PC3	SOT3-2 INT3R	PC3						
PC4	SCK3-2 INT4R	PC4						
PC5	SIN4-2 INT5R	PC5						
PC6	SOT4-2 INT6R	PC6						
PC7	SCK4-2 INT7R	PC7						
PD0	PPG9-2 INT16	PD0	Same as single-chip mode					
PD1	PPGB-2 INT17	PD1						
PD2	PPGD-2 INT18	PD2						
PD3	PPGF-2 INT19	PD3						
PD4	IN0-2 INT20	PD4						
PD5	IN1-2 INT21	PD5	Same as single-chip mode					
PD6	IN2-2 INT22	PD6						
PD7	IN3-2 INT23	PD7						

(Continued)

Port name	Specified function name	At a initial/reset			Sleep Sub sleep	In stop mode In RTC mode		Remarks
		Function name	Initial Value			HIZ = 0	HIZ = 1	
			External ROM mode vector (MD2-0 = 001)	Internal ROM mode vector (MD2-0 = 000)				
PE0	A00 INT24	A00	"H" level output	Output Hi-Z Input enabled	B : Address output P : Maintain previous state		Output Hi-Z Input disconnect	*1 *2
PE1	A01 INT25	A01						
PE2	A02 INT26	A02						
PE3	A03 INT27	A03						
PE4	A04 INT28	A04						
PE5	A05 INT29	A05						
PE6	A06 INT30	A06						
PE7	A07 INT31	A07						
PF0	A08 INT32	A08	"H" level output	Output Hi-Z Input enabled	B : Address output P : Maintain previous state		Output Hi-Z Input disconnect	*1 *2
PF1	A09 INT33	A09						
PF2	A10 INT34	A10						
PF3	A11 INT35	A11						
PF4	A12 INT36	A12						
PF5	A13 INT37	A13						
PF6	A14 INT38	A14						
PF7	A15 INT39	A15						
PG0	AN24	PG0	Same as single-chip mode					
PG1	AN25	PG1						
PG2	AN26	PG2						
PG3	AN27	PG3						

(Continued)

(Continued)

Port name	Specified function name	At a initial/reset			Sleep Sub sleep	In stop mode In RTC mode		Remarks
		Function name	Initial Value			HIZ = 0	HIZ = 1	
			External ROM mode vector (MD2-0 = 001)	Internal ROM mode vector (MD2-0 = 000)				
PG4	AN28	PG4	Same as single-chip mode					
PG5	AN29	PG5						
PG6	AN30	PG6						
PG7	AN31	PG7						

*1 : Pins become inputs and can be used to wakeup from STOP mode when the corresponding external interrupt is enabled in ENIR and the pin is selected as an external interrupt input pin in EISSR.

*2 : Outputs go to Hi-Z at power on or while the $\overline{\text{INIT}}$ pin is at the “L” level starting from the falling edge on the $\overline{\text{INIT}}$ pin.

Input enabled	:	This indicates that the input function is available in this state.
Input disconnect	:	Disconnects the external input at the input gate immediately adjacent to the pin . An "L" level is passed to internal circuits.
Output Hi-Z	:	Turns the pin to high-impedance by preventing the pin drive transistor from driving.
Output maintained	:	Indicates that pins maintain the output level they had prior to changing to this mode. In other words, the pin outputs the value in accordance with the peripheral operation if the internal peripheral that uses the output is operating, and the pin maintains its output level if the pin is set as a port.
Maintain previous state	:	Indicates that output pins maintain the output level they had prior to this mode, or input pins continue to operate.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	$AV_{CC} = V_{CC}$*1
	AVRH	V_{SS} – 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq$ AVRH
Input voltage	V_I	V_{SS} – 0.3	V_{CC} + 0.3	V	
Output voltage	V_O	V_{SS} – 0.3	V_{CC} + 0.3	V	
“L” level maximum output current*2	I_{OL1}	—	15	mA	
“L” level average output current*3	I_{OLAV1}	—	4	mA	
“L” level total maximum output current	ΣI_{OL1}	—	120	mA	
“L” level total average output current*4	ΣI_{OLAV1}	—	50	mA	
“H” level maximum output current*2	I_{OH1}	—	– 15	mA	
“H” level average output current*3	I_{OHAV1}	—	– 4	mA	
“H” level total maximum output current	ΣI_{OH1}	—	– 120	mA	
“H” level total average output current*4	ΣI_{OHAV1}	—	– 50	mA	
Power consumption	P_D	—	500	mW	
Operating temperature	T_A	– 40	+ 105	°C	Single-chip mode
		– 40	+ 85	°C	External bus mode
Storage temperature	Tstg	– 55	+ 150	°C	
+B Input rating (Maximum clamp current)	I_{IHH}	—	2	mA	*5

*1 : Ensure that AV_{CC} does not exceed V_{CC} when the power is turned on.

*2 : The maximum output current specifies the peak current for an individual pin.

*3 : The average output current specifies the average current that flows through an individual pin over a period of 100 ms. The average value is the operating current × operation ratio.

*4 : The total average output current specifies the average current that flows through all of the pins over a period of 100 ms. The average value is the operating current × operation ratio.

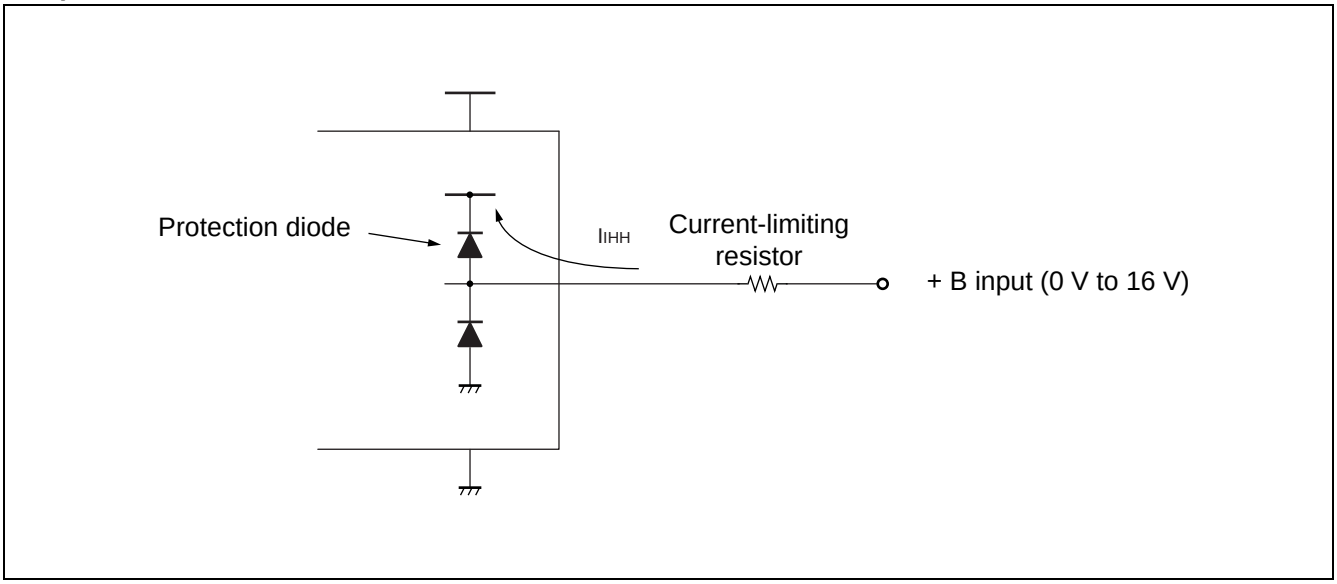
*5 : The +B input rating specifies the current for an individual pin.
[Pins applicable] P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0, PA1, PB0 to PB5, PC0 to PC7, PD0 to PD7, PE0 to PE7, PF0 to PF7, PG0 to PG7
(+B input to P56 and P57 not allowed on the MB91V280.)

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

[For +B input (12V to 16V)]

1. Do not connect the +B potential directly to a microcontroller pin.
2. Always place a current-limiting resistor between the +B signal and microcontroller pins.
   I_{IHH} = 2mA per pin (Max) [during normal operation and during transients such as when turning the power on or off]
3. Although the internal protection diode in the microcontroller causes the potential between the +B input-limiting resistor and microcontroller pin to be equal to the V_{CC} + on voltage of the protection diode, do not use a circuit structure that obstructs this operation or that causes this potential to be exceeded.

Sample recommended circuits:



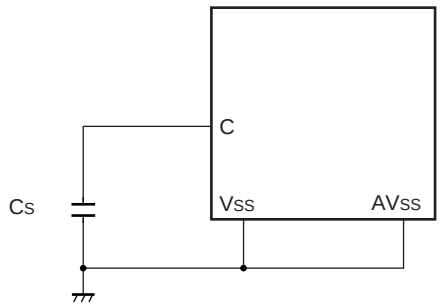
2. Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC} AV_{CC}	4.5	5.5	V	Normal operation
	V_{CC} AV_{CC}	3.5	5.5	V	Excluding A/D converter operation
	V_{CC}	3.0	5.5	V	Maintain RAM data during STOP mode
Smoothing capacitor*	C_S	1 (± 50 % tolerance)		µF	Use a ceramic capacitor or a capacitor of similar frequency characteristics. On the Vcc pin, use a bypass capacitor with a larger capacity than that of Cs.
Operating temperature	T_A	− 40	+ 105	°C	Single-chip mode
		− 40	+ 85	°C	External bus mode

* : Refer to the following figure for connection of smoothing capacitor Cs.

• C Pin Connection Diagram



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

3. DC Characteristics

(T_A : Recommended Operating Conditions, V_{CC} = 5.0 V ± 10 %, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IHS}	—	—	0.8 × V_{CC}	—	V_{CC} + 0.3	V	CMOS automotive input
	V_{IHC}	—	—	0.7 × V_{CC}	—	V_{CC} + 0.3	V	CMOS Schmitt input
	V_{IHT}	—	—	2.1	—	V_{CC} + 0.3	V	TTL input*1
	V_{IHM}	MD0 MD1 MD2	—	V_{CC} – 0.3	—	V_{CC} + 0.3	V	
	V_{IHI}	$\overline{INIT}$	—	0.8 × V_{CC}	—	V_{CC} + 0.3	V	
"L" level input voltage	V_{ILS}	—	—	V_{SS} – 0.3	—	0.5 × V_{CC}	V	CMOS automotive input
	V_{ILC}	—	—	V_{SS} – 0.3	—	0.3 × V_{CC}	V	CMOS Schmitt input
	V_{ILT}	—	—	V_{SS} – 0.3	—	0.8	V	TTL input*1
	V_{ILM}	MD0 MD1 MD2	—	V_{SS} – 0.3	—	V_{SS} + 0.3	V	
	V_{ILI}	$\overline{INIT}$	—	V_{SS} – 0.3	—	0.2 × V_{CC}	V	
Power supply current	I_{CC}	V_{CC}	*2	—	100	120	mA	Normal operation*11
			*3	—	70	90	mA	Normal operation*11
	I_{CCS}	V_{CC}	*4	—	40	55	mA	SLEEP operation*11
			*5	—	20	30	mA	SLEEP operation*11
	I_{CCL}	V_{CC}	*6	—	400	700	µA	Sub operation
	I_{CCSL}	V_{CC}	*7	—	300	600	µA	Sub-SLEEP operation
	I_{CCR32}	V_{CC}	*8	—	200	300	µA	32 kHz clock operation *12
	I_{CCR4}	V_{CC}	*9	—	700	1000	µA	4 MHz clock operation*12
	I_{CCH}	V_{CC}	*10	—	20	100	µA	STOP
Input leak current	I_{IL}	—	—	–5	—	5	µA	All input pins
Input capacitance	C_{IN}	—	—	—	5	15	pF	
Pull-up resistor	R_{UP}	—	—	25	50	100	kΩ	Selectable except for P44 to P47, P56, P57, P76, and P77
Pull-down resistor	R_{DOWN}	—	—	25	50	100	kΩ	Selectable except for P44 to P47, P56, P57, P76, and P77

(Continued)

(Continued)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level Output voltage	V_{OH}	—	I_{OH} = – 4 mA	V_{CC} – 0.5	—	—	V	Other than P44 to P47, P76 and P77
	V_{OHI}	P44 to P47 P76, P77	I_{OH} = – 3 mA	V_{CC} – 0.5	—	—	V	Pins also used for I^2C
"L" level Output voltage	V_{OL}	—	I_{OL} = 4 mA	—	—	0.4	V	Other than P44 to P47, P76 and P77
	V_{OLI}	P44 to P47 P76, P77	I_{OL} = 3 mA	—	—	0.4	V	Pins also used for I^2C

*1 : In external bus mode, only P00 to P07, P10 to P17, and P36 can be selected.

*2 : CLKB = 32 MHz, CLKP = 32 MHz, CLKT = 16 MHz, CANCLK = 16 MHz

*3 : CLKB = 32 MHz, CLKP = 8 MHz, CLKT = 4 MHz, CANCLK = 8 MHz

*4 : CPU halted for case *2.

*5 : CPU halted for case *3.

*6 : CLKB = CLKP = CLKT = CANCLK = 32 kHz, T_A = + 25 °C

*7 : CPU halted for case *6

*8 : CPU and peripheral circuits halted, main oscillation halted, 32 kHz clock operation, T_A= + 25 °C

*9 : CPU and peripheral circuits halted, sub-oscillation halted, 4 MHz clock operation, T_A= + 25 °C

*10 : CPU and peripheral circuits halted, all oscillation circuits halted, T_A = + 25 °C

*11 : The current consumption values for normal operation mode and SLEEP mode assume that the peripheral circuits are operating at maximum capacity.

*12 : The current consumption value for clock mode operation does not include the consumption of the external oscillator.

4. Flash Memory Program and Erase Characteristics

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	T_A = +25 °C V_{CC} = 5.0 V	—	1	5	s	Excludes time for internal write prior to erase.
Chip erase time	T_A = +25 °C V_{CC} = 5.0 V	—	14	—	s	Excludes time for internal write prior to erase.
Half-word write time	T_A = +25 °C V_{CC} = 5.0 V	—	16	3600	µs	Excludes system-level overhead time.
Chip write time	T_A = +25 °C V_{CC} = 5.0 V	—	2.1	—	s	Excludes system-level overhead time.
Erase/Write cycle	—	10000	—	—	cycle	
Data retention time	Average T_A = +85 °C	20*	—	—	year	

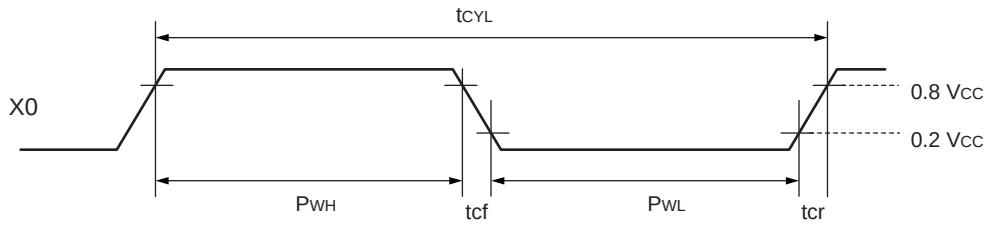
* : Calculated value based on technology reliability test data.
(Value calculated using the Arrhenius equation for the burn-in test results with an average temperature of +85 °C.)

5. AC Characteristics

(T_A : Recommended Operating Conditions, V_{CC} = 5.0 V ± 10 %, V_{SS} = AV_{SS} = 0.0 V)

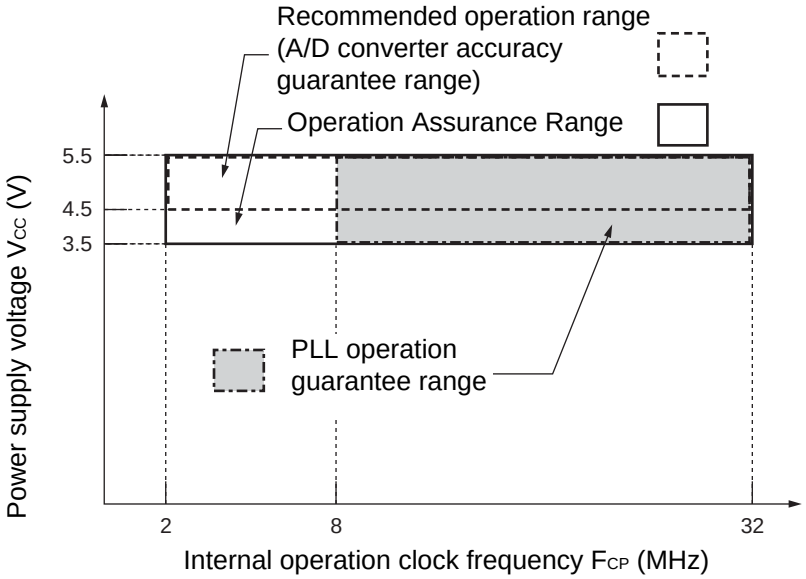
Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Source oscillation clock frequency	F_C	X0, X1	—	—	4	12	MHz	
	F_{CA}	X0A, X1A		—	32.768	100	kHz	
Source oscillation clock cycle time	t_{CYL}	X0, X1		83.3	250	—	ns	
	t_{CYLL}	X0A, X1A		10	30.5	—	µs	
Input clock pulse width	P_{WH} P_{WL}	X0		30	—	—	ns	Use a duty ratio in the range 40 % to 60 %.
Input clock rise time and fall time	tcr, tcf	X0		—	—	5	ns	When external clock is used
Internal operation clock frequency	F_{CP}	—		—	—	32	MHz	When main clock, PLL clock are used.
Internal operation clock cycle time	t_{CP}	—		31.25	—	—	ns	When main clock, PLL clock are used.

X0, X1 Clock Timing



• Operation Assurance Range

Relation between internal operation clock frequency and power supply voltage

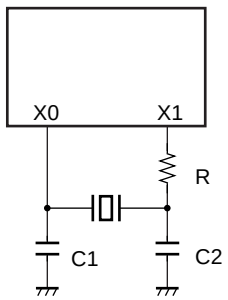


Note : Use a PLL operation stabilization wait time of 500 µs or more.

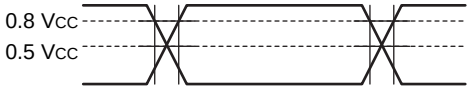
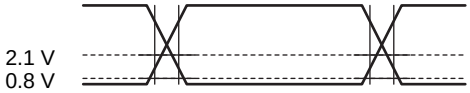
Relation between oscillation clock frequency and internal operation clock

		Internal operation clock frequency					
		Main clock	PLL clock				
			PLL multiplication rate = 2	PLL multiplication rate = 3	PLL multiplication rate = 4	PLL multiplication rate = 6	PLL multiplication rate = 8
Oscillation clock frequency	4 MHz	2 MHz	8 MHz	12 MHz	16 MHz	24 MHz	32 MHz
	8 MHz	4 MHz	16 MHz	24 MHz	32 MHz	—	—
	12 MHz	6 MHz	24 MHz	—	—	—	—

Sample oscillation circuit



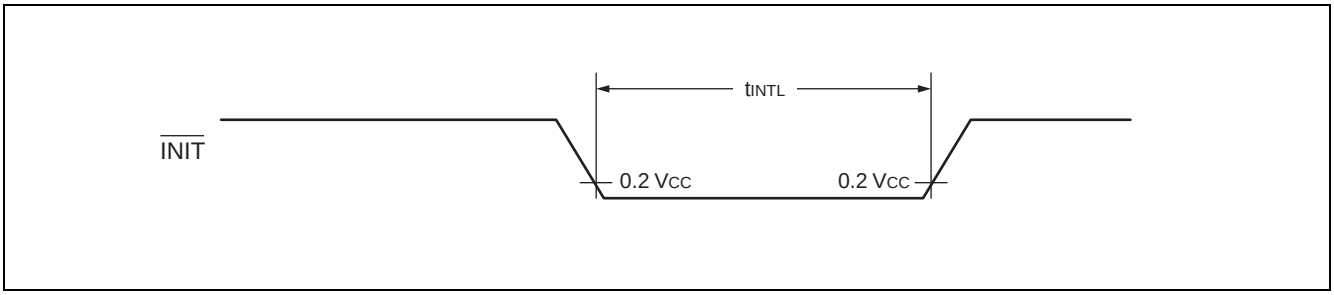
The AC standards assume the following measurement reference voltages.

Input signal waveform	Output signal waveform
Hysteresis input pin 	Output pin 
Hysteresis input pin (Automotive) 	—
TTL input pin 	—

• Reset input

(T_A : Recommended Operating Conditions, V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V)

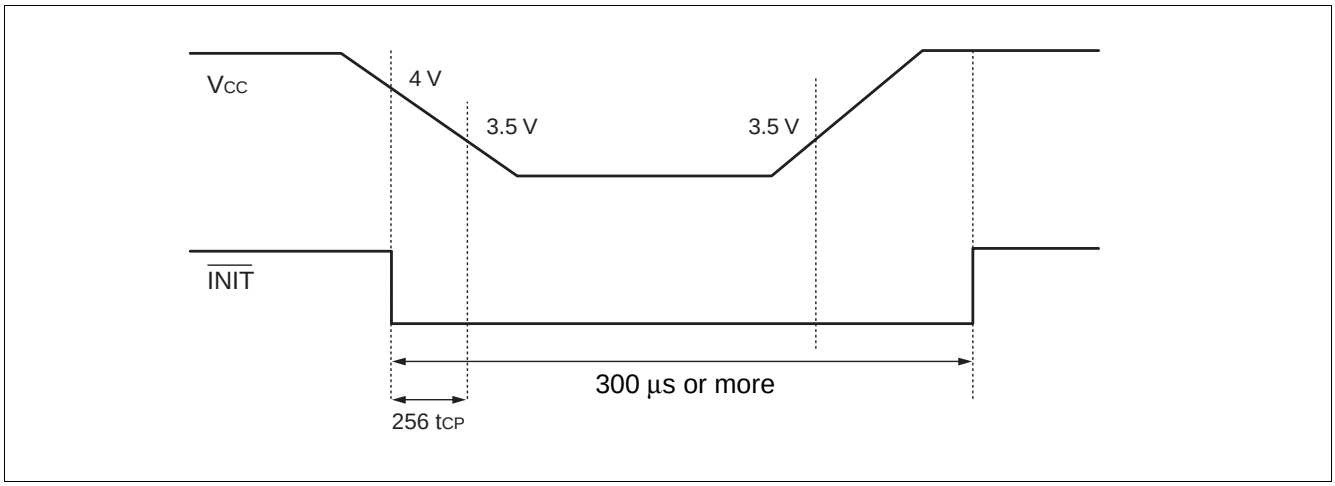
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
$\overline{INIT}$ input time	t_{INTL}	$\overline{INIT}$	—	10	—	µs	
				300	—	µs	At STOP
				8	—	ms	At power-on



The following reset input standard should be satisfied as RAM data protection standard.

V_{CC} (V)	Voltage drop time		External reset input standard ($\overline{INIT}$)	
	Min	Max	Min	Max
At drop of 4.0 ≥ 3.5 V	256 t_{CP}*	—	300 µs	—

* : t_{CP} : Period of the internal base clock.



To protect RAM data, input $\overline{INIT}$ of 256 t_{CP} or more before voltage drop at V_{CC} = 3.5 V or less.

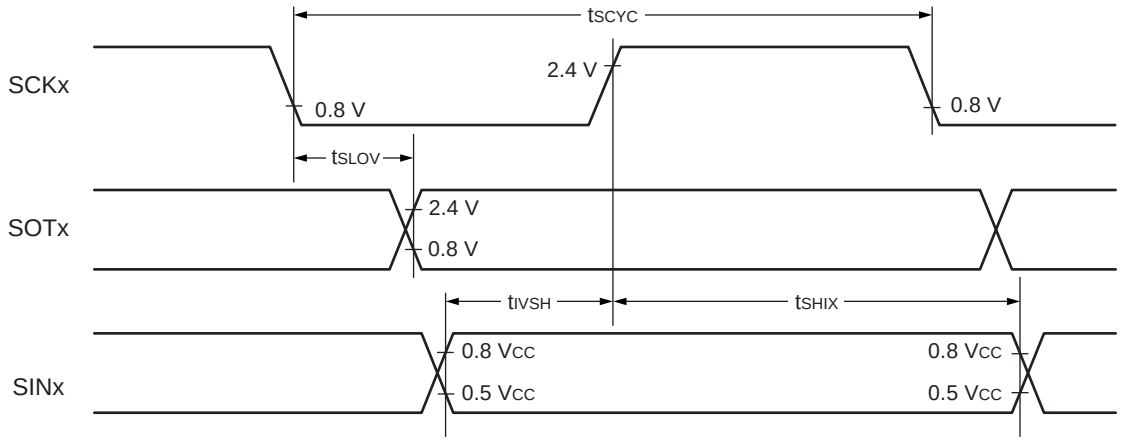
• UART Timing

(T_A : Recommended Operating Conditions, V_{CC} = 5.0 V ± 10 %, V_{SS} = AV_{SS} = 0.0 V)

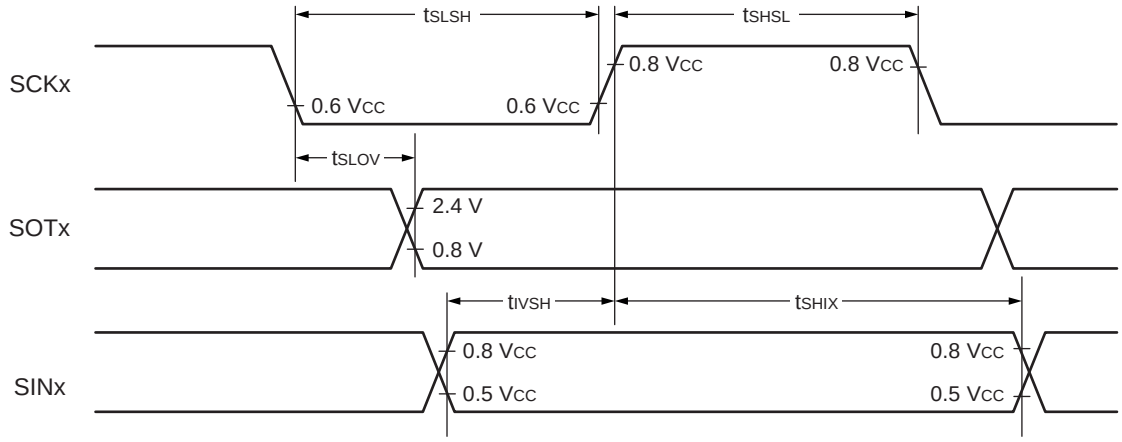
Parameter	Sym-bol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCKx	—	8 t_{CP}	—	ns	Internal shift clock mode Output pin capacitance is C_L = 80 pF + 1 × TTL
SCK↓→SOT delay time	t_{SLOV}	SCKx SOTx		– 80	+ 80	ns	
Valid SIN→SCK↑	t_{IVSH}	SCKx SINx		100	—	ns	
SCK↑→ valid SIN hold time	t_{SHIX}			60	—	ns	
Serial clock “H” pulse width	t_{SHSL}	SCKx	—	4 t_{CP}	—	ns	External shift clock mode Output pin capacitance is C_L = 80 pF + 1 × TTL
Serial clock “L” pulse width	t_{SLSH}			4 t_{CP}	—	ns	
SCK↓→SOT delay time	t_{SLOV}	SCKx SOTx		—	150	ns	
Valid SIN→SCK↑	t_{IVSH}	SCKx SINx		60	—	ns	
SCK↑→ valid SIN hold time	t_{SHIX}			60	—	ns	

Note : These are AC Characteristics in the clock synchronous mode.
C_L is the load capacitance connected to the pin for testing.

• Internal shift clock mode



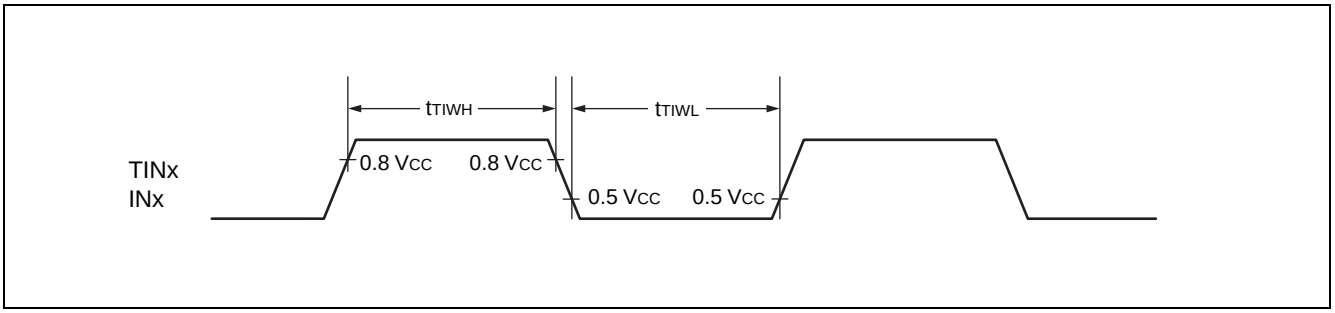
• External shift clock mode



• Timer input timing

(T_A : Recommended Operating Conditions, V_{CC} = 5.0 V ± 10 %, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH} t_{TIWL}	TINx INx	—	4 t_{CP}	—	ns	—



6. Electrical Characteristics for the A/D Converter

• Electrical characteristics

(T_A : Recommended Operating Conditions, V_{CC} = 5.0 V ± 10 %, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Sym-bol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	—	—	± 3.0	LSB	
Nonlinear error	—	—	—	—	± 2.5	LSB	
Differential linear error	—	—	—	—	± 1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN23	AV_{SS} − 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	V	1 LSB = (AVRH − AV_{SS}) / 1024
Full-scale transition voltage	V_{FST}	AN0 to AN23	AVRH − 3.5 LSB	AVRH − 1.5 LSB	AVRH + 0.5 LSB	V	
Sampling time	t_{SMP}	—	1.375	—	—	µs	*1
Compare time	t_{CMP}	—	1.375	—	—	µs	*2
A/D conversion time	t_{CNV}	—	2.750	—	—	µs	*3
Analog port input current	I_{AIN}	AN0 to AN23	—	—	10	µA	$V_{AVSS} \le V_{AIN} \le V_{AVCC}$
Analog input voltage	V_{AIN}	AN0 to AN23	0	—	AVRH	V	
Reference voltage	AVRH	AVRH	4.0	—	AV_{CC}	V	
Power supply current	I_A	AV_{CC}	—	2.4	4.7	mA	
	I_{AH}		—	—	5	µA	*4
Reference voltage supplying current	I_R	AVRH	—	600	900	µA	V_{AVRH} = 5.0 V
	I_{RH}		—	—	5	µA	*4
Interchannel disparity	—	AN0 to AN31	—	—	4	LSB	

*1 : For F_{CP} = 32 MHz, t_{SMP} = (Rext + Rin) × Cin × 7 = ST × CLKP period = 2 ch × 31.25 ns = 1.375 µs

*2 : For F_{CP} = 32 MHz, t_{CMP} = CKIN × 11 = CT × CLKP period × 11 = 4 h × 31.25 ns × 11 = 1.375 µs

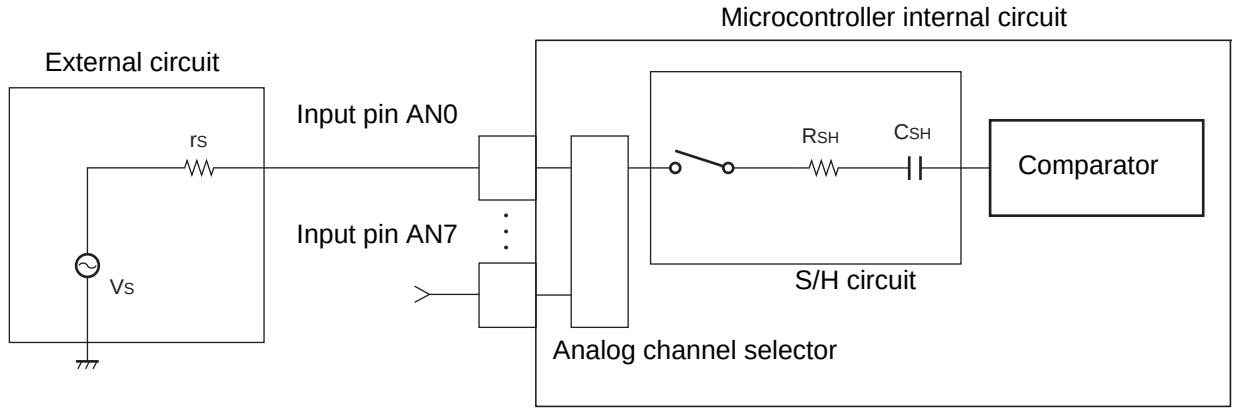
*3 : For F_{CP} = 32 MHz, this is equivalent to the conversion time per channel when t_{SMP} and t_{CMP} are selected.

*4 : Specifies the power supply current when the A/D converter is not operating and the CPU is in stop mode (Vcc = AVcc = AVRH = 5.0 V)

Notes : •The error becomes proportionately larger as the AVRH voltages go lower.

- Use the device with external circuits of the following output impedance r_S for analog inputs :
  External circuit output impedance r_S = 5 kΩ (Max)
- If the output impedance of the external circuit is too high, the analog voltage sampling time may be insufficient.
- If inserting a capacitor between the external circuit and an input pin to prevent direct current flow, select a capacitance several thousand times larger than C_{SH} to minimize the capacitive voltage divider effect due to the C_{SH} sampling capacitor in the chip.

• Analog input equivalent circuit



< Recommended parameter values for each component >
r_S : under 5 kΩ
R_{SH} = Approx. 2.5 kΩ
C_{SH} = Approx. 10 pF

Note : Parameter values for each component are indicative design values.

• Definition of terminology

Resolution

Represents the change in analog signal enabled to be detected by the A/D converter.

For 10-bit conversion, the analog voltage can be resolved into 2^{10} = 1024 increments.

Total error

This error indicates the difference between actual and theoretical values, and is the total value of errors that results from offset error, gain error, nonlinear error, and noise.

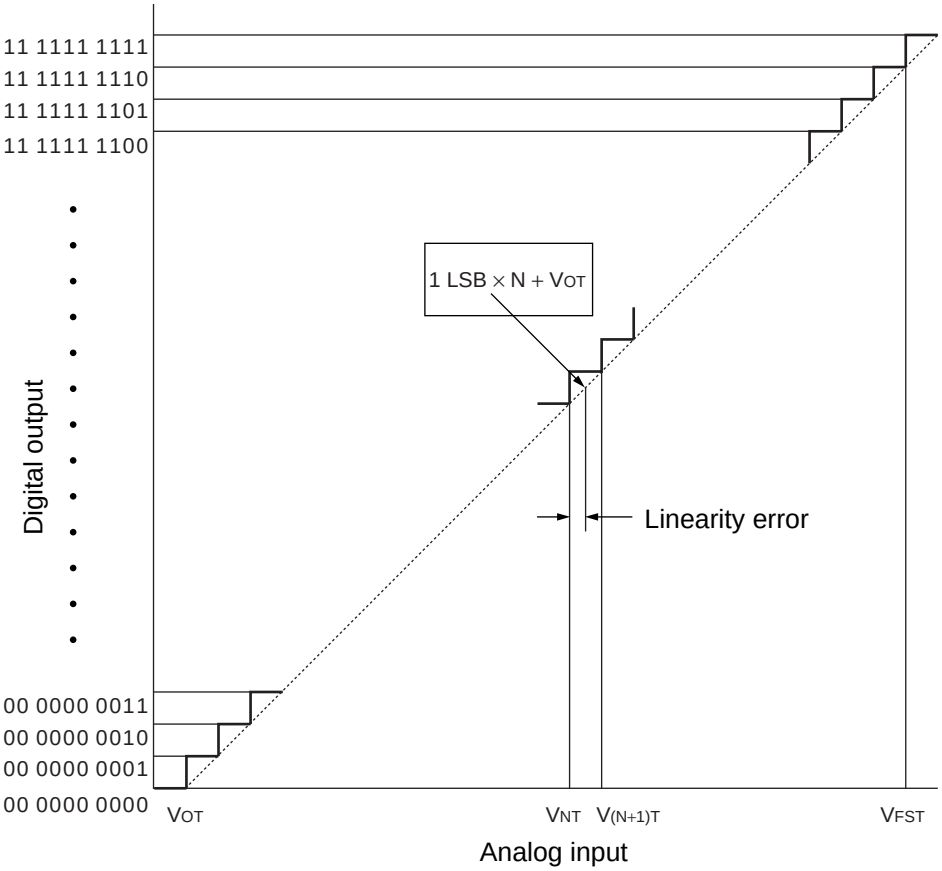
Linearity error

Represents the difference between the actual conversion characteristic and the line between the zero transition point (“00 0000 0000” ←→ “00 0000 0001”) and full scale transition point (“11 1111 1110”←→ “11 1111 1111”).

Differential linear error

Deviation of input voltage, which is required for changing output code by 1 LSB, from a desired value.

• Conversion characteristics for 10-bit A/D converter



V_{OT} = AV_{SS} + 0.5 LSB [V] (theoretical value)

V_{FST} = AVRH – 1.5 LSB [V] (theoretical value)

V_{FST} = Digital output voltage at which transition from (N – 1) to N occurs.

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}$$

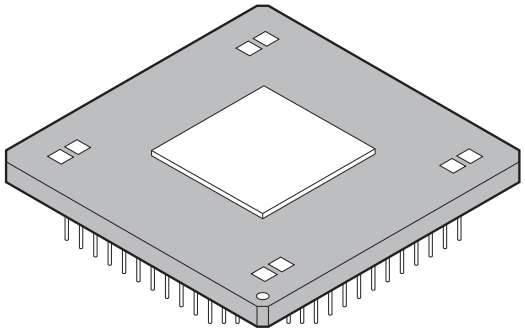
$$\text{Linearity error} = \frac{V_{NT} - (1\ \text{LSB} \times N + V_{OT})}{1\ \text{LSB}} \quad [\text{LSB}]$$

$$\text{Differential linear error} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1 \quad [\text{LSB}]$$

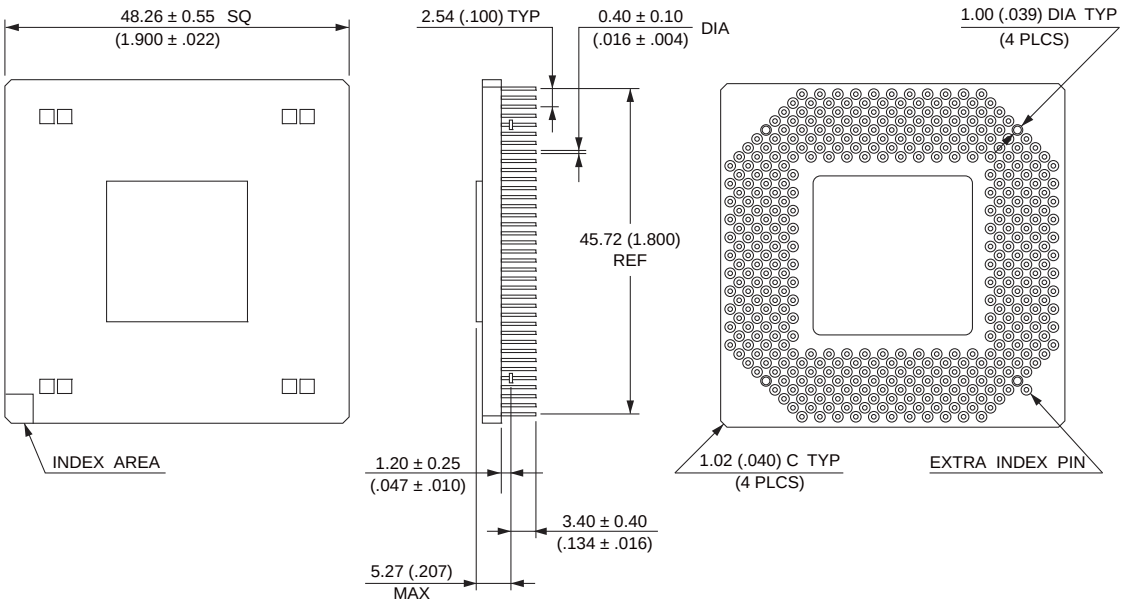
■ ORDERING INFORMATION

Part number	Package	Remarks
MB91V280CR	401-pin ceramic PGA (PGA-401C-A02)	Evaluation model
MB91F273SPMC	100-pin plastic LQFP (FPT-100P-M05)	Single clock model
MB91F273PMC	100-pin plastic LQFP (FPT-100P-M05)	Dual clock model

■ PACKAGE DIMENSIONS

401-pin ceramic PGA		
	Lead pitch	2.54 interstitial
	Pin matrix	37
	Sealing method	Metal seal
(PGA-401C-A02)		

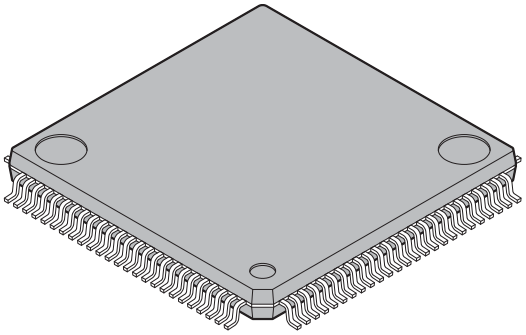
401-pin ceramic PGA
(PGA-401C-A02)



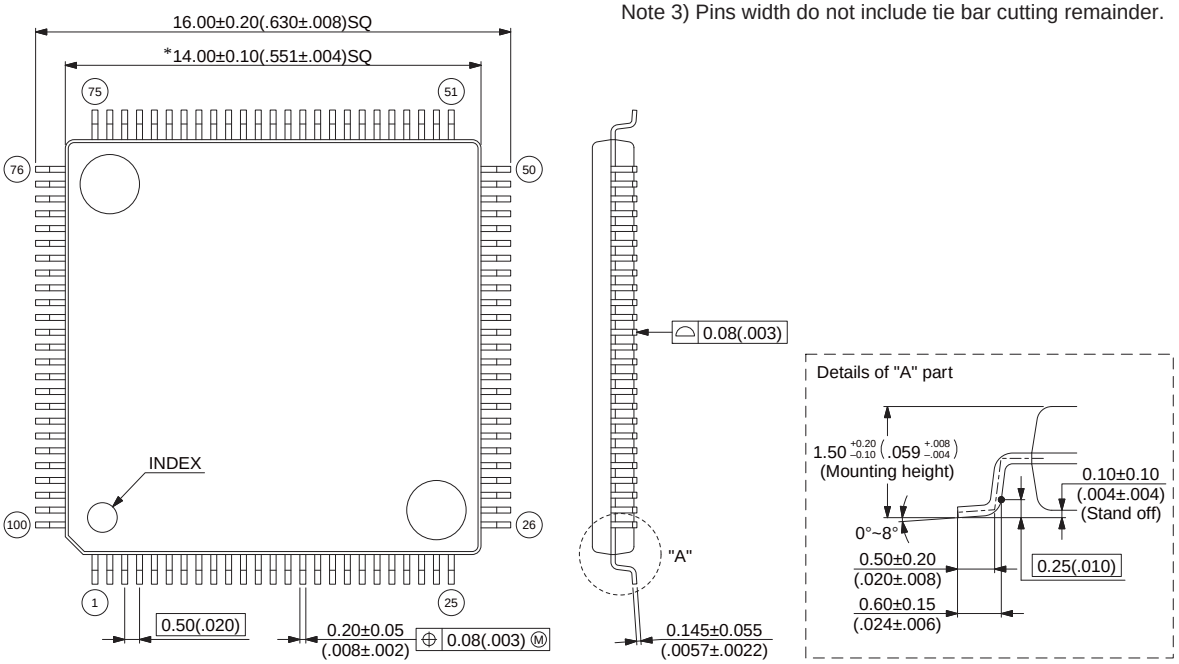
Dimensions in mm (inches).
Note: The values in parentheses are reference values.

(Continued)

(Continued)

100-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	14.0 × 14.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.65g
(FPT-100P-M05)	Code (Reference)	P-LFQFP100-14×14-0.50

100-pin plastic LQFP
(FPT-100P-M05)



Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.

Dimensions in mm (inches).
Note: The values in parentheses are reference values.

■ MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
—	—	Deleted the part number MB91F278(S).
4	■ FEATURES	Deleted “• Clock supervisor”.
26	■ HANDLING DEVICES	Added “• Serial Communication”.

The vertical lines marked in the left side of the page show the changes.

MEMO

MEMO

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