

# 32-bit Microcontroller

CMOS

## FR60 MB91319 Series

### MB91F318A/FV319A

#### ■ DESCRIPTION

The MB91319 series is the microcontrollers which use a high-performance 32-bit RISC-CPU and contains various types of I/O resources for the embedded control that requires high-performance and high-speed CPU processing.

It is suitable for the embedded control in TV or PDP, requiring high-performance CPU processing power.

This product is one of the FR60 family based on the FR30/40 family CPU with enhanced bus access. It is applicable to faster-speed application.

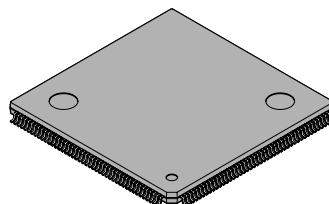
#### ■ FEATURE

- FR CPU
  - 32-bit RISC, load/store architecture with a five-stage pipeline
  - Operating frequency : 40 MHz (Use of PLL : Oscillation 10 MHz)
  - 16-bit fixed length instructions (basic instructions) , 1 instruction per cycle
  - Memory-to-memory transfer, bit manipulation, instruction for barrel shift etc. : Instruction set optimized for embedded applications
  - Function entry/exit instructions, multiple-register load/store instructions : Instructions adapted for high-level languages
  - Register interlock functions: Facilitating coding in assemblers

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#### ■ PACKAGE

176-pin plastic LQFP



(FPT-176P-M07)

# MB91319 Series

- Built-in multiplier with instruction-level support
  - 32-bit multiplication with sign : 5 cycles
  - 16-bit multiplication with sign : 3 cycles
- Interrupt (PC, PS save) : 6 cycles, 16 priority levels
- Harvard architecture allowing program access and data access to be executed simultaneously
- Instruction prefetch function implemented by a four-word queue in the CPU
- Instruction compatible with FR family

- Bus interface

This bus interface is used for internal macro IF (USB, OSDC)

- CS1, CS2, and CS3 areas are connected as following :  
CS1 area : Reserved, CS2 area : USB function, CS3 area : OSDC

- Internal memory

Memory	MB91FV319A	MB91F318A
RAM	64 KB	48 KB
FLASH (for program)	1 MB	1 MB
Memory for font	512 KB FLASH	384 KB MASK ROM

- DMAC (DMA Controller)

- 5 channels (ch0 and ch1 are connected to USB function. )
- Two forwarding factors (internal peripheral/software)
- Specifying of addressing mode 32-bit full address (increased/decreased/fixe)
- Transfer modes (demand transfer, burst transfer, step transfer, block transfer)
- Selectable transfer data size : 8, 16, or 32-bit

- Bit search module (for REALOS)

- Search for the position of the bit "1"/"0"-changed first in one word from the MSB

- Reload timer (including a channel for REALOS)

- 16-bit timer: 3 channels
- The internal clock is selectable from 2/8/32 divisions.

- UART

- Full duplex double buffer
- 5 channels
- Selectable parity ON/OFF
- Asynchronous (start-stop synchronized) or CLK-synchronous communications selectable
- Internal timer for dedicated baud rate
- External clock can be used as transfer clock.
- Assorted error detection functions (for parity, frame, and overrun errors)

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- I<sup>2</sup>C Interface \*
  - 4 channels (built-in bridge function)
  - Master/slave sending and receiving
  - Clock synchronization function
  - Detecting transmitting direction function
  - Bus error detection function
  - Standard mode (Max 100 Kbps) /High speed mode (Max 400 Kbps) supported
  - Built-in FIFO function with 16-byte data each for transmit/receive
  - Arbitration function
  - Slave address and general call address detection function
  - Start condition repeated generation and detection
  - 10-bit/7-bit slave address
  
- Interrupt controller
  - Total of external interrupt is 5. (one non-maskable interrupt pin ( $\overline{\text{NMI}}$ ) and four normal interrupt pins (INT3 to INT0) )
  - Interrupt from internal peripheral
  - Programmable priorities (16 levels) for all interrupts except the non-maskable interrupt
  - At the STOP, available use for Wake Up
  
- A/D converter
  - 10-bit resolution, 10 channels
  - Serial compared conversion type : Conversion time : approx. 10  $\mu\text{s}$
  - Conversion mode (single conversion mode, scan conversion mode)
  - Start-up factor (Software/external trigger)
  
- PPG
  - 4 channels are incorporated.
  - 16-bit down counter, 16-bit data register with buffer for setting cycles
  - The internal clock is selectable from 1/4/16/64 divisions.
  
- PWC
  - 1 channel (1 input) is incorporated.
  - 16-bit up counter
  - Easy digital low pass filter
  
- Multi function timer
  - 4 channels are incorporated.
  - Low pass filter eliminating noise below the clock setting
  - Capable of pulse width measurement according to fine settings using seven types of clock signals
  - Event count function from pin input
  - Interval timer function using seven kinds of clock and external input clock
  
- USB function
  - Full speed • double buffer of USB2.0 version
  - CONTROL IN/OUT, BULK IN/OUT, INTERRUPT IN

(Continued)

# MB91319 Series

(Continued)

- OSDC function
  - RGB: each 3 bits (16 colors available among 512 colors)
  - Analog RGB output: Max 50 MHz
  - Digital RGB output: Max 90 MHz
  - A font in 24 × 32 dots can be displayed up to 80 × 32.
  - Two-layered display of MAIN/CC (Font in CC layer is fixed at 18 dots in horizontal axis)
  - 4096 characters at the maximum (including 16 characters for font RAM)
- Closed caption decoder function
  - 2 channels are incorporated.
  - CC decode function
  - ID-1 (480i/480p) decode function
- PLL for video clock
  - 3 PLLs generating dot clock and VBI clock
- Other interval timer
  - 16-bit timer : 3 channels
  - Watchdog timer
- I/O port
  - Max 88 ports
- Other features
  - Built-in oscillation circuit as clock source
  - $\overline{\text{INIT}}$  is prepared as a reset pin.
  - Watchdog timer reset and software reset are also available.
  - Stop mode and sleep mode are supported as low-power consumption mode.
  - Gear function
  - Built-in timebase timer
  - Package : LQFP-176, 0.5mm pitch, 24 mm × 24 mm
  - CMOS technology : 0.25  $\mu\text{m}$  (EVA, FLASH)
  - Power supply voltage : 3.3 V  $\pm$  0.3 V, 2.5 V  $\pm$  0.2 V 2-power supply
- \* : "Purchase of Fujitsu I<sup>2</sup>C components conveys a license under the Philips I<sup>2</sup>C Patent Rights to use these components in an I<sup>2</sup>C system provided that the system conforms to the I<sup>2</sup>C Standard Specification as defined by Philips."



# MB91319 Series

## ■ PIN DESCRIPTION

Pin No.	Pin Name	Circuit type	Function
1	HSYNC1	G	Vertical synchronous input 1
2	HSYNC2	G	Vertical synchronous input 2
3	HSYNC3	G	Vertical synchronous input 3
4	VDDE	—	I/O power supply
5	VSS	—	Ground
6	VGS1/VCI1	—	Guard band ground
7	CPO1	K	Charge pump output
8	VSSP1	—	Dot clock PLL ground
9	VDDP1	—	Dot clock PLL power supply
10	VGS2/VCI2	—	Guard band ground
11	CPO2	K	Charge pump output
12	VSSP2	—	Dot clock PLL ground
13	VDDP2	—	Dot clock PLL power supply
14	VGS3/VCI3	—	Guard band ground
15	CPO3	K	Charge pump output
16	VSSP3	—	Dot clock PLL ground
17	VDDP3	—	Dot clock PLL power supply
18	VDDR	—	D/A power supply for R
19	VRef (1.1 V)	K	Power supply reference input
20	VR0 (2.7 k $\Omega$ )	K	Resistor connection pin
21	ROUT	K	R output (analog)
22	VSSR	—	D/A ground for R
23	VDDG	—	D/A power supply for G
24	GOUT	K	G output (analog)
25	VSSG	—	D/A ground for G
26	Vddb	—	D/A power supply for B
27	BOUT	K	B output (analog)
28	VSSB	—	D/A ground for B
29	VIN0	K	Data slicer input 0
30	VIN1	K	Data slicer input 1
31	VDDIS	—	Data slicer power supply
32	VSSS	—	Data slicer ground
33	VDDI	—	Internal logic power supply
34	AVCC	—	A/D power supply
35	AVRH	—	A/D reference power supply

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# MB91319 Series

Pin No.	Pin Name	Circuit type	Function
36	AVSS/AVRL	—	A/D ground
37	PC0	E	General-purpose port
	AN0		Analog input
38	PC1	E	General-purpose port
	AN1		Analog input
40	PC3	E	General-purpose port
	AN3		Analog input
41	PC4	E	General-purpose port
	AN4		Analog input
42	PC5	E	General-purpose port
	AN5		Analog input
43	PC6	E	General-purpose port
	AN6		Analog input
44	PC7	E	General-purpose port
	AN7		Analog input
45	P20	E	General-purpose port
	AN8		Analog input
46	P21	E	General-purpose port
	AN9		Analog input
47	P22	C	General-purpose port
48	P23	C	General-purpose port
49	P24	C	General-purpose port
50	P25	C	General-purpose port
51	P26	C	General-purpose port
52	P27	C	General-purpose port
53	P30	C	General-purpose port
54	P31	C	General-purpose port
55	P32	C	General-purpose port
56	VDDE	—	3.3 V power supply
57	X0	A	10 MHz oscillation pin
58	VSS	—	Ground
59	X1	A	10 MHz oscillation pin
60	VDDI	—	Internal logic power supply
61	$\overline{\text{TRST}}$	B	DSU tool reset (In MB91F318A, this pin is the open pin so do not connect with other pins.)

(Continued)

# MB91319 Series

Pin No.	Pin Name	Circuit type	Function
62	ICLK	M	DSU clock (In MB91F318A, this pin is the open pin so do not connect with other pins.)
63	IBREAK	L	DSU break (In MB91F318A, this pin is the open pin so do not connect with other pins.)
64	ICS0	O	DSU status (In MB91F318A, this pin is the open pin so do not connect with other pins.)
65	ICS1	O	DSU status (In MB91F318A, this pin is the open pin so do not connect with other pins.)
66	ICS2	O	DSU status (In MB91F318A, this pin is the open pin so do not connect with other pins.)
67	ICD0	P	DSU data (In MB91F318A, this pin is the open pin so do not connect with other pins.)
68	ICD1	P	DSU data (In MB91F318A, this pin is the open pin so do not connect with other pins.)
69	ICD2	P	DSU data (In MB91F318A, this pin is the open pin so do not connect with other pins.)
70	ICD3	P	DSU data (In MB91F318A, this pin is the open pin so do not connect with other pins.)
71	MD0	F	Mode pin
72	MD1	F	Mode pin
73	MD2	F	Mode pin
74	MD3	L	Mode pin
75	INIT	B	Initial (reset) pin
76	P80	J	General-purpose port
	SCL0		I <sup>2</sup> C clock pin
77	P81	J	General-purpose port
	SDA0		I <sup>2</sup> C data pin
78	P82	J	General-purpose port
	SCL1		I <sup>2</sup> C clock pin
79	P83	J	General-purpose port
	SDA1		I <sup>2</sup> C data pin
80	P84	C	General-purpose port
	SI0		UART0 serial input
81	P85	C	General-purpose port
	SO0		UART0 serial output
82	P86	C	General-purpose port
	SCK0		UART0 clock input/output

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# MB91319 Series

Pin No.	Pin Name	Circuit type	Function
83	P87	C	General-purpose port
	SI1		UART1 serial input
84	P90	C	General-purpose port
	SO1		UART1 serial output
85	P91	C	General-purpose port
	SCK1		UART1 clock input/output
86	P92	C	General-purpose port
	RIN		PWC input
87	P93	C	General-purpose port
	TMI0		Multi-functional timer 0 input
88	P94	C	General-purpose port
	TMI1		Multi-functional timer 1 input
89	P95	C	General-purpose port
	TMI2		Multi-functional timer 2 input
90	P96	C	General-purpose port
	TMI3		Multi-functional timer 3 input
91	P97	O	General-purpose port
	INT0		External interrupt input 0
92	VDDE	—	3.3 V power supply
93	X0A	A	32 kHz oscillation pin
94	VSS	—	Ground
95	X1A	A	32 kHz oscillation pin
96	VDDI	—	Internal logic power supply
97	PA0	O	General-purpose port
	INT1		External interrupt input 1
98	PA1	O	General-purpose port
	INT2		External interrupt input 2
99	PA2	O	General-purpose port
	INT3		External interrupt input 3
100	$\overline{\text{NMI}}$	B	$\overline{\text{NMI}}$ input
101	P33	C	General-purpose port
	TRG0		PPG0 trigger input
102	P34	C	General-purpose port
	TRG1		PPG1 trigger input

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# MB91319 Series

Pin No.	Pin Name	Circuit type	Function
103	P35	C	General-purpose port
	TRG2		PPG2 trigger input
104	P36	C	General-purpose port
	TRG3		PPG3 trigger input
105	P37	N	General-purpose port
	SCL2		I <sup>2</sup> C clock pin
106	P40	N	General-purpose port
	SDA2		I <sup>2</sup> C data pin
107	P41	N	General-purpose port
	SCL3		I <sup>2</sup> C clock pin
108	P42	N	General-purpose port
	SCL4		I <sup>2</sup> C clock pin
109	P43	N	General-purpose port
	SDA3		I <sup>2</sup> C data pin
110	P44	N	General-purpose port
	SDA4		I <sup>2</sup> C data pin
111	P45	C	General-purpose port
	SI2		UART2 serial input
112	P46	C	General-purpose port
	SO2		UART2 serial output
113	P47	C	General-purpose port
	SCK2		UART2 clock output
114	P50	C	General-purpose port
	SI3		UART3 serial input
115	P51	C	General-purpose port
	SO3		UART3 serial output
116	P52	C	General-purpose port
	SCK3		UART3 clock output
117	P53	C	General-purpose port
118	P54	C	General-purpose port
119	P55	C	General-purpose port
120	P56	C	General-purpose port
121	P57	C	General-purpose port
122	VDDI	—	Internal logic power supply
123	VSS	—	Ground

(Continued)

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Pin No.	Pin Name	Circuit type	Function
124	VDDE	—	3.3 V power supply
125	P70	C	General-purpose port
126	P71	C	General-purpose port
127	P72	C	General-purpose port
128	P73	C	General-purpose port
129	P74	C	General-purpose port
130	P00	C	General-purpose port
	SI4		UART4 serial input
	TIN0		Reload timer 0 trigger input
131	P01	C	General-purpose port
	SO4		UART4 serial output
	TIN1		Reload timer 1 trigger input
132	P02	C	General-purpose port
	SCK4		UART4 clock input
	TIN2		Reload timer 2 trigger input
133	P03	C	General-purpose port
	TO0		Reload timer 0 output
134	P04	C	General-purpose port
	TO1		Reload timer 1 output
135	P05	C	General-purpose port
	TO2		Reload timer 2 output
136	P06	C	General-purpose port
	TMO0		Multi-functional timer 0 output
137	P07	C	General-purpose port
	TMO1		Multi-functional timer 1 output
138	P10	C	General-purpose port
	TMO2		Multi-functional timer 2 output
139	P11	C	General-purpose port
	TMO3		Multi-functional timer 3 output
140	P12	C	General-purpose port
	PPG0		PPG0 output
141	P13	C	General-purpose port
	PPG1		PPG1 output
142	P14	C	General-purpose port
	PPG2		PPG2 output

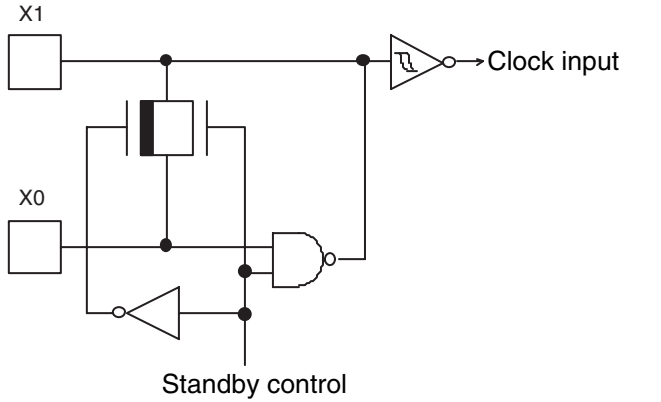
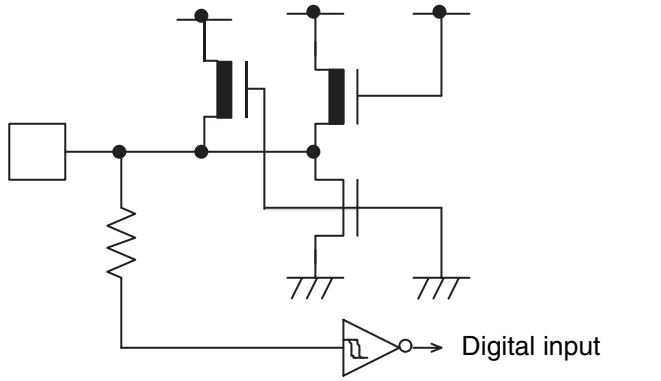
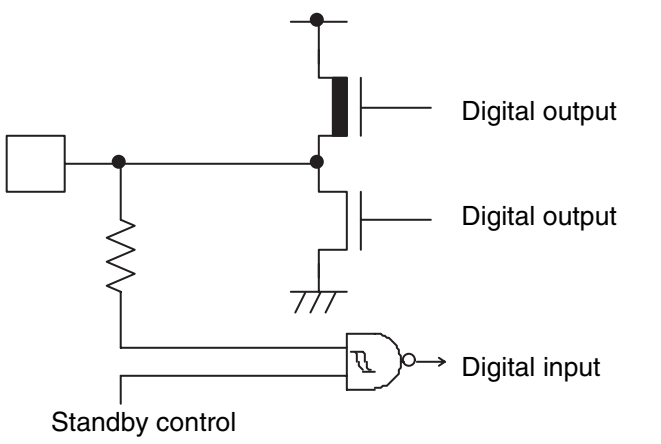
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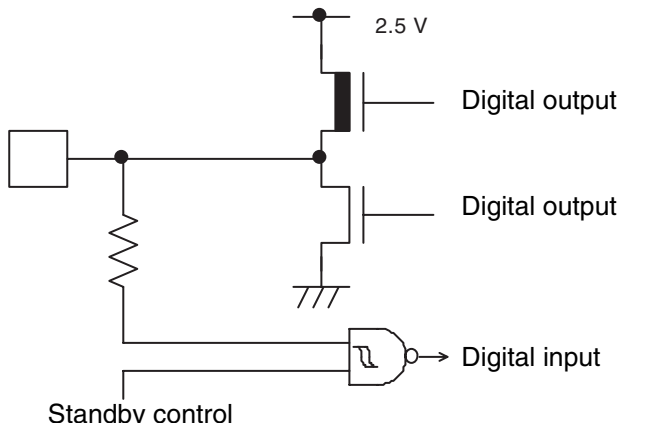
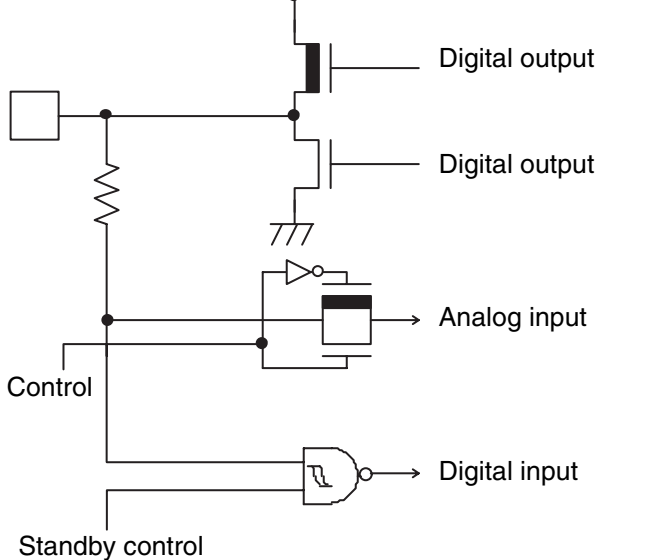
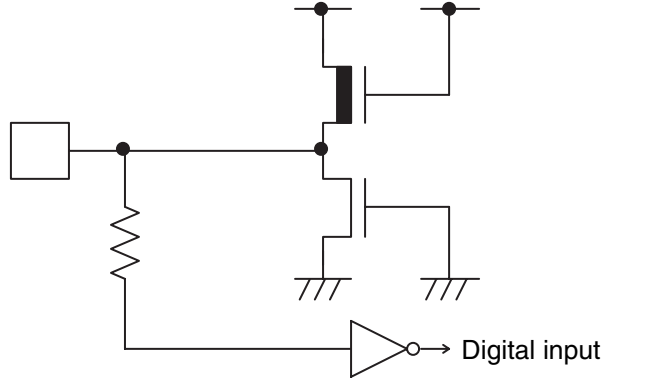
Pin No.	Pin Name	Circuit type	Function
143	P15	C	General-purpose port
	PPG3		PPG3 output
144	P16	C	General-purpose port
	ATRG		A/D conversion trigger input
145	P17	C	General-purpose port
146	PB0	C	General-purpose port
147	PB1	C	General-purpose port
148	PB2	I	General-purpose port
149	PB3	C	General-purpose port
150	PB4	C	General-purpose port
151	PB5	C	General-purpose port
152	PB6	H	General-purpose port
153	PB7	C	General-purpose port
154	VDDI	—	Internal power supply
155	X1B	A	48 MHz oscillation pin
156	VSS	—	Ground
157	X0B	A	48 MHz oscillation pin
158	VDDE	—	3.3 V power supply
159	UDM	USB	USB function
160	UDP		USB function
161	B0	D	RGB digital output
162	B1	D	RGB digital output
163	B2	D	RGB digital output
164	G0	D	RGB digital output
165	G1	D	RGB digital output
166	G2	D	RGB digital output
167	R0	D	RGB digital output
168	R1	D	RGB digital output
169	R2	D	RGB digital output
170	VDDI	—	Internal logic power supply
171	VOB2	D	Translucent color period output
172	VOB1	D	OSD display period output
173	FH	D	Horizontal synchronous output
174	DCKO	D	Dot clock output
175	DCKI	G	Dot clock input
176	VSYN	G	Vertical synchronous output

## ■ I/O CIRCUIT TYPE

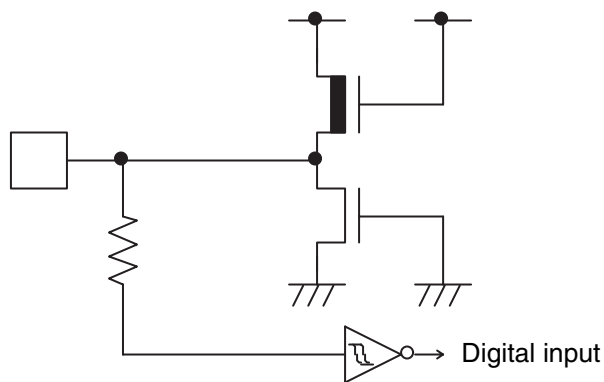
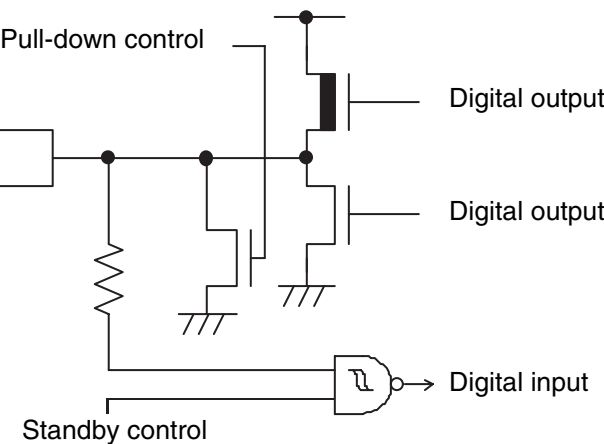
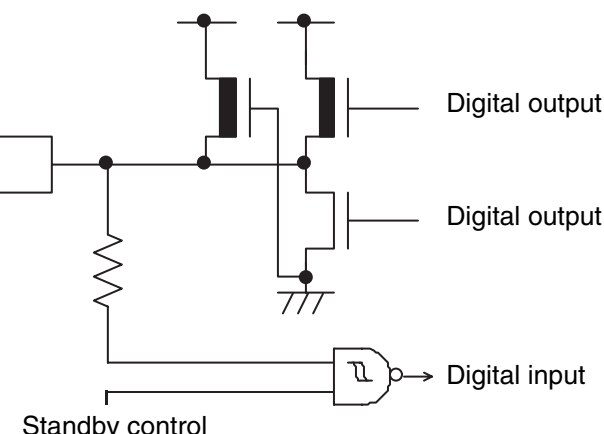
Type	Circuit type	Remarks
A		Oscillation circuit
B		<ul style="list-style-type: none"> <li>• CMOS level hysteresis input</li> <li>• With pull-up resistor</li> </ul>
C		<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• With standby control</li> </ul>

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# MB91319 Series

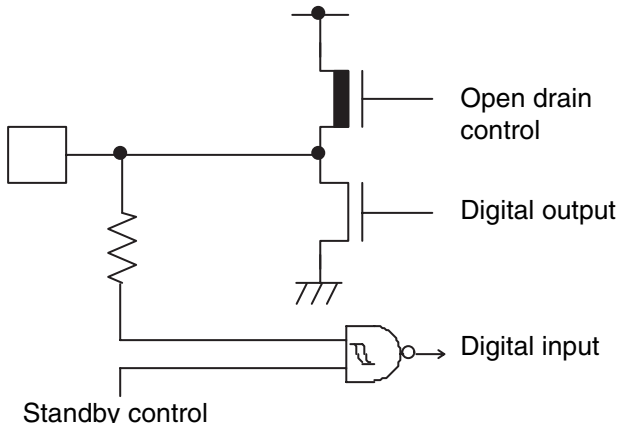
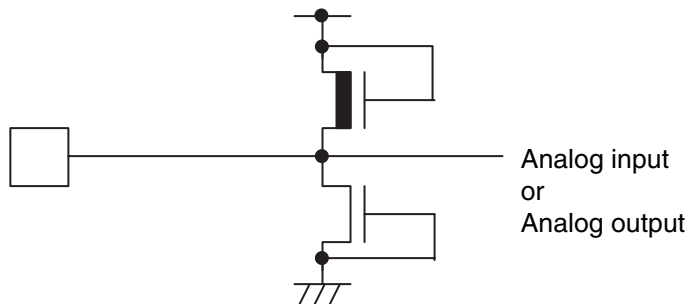
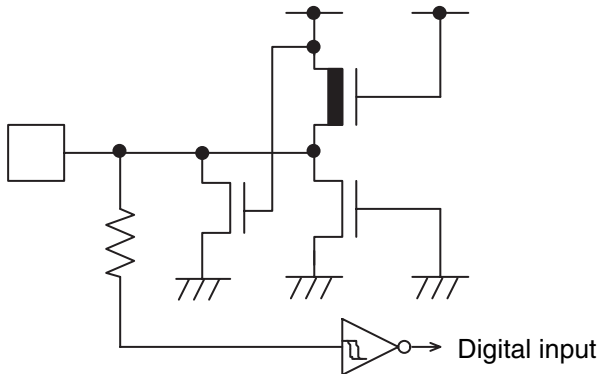
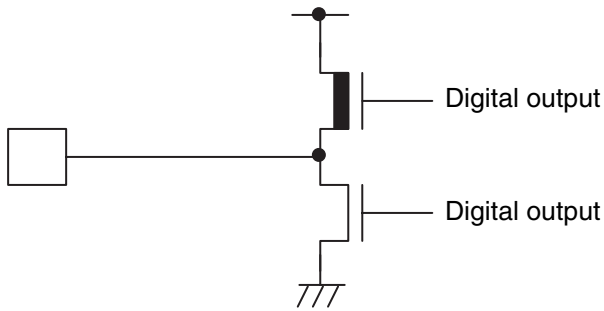
Type	Circuit type	Remarks
D		<ul style="list-style-type: none"> <li>• 2.5 V CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• With standby control</li> </ul>
E		<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• With standby control</li> <li>• With analog input switch</li> </ul>
F		<ul style="list-style-type: none"> <li>• CMOS level input</li> <li>• Without standby control</li> </ul>

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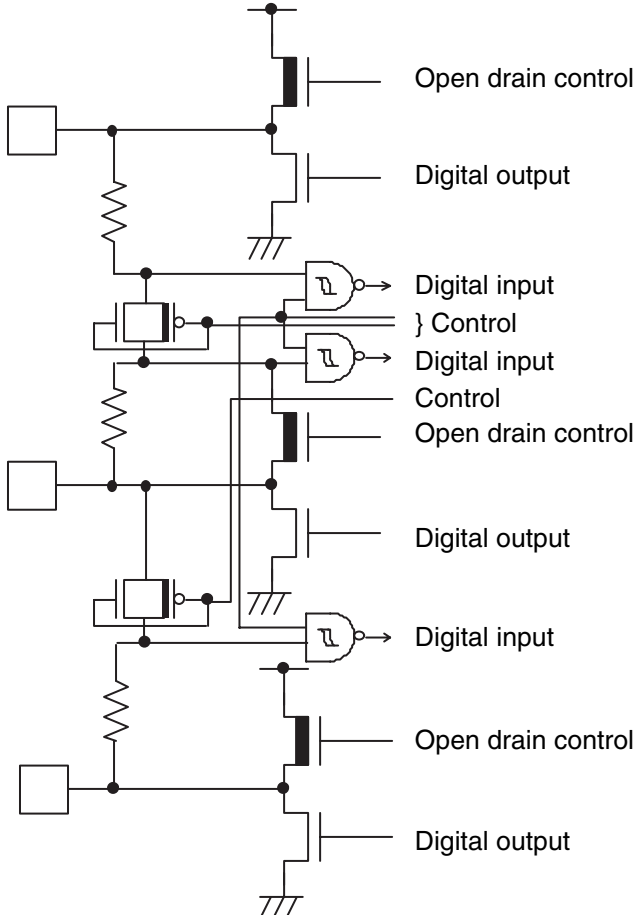
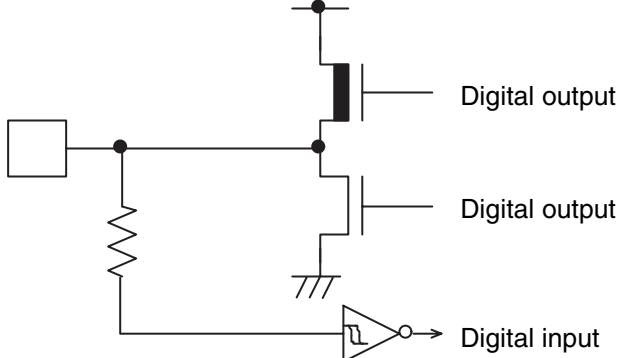
Type	Circuit type	Remarks
G		<ul style="list-style-type: none"> <li>• CMOS level hysteresis input</li> <li>• Without standby control</li> </ul>
H		<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• With standby control</li> <li>• With pull-down resistor</li> </ul>
I		<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• With standby control</li> <li>• With pull-up resistor</li> </ul>

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# MB91319 Series

Type	Circuit type	Remarks
J		<ul style="list-style-type: none"> <li>• Open drain output</li> <li>• CMOS level hysteresis input</li> <li>• With standby control</li> </ul>
K		Analog pin
L		<ul style="list-style-type: none"> <li>• CMOS level hysteresis input</li> <li>• With pull-down resistor</li> </ul>
M		CMOS level output

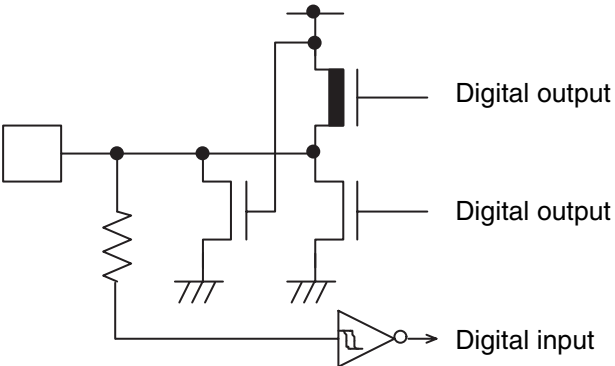
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Type	Circuit type	Remarks
N	 <p>The diagram for Type N shows two identical channels. Each channel consists of an open-drain control input (top), a digital output (middle), a digital input (bottom), and a control input (right). The control inputs are connected to AND gates. Pull-up resistors are connected to the digital outputs and digital inputs. The digital outputs are connected to the open-drain control inputs of the other channel.</p>	<ul style="list-style-type: none"> <li>• 3 ports for I<sup>2</sup>C</li> <li>• CMOS level hysteresis input</li> <li>• CMOS level output</li> <li>• With stop control</li> </ul>
O	 <p>The diagram for Type O shows a single channel with a digital output (top), a digital output (middle), and a digital input (bottom). The digital input is connected to an AND gate. A pull-up resistor is connected to the digital output.</p>	<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• Without standby control</li> </ul>

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# MB91319 Series

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Type	Circuit type	Remarks
P	 <p>The diagram shows a digital input connected to a pull-down resistor. The input signal is applied to the gates of two CMOS transistors. The output of the upper transistor is labeled 'Digital output'. The circuit is designed for CMOS level output with hysteresis input, without standby control, and with a pull-down resistor.</p>	<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• Without standby control</li> <li>• With pull-down resistor</li> </ul>

## ■ HANDLING DEVICES

- Preventing Latchup

Latch-up may occur in a CMOS IC if a voltage greater than  $V_{CC}$  or less than  $V_{SS}$  is applied to an input or output pin or if an above-rating voltage is applied between  $V_{CC}$  and  $V_{SS}$  pins. A latchup, if it occurs, significantly increases the power supply current and may cause thermal destruction of an element. When you use a CMOS IC, be very careful not to exceed the maximum rating.

- Treatment of Unused Input Pins

Do not leave an unused input pin open, since it may cause a malfunction. Handle by, for example, using a pull-up or pull-down resistor.

- Power Supply Pins

In products with multiple  $V_{CC}$  or  $V_{SS}$  pins, the pins of the same potential are internally connected in the device to avoid abnormal operations including latch-up. However, you must connect the pins to external power supply and a ground line to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with the  $V_{CC}$  and  $V_{SS}$  pins of this device at the low impedance.

It is also advisable to connect a ceramic capacitor of approximately 0.1  $\mu\text{F}$  as a bypass capacitor between  $V_{CC}$  and  $V_{SS}$  pins near this device.

- Crystal Oscillator Circuit

Noise near the X0 and X1 pins may cause the device to malfunction. Design the printed circuit board so that X0, X1, the crystal oscillator (or ceramic oscillator), and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended to design the PC board artwork with the X0 and X1 pins surrounded by ground plane because stable operation can be expected with such a layout.

- Mode Pins (MD0 to MD3)

These pins should be connected directly to  $V_{CC}$  or  $V_{SS}$ . To prevent the device erroneously switching to test mode due to noise, design the printed circuit board such that the distance between the mode pins and  $V_{CC}$  or  $V_{SS}$  is as short as possible and the connection impedance is low.

- Tool Reset Pins ( $\overline{\text{TRST}}$ )

When not using the tool, be sure to input the same signal as  $\overline{\text{INIT}}$  to these pins. Apply the same treatment to mass-produced products as well.

- Operation at Power-on

Be sure to execute setting initialized reset (INIT) with  $\overline{\text{INIT}}$  pin immediately after start-up.

Immediately after the power supply is turned on, hold the Low level input to the  $\overline{\text{INIT}}$  pin for the settling time required for the oscillator circuit to take the oscillation stabilization wait time for the oscillator circuit. (For INIT via the  $\overline{\text{INIT}}$  pin, the oscillation stabilization wait time setting is initialized to the minimum value.)

- Oscillation Input at Power On

When turning the power on, maintain clock input until the device is released from the oscillation stabilization wait state.

# MB91319 Series

- Notes on Power-ON/Shut-down

Do not apply  $V_{DDE}$  (external) alone continuously (for over an indication of one minute) with  $V_{DDI}$  (internal) disconnected not to cause a reliability problem with LSI.

When  $V_{DDE}$  (external) returns from the OFF state to the ON state, the circuit may fail to hold its internal state, for example, due to power supply noise.

Turn ON/OFF the power supply in the following order:

- At power-on  $V_{DDI}$  (internal)  $\rightarrow$  Analog  $\rightarrow V_{DDE}$  (external)  $\rightarrow$  Signal
- Turn off Signal  $\rightarrow V_{DDE}$  (external)  $\rightarrow$  Analog  $\rightarrow V_{DDI}$  (internal)

- Undefined Output on Power-ON

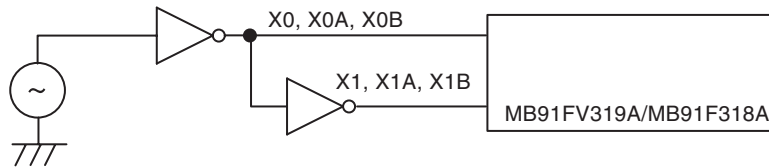
When the power is turned on, the output pin may remain unstable until the internal power supply becomes stable.

- Clock

About the attention when the external clock is used

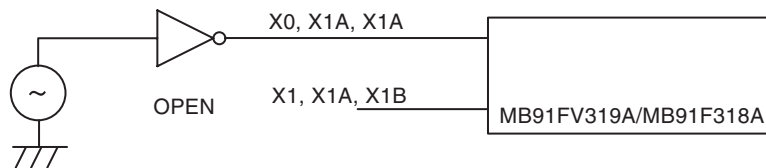
When the external clock is used, in principle, supply a clock signal to the X0 (X0A, X0B) pin and an opposite-phase clock signal to the X1 (X1A, X1B) pin at the same time. However, in this case the stop mode (oscillator stop mode) must not be used (This is because, in STOP mode, the X1 (X1A, X1B) pin stops at "H" output) . At 12.5 MHz or less, the device can be used with the clock signal supplied only to the X0 (X0A, X0B) pin.

- Using an External Clock (normal)



Note: The STOP mode (oscillation stop mode) cannot be used.

- Using an External Clock (available at 12.5 MHz or less)



Note : The X1 (X1A, X1B) pin must be designed to have a delay within 15 ns, at 10 MHz, from the signal to the X0 (X0A, X0B) pin.

- Restrictions

Common in MB91319 series

(1) Clock control block

Take the oscillation stabilization wait time during Low level input to the  $\overline{\text{INIT}}$  pin.

(2) Bit Search Module

The 0-detection data register (BSD0) , 1-detection data register (BSD1) , and transition-detection data register (BDSC) are only word-accessible.

(3) I/O port

Ports are accessed only in bytes.

(4) Low-power Consumption Mode

- To enter the standby mode, use the synchronous standby mode (set with the SYNC\_S bit as bit 8 in the TBCR : timebase counter control register) and be sure to use the following sequence:

(LD1 #value\_of\_standby, R0)

(LD1 #\_STCR, R12)

STB R0, @R12 ; Write to standby control register (STCR)

LDUB @R12, R0 ; STCR read for synchronous standby

LDUB @R12, R0 ; Dummy re-read of STCR

NOP ; NOP × 5 for adjusted timing

NOP

NOP

NOP

NOP

In addition, set the I-flag and the ILM and ICR registers to branch to an interrupt handler when the interrupt handler triggers the microcontroller to return from the standby mode.

(5) Notes on the PS register

As the PS register is processed by some instructions in advance, exception handling below may cause the interrupt handling routine to break when the debugger is used or the display contents of flags in the PS register to be updated.

As the microcontroller is designed to carry out reprocessing correctly upon returning from such an EIT event, it performs operations before and after the EIT as specified in either case.

- The following operations are performed when the instruction followed by a data event, when breaks when single-stepped, or when a DIVOU/DIVOS emulator menu instruction receives a user interrupt or NMI.

(1)The D0 and D1 flags are updated in advance.

(2)An EIT handling routine (user interrupt, NMI, or emulator) is executed.

(3)Upon returning from the EIT, the DIVOU/DIVOS instruction is executed and the D0 and D1 flags are updated to the same values as in (1) .

- The following operations are performed when the ORCCR, STILM, MOV Ri, and PS instructions are executed to allow the interrupt at the state which a user interrupt/NMI cause occurs.

(1)The PS register is updated in advance.

(2)An EIT handling routine (user interrupt and NMI) is executed.

(3)Upon returning from the EIT, the above instructions are executed and the PS register is updated to the same value as in (1) .

# MB91319 Series

## (6) Watchdog timer

The watchdog timer built in this model monitors a program that it defers a reset within a certain period of time. The watchdog timer resets the CPU if the program runs out of controls, preventing the reset defer function from being executed. Once the function of the watchdog timer is enabled, therefore, the watchdog timer keeps on operating programs until it resets the CPU.

As an exception, the watchdog timer defers a reset automatically under the condition in which the CPU stops program execution.

For those conditions to which this exception applies, see the function description of watchdog timer.

A watchdog reset may not be generated in the above situation caused by the system running out of control. In that case, please reset (INIT) by external INIT pin.

## (7) Notes on using A/D

The MB91319 series contains an A/D converter. Supply power to the AVCC at 3.3 V.

Evaluation chip MB91FV319A specific

## (8) Simultaneous generation of software break and user interrupt/NMI (only for MB91FV319A)

If a software break and a user interrupt/NMI occur simultaneously, the emulator debugger may cause the following symptoms.

- The debugger stops pointing to a location other than the programmed breakpoints.
- The halted program is not re-executed correctly.

If these phenomena occur, use a hardware break instead of the software break. If the monitor debugger has been used, avoid setting any break at the relevant location.

## (9) Step execution of RETI instruction

In an environment where interrupts frequently occur during single-step execution, only the relevant interrupt processing routines are executed repeatedly during single-step execution of the RETI instruction. This will prevent the main routine and low-interrupt-level programs from being executed. To avoid it, do not single-step RETI instructions.

When the relevant interrupt routine no longer requires being debugged, disable the relevant interrupt and perform debugging.

## (10) About an operand break

Do not apply a data event break to access to the area containing the address of a stack pointer.

## (11) Example of batch file for configuration

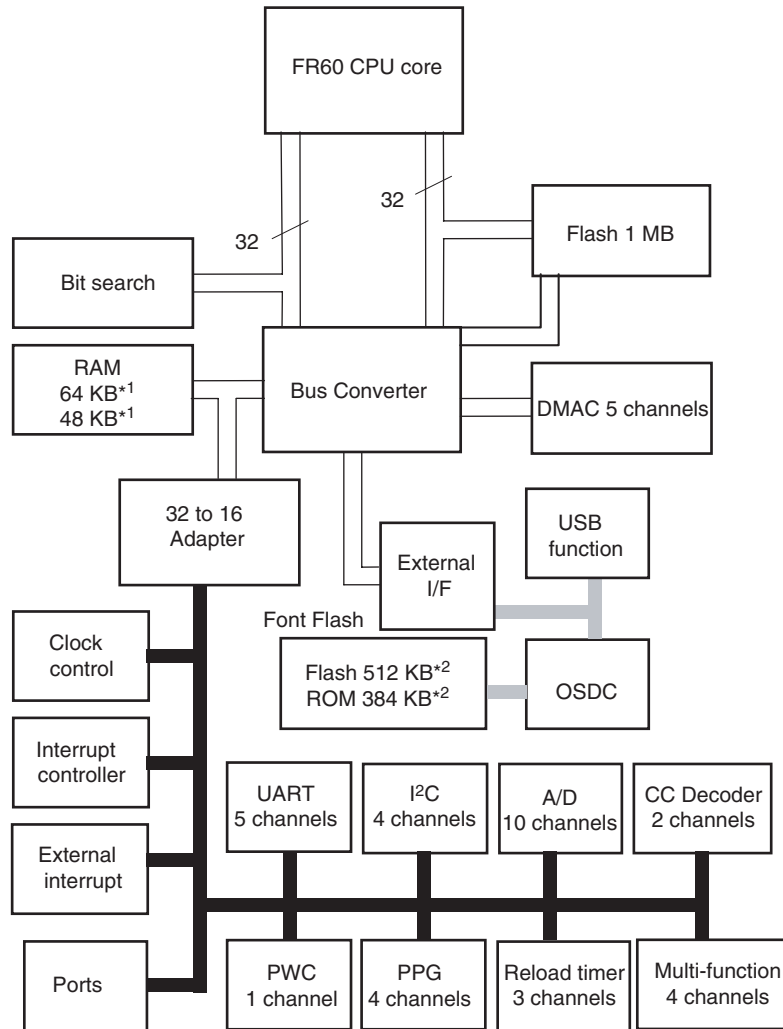
To debug a program downloaded to internal RAM, be sure to execute the following batch file after executing RESET.

```
#-----  
#Set MODR (0x7fd) = Enable In memory + 16-bit External Bus  
set mem/byte 0x7fd = 0x5  
#-----
```

## (12) Address in the built-in FLASH/ROM area (1 MB product)

The address 0X0017FFF8 in the built-in FLASH/ROM area has been reserved. You must configure the FE.

## ■ BLOCK DIAGRAM



\*1 : MB91FV319A contains the data RAM of 64KB, and MB91F318A contains that of 48KB.

\*2 : MB91FV319A contains the font ROM of 512KB flash memory, and MB91F318A contains that of 384KB mask ROM.

# MB91319 Series

## ■ MEMORY SPACE

The FR family has 4 GB of logical address space ( $2^{32}$  addresses) available to the CPU by linear access.

### • Direct Addressing Areas

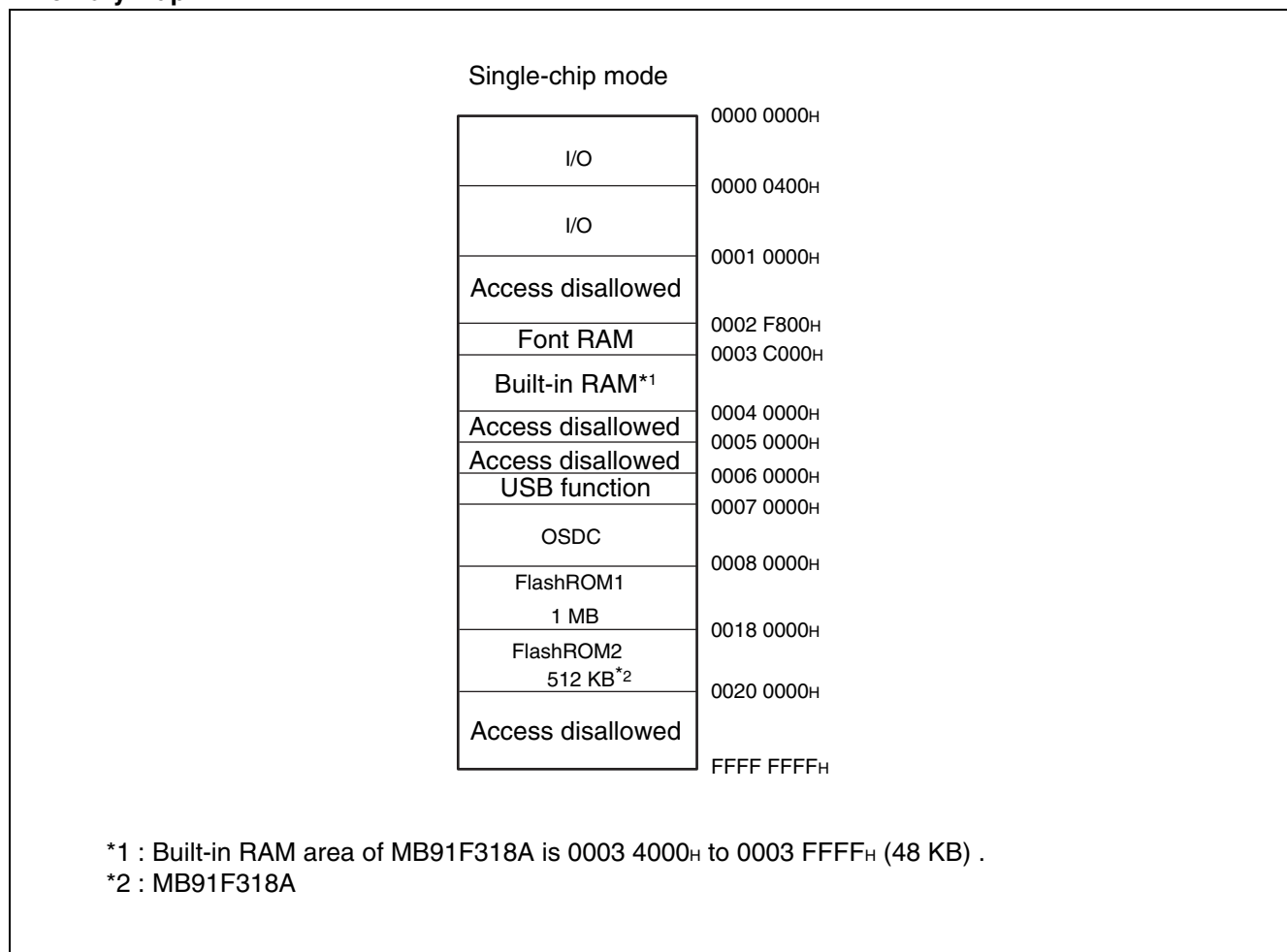
The following address space areas are used as I/O areas.

These areas are called direct addressing areas, in which the address of an operand can be specified directly during an instruction.

The size of directly addressable areas depends on the length of the data being accessed as shown below.

- Byte data access : 000<sub>H</sub> to 0FF<sub>H</sub>
- Half word data access : 000<sub>H</sub> to 1FF<sub>H</sub>
- Word data access : 000<sub>H</sub> to 3FF<sub>H</sub>

### • Memory Map



## ■ I/O MAP

This shows the correspondence between the memory space area and various peripheral resource registers.

[How to read the table]

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
00000000H	PDR0 [R/W] XXXXXXXX	PDR1 [R/W] XXXXXXXX	PDR2 [R/W] XXXXXXXX	PDR3 [R/W] XXXXXXXX	T-unit Port Data Register

Read/Write attribute

Initial value of register after a reset

Register name (First-column register at address 4n; second-column register at address 4n + 2)

Leftmost register address (For word-length access, column 1 of the register becomes the MSB of the data.)

Note : Initial values of register bits are represented as follows :

“1” : Initial Value “1”

“0” : Initial Value “0”

“X” : Initial Value “X”

“ - ” : No physical register at this location

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000000H to 00000FH	—	—	—	—	Reserved
000010H	PDR0[R/W] XXXXXXXX	PDR1[R/W] XXXXXXXX	PDR2[R/W] XXXXXXXX	PDR3[R/W] XXXXXXXX	R-bus Port Data Register
000014H	PDR4[R/W] XXXXXXXX	PDR5[R/W] XXXXXXXX	—	PDR7[R/W] --XXXXXX	
000018H	PDR8[R/W] XXXXXXXX	PDR9[R/W] XXXXXXXX	PDRA[R/W] -----XXX	PDRB[R/W] XXXXXXXX	
00001CH	PDRC[R/W] XXXXXXXX	—	—	—	
000020H	ADCTH[R/W] XXXXXX00	ADCTL[R/W] 0000X00	ADCH[R/W] 00000000 00000000		10-bit A/D Converter
000024H	ADAT0[R] XXXXXX00 00000000		ADAT1[R] XXXXXX00 00000000		
000028H	ADAT2[R] XXXXXX00 00000000		ADAT3[R] XXXXXX00 00000000		
00002CH	ADAT4[R] XXXXXX00 00000000		ADAT5[R] XXXXXX00 00000000		
000030H	ADAT6[R] XXXXXX00 00000000		ADAT7[R] XXXXXX00 00000000		

(Continued)

# MB91319 Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000034 <sub>H</sub>	—	—	—	—	Reserved
000038 <sub>H</sub>	—	—	—	—	
00003C <sub>H</sub>	—	—	—	—	
000040 <sub>H</sub>	EIRR [R/W] 00000000	ENIR [R/W] 00000000	ELVR [R/W] 00000000		Ext int
000044 <sub>H</sub>	DICR [R/W] -----0	HRCL [R/W] 0--11111	—		DLYI/I-unit
000048 <sub>H</sub>	TMRLR0 [W] XXXXXXXX XXXXXXXX		TMR0 [R] XXXXXXXX XXXXXXXX		Reload Timer 0
00004C <sub>H</sub>	—		TMCSR0 [R/W] ---0000 00000000		
000050 <sub>H</sub>	TMRLR1 [W] XXXXXXXX XXXXXXXX		TMR1 [R] XXXXXXXX XXXXXXXX		Reload Timer 1
000054 <sub>H</sub>	—		TMCSR1 [R/W] ---0000 00000000		
000058 <sub>H</sub>	TMRLR2 [W] XXXXXXXX XXXXXXXX		TMR2 [R] XXXXXXXX XXXXXXXX		Reload Timer 2
00005C <sub>H</sub>	—		TMCSR2 [R/W] ---0000 00000000		
000060 <sub>H</sub>	SSR0 [R/W] 00001-00	SIDR0 [R/W] XXXXXXXX	SCR0 [R/W] 00000100	SMR0 [R/W] 00--0-0-	UART0
000064 <sub>H</sub>	UTIM0 [R] (UTIMR [W]) 00000000 00000000		DRCL0 [W] -----	UTIMC0 [R/W] 0--00001	U-TIMER 0
000068 <sub>H</sub>	SSR1 [R/W] 00001-00	SIDR1 [R/W] XXXXXXXX	SCR1 [R/W] 00000100	SMR1 [R/W] 00--0-0-	UART1
00006C <sub>H</sub>	UTIM1 [R] (UTIMR [W]) 00000000 00000000		DRCL1 [W] -----	UTIMC1 [R/W] 0--00001	U-TIMER 1
000070 <sub>H</sub>	SSR2 [R/W] 00001-00	SIDR2 [R/W] XXXXXXXX	SCR2 [R/W] 00000100	SMR2 [R/W] 00--0-0-	UART2
000074 <sub>H</sub>	UTIM2 [R] (UTIMR [W]) 00000000 00000000		DRCL2 [W] -----	UTIMC2 [R/W] 0--00001	U-TIMER 2
000078 <sub>H</sub>	SSR3 [R/W] 00001-00	SIDR3 [R/W] XXXXXXXX	SCR3 [R/W] 00000100	SMR3 [R/W] 00--0-0-	UART3
00007C <sub>H</sub>	UTIM3 [R] (UTIMR [W]) 00000000 00000000		DRCL3 [W] -----	UTIMC3 [R/W] 0--00001	U-TIMER 3
000080 <sub>H</sub>	SSR4 [R/W] 00001-00	SIDR4 [R/W] XXXXXXXX	SCR4 [R/W] 00000100	SMR4 [R/W] 00--0-0-	UART4
000084 <sub>H</sub>	UTIM4 [R] (UTIMR [W]) 00000000 00000000		DRCL4 [W] -----	UTIMC4 [R/W] 0--00001	U-TIMER 4

(Continued)

# MB91319 Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000088 <sub>H</sub>	—		—		Reserved
00008C <sub>H</sub>	—		—		
000090 <sub>H</sub>	PWCCL[R/W] 0000--00	PWCCH[R/W] 00-00000	—		PWC
000094 <sub>H</sub>	PWCD[R] XXXXXXXX XXXXXXXX		—		
000098 <sub>H</sub>	PWCC2[R/W] 000-----	Reserved	—		PWC
00009C <sub>H</sub>	PWCUD[R] XXXXXXXX XXXXXXXX		—		
0000A0 <sub>H</sub>	—		—		Reserved
0000A4 <sub>H</sub>	—		—		
0000A8 <sub>H</sub>	—		—		
0000AC <sub>H</sub>	—		—		
0000B0 <sub>H</sub>	IFN0 [R] 00000000	IFRN0 [R/W] 00000000	IFCR0 [R/W] 00-00000	IFDR0 [R/W] 00000000	I <sup>2</sup> C Interface 0
0000B4 <sub>H</sub>	IBCR0 [R/W] 00000000	IBSR0 [R/W] 00000000	ITBA0 [R/W] -----00 00000000		
0000B8 <sub>H</sub>	ITMK0 [R/W] 00----11 11111111		ISMK0 [R/W] 01111111	ISBA0 [R/W] 00000000	
0000BC <sub>H</sub>	—	IDAR0 [R/W] 00000000	ICCR0 [R/W] 0-011111	IDBL0 [R/W] -----0	
0000C0 <sub>H</sub>	IFN1 [R] 00000000	IFRN1 [R/W] 00000000	IFCR1 [R/W] 00-00000	IFDR1 [R/W] 00000000	I <sup>2</sup> C Interface 1
0000C4 <sub>H</sub>	IBCR1 [R/W] 00000000	IBSR1 [R/W] 00000000	ITBA1 [R/W] -----00 00000000		
0000C8 <sub>H</sub>	ITMK1 [R/W] 00----11 11111111		ISMK1 [R/W] 01111111	ISBA1 [R/W] 00000000	
0000CC <sub>H</sub>	—	IDAR1 [R/W] 00000000	ICCR1 [R/W] 0-011111	IDBL1 [R/W] -----0	
0000D0 <sub>H</sub>	IFN2 [R] 00000000	IFRN2 [R/W] 00000000	IFCR2 [R/W] 00-00000	IFDR2 [R/W] 00000000	I <sup>2</sup> C Interface 2
0000D4 <sub>H</sub>	IBCR2 [R/W] 00000000	IBSR2 [R/W] 00000000	ITBA2 [R/W] -----00 00000000		
0000D8 <sub>H</sub>	ITMK2 [R/W] 00----11 11111111		ISMK2 [R/W] 01111111	ISBA2 [R/W] 00000000	
0000DC <sub>H</sub>	—	IDAR2 [R/W] 00000000	ICCR2 [R/W] 0-011111	IDBL2 [R/W] -----0	

(Continued)

# MB91319 Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000E0 <sub>H</sub>	IFN3 [R] 00000000	IFRN3 [R/W] 00000000	IFCR3 [R/W] 00-00000	IFDR3 [R/W] 00000000	I <sup>2</sup> C Interface 3
0000E4 <sub>H</sub>	IBCR3 [R/W] 00000000	IBSR3 [R/W] 00000000	ITBA3 [R/W] -----00 00000000		
0000E8 <sub>H</sub>	ITMK3 [R/W] 00----11 11111111		ISMK3 [R/W] 01111111	ISBA3 [R/W] 00000000	
0000EC <sub>H</sub>	—	IDAR3 [R/W] 00000000	ICCR3 [R/W] 0-011111	IDBL3 [R/W] -----0	
0000F0 <sub>H</sub>	T0LPCR [R/W] ----000	T0CCR [R/W] 0-010000	T0TCR [R/W] 00000000	T0R [R/W] ---00000	Multi-functional Timer
0000F4 <sub>H</sub>	T0DRR [R/W] XXXXXXXX XXXXXXXX		T0CRR [R/W] XXXXXXXX XXXXXXXX		
0000F8 <sub>H</sub>	T1LPCR [R/W] ----000	T1CCR [R/W] 0-000000	T1TCR [R/W] 00000000	T1R [R/W] ---00000	
0000FC <sub>H</sub>	T1DRR [R/W] XXXXXXXX XXXXXXXX		T1CRR [R/W] XXXXXXXX XXXXXXXX		
000100 <sub>H</sub>	T2LPCR [R/W] ----000	T2CCR [R/W] 0-000000	T2TCR [R/W] 00000000	T2R [R/W] ---00000	
000104 <sub>H</sub>	T2DRR [R/W] XXXXXXXX XXXXXXXX		T2CRR [R/W] XXXXXXXX XXXXXXXX		
000108 <sub>H</sub>	T3LPCR [R/W] ----000	T3CCR [R/W] 0-000000	T3TCR [R/W] 00000000	T3R [R/W] ---00000	
00010C <sub>H</sub>	T3DRR [R/W] XXXXXXXX XXXXXXXX		T3CRR [R/W] XXXXXXXX XXXXXXXX		
000110 <sub>H</sub>	TMODE [R/W] ----- 0--		—	—	
000114 <sub>H</sub> to 00011F <sub>H</sub>	—		—		Reserved
000120 <sub>H</sub>	PTMR0 [R] 11111111 11111111		PCSR0 [W] XXXXXXXX XXXXXXXX		PPG0
000124 <sub>H</sub>	PDUT0 [W] XXXXXXXX XXXXXXXX		PCNH0 [R/W] 00000000	PCNL0 [R/W] 00000000	
000128 <sub>H</sub>	PTMR1 [R] 11111111 11111111		PCSR1 [W] XXXXXXXX XXXXXXXX		PPG1
00012C <sub>H</sub>	PDUT1 [W] XXXXXXXX XXXXXXXX		PCNH1 [R/W] 00000000	PCNL1 [R/W] 00000000	
000130 <sub>H</sub>	PTMR2 [R] 11111111 11111111		PCSR2 [W] XXXXXXXX XXXXXXXX		PPG2
000134 <sub>H</sub>	PDUT2 [W] XXXXXXXX XXXXXXXX		PCNH2 [R/W] 00000000	PCNL2 [R/W] 00000000	

(Continued)

# MB91319 Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000138 <sub>H</sub>	PTMR3 [R] 11111111 11111111		PCSR3[W] XXXXXXXX XXXXXXXX		PPG3
00013C <sub>H</sub>	PDUT3 [W] XXXXXXXX XXXXXXXX		PCNH3 [R/W] 00000000	PCNL3 [R/W] 00000000	
000140 <sub>H</sub> to 00014C <sub>H</sub>	—				Reserved
000150 <sub>H</sub> to 00015C <sub>H</sub>	—				Reserved
000160 <sub>H</sub>	DSLCO0 0-----	DSLCO10 -011----	CCDC0 00-00011	VSEP0 00--0001	CCD Slicer 0 channel
000164 <sub>H</sub>	CSYSEP0 -101-011	HMASK0 --100000	HCLR0 ---00110	FLD0 00100000	
000168 <sub>H</sub>	HCNT0 00000000	C21H0 0-111111	CRIP0 11111111	CRIC0 000-0000	
00016C <sub>H</sub>	CSTB0 11111111	CDTH0 11111111	CDAT00 00000000	CDAT10 00000000	
000170 <sub>H</sub>	ID1C0 0----00	ID20H0 0-111111	IDREF0 0-111111	IDTH0 11111111	
000174 <sub>H</sub>	IDSTB0 11111111	IDDAT00 --000000	IDDAT10 00000000	IDDAT20 --000000	
000178 <sub>H</sub>	DSAC10 ---000-0	DSAC20 10110011	DSAC30 00-00-00	—	
00017C <sub>H</sub>	—	—	—	—	
000180 <sub>H</sub>	DSLCO1 0-----	DSLCO11 -011----	CCDC1 00-00011	VSEP1 00--0001	CCD Slicer 1 channel
000184 <sub>H</sub>	CSYTSEP1 -101-011	HMASK1 --100000	HCLR1 ---00110	FLD1 00100000	
000188 <sub>H</sub>	HCNT1 00000000	C21H1 0-111111	CRIP1 11111111	CRIC1 000-0000	
00018C <sub>H</sub>	CSTB1 11111111	CDTH1 11111111	CDAT01 00000000	CDAT1 00000000	
000190 <sub>H</sub>	ID1C1 0-----00	ID20H1 0-111111	IDREF1 0-111111	IDTH1 11111111	
000194 <sub>H</sub>	IDSTB1 11111111	IDDAT01 --000000	IDDAT11 00000000	IDDAT21 --000000	
000198 <sub>H</sub>	DSAC11 ---000-0	DSAC21 10110011	DSAC31 00-00-00	—	
00019C <sub>H</sub>	—	—	—	—	

(Continued)

# MB91319 Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0001A0 <sub>H</sub> to 0001FC <sub>H</sub>	—				Reserved
000200 <sub>H</sub>	DMACA0 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000204 <sub>H</sub>	DMACB0 [R/W] 00000000 00000000 00000000 00000000				
000208 <sub>H</sub>	DMACA1 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00020C <sub>H</sub>	DMACB1 [R/W] 00000000 00000000 00000000 00000000				
000210 <sub>H</sub>	DMACA2 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000214 <sub>H</sub>	DMACB2 [R/W] 00000000 00000000 00000000 00000000				
000218 <sub>H</sub>	DMACA3 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00021C <sub>H</sub>	DMACB3 [R/W] 00000000 00000000 00000000 00000000				
000220 <sub>H</sub>	DMACA4 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000224 <sub>H</sub>	DMACB4 [R/W] 00000000 00000000 00000000 00000000				
000228 <sub>H</sub>	—				Reserved
00022C <sub>H</sub> to 00023C <sub>H</sub>	—				
000240 <sub>H</sub>	DMACR [R/W] 0XX00000 XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
000244 <sub>H</sub> to 0002FC <sub>H</sub>	—				Reserved
000300 <sub>H</sub> to 0003EC <sub>H</sub>	—				
0003F0 <sub>H</sub>	BSD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit Search Module
0003F4 <sub>H</sub>	BSD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003F8 <sub>H</sub>	BSDC [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003FC <sub>H</sub>	BSRR [R] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

(Continued)

# MB91319 Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000400 <sub>H</sub>	DDR0 [R/W] 00000000	DDR1 [R/W] 00000000	DDR2 [R/W] 00000000	DDR3 [R/W] 00000000	R-bus Port Direction Register
000404 <sub>H</sub>	DDR4 [R/W] 00000000	DDR5 [R/W] 00000000	—	DDR7 [R/W] --000000	
000408 <sub>H</sub>	DDR8 [R/W] 00000000	DDR9 [R/W] 00000000	DDRA [R/W] ----000	DDRB [R/W] 00000000	
00040C <sub>H</sub>	DDRC [R/W] 00000000	—	—	—	
000410 <sub>H</sub>	PFR0 [R/W] 0--00000	PFR1 [R/W] 00000000	PFR2 [R/W] 00000000	PFR3 [R/W] 00000000	R-bus Port Function Register
000414 <sub>H</sub>	PFR4 [R/W] 0000--00	PFR5 [R/W] 11111111	PFR6 [R/W] 11111111	PFR7 [R/W] 11111111	
000418 <sub>H</sub>	PFR8 [R/W] 11111111	PFR9 [R/W] 11111111	PFRA [R/W] 11111111	PFRB [R/W] 11111111	
00041C <sub>H</sub>	PFRC [R/W] 1111---1	PFRD [R/W] ---11111	—	—	
000420 <sub>H</sub> to 00043C <sub>H</sub>	—				Reserved
000440 <sub>H</sub>	ICR00 [R/W] ---11111	ICR01 [R/W] ---11111	ICR02 [R/W] ---11111	ICR03 [R/W] ---11111	Interrupt Control Unit
000444 <sub>H</sub>	ICR04 [R/W] ---11111	ICR05 [R/W] ---11111	ICR06 [R/W] ---11111	ICR07 [R/W] ---11111	
000448 <sub>H</sub>	ICR08 [R/W] ---11111	ICR09 [R/W] ---11111	ICR10 [R/W] ---11111	ICR11 [R/W] ---11111	
00044C <sub>H</sub>	ICR12 [R/W] ---11111	ICR13 [R/W] ---11111	ICR14 [R/W] ---11111	ICR15 [R/W] ---11111	
000450 <sub>H</sub>	ICR16 [R/W] ---11111	ICR17 [R/W] ---11111	ICR18 [R/W] ---11111	ICR19 [R/W] ---11111	
000454 <sub>H</sub>	ICR20 [R/W] ---11111	ICR21 [R/W] ---11111	ICR22 [R/W] ---11111	ICR23 [R/W] ---11111	
000458 <sub>H</sub>	ICR24 [R/W] ---11111	ICR25 [R/W] ---11111	ICR26 [R/W] ---11111	ICR27 [R/W] ---11111	
00045C <sub>H</sub>	ICR28 [R/W] ---11111	ICR29 [R/W] ---11111	ICR30 [R/W] ---11111	ICR31 [R/W] ---11111	
000460 <sub>H</sub>	ICR32 [R/W] ---11111	ICR33 [R/W] ---11111	ICR34 [R/W] ---11111	ICR35 [R/W] ---11111	
000464 <sub>H</sub>	ICR36 [R/W] ---11111	ICR37 [R/W] ---11111	ICR38 [R/W] ---11111	ICR39 [R/W] ---11111	
000468 <sub>H</sub>	ICR40 [R/W] ---11111	ICR41 [R/W] ---11111	ICR42 [R/W] ---11111	ICR43 [R/W] ---11111	
00046C <sub>H</sub>	ICR44 [R/W] ---11111	ICR45 [R/W] ---11111	ICR46 [R/W] ---11111	ICR47 [R/W] ---11111	

(Continued)

# MB91319 Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000470 <sub>H</sub> to 00047C <sub>H</sub>	—				Reserved
000480 <sub>H</sub>	RSRR [R/W] 10000000*2	STCR [R/W] 00110011*2	TBCR [R/W] 00XXXX00*1	CTBR [W] XXXXXXXX	Clock Control Unit
000484 <sub>H</sub>	CLKR [R/W] 00000000*1	WPR [W] XXXXXXXX	DIVR0 [R/W] 00000011*1	DIVR1[R/W] 00000000*1	
000488 <sub>H</sub>	—	—	OSCCR [R/W] XXXXXXXX0	—	Reserved
00048C <sub>H</sub>	WPCR [R/W] B 00---000	—	—	—	Watch Timer
000490 <sub>H</sub>	OSCR [R/W] B 00---000	—	—	—	Main Oscillation Stabilization Wait Timer
000494 <sub>H</sub> to 0005FC <sub>H</sub>	—				Reserved
000600 <sub>H</sub> to 0007FC <sub>H</sub>	—				Reserved
000800 <sub>H</sub> to 000AFC <sub>H</sub>	—				Reserved
000B00 <sub>H</sub>	ESTS0 [R/W] X0000000	ESTS1 [R/W] XXXXXXXX	ESTS2 [R] 1XXXXXXXX	—	DSU
000B04 <sub>H</sub>	ECTL0 [R/W] 0X000000	ECTL1 [R/W] 00000000	ECTL2 [W] 000X0000	ECTL3 [R/W] 00X00X11	
000B08 <sub>H</sub>	ECNT0 [W] XXXXXXXX	ECNT1 [W] XXXXXXXX	EUSA [W] XXX00000	EDTC [W] 0000XXXX	
000B0C <sub>H</sub>	EWP1 [R] 00000000 00000000		—		
000B10 <sub>H</sub>	EDTR0 [W] XXXXXXXX XXXXXXXX		EDTR1 [W] XXXXXXXX XXXXXXXX		
000B14 <sub>H</sub> to 000B1C <sub>H</sub>	—				
000B20 <sub>H</sub>	EIA0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B24 <sub>H</sub>	EIA1 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

(Continued)

# MB91319 Series

Address	Register				Block	
	+ 0	+ 1	+ 2	+ 3		
000B28 <sub>H</sub>	EIA2 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DSU	
000B2C <sub>H</sub>	EIA3 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000B30 <sub>H</sub>	EIA4 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000B34 <sub>H</sub>	EIA5 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000B38 <sub>H</sub>	EIA6 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000B3C <sub>H</sub>	EIA7 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000B40 <sub>H</sub>	EDTA [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000B44 <sub>H</sub>	EDTM [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000B48 <sub>H</sub>	EOA0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000B4C <sub>H</sub>	EOA1 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000B50 <sub>H</sub>	EPCR [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000B54 <sub>H</sub>	EPSR [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000B58 <sub>H</sub>	EIAM0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000B5C <sub>H</sub>	EIAM1 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000B60 <sub>H</sub>	EOAM0/EODM0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000B64 <sub>H</sub>	EOAM1/EODM1 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000B68 <sub>H</sub>	EOD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000B6C <sub>H</sub>	EOD1 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000B70 <sub>H</sub> to 000FFC <sub>H</sub>	—					Reserved

(Continued)

# MB91319 Series

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
001000 <sub>H</sub>	DMASA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
001004 <sub>H</sub>	DMADA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001008 <sub>H</sub>	DMASA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00100C <sub>H</sub>	DMADA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001010 <sub>H</sub>	DMASA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001014 <sub>H</sub>	DMADA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001018 <sub>H</sub>	DMASA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00101C <sub>H</sub>	DMADA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001020 <sub>H</sub>	DMASA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001024 <sub>H</sub>	DMADA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001028 <sub>H</sub> to 006FFC <sub>H</sub>	—				Reserved
007000 <sub>H</sub>	FLCR [R/W] 0110X000	—			Program FLASH I/F
007004 <sub>H</sub>	FLWC [R/W] 00010011	—			
007008 <sub>H</sub> to 0070FF <sub>H</sub>	—				Reserved
007100 <sub>H</sub>	FNCR [R/W] 0110X000	—			Font FLASH I/F
007104 <sub>H</sub>	FNWT [R/W] 00010011	—			

\*1 : The initial value of the register varies with the reset level. The initial value shown is the one after an INIT level reset.

\*2 : The initial value of the register varies with the reset level. The initial value shown is the one after an INIT level reset by the INIT pin.

# MB91319 Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
050000 <sub>H</sub> to 050024 <sub>H</sub>	Reserved				Reserved
050028 <sub>H</sub> to 05FFFF <sub>H</sub>	Reserved				Reserved
060000 <sub>H</sub>	FIFO0o [R] XXXXXXXX XXXXXXXX		FIFO0i [W] XXXXXXXX XXXXXXXX		USB Function
060004 <sub>H</sub>	FIFO1 [R] XXXXXXXX XXXXXXXX		FIFO2 [W] XXXXXXXX XXXXXXXX		
060008 <sub>H</sub>	FIFO3 [R] XXXXXXXX XXXXXXXX		—		
06000C <sub>H</sub> to 06001F <sub>H</sub>	Reserved				
060020 <sub>H</sub>	Reserved		CONT1 [R/W] 000XX0XX XXX00000		
060024 <sub>H</sub>	CONT2 [R/W] XXXXXXXX XXX00000		CONT3 [R/W] XXXXXXXX XXX00000		
060028 <sub>H</sub>	CONT4 [R/W] XXXXXXXX XXX00000		CONT5 [R/W] XXXXXXXX XXXX00XX		
06002C <sub>H</sub>	CONT6 [R/W] XXXXXXXX XXXX00XX		CONT7 [R/W] XXXXXXXX XXX00000		
060030 <sub>H</sub>	CONT8 [R/W] XXXXXXXX XXX00000		CONT9 [R/W] 0XX0XXXX 0XXX0000		
060034 <sub>H</sub>	CONT10 [R/W] 00000000 X00000XX		TTSIZE [R/W] 00010001 00010001		
060038 <sub>H</sub>	TRSIZE [R/W] 00010001 00010001		Reserved		
06003C <sub>H</sub>	Reserved				
060040 <sub>H</sub>	RSIZE0 [R] XXXXXXXX XXXX0000		Reserved		
060044 <sub>H</sub>	RSIZE1 [R] XXXXXXXX X0000000		Reserved		
060048 <sub>H</sub> to 06005F <sub>H</sub>	Reserved				
060060 <sub>H</sub>	Reserved		ST1 [R/W] XXXXXX00 00000000		
060064 <sub>H</sub>	Reserved				

(Continued)

# MB91319 Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
060068 <sub>H</sub>	ST2 [R] XXXXXXXX X0000000		ST3 [R/W] 00XXXXXXXX X0000000		USB Function
06006C <sub>H</sub>	ST4 [R/W] XXXXX000 00000000		ST5 [R/W] 0XX00XXX XX000000		
060070 <sub>H</sub> to 06007F <sub>H</sub>	Reserved				
060080 <sub>H</sub> to 06FFFF <sub>H</sub>	Reserved				Reserved
078000 <sub>H</sub>	OSD_VADR [W] XXXXXXXX XXXXXXXX		OSD_CD1 [W] XXXXXXXX XXXXXXXX		OSDC (MAIN)
078004 <sub>H</sub>	OSD_CD2 [W] XXXXXXXX XXXXXXXX		OSD_RCD1 [W] XXXXXXXX XXXXXXXX		
078008 <sub>H</sub>	OSD_RCD2 [W] XXXXXXXX XXXXXXXX		OSD_SOC1 [W] XXXXXXXX 0000XXXX		
07800C <sub>H</sub>	OSD_SOC2 [W] XXXXXXXX XXXXXXXX		OSD_VDPC [W] XXXXXXXX XXXXXXXX		
078010 <sub>H</sub>	OSD_HDPC [W] XXXXXXXX XXXXXXXX		OSD_CVSC [W] XXXXXXXX XXXXXXXX		
078014 <sub>H</sub>	OSD_SBFCC [W] XXXXXXXX XXXXXXXX		OSD_THCC [W] XXXXXXXX XXXXXXXX		
078018 <sub>H</sub>	OSD_GFCC [W] XXXXXXXX XXXXXXXX		OSD_SBCC1 [W] XXXXXXXX XXXXXXXX		
07801C <sub>H</sub>	OSD_SBCC2 [W] XXXXXXXX XXXXXXXX		OSD_SPCC1 [W] XXXXXXXX XXXXXXXX		
078020 <sub>H</sub>	OSD_SPCC2 [W] XXXXXXXX XXXXXXXX		OSD_SPCC3 [W] XXXXXXXX XXXXXXXX		
078024 <sub>H</sub>	OSD_SPCC4 [W] XXXXXXXX XXXXXXXX		OSD_SYNCC [W] XXXXXXXX XXXXXXXX		
078028 <sub>H</sub>	—		—		
07802C <sub>H</sub>	—		OSD_IOC1 [W] XXXXXXXX XXXXXX00		
078030 <sub>H</sub>	OSD_IOC2 [W] XXXXXXXX XXXXXXXX		OSD_DPC1 [W] XXXXXXXX XXXXXXXX		
078034 <sub>H</sub>	OSD_DPC2 [W] XXXXXXXX XXXXXXXX		OSD_DPC3 [W] XXXXXXXX XXXXXXXX		
078038 <sub>H</sub>	OSD_DPC4 [W] XXXXXXXX XXXXXXXX		OSD_IRC [W] XXXXXXXX XXXXXXXX		
07803C <sub>H</sub>	OSD_PLT0 [W] XXXXXXXX XXXXXXXX		OSD_PLT1 [W] XXXXXXXX XXXXXXXX		

(Continued)

# MB91319 Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
078040 <sub>H</sub>	OSD_PLT2 [W] XXXXXXXX XXXXXXXX		OSD_PLT3 [W] XXXXXXXX XXXXXXXX		OSDC (MAIN)
078044 <sub>H</sub>	OSD_PLT4 [W] XXXXXXXX XXXXXXXX		OSD_PLT5 [W] XXXXXXXX XXXXXXXX		
078048 <sub>H</sub>	OSD_PLT6 [W] XXXXXXXX XXXXXXXX		OSD_PLT7 [W] XXXXXXXX XXXXXXXX		
07804C <sub>H</sub>	OSD_PLT8 [W] XXXXXXXX XXXXXXXX		OSD_PLT9 [W] XXXXXXXX XXXXXXXX		
078050 <sub>H</sub>	OSD_PLT10 [W] XXXXXXXX XXXXXXXX		OSD_PLT11 [W] XXXXXXXX XXXXXXXX		
078054 <sub>H</sub>	OSD_PLT12 [W] XXXXXXXX XXXXXXXX		OSD_PLT13 [W] XXXXXXXX XXXXXXXX		
078058 <sub>H</sub>	OSD_PLT14 [W] XXXXXXXX XXXXXXXX		OSD_PLT15 [W] XXXXXXXX XXXXXXXX		
07805C <sub>H</sub>	OSD_ACT1 [W] XXXXXXXX XXXXXXXX		OSD_ACT2 [W] XXXXXXXX XXXXXXXX		
078060 <sub>H</sub>	OSD_PLACC11 [W] XXXXXXXX XXXXXXXX		OSD_PLACC12 [W] XXXXXXXX XXXXXXXX		
078064 <sub>H</sub>	OSD_PLACC2 [W] XXXXXXXX XXXXXXXX		OSD_PLACC3 [W] XXXXXXXX XXXXXXXX		
078068 <sub>H</sub>	OSD_PLBCC11 [W] XXXXXXXX XXXXXXXX		OSD_PLBCC12 [W] XXXXXXXX XXXXXXXX		
07806C <sub>H</sub>	OSD_PLBCC2 [W] XXXXXXXX XXXXXXXX		OSD_PLBCC3 [W] XXXXXXXX XXXXXXXX		
078070 <sub>H</sub>	OSD_PLCC11[W] XXXXXXXX XXXXXXXX		OSD_PLCC12[W] XXXXXXXX XXXXXXXX		
078074 <sub>H</sub>	OSD_PLCC2[W] XXXXXXXX XXXXXXXX		OSD_PLCC3[W] XXXXXXXX XXXXXXXX		
078078 <sub>H</sub>	OSD_CSC1 [W] XXXXXXXX XXXXXXXX		OSD_CSC2 [W] XXXXXXXX XXXXXXXX		
07807C <sub>H</sub> to 0780FF <sub>H</sub>	—		—		
078100 <sub>H</sub>	CCOSD_VADR [W] XXXXXXXX XXXXXXXX		CCOSD_CD1 [W] XXXXXXXX XXXXXXXX		OSDC (CC)
078104 <sub>H</sub>	CCOSD_CD2 [W] XXXXXXXX XXXXXXXX		CCOSD_RCD1 [W] XXXXXXXX XXXXXXXX		
078108 <sub>H</sub>	CCOSD_RCD2 [W] XXXXXXXX XXXXXXXX		CCOSD_SOC1 [W] XXXXXXXX 0000XXXX		
07810C <sub>H</sub>	CCOSD_SOC2 [W] XXXXXXXX XXXXXXXX		CCOSD_VDPC [W] XXXXXXXX XXXXXXXX		

(Continued)

# MB91319 Series

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
078110 <sub>H</sub>	CCOSD_HDPC [W] XXXXXXXX XXXXXXXX		CCOSD_CVSC [W] XXXXXXXX XXXXXXXX		OSDC (CC)
078114 <sub>H</sub>	—		CCOSD_THCC [W] XXXXXXXX XXXXXXXX		
078118 <sub>H</sub>	—		—		
07811C <sub>H</sub>	—		—		
078120 <sub>H</sub>	—		—		
078124 <sub>H</sub>	—		—		
078128 <sub>H</sub>	—		—		
07812C <sub>H</sub>	—		—		
078130 <sub>H</sub>	—		CCOSD_DPC1 [W] XXXXXXXX XXXXXXXX		
078134 <sub>H</sub>	CCOSD_DPC2 [W] XXXXXXXX XXXXXXXX		CCOSD_DPC3 [W] XXXXXXXX XXXXXXXX		
078138 <sub>H</sub>	CCOSD_DPC4 [W] XXXXXXXX XXXXXXXX		CCOSD_IRC [W] XXXXXXXX XXXXXXXX		
07813C <sub>H</sub>	CCOSD_PLT0 [W] XXXXXXXX XXXXXXXX		CCOSD_PLT1 [W] XXXXXXXX XXXXXXXX		
078140 <sub>H</sub>	CCOSD_PLT2 [W] XXXXXXXX XXXXXXXX		CCOSD_PLT3 [W] XXXXXXXX XXXXXXXX		
078144 <sub>H</sub>	CCOSD_PLT4 [W] XXXXXXXX XXXXXXXX		CCOSD_PLT5 [W] XXXXXXXX XXXXXXXX		
078148 <sub>H</sub>	CCOSD_PLT6 [W] XXXXXXXX XXXXXXXX		CCOSD_PLT7 [W] XXXXXXXX XXXXXXXX		
07814C <sub>H</sub>	CCOSD_PLT8 [W] XXXXXXXX XXXXXXXX		CCOSD_PLT9 [W] XXXXXXXX XXXXXXXX		
078150 <sub>H</sub>	CCOSD_PLT10 [W] XXXXXXXX XXXXXXXX		CCOSD_PLT11 [W] XXXXXXXX XXXXXXXX		
078154 <sub>H</sub>	CCOSD_PLT12 [W] XXXXXXXX XXXXXXXX		CCOSD_PLT13 [W] XXXXXXXX XXXXXXXX		
078158 <sub>H</sub>	CCOSD_PLT14 [W] XXXXXXXX XXXXXXXX		CCOSD_PLT15 [W] XXXXXXXX XXXXXXXX		
07815C <sub>H</sub>	—		—		
078160 <sub>H</sub> to 07FFFF <sub>H</sub>	Reserved				Reserved

## ■ INTERRUPT FACTORS, INTERRUPT VECTORS, AND INTERRUPT REGISTER

Interrupt factor	Interrupt number		Interrupt level	Offset	Address of TBR default	RN
	Decimal	Hexa-decimal				
Reset	0	00	—	3FC <sub>H</sub>	000FFFFC <sub>H</sub>	—
Mode vector	1	01	—	3F8 <sub>H</sub>	000FFFF8 <sub>H</sub>	—
System reserved	2	02	—	3F4 <sub>H</sub>	000FFFF4 <sub>H</sub>	—
System reserved	3	03	—	3F0 <sub>H</sub>	000FFFF0 <sub>H</sub>	—
System reserved	4	04	—	3EC <sub>H</sub>	000FFFE <sub>C</sub>	—
System reserved	5	05	—	3E8 <sub>H</sub>	000FFFE8 <sub>H</sub>	—
System reserved	6	06	—	3E4 <sub>H</sub>	000FFFE4 <sub>H</sub>	—
Coprocessor absent trap	7	07	—	3E0 <sub>H</sub>	000FFFE0 <sub>H</sub>	—
Coprocessor error trap	8	08	—	3DC <sub>H</sub>	000FFFD <sub>C</sub>	—
INTE instruction	9	09	—	3D8 <sub>H</sub>	000FFFD8 <sub>H</sub>	—
Instruction break exception	10	0A	—	3D4 <sub>H</sub>	000FFFD4 <sub>H</sub>	—
Operand break trap	11	0B	—	3D0 <sub>H</sub>	000FFFD0 <sub>H</sub>	—
Step trace trap	12	0C	—	3CC <sub>H</sub>	000FFFC <sub>C</sub>	—
NMI request (tool)	13	0D	—	3C8 <sub>H</sub>	000FFFC8 <sub>H</sub>	—
Undefined instruction exception	14	0E	—	3C4 <sub>H</sub>	000FFFC4 <sub>H</sub>	—
NMI request	15	0F	15 (F <sub>H</sub> ) fixed	3C0 <sub>H</sub>	000FFFC0 <sub>H</sub>	—
External interrupt 0	16	10	ICR00	3BC <sub>H</sub>	000FFFB <sub>C</sub>	—
External interrupt 1	17	11	ICR01	3B8 <sub>H</sub>	000FFFB8 <sub>H</sub>	—
External interrupt 2	18	12	ICR02	3B4 <sub>H</sub>	000FFFB4 <sub>H</sub>	—
External interrupt 3	19	13	ICR03	3B0 <sub>H</sub>	000FFFB0 <sub>H</sub>	—
External interrupt 4 (USB function)	20	14	ICR04	3AC <sub>H</sub>	000FFFA <sub>C</sub>	—
External interrupt 5 (OSDC-MAIN)	21	15	ICR05	3A8 <sub>H</sub>	000FFFA8 <sub>H</sub>	—
External interrupt 6 (OSDC-CC)	22	16	ICR06	3A4 <sub>H</sub>	000FFFA4 <sub>H</sub>	—
System reserved	23	17	ICR07	3A0 <sub>H</sub>	000FFFA0 <sub>H</sub>	—
Reload timer 0	24	18	ICR08	39C <sub>H</sub>	000FFF9 <sub>C</sub>	8
Reload timer 1	25	19	ICR09	398 <sub>H</sub>	000FFF98 <sub>H</sub>	9
Reload timer 2	26	1A	ICR10	394 <sub>H</sub>	000FFF94 <sub>H</sub>	10
UART0 (Reception completed)	27	1B	ICR11	390 <sub>H</sub>	000FFF90 <sub>H</sub>	0
UART1 (Reception completed)	28	1C	ICR12	38C <sub>H</sub>	000FFF8 <sub>C</sub>	1
UART2 (Reception completed)	29	1D	ICR13	388 <sub>H</sub>	000FFF88 <sub>H</sub>	2
UART0 (Transmission completed)	30	1E	ICR14	384 <sub>H</sub>	000FFF84 <sub>H</sub>	3
UART1 (Transmission completed)	31	1F	ICR15	380 <sub>H</sub>	000FFF80 <sub>H</sub>	4

(Continued)

# MB91319 Series

Interrupt factor	Interrupt number		Interrupt level	Offset	Address of TBR default	RN
	Decimal	Hexa-decimal				
UART2 (Transmission completed)	32	20	ICR16	37C <sub>H</sub>	000FFF7C <sub>H</sub>	5
DMAC0 (end, error)	33	21	ICR17	378 <sub>H</sub>	000FFF78 <sub>H</sub>	—
DMAC1 (end, error)	34	22	ICR18	374 <sub>H</sub>	000FFF74 <sub>H</sub>	—
DMAC2 (end, error)	35	23	ICR19	370 <sub>H</sub>	000FFF70 <sub>H</sub>	—
DMAC3 (end, error)	36	24	ICR20	36C <sub>H</sub>	000FFF6C <sub>H</sub>	—
DMAC4 (end, error)	37	25	ICR21	368 <sub>H</sub>	000FFF68 <sub>H</sub>	—
A/D	38	26	ICR22	364 <sub>H</sub>	000FFF64 <sub>H</sub>	—
PPG0	39	27	ICR23	360 <sub>H</sub>	000FFF60 <sub>H</sub>	—
PPG1	40	28	ICR24	35C <sub>H</sub>	000FFF5C <sub>H</sub>	—
PPG2	41	29	ICR25	358 <sub>H</sub>	000FFF58 <sub>H</sub>	—
PPG3	42	2A	ICR26	354 <sub>H</sub>	000FFF54 <sub>H</sub>	—
PWC	43	2B	ICR27	350 <sub>H</sub>	000FFF50 <sub>H</sub>	—
CCD0	44	2C	ICR28	34C <sub>H</sub>	000FFF4C <sub>H</sub>	—
CCD1	45	2D	ICR29	348 <sub>H</sub>	000FFF48 <sub>H</sub>	—
Main oscillation wait	46	2E	ICR30	344 <sub>H</sub>	000FFF44 <sub>H</sub>	—
Timebase timer overflow	47	2F	ICR31	340 <sub>H</sub>	000FFF40 <sub>H</sub>	—
System reserved	48	30	ICR32	33C <sub>H</sub>	000FFF3C <sub>H</sub>	—
Watch timer	49	31	ICR33	338 <sub>H</sub>	000FFF38 <sub>H</sub>	—
I <sup>2</sup> C ch0	50	32	ICR34	334 <sub>H</sub>	000FFF34 <sub>H</sub>	—
I <sup>2</sup> C ch1	51	33	ICR35	330 <sub>H</sub>	000FFF30 <sub>H</sub>	—
I <sup>2</sup> C ch2	52	34	ICR36	32C <sub>H</sub>	000FFF2C <sub>H</sub>	—
I <sup>2</sup> C ch3	53	35	ICR37	328 <sub>H</sub>	000FFF28 <sub>H</sub>	—
UART3 (Reception completed)	54	36	ICR38	324 <sub>H</sub>	000FFF24 <sub>H</sub>	—
UART4 (Reception completed)	55	37	ICR39	320 <sub>H</sub>	000FFF20 <sub>H</sub>	—
UART3 (Transmission completed)	56	38	ICR40	31C <sub>H</sub>	000FFF1C <sub>H</sub>	—
UART4 (Reception completed)	57	39	ICR41	318 <sub>H</sub>	000FFF18 <sub>H</sub>	—
Multi-functional timer 0	58	3A	ICR42	314 <sub>H</sub>	000FFF14 <sub>H</sub>	—
Multi-functional timer 1	59	3B	ICR43	310 <sub>H</sub>	000FFF10 <sub>H</sub>	—
Multi-functional timer 2	60	3C	ICR44	30C <sub>H</sub>	000FFF0C <sub>H</sub>	—
Multi-functional timer 3	61	3D	ICR45	308 <sub>H</sub>	000FFF08 <sub>H</sub>	—
System reserved	62	3E	ICR46	304 <sub>H</sub>	000FFF04 <sub>H</sub>	—
Delay interrupt factor bit	63	3F	ICR47	300 <sub>H</sub>	000FFF00 <sub>H</sub>	—
System reserved (Used by REALOS)	64	40	—	2FC <sub>H</sub>	000FFEFC <sub>H</sub>	—
System reserved (Used by REALOS)	65	41	—	2F8 <sub>H</sub>	000FFE8 <sub>H</sub>	—

(Continued)

(Continued)

Interrupt factor	Interrupt number		Interrupt level	Offset	Address of TBR default	RN
	Decimal	Hexa-decimal				
System reserved	66	42	—	2F4 <sub>H</sub>	000FFE4 <sub>H</sub>	—
System reserved	67	43	—	2F0 <sub>H</sub>	000FFE0 <sub>H</sub>	—
System reserved	68	44	—	2EC <sub>H</sub>	000FEEC <sub>H</sub>	—
System reserved	69	45	—	2E8 <sub>H</sub>	000FEE8 <sub>H</sub>	—
System reserved	70	46	—	2E4 <sub>H</sub>	000FEE4 <sub>H</sub>	—
System reserved	71	47	—	2E0 <sub>H</sub>	000FEE0 <sub>H</sub>	—
System reserved	72	48	—	2DC <sub>H</sub>	000FEDC <sub>H</sub>	—
System reserved	73	49	—	2D8 <sub>H</sub>	000FED8 <sub>H</sub>	—
System reserved	74	4A	—	2D4 <sub>H</sub>	000FED4 <sub>H</sub>	—
System reserved	75	4B	—	2D0 <sub>H</sub>	000FED0 <sub>H</sub>	—
System reserved	76	4C	—	2CC <sub>H</sub>	000FECC <sub>H</sub>	—
System reserved	77	4D	—	2C8 <sub>H</sub>	000FEC8 <sub>H</sub>	—
System reserved	78	4E	—	2C4 <sub>H</sub>	000FEC4 <sub>H</sub>	—
System reserved	79	4F	—	2C0 <sub>H</sub>	000FEC0 <sub>H</sub>	—
Used by INT instruction	80 to 255	50 to FF	—	2BC <sub>H</sub> to 000 <sub>H</sub>	000FEBC <sub>H</sub> to 00FFC00 <sub>H</sub>	—

# MB91319 Series

## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage *	V <sub>DDE</sub> (3.3 V)	V <sub>SS</sub> - 0.5	V <sub>SS</sub> + 4.0	V	
	V <sub>DDI</sub> (2.5 V)	V <sub>SS</sub> - 0.5	V <sub>SS</sub> + 3.0	V	
Analog power supply voltage *	AV <sub>CC</sub>	V <sub>SS</sub> - 0.5	V <sub>SS</sub> + 4.0	V	
Input voltage *	V <sub>I</sub>	V <sub>SS</sub> - 0.5	V <sub>DDE</sub> + 0.5	V	
Analog pin input voltage *	V <sub>IA</sub>	V <sub>SS</sub> - 0.5	AV <sub>CC</sub> + 0.5	V	
Output voltage *	V <sub>O</sub>	V <sub>SS</sub> - 0.5	V <sub>DDE</sub> + 0.5	V	
Storage temperature	T <sub>stg</sub>	- 40	+ 125	°C	

\* : The parameter is based on V<sub>SS</sub> = 0 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

### 2. Recommended Operating Conditions

(V<sub>SS</sub> = 0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Operating temperature	T <sub>a</sub>	- 40	+ 70	°C	
Power supply voltage	V <sub>DDE</sub> (3.3 V)	3.00	3.6	V	
	V <sub>DDI</sub> (2.5 V)	2.30	2.70		
Analog power supply voltage	AV <sub>CC</sub>	3.00	V <sub>DDE</sub>	V	

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

## 3. DC Characteristics

### (1) CPU

( $T_a = -10\text{ }^\circ\text{C}$  to  $+70\text{ }^\circ\text{C}$ ,  $V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{DDI} = 2.5\text{ V} \pm 0.2\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Power supply current	$I_{CCT}$	Watch mode $T_a = +25\text{ }^\circ\text{C}$ , $f_{clk} = 32\text{ kHz}$	—	800	1300	$\mu\text{A}$	Dot clock PLL stop USB clock stop
	$I_{CC}$	ROM product normal operation $T_a = +25\text{ }^\circ\text{C}$ , $f_{cp} = 40\text{ MHz}$ , $f_{cpp} = 20\text{ MHz}$	—	240	280	$\text{mA}$	Font Mask ROM Dot clock at 90 MHz
	$I_{CCS}$	Main sleep mode $T_a = +25\text{ }^\circ\text{C}$ , $f_{cp} = 40\text{ MHz}$ , $f_{cpp} = 20\text{ MHz}$	—	160	200	$\text{mA}$	Dot clock PLL stop
	$I_{CCL}$	Sub RUN mode $T_a = +25\text{ }^\circ\text{C}$ , $f_{clk} = 32\text{ kHz}$	—	1000	1700	$\mu\text{A}$	Dot clock PLL stop USB clock stop
	$I_{CCH}$	Main stop mode $T_a = +25\text{ }^\circ\text{C}$ , $f_{clk} = 0\text{ kHz}$	—	150	400	$\mu\text{A}$	Font Mask ROM
		Main stop mode $T_a = +70\text{ }^\circ\text{C}$ , $f_{clk} = 0\text{ kHz}$	—	1200	4000	$\mu\text{A}$	Font Mask ROM
"H" level input voltage	$V_{IH}$	—	$V_{CC} \times 0.8$	—	$V_{CC}$	$\text{V}$	
"L" level input voltage	$V_{IL}$	$V_{CC} = 3.3\text{ V}$	$V_{SS}$	—	$V_{CC} \times 0.2$	$\text{V}$	P00 to P74, PA0 to PA2, PB0 to PB7, PC0 to PC7, DCKI, HSYNC1 to HSYNC3, VSYNC
		$V_{CC} = 2.5\text{ V}$			$V_{CC} \times 0.15$	$\text{V}$	B0 to B2, G0 to G2, R0 to R2, VOB1, VOB2, DCKO, FH
"H" level output voltage	$V_{OH}$	$V_{CC} = 3.3\text{ V}$ , $I_{OH} = -4\text{ mA}$	$V_{CC} - 0.5$	—	$V_{CC}$	$\text{V}$	P0 to PC
		$V_{CC} = 2.5\text{ V}$ , $I_{OH} = -4\text{ mA}$				$\text{V}$	B0 to B2, G0 to G2, R0 to R2, VOB1, VOB2, DCKO, FH
"L" level output voltage	$V_{OL}$	$V_{CC} = 3.3\text{ V}$ , $I_{OL} = 4\text{ mA}$	$V_{SS}$	—	0.4	$\text{V}$	P0 to PC
		$V_{CC} = 2.5\text{ V}$ , $I_{OL} = 4\text{ mA}$				$\text{V}$	B0 to B2, G0 to G2, R0 to R2, VOB1, VOB2, DCKO, FH
Input leak current	$I_{IL}$	—	-5	—	5	$\mu\text{A}$	
I <sup>2</sup> C bus switch connection resistance	$R_{BS}$	—	—	—	130	$\Omega$	Between SCL2 and SCL3 Between SDA2 and SDA3 Between SCL3 and SCL4 Between SDA3 and SDA4

(Continued)

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(Continued)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Analog RGB reference voltage	V <sub>REF</sub>	—	1.05	1.10	1.15	V	VREF
Analog RGB reference resistance	R <sub>REF</sub>	—	2.4	2.7	—	kΩ	Between VR0 and GND
Analog RGB output impedance	R <sub>L</sub>	—	—	150	160	Ω	ROUT, GOUT, BOUT

## (2) USB

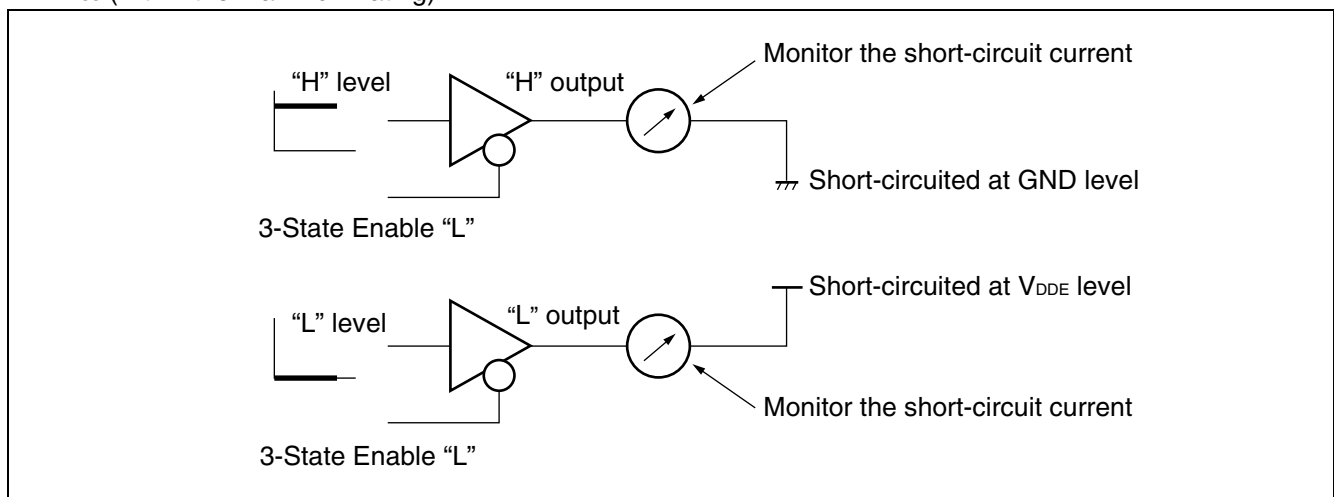
### • DC Characteristics (1)

( $T_a = -10\text{ }^{\circ}\text{C}$  to  $+70\text{ }^{\circ}\text{C}$ ,  $V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{DDI} = 2.5\text{ V} \pm 0.2\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Pin	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	$V_{OH}$	—	$I_{OH} = -100\text{ }\mu\text{A}$	$V_{DDE} - 0.2$	—	$V_{DDE}$	V	
"L" level output voltage	$V_{OL}$	—	$I_{OL} = 100\text{ }\mu\text{A}$	0	—	0.2	V	
"H" level output current	$I_{OH}$	—	At Full Speed Mode $V_{OH} = V_{DDE} - 0.4\text{ V}$	-20	—	—	mA	
			At Low Speed Mode $V_{OH} = V_{DDE} - 0.4\text{ V}$	-6	—	—	mA	
"L" level output current	$I_{OL}$	—	At Full Speed Mode $V_{OL} = 0.4\text{ V}$	20	—	—	mA	
			At Low Speed Mode $V_{OL} = 0.4\text{ V}$	6	—	—	mA	
Output short-circuit current	$I_{OS}$	—	—	—	—	300	mA	*1
Input leak current	$I_{LZ}$	—	—	—	—	$\pm 5$	$\mu\text{A}$	*2

\*1 : About the output short-circuit current  $I_{OS}$

Output short-circuit current  $I_{OS}$  is the maximum current that flows when the output pin is connected to  $V_{DDE}$  or  $V_{SS}$  (within the maximum rating) .

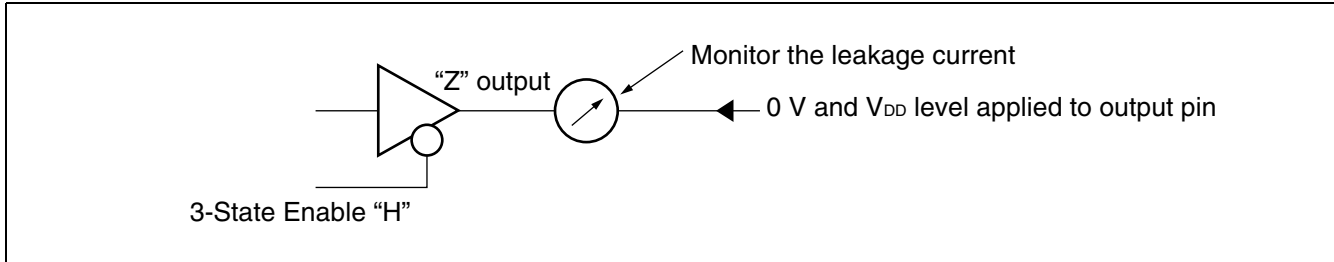


About the output short-circuit current : The current is "the short-circuit current per differential output pin". As the USB I/O buffer is a differential output, the short-circuit current should be considered for both of the output pins.

# MB91319 Series

\*2 : About measurement of "Z" leakage current  $I_{LZ}$

Input leakage current  $I_{LZ}$  is measured with the USB I/O buffer in the high-impedance state when the  $V_{DDE}$  or  $V_{SS}$  voltage is applied to the bidirectional pin.



- DC Characteristics (2)

Conform to the USB Specification Revision 1.1.

( $T_a = -10\text{ }^\circ\text{C}$  to  $+70\text{ }^\circ\text{C}$ ,  $V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{DDI} = 2.5\text{ V} \pm 0.2\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Input Voltage :					
High (driven)	$V_{IH}$	2.0	—	V	*1
Low	$V_{IL}$	—	0.8	V	*1
Differential Input Sensitivity	$V_{DI}$	0.2	—	V	*2
Common Mode Input Voltage	$V_{CM}$	0.8	2.5	V	*2
Output Voltage :					
Low	$V_{OL}$	0.0	0.3	V	*3
High (driven)	$V_{OH}$	2.8	3.6	V	*3
Output Signal Crossover Voltage	$V_{CRS}$	1.3	2.0	V	*4
Terminations :					
Pull-Up Resistor on Upstream Port	$R_{PU}$	1.425	1.575	$k\Omega$	$1.5\text{ k}\Omega \pm 5\%$
Pull-Down Resistor on Downstream Port	$R_{PD}$	1.425	1.575	$k\Omega$	$1.5\text{ k}\Omega \pm 5\%$
Termination voltage for upstream port pull-up	$V_{TERM}$	3.0	3.6	V	*5

\*1 : About input voltage  $V_{IH}$ ,  $V_{IL}$

The switching threshold voltage of the USB I/O buffer's single-end receiver is set within the range from  $V_{IL}(\text{Max}) = 0.8\text{ V}$  to  $V_{IH}(\text{Min}) = 2.0\text{ V}$  (TTL input standard) .

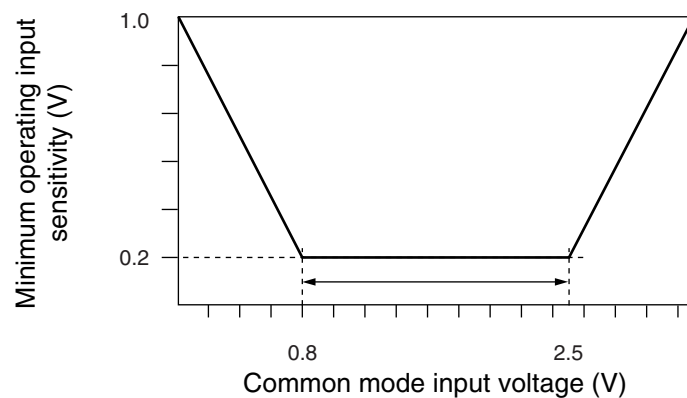
For  $V_{IH}$  and  $V_{IL}$ , the LSI has some hysteresis to reduce noise susceptibility.

\*2 : About input voltage  $V_{DI}$ ,  $V_{CM}$

A differential receiver is used to receive USB differential data signals.

The differential receiver has a differential input sensitivity of 200 mV when the differential data input falls within the range from 0.8 V to 2.5 V with respect to the local ground reference level.

The above voltage range is referred to as common-mode input voltage range.



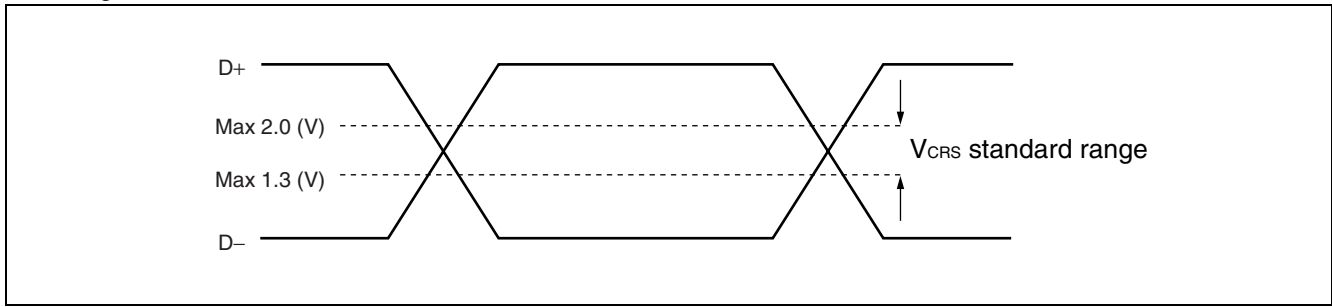
# MB91319 Series

**\*3 : About output voltage  $V_{OL}$ ,  $V_{OH}$**

The output driving performance levels of the driver are 0.3 V or less (to 3.6 V, 1.5 k $\Omega$  load) in the low state ( $V_{OL}$ ) and 2.8 V or more (to ground, 1.5 k $\Omega$  load) in the high state ( $V_{OH}$ ) .

**\*4 : About output voltage  $V_{CRS}$**

The cross voltage of the external differential output signals (D+ and D-) for the USB I/O buffer falls within the range from 1.3 V to 2.0 V.



**\*5 : About terminations  $V_{TERM}$**

$V_{TERM}$  indicates the pull-up voltage at the upstream port.

## 4. AC Characteristics

### (1) Clock Timing

( $T_a = -10\text{ }^\circ\text{C}$  to  $+70\text{ }^\circ\text{C}$ ,  $V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{DDI} = 2.5\text{ V} \pm 0.2\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
Clock frequency	$f_c$	X0, X1	—	6.25	10	MHz	PLL system (operation at a maximum internal speed of 40 MHz by quadrupling a self-oscillation frequency of 10 MHz via PLL)
Internal operating clock frequency	$f_{CP}$	—	—	1.56*	40	MHz	CPU system ( $t_{CP} = 1/f_{CP}$ )
	$f_{CPP}$			1.56*	20	MHz	Peripheral system ( $t_{CPP} = 1/f_{CPP}$ )
	$f_{CPT}$			1.56*	20	MHz	External bus system ( $t_{CPT} = 1/f_{CPT}$ )

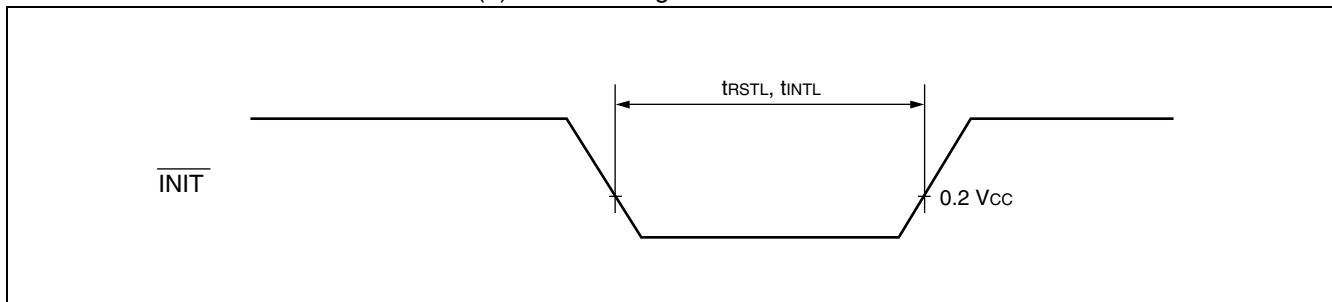
\* : The numeric value when inputting the 6.25 MHz (the minimum clock frequency) to X0 and using the PLL system and the gear ratio 1/16 of the oscillator circuit.

### (2) Reset Input

( $T_a = -10\text{ }^\circ\text{C}$  to  $+70\text{ }^\circ\text{C}$ ,  $V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{DDI} = 2.5\text{ V} \pm 0.2\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
INIT input time (at power-on)	$t_{INTL}$	$\overline{\text{INIT}}$	—	Oscillation stabilization wait time of oscillator + $t_{CP} \times 10$	—	$\mu\text{s}$	
INIT input time (other than at power-on)				$t_{CP} \times 10$	—	ns	
INIT input time (at recovering stop)				Oscillation stabilization wait time of oscillator + $t_{CP} \times 10$	—	$\mu\text{s}$	

Note:  $t_{CP}$  is the internal clock time. See “(1) Clock Timing”.



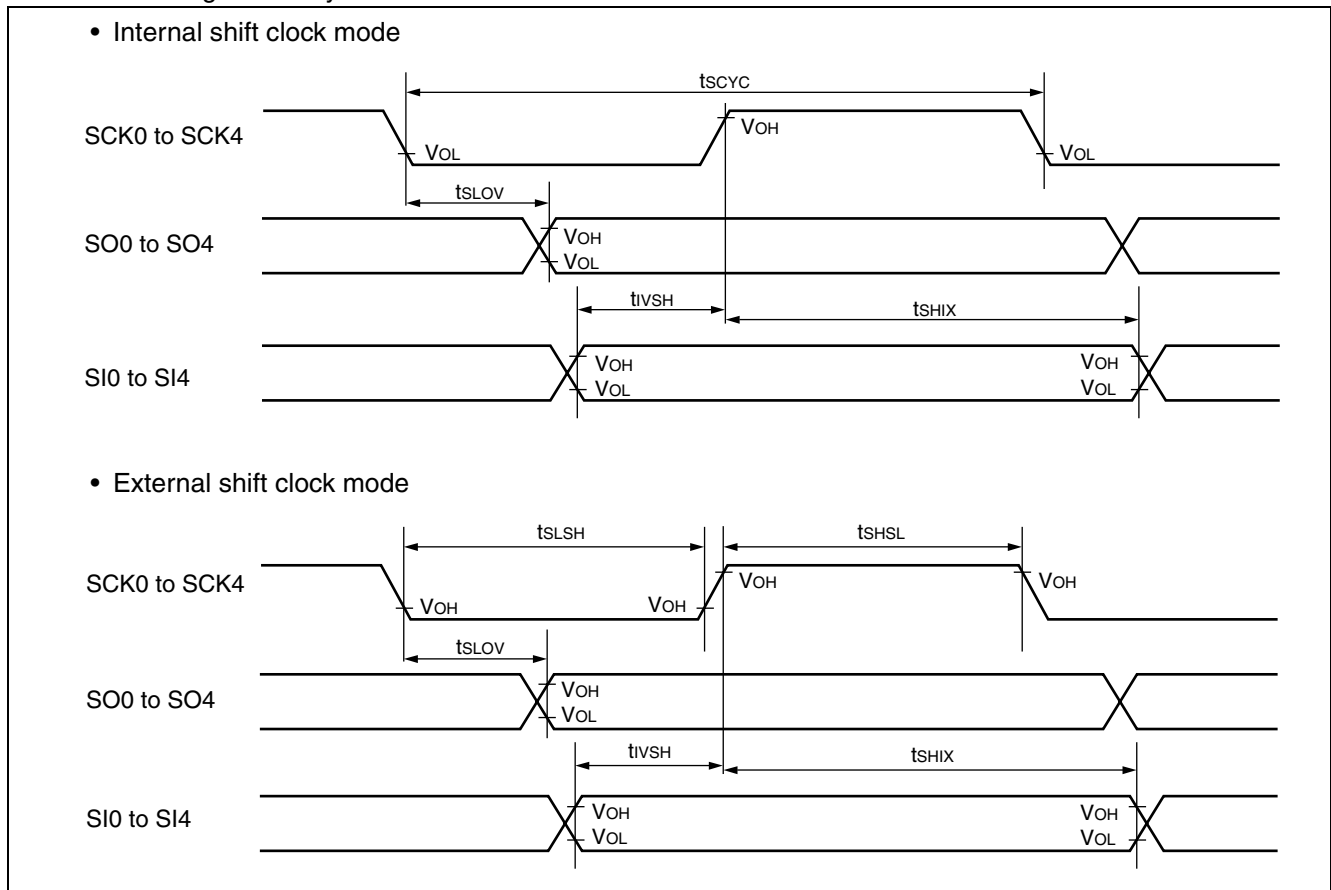
# MB91319 Series

## (3) UART Timing

( $T_a = -10\text{ }^\circ\text{C}$  to  $+70\text{ }^\circ\text{C}$ ,  $V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{DDI} = 2.5\text{ V} \pm 0.2\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	$t_{SCYC}$	SCK0 to SCK4	Internal shift lock mode	$8 t_{CPP}$	—	ns	
SCK $\downarrow$ $\rightarrow$ SO delay time	$t_{SLOV}$	SCK0 to SCK4, SO0 to SO4		-80	80	ns	
Valid SIN $\rightarrow$ SCK $\uparrow$	$t_{IVSH}$	SCK0 to SCK4, SI0 to SI4		100	—	ns	
SCK $\uparrow$ $\rightarrow$ valid SI hold time	$t_{SHIX}$	SCK0 to SCK4, SI0 to SI4		60	—	ns	
Serial clock "H" pulse width	$t_{SHSL}$	SCK0 to SCK4	External shift lock mode	$4 t_{CPP}$	—	ns	
Serial clock "L" pulse width	$t_{LSLH}$	SCK0 to SCK4		$4 t_{CPP}$	—	ns	
SCK $\downarrow$ $\rightarrow$ SO delay time	$t_{SLOV}$	SCK0 to SCK4, SO0 to SO4		—	150	ns	
Valid SI $\rightarrow$ SCK $\uparrow$	$t_{IVSH}$	SCK0 to SCK4, SI0 to SI4		60	—	ns	
Valid SCK $\uparrow$ $\rightarrow$ valid SI hold time	$t_{SHIX}$	SCK0 to SCK4, SI0 to SI4		60	—	ns	

Note : •  $t_{CPP}$  indicates the peripheral clock cycle time. See "(1) Clock Timing".  
 • AC rating in CLK synchronous mode.

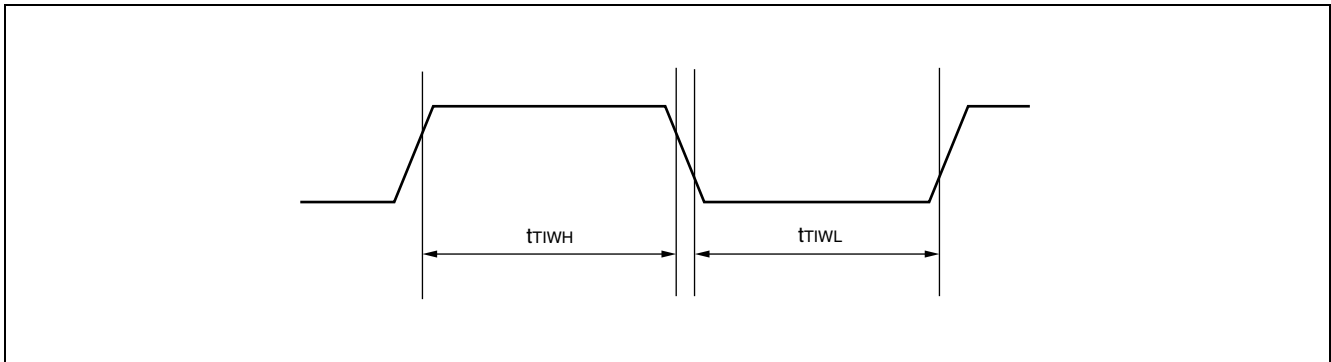


## (4) Reload timer clock , PPG timer input, multi-functional timer input timing

( $T_a = -10\text{ }^{\circ}\text{C}$  to  $+70\text{ }^{\circ}\text{C}$ ,  $V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{DDI} = 2.5\text{ V} \pm 0.2\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	$t_{TIWH}$ $t_{TIWL}$	TIN0 to TIN2, PPG0 to PPG3, TRG0 to TRG3, TMI0 to TMI3	—	$2 t_{CPP}$	—	ns	

Note :  $t_{CPP}$  indicates the peripheral clock cycle time. See “(1) Clock Timing”.

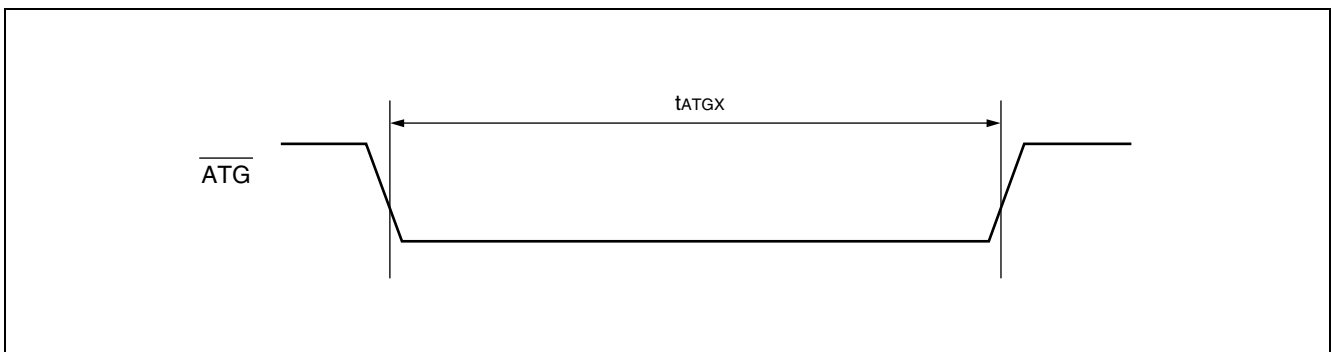


## (5) Trigger Input Timing

( $T_a = -10\text{ }^{\circ}\text{C}$  to  $+70\text{ }^{\circ}\text{C}$ ,  $V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{DDI} = 2.5\text{ V} \pm 0.2\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
A/D activation trigger input time	$t_{ATGX}$	$\overline{ATG}$	—	$5 t_{CPP}$	—	ns	

Note :  $t_{CPP}$  indicates the peripheral clock cycle time. See “(1) Clock Timing”.

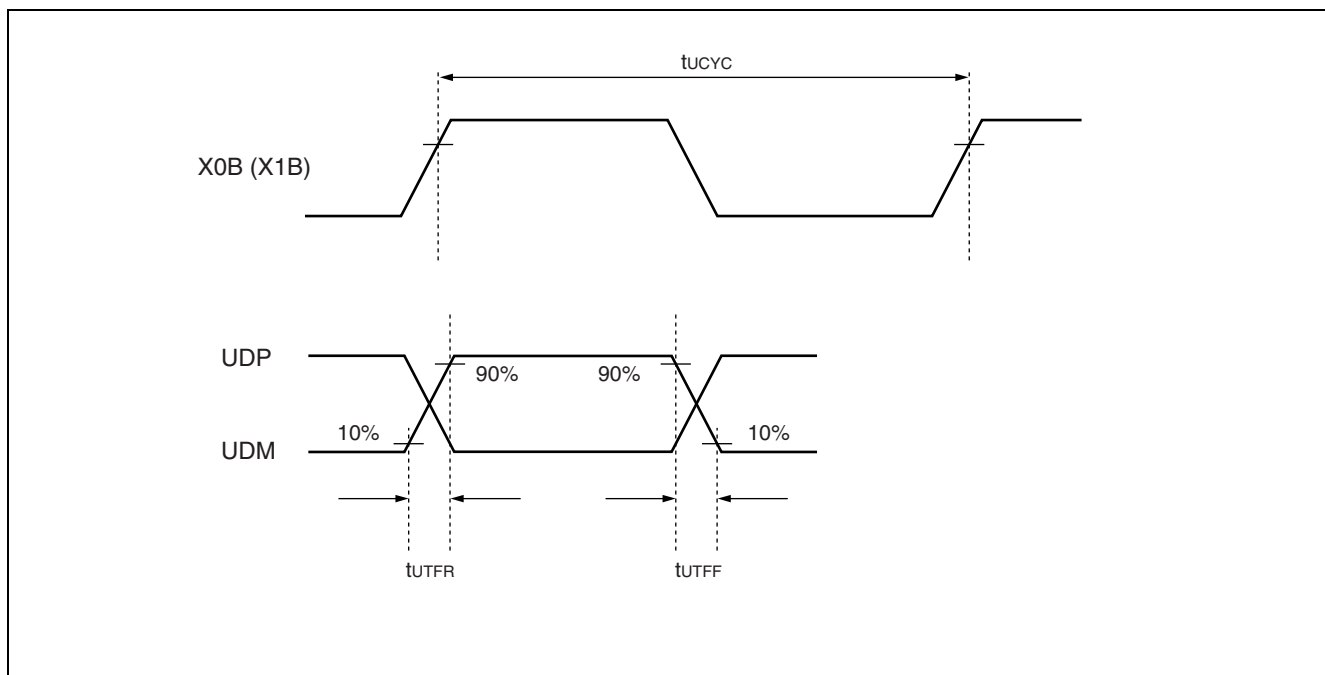


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## (6) USB interface

( $T_a = -10\text{ }^{\circ}\text{C}$  to  $+70\text{ }^{\circ}\text{C}$ ,  $V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{DDI} = 2.5\text{ V} \pm 0.2\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Pin	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input clock	$t_{CYC}$	X0B, X1B	—	—	48*1	—	MHz	Self-oscillation 500 ppm accuracy *1
		X0B	—	—	—	—		External input 500 ppm accuracy *1
Rise Time	$t_{UTFR}$	UDP/ UDM	At Full Speed Mode	4	—	20	ns	*2
Fall Time	$t_{UTFF}$	UDP/ UDM	At Full Speed Mode	4	—	20	ns	*2
Differential Rise and Fall Timing Matching	$t_{UTFRFM}$	UDP/ UDM	At Full Speed Mode	90	—	111.11	%	*2
Driver Output Resistance	$t_{ZDRV}$	UDP, UDM	—	28	—	44	$\Omega$	*3



\*1 : The AC characteristics of the USB interface conform to USB Specification Revision 1.1.

\*2 : About driver characteristics  $t_{UTFR}$ ,  $t_{UTFF}$ ,  $t_{UTFRFM}$

These items specify the differential data signal rise (Rise Time) and fall (Fall time) times.

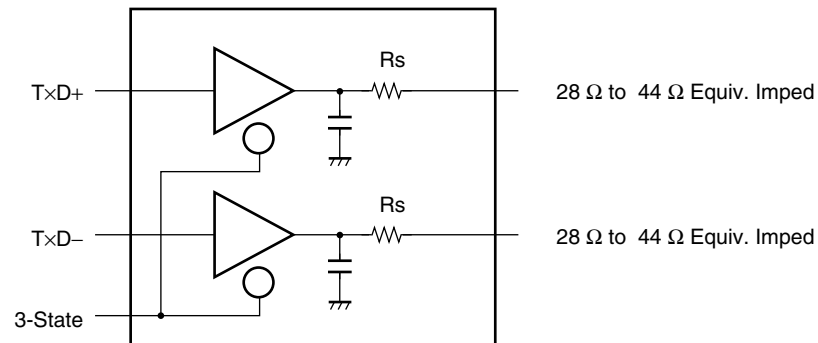
These are defined as the times between 10% to 90% of the output signal voltage.

For the full-speed buffer,  $t_{UTFR}$  and  $t_{UTFF}$  are specified such that the  $t_{UTFR}/t_{UTFF}$  ratio falls within  $\pm 10\%$  to minimize RFI radiation.

### \*3 : About driver characteristics ZDRV

USB full-speed connection is performed via a shielded twisted-pair cable at a characteristic impedance of  $90\ \Omega \pm 15\%$ . The USB Standard stipulates that the USB driver's output impedance must be within the range of  $28\ \Omega$  to  $44\ \Omega$ . The USB Standard also stipulates that a discrete serial resistor ( $R_s$ ) must be added to have balance while satisfying the above standard.

The output impedance of the USB I/O buffer on this LSI is about  $3\ \Omega$  to  $19\ \Omega$ . Therefore, serial resistor  $R_s$  to be added must be  $25\ \Omega$  to  $30\ \Omega$  ( $27\ \Omega$  recommended) .



Driver output impedance  $3\ \Omega$  to  $19\ \Omega$   
 $R_s$  serial resistance:  $25\ \Omega$  to  $30\ \Omega$   
Add a serial resistor of preferably  $27\ \Omega$

# MB91319 Series

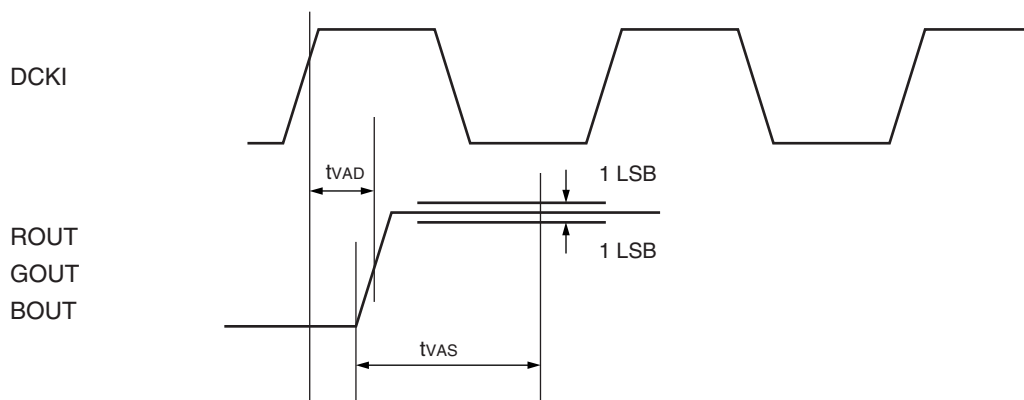
## (7) Analog RGB

( $T_a = -10\text{ }^\circ\text{C}$  to  $+70\text{ }^\circ\text{C}$ ,  $V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{DDI} = 2.5\text{ V} \pm 0.2\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Pin	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Analog RGB output delay	$t_{VAD}$	ROUT, GOUT, BOUT	$V_{REF} = 1.1\text{ V}$ , $V_{DDR} = V_{DDG} =$	—	12	—	ns	50 MHz (Max)
Analog RGB output settling time	$t_{VAS}$	ROUT, GOUT, BOUT	$V_{DDB} = 2.5\text{ V}$ , $V_{RO}^* = 2.7\text{ k}\Omega$	—	—	20	ns	

\* :  $V_{RO}$  is an external resistor for DAC.

### • Display signal output timing



## (8) Digital RGB

Vertical synchronous, horizontal synchronous, and display output control signal input timing

( $T_a = -10\text{ }^\circ\text{C}$  to  $+70\text{ }^\circ\text{C}$ ,  $V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{DDI} = 2.5\text{ V} \pm 0.2\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

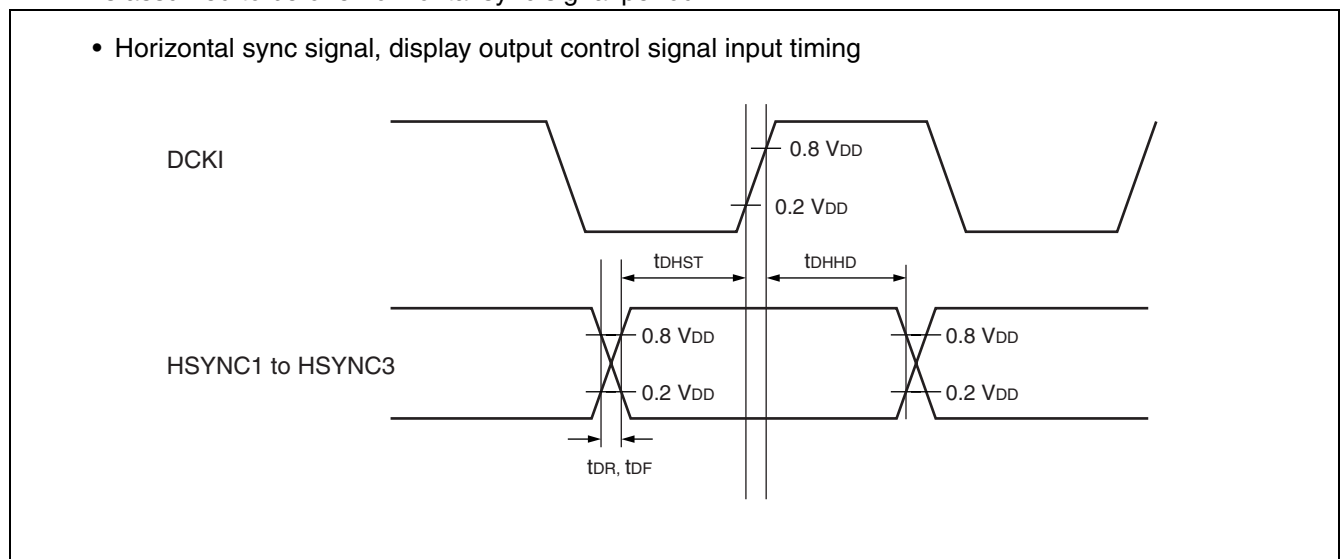
Parameter	Symbol	Pin	Value		Unit	Remarks
			Min	Max		
Horizontal sync signal cycle time	$t_{HCYC}$	HSYNC1 to HSYNC3	$100 + t_{WH}$	—	Dot clock	
Horizontal sync signal pulse width	$t_{WH}$	HSYNC1 to HSYNC3	20	—	Dot clock	*1
			—	6	$\mu\text{s}$	
Horizontal sync signal setup time	$t_{DHST}$	HSYNC1 to HSYNC3	4	—	ns	
Horizontal sync signal hold time	$t_{DHHD}$		0	—	ns	
Vertical sync signal setup time	$t_{HVST}$	VSYNC	5	$1H^{*2} - 5$	Dot clock	
Vertical sync signal hold time	$t_{HVHD}$		3	—	$H^{*2}$	
Input sync signal rise/fall time	$t_{DR}$	HSYNC1 to HSYNC3, VSYNC	—	2	ns	
	$t_{DF}$					

\*1 : During the horizontal sync signal pulse period, the device stops its internal OSDG operation, disabling writing to the internal VRAM. Therefore, set the horizontal sync signal pulse width and VRAM write cycle to ensure that : horizontal sync signal pulse width < VRAM write cycle.

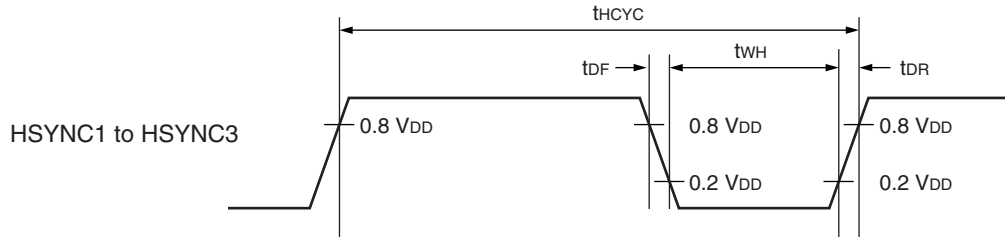
Precisely, adjust the command issuance interval not to issue command 2 or command 4 (VRAM write command) more than twice in the horizontal sync signal pulse width period.

If the above condition is not satisfied, the device may fail writing to VRAM.

\*2 : 1H is assumed to be one horizontal sync signal period.

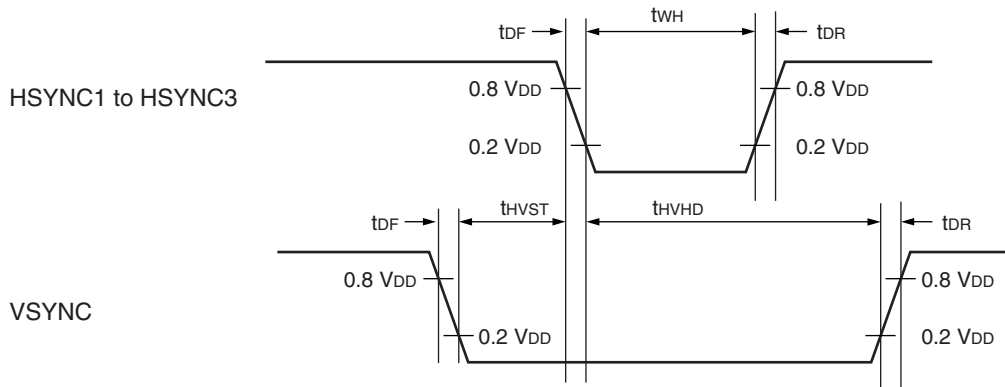


- Horizontal sync signal input

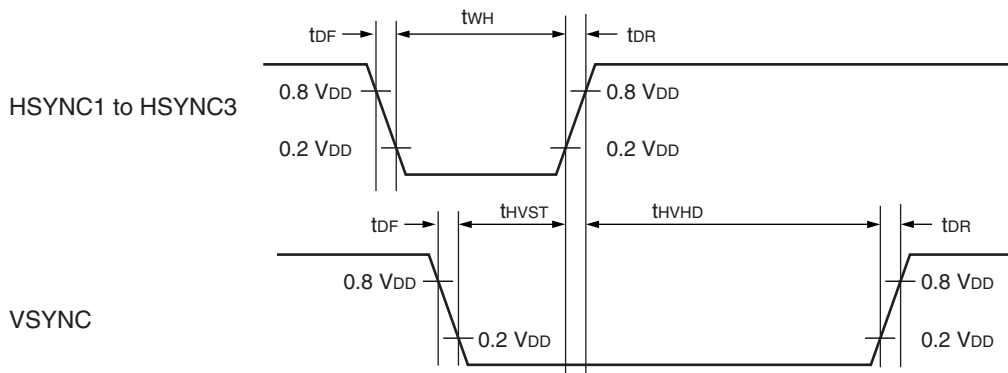


- Vertical sync signal input timing

- VSYNC detection at the leading edge of HSYNC



- VSYNC detection at the trailing edge of HSYNC



## (9) Display signal timing

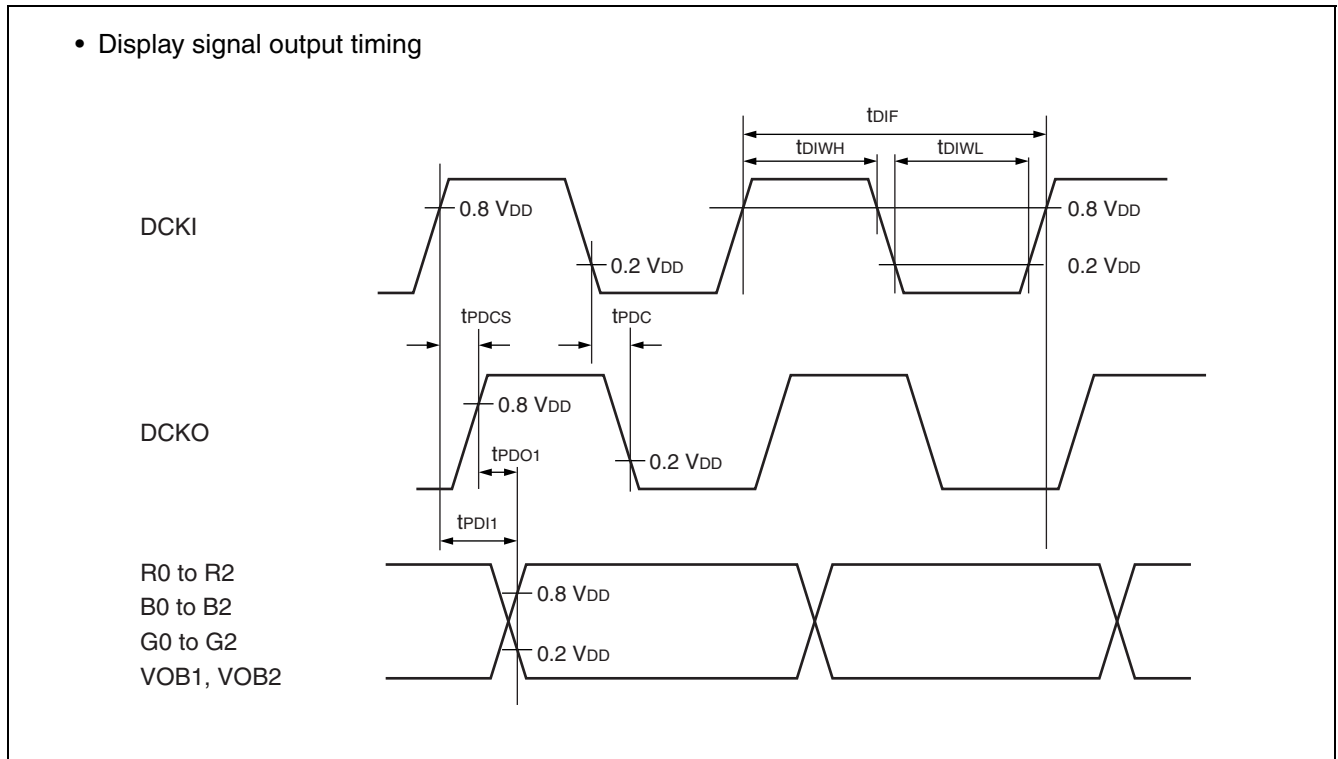
( $T_a = -10\text{ }^{\circ}\text{C}$  to  $+70\text{ }^{\circ}\text{C}$ ,  $V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{DDI} = 2.5\text{ V} \pm 0.2\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Pin	Value		Unit	Remarks
			Min	Max		
Dot clock cycle time	$t_{DIF}$	DCKI	11	90	MHz	*1
Dot clock pulse time	$t_{DIWH}$	DCKI	5	—	ns	*1
	$t_{DIWL}$		5	—	ns	
Dot clock output delay time 1	$t_{PDC}$	DCKO	3	8	ns	*2
Display signal output delay time I1	$t_{PDI1}$	R0 to R2, B0 to B2, G0 to G2, VOB1, VOB2	2	8	ns	*2
Display signal output delay time O1	$t_{PDO1}$	R0 to R2, B0 to B2, G0 to G2, VOB1, VOB2	-4	5	ns	*2

\*1 : Input a continuous dot clock signal without a break.

\*2 : Output load 16 pF

Note : The actual display output varies depending on how the display output/position is controlled for each display layer.



# MB91319 Series

## (10-a) External circuit for data slicer

( $T_a = -10\text{ }^\circ\text{C}$  to  $+70\text{ }^\circ\text{C}$ ,  $V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{DDI} = 2.5\text{ V} \pm 0.2\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

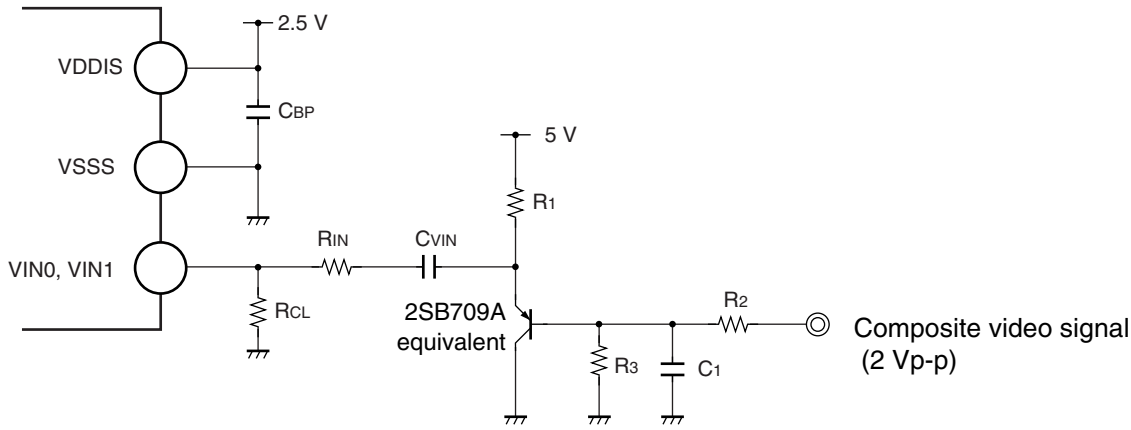
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Video signal input level	$V_{VIN}$	VIN0, VIN1	1.0	—	1.5	Vp-p	

## (10-b) External circuit for data slicer

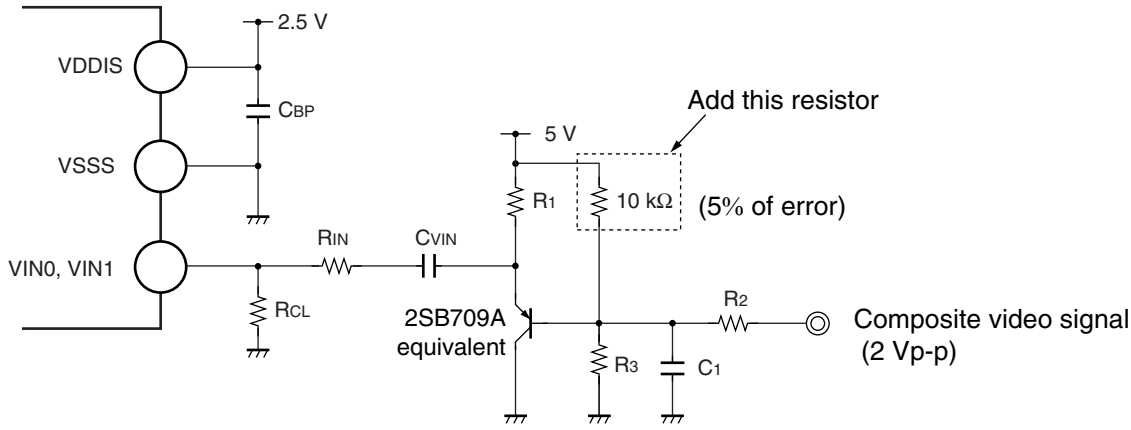
( $T_a = -10\text{ }^\circ\text{C}$  to  $+70\text{ }^\circ\text{C}$ ,  $V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{DDI} = 2.5\text{ V} \pm 0.2\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Coupling condenser for VIN pin	$C_{VIN}$	VIN0, VIN1	—	—	0.1	$\mu\text{F}$	More than B features 10% of error Ceramic condenser
Resistor for clamp	$R_{CL}$	VIN0, VIN1	—	—	1	$\text{M}\Omega$	5% of error
Input resistance for VIN pin	$R_{IN}$	VIN0, VIN1	—	—	0	$\Omega$	5% of error
Condenser of low pass filter for VIN	$C_1$	—	—	—	82	pF	More than B features 10% of error Ceramic condenser
Power supply bypass condenser	$C_{BP}$	VDDIS, VSSS	—	—	0.1	$\mu\text{F}$	Ceramic condenser
Resistance for video signal input buffer	$R_1$	—	—	—	2.2	$\text{k}\Omega$	5% of error
Video signal input level correcting resistor	$R_2$	—	—	—	4.7	$\text{k}\Omega$	5% of error
Video signal input level correcting resistor	$R_3$	—	—	10	12	$\text{k}\Omega$	5% of error

(1) When the input composite video signals have been DC clamped



(2) When the input composite video signals have not been DC clamped



External recommended circuit for data slicer

# MB91319 Series

## (11) I<sup>2</sup>C timing

- At master mode operating

(Ta = -10 °C to +70 °C, V<sub>DDE</sub> = 3.3 V ± 0.3 V, V<sub>DDI</sub> = 2.5 V ± 0.2 V, V<sub>SS</sub> = 0 V)

Parameter	Sym- bol	Conditions	Typical mode		High-speed mode*3		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	f <sub>SCL</sub>	R = 1 kΩ C = 50 pF*4	0	100	0	400	kHz	
“L” period of SCL clock	t <sub>LOW</sub>		4.7	—	1.3	—	μs	
“H” period of SCL clock	t <sub>HIGH</sub>		4.0	—	0.6	—	μs	
Bus free time between [STOP condition] and [START condition]	t <sub>BUS</sub>		4.7	—	1.3	—	μs	
SCL↓ → SDA output delay time	t <sub>DLDAT</sub>		—	5 × M*1	—	5 × M*1	ns	
Setup time of [repeat START condition] SCL↑ → SDA↓	t <sub>SUSTA</sub>		4.7	—	0.6	—	μs	
Hold time of [repeat START condition] SDA↓ → SCL↓	t <sub>HDSTA</sub>		4.0	—	0.6	—	μs	After that, the first clock pulse is generated.
Setup time of [STOP condition] SCL↑ → SDA↑	t <sub>SUSTO</sub>		4.0	—	0.6	—	μs	
SDA data input hold time (vs. SCL↓)	t <sub>HDDAT</sub>		2 × M*1	—	2 × M*1	—	μs	
SDA data input setup time (vs. SCL↑)	t <sub>SUDAT</sub>		250	—	100*2	—	ns	

\*1 : M = Resource clock cycle (ns)

\*2 : A Fast-mode I<sup>2</sup>C bus device can be used for a standard mode I<sup>2</sup>C bus system as long as the device satisfies a requirement of “t<sub>SUDAT</sub> ≥ 250 ns”.

When the device does not extend the “L” period of the SCL signal, the next data must be outputted to the SDA line within 1250 ns (maximum SDA/SCL rise time + t<sub>SUDAT</sub>) in which the SCL line is released.

\*3 : For use at over 100 kHz, set the resource clock to at least 6 MHz.

\*4 : R and C represent the pull-up resistor and load capacitor of the SCL and SDA output lines.

- At slave mode operating

( $T_a = -10\text{ }^\circ\text{C}$  to  $+70\text{ }^\circ\text{C}$ ,  $V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{DDI} = 2.5\text{ V} \pm 0.2\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Conditions	Typical mode		High-speed mode*3		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	$f_{SCL}$	R = 1 k $\Omega$ C = 50 pF*4	0	100	0	400	kHz	
“L” period of SCL clock	$t_{LOW}$		4.7	—	1.3	—	$\mu\text{s}$	
“H” period of SCL clock	$t_{HIGH}$		4.0	—	0.6	—	$\mu\text{s}$	
SCL $\downarrow$ $\rightarrow$ SDA output delay time	$t_{DL DAT}$		—	$5 \times M^{*1}$	—	$5 \times M^{*1}$	ns	
Bus free time between [STOP condition and START condition]	$t_{BUS}$		4.7	—	1.3	—	$\mu\text{s}$	
SDA data input hold time (vs. SCL $\downarrow$ )	$t_{HDDAT}$		$2 \times M^{*1}$	—	$2 \times M^{*1}$	—	$\mu\text{s}$	
SDA data input setup time (vs. SCL $\uparrow$ )	$t_{SUDAT}$		250	—	$100^{*2}$	—	ns	
Setup time of [repeat START condition] SCL $\uparrow$ $\rightarrow$ SDA $\downarrow$	$t_{SUSTA}$		4.7	—	0.6	—	$\mu\text{s}$	
Hold time of [repeat START condition] SDA $\downarrow$ $\rightarrow$ SCL $\downarrow$	$t_{HDSTA}$		4.0	—	0.6	—	$\mu\text{s}$	After that, the first clock pulse is generated.
Setup time of [STOP condition] SCL $\uparrow$ $\rightarrow$ SDA $\uparrow$	$t_{SUSTO}$		4.0	—	0.6	—	$\mu\text{s}$	

\*1 : M = Resource clock cycle (ns)

\*2 : A Fast-mode I<sup>2</sup>C bus device can be used for a standard mode I<sup>2</sup>C bus system as long as the device satisfies a requirement of “ $t_{SUDAT} \geq 250\text{ ns}$ ”.

When the device does not extend the “L” period of the SCL signal, the next data must be outputted to the SDA line within 1250 ns (maximum SDA/SCL rise time +  $t_{SUDAT}$ ) in which the SCL line is released.

\*3 : For use at over 100 kHz, set the resource clock to at least 6 MHz.

\*4 : R and C represent the pull-up resistor and load capacitor of the SCL and SDA output lines.

# MB91319 Series

## 5. 0.25 μm Technology About the Power-on Sequence for Dual-power-supply Models

- The power supplies must be turned on in the VDDI → AVCC, AVRH, VDDE order and off in the VDDE → AVCC, AVRH, VDDI order.

## 6. Electrical Characteristics for the A/D Converter

( $T_a = -10\text{ }^{\circ}\text{C}$  to  $+70\text{ }^{\circ}\text{C}$ ,  $V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{DDI} = 2.5\text{ V} \pm 0.2\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  
 $V_{SSE} = V_{SSI} = AV_{SS} = 0\text{ V}$ ,  $AVRH = 3.0\text{ V}$  to  $3.6\text{ V}$ )

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Resolution	—	—	10	bit	
Total error*1	- 5.5	—	+ 5.5	LSB	AV <sub>CC</sub> = 3.3 V, AVRH = 3.3 V (at CPU sleep)
Nonlinear error*1	- 3.5	—	+ 3.5	LSB	
Differential linear error*1	- 2.0	—	+ 2.0	LSB	
Zero transition voltage*1	- 4.0	—	+ 6.0	LSB	
Full transition voltage*1	AVRH - 5.5	—	AVRH + 3.0	LSB	
Conversion time	10*2	—	—	μs	
Power supply voltage (analog + digital)	—	3.6	—	mA	
	—	—	5	μA	At stop converting
Reference power supply current (between AVRH and AVRL)	—	470	—	μA	AVRH = 3.0 V, AVRL = 0.0 V
	—	—	10	μA	At stop converting
Analog input capacitance	—	40	—	pF	
Interchannel disparity	—	—	4	LSB	

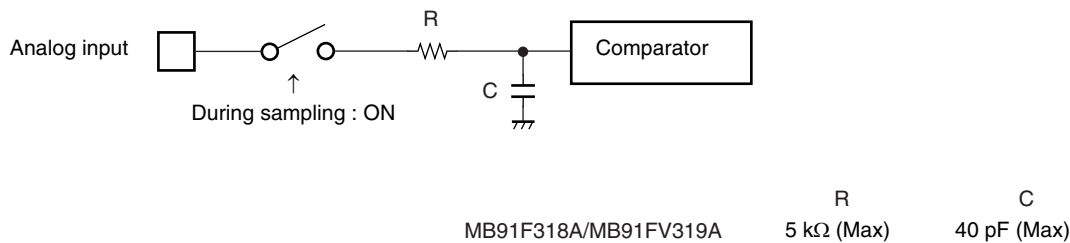
\*1 : Measured in the CPU sleep state

\*2 : Depends on the clock cycle of the clock signal supplied to peripheral resources.

## • About the external impedance of the analog input and its sampling time

- A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sampling and hold capacitor is insufficient, adversely affecting A/D conversion precision.

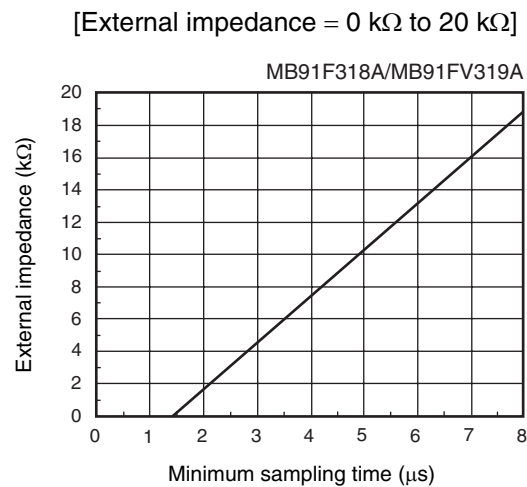
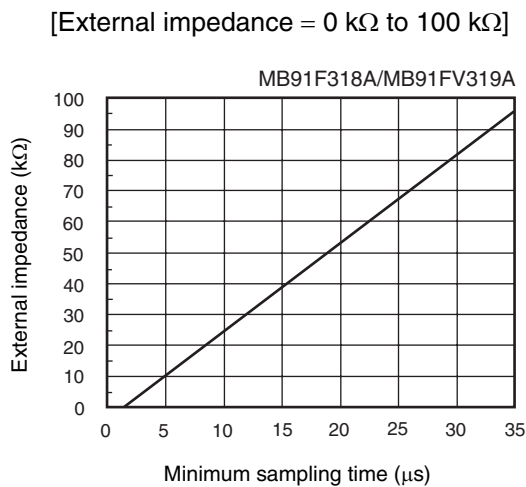
### • Analog input circuit model



Note : The values are reference values.

- To satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the resistor value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value.

### • The relationship between the external impedance and minimum sampling time



- If the sampling time cannot be sufficient, connect a capacitor of about 0.1 μF to the analog input pin.

## • About errors

- As  $|AVRH - AV_{SS}|$  becomes smaller, values of relative errors grow larger.

# MB91319 Series

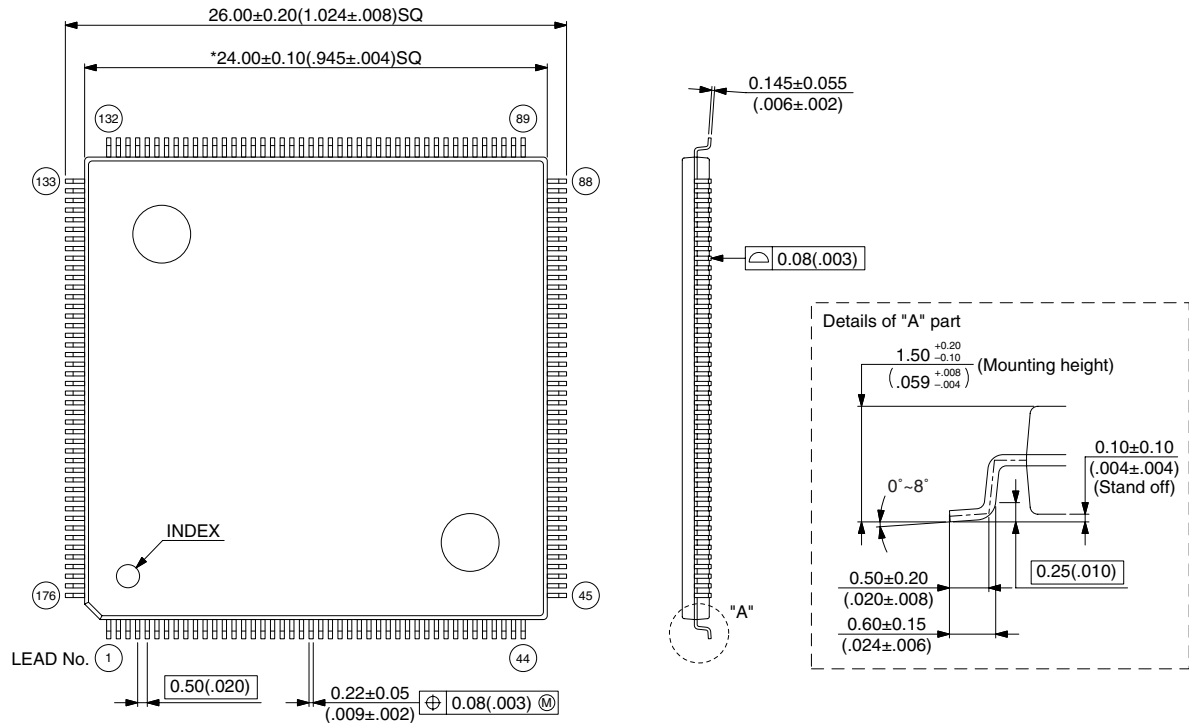
## ■ ORDERING INFORMATION

Part number	Package	Remarks
MB91FV319APMT-ES	176-pin plastic LQFP (FPT-176P-M07)	For developing tool

## ■ PACKAGE DIMENSION

176-pin plastic LQFP  
(FPT-176P-M07)

- Note 1) \* : Values do not include resin protrusion.  
Resin protrusion is +0.25 (.010) Max (each side) .  
Note 2) Pins width and pins thickness include plating thickness  
Note 3) Pins width do not include tie bar cutting remainder.



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Dimensions in mm (inches) .

Note : The values in parentheses are reference values.

**MEMO**



**MEMO**



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