

# 32-bit Microcontroller

CMOS

## FR60 MB91460H Series

### MB91F464HB

#### ■ DESCRIPTION

MB91460H series is a line of general-purpose 32-bit RISC microcontrollers designed for embedded control applications which require high-speed real-time processing, such as consumer devices and on-board vehicle systems. This series uses the FR60 CPU, which is compatible with the FR family\* of CPUs.

This series contains the LIN-USART and CAN controllers.

\* : FR, the abbreviation of FUJITSU RISC controller, is a line of products of FUJITSU Microelectronics Limited.

#### ■ FEATURES

##### 1. FR60 CPU core

- 32-bit RISC, load/store architecture, five-stage pipeline
- 16-bit fixed-length instructions (basic instructions)
- Instruction execution speed: 1 instruction per cycle
- Instructions including memory-to-memory transfer, bit manipulation, and barrel shift instructions: Instructions suitable for embedded applications
- Function entry/exit instructions and register data multi-load store instructions : Instructions supporting C language
- Register interlock function: Facilitating assembly-language coding
- Built-in multiplier with instruction-level support
  - Signed 32-bit multiplication: 5 cycles
  - Signed 16-bit multiplication: 3 cycles
- Interrupts (save PC/PS) : 6 cycles (16 priority levels)
- Harvard architecture enabling program access and data access to be performed simultaneously
- Instructions compatible with the FR family

For the information for microcontroller supports, see the following web site.

This web site includes the "**Customer Design Review Supplement**" which provides the latest cautions on system development and the minimal requirements to be checked to prevent problems before the system development.

<http://edevic.fujitsu.com/micom/en-support/>

## 2. Internal peripheral resources

- General-purpose ports : Maximum 108 ports
- DMAC (DMA Controller)
  - Maximum of 5 channels able to operate simultaneously
  - 2 transfer sources (internal peripheral/software)
  - Activation source can be selected using software
  - Addressing mode specifies full 32-bit addresses (increment/decrement/fixed)
  - Transfer mode (demand transfer/burst transfer/step transfer/block transfer)
  - Transfer data size selectable from 8/16/32-bit
  - Multi-byte transfer enabled (by software)
  - DMAC descriptor in I/O areas (200<sub>H</sub> to 240<sub>H</sub>, 1000<sub>H</sub> to 1024<sub>H</sub>)
- A/D converter (successive approximation type)
  - 10-bit resolution: maximum 32 channels
  - Conversion time: minimum 1  $\mu$ s
- External interrupt inputs : maximum 16 channels
  - 3 channels shared with CAN RX or I<sup>2</sup>C pins
- Bit search module (for REALOS)
  - Function to search the first bit position of "1", "0", "changed" from the MSB (most significant bit) within one word
- LIN-USART (full duplex double buffer): 4 or 7 channels
  - Clock synchronous/asynchronous selectable
  - Sync-break detection
  - Internal dedicated baud rate generator
- I<sup>2</sup>C bus interface (supports 400 kbps): 2 channels
  - Master/slave transmission and reception
  - Arbitration function, clock synchronization function
- CAN controller (C-CAN): 1 channel
  - Maximum transfer speed: 1 Mbps
  - 32 transmission/reception message buffers
- Sound generator : 1 channel
  - Tone frequency : PWM frequency divide-by-two (reload value + 1)
- Alarm comparator : 1 channel
  - Monitor external voltage
  - Generate an interrupt in case of voltage lower/higher than the defined thresholds (reference voltage)
- 16-bit PPG timer : maximum 16 channels
- 16-bit reload timer: 8 channels
- 16-bit free-run timer: 8 channels (1 channel each for ICU and OCU)
- Input capture: maximum 8 channels (operates in conjunction with the free-run timer)
- Output compare: maximum 8 channels (operates in conjunction with the free-run timer)
- Up/Down counter: 2 channels (2\*8-bit or 1\*16-bit)
- Watchdog timer
- Real-time clock
- Low-power consumption modes : Sleep/stop mode function
- Low voltage detection circuit

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*(Continued)*

- Clock supervisor  
Monitors the sub-clock (32 kHz) and the main clock (4 MHz) , and switches to a recovery clock (CR oscillator, etc.) when the oscillations stop.
- Clock modulator
- Clock monitor
- Sub-clock calibration  
Corrects the real-time clock timer when operating with the 32 kHz or CR oscillator
- Main oscillator stabilization timer  
Generates an interrupt in sub-clock mode after the stabilization wait time has elapsed on the 23-bit stabilization wait time counter
- Sub-oscillator stabilization timer  
Generates an interrupt in main clock mode after the stabilization wait time has elapsed on the 15-bit stabilization wait time counter

### **3. Package and technology**

- Package : QFP-144
- CMOS 180 nm technology
- Power supply range 3 V to 5 V (1.8 V internal logic provided by a step-down voltage converter)
- Operating temperature range: between - 40°C and + 105°C

# MB91460H Series

## ■ PRODUCT LINEUP

Feature	MB91FV460B	MB91F464HB
Max. core frequency (CLKB)	100 MHz	100 MHz
Max. resource frequency (CLKP)	50 MHz	50 MHz
Max. external bus frequency (CLKT)	50 MHz	50 MHz
Max. CAN frequency (CLKCAN)	50 MHz	50 MHz
Technology	0.18μm	0.18μm
Watchdog	yes	yes
Watchdog (RC osc. based)	yes (disengageable)	yes
Bit Search	yes	yes
Reset input (INITX)	yes	yes
Clock Modulator	yes	yes
Clock Monitor	yes	yes
Low Power Mode	yes	yes
DMA	5 ch	5 ch
MMU/MPU	MPU (16 ch) <sup>1)</sup>	MPU (8 ch) <sup>1)</sup>
Flash memory	Internal Flash memory 2112KB + external emulation SRAM with 64bit read data	416 KByte
Flash Protection	yes	yes
D-RAM	64 KByte	24 KByte
ID-RAM	64 KByte	16 KByte
Flash-Cache (Instruction cache)	16 KByte	8 KByte
Boot-ROM / BI-ROM	16 KByte Boot Flash + 1KB Boot ROM	4 KByte
RTC	1 ch	1 ch
Free Running Timer	12 ch	8 ch <sup>2)</sup>
ICU	10 ch	MD_3=0: 8 ch MD_3=1: 4 ch <sup>3)</sup>
OCU	8 ch	MD_3=0: 8 ch MD_3=1: 4 ch <sup>4)</sup>
Reload Timer	16 ch	8 ch <sup>5)</sup>
PPG 16-bit	32 ch	MD_3=0: 16 ch MD_3=1: 8 ch <sup>6)</sup>
Sound Generator	1 ch (old) + 1 ch (new)	1 ch (old)
Up/Down Counter (8/16 bit)	4 ch (8-bit) / 2 ch (16-bit)	MD_3=0: 2 ch (8-bit) / 1 ch (16bit) MD_3=1: NA <sup>7)</sup>
C_CAN	6 ch (128msg)	1 ch (32msg)
LIN-USART	16 ch (FIFO)	MD_3=0: 3 ch + 4 ch FIFO <sup>8)</sup> MD_3=1: 4 ch FIFO
°C (400K)	8 ch	2 ch
FR external bus	yes (32bit addr, 32bit data)	MD_3=0: no MD_3=1: yes (22bit addr, 16bit data)

# MB91460H Series

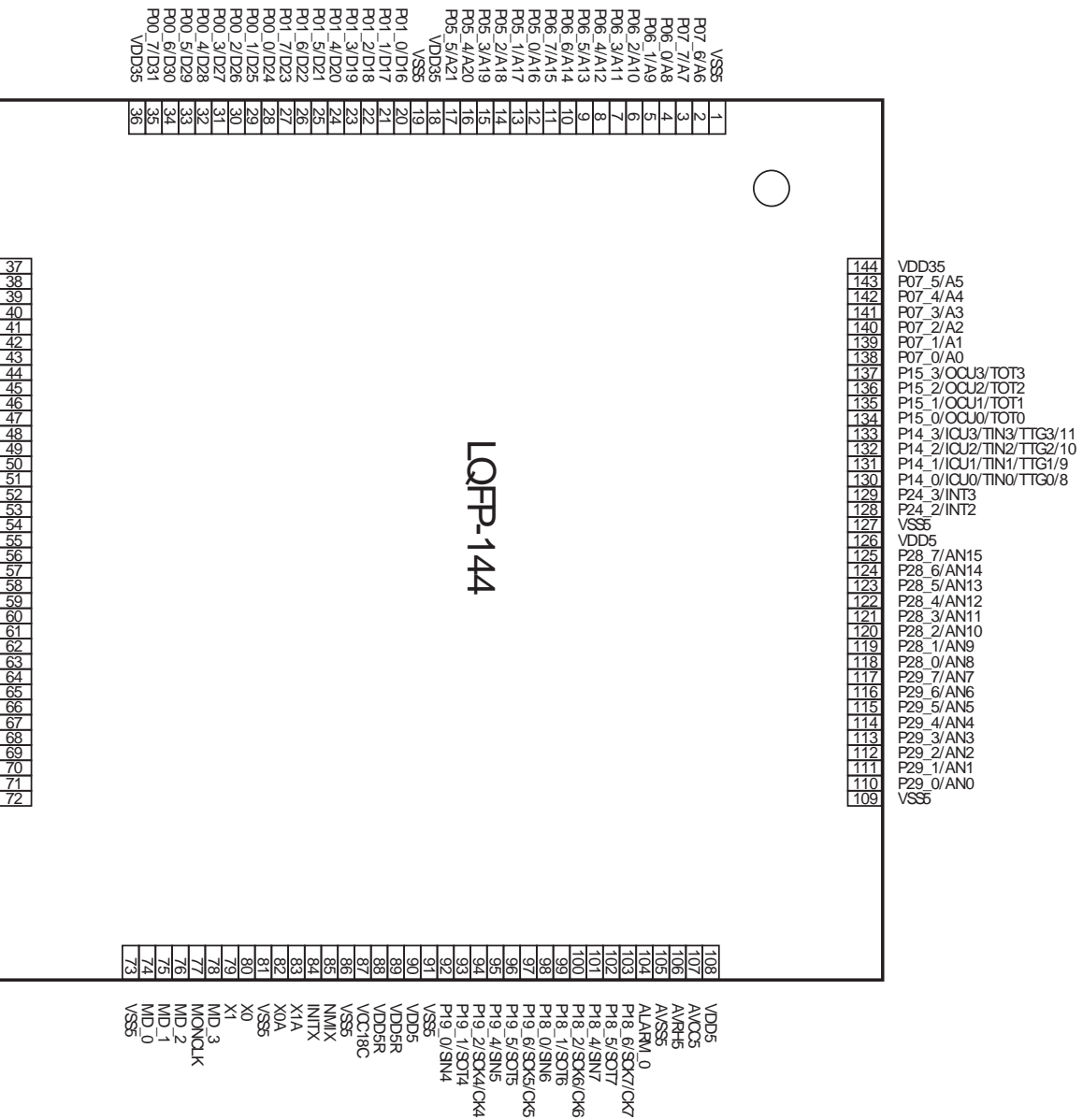
Feature	MB91FV460B	MB91F464HB
External Interrupts	32 ch	MD_3=0: 16 ch MD_3=1: 12 ch <sup>9</sup>
NMI Interrupts	1 ch	1 ch
ADC (10-bit)	32 ch + 22 ch	MD_3=0: 32 ch MD_3=1: 16 ch
Alarm Comparator	2 ch	1 ch
Supply Supervisor (low voltage detection)	yes	yes
Clock Supervisor	yes	yes
Main clock oscillator	4 MHz	4 MHz
Sub clock oscillator	32kHz	32kHz
RC oscillator	100kHz / 2MHz	100kHz / 2MHz
PLL	x 25	x 25
DSU4	yes	no
EDSU	yes (32 BP) <sup>1</sup>	yes (16 BP) <sup>1</sup>
Supply voltage	1.8V + 3V/5V	3V/5V
Regulator	no	yes
Power consumption	1.5 W	< 1 W
Temperature Range (Ta)	0..70 C	-40..105 C
Package	BGA-896	QFP-144
Power on to PLL run	< 20 ms	< 20 ms
Flash Download Time	< 8 sec. typical	< 5 sec. typical

# MB91460H Series

## ■ PIN ASSIGNMENT

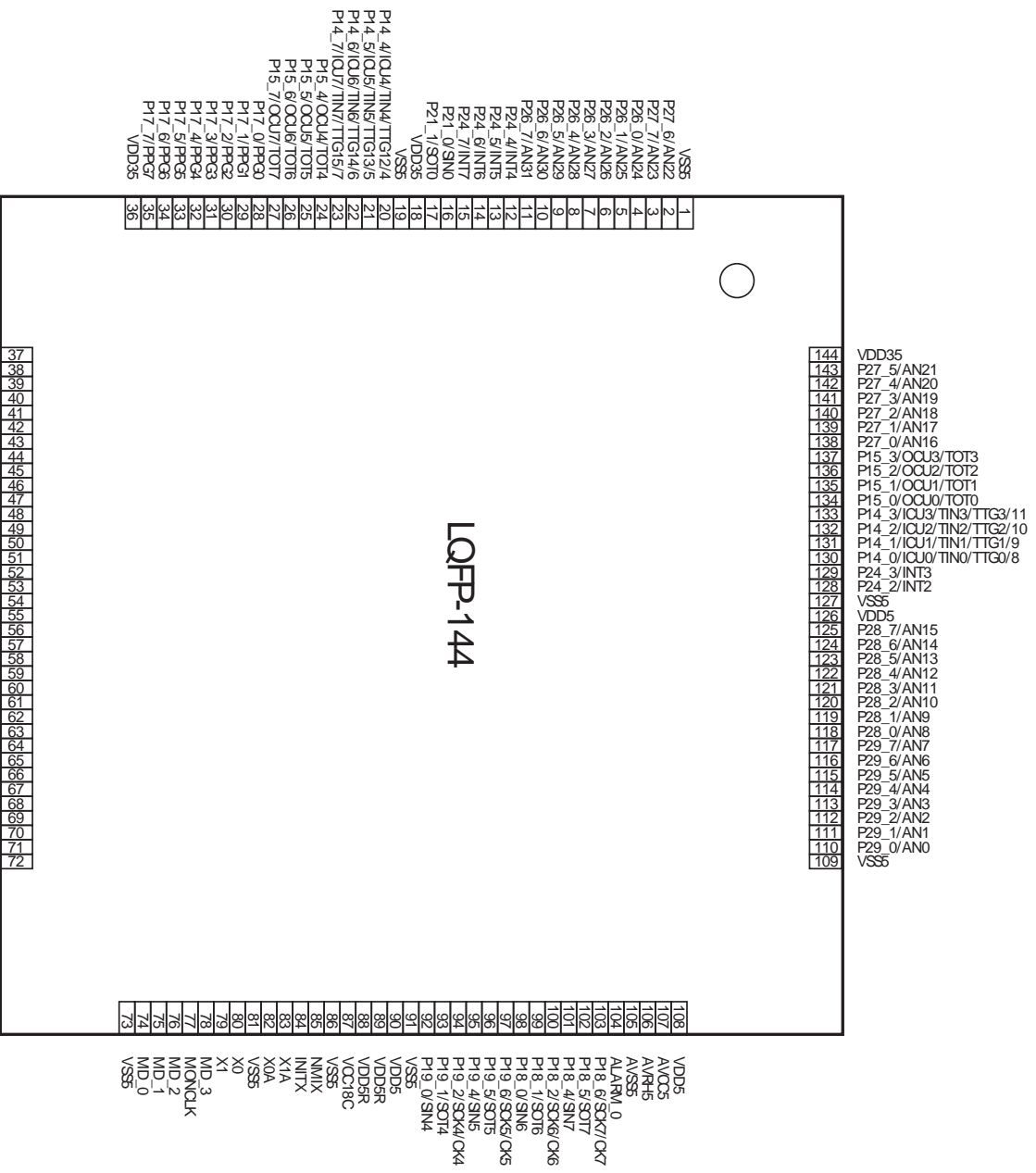
### 1. MB91F464HB with MD\_3=1

(TOP VIEW)



## 2. MB91F46HB with MD\_3=0

(TOP VIEW)



# MB91460H Series

## ■ PIN DESCRIPTION

### 1. MB91F464HB with MD\_3=1

Pin no.	Pin name	I/O	I/O circuit type*	Function
2, 3	P07_6, P07_7	I/O	B	General-purpose input/output port
	A6, A7			Signal pins of external address bus (bit6 to bit7)
4 to 11	P06_0 to P06_7	I/O	B	General-purpose input/output port
	A8 to A15			Signal pins of external address bus (bit8 to bit15)
12 to 17	P05_0 to P05_5	I/O	A	General-purpose input/output port
	A16 to A21			Signal pins of external address bus (bit16 to bit21)
20 to 27	P01_0 to P01_7	I/O	A	General-purpose input/output port
	D16 to D23			Signal pins of external data bus (bit16 to bit23)
28 to 35	P00_0 to P00_7	I/O	A	General-purpose input/output port
	D24 to D31			Signal pins of external data bus (bit24 to bit31)
38	P10_0	I/O	A	General-purpose input/output port
	SYSCLOCK			External bus clock output pin
39	P09_0	I/O	A	General-purpose input/output port
	CSX0			Chip select output pins
40	P09_1	I/O	A	General-purpose input/output port
	CSX1			Chip select output pins
41	P08_0	I/O	A	General-purpose input/output port
	WRX0			External write strobe output pins
42	P08_4	I/O	A	General-purpose input/output port
	RDX			External read strobe output pin
43	P08_7	I/O	A	General-purpose input/output port
	RDY			External ready input pin
44	P08_1	I/O	A	General-purpose input/output port
	WRX1			External write strobe output pins
	INT0			External interrupt input, can only be used in general-purpose IO port mode
45	P24_1	I/O	A	General-purpose input/output port
	INT1			External interrupt input pins
46	P23_0	I/O	A	General-purpose input/output port
	RX0			RX input pin of CAN0
	INT8			External interrupt input pins
47	P23_1	I/O	A	General-purpose input/output port
	TX0			TX output pin of CAN0

# MB91460H Series

Pin no.	Pin name	I/O	I/O circuit type*	Function
48	P23_2	I/O	A	General-purpose input/output port
	INT9			External interrupt input pins
49	P23_3	I/O	A	General-purpose input/output port
50	P23_4	I/O	A	General-purpose input/output port
	INT10			External interrupt input pin
51	P23_5	I/O	A	General-purpose input/output port
52	P23_6	I/O	A	General-purpose input/output port
	INT11			External interrupt input pin
53	P23_7	I/O	A	General-purpose input/output port
56	P22_0	I/O	A	General-purpose input/output port
	INT12			External interrupt input pin
57	P22_1	I/O	A	General-purpose input/output port
58	P22_2	I/O	A	General-purpose input/output port
	INT13			External interrupt input pin
59	P22_3	I/O	A	General-purpose input/output port
60	P22_4	I/O	C	General-purpose input/output port
	SDA0			I <sup>2</sup> C bus DATA input/output pin (open drain)
	INT14			External interrupt input pin
61	P22_5	I/O	C	General-purpose input/output port
	SCL0			I <sup>2</sup> C bus clock input/output pin (open drain)
62	P22_6	I/O	C	General-purpose input/output port
	SDA1			I <sup>2</sup> C bus DATA input/output pin (open drain)
	INT15			External interrupt input pin
63	P22_7	I/O	C	General-purpose input/output port
	SCL1			I <sup>2</sup> C bus clock input/output pin (open drain)
64	P16_0	I/O	A	General-purpose input/output port
	PPG8			Output pins of PPG timer
65	P16_1	I/O	A	General-purpose input/output port
	PPG9			Output pins of PPG timer
66	P16_2	I/O	A	General-purpose input/output port
	PPG10			Output pins of PPG timer
67	P16_3	I/O	A	General-purpose input/output port
	PPG11			Output pins of PPG timer
68	P16_4	I/O	A	General-purpose input/output port
	PPG12			Output pins of PPG timer
	SGA			SGA output pin of sound generator

# MB91460H Series

Pin no.	Pin name	I/O	I/O circuit type*	Function
69	P16_5	I/O	A	General-purpose input/output port
	PPG13			Output pins of PPG timer
	SGO			SGO output pin of sound generator
70	P16_6	I/O	A	General-purpose input/output port
	PPG14			Output pins of PPG timer
71	P16_7	I/O	A	General-purpose input/output port
	PPG15			Output pins of PPG timer
	ATGX			A/D converter external trigger input pin
74 to 76	MD_0 to MD_2	I	G	Mode setting pins
77	MONCLK	O	M	Clock monitor pin
78	MD_3	I	H	Mode setting pin
79	X1	—	J1	Clock (oscillation) output
80	X0	—	J1	Clock (oscillation) input
82	X0A	—	J2	Sub clock (oscillation) input
83	X1A	—	J2	Sub clock (oscillation) output
84	INITX	I	H	External reset input pin
85	NMIX	I	H	Non-maskable interrupt input pin
92	P19_0	I/O	A	General-purpose input/output port
	SIN4			Data input pin of USART4
93	P19_1	I/O	A	General-purpose input/output port
	SOT4			Data output pin of USART4
94	P19_2	I/O	A	General-purpose input/output port
	SCK4			Clock input/output pin of USART4
	CK4			External clock input pin of free-run timer 4
95	P19_4	I/O	A	General-purpose input/output port
	SIN5			Data input pin of USART5
96	P19_5	I/O	A	General-purpose input/output port
	SOT5			Data output pin of USART5
97	P19_6	I/O	A	General-purpose input/output port
	SCK5			Clock input/output pin of USART5
	CK5			External clock input pin of free-run timer 5
98	P18_0	I/O	A	General-purpose input/output port
	SIN6			Data input pin of USART6
99	P18_1	I/O	A	General-purpose input/output port
	SOT6			Data output pin of USART6

# MB91460H Series

Pin no.	Pin name	I/O	I/O circuit type*	Function
100	P18_2	I/O	A	General-purpose input/output port
	SCK6			Clock input/output pin of USART6
	CK6			External clock input pin of free-run timer 6
101	P18_4	I/O	A	General-purpose input/output port
	SIN7			Data input pin of USART7
102	P18_5	I/O	A	General-purpose input/output port
	SOT7			Data output pin of USART7
103	P18_6	I/O	A	General-purpose input/output port
	SCK7			Clock input/output pin of USART7
	CK7			External clock input pin of free-run timer 7
104	ALARM_0	I	N	Alarm comparator input pin
110 to 117	P29_0 to P29_7	I/O	B	General-purpose input/output port
	AN0 to AN7			Analog input pins of A/D converter
118 to 125	P28_0 to P28_7	I/O	B	General-purpose input/output port
	AN8 to AN15			Analog input pins of A/D converter
128	P24_2	I/O	A	General-purpose input/output port
	INT2			External interrupt input pin
129	P24_3	I/O	A	General-purpose input/output port
	INT3			External interrupt input pin
130 to 133	P14_0 to P14_3	I/O	A	General-purpose input/output port
	ICU0 to ICU3			Input capture input pins
	TIN0 to TIN3			External trigger input pins of reload timer
	TTG0/8 to TTG3/11			External trigger input pins of PPG timer
134 to 137	P15_0 to P15_3	I/O	A	General-purpose input/output port
	OCU0 to OCU3			Output compare output pins
	TOT0 to TOT3			Reload timer output pins
138 to 143	P07_0 to P07_5	I/O	B	General-purpose input/output port
	A0 to A5			Signal pins of external address bus (bit0 to bit5)

# MB91460H Series

## [Power supply/Ground pins]

Pin no.	Pin name	I/O	Function
1, 19, 37, 55, 73, 81, 86, 91, 109, 127	VSS5	Supply	Ground pins
54, 72, 90, 108, 126	VDD5		Power supply pins
88, 89	VDD5R		Power supply pins for internal regulator
105	AVSS5		Analog ground pin for A/D converter
107	AVCC5		Power supply pin for A/D converter
106	AVRH5		Reference power supply pin for A/D converter
87	VCC18C		Capacitor connection pin for internal regulator
18, 36, 144	VDD35		Power supply pins for external bus part of I/O ring

## 2. MB91F464HB with MD\_3=0

Pin no.	Pin name	I/O	I/O circuit type*	Function
2 to 3	P27_6 to P27_7	I/O	B	General-purpose input/output ports
	AN22 to AN23			Analog input pins of A/D converter
4 to 11	P26_0 to P26_7	I/O	B	General-purpose input/output ports
	AN24 to AN31			Analog input pins of A/D converter
12 to 15	P24_4 to P24_7	I/O	A	General-purpose input/output ports
	INT4 to INT7			External interrupt input pins
16	P21_0	I/O	A	General-purpose input/output ports
	SIN0			Data input pin of USART0
17	P21_1	I/O	A	General-purpose input/output ports
	SOT0			Data output pin of USART0
20 to 23	P14_4 to P14_7	I/O	A	General-purpose input/output ports
	ICU4 to ICU7			Input capture input pins
	TIN4 to TIN7			External trigger input pins of reload timer
	TTG4/12 to TTG7/15			External trigger input pins of PPG timer
24 to 27	P15_4 to P15_7	I/O	A	General-purpose input/output ports
	OCU4 to OCU7			Output compare output pins
	TOT4 to TOT7			Reload timer output pins
28 to 35	P17_0 to P17_7	I/O	A	General-purpose input/output ports
	PPG0 to PPG7			Output pins of PPG timer
38	P20_0	I/O	A	General-purpose input/output ports
	SIN2			Data input pin of USART2
	AIN0			Up/down counter input pin
39	P20_1	I/O	A	General-purpose input/output ports
	SOT2			Data output pin of USART2
	BIN0			Up/down counter input pin
40	P20_2	I/O	A	General-purpose input/output ports
	SCK2			Clock input/output pin of USART2
	ZIN0			Up/down counter input pin
	CK2			External clock input pin of free-run timer 2
41	P20_4	I/O	A	General-purpose input/output ports
	SIN3			Data input pin of USART3
	AIN1			Up/down counter input pin
42	P20_5	I/O	A	General-purpose input/output ports
	SOT3			Data output pin of USART3
	BIN1			Up/down counter input pin

# MB91460H Series

Pin no.	Pin name	I/O	I/O circuit type*	Function
43	P20_6	I/O	A	General-purpose input/output ports
	SCK3			Clock input/output pin of USART3
	ZIN1			Up/down counter input pin
	CK3			External clock input pin of free-run timer 3
44	P24_0	I/O	A	General-purpose input/output ports
	INT0			External interrupt input pin
45	P24_1	I/O	A	General-purpose input/output ports
	INT1			External interrupt input pin
46	P23_0	I/O	A	General-purpose input/output port
	RX0			RX input pin of CAN0
	INT8			External interrupt input pins
47	P23_1	I/O	A	General-purpose input/output port
	TX0			TX output pin of CAN0
48	P23_2	I/O	A	General-purpose input/output port
	INT9			External interrupt input pins
49	P23_3	I/O	A	General-purpose input/output port
50	P23_4	I/O	A	General-purpose input/output port
	INT10			External interrupt input pin
51	P23_5	I/O	A	General-purpose input/output port
52	P23_6	I/O	A	General-purpose input/output port
	INT11			External interrupt input pin
53	P23_7	I/O	A	General-purpose input/output port
56	P22_0	I/O	A	General-purpose input/output port
	INT12			External interrupt input pin
57	P22_1	I/O	A	General-purpose input/output port
58	P22_2	I/O	A	General-purpose input/output port
	INT13			External interrupt input pin
59	P22_3	I/O	A	General-purpose input/output port
60	P22_4	I/O	C	General-purpose input/output ports
	SDA0			I <sup>2</sup> C bus DATA input/output pin (open drain)
	INT14			External interrupt input pin
61	P22_5	I/O	C	General-purpose input/output ports
	SCL0			I <sup>2</sup> C bus clock input/output pin (open drain)
62	P22_6	I/O	C	General-purpose input/output ports
	SDA1			I <sup>2</sup> C bus DATA input/output pin (open drain)
	INT15			External interrupt input pin

# MB91460H Series

Pin no.	Pin name	I/O	I/O circuit type*	Function
63	P22_7	I/O	C	General-purpose input/output ports
	SCL1			I <sup>2</sup> C bus clock input/output pin (open drain)
64 to 67	P16_0 to P16_3	I/O	A	General-purpose input/output ports
	PPG8 to PPG11			Output pins of PPG timer
68	P16_4	I/O	A	General-purpose input/output ports
	PPG12			Output pins of PPG timer
	SGA			SGA output pin of sound generator
69	P16_5	I/O	A	General-purpose input/output ports
	PPG13			Output pins of PPG timer
	SGO			SGO output pin of sound generator
70	P16_6	I/O	A	General-purpose input/output ports
	PPG14			Output pins of PPG timer
71	P16_7	I/O	A	General-purpose input/output ports
	PPG15			Output pins of PPG timer
	ATGX			A/D converter external trigger input pin
74 to 76	MD_0 to MD_2	I	G	Mode setting pins
77	MONCLK	O	M	Clock monitor pin
78	MD_3	I	H	Mode setting pins
79	X1	—	J1	Clock (oscillation) output
80	X0	—	J1	Clock (oscillation) input
82	X0A	—	J2	Sub clock (oscillation) input
83	X1A	—	J2	Sub clock (oscillation) output
84	INITX	I	H	External reset input pin
85	NMIX	I	H	Non-maskable interrupt input pin
92	P19_0	I/O	A	General-purpose input/output ports
	SIN4			Data input pin of USART4
93	P19_1	I/O	A	General-purpose input/output ports
	SOT4			Data output pin of USART4
94	P19_2	I/O	A	General-purpose input/output ports
	SCK4			Clock input/output pin of USART4
	CK4			External clock input pin of free-run timer 4
95	P19_4	I/O	A	General-purpose input/output ports
	SIN5			Data input pin of USART5
96	P19_5	I/O	A	General-purpose input/output ports
	SOT5			Data output pin of USART5

# MB91460H Series

Pin no.	Pin name	I/O	I/O circuit type*	Function
97	P19_6	I/O	A	General-purpose input/output ports
	SCK5			Clock input/output pin of USART5
	CK5			External clock input pin of free-run timer 5
98	P18_0	I/O	A	General-purpose input/output ports
	SIN6			Data input pin of USART6
99	P18_1	I/O	A	General-purpose input/output ports
	SOT6			Data output pin of USART6
100	P18_2	I/O	A	General-purpose input/output ports
	SCK6			Clock input/output pin of USART6
	CK6			External clock input pin of free-run timer 6
101	P18_4	I/O	A	General-purpose input/output ports
	SIN7			Data input pin of USART7
102	P18_5	I/O	A	General-purpose input/output ports
	SOT7			Data output pin of USART7
103	P18_6	I/O	A	General-purpose input/output ports
	SCK7			Clock input/output pin of USART7
	CK7			External clock input pin of free-run timer 7
104	ALARM_0	I	N	Alarm comparator input pin
110 to 117	P29_0 to P29_7	I/O	B	General-purpose input/output ports
	AN0 to AN7			Analog input pins of A/D converter
118 to 125	P28_0 to P28_7	I/O	B	General-purpose input/output ports
	AN8 to AN15			Analog input pins of A/D converter
128	P24_2	I/O	A	General-purpose input/output ports
	INT2			External interrupt input pin
129	P24_3	I/O	A	General-purpose input/output ports
	INT3			External interrupt input pin
130 to 133	P14_0 to P14_3	I/O	A	General-purpose input/output ports
	ICU0 to ICU3			Input capture input pins
	TIN0 to TIN3			External trigger input pins of reload timer
	TTG0/8 to TTG3/11			External trigger input pins of PPG timer
134 to 137	P15_0 to P15_3	I/O	A	General-purpose input/output ports
	OCU0 to OCU3			Output compare output pins
	TOT0 to TOT3			Reload timer output pins
138 to 143	P27_0 to P27_5	I/O	B	General-purpose input/output ports
	AN16 to AN21			Analog input pins of A/D converter

\* : For information about the I/O circuit type, refer to “■ I/O CIRCUIT TYPES”.

**[Power supply/Ground pins]**

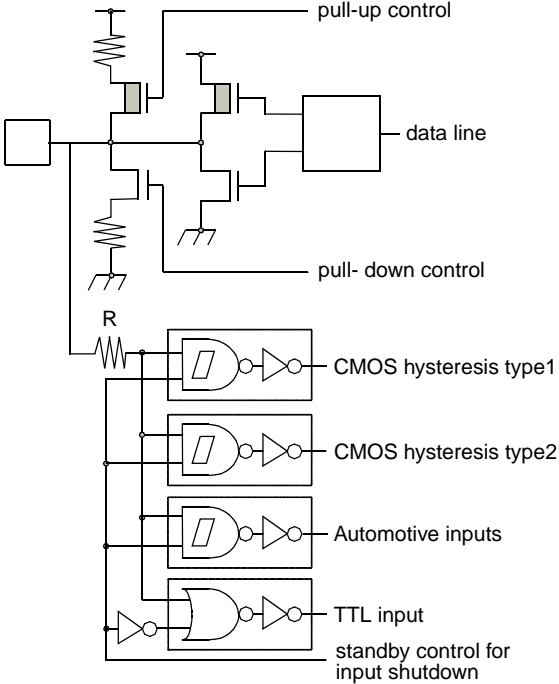
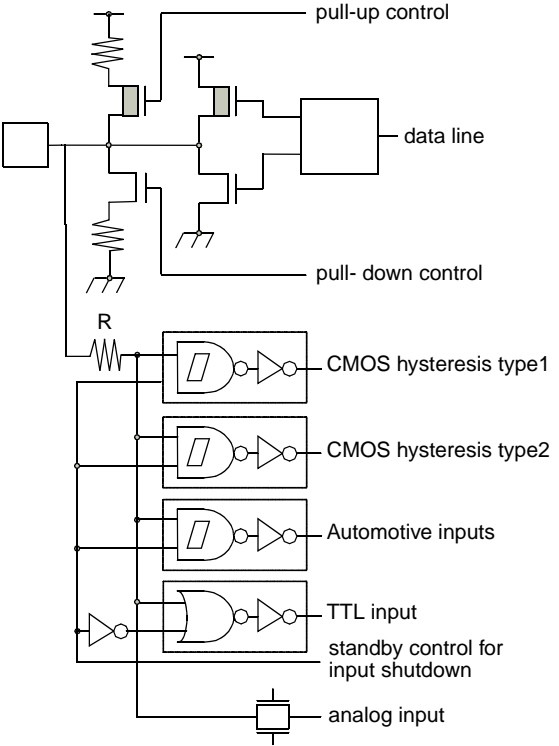
Pin no.	Pin name	I/O	Function
1, 19, 37, 55, 73, 81, 86, 91, 109, 127	VSS5	Supply	Ground pins
54, 72, 90, 108, 126	VDD5		Power supply pins
88, 89	VDD5R		Power supply pins for internal regulator
105	AVSS5		Analog ground pin for A/D converter
107	AVCC5		Power supply pin for A/D converter
106	AVRH5		Reference power supply pin for A/D converter
87	VCC18C		Capacitor connection pin for internal regulator
18, 36, 144	VDD35		Power supply pins for external bus part of I/O ring

\* : For information about the I/O circuit type, refer to “■ I/O CIRCUIT TYPES”.

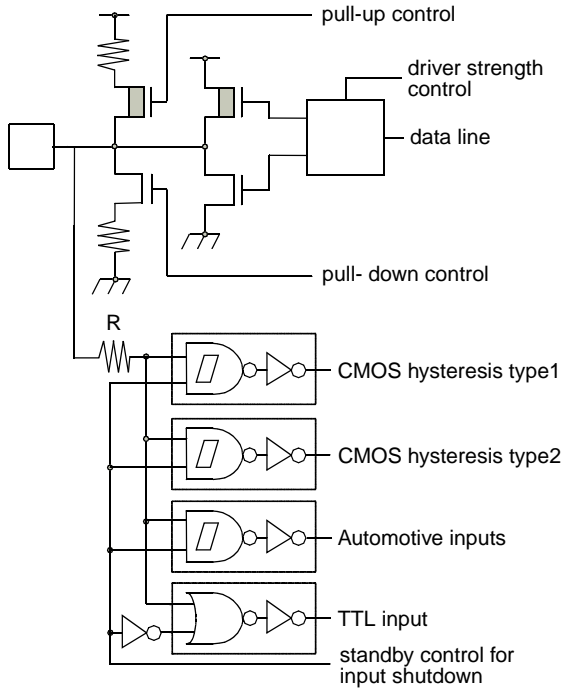
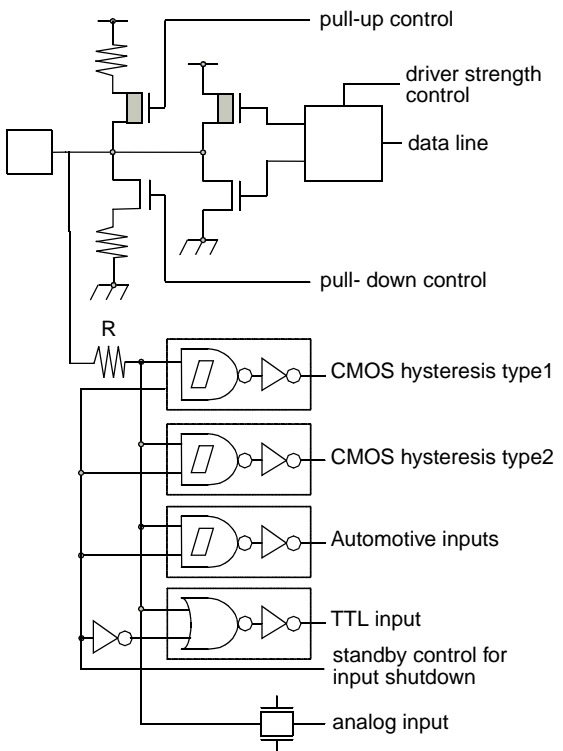
# MB91460H Series

## I/O CIRCUIT TYPES

Type	Circuit	Remarks
A	<p>pull-up control</p> <p>driver strength control</p> <p>data line</p> <p>pull-down control</p> <p>R</p> <p>CMOS hysteresis type1</p> <p>CMOS hysteresis type2</p> <p>Automotive inputs</p> <p>TTL input</p> <p>standby control for input shutdown</p>	<p>CMOS level output (programmable <math>I_{OL} = 5\text{mA}</math>, <math>I_{OH} = -5\text{mA}</math> and <math>I_{OL} = 2\text{mA}</math>, <math>I_{OH} = -2\text{mA}</math>)</p> <p>2 different CMOS hysteresis inputs with input shutdown function</p> <p>Automotive input with input shutdown function</p> <p>TTL input with input shutdown function</p> <p>Programmable pull-up resistor: 50k<math>\Omega</math> approx.</p>
B	<p>pull-up control</p> <p>driver strength control</p> <p>data line</p> <p>pull-down control</p> <p>R</p> <p>CMOS hysteresis type1</p> <p>CMOS hysteresis type2</p> <p>Automotive inputs</p> <p>TTL input</p> <p>standby control for input shutdown</p> <p>analog input</p>	<p>CMOS level output (programmable <math>I_{OL} = 5\text{mA}</math>, <math>I_{OH} = -5\text{mA}</math> and <math>I_{OL} = 2\text{mA}</math>, <math>I_{OH} = -2\text{mA}</math>)</p> <p>2 different CMOS hysteresis inputs with input shutdown function</p> <p>Automotive input with input shutdown function</p> <p>TTL input with input shutdown function</p> <p>Programmable pull-up resistor: 50k<math>\Omega</math> approx.</p> <p>Analog input</p>

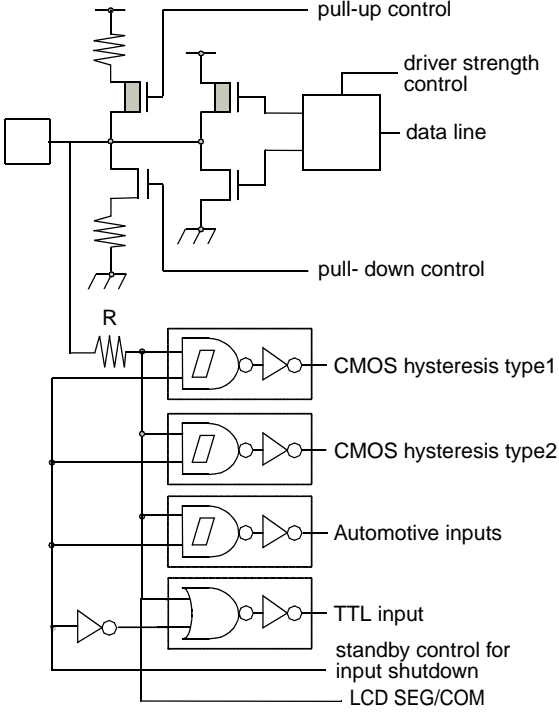
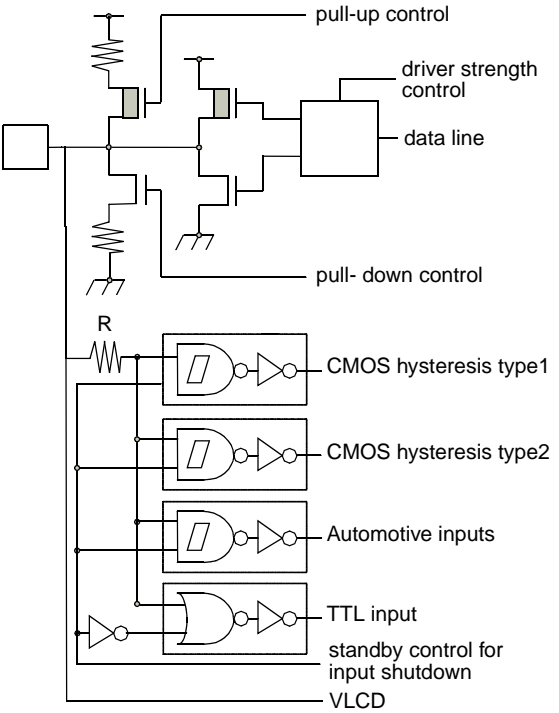
Type	Circuit	Remarks
C	 <p>The diagram for Type C shows a pull-up/pull-down control circuit. It includes a pull-up control line connected to a resistor and a pull-down control line connected to ground. A data line is connected to the output of a CMOS buffer. A resistor R is connected to the input of the buffer. The input is connected to four different input types: CMOS hysteresis type1, CMOS hysteresis type2, Automotive inputs, and TTL input. A standby control for input shutdown is also shown.</p>	<p>CMOS level output (<math>I_{OL} = 3mA</math>, <math>I_{OH} = -3mA</math>)                  2 different CMOS hysteresis inputs with input shutdown function                  Automotive input with input shutdown function                  TTL input with input shutdown function                  Programmable pull-up resistor: 50kΩ approx.</p>
D	 <p>The diagram for Type D is similar to Type C, but it includes an additional analog input connected to the input of the buffer through a resistor.</p>	<p>CMOS level output (<math>I_{OL} = 3mA</math>, <math>I_{OH} = -3mA</math>)                  2 different CMOS hysteresis inputs with input shutdown function                  Automotive input with input shutdown function                  TTL input with input shutdown function                  Programmable pull-up resistor: 50kΩ approx.                  Analog input</p>

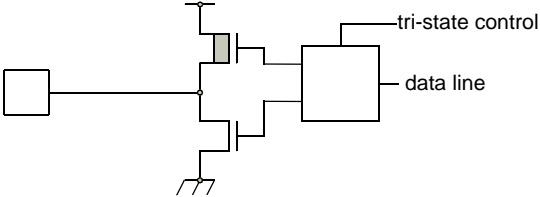
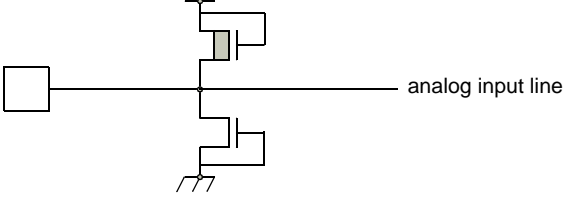
# MB91460H Series

Type	Circuit	Remarks
E	 <p>pull-up control</p> <p>driver strength control</p> <p>data line</p> <p>pull-down control</p> <p>R</p> <p>CMOS hysteresis type1</p> <p>CMOS hysteresis type2</p> <p>Automotive inputs</p> <p>TTL input</p> <p>standby control for input shutdown</p>	<p>CMOS level output            (programmable <math>I_{OL} = 5\text{mA}</math>, <math>I_{OH} = -5\text{mA}</math>            and <math>I_{OL} = 2\text{mA}</math>, <math>I_{OH} = -2\text{mA}</math>,            and <math>I_{OL} = 30\text{mA}</math>, <math>I_{OH} = -30\text{mA}</math>)</p> <p>2 different CMOS hysteresis inputs with input shutdown function</p> <p>Automotive input with input shutdown function</p> <p>TTL input with input shutdown function</p> <p>Programmable pull-up resistor: 50k<math>\Omega</math> approx.</p>
F	 <p>pull-up control</p> <p>driver strength control</p> <p>data line</p> <p>pull-down control</p> <p>R</p> <p>CMOS hysteresis type1</p> <p>CMOS hysteresis type2</p> <p>Automotive inputs</p> <p>TTL input</p> <p>standby control for input shutdown</p> <p>analog input</p>	<p>CMOS level output            (programmable <math>I_{OL} = 5\text{mA}</math>, <math>I_{OH} = -5\text{mA}</math>            and <math>I_{OL} = 2\text{mA}</math>, <math>I_{OH} = -2\text{mA}</math>,            and <math>I_{OL} = 30\text{mA}</math>, <math>I_{OH} = -30\text{mA}</math>)</p> <p>2 different CMOS hysteresis inputs with input shutdown function</p> <p>Automotive input with input shutdown function</p> <p>TTL input with input shutdown function</p> <p>Programmable pull-up resistor: 50k<math>\Omega</math> approx.</p> <p>Analog input</p>

Type	Circuit	Remarks
G		Mask ROM and EVA device: CMOS Hysteresis input pin Flash device: CMOS input pin 12 V withstand (for MD [2:0])
H		CMOS Hysteresis input pin Pull-up resistor value: 50 kΩ approx.
J1		High-speed oscillation circuit: <ul style="list-style-type: none"> <li>• Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin)</li> <li>• Feedback resistor = approx. <math>2 * 0.5 \text{ M}\Omega</math>. Feedback resistor is grounded in the center when the oscillator is disabled or in FCI mode.</li> </ul>
J2		Low-speed oscillation circuit: <ul style="list-style-type: none"> <li>• Feedback resistor = approx. <math>2 * 5 \text{ M}\Omega</math>. Feedback resistor is grounded in the center when the oscillator is disabled.</li> </ul>

# MB91460H Series

Type	Circuit	Remarks
K	 <p>pull-up control</p> <p>driver strength control</p> <p>data line</p> <p>pull-down control</p> <p>R</p> <p>CMOS hysteresis type1</p> <p>CMOS hysteresis type2</p> <p>Automotive inputs</p> <p>TTL input</p> <p>standby control for input shutdown</p> <p>LCD SEG/COM</p>	<p>CMOS level output (programmable <math>I_{OL} = 5\text{mA}</math>, <math>I_{OH} = -5\text{mA}</math> and <math>I_{OL} = 2\text{mA}</math>, <math>I_{OH} = -2\text{mA}</math>)</p> <p>2 different CMOS hysteresis inputs with input shutdown function</p> <p>Automotive input with input shutdown function</p> <p>TTL input with input shutdown function</p> <p>Programmable pull-up resistor: 50kΩ approx.</p> <p>LCD SEG/COM output</p>
L	 <p>pull-up control</p> <p>driver strength control</p> <p>data line</p> <p>pull-down control</p> <p>R</p> <p>CMOS hysteresis type1</p> <p>CMOS hysteresis type2</p> <p>Automotive inputs</p> <p>TTL input</p> <p>standby control for input shutdown</p> <p>VLCD</p>	<p>CMOS level output (programmable <math>I_{OL} = 5\text{mA}</math>, <math>I_{OH} = -5\text{mA}</math> and <math>I_{OL} = 2\text{mA}</math>, <math>I_{OH} = -2\text{mA}</math>)</p> <p>2 different CMOS hysteresis inputs with input shutdown function</p> <p>Automotive input with input shutdown function)</p> <p>TTL input with input shutdown function</p> <p>Programmable pull-up resistor: 50kΩ approx.</p> <p>Analog input</p> <p>LCD Voltage input</p>

Type	Circuit	Remarks
M		<p>CMOS level tri-state output (<math>I_{OL} = 5\text{mA}</math>, <math>I_{OH} = -5\text{mA}</math>)</p>
N		<p>Analog input pin with protection</p>

## ■ HANDLING DEVICES

### 1. Preventing Latch-up

Latch-up may occur in a CMOS IC if a voltage higher than ( $V_{DD5}$ ,  $V_{DD35}$  or  $HV_{DD5}$  \*) or less than ( $V_{SS5}$  or  $HV_{SS5}$  \*) is applied to an input or output pin or if a voltage exceeding the rating is applied between the power supply pins and ground pins. If latch-up occurs, the power supply current increases rapidly, sometimes resulting in thermal breakdown of the device. Therefore, be very careful not to apply voltages in excess of the absolute maximum ratings.

Note \*1:  $HV_{DD5}$ ,  $HV_{SS5}$  are available only on devices having Stepper Motor Controller.

### 2. Handling of unused input pins

If unused input pins are left open, abnormal operation may result. Any unused input pins should be connected to pull-up or pull-down resistor ( $2K\Omega$  to  $10K\Omega$ ) or enable internal pullup or pulldown resistors (PPER/PPCR) before the input enable (PORTEN) is activated by software. The mode pins MD\_x can be connected to  $V_{SS5}$  or  $V_{DD5}$  directly. Unused ALARM input pins can be connected to  $AV_{SS5}$  directly.

### 3. Power supply pins

In MB91460 series, devices including multiple power supply pins and ground pins are designed as follows; pins necessary to be at the same potential are interconnected internally to prevent malfunctions such as latch-up. All of the power supply pins and ground pins must be externally connected to the power supply and ground respectively in order to reduce unnecessary radiation, to prevent strobe signal malfunctions due to the ground level rising and to follow the total output current ratings. Furthermore, the power supply pins and ground pins of the MB91460 series must be connected to the current supply source via a low impedance.

It is also recommended to connect a ceramic capacitor of approximately  $0.1 \mu\text{F}$  as a bypass capacitor between power supply pin and ground pin near this device.

This series has a built-in step-down regulator. Connect a bypass capacitor of  $4.7 \mu\text{F}$  (use a X7R ceramic capacitor) to VCC18C pin for the regulator.

### 4. Crystal oscillator circuit

Noise in proximity to the X0 (X0A) and X1 (X1A) pins can cause the device to operate abnormally. Printed circuit boards should be designed so that the X0 (X0A) and X1 (X1A) pins, and crystal oscillator, as well as bypass capacitors connected to ground, are located near the device and ground.

It is recommended that the printed circuit board layout be designed such that the X0 and X1 pins or X0A and X1A pins are surrounded by ground plane for the stable operation.

Please request the oscillator manufacturer to evaluate the oscillational characteristics of the crystal and this device.

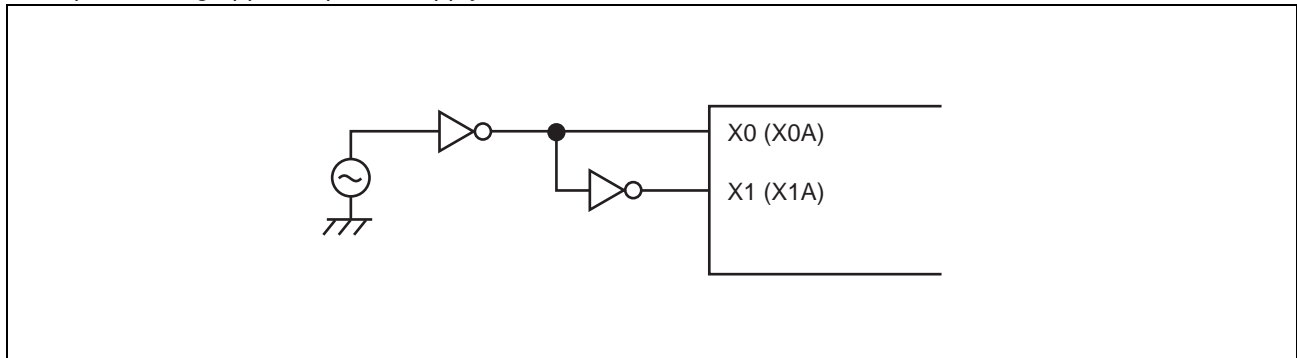
### 5. Notes on using external clock

When using the external clock, it is necessary to simultaneously supply the X0 (X0A) and the X1 (X1A) pins. In the described combination, X1 (X1A) should be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins. At X0 and X1, a frequency up to 16 MHz is possible.

*(Continued)*

(Continued)

Example of using opposite phase supply



## 6. Mode pins (MD\_x)

These pins should be connected directly to the power supply or ground pins. To prevent the device from entering test mode accidentally due to noise, minimize the lengths of the patterns between each mode pin and power supply pin or ground pin on the printed circuit board as possible and connect them with low impedance.

## 7. Notes on operating in PLL clock mode

If the oscillator is disconnected or the clock input stops when the PLL clock is selected, the microcontroller may continue to operate at the free-running frequency of the self-oscillating circuit of the PLL. However, this self-running operation cannot be guaranteed.

## 8. Pull-up control

The AC standard is not guaranteed in case a pull-up resistor is connected to the pin serving as an external bus pin.

## ■ NOTES ON DEBUGGER

### 1. Execution of the RETI Command

If single-step execution is used in an environment where an interrupt occurs frequently, the corresponding interrupt handling routine will be executed repeatedly to the exclusion of other processing. This will prevent the main routine and the handlers for low priority level interrupts from being executed (For example, if the time-base timer interrupt is enabled, stepping over the RETI instruction will always break on the first line of the time-base timer interrupt handler).

Disable the corresponding interrupts when the corresponding interrupt handling routine no longer needs debugging.

### 2. Break function

If the range of addresses that cause a hardware break (including event breaks) is set to the address of the current system stack pointer or to an area that contains the stack pointer, execution will break after each instruction regardless of whether the user program actually contains data access instructions.

To prevent this, do not set (word) access to the area containing the address of the system stack pointer as the target of the hardware break (including an event breaks).

### 3. Operand break

It may cause malfunctions if a stack pointer exists in the area which is set as the DSU operand break. Do not set the access to the areas containing the address of system stack pointer as a target of data event break.

### 4. Notes on PS register

As the PS register is processed in advance by some instructions, when the debugger is being used, the exception handling may result in execution breaking in an interrupt handling routine or the displayed values of the flags in the PS register being updated.

As the microcontroller is designed to carry out reprocessing correctly upon returning from such an EIT event, the operation before and after the EIT always proceeds according to specification.

- **The following behavior may occur if any of the following occurs in the instruction immediately after a DIV0U/DIV0S instruction:**

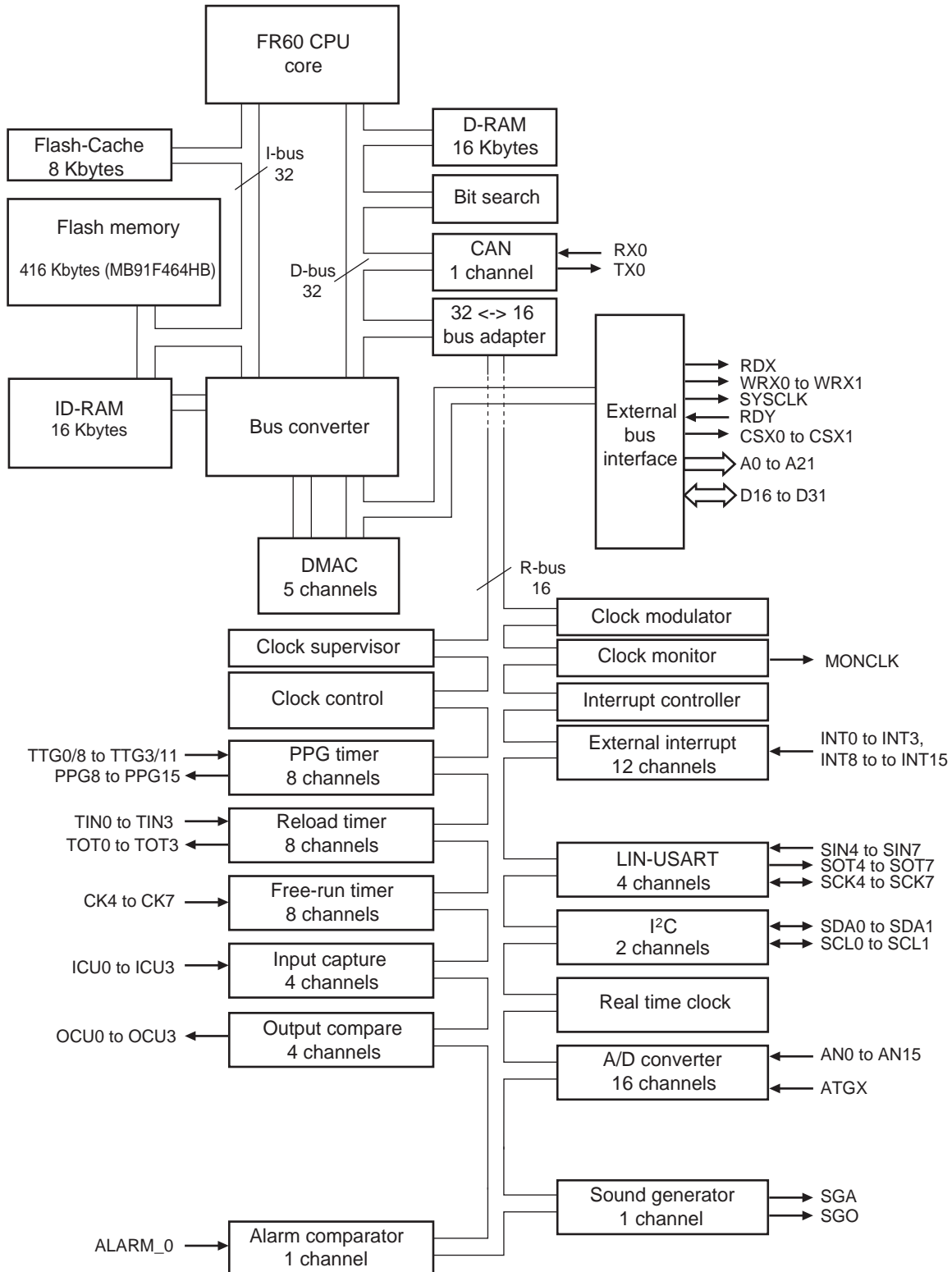
- (a) a user interrupt or NMI is accepted;
- (b) single-step execution is performed;
- (c) execution breaks due to a data event or from the emulator menu.
  1. D0 and D1 flags are updated in advance.
  2. An EIT handling routine (user interrupt/NMI or emulator) is executed.
  3. Upon returning from the EIT, the DIV0U/DIV0S instruction is executed and the D0 and D1 flags are updated to the same values as those in 1.

- **The following behavior occurs when an ORCCR, STILM, MOV Ri,PS instruction is executed to enable a user interrupt or NMI source while that interrupt is in the active state.**

1. The PS register is updated in advance.
2. An EIT handling routine (user interrupt/NMI or emulator) is executed.
3. Upon returning from the EIT, the above instructions are executed and the PS register is updated to the same value as in 1.

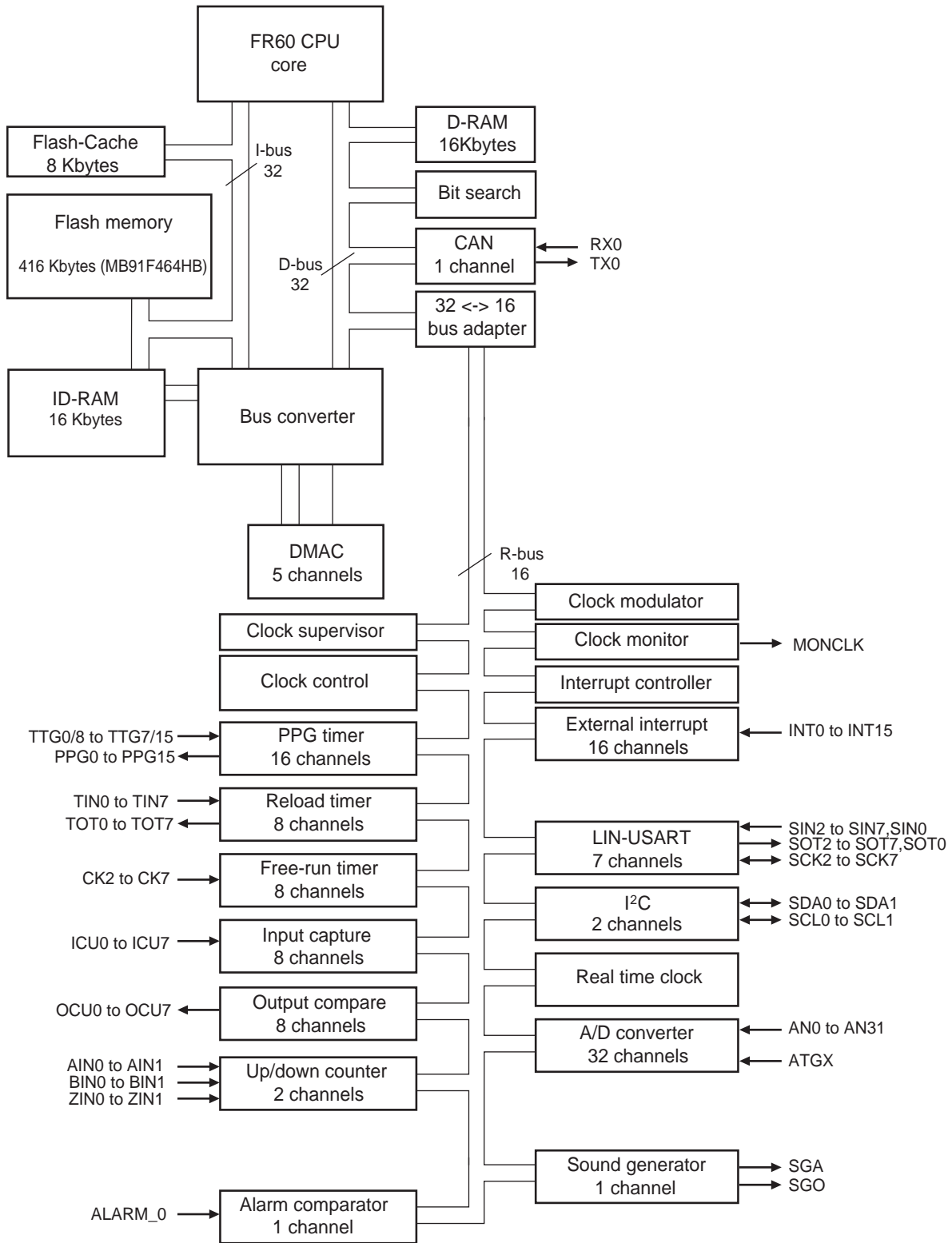
## ■ BLOCK DIAGRAM

### 1. MB91F464HB with MD\_3=1



# MB91460H Series

## 2. MB91F464HB with MD\_3=0



## ■ CPU AND CONTROL UNIT

The FR family CPU is a high performance core that is designed based on the RISC architecture with advanced instructions for embedded applications.

### 1. Features

- Adoption of RISC architecture  
Basic instruction: 1 instruction per cycle
- General-purpose registers: 32-bit × 16 registers
- 4 Gbytes linear memory space
- Multiplier installed  
32-bit × 32-bit multiplication: 5 cycles  
16-bit × 16-bit multiplication: 3 cycles
- Enhanced interrupt processing function  
Quick response speed (6 cycles)  
Multiple-interrupt support  
Level mask function (16 levels)
- Enhanced instructions for I/O operation  
Memory-to-memory transfer instruction  
Bit processing instruction  
Basic instruction word length: 16 bits
- Low-power consumption  
Sleep mode/stop mode

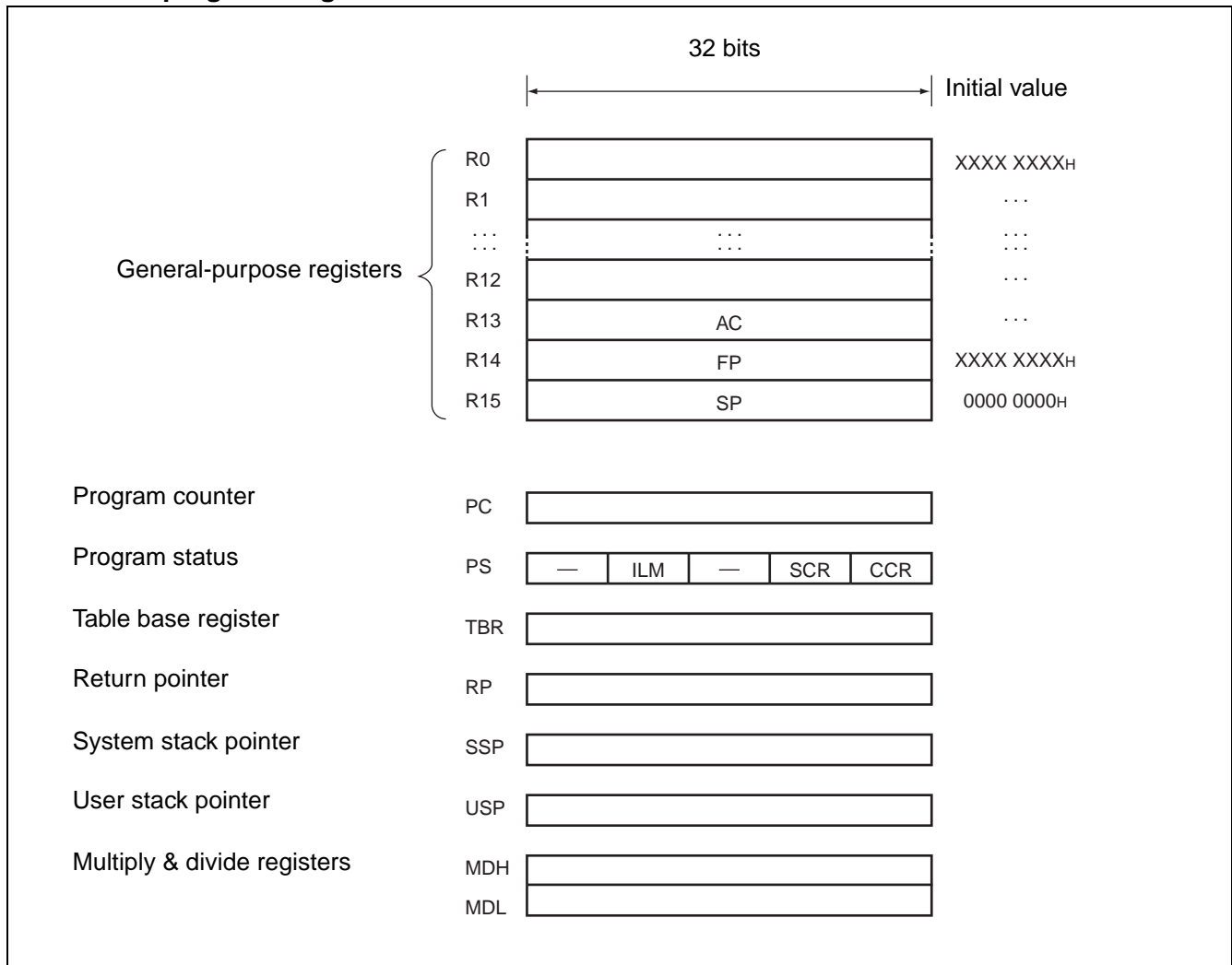
### 2. Internal architecture

- The FR family CPU uses the Harvard architecture in which the instruction bus and data bus are independent of each other.
- A 32-bit ↔ 16-bit buffer is connected to the 32-bit bus (D-bus) to provide an interface between the CPU and peripheral resources.
- A Harvard ↔ Princeton bus converter is connected to both the I-bus and D-bus to provide an interface between the CPU and the bus controller.

# MB91460H Series

## 3. Programming model

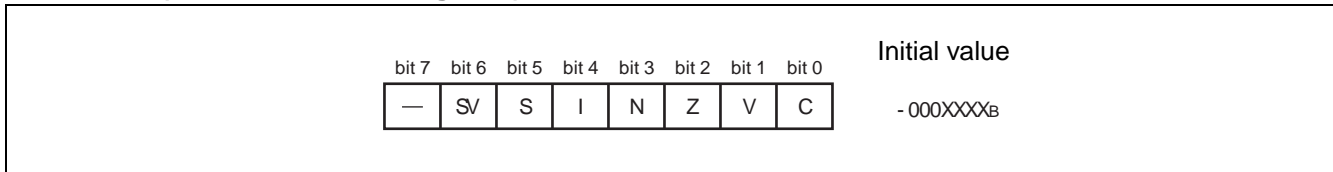
### 3.1. Basic programming model





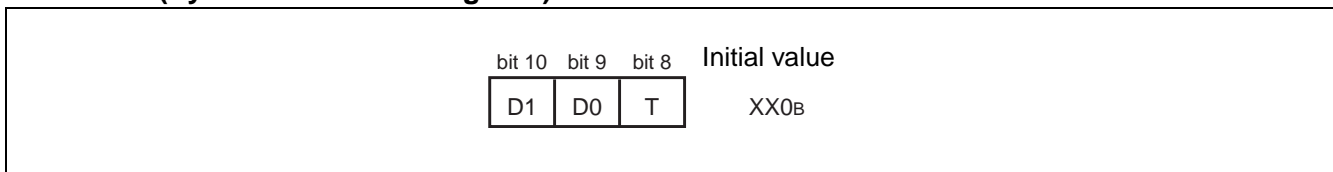
# MB91460H Series

## 4.3. CCR (Condition Code Register)



- SV : Supervisor flag
- S : Stack flag
- I : Interrupt enable flag
- N : Negative enable flag
- Z : Zero flag
- V : Overflow flag
- C : Carry flag

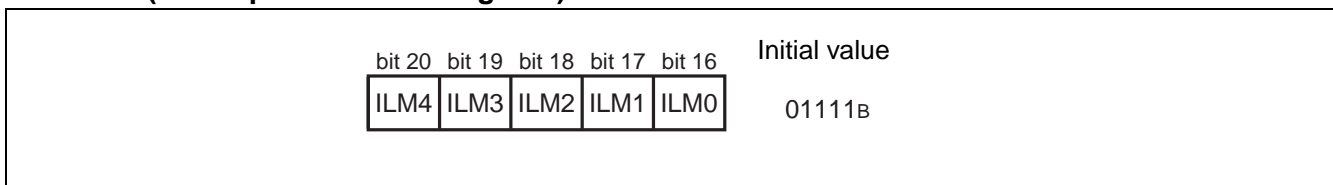
## 4.4. SCR (System Condition Register)



Flag for step division (D1, D0)  
This flag stores interim data during execution of step division.

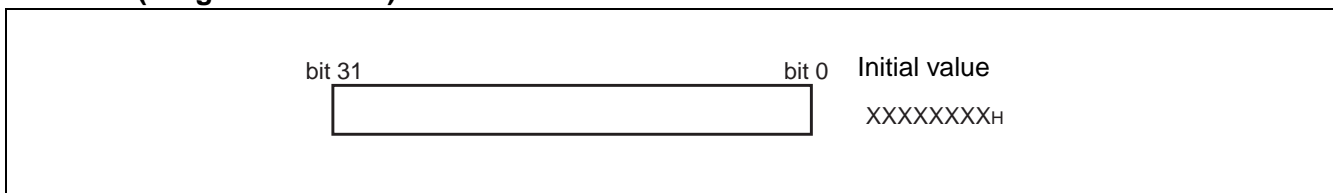
Step trace trap flag (T)  
This flag indicates whether the step trace trap is enabled or disabled.  
The step trace trap function is used by emulators. When an emulator is in use, it cannot be used in execution of user programs.

## 4.5. ILM (Interrupt Level Mask register)



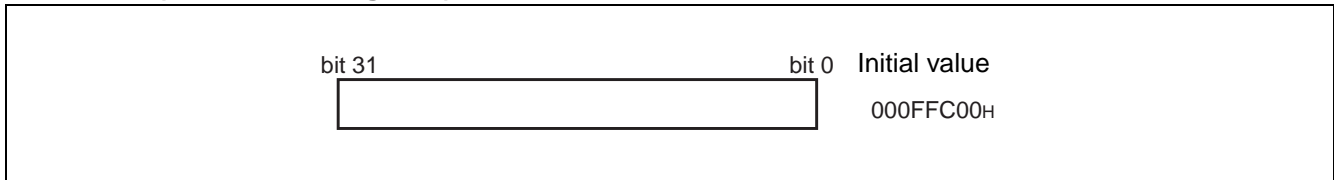
This register stores interrupt level mask values, and the values stored in ILM4 to ILM0 are used for level masking.  
The register is initialized to value “01111<sub>B</sub>” at reset.

## 4.6. PC (Program Counter)



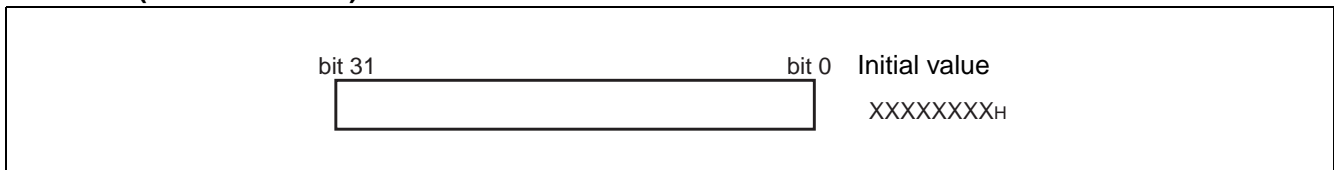
The program counter indicates the address of the instruction that is being executed.  
The initial value at reset is undefined.

## 4.7. TBR (Table Base Register)



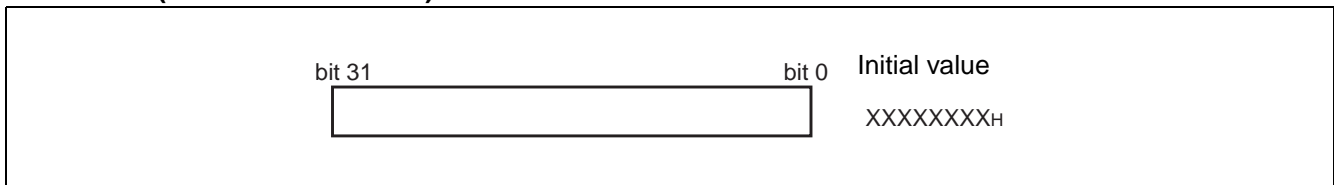
The table base register stores the starting address of the vector table used in EIT processing.  
The initial value at reset is 000FFC00H.

## 4.8. RP (Return Pointer)



The return pointer stores the address for return from subroutines.  
During execution of a CALL instruction, the PC value is transferred to this RP register.  
During execution of a RET instruction, the contents of the RP register are transferred to PC.  
The initial value at reset is undefined.

## 4.9. USP (User Stack Pointer)



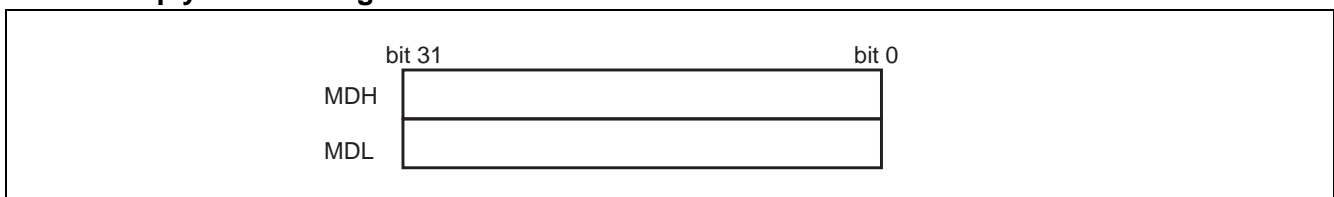
The user stack pointer, when the S flag is "1", this register functions as the R15 register.

- The USP register can also be explicitly specified.

The initial value at reset is undefined.

- This register cannot be used with RETI instructions.

## 4.10. Multiply & divide registers



These registers are for multiplication and division, and are each 32 bits in length.  
The initial value at reset is undefined.

## ■ EMBEDDED PROGRAM/DATA MEMORY (FLASH)

### 1. Flash features

- MB91F464HB : 416 Kbytes (6 × 64 Kbytes + 4 × 8 Kbytes = 3.25 Mbits)
- Programmable wait states for read/write access
- Flash and Boot security with security vector at 0x0014:8000 - 0x0014:800F
- Boot security
- Basic specification: Same as MBM29LV400TC (except size and part of sector configuration)

### 2. Operation modes:

#### (1) 32-bit CPU mode:

- CPU reads and executes programs in word (32-bit) length units.
- Actual Flash Memory access is performed in word (32-bit) length units.

#### (2) 16-bit CPU mode:

- CPU reads and writes in half-word (16-bit) length units.
- Program execution from the Flash is not possible.
- Actual Flash Memory access is performed in word (16-bit) length units.

#### (3) Flash memory mode (external access to Flash memory enabled)

Note: The operation mode of the flash memory can be selected using a Boot-ROM function. The function start address is 0xBF60. The parameter description is given in the Hardware Manual in chapter 54.6 "Flash Access Mode Switching".

## 3. Flash access in CPU mode

### 3.1. Flash configuration

#### 3.1.1. Flash memory map MB91F464HB

Address									
0014:FFFFh 0014:C000h	SA6 (8KB)				SA7 (8KB)				ROMS7
0014:BFFFh 0014:8000h	SA4 (8KB)				SA5 (8KB)				
0014:7FFFh 0014:4000h	SA2 (8KB)				SA3 (8KB)				
0014:3FFFh 0014:0000h	SA0 (8KB)				SA1 (8KB)				
0013:FFFFh 0012:0000h	SA22 (64KB)				SA23 (64KB)				ROMS6
0011:FFFFh 0010:0000h	SA20 (64KB)				SA21 (64KB)				
000F:FFFFh 000E:0000h	SA18 (64KB)				SA19 (64KB)				ROMS5
000D:FFFFh 000C:0000h	SA16 (64KB)				SA17 (64KB)				ROMS4
000B:FFFFh 000A:0000h	SA14 (64KB)				SA15 (64KB)				ROMS3
0009:FFFFh 0008:0000h	SA12 (64KB)				SA13 (64KB)				ROMS2
0007:FFFFh 0006:0000h	SA10 (64KB)				SA11 (64KB)				ROMS1
0005:FFFFh 0004:0000h	SA8 (64KB)				SA9 (64KB)				ROMS0
	addr+0	addr+1	addr+2	addr+3	addr+4	addr+5	addr+6	addr+7	
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
32bit read	dat[31:0]				dat[31:0]				
Legend	Memory not available in this area				Memory available in this area				

# MB91460H Series

## 3.2. Flash access timing settings in CPU mode

The following tables list all settings for a given maximum Core Frequency (through the setting of CLKB or maximum clock modulation) for Flash read and write access.

### 3.2.1. Flash read timing settings (synchronous read)

Core clock (CLKB)	ATD	ALEH	EQ	WEXH	WTC	Remark
to 24 MHz	0	0	0	-	1	
to 48 MHz	0	0	1	-	2	
to 96 MHz	1	1	3	-	4	
to 100 MHz	1	1	3	-	4	

### 3.2.2. Flash write timing settings (synchronous write)

Core clock (CLKB)	ATD	ALEH	EQ	WEXH	WTC	Remark
to 16 MHz	0	-	-	0	3	
to 32 MHz	0	-	-	0	4	
to 48 MHz	0	-	-	0	5	
to 64 MHz	1	-	-	0	6	
to 96 MHz	1	-	-	0	7	
to 100 MHz	1	-	-	0	7	

### 3.3. Address mapping from CPU to parallel programming mode

The following tables show the calculation from CPU addresses to flash macro addresses which are used in parallel programming.

#### 3.3.1. Address mapping MB91F464HB

CPU Address (addr)	Condition	Flash sectors	FA (flash address) Calculation
14:8000h to 14:FFFFh	addr[2]==0	SA4, SA6 (8 Kbyte)	$FA := addr - addr\%00:4000h + (addr\%00:4000h)/2 - (addr/2)\%4 + addr\%4 - 0D:0000h$
14:8000h to 14:FFFFh	addr[2]==1	SA5, SA7 (8 Kbyte)	$FA := addr - addr\%00:4000h + (addr\%00:4000h)/2 + 00:2000h - (addr/2)\%4 + addr\%4 - 0D:0000h$
0A:0000h to 0F:FFFFh	addr[2]==0	SA14, SA16, SA18 (64 Kbyte)	$FA := addr - addr\%02:0000 + (addr\%02:0000h)/2 - (addr/2)\%4 + addr\%4$
0A:0000h to 0F:FFFFh	addr[2]==1	SA15, SA17, SA19 (64 Kbyte)	$FA := addr - addr\%02:0000h + (addr\%02:0000h)/2 + 01:0000h - (addr/2)\%4 + addr\%4$

Note: FA result is without 20:0000h offset for parallel Flash programming.

Set offset by keeping FA[21] = 1 as described in section "Parallel Flash programming mode".

# MB91460H Series

## 4. Parallel Flash programming mode

### 4.1. Flash configuration in parallel Flash programming mode

Parallel Flash programming mode (MD[2:0] = 111):

MB91F464HB	
FA[20:0] 001F:FFFh 001F:0000h	SA19 (64KB)
001E:FFFh 001E:0000h	SA18 (64KB)
001D:FFFh 001D:0000h	SA17 (64KB)
001C:FFFh 001C:0000h	SA16 (64KB)
001B:FFFh 001B:0000h	SA15 (64KB)
001A:FFFh 001A:0000h	SA14 (64KB)
	SA13 (64KB)
	SA12 (64KB)
	SA11 (64KB)
	SA10 (64KB)
	SA9 (64KB)
	SA8 (64KB)
0017:FFFh 0017:E000h	SA7 (8KB)
0017:DFFFh 0017:C000h	SA6 (8KB)
0017:BFFFh 0017:A000h	SA5 (8KB)
0017:9FFFh 0017:8000h	SA4 (8KB)
	SA3 (8KB)
	SA2 (8KB)
	SA1 (8KB)
	SA0 (8KB)
	FA[1:0]=00      FA[1:0]=10
16bit write mode	DQ[15:0]      DQ[15:0]

Remark: Always keep FA[0] = 0 and FA[20] = 1

Legend	Memory available in this area
	Memory not available in this area

## 4.2. Pin connections in parallel programming mode

Resetting after setting the MD[2:0] pins to [111] will halt CPU functioning. At this time, the Flash memory's interface circuit enables direct control of the Flash memory unit from external pins by directly linking some of the signals to GP-Ports. Please see table below for signal mapping.

In this mode, the Flash memory appears to the external pins as a stand-alone unit. This mode is generally set when writing/erasing using the parallel Flash programmer. In this mode, all operations of the 8.5 Mbits Flash memory's Auto Algorithms are available.

Correspondence between MBM29LV400TC and Flash Memory Control Signals

MBM29LV400TC External pins	FR-CPU mode	MB91F464HB external pins			Comment
		Flash memory mode	Normal function	Pin number	
-	INITX	-	INITX	84	
RESET	-	FRSTX	GP16_6	70	
-	-	MD2	MD2	76	Set to '1'
-	-	MD1	MD1	75	Set to '1'
-	-	MD0	MD0	74	Set to '1'
RY/BY	FMCS:RDY bit	RY/BYX	GP18_2	100	
BYTE	Internally fixed to 'H'	BYTEX	GP16_4	68	
WE	Internal control sig- nal + control via inter- face circuit	WEX	GP16_7	71	
OE		OEX	GP07_7	3	
CE		CEX	GP07_6	2	
-		ATDIN	GP18_6	103	Set to '0'
-		EQIN	GP18_5	102	Set to '0'
-		TESTX	GP16_5	69	Set to '1'
-		RDYI	GP18_4	101	Set to '0'
A-1		Internal address bus	FA0	GP05_5	17
A0 to A3	FA1 to FA4		GP19_0 to GP19_2, GP19_4	92 to 95	
A4 to A7	FA5 to FA8		GP19_5 to GP19_6, GP18_0 to GP18_1	96 to 99	
A8 to A11	FA9 to FA12		GP06_0 to GP06_3	4 to 7	
A12 to A15	FA13 to FA16		GP06_4 to GP06_7	8 to 11	
A16 to A18	FA17 to FA19		GP05_0 to GP05_2	12 to 14	
A19	FA20		GP05_3	15	Set to '1'
DQ0 to DQ7	Internal data bus		DQ0 to DQ7	GP00_0 to GP00_7	28 to 35
DQ8 to DQ15		DQ8 to DQ15	GP01_0 to GP01_7	20 to 27	

## 5. Poweron Sequence in parallel programming mode

The flash memory can be accessed in programming mode after a certain wait time, which is needed for Security Vector fetch:

- Minimum wait time after VDD5/VDD5R power on: 2.76 ms
- Minimum wait time after INITX rising: 1.0 ms

## 6. Flash Security

### 6.1. Vector addresses

Two Flash Security Vectors (FSV1, FSV2) are located parallel to the Boot Security Vectors (BSV1, BSV2) controlling the protection functions of the Flash Security Module:

FSV1: 0x14:8000      BSV1: 0x14:8004  
 FSV2: 0x14:8008      BSV2: 0x14:800C

### 6.2. Security Vector FSV1

The setting of the Flash Security Vector FSV1 is responsible for the read and write protection modes and the individual write protection of the 8 KBytes sectors.

#### 6.2.1. FSV1 (bit31 to bit16)

The setting of the Flash Security Vector FSV1 bits [31:16] is responsible for the read and write protection modes.

Explanation of the bits in the Flash Security Vector FSV1[31:16]

FSV1[31:19]	FSV1[18] Write Protection Level	FSV1[17] Write Protection	FSV1[16] Read Protection	Flash Security Mode
set all to '0'	set to '0'	set to '0'	set to '1'	Read Protection (all device modes, except INTVEC mode MD[2:0]="000")
set all to '0'	set to '0'	set to '1'	set to '0'	Write Protection (all device modes, without exception)
set all to '0'	set to '0'	set to '1'	set to '1'	Read Protection (all device modes, except INTVEC mode MD[2:0]="000") and Write Protection (all device modes)
set all to '0'	set to '1'	set to '0'	set to '1'	Read Protection (all device modes, except INTVEC mode MD[2:0]="000")
set all to '0'	set to '1'	set to '1'	set to '0'	Write Protection (all device modes, except INTVEC mode MD[2:0]="000")
set all to '0'	set to '1'	set to '1'	set to '1'	Read Protection (all device modes, except INTVEC mode MD[2:0]="000") and Write Protection (all device modes except INTVEC mode MD[2:0]="000")

## 6.2.2. FSV1 (bit15 to bit0) MB91F464HB

The setting of the Flash Security Vector FSV1 bits [15:0] is responsible for the individual write protection of the 8 KBytes sectors. It is only evaluated if write protection bit FSV1[17] is set.

Explanation of the bits in the Flash Security Vector FSV1[15:0]

FSV1 bit	Sector	Enable Write Protection	Disable Write Protection	Comment
FSV1[3:0]	—	—	—	not available
FSV1[4]	SA4	set to "0"	—	Write protection is mandatory!
FSV1[5]	SA5	set to "0"	set to "1"	
FSV1[6]	SA6	set to "0"	set to "1"	
FSV1[7]	SA7	set to "0"	set to "1"	
FSV1[15:8]	—	—	—	not available

Note: It is mandatory to always set the sector where the Flash Security Vectors FSV1 and FSV2 are located to write protected (here sector SA4). Otherwise it is possible to overwrite the Security Vector to a setting where it is possible to either read out the Flash content or manipulate data by writing.

See section "Flash access in CPU mode" for an overview about the sector organisation of the Flash Memory.

# MB91460H Series

## 6.3. Security Vector FSV2 MB91F464HB

The setting of the Flash Security Vector FSV2 bits [31:0] is responsible for the individual write protection of the 64 KByte sectors. It is only evaluated if write protection bit FSV1[17] is set.

Explanation of the bits in the Flash Security Vector FSV2[31:0]

FSV2 bit	Sector	Enable Write Protection	Disable Write Protection	Comment
FSV2[5:0]	—	—	—	not available
FSV2[6]	SA14	set to "0"	set to "1"	
FSV2[7]	SA15	set to "0"	set to "1"	
FSV2[8]	SA16	set to "0"	set to "1"	
FSV2[9]	SA17	set to "0"	set to "1"	
FSV2[10]	SA18	set to "0"	set to "1"	
FSV2[11]	SA19	set to "0"	set to "1"	
FSV2[31:12]	—	—	—	not available

Note : See section "Flash access in CPU mode" for an overview about the sector organisation of the Flash Memory.

## ■ MEMORY SPACE

The FR family has 4 Gbytes of logical address space ( $2^{32}$  addresses) available to the CPU by linear access.

- Direct addressing area

The following address space area is used for I/O.

This area is called direct addressing area, and the address of an operand can be specified directly in an instruction.

The size of directly addressable area depends on the length of the data being accessed as shown below.

Byte data access : 000<sub>H</sub> to 0FF<sub>H</sub>

Half word access : 000<sub>H</sub> to 1FF<sub>H</sub>

Word data access : 000<sub>H</sub> to 3FF<sub>H</sub>

# MB91460H Series

## ■ MEMORY MAPS

### 1. MB91F464HB

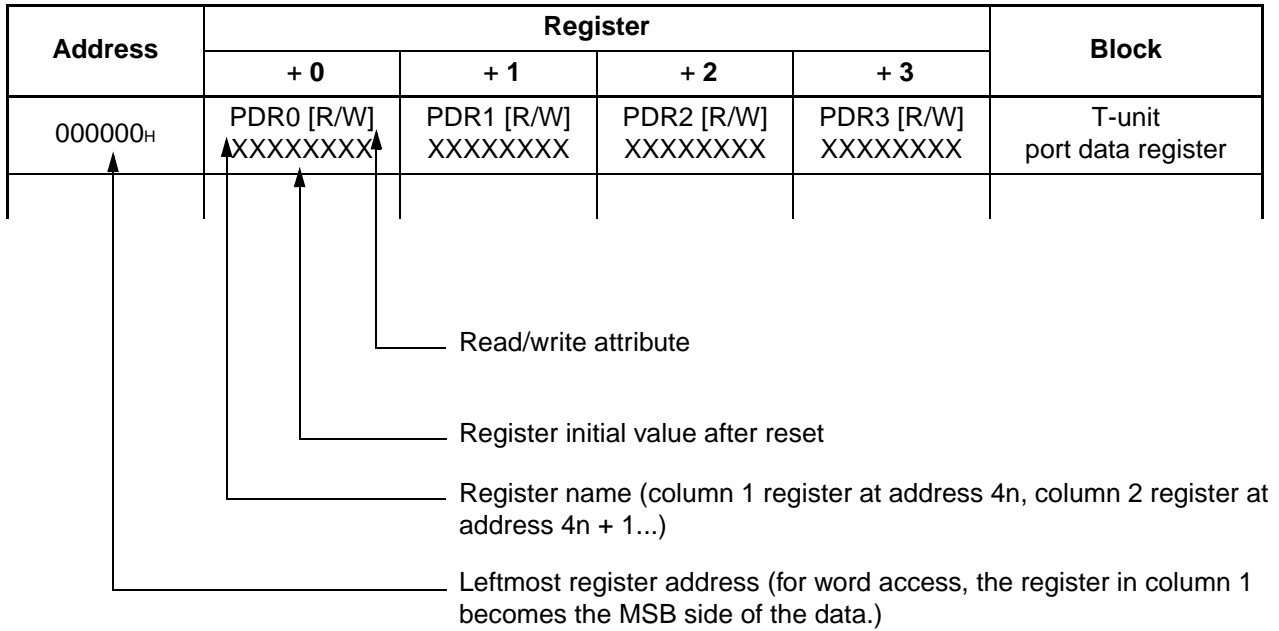
MB91F464HB

00000000H	I/O (direct addressing area)
00000400H	I/O
00001000H	DMA
00002000H	
00004000H	Flash-Cache (8 Kbytes)
00006000H	
00007000H	Flash memory control
00008000H	
0000B000H	Boot ROM (4 Kbytes)
0000C000H	CAN
0000D000H	
0002C000H	D-RAM (0 wait, 16 Kbytes)
00030000H	ID-RAM (16 Kbytes)
00034000H	
00040000H	External bus area
00080000H	
000A0000H	Flash memory (384 Kbytes)
00100000H	External bus area
00148000H	Flash memory (32 Kbytes)
00150000H	
00180000H	External bus area
00500000H	External data bus
FFFFFFFFH	

Note: Access prohibited areas

## ■ I/O MAP

### 1. MB91F464HB



Note : Initial values of register bits are represented as follows:

“ 1 ” : Initial value “ 1 ”

“ 0 ” : Initial value “ 0 ”

“ X ” : Initial value “ undefined ”

“ - ” : No physical register at this location

Access is barred with an undefined data access attribute.

# MB91460H Series

Address	Register				Block
	+0	+1	+2	+3	
000000H	PDR00 [R/W] XXXXXXXX	PDR01 [R/W] XXXXXXXX	Reserved	Reserved	R-bus Port Data Register
000004H	Reserved	PDR05 [R/W] -- XXXXXX	PDR06 [R/W] XXXXXXXX	PDR07 [R/W] XXXXXXXX	
000008H	PDR08 [R/W] X -- X --- X	PDR09 [R/W] ----- XX	PDR10 [R/W] ----- X	Reserved	
00000CH	Reserved	Reserved	PDR14 [R/W] XXXXXXXX	PDR15 [R/W] XXXXXXXX	
000010H	PDR16 [R/W] XXXXXXXX	PDR17 [R/W] XXXXXXXX	PDR18 [R/W] - XXX - XXX	PDR19 [R/W] - XXX - XXX	
000014H	PDR20 [R/W] - XXX - XXX	PDR21 [R/W] ----- XX	PDR22 [R/W] XXXXXXXX	PDR23 [R/W] XXXXXXXX	
000018H	PDR24 [R/W] XXXXXXXX	Reserved	PDR26 [R/W] XXXXXXXX	PDR27 [R/W] XXXXXXXX	
00001CH	PDR28 [R/W] XXXXXXXX	PDR29 [R/W] XXXXXXXX	Reserved	Reserved	
000020H to 00002CH	Reserved				
000030H	EIRR0 [R/W] XXXXXXXX	ENIR0 [R/W] 00000000	ELVR0 [R/W] 00000000 00000000		External interrupt (INT 0 to INT 7)
000034H	EIRR1 [R/W] XXXXXXXX	ENIR1 [R/W] 00000000	ELVR1 [R/W] 00000000 00000000		External interrupt (INT 8 to INT 15)
000038H	DICR [R/W] ----- 0	HRCL [R/W] 0 -- 11111	RBSYNC		Delay interrupt
00003CH	Reserved				Reserved
000040H	SCR00 [R/W,W] 00000000	SMR00 [R/W,W] 00000000	SSR00 [R/W,R] 00001000	RDR00/TDR00 [R/W] 00000000	LIN-USART 0
000044H	ESCR00 [R/W] 00000X00	ECCR00 [R/W,R,W] -00000XX	Reserved		
000048H 00004CH	Reserved				Reserved
000050H	SCR02 [R/W,W] 00000000	SMR02 [R/W,W] 00000000	SSR02 [R/W,R] 00001000	RDR02/TDR02 [R/W] 00000000	LIN-USART 2
000054H	ESCR02 [R/W] 00000X00	ECCR02 [R/W,R,W] -00000XX	Reserved		

# MB91460H Series

Address	Register				Block
	+0	+1	+2	+3	
000058 <sub>H</sub>	SCR03 [R/W,W] 00000000	SMR03 [R/W,W] 00000000	SSR03 [R/W,R] 00001000	RDR03/TDR03 [R/W] 00000000	LIN-USART 3
00005C <sub>H</sub>	ESCR03 [R/W] 00000X00	ECCR03 [R/W,R,W] -00000XX	Reserved		
000060 <sub>H</sub>	SCR04 [R/W,W] 00000000	SMR04 [R/W,W] 00000000	SSR04 [R/W,R] 00001000	RDR04/TDR04 [R/W] 00000000	LIN-USART 4 with FIFO
000064 <sub>H</sub>	ESCR04 [R/W] 00000X00	ECCR04 [R/W,R,W] -00000XX	FSR04 [R] - - - 00000	FCR04 [R/W] 0001 - 000	
000068 <sub>H</sub>	SCR05 [R/W,W] 00000000	SMR05 [R/W,W] 00000000	SSR05 [R/W,R] 00001000	RDR05/TDR05 [R/W] 00000000	LIN-USART 5 with FIFO
00006C <sub>H</sub>	ESCR05 [R/W] 00000X00	ECCR05 [R/W,R,W] -00000XX	FSR05 [R] - - - 00000	FCR05 [R/W] 0001 - 000	
000070 <sub>H</sub>	SCR06 [R/W,W] 00000000	SMR06 [R/W,W] 00000000	SSR06 [R/W,R] 00001000	RDR06/TDR06 [R/W] 00000000	LIN-USART 6 with FIFO
000074 <sub>H</sub>	ESCR06 [R/W] 00000X00	ECCR06 [R/W,R,W] -00000XX	FSR06 [R] - - - 00000	FCR06 [R/W] 0001 - 000	
000078 <sub>H</sub>	SCR07 [R/W,W] 00000000	SMR07 [R/W,W] 00000000	SSR07 [R/W,R] 00001000	RDR07/TDR07 [R/W] 00000000	LIN-USART 7 with FIFO
00007C <sub>H</sub>	ESCR07 [R/W] 00000X00	ECCR07 [R/W,R,W] -00000XX	FSR07 [R] - - - 00000	FCR07 [R/W] 0001 - 000	
000080 <sub>H</sub>	BGR100 [R/W] 00000000	BGR000 [R/W] 00000000	Reserved	Reserved	Baud rate Generator LIN-USART 0 to 7
000084 <sub>H</sub>	BGR102 [R/W] 00000000	BGR002 [R/W] 00000000	BGR103 [R/W] 00000000	BGR003 [R/W] 00000000	
000088 <sub>H</sub>	BGR104 [R/W] 00000000	BGR004 [R/W] 00000000	BGR105 [R/W] 00000000	BGR005 [R/W] 00000000	
00008C <sub>H</sub>	BGR106 [R/W] 00000000	BGR006 [R/W] 00000000	BGR107 [R/W] 00000000	BGR007 [R/W] 00000000	
000090 <sub>H</sub> to 0000CC <sub>H</sub>	Reserved				Reserved

# MB91460H Series

Address	Register				Block
	+0	+1	+2	+3	
0000D0 <sub>H</sub>	IBCR0 [R/W] 00000000	IBSR0 [R] 00000000	ITBAH0 [R/W] ----- 00	ITBAL0 [R/W] 00000000	I <sup>2</sup> C 0
0000D4 <sub>H</sub>	ITMKH0 [R/W] 00 ---- 11	ITMKL0 [R/W] 11111111	ISMK0 [R/W] 01111111	ISBA0 [R/W] - 0000000	
0000D8 <sub>H</sub>	Reserved	IDAR0 [R/W] 00000000	ICCR0 [R/W] - 0011111	Reserved	
0000DC <sub>H</sub>	IBCR1 [R/W] 00000000	IBSR1 [R] 00000000	ITBAH1 [R/W] ----- 00	ITBAL1 [R/W] 00000000	I <sup>2</sup> C 1
0000E0 <sub>H</sub>	ITMKH1 [R/W] 00 ---- 11	ITMKL1 [R/W] 11111111	ISMK1 [R/W] 01111111	ISBA1 [R/W] - 0000000	
0000E4 <sub>H</sub>	Reserved	IDAR1 [R/W] 00000000	ICCR1 [R/W] - 0011111	Reserved	
0000E8 <sub>H</sub> to 0000FC <sub>H</sub>	Reserved				Reserved
000100 <sub>H</sub>	GCN10 [R/W] 00110010 00010000		Reserved	GCN20 [R/W] ---- 0000	PPG Control 0 to 3
000104 <sub>H</sub>	GCN11 [R/W] 00110010 00010000		Reserved	GCN21 [R/W] ---- 0000	PPG Control 4 to 7
000108 <sub>H</sub>	GCN12 [R/W] 00110010 00010000		Reserved	GCN22 [R/W] ---- 0000	PPG Control 8 to 11
000110 <sub>H</sub>	PTMR00 [R] 11111111 11111111		PCSR00 [W] XXXXXXXX XXXXXXXX		PPG 0
000114 <sub>H</sub>	PDUT00 [W] XXXXXXXX XXXXXXXX		PCNH00 [R/W] 0000000 -	PCNL00 [R/W] 000000 - 0	
000118 <sub>H</sub>	PTMR01 [R] 11111111 11111111		PCSR01 [W] XXXXXXXX XXXXXXXX		PPG 1
00011C <sub>H</sub>	PDUT01 [W] XXXXXXXX XXXXXXXX		PCNH01 [R/W] 0000000 -	PCNL01 [R/W] 000000 - 0	
000120 <sub>H</sub>	PTMR02 [R] 11111111 11111111		PCSR02 [W] XXXXXXXX XXXXXXXX		PPG 2
000124 <sub>H</sub>	PDUT02 [W] XXXXXXXX XXXXXXXX		PCNH02 [R/W] 0000000 -	PCNL02 [R/W] 000000 - 0	
000128 <sub>H</sub>	PTMR03 [R] 11111111 11111111		PCSR03 [W] XXXXXXXX XXXXXXXX		PPG 3
00012C <sub>H</sub>	PDUT03 [W] XXXXXXXX XXXXXXXX		PCNH03 [R/W] 0000000 -	PCNL03 [R/W] 000000 - 0	
000130 <sub>H</sub>	PTMR04 [R] 11111111 11111111		PCSR04 [W] XXXXXXXX XXXXXXXX		PPG 4
000134 <sub>H</sub>	PDUT04 [W] XXXXXXXX XXXXXXXX		PCNH04 [R/W] 0000000 -	PCNL04 [R/W] 000000 - 0	

# MB91460H Series

Address	Register				Block
	+0	+1	+2	+3	
000138H	PTMR05 [R] 11111111 11111111		PCSR05 [W] XXXXXXXX XXXXXXXX		PPG 5
00013CH	PDUT05 [W] XXXXXXXX XXXXXXXX		PCNH05 [R/W] 0000000 -	PCNL05 [R/W] 000000 - 0	
000140H	PTMR06 [R] 11111111 11111111		PCSR06 [W] XXXXXXXX XXXXXXXX		PPG 6
000144H	PDUT06 [W] XXXXXXXX XXXXXXXX		PCNH06 [R/W] 0000000 -	PCNL06 [R/W] 000000 - 0	
000148H	PTMR07 [R] 11111111 11111111		PCSR07 [W] XXXXXXXX XXXXXXXX		PPG 7
00014CH	PDUT07 [W] XXXXXXXX XXXXXXXX		PCNH07 [R/W] 0000000 -	PCNL07 [R/W] 000000 - 0	
000150H	PTMR08 [R] 11111111 11111111		PCSR08 [W] XXXXXXXX XXXXXXXX		PPG 8
000154H	PDUT08 [W] XXXXXXXX XXXXXXXX		PCNH08 [R/W] 0000000 -	PCNL08 [R/W] 000000 - 0	
000158H	PTMR09 [R] 11111111 11111111		PCSR09 [W] XXXXXXXX XXXXXXXX		PPG 9
00015CH	PDUT09 [W] XXXXXXXX XXXXXXXX		PCNH09 [R/W] 0000000 -	PCNL09 [R/W] 000000 - 0	
000160H	PTMR10 [R] 11111111 11111111		PCSR10 [W] XXXXXXXX XXXXXXXX		PPG 10
000164H	PDUT10 [W] XXXXXXXX XXXXXXXX		PCNH10 [R/W] 0000000 -	PCNL10 [R/W] 000000 - 0	
000168H	PTMR11 [R] 11111111 11111111		PCSR11 [W] XXXXXXXX XXXXXXXX		PPG 11
00016CH	PDUT11 [W] XXXXXXXX XXXXXXXX		PCNH11 [R/W] 0000000 -	PCNL11 [R/W] 000000 - 0	
000170H to 00017CH	Reserved				Reserved
000180H	Reserved	ICS01 [R/W] 00000000	Reserved	ICS23 [R/W] 00000000	Input Capture 0 to 3
000184H	ICP0 [R] XXXXXXXX XXXXXXXX		ICP1 [R] XXXXXXXX XXXXXXXX		
000188H	ICP2 [R] XXXXXXXX XXXXXXXX		ICP3 [R] XXXXXXXX XXXXXXXX		

# MB91460H Series

Address	Register				Block
	+0	+1	+2	+3	
00018C <sub>H</sub>	OCS01 [R/W] ---0--00 0000--00		OCS23 [R/W] ---0--00 0000--00		Output Compare 0 to 3
000190 <sub>H</sub>	OCCP0 [R/W] XXXXXXXX XXXXXXXX		OCCP1 [R/W] XXXXXXXX XXXXXXXX		
000194 <sub>H</sub>	OCCP2 [R/W] XXXXXXXX XXXXXXXX		OCCP3 [R/W] XXXXXXXX XXXXXXXX		
000198 <sub>H</sub>	SGCRH [R/W] 0000--00	SGCRL [R/W] --0--000	SGFR [R/W, R] XXXXXXXX XXXXXXXX		Sound Generator
00019C <sub>H</sub>	SGAR [R/W] 00000000	Reserved	SGTR [R/W] XXXXXXXX	SGDR [R/W] XXXXXXXX	
0001A0 <sub>H</sub>	ADERH [R/W] 00000000 00000000		ADERL [R/W] 00000000 00000000		A/D Converter
0001A4	ADCS1 [R/W] 00000000	ADCS0 [R/W] 00000000	ADCR1 [R] 000000XX	ADCR0 [R] XXXXXXXX	
0001A8 <sub>H</sub>	ADCT1 [R/W] 00010000	ADCT0 [R/W] 00101100	ADSCH [R/W] ---00000	ADECH [R/W] ---00000	
0001AC <sub>H</sub>	Reserved	ACSR0 [R/W] -11XXX00	Reserved	Reserved	
0001B0 <sub>H</sub>	TMRLR0 [W] XXXXXXXX XXXXXXXX		TMR0 [R] XXXXXXXX XXXXXXXX		Reload Timer 0 (PPG 0, PPG 1)
0001B4 <sub>H</sub>	Reserved		TMCSRH0 [R/W] ---00000	TMCSRL0 [R/W] 0-000000	
0001B8 <sub>H</sub>	TMRLR1 [W] XXXXXXXX XXXXXXXX		TMR1 [R] XXXXXXXX XXXXXXXX		Reload Timer 1 (PPG 2, PPG 3)
0001BC <sub>H</sub>	Reserved		TMCSRH1 [R/W] ---00000	TMCSRL1 [R/W] 0-000000	
0001C0 <sub>H</sub>	TMRLR2 [W] XXXXXXXX XXXXXXXX		TMR2 [R] XXXXXXXX XXXXXXXX		Reload Timer 2 (PPG 4, PPG 5)
0001C4 <sub>H</sub>	Reserved		TMCSRH2 [R/W] ---00000	TMCSRL2 [R/W] 0-000000	
0001C8 <sub>H</sub>	TMRLR3 [W] XXXXXXXX XXXXXXXX		TMR3 [R] XXXXXXXX XXXXXXXX		Reload Timer 3 (PPG 6, PPG 7)
0001CC <sub>H</sub>	Reserved		TMCSRH3 [R/W] ---00000	TMCSRL3 [R/W] 0-000000	
0001D0 <sub>H</sub>	TMRLR4 [W] XXXXXXXX XXXXXXXX		TMR4 [R] XXXXXXXX XXXXXXXX		Reload Timer 4 (PPG 8, PPG 9)
0001D4 <sub>H</sub>	Reserved		TMCSRH4 [R/W] ---00000	TMCSRL4 [R/W] 0-000000	

# MB91460H Series

Address	Register				Block
	+0	+1	+2	+3	
0001D8 <sub>H</sub>	TMRLR5 [W] XXXXXXXX XXXXXXXX		TMR5 [R] XXXXXXXX XXXXXXXX		Reload Timer 5 (PPG 10, PPG 11)
0001DC <sub>H</sub>	Reserved		TMCSRH5 [R/W] - - - 00000	TMCSRL5 [R/W] 0 - 000000	
0001E0 <sub>H</sub>	TMRLR6 [W] XXXXXXXX XXXXXXXX		TMR6 [R] XXXXXXXX XXXXXXXX		Reload Timer 6 (PPG 12, PPG 13)
0001E4 <sub>H</sub>	Reserved		TMCSRH6 [R/W] - - - 00000	TMCSRL6 [R/W] 0 - 000000	
0001E8 <sub>H</sub>	TMRLR7 [W] XXXXXXXX XXXXXXXX		TMR7 [R] XXXXXXXX XXXXXXXX		Reload Timer 7 (PPG 14, PPG 15) (A/D Converter)
0001EC <sub>H</sub>	Reserved		TMCSRH7 [R/W] - - - 00000	TMCSRL7 [R/W] 0 - 000000	
0001F0 <sub>H</sub>	TCDT0 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS0 [R/W] 00000000	Free Running Timer 0 (ICU 0, ICU 1)
0001F4 <sub>H</sub>	TCDT1 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS1 [R/W] 00000000	Free Running Timer 1 (ICU 2, ICU 3)
0001F8 <sub>H</sub>	TCDT2 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS2 [R/W] 00000000	Free Running Timer 2 (OCU 0, OCU 1)
0001FC <sub>H</sub>	TCDT3 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS3 [R/W] 00000000	Free Running Timer 3 (OCU 2, OCU 3)
000200 <sub>H</sub>	DMACA0 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000204 <sub>H</sub>	DMACB0 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000208 <sub>H</sub>	DMACA1 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00020C <sub>H</sub>	DMACB1 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000210 <sub>H</sub>	DMACA2 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000214 <sub>H</sub>	DMACB2 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000218 <sub>H</sub>	DMACA3 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00021C <sub>H</sub>	DMACB3 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				

# MB91460H Series

Address	Register				Block
	+0	+1	+2	+3	
000220H	DMACA4 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000224H	DMACB4 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000228H to 00023CH	Reserved				
000240H	DMACR [R/W] 00 -- 0000	Reserved			
000244H to 0002CCH	Reserved				Reserved
0002D0H	Reserved	ICS045 [R/W] 00000000	Reserved	ICS67 [R/W] 00000000	Input Capture 4 to 7
0002D4H	IPCP4 [R] XXXXXXXX XXXXXXXX		IPCP5 [R] XXXXXXXX XXXXXXXX		
0002D8H	IPCP6 [R] XXXXXXXX XXXXXXXX		IPCP7 [R] XXXXXXXX XXXXXXXX		
0002DC H	OCS45 [R/W] --- 0 -- 00 0000 -- 00		OCS67 [R/W] --- 0 -- 00 0000 -- 00		
0002E0H	OCCP4 [R/W] XXXXXXXX XXXXXXXX		OCCP5 [R/W] XXXXXXXX XXXXXXXX		Output Compare 4 to 7
0002E4H	OCCP6 [R/W] XXXXXXXX XXXXXXXX		OCCP7 [R/W] XXXXXXXX XXXXXXXX		
0002E8H to 0002ECH	Reserved				
0002F0H	TCDT4 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS4 [R/W] 00000000	Free Running Timer 4 (ICU 4, ICU 5)
0002F4H	TCDT5 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS5 [R/W] 00000000	Free Running Timer 5 (ICU 6, ICU 7)
0002F8H	TCDT6 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS6 [R/W] 00000000	Free Running Timer 6 (OCU 4, OCU 5)
0002FCH	TCDT7 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS7 [R/W] 00000000	Free Running Timer 7 (OCU 6, OCU 7)

# MB91460H Series

Address	Register				Block
	+0	+1	+2	+3	
000300 <sub>H</sub>	UDRC1 [W] 00000000	UDRC0 [W] 00000000	UDCR1 [R] 00000000	UDCR0 [R] 00000000	Up/Down Counter 0 to 1
000304 <sub>H</sub>	UDCCH0 [R/W] 00000000	UDCCL0 [R/W] 00001000	Reserved	UDCS0 [R/W] 00000000	
000308 <sub>H</sub>	UDCCH1 [R/W] 00000000	UDCCL1 [R/W] 00001000	Reserved	UDCS1 [R/W] 00000000	
00030C <sub>H</sub> to 00031C <sub>H</sub>	Reserved				Reserved
000320 <sub>H</sub>	GCN13 [R/W] 00110010 00010000		Reserved	GCN23 [R/W] ---- 0000	PPG Control 12 to 15
000324 <sub>H</sub> to 00032C <sub>H</sub>	Reserved				Reserved
000330 <sub>H</sub>	PTMR12 [R] 11111111 11111111		PCSR12 [W] XXXXXXXX XXXXXXXX		PPG 12
000334 <sub>H</sub>	PDUT12 [W] XXXXXXXX XXXXXXXX		PCNH12 [R/W] 0000000 -	PCNL12 [R/W] 000000 - 0	
000338 <sub>H</sub>	PTMR13 [R] 11111111 11111111		PCSR13 [W] XXXXXXXX XXXXXXXX		PPG 13
00033C <sub>H</sub>	PDUT13 [W] XXXXXXXX XXXXXXXX		PCNH13 [R/W] 0000000 -	PCNL13 [R/W] 000000 - 0	
000340 <sub>H</sub>	PTMR14 [R] 11111111 11111111		PCSR14 [W] XXXXXXXX XXXXXXXX		PPG 14
000344 <sub>H</sub>	PDUT14 [W] XXXXXXXX XXXXXXXX		PCNH14 [R/W] 0000000 -	PCNL14 [R/W] 000000 - 0	
000348 <sub>H</sub>	PTMR15 [R] 11111111 11111111		PCSR15 [W] XXXXXXXX XXXXXXXX		PPG 15
00034C <sub>H</sub>	PDUT15 [W] XXXXXXXX XXXXXXXX		PCNH15 [R/W] 0000000 -	PCNL15 [R/W] 000000 - 0	
000350 <sub>H</sub> to 00038C <sub>H</sub>	Reserved				Reserved
000390 <sub>H</sub>	ROMS [R] 11111111 01000011		Reserved		ROM Select Register
000394 <sub>H</sub> to 0003EC <sub>H</sub>	Reserved				Reserved

# MB91460H Series

Address	Register				Block
	+0	+1	+2	+3	
0003F0H	BSD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit Search Module
0003F4H	BSD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003F8H	BSDC [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003FCH	BSRR [R] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000400H to 00043CH	Reserved				
000440H	ICR00 [R/W] ---11111	ICR01 [R/W] ---11111	ICR02 [R/W] ---11111	ICR03 [R/W] ---11111	Interrupt Controller
000444H	ICR04 [R/W] ---11111	ICR05 [R/W] ---11111	ICR06 [R/W] ---11111	ICR07 [R/W] ---11111	
000448H	ICR08 [R/W] ---11111	ICR09 [R/W] ---11111	ICR10 [R/W] ---11111	ICR11 [R/W] ---11111	
00044CH	ICR12 [R/W] ---11111	ICR13 [R/W] ---11111	ICR14 [R/W] ---11111	ICR15 [R/W] ---11111	
000450H	ICR16 [R/W] ---11111	ICR17 [R/W] ---11111	ICR18 [R/W] ---11111	ICR19 [R/W] ---11111	
000454H	ICR20 [R/W] ---11111	ICR21 [R/W] ---11111	ICR22 [R/W] ---11111	ICR23 [R/W] ---11111	
000458H	ICR24 [R/W] ---11111	ICR25 [R/W] ---11111	ICR26 [R/W] ---11111	ICR27 [R/W] ---11111	
00045CH	ICR28 [R/W] ---11111	ICR29 [R/W] ---11111	ICR30 [R/W] ---11111	ICR31 [R/W] ---11111	
000460H	ICR32 [R/W] ---11111	ICR33 [R/W] ---11111	ICR34 [R/W] ---11111	ICR35 [R/W] ---11111	
000464H	ICR36 [R/W] ---11111	ICR37 [R/W] ---11111	ICR38 [R/W] ---11111	ICR39 [R/W] ---11111	
000468H	ICR40 [R/W] ---11111	ICR41 [R/W] ---11111	ICR42 [R/W] ---11111	ICR43 [R/W] ---11111	
00046CH	ICR44 [R/W] ---11111	ICR45 [R/W] ---11111	ICR46 [R/W] ---11111	ICR47 [R/W] ---11111	
000470H	ICR48 [R/W] ---11111	ICR49 [R/W] ---11111	ICR50 [R/W] ---11111	ICR51 [R/W] ---11111	
000474H	ICR52 [R/W] ---11111	ICR53 [R/W] ---11111	ICR54 [R/W] ---11111	ICR55 [R/W] ---11111	
000478H	ICR56 [R/W] ---11111	ICR57 [R/W] ---11111	ICR58 [R/W] ---11111	ICR59 [R/W] ---11111	

# MB91460H Series

Address	Register				Block
	+0	+1	+2	+3	
00047C <sub>H</sub>	ICR60 [R/W] ---11111	ICR61 [R/W] ---11111	ICR62 [R/W] ---11111	ICR63 [R/W] ---11111	Interrupt Controller
000480 <sub>H</sub>	RSRR [R/W] 10000000	STCR [R/W] 00110011	TBCR [R/W] 00XXXX00	CTBR [W] XXXXXXXX	Clock Control
000484 <sub>H</sub>	CLKR [R/W] ---- 0000	WPR [W] XXXXXXXX	DIVR0 [R/W] 00000011	DIVR1 [R/W] 00000000	
000488 <sub>H</sub>	Reserved				Reserved
00048C <sub>H</sub>	PLLDIVM [R/W] ---- 0000	PLLDIVN [R/W] -- 000000	PLLDIVG [R/W] ---- 0000	PLLMULG [R/W] 00000000	PLL Interface
000490 <sub>H</sub>	PLLCTRL [R/W] ---- 0000	Reserved			
000494 <sub>H</sub>	OSCC1 [R/W] ----- 010	OSCS1 [R/W] 00001111	OSCC2 [R/W] ----- 010	OSCS2 [R/W] 00001111	Main/Sub Oscillator Control (Reserved)
000498 <sub>H</sub>	PORTEN [R/W] ----- 00	Reserved			Port Input Enable Control
0004A0 <sub>H</sub>	Reserved	WT CER [R/W] ----- 00	WT CR [R/W] 00000000 000 - 00 - 0		Real Time Clock (Watch Timer)
0004A4 <sub>H</sub>	Reserved	WT BR [R/W] --- XXXXX XXXXXXXX XXXXXXXX			
0004A8 <sub>H</sub>	WTHR [R/W] --- 00000	WT MR [R/W] -- 000000	WTSR [R/W] -- 000000	Reserved	
0004AC <sub>H</sub>	CSVTR [R/W] --- 00010	CSVCR [R/W] - 011100	CSCFG [R/W] 0X000000	CMCFG [R/W] 00000000	Clock-Supervisor/Selector/Monitor
0004B0 <sub>H</sub>	CUCR [R/W] ----- 0 -- 00		CUTD [R/W] 10000000 00000000		Calibration of Sub Clock
0004B4 <sub>H</sub>	CUTR1 [R] ----- 00000000		CUTR2 [R] 00000000 00000000		
0004B8 <sub>H</sub>	CMPR [R/W] -- 000010 11111101		Reserved	CMCR [R/W] - 001 -- 00	Clock Modulator
0004BC <sub>H</sub>	CMT1 [R/W] 00000000 1 --- 0000		CMT2 [R/W] -- 000000 -- 000000		
0004C0 <sub>H</sub>	CANPRE [R/W] 0 --- 0000	CANCKD [R/W] -- 000000	Reserved		CAN Clock Control
0004C4 <sub>H</sub>	LVSEL [R/W] 00000111	LVDET [R/W] 00000 - 00	HWWE [R/W] ----- 00	HWWD [R/W,W] 00011000	Low Voltage Detection/ Hardware Watchdog
0004C8 <sub>H</sub>	OSCRH [R/W] 000 -- 001	OSCRL [R/W] ----- 000	WPCRH [R/W] 000 -- 001	WPCRL [R/W] ----- 00	Main-/Sub-Oscillation Stabilisation Timer

# MB91460H Series

Address	Register				Block
	+0	+1	+2	+3	
0004CC <sub>H</sub>	OSCCR [R/W] -----00	Reserved	REGSEL [R/W] --000110	REGCTR [R/W] ---0--00	Main- Oscillation Standby Control / Main/Sub Regulator Control
0004D0 <sub>H</sub> to 00063C <sub>H</sub>	Reserved				Reserved
000640 <sub>H</sub>	ASR0 [R/W] 00000000 00000000		ACR0 [R/W] 1111**00 00000000 <sup>2</sup>		External Bus Unit
000644 <sub>H</sub>	ASR1 [R/W] XXXXXXXX XXXXXXXX		ACR1 [R/W] XXXXXXXX XXXXXXXX		
000648 <sub>H</sub>	ASR2 [R/W] XXXXXXXX XXXXXXXX		ACR2 [R/W] XXXXXXXX XXXXXXXX		
00064C <sub>H</sub>	ASR3 [R/W] XXXXXXXX XXXXXXXX		ACR3 [R/W] XXXXXXXX XXXXXXXX		
000650 <sub>H</sub>	ASR4 [R/W] XXXXXXXX XXXXXXXX		ACR4 [R/W] XXXXXXXX XXXXXXXX		
000654 <sub>H</sub>	ASR5 [R/W] XXXXXXXX XXXXXXXX		ACR5 [R/W] XXXXXXXX XXXXXXXX		
000658 <sub>H</sub>	ASR6 [R/W] XXXXXXXX XXXXXXXX		ACR6 [R/W] XXXXXXXX XXXXXXXX		
00065C <sub>H</sub>	ASR7 [R/W] XXXXXXXX XXXXXXXX		ACR7 [R/W] XXXXXXXX XXXXXXXX		
000660 <sub>H</sub>	AWR0 [R/W] 01111111 1111*11		AWR1 [R/W] XXXXXXXX XXXXXXXX		
000664 <sub>H</sub>	AWR2 [R/W] XXXXXXXX XXXXXXXX		AWR3 [R/W] XXXXXXXX XXXXXXXX		
000668 <sub>H</sub>	AWR4 [R/W] XXXXXXXX XXXXXXXX		AWR5 [R/W] XXXXXXXX XXXXXXXX		
00066C <sub>H</sub>	AWR6 [R/W] XXXXXXXX XXXXXXXX		AWR7 [R/W] XXXXXXXX XXXXXXXX		
000670 <sub>H</sub>	MCRA [R/W] XXXXXXXX	MCRB [R/W] XXXXXXXX	Reserved		
000674 <sub>H</sub>	Reserved				
000678 <sub>H</sub>	IOWR0 [R/W] XXXXXXXX	IOWR1 [R/W] XXXXXXXX	IOWR2 [R/W] XXXXXXXX	IOWR3 [R/W] XXXXXXXX	
00067C <sub>H</sub>	Reserved				
000680 <sub>H</sub>	CSER [R/W] 00000001	CHER [R/W] 11111111	Reserved	TCR [R/W] 0000**** <sup>3</sup>	
000684 <sub>H</sub>	RCRH [R/W] 00XXXXXX	RCRL [R/W] XXXX0XXX	Reserved		

# MB91460H Series

Address	Register				Block
	+0	+1	+2	+3	
000688H to 0007F8H	Reserved				External Bus Unit
0007FC <sub>H</sub>	Reserved	MODR [W] XXXXXXXX	Reserved		Mode Register
000800H to 000CFC <sub>H</sub>	Reserved				Reserved
000D00 <sub>H</sub>	PDRD00 [R] XXXXXXXX	PDRD01 [R] XXXXXXXX	Reserved		R-bus Port Data Direct Read Register
000D04 <sub>H</sub>	Reserved	PDRD05 [R] -- XXXXXX	PDRD06 [R] XXXXXXXX	PDRD07 [R] XXXXXXXX	
000D08 <sub>H</sub>	PDRD08 [R] X -- X --- X	PDRD09 [R] ----- XX	PDRD10 [R] ----- X	Reserved	
000D0C <sub>H</sub>	Reserved		PDRD14 [R] XXXXXXXX	PDRD15 [R] XXXXXXXX	
000D10 <sub>H</sub>	PDRD16 [R] XXXXXXXX	PDRD17 [R] XXXXXXXX	PDRD18 [R] - XXX - XXX	PDRD19 [R] - XXX - XXX	
000D14 <sub>H</sub>	PDRD20 [R] - XXX - XXX	PDRD21 [R] ----- X	PDRD22 [R] XXXXXXXX	PDRD23 [R] XXXXXXXX	
000D18 <sub>H</sub>	PDRD24 [R] XXXXXXXX	Reserved	PDRD26 [R] XXXXXXXX	PDRD27 [R] XXXXXXXX	
000D1C <sub>H</sub>	PDRD28 [R] XXXXXXXX	PDRD29 [R] XXXXXXXX	Reserved		
000D20H to 000D3C <sub>H</sub>	Reserved				
000D40 <sub>H</sub>	DDR00 [R/W] 00000000	DDR01 [R/W] 00000000	Reserved		R-bus Port Direction Register
000D44 <sub>H</sub>	Reserved	DDR05 [R/W] -- 000000	DDR06 [R/W] 00000000	DDR07 [R/W] 00000000	
000D48 <sub>H</sub>	DDR08 [R/W] 0 -- 0 --- 0	DDR09 [R/W] ----- 00	DDR10 [R/W] ----- 0	Reserved	
000D4C <sub>H</sub>	Reserved		DDR14 [R/W] 00000000	DDR15 [R/W] 00000000	
000D50 <sub>H</sub>	DDR16 [R/W] 00000000	DDR17 [R/W] 00000000	DDR18 [R/W] - 000 - 000	DDR19 [R/W] - 000 - 000	
000D54 <sub>H</sub>	DDR20 [R/W] - 000 - 000	DDR21 [R/W] ----- 00	DDR22 [R/W] 00000000	DDR23 [R/W] 00000000	
000D58 <sub>H</sub>	DDR24 [R/W] 00000000	Reserved	DDR26 [R/W] 00000000	DDR27 [R/W] 00000000	
000D5C <sub>H</sub>	DDR28 [R/W] 00000000	DDR29 [R/W] 00000000	Reserved		

# MB91460H Series

Address	Register				Block
	+0	+1	+2	+3	
000D60H to 000D7CH	Reserved				Reserved
000D80H	PFR00 [R/W] 11111111	PFR01 [R/W] 11111111	Reserved		R-bus Port Function Register
000D84H	Reserved	PFR05 [R/W] -- 111111	PFR06 [R/W] 11111111	PFR07 [R/W] 11111111	
000D88H	PFR08 [R/W] 1 -- 1 -- 11	PFR09 [R/W] ----- 11	PFR10 [R/W] -----1	Reserved	
000D8CH	Reserved		PFR14 [R/W] 00000000	PFR15 [R/W] 00000000	
000D90H	PFR16 [R/W] 00000000	PFR17 [R/W] 00000000	PFR18 [R/W] - 000 - 000	PFR19 [R/W] - 000 - 000	
000D94H	PFR20 [R/W] - 000 - 000	PFR21 [R/W] ----- 00	PFR22 [R/W] 0000-0-0	PFR23 [R/W] -0000000	
000D98H	PFR24 [R/W] 00000000	Reserved	PFR26 [R/W] 00000000	PFR27 [R/W] 00000000	
000D9CH	PFR28 [R/W] 00000000	PFR29 [R/W] 00000000	Reserved		
000DA0H to 000DC4H	Reserved				
000DC8H	Reserved		EPFR10 [R/W] ----- 0	Reserved	R-bus Port Extra Function Register
000DCC8H	Reserved		EPFR14 [R/W] 00000000	EPFR15 [R/W] 00000000	
000DD0H	EPFR16 [R/W] 0 - 00 - - - -	Reserved	EPFR18 [R/W] - 000 - 000	EPFR19 [R/W] - 0 - - - 0 - -	
000DD4H	EPFR20 [R/W] - 000 - 000	EPFR21 [R/W] -----	Reserved		
000DD8H	Reserved		EPFR26 [R/W] 00000000	EPFR27 [R/W] 00000000	
000DDCH to 000DFCH	Reserved				Reserved

# MB91460H Series

Address	Register				Block
	+0	+1	+2	+3	
000E00H	PODR00 [R/W] 00000000	PODR01 [R/W] 00000000	Reserved		R-bus Port Output Drive Select Register
000E04H	Reserved	PODR05 [R/W] -- 000000	PODR06 [R/W] 00000000	PODR07 [R/W] 00000000	
000E08H	PODR08 [R/W] 0 -- 0 --- 0	PODR09 [R/W] ----- 00	PODR10 [R/W] ----- 0	Reserved	
000E0CH	Reserved		PODR14 [R/W] 00000000	PODR15 [R/W] 00000000	
000E10H	PODR16 [R/W] 00000000	PODR17 [R/W] 00000000	PODR18 [R/W] - 000 - 000	PODR19 [R/W] - 000 - 000	
000E14H	PODR20 [R/W] - 000 - 000	PODR21 [R/W] ----- 00	PODR22 [R/W] 00000000	PODR23 [R/W] 00000000	
000E18H	PODR24 [R/W] 00000000	Reserved	PODR26 [R/W] 00000000	PODR27 [R/W] 00000000	
000E1CH	PODR28 [R/W] 00000000	PODR29 [R/W] 00000000	Reserved		
000E20H to 000E3CH	Reserved				Reserved
000E40H	PILR00 [R/W] 00000000	PILR01 [R/W] 00000000	Reserved		R-bus Port Input Level Select Register
000E44H	Reserved	PILR05 [R/W] -- 000000	PILR06 [R/W] 00000000	PILR07 [R/W] 00000000	
000E48H	PILR08 [R/W] 0 -- 0 --- 0	PILR09 [R/W] ----- 00	PILR10 [R/W] ----- 0	Reserved	
000E4CH	Reserved		PILR14 [R/W] 00000000	PILR15 [R/W] 00000000	
000E50H	PILR16 [R/W] 00000000	PILR17 [R/W] 00000000	PILR18 [R/W] ----- 000	PILR19 [R/W] - 000 - 000	
000E54H	PILR20 [R/W] - 000 - 000	PILR21 [R/W] ----- 00	PILR22 [R/W] 00000000	PILR23 [R/W] 00000000	
000E58H	PILR24 [R/W] 00000000	Reserved	PILR26 [R/W] 00000000	PILR27 [R/W] 00000000	
000E5CH	PILR28 [R/W] 00000000	PILR29 [R/W] 00000000	Reserved		
000E60H to 000E7CH	Reserved				Reserved

# MB91460H Series

Address	Register				Block
	+0	+1	+2	+3	
000E80 <sub>H</sub>	EPILR00 [R/W] 00000000	EPILR01 [R/W] 00000000	Reserved		R-bus Port Extra Input Level Select Register
000E84 <sub>H</sub>	Reserved	EPILR05 [R/W] -- 000000	EPILR06 [R/W] 00000000	EPILR07 [R/W] 00000000	
000E88 <sub>H</sub>	EPILR08 [R/W] 0--0---0	EPILR09 [R/W] -----00	EPILR10 [R/W] -----0	Reserved	
000E8C <sub>H</sub>	Reserved		EPILR14 [R/W] 00000000	EPILR15 [R/W] 00000000	
000E90 <sub>H</sub>	EPILR16 [R/W] 00000000	EPILR17 [R/W] 00000000	EPILR18 [R/W] -----000	EPILR19 [R/W] -000-000	
000E94 <sub>H</sub>	EPILR20 [R/W] -000-000	EPILR21 [R/W] -----00	EPILR22 [R/W] 00000000	EPILR23 [R/W] 00000000	
000E98 <sub>H</sub>	EPILR24 [R/W] 00000000	Reserved	EPILR26 [R/W] 00000000	EPILR27 [R/W] 00000000	
000E9C <sub>H</sub>	EPILR28 [R/W] 00000000	EPILR29 [R/W] 00000000	Reserved		
000EA0 <sub>H</sub> to 000EBC <sub>H</sub>	Reserved				Reserved
000EC0 <sub>H</sub>	PPER00 [R/W] 00000000	PPER01 [R/W] 00000000	Reserved		R-bus Port Pull-Up/Down Enable Register
000EC4 <sub>H</sub>	Reserved	PPER05 [R/W] -- 000000	PPER06 [R/W] 00000000	PPER07 [R/W] 00000000	
000EC8 <sub>H</sub>	PPER08 [R/W] 0--0---0	PPER09 [R/W] -----00	PPER10 [R/W] -----0	Reserved	
000ECC <sub>H</sub>	Reserved		PPER14 [R/W] 00000000	PPER15 [R/W] 00000000	
000ED0 <sub>H</sub>	PPER16 [R/W] 00000000	PPER17 [R/W] 00000000	PPER18 [R/W] -000-000	PPER19 [R/W] -000-000	
000ED4 <sub>H</sub>	PPER20 [R/W] -000-000	PPER21 [R/W] -----00	PPER22 [R/W] 00000000	PPER23 [R/W] 00000000	
000ED8 <sub>H</sub>	PPER24 [R/W] 00000000	Reserved	PPER26 [R/W] 00000000	PPER27 [R/W] 00000000	
000EDC <sub>H</sub>	PPER28 [R/W] 00000000	PPER29 [R/W] 00000000	Reserved		
000EE0 <sub>H</sub> to 000EFC <sub>H</sub>	Reserved				Reserved

# MB91460H Series

Address	Register				Block
	+0	+1	+2	+3	
000F00 <sub>H</sub>	PPCR00 [R/W] 11111111	PPCR01 [R/W] 11111111	Reserved		R-bus Port Pull-Up/Down Control Register
000F04 <sub>H</sub>	Reserved	PPCR05 [R/W] -- 111111	PPCR06 [R/W] 11111111	PPCR07 [R/W] 11111111	
000F08 <sub>H</sub>	PPCR08 [R/W] 1 -- 1 --- 1	PPCR09 [R/W] ----- 11	PPCR10 [R/W] ----- 1	Reserved	
000F0C <sub>H</sub>	Reserved		PPCR14 [R/W] 00000000	PPCR15 [R/W] 11111111	
000F10 <sub>H</sub>	PPCR16 [R/W] 00000000	PPCR17 [R/W] 00000000	PPCR18 [R/W] - 111- 111	PPCR19 [R/W] - 111- 111	
000F14 <sub>H</sub>	PPCR20 [R/W] - 111- 111	PPCR21 [R/W] ----- 11	PPCR22 [R/W] 11111111	PPCR23 [R/W] 11111111	
000F18 <sub>H</sub>	PPCR24 [R/W] 11111111	Reserved	PPCR26 [R/W] 11111111	PPCR27 [R/W] 11111111	
000F1C <sub>H</sub>	PPCR28 [R/W] 11111111	PPCR29 [R/W] 11111111	Reserved		
000F20 <sub>H</sub> to 000F3C <sub>H</sub>	Reserved				Reserved
001000 <sub>H</sub>	DMASA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
001004 <sub>H</sub>	DMADA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001008 <sub>H</sub>	DMASA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00100C <sub>H</sub>	DMADA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001010 <sub>H</sub>	DMASA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001014 <sub>H</sub>	DMADA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001018 <sub>H</sub>	DMASA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00101C <sub>H</sub>	DMADA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001020 <sub>H</sub>	DMASA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001024 <sub>H</sub>	DMADA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001028 <sub>H</sub> to 003FFC <sub>H</sub>	Reserved				Reserved

# MB91460H Series

Address	Register				Block
	+0	+1	+2	+3	
002000 <sub>H</sub> to 006FFC <sub>H</sub>	Flash-cache size is 8 Kbytes : 004000 <sub>H</sub> to 005FFC <sub>H</sub>				Flash-cache / I-RAM area
007000 <sub>H</sub>	FMCS [R/W] 01101000	FMCR [R/W] ---- 0000	FCHCR [R/W] ----- 00 10000011		Flash Memory/ I-Cache Control Register
007004 <sub>H</sub>	FMWT [R/W] 11111111 11111111		Reserved	FMPS [R/W] ----- 000	
007008 <sub>H</sub>	FMAC [R] 00000000 00000000 00000000 00000000				
00700C <sub>H</sub>	FCHA0 [R/W] ----- -- 000000 00000000 00000000				I-Cache Non-cache- able area setting Register
007010 <sub>H</sub>	FCHA1 [R/W] ----- -- 000000 00000000 00000000				
007014 <sub>H</sub> to 007FFC <sub>H</sub>	Reserved				Reserved
008000 <sub>H</sub> to 00BFFC <sub>H</sub>	Boot-ROM size is 4 Kbytes : 00B000 <sub>H</sub> to 00BFFC <sub>H</sub> (instruction access is 1 wait cycle, data access is 1 wait cycle)				Boot ROM area
00C000 <sub>H</sub>	CTRLR0 [R/W] 00000000 00000001		STATR0 [R/W] 00000000 00000000		CAN 0 Control Register
00C004 <sub>H</sub>	ERRCNT0 [R] 00000000 00000000		BTR0 [R/W] 00100011 00000001		
00C008 <sub>H</sub>	INTR0 [R] 00000000 00000000		TESTR0 [R/W] 00000000 X0000000		
00C00C <sub>H</sub>	BRPE0 [R/W] 00000000 00000000		CBSYNC0		

# MB91460H Series

Address	Register				Block
	+0	+1	+2	+3	
00C010 <sub>H</sub>	IF1CREQ0 [R/W] 00000000 00000001		IF1CMSK0 [R/W] 00000000 00000000		CAN 0 IF 1 Register
00C014 <sub>H</sub>	IF1MSK20 [R/W] 11111111 11111111		IF1MSK10 [R/W] 11111111 11111111		
00C018 <sub>H</sub>	IF1ARB20 [R/W] 00000000 00000000		IF1ARB10 [R/W] 00000000 00000000		
00C01C <sub>H</sub>	IF1MCTR0 [R/W] 00000000 00000000		Reserved		
00C020 <sub>H</sub>	IF1DTA10 [R/W] 00000000 00000000		IF1DTA20 [R/W] 00000000 00000000		
00C024 <sub>H</sub>	IF1DTB10 [R/W] 00000000 00000000		IF1DTB20 [R/W] 00000000 00000000		
00C028 <sub>H</sub> to 00C02C <sub>H</sub>	Reserved				
00C030 <sub>H</sub>	IF1DTA20 [R/W] 00000000 00000000		IF1DTA10 [R/W] 00000000 00000000		
00C034 <sub>H</sub>	IF1DTB20 [R/W] 00000000 00000000		IF1DTB10 [R/W] 00000000 00000000		
00C038 <sub>H</sub> to 00C03C <sub>H</sub>	Reserved				
00C040 <sub>H</sub>	IF2CREQ0 [R/W] 00000000 00000001		IF2CMSK0 [R/W] 00000000 00000000		CAN 0 IF 2 Register
00C044 <sub>H</sub>	IF2MSK20 [R/W] 11111111 11111111		IF2MSK10 [R/W] 11111111 11111111		
00C048 <sub>H</sub>	IF2ARB20 [R/W] 00000000 00000000		IF2ARB10 [R/W] 00000000 00000000		

# MB91460H Series

Address	Register				Block
	+0	+1	+2	+3	
00C04 <sub>H</sub>	IF2MCTR0 [R/W] 00000000 00000000		Reserved		CAN 0 Status Flags
00C05 <sub>H</sub>	IF2DTA10 [R/W] 00000000 00000000		IF2DTA20 [R/W] 00000000 00000000		
00C05 <sub>4H</sub>	IF2DTB10 [R/W] 00000000 00000000		IF2DTB20 [R/W] 00000000 00000000		
00C05 <sub>8H</sub> to 00C05 <sub>CH</sub>	Reserved				
00C06 <sub>0H</sub>	IF2DTA20 [R/W] 00000000 00000000		IF2DTA10 [R/W] 00000000 00000000		
00C06 <sub>4H</sub>	IF2DTB20 [R/W] 00000000 00000000		IF2DTB10 [R/W] 00000000 00000000		
00C06 <sub>8H</sub> to 00C07 <sub>CH</sub>	Reserved				
00C08 <sub>0H</sub>	TREQR20 [R] 00000000 00000000		TREQR10 [R] 00000000 00000000		
00C08 <sub>4H</sub> to 00C08 <sub>CH</sub>	Reserved		Reserved		
00C09 <sub>0H</sub>	NEWDT20 [R] 00000000 00000000		NEWDT10 [R] 00000000 00000000		
00C09 <sub>4H</sub> to 00C09 <sub>CH</sub>	Reserved		Reserved		
00C0A <sub>0H</sub>	INTPND20 [R] 00000000 00000000		INTPND10 [R] 00000000 00000000		
00C0A <sub>4H</sub> to 00C0A <sub>CH</sub>	Reserved		Reserved		
00C0B <sub>0H</sub>	MSGVAL20 [R] 00000000 00000000		MSGVAL10 [R] 00000000 00000000		
00C0B <sub>4H</sub> to 00C0F <sub>CH</sub>	Reserved		Reserved		
00C10 <sub>0H</sub> to 00E <sub>FFCH</sub>	Reserved				Reserved

# MB91460H Series

Address	Register				Block
	+0	+1	+2	+3	
00F00H	BCTRL [R/W] ----- 11111100 00000000				EDSU / MPU
00F04H	BSTAT [R/W] ----- 000 00000000 10 -- 000000				
00F08H	BIAC [R] ----- 00000000 00000000				
00F0CH	BOAC [R] ----- 00000000 00000000				
00F010H	BIRQ [R/W] ----- 00000000 00000000				
00F014H to 00F01CH	Reserved				
00F020H	BCR0 [R/W] ----- 00000000 00000000 00000000				
00F024H	BCR1 [R/W] ----- 00000000 00000000 00000000				
00F028H	BCR2 [R/W] ----- 00000000 00000000 00000000				
00F02CH	BCR3 [R/W] ----- 00000000 00000000 00000000				
00F030H to 00F07CH	Reserved				Reserved

# MB91460H Series

Address	Register				Block
	+0	+1	+2	+3	
00F080 <sub>H</sub>	BAD0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				EDSU / MPU
00F084 <sub>H</sub>	BAD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F088 <sub>H</sub>	BAD2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F08C <sub>H</sub>	BAD3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F090 <sub>H</sub>	BAD4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F094 <sub>H</sub>	BAD5 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F098 <sub>H</sub>	BAD6 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F09C <sub>H</sub>	BAD7 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0A0 <sub>H</sub>	BAD8 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0A4 <sub>H</sub>	BAD9 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0A8 <sub>H</sub>	BAD10 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0AC <sub>H</sub>	BAD11 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0B0 <sub>H</sub>	BAD12 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0B4 <sub>H</sub>	BAD13 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0B8 <sub>H</sub>	BAD14 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0BC <sub>H</sub>	BAD15 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0C0 <sub>H</sub> to 01FFFC <sub>H</sub>	Reserved				EDSU / MPU
020000 <sub>H</sub> to 02FFFC <sub>H</sub>	D-RAM size is 16 Kbytes : 02C000 <sub>H</sub> - 02FFFC <sub>H</sub> (data access is 0 wait cycles)				D-RAM area
030000 <sub>H</sub> to 03FFFC <sub>H</sub>	ID-RAM size is 16 Kbytes : 030000 <sub>H</sub> - 03FFFC <sub>H</sub> (instruction access is 0 wait cycles, data access is 1 wait cycle)				ID-RAM area

\*1 : depends on the number of available CAN channels

\*2 : ACR0 [11 : 10] depends on Mode vector fetch information on bus width

\*3 : TCR [3 : 0] INIT value = 0000, keeps value after RST

# MB91460H Series

## 2. Flash memory and external bus area

### 2.1. MB91F464HB

32bit read	dat[31:0]				dat[31:0]				
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
Address	Register								Block
	+ 0	+ 1	+ 2	+ 3	+ 4	+ 5	+ 6	+ 7	
040000 <sub>H</sub> to 05FFF8 <sub>H</sub>	Reserved				Reserved				ROMS0
060000 <sub>H</sub> to 07FFF8 <sub>H</sub>	Reserved				Reserved				ROMS1
080000 <sub>H</sub> to 09FFF8 <sub>H</sub>	Reserved				Reserved				ROMS2
0A0000 <sub>H</sub> to 0BFFF8 <sub>H</sub>	SA14 (64KB)				SA15 (64KB)				ROMS3
0C0000 <sub>H</sub> to 0DFFF8 <sub>H</sub>	SA16 (64KB)				SA17 (64KB)				ROMS4
0E0000 <sub>H</sub> to 0FFFF0 <sub>H</sub>	SA18 (64KB)				SA19 (64KB)				ROMS5
0FFFF8 <sub>H</sub>	FMV [R] 06 00 00 00 <sub>H</sub>				FRV [R] 00 00 BF F8 <sub>H</sub>				
100000 <sub>H</sub> to 11FFF8 <sub>H</sub>	External Bus Area								ROMS6
120000 <sub>H</sub> to 13FFF8 <sub>H</sub>									
140000 <sub>H</sub> to 143FF8 <sub>H</sub>	External Bus Area								ROMS7
144000 <sub>H</sub> to 17FF8 <sub>H</sub>									
148000 <sub>H</sub> to 14BFF8 <sub>H</sub>	SA4 (8KB)				SA5 (8KB)				
14C000 <sub>H</sub> to 14FFF8 <sub>H</sub>	SA6 (8KB)				SA7 (8KB)				
150000 <sub>H</sub> to 17FFF8 <sub>H</sub>	Reserved								

(Continued)

# MB91460H Series

(Continued)

32bit read	dat[31:0]				dat[31:0]				Block
	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
16bit read/write	Register								Block
	+ 0	+ 1	+ 2	+ 3	+ 4	+ 5	+ 6	+ 7	
18000H to 1BFFF8H	External Bus Area								ROMS8
1C000H to 1FFFF8H									ROMS9
20000H to 27FFF8H									ROMS10
28000H to 2FFFF8H									ROMS11
30000H to 37FFF8H									ROMS12
38000H to 3FFFF8H									ROMS13
40000H to 47FFF8H									ROMS14
48000H to 4FFFF8H									ROMS15

Note: Write operations to address 0FFFF8H and 0FFFC8H are not possible. When reading these addresses, the values shown above will be read.

# MB91460H Series

## ■ INTERRUPT VECTOR TABLE

Interrupt	Interrupt number		Interrupt level *1		Interrupt vector *2		DMA Resource number
	Decimal	Hexadecimal	Setting Register	Register address	Offset	Default vector address	
Reset	0	00	—	—	3FC <sub>H</sub>	000FFFFC <sub>H</sub>	—
Mode vector	1	01	—	—	3F8 <sub>H</sub>	000FFF8 <sub>H</sub>	—
System reserved	2	02	—	—	3F4 <sub>H</sub>	000FFF4 <sub>H</sub>	—
System reserved	3	03	—	—	3F0 <sub>H</sub>	000FFF0 <sub>H</sub>	—
System reserved	4	04	—	—	3EC <sub>H</sub>	000FFFE <sub>H</sub>	—
CPU supervisor mode (INT #5 instruction) *5	5	05	—	—	3E8 <sub>H</sub>	000FFFE8 <sub>H</sub>	—
Memory Protection exception *5	6	06	—	—	3E4 <sub>H</sub>	000FFFE4 <sub>H</sub>	—
System reserved	7	07	—	—	3E0 <sub>H</sub>	000FFFE0 <sub>H</sub>	—
System reserved	8	08	—	—	3DC <sub>H</sub>	000FFFD <sub>H</sub>	—
System reserved	9	09	—	—	3D8 <sub>H</sub>	000FFFD8 <sub>H</sub>	—
System reserved	10	0A	—	—	3D4 <sub>H</sub>	000FFFD4 <sub>H</sub>	—
System reserved	11	0B	—	—	3D0 <sub>H</sub>	000FFFD0 <sub>H</sub>	—
System reserved	12	0C	—	—	3CC <sub>H</sub>	000FFFC <sub>H</sub>	—
System reserved	13	0D	—	—	3C8 <sub>H</sub>	000FFFC8 <sub>H</sub>	—
Undefined instruction exception	14	0E	—	—	3C4 <sub>H</sub>	000FFFC4 <sub>H</sub>	—
NMI request	15	0F	F <sub>H</sub> fixed		3C0 <sub>H</sub>	000FFFC0 <sub>H</sub>	—
External Interrupt 0	16	10	ICR00	440 <sub>H</sub>	3BC <sub>H</sub>	000FFFBC <sub>H</sub>	0, 16
External Interrupt 1	17	11			3B8 <sub>H</sub>	000FFFB8 <sub>H</sub>	1, 17
External Interrupt 2	18	12	ICR01	441 <sub>H</sub>	3B4 <sub>H</sub>	000FFFB4 <sub>H</sub>	2, 18
External Interrupt 3	19	13			3B0 <sub>H</sub>	000FFFB0 <sub>H</sub>	3, 19
External Interrupt 4	20	14	ICR02	442 <sub>H</sub>	3AC <sub>H</sub>	000FFFAC <sub>H</sub>	20
External Interrupt 5	21	15			3A8 <sub>H</sub>	000FFFA8 <sub>H</sub>	21
External Interrupt 6	22	16	ICR03	443 <sub>H</sub>	3A4 <sub>H</sub>	000FFFA4 <sub>H</sub>	22
External Interrupt 7	23	17			3A0 <sub>H</sub>	000FFFA0 <sub>H</sub>	23
External Interrupt 8	24	18	ICR04	444 <sub>H</sub>	39C <sub>H</sub>	000FFF9C <sub>H</sub>	—
External Interrupt 9	25	19			398 <sub>H</sub>	000FFF98 <sub>H</sub>	—
External Interrupt 10	26	1A	ICR05	445 <sub>H</sub>	394 <sub>H</sub>	000FFF94 <sub>H</sub>	—
External Interrupt 11	27	1B			390 <sub>H</sub>	000FFF90 <sub>H</sub>	—
External Interrupt 12	28	1C	ICR06	446 <sub>H</sub>	38C <sub>H</sub>	000FFF8C <sub>H</sub>	—
External Interrupt 13	29	1D			388 <sub>H</sub>	000FFF88 <sub>H</sub>	—
External Interrupt 14	30	1E	ICR07	447 <sub>H</sub>	384 <sub>H</sub>	000FFF84 <sub>H</sub>	—
External Interrupt 15	31	1F			380 <sub>H</sub>	000FFF80 <sub>H</sub>	—

# MB91460H Series

Interrupt	Interrupt number		Interrupt level *1		Interrupt vector *2		DMA Resource number
	Decimal	Hexadecimal	Setting Register	Register address	Offset	Default vector address	
Reload Timer 0	32	20	ICR08	448 <sub>H</sub>	37 <sub>C<sub>H</sub></sub>	000FFF7C <sub>H</sub>	4, 32
Reload Timer 1	33	21			378 <sub>H</sub>	000FFF78 <sub>H</sub>	5, 33
Reload Timer 2	34	22	ICR09	449 <sub>H</sub>	374 <sub>H</sub>	000FFF74 <sub>H</sub>	34
Reload Timer 3	35	23			370 <sub>H</sub>	000FFF70 <sub>H</sub>	35
Reload Timer 4	36	24	ICR10	44A <sub>H</sub>	36 <sub>C<sub>H</sub></sub>	000FFF6C <sub>H</sub>	36
Reload Timer 5	37	25			368 <sub>H</sub>	000FFF68 <sub>H</sub>	37
Reload Timer 6	38	26	ICR11	44B <sub>H</sub>	364 <sub>H</sub>	000FFF64 <sub>H</sub>	38
Reload Timer 7	39	27			360 <sub>H</sub>	000FFF60 <sub>H</sub>	39
Free Run Timer 0	40	28	ICR12	44C <sub>H</sub>	35 <sub>C<sub>H</sub></sub>	000FFF5C <sub>H</sub>	40
Free Run Timer 1	41	29			358 <sub>H</sub>	000FFF58 <sub>H</sub>	41
Free Run Timer 2	42	2A	ICR13	44D <sub>H</sub>	354 <sub>H</sub>	000FFF54 <sub>H</sub>	42
Free Run Timer 3	43	2B			350 <sub>H</sub>	000FFF50 <sub>H</sub>	43
Free Run Timer 4	44	2C	ICR14	44E <sub>H</sub>	34 <sub>C<sub>H</sub></sub>	000FFF4C <sub>H</sub>	44
Free Run Timer 5	45	2D			348 <sub>H</sub>	000FFF48 <sub>H</sub>	45
Free Run Timer 6	46	2E	ICR15	44F <sub>H</sub>	344 <sub>H</sub>	000FFF44 <sub>H</sub>	46
Free Run Timer 7	47	2F			340 <sub>H</sub>	000FFF40 <sub>H</sub>	47
CAN 0	48	30	ICR16	450 <sub>H</sub>	33 <sub>C<sub>H</sub></sub>	000FFF3C <sub>H</sub>	—
Reserved	49	31			338 <sub>H</sub>	000FFF38 <sub>H</sub>	—
Reserved	50	32	ICR17	451 <sub>H</sub>	334 <sub>H</sub>	000FFF34 <sub>H</sub>	—
Reserved	51	33			330 <sub>H</sub>	000FFF30 <sub>H</sub>	—
Reserved	52	34	ICR18	452 <sub>H</sub>	32 <sub>C<sub>H</sub></sub>	000FFF2C <sub>H</sub>	—
Reserved	53	35			328 <sub>H</sub>	000FFF28 <sub>H</sub>	—
LIN-USART 0 RX	54	36	ICR19	453 <sub>H</sub>	324 <sub>H</sub>	000FFF24 <sub>H</sub>	6, 48
LIN-USART 0 TX	55	37			320 <sub>H</sub>	000FFF20 <sub>H</sub>	7, 49
Reserved	56	38	ICR20	454 <sub>H</sub>	31 <sub>C<sub>H</sub></sub>	000FFF1C <sub>H</sub>	8, 50
Reserved	57	39			318 <sub>H</sub>	000FFF18 <sub>H</sub>	9, 51
LIN-USART 2 RX	58	3A	ICR21	455 <sub>H</sub>	314 <sub>H</sub>	000FFF14 <sub>H</sub>	52
LIN-USART 2 TX	59	3B			310 <sub>H</sub>	000FFF10 <sub>H</sub>	53
LIN-USART 3 RX	60	3C	ICR22	456 <sub>H</sub>	30 <sub>C<sub>H</sub></sub>	000FFF0C <sub>H</sub>	54
LIN-USART 3 TX	61	3D			308 <sub>H</sub>	000FFF08 <sub>H</sub>	55
System Reserved	62	3E	ICR23 *3	457 <sub>H</sub>	304 <sub>H</sub>	000FFF04 <sub>H</sub>	—
Delayed Interrupt	63	3F			300 <sub>H</sub>	000FFF00 <sub>H</sub>	—
System Reserved *4	64	40	ICR24	458 <sub>H</sub>	2F <sub>C<sub>H</sub></sub>	000FFEFC <sub>H</sub>	—
System Reserved *4	65	41			2F8 <sub>H</sub>	000FFE8 <sub>H</sub>	—

# MB91460H Series

Interrupt	Interrupt number		Interrupt level *1		Interrupt vector *2		DMA Resource number
	Decimal	Hexadecimal	Setting Register	Register address	Offset	Default vector address	
LIN-USART (FIFO) 4 RX	66	42	ICR25	459 <sub>H</sub>	2F4 <sub>H</sub>	000FFEF4 <sub>H</sub>	10, 56
LIN-USART (FIFO) 4 TX	67	43			2F0 <sub>H</sub>	000FFEF0 <sub>H</sub>	11, 57
LIN-USART (FIFO) 5 RX	68	44	ICR26	45A <sub>H</sub>	2EC <sub>H</sub>	000FFEEC <sub>H</sub>	12, 58
LIN-USART (FIFO) 5 TX	69	45			2E8 <sub>H</sub>	000FFEE8 <sub>H</sub>	13, 59
LIN-USART (FIFO) 6 RX	70	46	ICR27	45B <sub>H</sub>	2E4 <sub>H</sub>	000FFEE4 <sub>H</sub>	60
LIN-USART (FIFO) 6 TX	71	47			2E0 <sub>H</sub>	000FFEE0 <sub>H</sub>	61
LIN-USART (FIFO) 7 RX	72	48	ICR28	45C <sub>H</sub>	2DC <sub>H</sub>	000FFEDC <sub>H</sub>	62
LIN-USART (FIFO) 7 TX	73	49			2D8 <sub>H</sub>	000FFED8 <sub>H</sub>	63
I <sup>2</sup> C 0	74	4A	ICR29	45D <sub>H</sub>	2D4 <sub>H</sub>	000FFED4 <sub>H</sub>	—
I <sup>2</sup> C 1	75	4B			2D0 <sub>H</sub>	000FFED0 <sub>H</sub>	—
Reserved	76	4C	ICR30	45E <sub>H</sub>	2CC <sub>H</sub>	000FFEC <sub>H</sub>	64
Reserved	77	4D			2C8 <sub>H</sub>	000FFEC8 <sub>H</sub>	65
Reserved	78	4E	ICR31	45F <sub>H</sub>	2C4 <sub>H</sub>	000FFEC4 <sub>H</sub>	66
Reserved	79	4F			2C0 <sub>H</sub>	000FFEC0 <sub>H</sub>	67
Reserved	80	50	ICR32	460 <sub>H</sub>	2BC <sub>H</sub>	000FFEB <sub>H</sub>	68
Reserved	81	51			2B8 <sub>H</sub>	000FFEB8 <sub>H</sub>	69
Reserved	82	52	ICR33	461 <sub>H</sub>	2B4 <sub>H</sub>	000FFEB4 <sub>H</sub>	70
Reserved	83	53			2B0 <sub>H</sub>	000FFEB0 <sub>H</sub>	71
Reserved	84	54	ICR34	462 <sub>H</sub>	2AC <sub>H</sub>	000FFEAC <sub>H</sub>	72
Reserved	85	55			2A8 <sub>H</sub>	000FFE8 <sub>H</sub>	73
Reserved	86	56	ICR35	463 <sub>H</sub>	2A4 <sub>H</sub>	000FFE4 <sub>H</sub>	74
Reserved	87	57			2A0 <sub>H</sub>	000FFE0 <sub>H</sub>	75
Reserved	88	58	ICR36	464 <sub>H</sub>	29C <sub>H</sub>	000FFE9 <sub>H</sub>	76
Reserved	89	59			298 <sub>H</sub>	000FFE98 <sub>H</sub>	77
Reserved	90	5A	ICR37	465 <sub>H</sub>	294 <sub>H</sub>	000FFE94 <sub>H</sub>	78
Reserved	91	5B			290 <sub>H</sub>	000FFE90 <sub>H</sub>	79
Input Capture 0	92	5C	ICR38	466 <sub>H</sub>	28C <sub>H</sub>	000FFE8 <sub>H</sub>	80
Input Capture 1	93	5D			288 <sub>H</sub>	000FFE88 <sub>H</sub>	81
Input Capture 2	94	5E	ICR39	467 <sub>H</sub>	284 <sub>H</sub>	000FFE84 <sub>H</sub>	82
Input Capture 3	95	5F			280 <sub>H</sub>	000FFE80 <sub>H</sub>	83
Input Capture 4	96	60	ICR40	468 <sub>H</sub>	27C <sub>H</sub>	000FFE7 <sub>H</sub>	84
Input Capture 5	97	61			278 <sub>H</sub>	000FFE78 <sub>H</sub>	85
Input Capture 6	98	62	ICR41	469 <sub>H</sub>	274 <sub>H</sub>	000FFE74 <sub>H</sub>	86
Input Capture 7	99	63			270 <sub>H</sub>	000FFE70 <sub>H</sub>	87

# MB91460H Series

Interrupt	Interrupt number		Interrupt level *1		Interrupt vector *2		DMA Resource number
	Decimal	Hexadecimal	Setting Register	Register address	Offset	Default vector address	
Output Compare 0	100	64	ICR42	46A <sub>H</sub>	26C <sub>H</sub>	000FFE6C <sub>H</sub>	88
Output Compare 1	101	65			268 <sub>H</sub>	000FFE68 <sub>H</sub>	89
Output Compare 2	102	66	ICR43	46B <sub>H</sub>	264 <sub>H</sub>	000FFE64 <sub>H</sub>	90
Output Compare 3	103	67			260 <sub>H</sub>	000FFE60 <sub>H</sub>	91
Output Compare 4	104	68	ICR44	46C <sub>H</sub>	25C <sub>H</sub>	000FFE5C <sub>H</sub>	92
Output Compare 5	105	69			258 <sub>H</sub>	000FFE58 <sub>H</sub>	93
Output Compare 6	106	6A	ICR45	46D <sub>H</sub>	254 <sub>H</sub>	000FFE54 <sub>H</sub>	94
Output Compare 7	107	6B			250 <sub>H</sub>	000FFE50 <sub>H</sub>	95
Sound Generator	108	6C	ICR46	46E <sub>H</sub>	24C <sub>H</sub>	000FFE4C <sub>H</sub>	—
Reserved	109	6D			248 <sub>H</sub>	000FFE48 <sub>H</sub>	—
System Reserved	110	6E	ICR47 *3	46F <sub>H</sub>	244 <sub>H</sub>	000FFE44 <sub>H</sub>	—
System Reserved	111	6F			240 <sub>H</sub>	000FFE40 <sub>H</sub>	—
PPG 0	112	70	ICR48	470 <sub>H</sub>	23C <sub>H</sub>	000FFE3C <sub>H</sub>	15, 96
PPG 1	113	71			238 <sub>H</sub>	000FFE38 <sub>H</sub>	97
PPG 2	114	72	ICR49	471 <sub>H</sub>	234 <sub>H</sub>	000FFE34 <sub>H</sub>	98
PPG 3	115	73			230 <sub>H</sub>	000FFE30 <sub>H</sub>	99
PPG 4	116	74	ICR50	472 <sub>H</sub>	22C <sub>H</sub>	000FFE2C <sub>H</sub>	100
PPG 5	117	75			228 <sub>H</sub>	000FFE28 <sub>H</sub>	101
PPG 6	118	76	ICR51	473 <sub>H</sub>	224 <sub>H</sub>	000FFE24 <sub>H</sub>	102
PPG 7	119	77			220 <sub>H</sub>	000FFE20 <sub>H</sub>	103
PPG 8	120	78	ICR52	474 <sub>H</sub>	21C <sub>H</sub>	000FFE1C <sub>H</sub>	104
PPG 9	121	79			218 <sub>H</sub>	000FFE18 <sub>H</sub>	105
PPG 10	122	7A	ICR53	475 <sub>H</sub>	214 <sub>H</sub>	000FFE14 <sub>H</sub>	106
PPG 11	123	7B			210 <sub>H</sub>	000FFE10 <sub>H</sub>	107
PPG 12	124	7C	ICR54	476 <sub>H</sub>	20C <sub>H</sub>	000FFE0C <sub>H</sub>	108
PPG 13	125	7D			208 <sub>H</sub>	000FFE08 <sub>H</sub>	109
PPG 14	126	7E	ICR55	477 <sub>H</sub>	204 <sub>H</sub>	000FFE04 <sub>H</sub>	110
PPG 15	127	7F			200 <sub>H</sub>	000FFE00 <sub>H</sub>	111
Up/Down Counter 0	128	80	ICR56	478 <sub>H</sub>	1FC <sub>H</sub>	000FFDFC <sub>H</sub>	—
Up/Down Counter 1	129	81			1F8 <sub>H</sub>	000FFDF8 <sub>H</sub>	—
Reserved	130	82	ICR57	479 <sub>H</sub>	1F4 <sub>H</sub>	000FFDF4 <sub>H</sub>	—
Reserved	131	83			1F0 <sub>H</sub>	000FFDF0 <sub>H</sub>	—
Real Time Clock	132	84	ICR58	47A <sub>H</sub>	1EC <sub>H</sub>	000FFDEC <sub>H</sub>	—
Calibration Unit	133	85			1E8 <sub>H</sub>	000FFDE8 <sub>H</sub>	—

# MB91460H Series

Interrupt	Interrupt number		Interrupt level *1		Interrupt vector *2		DMA Resource number
	Decimal	Hexadecimal	Setting Register	Register address	Offset	Default vector address	
A/D Converter 0	134	86	ICR59	47BH	1E4H	000FFDE4H	14, 112
System reserved	135	87			1E0H	000FFDE0H	—
Alarm Comparator 0	136	88	ICR60	47CH	1DC <sub>H</sub>	000FFDDC <sub>H</sub>	—
Reserved	137	89			1D8 <sub>H</sub>	000FFDD8 <sub>H</sub>	—
Low Voltage Detection	138	8A	ICR61	47DH	1D4 <sub>H</sub>	000FFDD4 <sub>H</sub>	—
Reserved	139	8B			1D0 <sub>H</sub>	000FFDD0 <sub>H</sub>	—
Time base Overflow	140	8C	ICR62	47EH	1CC <sub>H</sub>	000FFDCC <sub>H</sub>	—
PLL Clock Gear	141	8D			1C8 <sub>H</sub>	000FFDC8 <sub>H</sub>	—
DMA Controller	142	8E	ICR63	47FH	1C4 <sub>H</sub>	000FFDC4 <sub>H</sub>	—
Main/Sub OSC stability wait	143	8F			1C0 <sub>H</sub>	000FFDC0 <sub>H</sub>	—
Security vector	144	90	—	—	1BC <sub>H</sub>	000FFDBC <sub>H</sub>	—
Used by the INT instruction.	145 to 255	91 to FF	—	—	1B8 <sub>H</sub> to 000 <sub>H</sub>	000FFDB8 <sub>H</sub> to 000FFC00 <sub>H</sub>	—

\*1 : The Interrupt Control Registers (ICRs) are located in the interrupt controller and set the interrupt level for each interrupt request. An ICR is provided for each interrupt request.

\*2 : The vector address for each EIT (exception, interrupt or trap) is calculated by adding the listed offset to the table base register value (TBR) . The TBR specifies the top of the EIT vector table. The addresses listed in the table are for the default TBR value (000FFC00<sub>H</sub>) . The TBR is initialized to this value by a reset. The TBR is set to 000FFC00<sub>H</sub> after the internal boot ROM is executed.

\*3 : ICR23 and ICR47 can be exchanged by setting the REALOS compatibility bit (addr 0C03<sub>H</sub> : IOS[0])

\*4 : Used by REALOS

\*5 : Memory Protection Unit (MPU) support

## ■ RECOMMENDED SETTINGS

### 1. PLL and Clockgear settings

Please note that for MB91F464HB the core base clock frequencies are valid in the 1.8V operation mode of the Main regulator and Flash .

#### Recommended PLL divider and clockgear settings

PLL Input (CLK) [MHz]	Frequency Parameter		Clockgear Parameter		PLL Output (X) [MHz]	Core Base Clock [MHz]	Remarks
	DIVM	DIVN	DIVG	MULG	MULG		
4	2	25	16	24	200	100	
4	2	24	16	24	192	96	
4	2	23	16	24	184	92	
4	2	22	16	24	176	88	
4	2	21	16	20	168	84	
4	2	20	16	20	160	80	
4	2	19	16	20	152	76	
4	2	18	16	20	144	72	
4	2	17	16	16	136	68	
4	2	16	16	16	128	64	
4	2	15	16	16	120	60	
4	2	14	16	16	112	56	
4	2	13	16	12	104	52	
4	2	12	16	12	96	48	
4	2	11	16	12	88	44	
4	4	10	16	24	160	40	
4	4	9	16	24	144	36	
4	4	8	16	24	128	32	
4	4	7	16	24	112	28	
4	6	6	16	24	144	24	
4	8	5	16	28	160	20	
4	10	4	16	32	160	16	
4	12	3	16	32	144	12	

# MB91460H Series

## 2. Clock Modulator settings

The following table shows all possible settings for the Clock Modulator in a base clock frequency range from 32MHz up to 88MHz.

The Flash access time settings need to be adjusted according to Fmax while the PLL and clockgear settings should be set according to base clock frequency.

### Clock Modulator settings, frequency range and supported supply voltage

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]
1	3	026F	88	79.5	98.5
1	3	026F	84	76.1	93.8
1	3	026F	80	72.6	89.1
1	5	02AE	80	68.7	95.8
2	3	046E	80	68.7	95.8
1	3	026F	76	69.1	84.5
1	5	02AE	76	65.3	90.8
1	7	02ED	76	62	98.1
2	3	046E	76	65.3	90.8
3	3	066D	76	62	98.1
1	3	026F	72	65.5	79.9
1	5	02AE	72	62	85.8
1	7	02ED	72	58.8	92.7
2	3	046E	72	62	85.8
3	3	066D	72	58.8	92.7
1	3	026F	68	62	75.3
1	5	02AE	68	58.7	80.9
1	7	02ED	68	55.7	87.3
1	9	032C	68	53	95
2	3	046E	68	58.7	80.9
2	5	04AC	68	53	95
3	3	066D	68	55.7	87.3
4	3	086C	68	53	95
1	3	026F	64	58.5	70.7
1	5	02AE	64	55.3	75.9
1	7	02ED	64	52.5	82
1	9	032C	64	49.9	89.1
1	11	036B	64	47.6	97.6
2	3	046E	64	55.3	75.9
2	5	04AC	64	49.9	89.1

# MB91460H Series

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]
3	3	066D	64	52.5	82
4	3	086C	64	49.9	89.1
5	3	0A6B	64	47.6	97.6
1	3	026F	60	54.9	66.1
1	5	02AE	60	51.9	71
1	7	02ED	60	49.3	76.7
1	9	032C	60	46.9	83.3
1	11	036B	60	44.7	91.3
2	3	046E	60	51.9	71
2	5	04AC	60	46.9	83.3
3	3	066D	60	49.3	76.7
4	3	086C	60	46.9	83.3
5	3	0A6B	60	44.7	91.3
1	3	026F	56	51.4	61.6
1	5	02AE	56	48.6	66.1
1	7	02ED	56	46.1	71.4
1	9	032C	56	43.8	77.6
1	11	036B	56	41.8	84.9
1	13	03AA	56	39.9	93.8
2	3	046E	56	48.6	66.1
2	5	04AC	56	43.8	77.6
2	7	04EA	56	39.9	93.8
3	3	066D	56	46.1	71.4
3	5	06AA	56	39.9	93.8
4	3	086C	56	43.8	77.6
5	3	0A6B	56	41.8	84.9
6	3	0C6A	56	39.9	93.8
1	3	026F	52	47.8	57
1	5	02AE	52	45.2	61.2
1	7	02ED	52	42.9	66.1
1	9	032C	52	40.8	71.8
1	11	036B	52	38.8	78.6
1	13	03AA	52	37.1	86.8
1	15	03E9	52	35.5	96.9
2	3	046E	52	45.2	61.2
2	5	04AC	52	40.8	71.8

# MB91460H Series

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]
2	7	04EA	52	37.1	86.8
3	3	066D	52	42.9	66.1
3	5	06AA	52	37.1	86.8
4	3	086C	52	40.8	71.8
5	3	0A6B	52	38.8	78.6
6	3	0C6A	52	37.1	86.8
7	3	0E69	52	35.5	96.9
1	3	026F	48	44.2	52.5
1	5	02AE	48	41.8	56.4
1	7	02ED	48	39.6	60.9
1	9	032C	48	37.7	66.1
1	11	036B	48	35.9	72.3
1	13	03AA	48	34.3	79.9
1	15	03E9	48	32.8	89.1
2	3	046E	48	41.8	56.4
2	5	04AC	48	37.7	66.1
2	7	04EA	48	34.3	79.9
3	3	066D	48	39.6	60.9
3	5	06AA	48	34.3	79.9
4	3	086C	48	37.7	66.1
5	3	0A6B	48	35.9	72.3
6	3	0C6A	48	34.3	79.9
7	3	0E69	48	32.8	89.1
1	3	026F	44	40.6	48.1
1	5	02AE	44	38.4	51.6
1	7	02ED	44	36.4	55.7
1	9	032C	44	34.6	60.4
1	11	036B	44	33	66.1
1	13	03AA	44	31.5	73
1	15	03E9	44	30.1	81.4
2	3	046E	44	38.4	51.6
2	5	04AC	44	34.6	60.4
2	7	04EA	44	31.5	73
2	9	0528	44	28.9	92.1
3	3	066D	44	36.4	55.7
3	5	06AA	44	31.5	73

# MB91460H Series

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]
4	3	086C	44	34.6	60.4
4	5	08A8	44	28.9	92.1
5	3	0A6B	44	33	66.1
6	3	0C6A	44	31.5	73
7	3	0E69	44	30.1	81.4
8	3	1068	44	28.9	92.1
1	3	026F	40	37	43.6
1	5	02AE	40	34.9	46.8
1	7	02ED	40	33.1	50.5
1	9	032C	40	31.5	54.8
1	11	036B	40	30	59.9
1	13	03AA	40	28.7	66.1
1	15	03E9	40	27.4	73.7
2	3	046E	40	34.9	46.8
2	5	04AC	40	31.5	54.8
2	7	04EA	40	28.7	66.1
2	9	0528	40	26.3	83.3
3	3	066D	40	33.1	50.5
3	5	06AA	40	28.7	66.1
3	7	06E7	40	25.3	95.8
4	3	086C	40	31.5	54.8
4	5	08A8	40	26.3	83.3
5	3	0A6B	40	30	59.9
6	3	0C6A	40	28.7	66.1
7	3	0E69	40	27.4	73.7
8	3	1068	40	26.3	83.3
9	3	1267	40	25.3	95.8
1	3	026F	36	33.3	39.2
1	5	02AE	36	31.5	42
1	7	02ED	36	29.9	45.3
1	9	032C	36	28.4	49.2
1	11	036B	36	27.1	53.8
1	13	03AA	36	25.8	59.3
1	15	03E9	36	24.7	66.1
2	3	046E	36	31.5	42
2	5	04AC	36	28.4	49.2

# MB91460H Series

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]
2	7	04EA	36	25.8	59.3
2	9	0528	36	23.7	74.7
3	3	066D	36	29.9	45.3
3	5	06AA	36	25.8	59.3
3	7	06E7	36	22.8	85.8
4	3	086C	36	28.4	49.2
4	5	08A8	36	23.7	74.7
5	3	0A6B	36	27.1	53.8
6	3	0C6A	36	25.8	59.3
7	3	0E69	36	24.7	66.1
8	3	1068	36	23.7	74.7
9	3	1267	36	22.8	85.8
1	3	026F	32	29.7	34.7
1	5	02AE	32	28	37.3
1	7	02ED	32	26.6	40.2
1	9	032C	32	25.3	43.6
1	11	036B	32	24.1	47.7
1	13	03AA	32	23	52.5
1	15	03E9	32	22	58.6
2	3	046E	32	28	37.3
2	5	04AC	32	25.3	43.6
2	7	04EA	32	23	52.5
2	9	0528	32	21.1	66.1
2	11	0566	32	19.5	89.1
3	3	066D	32	26.6	40.2
3	5	06AA	32	23	52.5
3	7	06E7	32	20.3	75.9
4	3	086C	32	25.3	43.6
4	5	08A8	32	21.1	66.1
5	3	0A6B	32	24.1	47.7
5	5	0AA6	32	19.5	89.1
6	3	0C6A	32	23	52.5
7	3	0E69	32	22	58.6
8	3	1068	32	21.1	66.1
9	3	1267	32	20.3	75.9
10	3	1466	32	19.5	89.1

## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute maximum ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply slew rate	—	—	50	V/ms	
Power supply voltage 1*1	V <sub>DD5R</sub>	- 0.3	+ 6.0	V	
Power supply voltage 2*1	V <sub>DD5</sub>	- 0.3	+ 6.0	V	
Relationship of the supply voltages	AV <sub>CC5</sub>	V <sub>DD5</sub> -0.3 V <sub>DD35</sub> -0.3	V <sub>DD5</sub> +0.3 V <sub>DD35</sub> +0.3	V	At least one pin of the Ports 26 to 29 (ANn) is used as digital input or output.
		V <sub>SS5</sub> -0.3 V <sub>DD35</sub> -0.3	V <sub>DD5</sub> +0.3 V <sub>DD35</sub> +0.3	V	All pins of the Ports 26 to 29 (ANn) follow the condition of V <sub>IA</sub> .
Analog power supply voltage*1	AV <sub>CC5</sub>	- 0.3	+ 6.0	V	*2
Analog reference power supply voltage*1	AVRH	- 0.3	+ 6.0	V	*2
Input voltage 1*1	V <sub>I1</sub>	V <sub>SS5</sub> - 0.3	V <sub>DD5</sub> + 0.3	V	
Analog pin input voltage*1	V <sub>IA</sub>	AV <sub>SS5</sub> - 0.3	AV <sub>CC5</sub> + 0.3	V	
Output voltage 1*1	V <sub>O1</sub>	V <sub>SS5</sub> - 0.3	V <sub>DD5</sub> + 0.3	V	
Maximum clamp current	I <sub>CLAMP</sub>	- 4.0	+ 4.0	mA	*3
Total maximum clamp current	Σ  I <sub>CLAMP</sub>	—	20	mA	*3
“L” level maximum output current*4	I <sub>OL</sub>	—	10	mA	
“L” level average output current*5	I <sub>OLAV</sub>	—	8	mA	
“L” level total maximum output current	ΣI <sub>OL</sub>	—	100	mA	
“L” level total average output current*6	ΣI <sub>OLAV</sub>	—	50	mA	
“H” level maximum output current*4	I <sub>OH</sub>	—	- 10	mA	
“H” level average output current*5	I <sub>OHAV</sub>	—	- 4	mA	
“H” level total maximum output current	ΣI <sub>OH</sub>	—	- 100	mA	
“H” level total average output current*6	ΣI <sub>OHAV</sub>	—	- 25	mA	
Power consumption	P <sub>D</sub>	—	600	mW	at T <sub>A</sub> = 105°C
Operating temperature	T <sub>A</sub>	- 40	+ 105	°C	
Storage temperature	T <sub>stg</sub>	- 55	+ 150	°C	

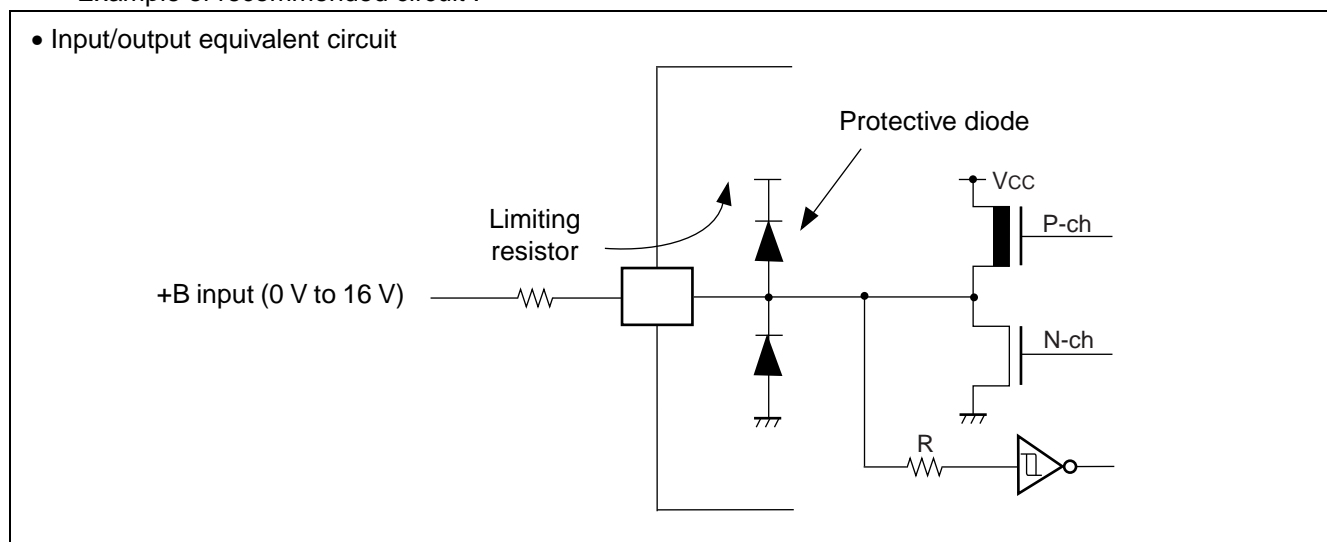
\*1 : The parameter is based on V<sub>SS5</sub> = AV<sub>SS5</sub> = 0.0 V.

# MB91460H Series

\*2 :  $AV_{CC5}$  and  $AVRH5$  must not exceed  $V_{DD5} + 0.3$  V.

\*3 : • Use within recommended operating conditions.

- Use with DC voltage (current).
- +B signals are input signals that exceed the  $V_{DD5}$  voltage. +B signals should always be applied by connecting a limiting resistor between the +B signal and the microcontroller.
- The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed the rated value at any time, either instantaneously or for an extended period, when the +B signal is input.
- Note that when the microcontroller drive current is low, such as in the low power consumption modes, the +B input potential can increase the potential at the power supply pin via a protective diode, possibly affecting other devices.
- Note that if the +B signal is input when the microcontroller is off (not fixed at 0 V), power is supplied through the +B input pin; therefore, the microcontroller may partially operate.
- Note that if the +B signal is input at power-on, since the power is supplied through the pin, the power-on reset may not function in the power supply voltage.
- Do not leave +B input pins open.
- Example of recommended circuit :



\*4 : Maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

\*5 : Average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 100 ms period.

\*6 : Total average output current is defined as the value of the average current flowing through all of the corresponding pins for a 100 ms period.

**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## 2. Recommended operating conditions

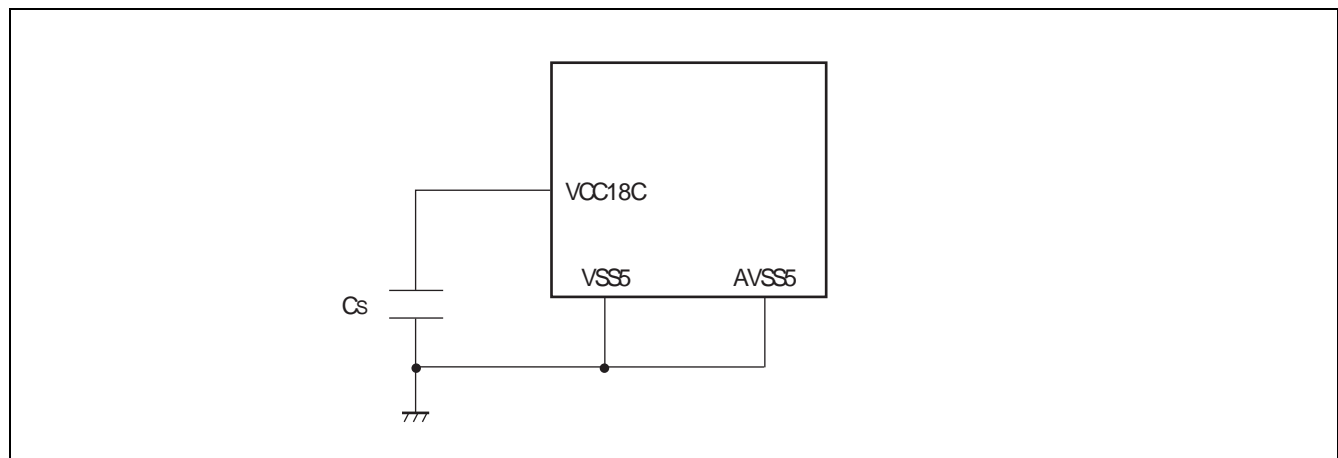
(V<sub>SS5</sub> = AV<sub>SS5</sub> = 0.0 V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V <sub>DD5</sub>	3.0	—	5.5	V	
	V <sub>DD5R</sub>	3.0	—	5.5	V	Internal regulator
	AV <sub>CC5</sub>	3.0	—	5.5	V	A/D converter
Smoothing capacitor at VCC18C pin	C <sub>s</sub>	—	4.7	—	μF	Use a X7R ceramic capacitor or a capacitor that has similar frequency characteristics.
Power supply slew rate		—	—	50	V/ms	
Operating temperature	T <sub>A</sub>	- 40	—	+ 105	°C	
Main Oscillation stabilisation time		10			ms	
Lock-up time PLL (4 MHz ->16 ...100MHz)				0.6	ms	
ESD Protection (Human body model)	V <sub>surge</sub>	2			kV	R <sub>discharge</sub> = 1.5kΩ C <sub>discharge</sub> = 100pF
RC Oscillator	f <sub>RC100kHz</sub>	50	100	200	kHz MHz	VDD <sub>CORE</sub> ≥ 1.65V
	f <sub>RC2MHz</sub>	1	2	4		

**WARNING:** The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.



# MB91460H Series

## 3. DC characteristics

( $V_{DD5} = AV_{CC5} = 3.0\text{ V to }5.5\text{ V}$ ,  $V_{SS5} = AV_{SS5} = 0\text{ V}$ ,  $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input "H" voltage	$V_{IH}$	—	Port inputs if CMOS Hysteresis 0.8/0.2 input is selected	$0.8 \times V_{DD}$	—	$V_{DD} + 0.3$	V	CMOS hysteresis input
		—	Port inputs if CMOS Hysteresis 0.7/0.3 input is selected	$0.7 \times V_{DD}$	—	$V_{DD} + 0.3$	V	$4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$
				$0.74 \times V_{DD}$	—	$V_{DD} + 0.3$	V	$3\text{ V} \leq V_{DD} < 4.5\text{ V}$
		—	AUTOMOTIVE Hysteresis input is selected	$0.8 \times V_{DD}$	—	$V_{DD} + 0.3$	V	
	—	Port inputs if TTL input is selected	2.0	—	$V_{DD} + 0.3$	V		
	$V_{IHR}$	INITX	—	$0.8 \times V_{DD}$	—	$V_{DD} + 0.3$	V	INITX input pin (CMOS Hysteresis)
	$V_{IHM}$	MD_3 to MD_0	—	$V_{DD} - 0.3$	—	$V_{DD} + 0.3$	V	Mode input pins
	$V_{IHX0S}$	X0, X0A	—	2.5	—	$V_{DD} + 0.3$	V	External clock in "Oscillation mode"
$V_{IHX0F}$	X0	—	$0.8 \times V_{DD}$	—	$V_{DD} + 0.3$	V	External clock in "Fast Clock Input mode"	
Input "L" voltage	$V_{IL}$	—	Port inputs if CMOS Hysteresis 0.8/0.2 input is selected	$V_{SS} - 0.3$	—	$0.2 \times V_{DD}$	V	
		—	Port inputs if CMOS Hysteresis 0.7/0.3 input is selected	$V_{SS} - 0.3$	—	$0.3 \times V_{DD}$	V	
		—	Port inputs if AUTOMOTIVE Hysteresis input is selected	$V_{SS} - 0.3$	—	$0.5 \times V_{DD}$	V	$4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$
				$V_{SS} - 0.3$	—	$0.46 \times V_{DD}$	V	$3\text{ V} \leq V_{DD} < 4.5\text{ V}$
	—	Port inputs if TTL input is selected	$V_{SS} - 0.3$	—	0.8	V		
	$V_{ILR}$	INITX	—	$V_{SS} - 0.3$	—	$0.2 \times V_{DD}$	V	INITX input pin (CMOS Hysteresis)
	$V_{ILM}$	MD_3 to MD_0	—	$V_{SS} - 0.3$	—	$V_{SS} + 0.3$	V	Mode input pins
	$V_{ILXDS}$	X0, X0A	—	$V_{SS} - 0.3$	—	0.5	V	External clock in "Oscillation mode"

# MB91460H Series

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input "L" voltage	V <sub>ILXDF</sub>	X0	—	V <sub>SS</sub> - 0.3	—	0.2 × V <sub>DD</sub>	V	External clock in "Fast Clock Input mode"
Output "H" voltage	V <sub>OH2</sub>	Normal outputs	4.5V ≤ V <sub>DD</sub> ≤ 5.5V, I <sub>OH</sub> = - 2mA	V <sub>DD</sub> - 0.5	—	—	V	Driving strength set to 2 mA
			3.0V ≤ V <sub>DD</sub> < 4.5V, I <sub>OH</sub> = - 1.6mA					
	V <sub>OH5</sub>	Normal outputs	4.5V ≤ V <sub>DD</sub> ≤ 5.5V, I <sub>OH</sub> = - 5mA	V <sub>DD</sub> - 0.5	—	—	V	Driving strength set to 5 mA
3.0V ≤ V <sub>DD</sub> < 4.5V, I <sub>OH</sub> = - 3mA								
V <sub>OH3</sub>	I <sup>2</sup> C outputs	3.0V ≤ V <sub>DD</sub> ≤ 5.5V, I <sub>OH</sub> = - 3mA	V <sub>DD</sub> - 0.5	—	—	V		
Output "L" voltage	V <sub>OL2</sub>	Normal outputs	4.5V ≤ V <sub>DD</sub> ≤ 5.5V, I <sub>OL</sub> = + 2mA	—	—	0.4	V	Driving strength set to 2 mA
			3.0V ≤ V <sub>DD</sub> < 4.5V, I <sub>OL</sub> = + 1.6mA					
	V <sub>OL5</sub>	Normal outputs	4.5V ≤ V <sub>DD</sub> ≤ 5.5V, I <sub>OL</sub> = + 5mA	—	—	0.4	V	Driving strength set to 5 mA
3.0V ≤ V <sub>DD</sub> < 4.5V, I <sub>OL</sub> = + 3mA								
V <sub>OL3</sub>	I <sup>2</sup> C outputs	3.0V ≤ V <sub>DD</sub> ≤ 5.5V, I <sub>OL</sub> = + 3mA	—	—	0.4	V		
Input leakage current	I <sub>IL</sub>	Pnn_m*1	3.0V ≤ V <sub>DD</sub> ≤ 5.5V V <sub>SS5</sub> < V <sub>I</sub> < V <sub>DD</sub> T <sub>A</sub> =25 °C	- 1	—	+ 1	μA	
			3.0V ≤ V <sub>DD</sub> ≤ 5.5V V <sub>SS5</sub> < V <sub>I</sub> < V <sub>DD</sub> T <sub>A</sub> =105 °C	- 3	—	+ 3		
Analog input leakage current	I <sub>AIN</sub>	ANn*2	3.0V ≤ V <sub>DD</sub> ≤ 5.5V T <sub>A</sub> =25 °C	- 1	—	+ 1	μA	
			3.0V ≤ V <sub>DD</sub> ≤ 5.5V T <sub>A</sub> =105 °C	- 3	—	+ 3	μA	
Pull-up resistance	R <sub>UP</sub>	Pnn_m*3	3.0V ≤ V <sub>DD</sub> ≤ 3.6V	40	100	160	kΩ	
		INITX	4.5V ≤ V <sub>DD</sub> ≤ 5.5V	25	50	100		
Pull-down resistance	R <sub>DOWN</sub>	Pnn_m*4	3.0V ≤ V <sub>DD</sub> ≤ 3.6V	40	100	180	kΩ	
			4.5V ≤ V <sub>DD</sub> ≤ 5.5V	25	50	100		

# MB91460H Series

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input capacitance	C <sub>IN</sub>	All except V <sub>DD5</sub> , V <sub>DD5R</sub> , V <sub>SS5</sub> , AV <sub>CC5</sub> , AV <sub>SS5</sub> , AVRH5	f = 1 MHz	-	5	15	pF	
Power supply current  MB91 F464HB	I <sub>CC</sub>	V <sub>DD5R</sub>	CLKB: 100 MHz CLKP: 50 MHz CLKT: 50 MHz CLKCAN: 50 MHz	-	100	130	mA	Code fetch from Flash
	I <sub>CCH</sub>	V <sub>DD5R</sub>	T <sub>A</sub> = +25 °C	-	30	150	μA	At stop mode *5
			T <sub>A</sub> = +105 °C	-	300	2000	μA	
			T <sub>A</sub> = +25 °C	-	100	500	μA	RTC : 4 MHz mode *5
			T <sub>A</sub> = +105 °C	-	500	2400	μA	
			T <sub>A</sub> = +25 °C	-	50	250	μA	
	T <sub>A</sub> = +105 °C	-	400	2200	μA			
	I <sub>LVE</sub>	V <sub>DD5</sub>	—	—	70	150	μA	External low voltage detection
	I <sub>LVI</sub>	V <sub>DD5R</sub>	—	—	50	100	μA	Internal low voltage detection
	I <sub>OSC</sub>	V <sub>DD5</sub>	-	-	250	500	μA	Main clock (4 MHz)
-			-	20	40	μA	Sub clock (32 kHz)	

1. Pnn\_m includes all GPIO pins. Analog (AN) channels and PullUp/PullDown are disabled.
2. ANn includes all pins where AN channels are enabled.
3. Pnn\_m includes all GPIO pins. The pull up resistors must be enabled by PPER/PPCR setting and the pins must be in input direction.
4. Pnn\_m includes all GPIO pins. The pull down resistors must be enabled by PPER/PPCR setting and the pins must be in input direction.

## 4. A/D converter characteristics

( $V_{DD5} = AV_{CC5} = 3.0\text{ V to }5.5\text{ V}$ ,  $V_{SS5} = AV_{SS5} = 0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C to }+105\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	-3	—	+3	LSB	
Nonlinearity error	—	—	-2.5	—	+2.5	LSB	
Differential nonlinearity error	—	—	-1.9	—	+1.9	LSB	
Zero reading voltage	$V_{OT}$	ANn	AVRL-1.5 LSB	AVRL + 0.5 LSB	AVRL + 2.5 LSB	V	
Full scale reading voltage	$V_{FST}$	ANn	AVRH-3.5 LSB	AVRH-1.5 LSB	AVRH + 0.5 LSB	V	
Compare time	$T_{comp}$	—	0.6	—	16,500	$\mu\text{s}$	$4.5\text{ V} \leq AV_{CC5} \leq 5.5\text{ V}$
			2.0	—	—	$\mu\text{s}$	$3.0\text{ V} \leq AV_{CC5} \leq 4.5\text{ V}$
Sampling time	$T_{samp}$	—	0.4	—	—	$\mu\text{s}$	$4.5\text{ V} \leq AV_{CC5} \leq 5.5\text{ V}$ , $R_{EXT} < 2\text{ k}\Omega$
			1.0	—	—	$\mu\text{s}$	$3.0\text{ V} \leq AV_{CC5} \leq 4.5\text{ V}$ , $R_{EXT} < 1\text{ k}\Omega$
Conversion time	$T_{conv}$	—	1.0	—	—	$\mu\text{s}$	$4.5\text{ V} \leq AV_{CC5} \leq 5.5\text{ V}$
			3.0	—	—	$\mu\text{s}$	$3.0\text{ V} \leq AV_{CC5} \leq 4.5\text{ V}$
Input capacitance	$C_{IN}$	ANn	—	—	11	pF	
Input resistance	$R_{IN}$	ANn	—	—	2.6	k $\Omega$	$4.5\text{ V} \leq AV_{CC5} \leq 5.5\text{ V}$
			—	—	12.1	k $\Omega$	$3.0\text{ V} \leq AV_{CC5} \leq 4.5\text{ V}$
Analog input leakage current	$I_{AIN}$	ANn	-1	—	+1	$\mu\text{A}$	$T_A = +25\text{ }^\circ\text{C}$
			-3	—	+3	$\mu\text{A}$	$T_A = +105\text{ }^\circ\text{C}$
Analog input voltage range	$V_{AIN}$	ANn	AVRL	—	AVRH	V	
Offset between input channels	—	ANn	—	—	4	LSB	

(Continued)

Note : The accuracy gets worse as AVRH - AVRL becomes smaller

# MB91460H Series

(Continued)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Reference voltage range	AVRH	AVRH5	$0.75 \times AV_{CC5}$	—	$AV_{CC5}$	V	
	AVRL	AV <sub>SS5</sub>	$AV_{SS5}$	—	$AV_{CC5} \times 0.25$	V	
Power supply current per ADC macro *3	I <sub>A</sub>	AV <sub>CC5</sub>	—	2.5	5	mA	A/D Converter active
	I <sub>AH</sub>	AV <sub>CC5</sub>	—	—	5	μA	A/D Converter not operated *1
Reference voltage current per ADC macro *3	I <sub>R</sub>	AVRH5	—	0.7	1	mA	A/D Converter active
	I <sub>RH</sub>	AVRH5	—	—	5	μA	A/D Converter not operated *2

\*1 : Supply current at AV<sub>CC5</sub>, if A/D converter and ALARM comparator are not operating, (V<sub>DD5</sub> = AV<sub>CC5</sub> = AVRH = 5.0 V)

\*2 : Input current at AVRH5, if A/D converter is not operating, (V<sub>DD5</sub> = AV<sub>CC5</sub> = AVRH = 5.0 V)

\*3 : The current consumption per ADC macro is given here. On devices having more than one A/D converter, the current values have to be multiplied by the number of macros.

## Sampling Time Calculation

$$T_{\text{samp}} = (2.6 \text{ k}\Omega + R_{\text{EXT}}) \times 11 \text{ pF} \times 7; \text{ for } 4.5\text{V} \leq AV_{CC5} \leq 5.5\text{V}$$

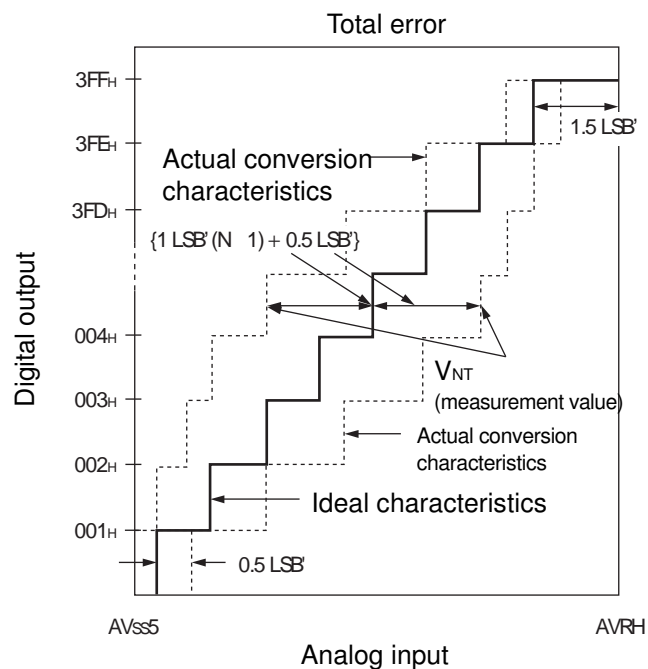
$$T_{\text{samp}} = (12.1 \text{ k}\Omega + R_{\text{EXT}}) \times 11 \text{ pF} \times 7; \text{ for } 3.0\text{V} \leq AV_{CC5} < 4.5\text{V}$$

## Conversion Time Calculation

$$T_{\text{conv}} = T_{\text{samp}} + T_{\text{comp}}$$

## Definition of A/D converter terms

- Resolution  
Analog variation that is recognizable by the A/D converter.
- Nonlinearity error  
Deviation between actual conversion characteristics and a straight line connecting the zero transition point (00 0000 0000<sub>B</sub> ↔ 00 0000 0001<sub>B</sub>) and the full scale transition point (11 1111 1110<sub>B</sub> ↔ 11 1111 1111<sub>B</sub>).
- Differential nonlinearity error  
Deviation of the input voltage from the ideal value that is required to change the output code by 1 LSB.
- Total error  
This error indicates the difference between actual and theoretical values, including the zero transition error, full scale transition error, and nonlinearity error.



$$1\text{LSB}' \text{ (ideal value)} = \frac{\text{AVRH} - \text{AV}_{\text{ss5}}}{1024} \text{ [V]}$$

$$\text{Total error of digital output } N = \frac{V_{\text{NT}} - \{1 \text{ LSB}' \times (N - 1) + 0.5 \text{ LSB}'\}}{1 \text{ LSB}'}$$

N : A/D converter digital output value

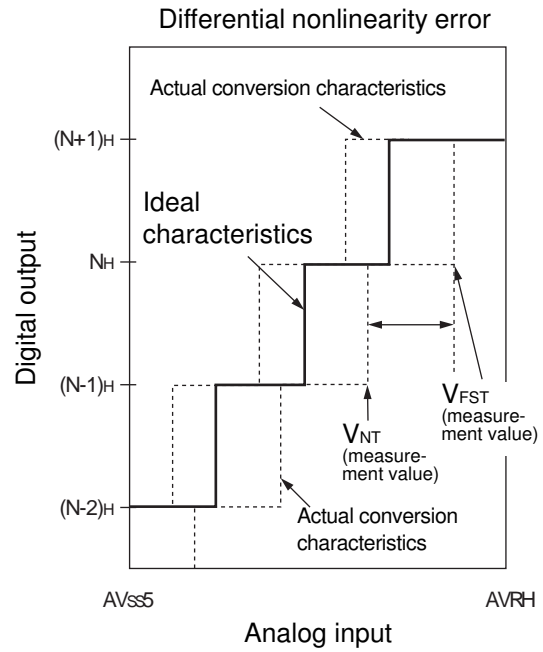
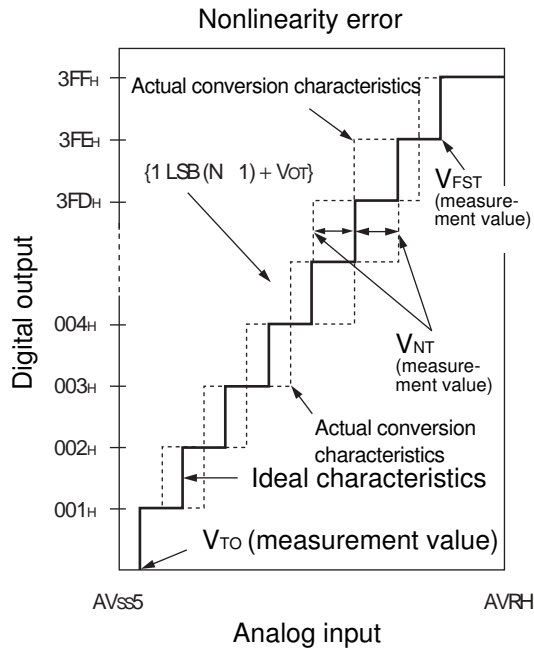
V<sub>OT'</sub> (ideal value) = AV<sub>ss5</sub> + 0.5 LSB' [V]

V<sub>FST'</sub> (ideal value) = AV<sub>RH</sub> - 1.5 LSB' [V]

V<sub>NT</sub> : Voltage at which the digital output changes from (N + 1)<sub>H</sub> to N<sub>H</sub>

(Continued)

(Continued)



$$\text{Nonlinearity error of digital output } N = \frac{V_{NT} - \{1\text{LSB} \times (N - 1) + V_{OT}\}}{1\text{LSB}} \text{ [LSB]}$$

$$\text{Differential nonlinearity error of digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1\text{LSB}} - 1 \text{ [LSB]}$$

$$1\text{LSB} = \frac{V_{FST} - V_{OT}}{1022} \text{ [V]}$$

N : A/D converter digital output value

V<sub>OT</sub> : Voltage at which the digital output changes from 000<sub>H</sub> to 001<sub>H</sub>.

V<sub>FST</sub> : Voltage at which the digital output changes from 3FE<sub>H</sub> to 3FF<sub>H</sub>.

## 5. Alarm comparator characteristics

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Power supply current	I <sub>A5ALMF</sub>	AV <sub>CC5</sub>	—	25	40	μA	Alarm comparator enabled in fast mode (per channel) *1
	I <sub>A5ALMS</sub>		—	7	10	μA	Alarm comparator enabled in normal mode (per channel) *1
	I <sub>A5ALMH</sub>		—	—	5	μA	Alarm comparator disabled
ALARM pin input current	I <sub>ALIN</sub>	ALARM_n	- 1	—	+ 1	μA	T <sub>A</sub> =25 °C
			- 3	—	+ 3	μA	T <sub>A</sub> =105 °C
ALARM pin input voltage range	V <sub>ALIN</sub>		0	—	AV <sub>CC5</sub>	V	
Alarm upper limit voltage	V <sub>IAH</sub>		AV <sub>CC5</sub> × 0.78 - 3%	AV <sub>CC5</sub> × 0.78	AV <sub>CC5</sub> × 0.78 + 3%	V	
Alarm lower limit voltage	V <sub>IAL</sub>		AV <sub>CC5</sub> × 0.36 - 5%	AV <sub>CC5</sub> × 0.36	AV <sub>CC5</sub> × 0.36 + 5%	V	
Alarm hysteresis voltage	V <sub>IAHYS</sub>		50	—	250	mV	
Alarm input resistance	R <sub>IN</sub>		5	—	—	MΩ	
Comparison time	t <sub>COMPF</sub>		—	0.1	0.2	μs	Alarm comparator enabled in fast mode *1
	t <sub>COMPS</sub>		—	1	2	μs	Alarm comparator enabled in normal mode *1

Note: \*1 : The fast Alarm Comparator mode is enabled by setting ACSR.MD=1  
Setting ACSR.MD=0 sets the normal mode.

# MB91460H Series

## 6. FLASH memory program/erase characteristics

### 6.1. MB91F464HB

( $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V}$ )

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	0.9	3.6	s	Erase programming time not included
Chip erase time	-	n*0.9	n*3.6	s	n is the number of Flash sector of the device
Word (16-bit or 32-bit width) programming time	-	23	370	$\mu\text{s}$	System overhead time not included
Programme/Erase cycle	10 000			cycle	
Flash data retention time	20			year	*1

\*1: This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to convert high temperature measurements into normalized value at  $85^\circ\text{C}$ )

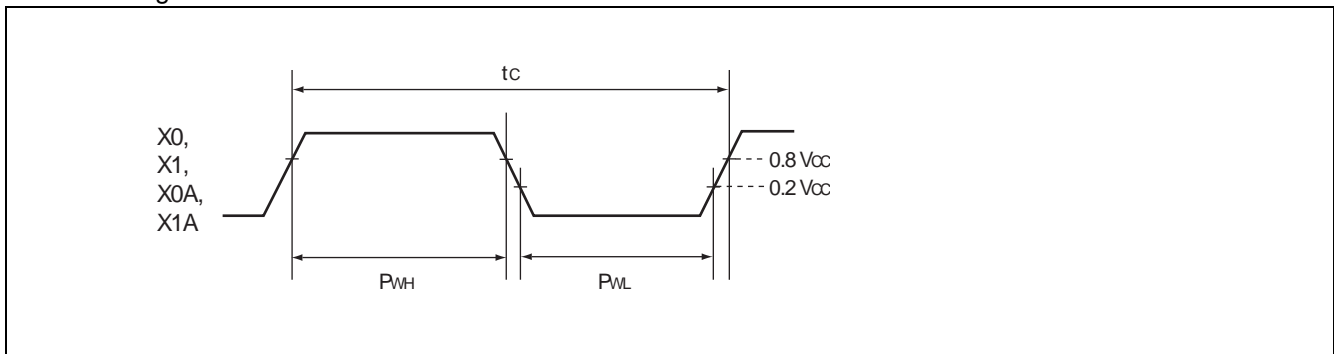
## 7. AC characteristics

### 7.1. Clock timing

( $V_{DD5} = 3.0\text{ V to } 5.5\text{ V}$ ,  $V_{SS5} = AV_{SS5} = 0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C to } +105\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Value			Unit	Condition
			Min	Typ	Max		
Clock frequency	$f_c$	X0 X1	3.5	4	16	MHz	Opposite phase external supply or crystal
		X0A X1A	32	32.768	100	kHz	

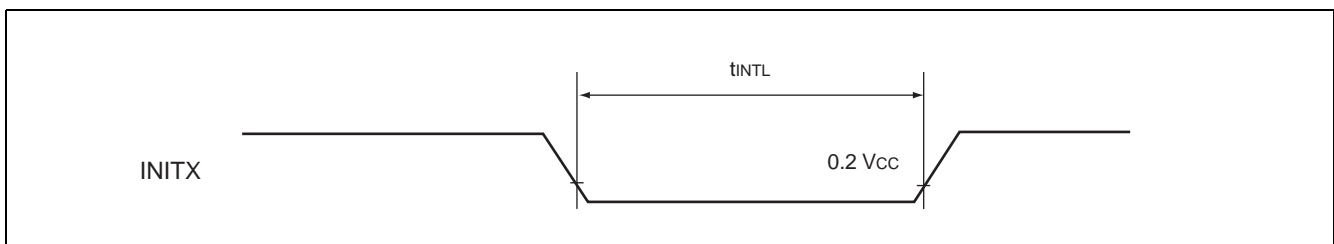
#### • Clock timing condition



### 7.2. Reset input ratings

( $V_{DD5} = 3.0\text{ V to } 5.5\text{ V}$ ,  $V_{SS5} = AV_{SS5} = 0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C to } +105\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
INITX input time (at power-on)	$t_{INTL}$	INITX	—	8	—	ms
INITX input time (other than the above)				20	—	$\mu\text{s}$



# MB91460H Series

## 7.3. LIN-USART Timings at V<sub>DD5</sub> = 3.0 to 5.5 V

- Conditions during AC measurements  
All AC tests were measured under the following conditions:
  - I<sub>Odrive</sub> = 5 mA
  - V<sub>DD5</sub> = 3.0 V to 5.5 V, I<sub>load</sub> = 3 mA
  - V<sub>SS5</sub> = 0 V
  - T<sub>a</sub> = -40 °C to +105 °C
  - C<sub>i</sub> = 50 pF (load capacity value of pins when testing)
  - VOL = 0.2 x V<sub>DD5</sub>
  - VOH = 0.8 x V<sub>DD5</sub>
  - EPILR = 0, PILR = 1 (Automotive Level = worst case)

(V<sub>DD5</sub> = 3.0 V to 5.5 V, V<sub>SS5</sub> = AV<sub>SS5</sub> = 0 V, T<sub>A</sub> = -40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	V <sub>DD5</sub> = 3.0 V to 4.5 V		V <sub>DD5</sub> = 4.5 V to 5.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t <sub>SCYCI</sub>	SCKn	Internal clock operation (master mode)	4 t <sub>CLKP</sub>	—	4 t <sub>CLKP</sub>	—	ns
SCK ↓ → SOT delay time	t <sub>SLOVI</sub>	SCKn SOTn		- 30	30	- 20	20	ns
SOT → SCK ↓ delay time	t <sub>OVSHI</sub>	SCKn SOTn		m x t <sub>CLKP</sub> - 30*	—	m x t <sub>CLKP</sub> - 20*	—	ns
Valid SIN → SCK ↑ setup time	t <sub>IVSHI</sub>	SCKn SINn		t <sub>CLKP</sub> + 55	—	t <sub>CLKP</sub> + 45	—	ns
SCK ↑ → valid SIN hold time	t <sub>SHIXI</sub>	SCKn SINn		0	—	0	—	ns
Serial clock “H” pulse width	t <sub>SHSLE</sub>	SCKn	External clock operation (slave mode)	t <sub>CLKP</sub> + 10	—	t <sub>CLKP</sub> + 10	—	ns
Serial clock “L” pulse width	t <sub>SLSHE</sub>	SCKn		t <sub>CLKP</sub> + 10	—	t <sub>CLKP</sub> + 10	—	ns
SCK ↓ → SOT delay time	t <sub>SLOVE</sub>	SCKn SOTn		—	2 t <sub>CLKP</sub> + 55	—	2 t <sub>CLKP</sub> + 45	ns
Valid SIN → SCK ↑ setup time	t <sub>IVSHE</sub>	SCKn SINn		10	—	10	—	ns
SCK ↑ → valid SIN hold time	t <sub>SHIXE</sub>	SCKn SINn		t <sub>CLKP</sub> + 10	—	t <sub>CLKP</sub> + 10	—	ns
SCK rising time	t <sub>FE</sub>	SCKn		—	20	—	20	ns
SCK falling time	t <sub>RE</sub>	SCKn	—	20	—	20	ns	

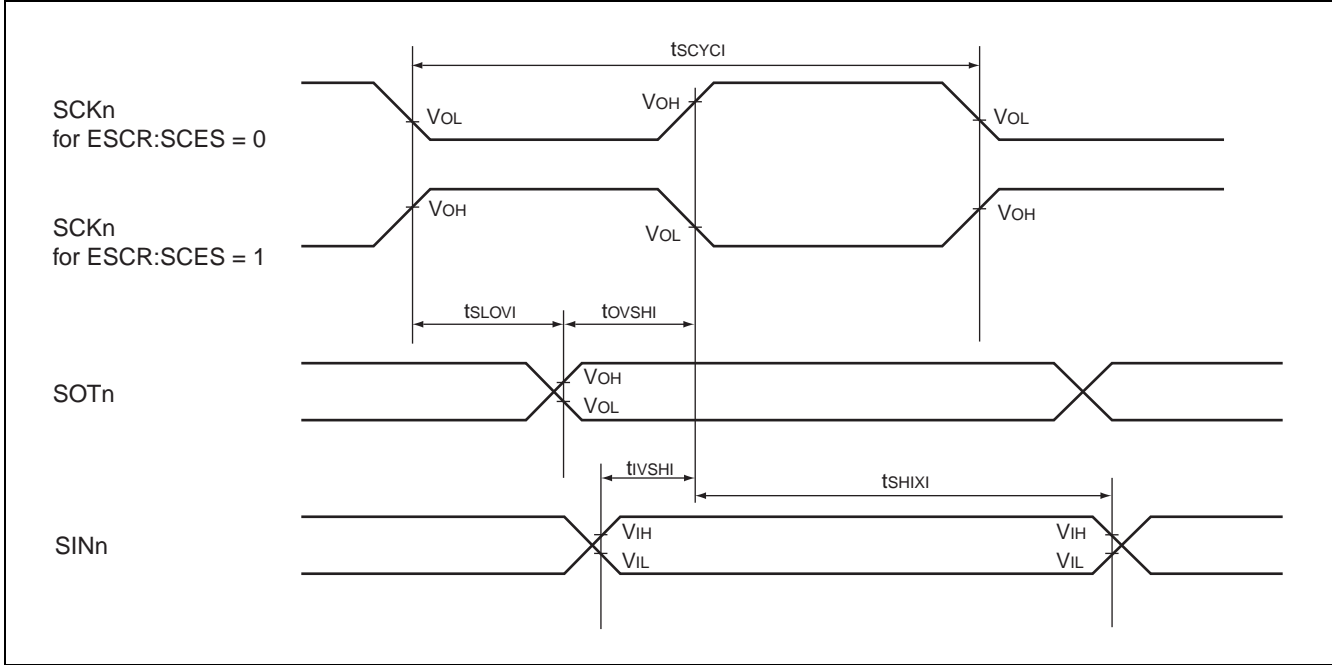
\* : Parameter m depends on t<sub>SCYCI</sub> and can be calculated as :

- if t<sub>SCYCI</sub> = 2\*k\*t<sub>CLKP</sub>, then m = k, where k is an integer > 2
- if t<sub>SCYCI</sub> = (2\*k + 1)\*t<sub>CLKP</sub>, then m = k + 1, where k is an integer > 1

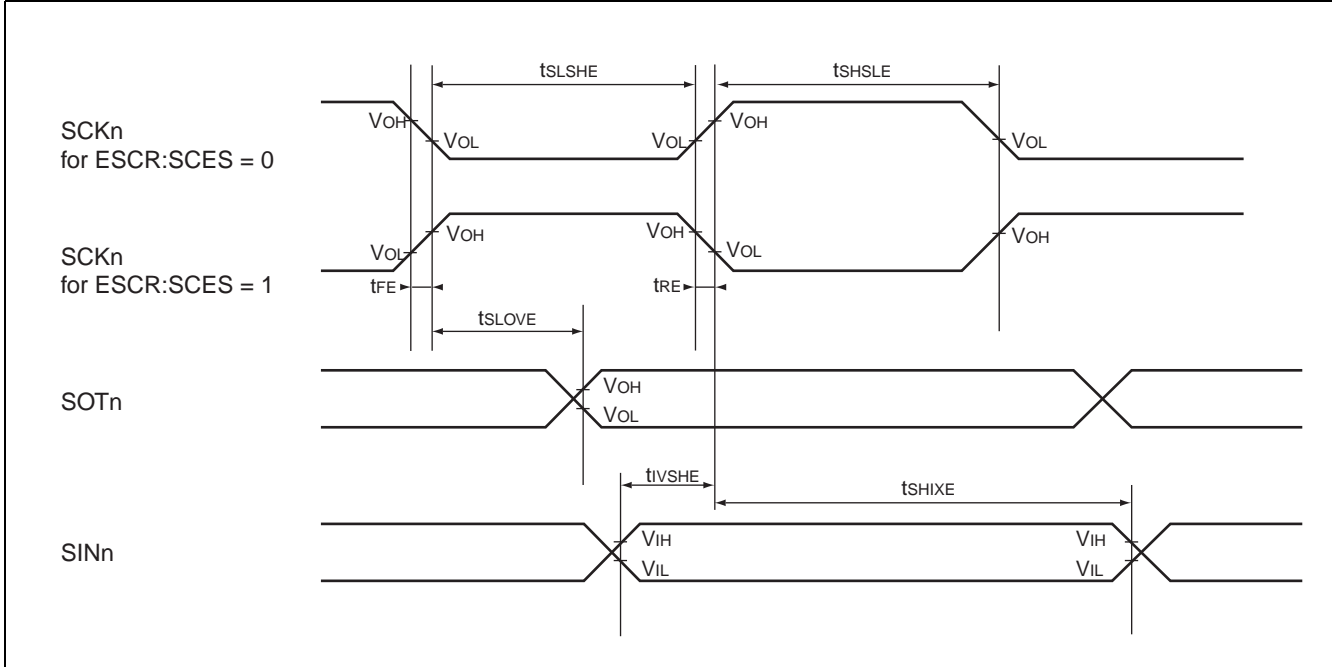
Notes : • The above values are AC characteristics for CLK synchronous mode.

- t<sub>CLKP</sub> is the cycle time of the peripheral clock.

• Internal clock mode (master mode)



• External clock mode (slave mode)



# MB91460H Series

## 7.4. I<sup>2</sup>C AC Timings at V<sub>DD5</sub> = 3.0 to 5.5 V

- Conditions during AC measurements

All AC tests were measured under the following conditions:

- I<sub>Odrive</sub> = 3 mA
- V<sub>DD5</sub> = 3.0 V to 5.5 V, I<sub>load</sub> = 3 mA
- V<sub>SS5</sub> = 0 V
- T<sub>A</sub> = -40 °C to +105 °C
- C<sub>i</sub> = 50 pF
- V<sub>OL</sub> = 0.3 × V<sub>DD5</sub>
- V<sub>OH</sub> = 0.7 × V<sub>DD5</sub>
- EPILR = 0, PILR = 0 (CMOS Hysteresis 0.3 × V<sub>DD5</sub>/0.7 × V<sub>DD5</sub>)

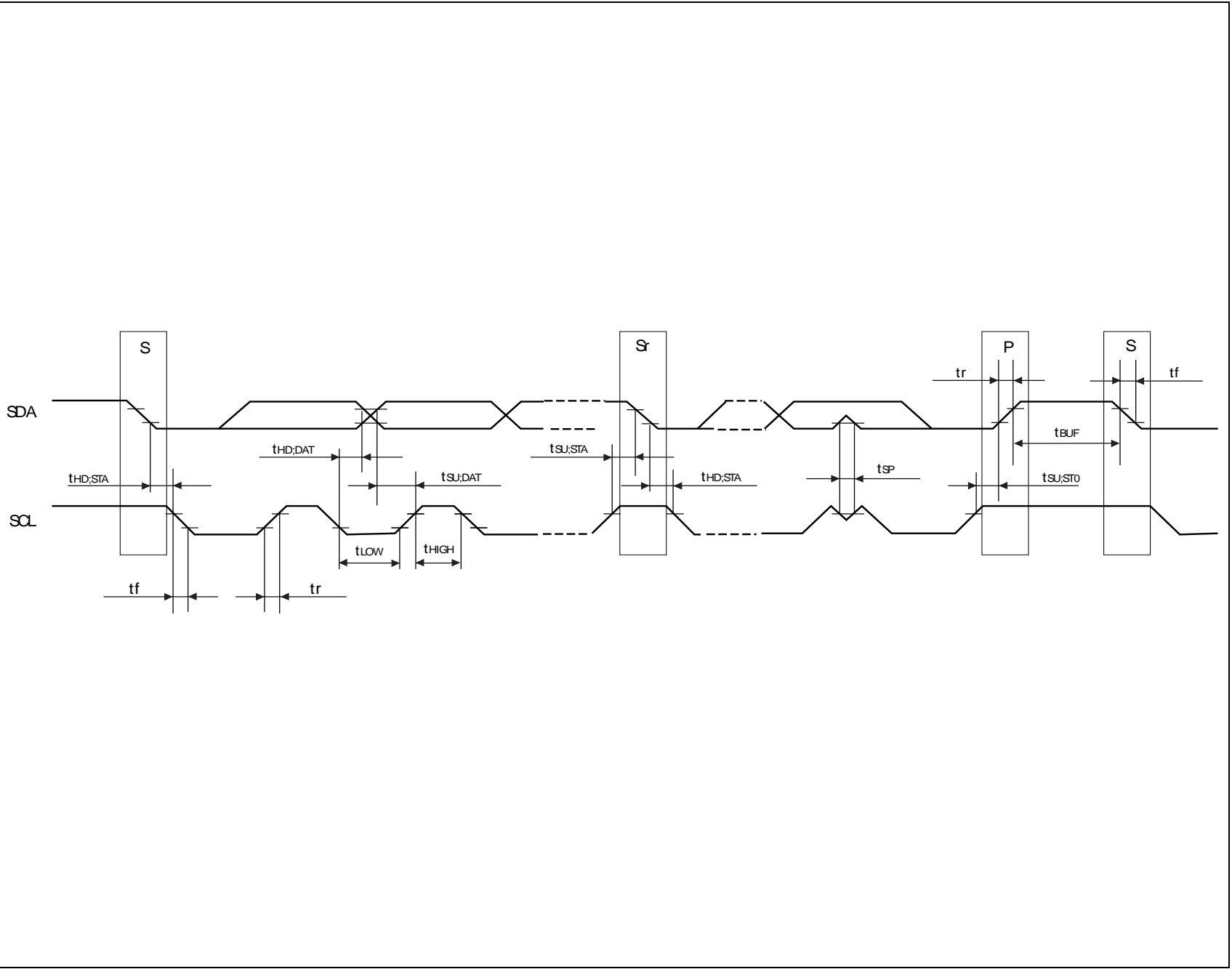
Fast mode:

(V<sub>DD5</sub> = 3.5 V to 5.5 V, V<sub>SS5</sub> = AV<sub>SS5</sub> = 0 V, T<sub>A</sub> = -40 °C to +105 °C)

Parameter	Symbol	Pin name	Value		Unit	Remark
			Min	Max		
SCL clock frequency	f <sub>SCL</sub>	SCLn	0	400	kHz	
Hold time (repeated) START condition. After this period, the first clock pulse is generated	t <sub>HD;STA</sub>	SCLn, SDAn	0.6	—	μs	
LOW period of the SCL clock	t <sub>LOW</sub>	SCLn	1.3	—	μs	
HIGH period of the SCL clock	t <sub>HIGH</sub>	SCLn	0.6	—	μs	
Setup time for a repeated START condition	t <sub>SU;STA</sub>	SCLn, SDAn	0.6	—	μs	
Data hold time for I <sup>2</sup> C-bus devices	t <sub>HD;DAT</sub>	SCLn, SDAn	0	0.9	μs	
Data setup time	t <sub>SU;DAT</sub>	SCLn SDAn	100	—	ns	
Rise time of both SDA and SCL signals	t <sub>r</sub>	SCLn, SDAn	20 + 0.1Cb	300	ns	
Fall time of both SDA and SCL signals	t <sub>f</sub>	SCLn, SDAn	20 + 0.1Cb	300	ns	
Setup time for STOP condition	t <sub>SU;STO</sub>	SCLn, SDAn	0.6	—	μs	
Bus free time between a STOP and START condition	t <sub>BUF</sub>	SCLn, SDAn	1.3	—	μs	
Capacitive load for each bus line	C <sub>b</sub>	SCLn, SDAn	—	400	pF	
Pulse width of spike suppressed by input filter	t <sub>SP</sub>	SCLn, SDAn	0	(1..1.5) × t <sub>CLKP</sub>	ns	*1

\*1 The noise filter will suppress single spikes with a pulse width of 0ns and between (1 to 1.5) cycles of peripheral clock, depending on the phase relationship between I<sup>2</sup>C signals (SDA, SCL) and peripheral clock.

Note: t<sub>CLKP</sub> is the cycle time of the peripheral clock.



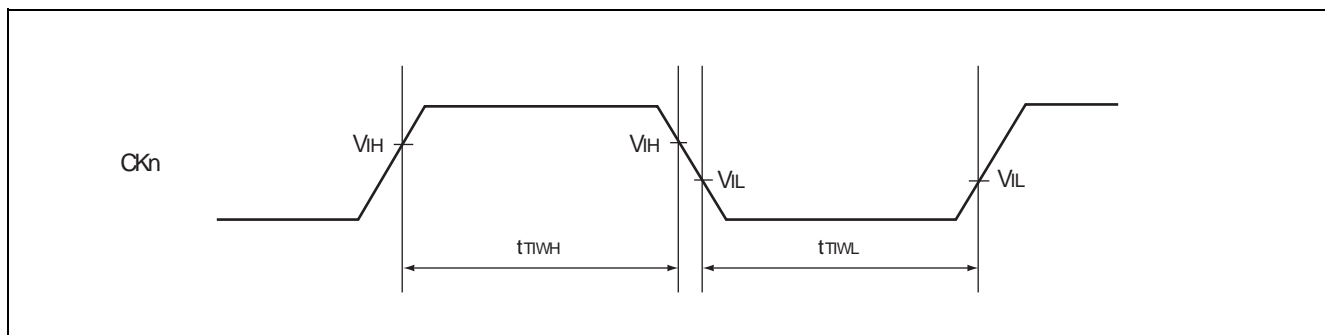
# MB91460H Series

## 7.5. Free-run timer clock

( $V_{DD5} = 3.0\text{ V to } 5.5\text{ V}$ ,  $V_{SS5} = AV_{SS5} = 0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C to } +105\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Input pulse width	$t_{TIWH}$ $t_{TIWL}$	CKn	—	$4t_{CLKP}$	—	ns

Note :  $t_{CLKP}$  is the cycle time of the peripheral clock.

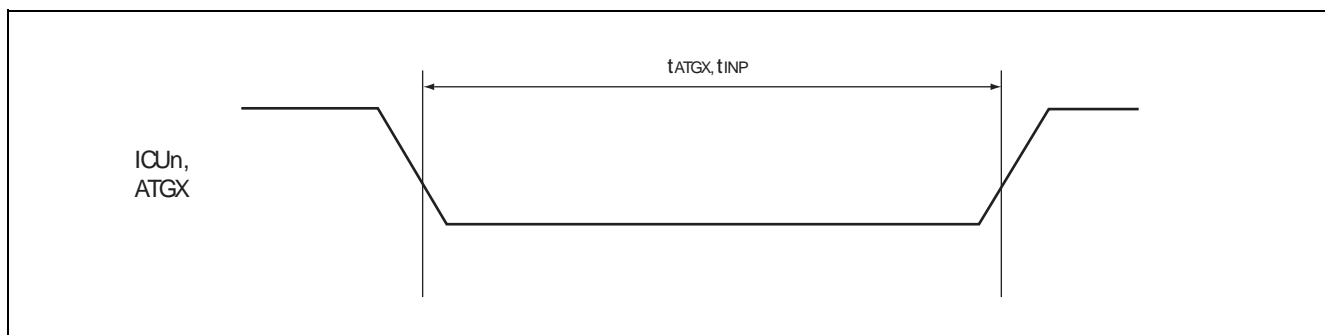


## 7.6. Trigger input timing

( $V_{DD5} = 3.0\text{ V to } 5.5\text{ V}$ ,  $V_{SS5} = AV_{SS5} = 0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C to } +105\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Input capture input trigger	$t_{INP}$	ICUn	—	$5t_{CLKP}$	—	ns
A/D converter trigger	$t_{ATGX}$	ATGX	—	$5t_{CLKP}$	—	ns

Note :  $t_{CLKP}$  is the cycle time of the peripheral clock.



## 7.7. External Bus AC Timings at $V_{DD35} = 3.0$ to $5.5$ V

- Conditions during AC measurements  
All AC tests were measured under the following conditions:
  - $I_{Odrive} = 5$  mA
  - $V_{DD35} = 4.5$  V to  $5.5$  V,  $I_{load} = 3$  mA
  - $V_{SS5} = 0$  V
  - $T_a = -40$  °C to  $+105$  °C
  - $C_i = 50$  pF
  - $V_{OL} = 0.5 \times V_{DD35}$
  - $V_{OH} = 0.5 \times V_{DD35}$
  - $EPILR = 0$ ,  $PILR = 1$  (Automotive Level = worst case)

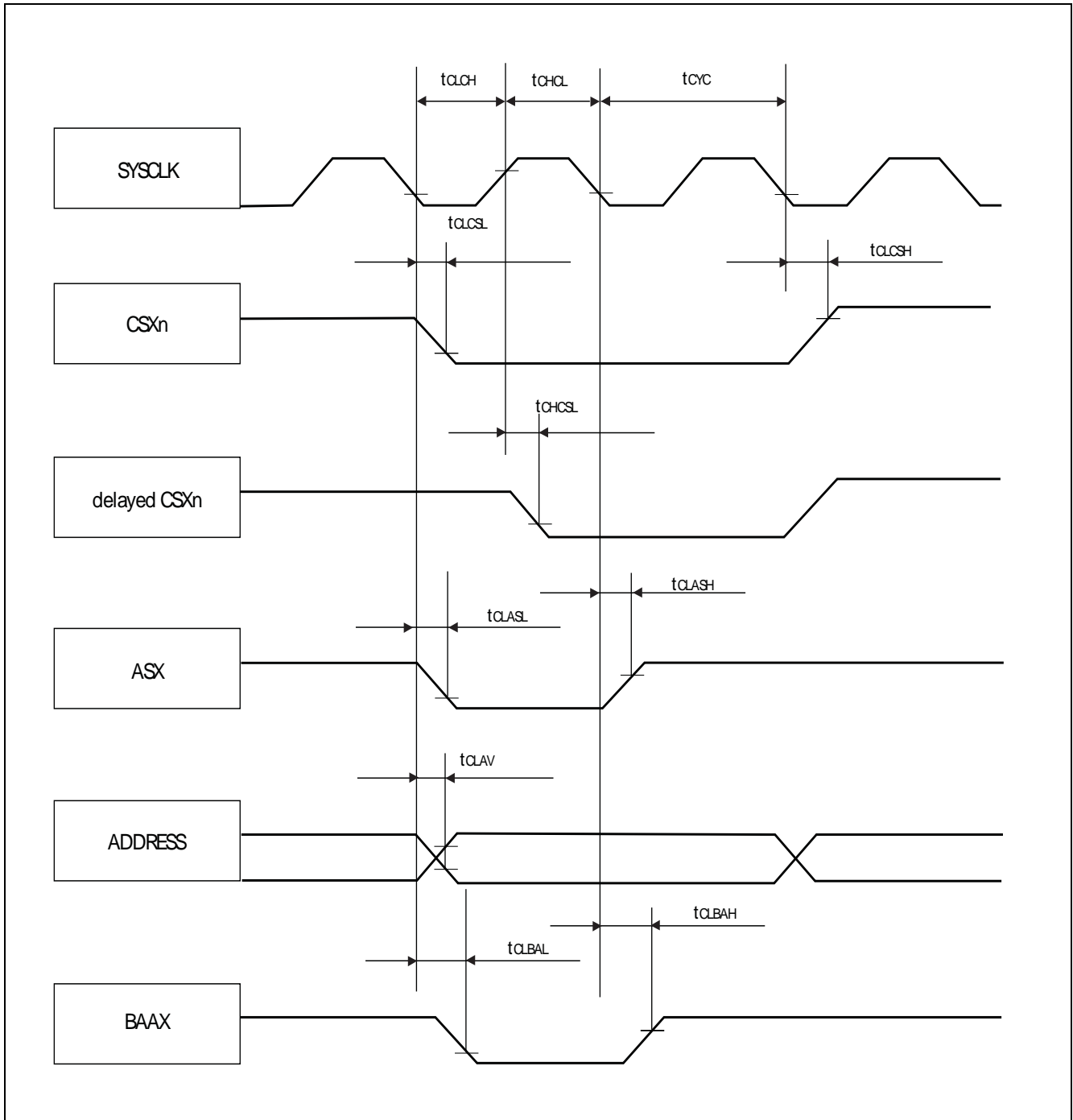
### 7.7.1. Basic Timing

( $V_{DD35} = 3.0$  V to  $5.5$  V,  $V_{SS5} = AV_{SS5} = 0$  V,  $T_A = -40$  °C to  $+105$  °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
SYSCLK	$t_{CLCH}$	SYSCLK	$1/2 \times t_{CLKT} - 1$	$1/2 \times t_{CLKT} + 9$	ns
	$t_{CHCL}$		$1/2 \times t_{CLKT} - 9$	$1/2 \times t_{CLKT} + 1$	ns
SYSCLK ↓ to CSXn delay time	$t_{CLCSL}$	SYSCLK CSXn	—	8	ns
	$t_{CLCSH}$		—	12	ns
SYSCLK ↑ to CSXn delay time (Addr → CS delay)	$t_{CHCSL}$		-6	+1	ns
SYSCLK ↓ to Address valid delay time	$t_{CLAV}$	SYSCLK A21 to A0	—	13	ns

Note :  $t_{CLKT}$  is the cycle time of the external bus clock.

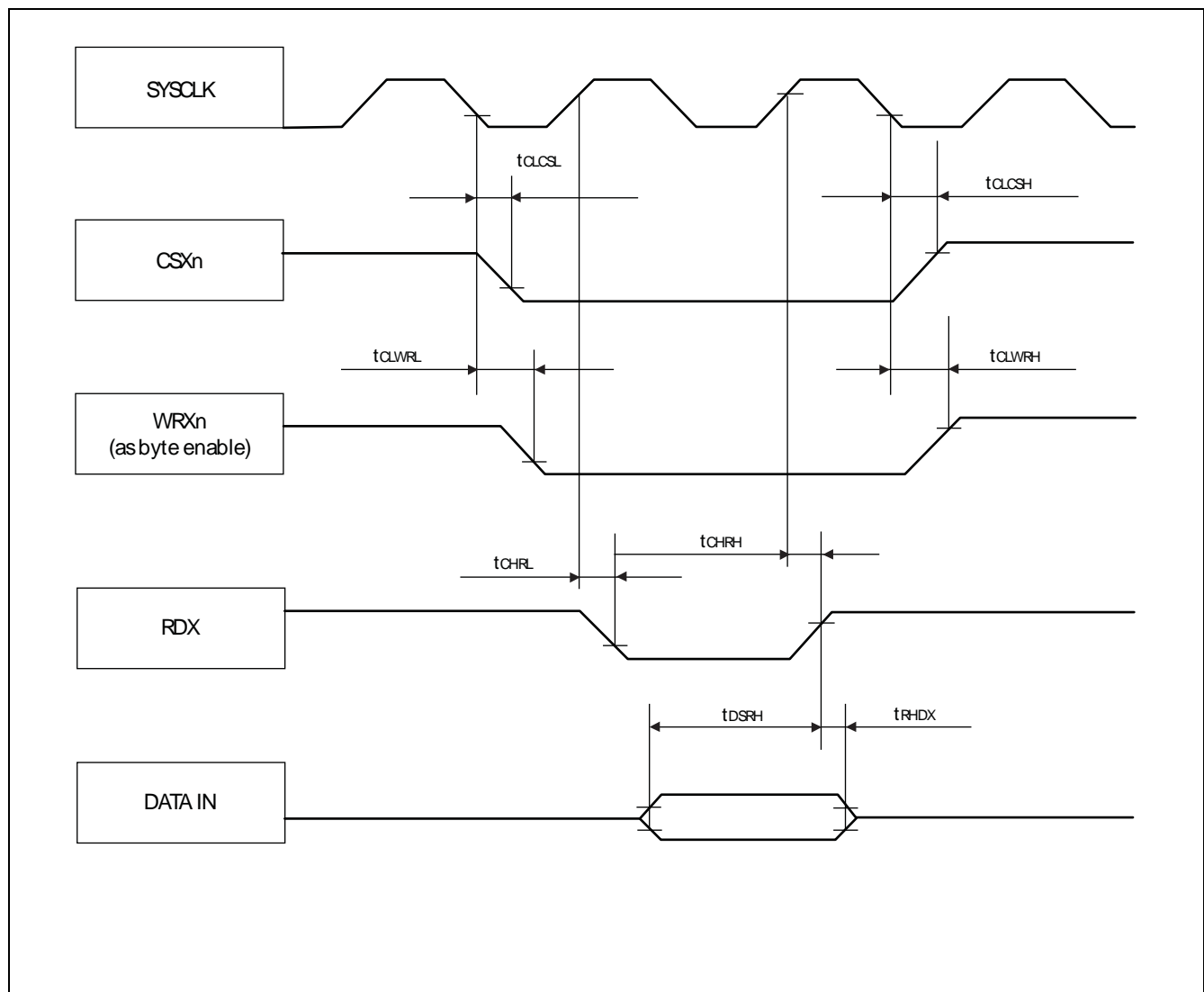
# MB91460H Series



## 7.7.2. Synchronous/Asynchronous read access

( $V_{DD35} = 3.0\text{ V to } 5.5\text{ V}$ ,  $V_{SS5} = AV_{SS5} = 0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C to } +105\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
SYSCLK $\uparrow$ to RDX delay time	TCHRL	SYSCLK	-7	1	ns
	TCHRH	RDX	-4	2	ns
Data valid to RDX $\uparrow$ setup time	TDSRH	RDX D31 to D16	33	—	ns
RDX $\uparrow$ to Data valid hold time	TRHDX	RDX D31 to D16	0	—	ns
SYSCLK $\downarrow$ to WRXn (as byte enable) delay time	TCLWRL	SYSCLK	—	8	ns
	TCLWRH	WRXn	0	—	ns
SYSCLK $\downarrow$ to CSXn delay time	TCLCSL	SYSCLK	—	8	ns
	TCLCSH	CSXn	—	12	ns

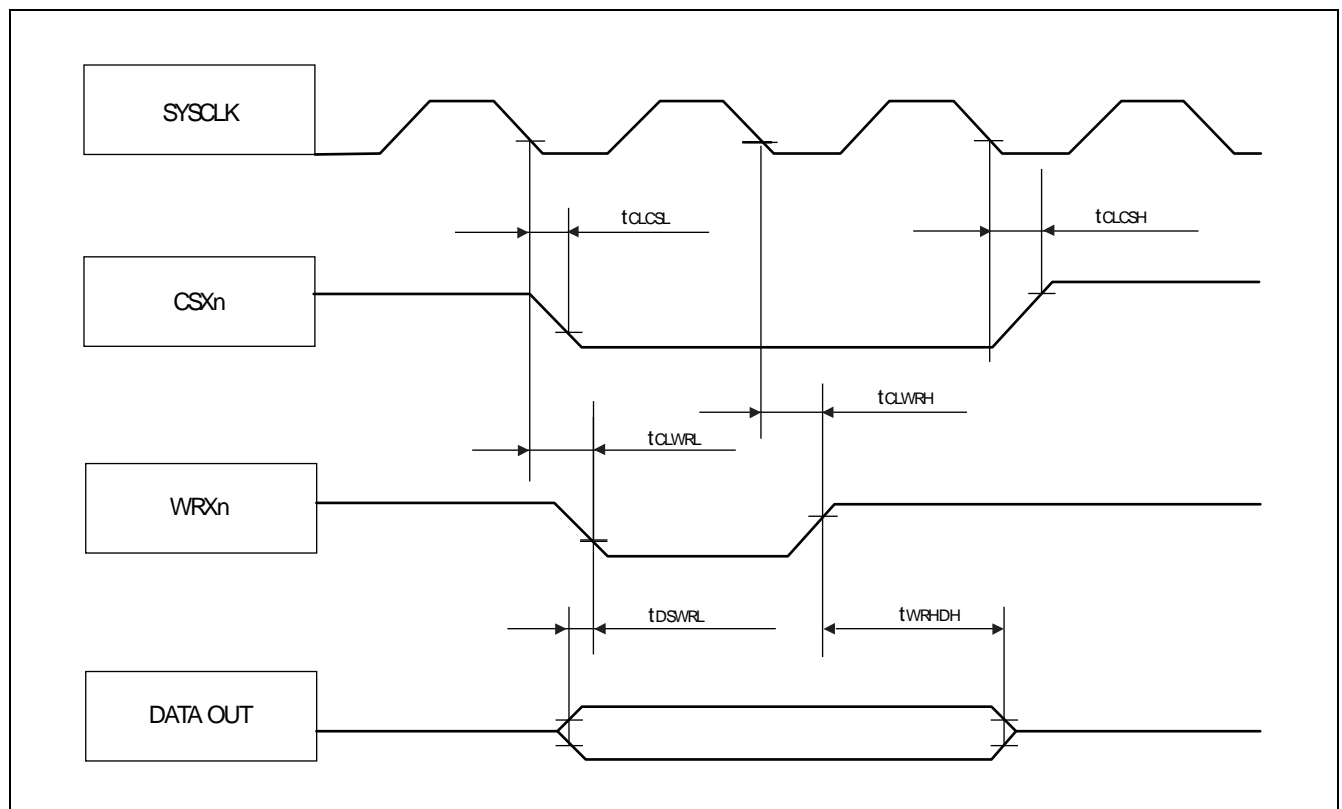


# MB91460H Series

## 7.7.3. Synchronous write access

( $V_{DD35} = 3.0\text{ V to }5.5\text{ V}$ ,  $V_{SS5} = AV_{SS5} = 0\text{ V}$ ,  $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ )

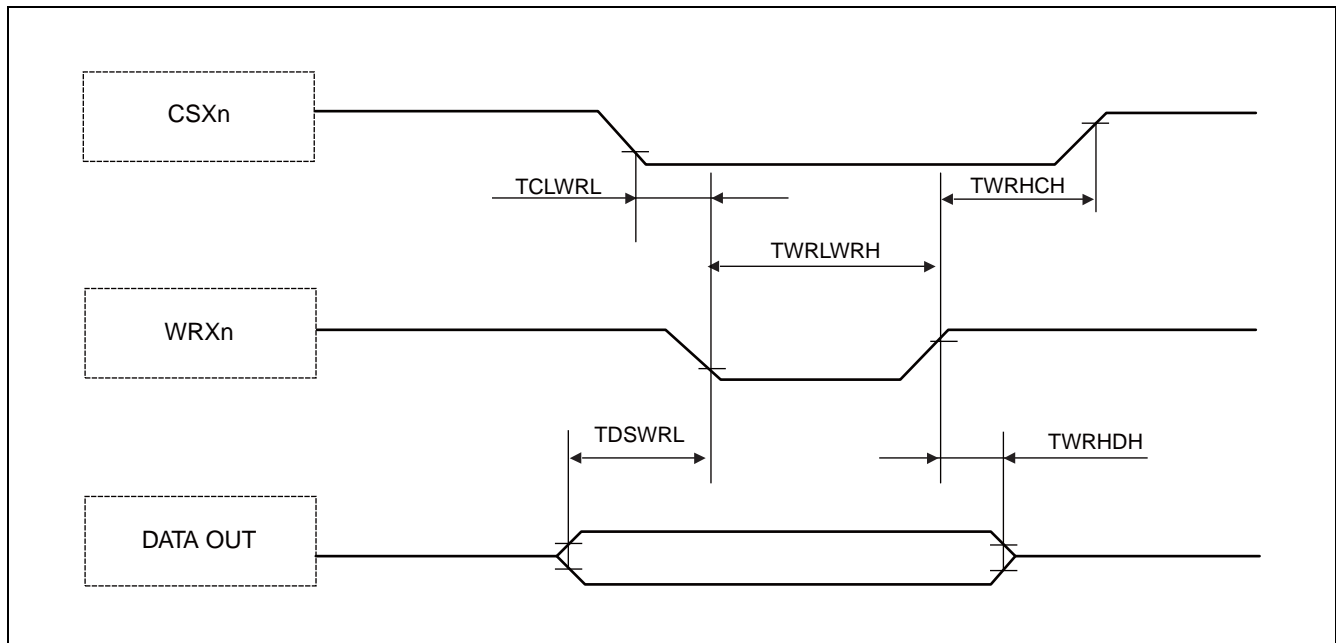
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
SYSCLK ↓ to WRXn delay time	TCLWRL	SYSCLK WRXn	—	8	ns
	TCLWRH		0	—	ns
Data valid to WRXn ↓ setup time	TDSWRL	WRXn D31 to D16	-7	—	ns
WRXn ↑ to Data valid hold time	TWRHDH	WRXn D31 to D16	$t_{CLKT} - 20$	—	ns
SYSCLK ↓ to CSXn delay time	TCLCSL	SYSCLK CSXn	—	8	ns
	TCLCSH		—	12	ns



## 7.7.4. Asynchronous write access

( $V_{DD35} = 3.0\text{ V to }5.5\text{ V}$ ,  $V_{SS5} = AV_{SS5} = 0\text{ V}$ ,  $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$ )

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
WRXn ↓ to WRXn ↑ pulse width	TWRLWRH	WRXn	$t_{CLKT}$	—	ns
Data valid to WRXn ↓ setup time	TDSWRL	WRXn D31 to D16	$1/2 \times t_{CLKT} - 10$	—	ns
WRXn ↑ to Data valid hold time	TWRHDH	WRXn D31 to D16	$1/2 \times t_{CLKT} - 19$	—	ns
WRXn to CSXn delay time	TCLWRL	WRXn	—	$1/2 \times t_{CLKT}$	ns
	TWRHCH	CSXn	$1/2 \times t_{CLKT}$	—	ns

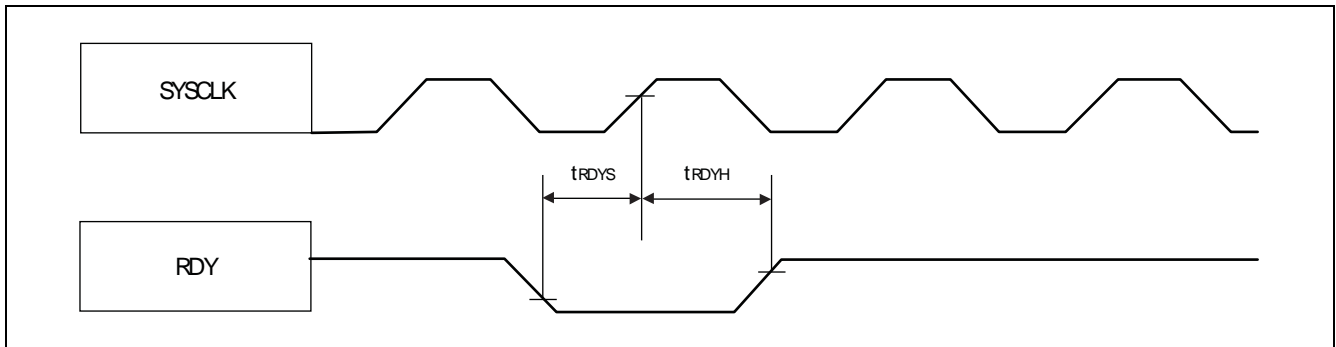


# MB91460H Series

## 7.7.5. RDY waitcycle insertion

( $V_{DD35} = 3.0\text{ V to }5.5\text{ V}$ ,  $V_{SS5} = AV_{SS5} = 0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C to }+105\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
RDY setup time	TRDYS	SYSCLK RDY	34	—	ns
RDY hold time	TRDYH	SYSCLK RDY	0	—	ns

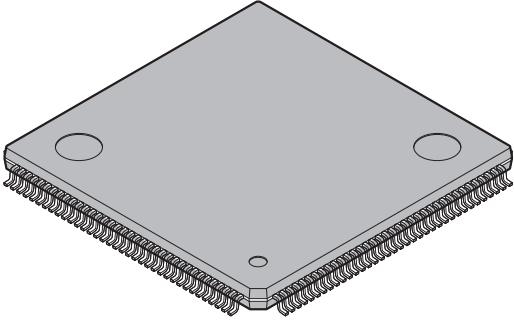


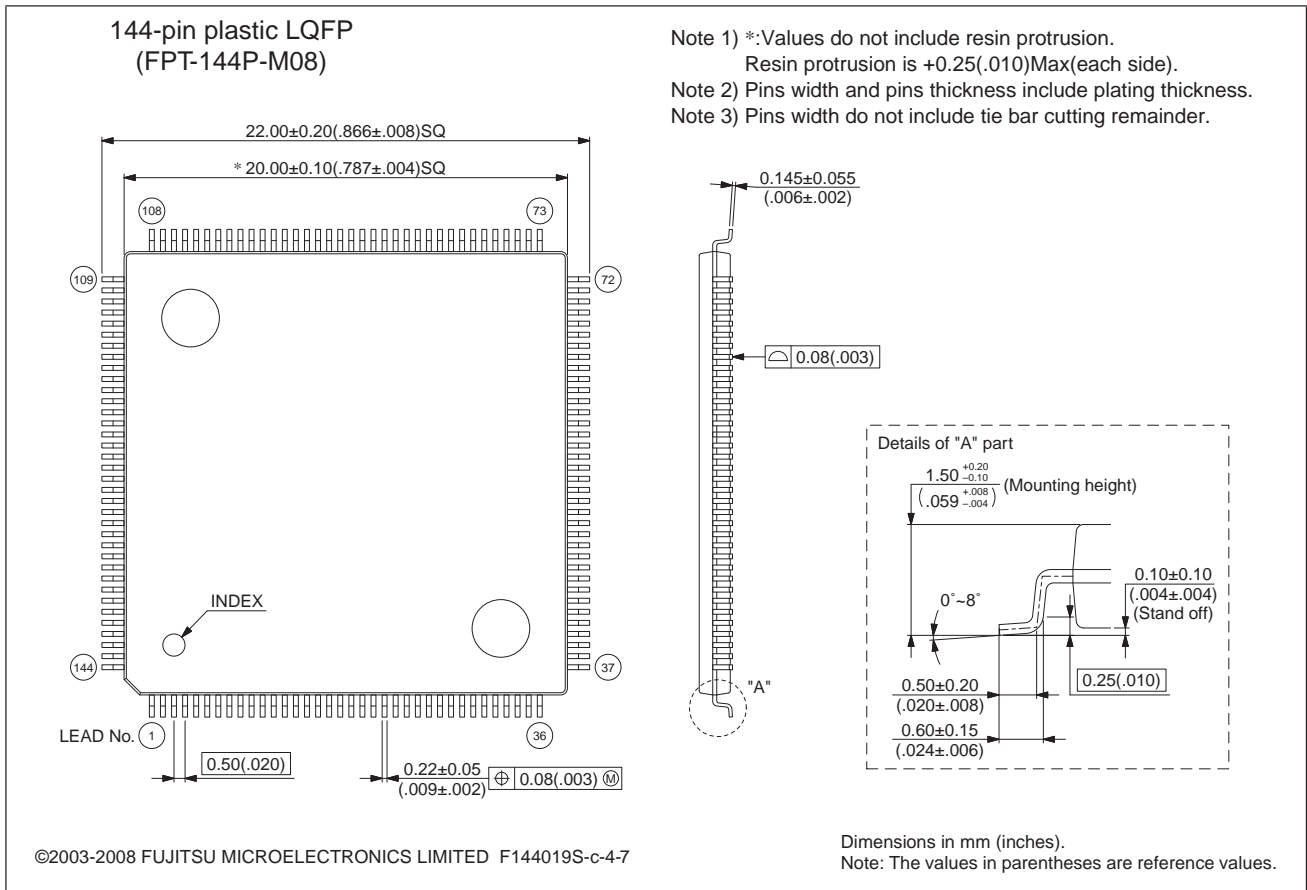
## ■ ORDERING INFORMATION

Part number	Package	Remarks
MB91F464HBPMC-GSE2	144-pin plastic LQFP (FPT-144P-M08)	Lead-free package

# MB91460H Series

## PACKAGE DIMENSION

<p>144-pin plastic LQFP</p>  <p>(FPT-144P-M08)</p>	Lead pitch	0.50 mm
	Package width × package length	20.0 × 20.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	1.20g
	Code (Reference)	P-LFQFP144-20×20-0.50



Please confirm the latest Package dimension by following URL.

<http://edevice.fujitsu.com/package/en-search/>

■ REVISION HISTORY

Version	Date	Remark
2.0	2009-01-07	Initial version

# MB91460H Series

## ■ MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
87	4. A/D converter characteristics	Corrected "Zero reading voltage" and "Full scale reading voltage".

The vertical lines marked in the left side of the page show the changes.

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# MB91460H Series

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