FUJITSU MICROELECTRONICS
DATA SHEET

DS07-16505-3E

32-bit Microcontroller

CMOS

FR60 MB91310 Series

MB91F312A/FV310A

■ DESCRIPTION

The FR* families are lines of single-chip microcontrollers based on a 32-bit high-performance RISC CPU, incorporating a variety of I/O resources for embedded control applications which require high CPU performance for high-speed processing.
The FR families are best suited for embedded applications which require high-performance CPU power for processing, such as TV and POP control.
Based on the FR30/FR40 family CPU, this FR60 family is enhanced in bus access for use in faster applications.

* : FR, the abbreviation of FUJITSU RISC controller, is a line of products of Fujitsu Microelectronics Limited.

■ FEATURE

- FR CPU
  - 32-bit RISC, load/store architecture with a five-stage pipeline
  - Operating frequency: 40 MHz (using PLL at an oscillation frequency of 10 MHz)
  - 16 - bit fixed length instructions (basic instructions), 1 instruction per cycle
  - Instruction set optimized for embedded applications: Memory-to-memory transfer, bit manipulation, barrel shift etc.

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For the information for microcontroller supports, see the following web site.

http://edevice.fujitsu.com/micom/en-support/

2008.10

- Instructions adapted for high-level languages: Function entry/exit instructions, multiple-register load/store instructions
- Register interlock functions : Facilitating coding in assemblers
- On-chip multiplier supported at the instruction level.
  Signed 32-bit multiplication : 5 cycles.
  Signed 16-bit multiplication : 3 cycles
- Interrupt (PC, PS save) : 6 cycles, 16 priority levels
- Harvard architecture allowing program access and data access to be executed simultaneously
- Instruction prefetch function implemented by a four-word queue in the CPU
- Instruction compatible with FR family

• Bus interface
  This bus interface is used for macro connection. (USB, OSDC)
  - Operating frequency Max 20 MHz
  - 16-bit data input/output (Interface to the USB and OSDC)
  - Chip-select signals can be output for completely independent eight areas allocatable in a minimum of 64 Kbytes. The $\overline{CS1}$, $\overline{CS2}$, and $\overline{CS3}$ areas are reserved as follows. $\overline{CS0}$, $\overline{CS4}$, to $\overline{CS3}$ are unusable.
    $\overline{CS1}$ area : USB host
    $\overline{CS2}$ area : USB function
    $\overline{CS3}$ area : OSDC
  - Basic bus cycle : 2 cycles
  - Programmable automatic wait cycle generator capable of inserting wait cycles for each area
    $\overline{CS1}$, $\overline{CS2}$ and $\overline{CS3}$ are reserved; their settings are fixed.

• Built-in RAM
  - 16 Kbytes built RAM capacity
  - This RAM can be used as instruction RAM by writing instruction code as well as data.

• DMAC (DMA Controller)
  - Connected to five channels (ch.0, ch.1 → USB function).
  - 3 forwarding factors (internal peripheral/software)
  - Addressing using 32-bit full addressing mode (increment, decrement, fixed)
  - Demand transfer, burst transfer, step transfer, or block transfer
  - Selectable transfer data size: 8-bit, 16-bit, or 32-bit

• Bit search module (for REALOS)
  - Search for the position of the bit 1/0-changed first in one word from the MSB

• Reload timer (including 1 channel for REALOS)
  - 16-bit PPG timer ch.3
  - Internal clock: Frequency division selectable from 2, 8, and 32

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- UART
  - Full duplex double buffer
  - UART : 5 channels
  - With parity / no parity selection
  - Asynchronous (start - stop synchronized) or CLK - synchronous communications selectable
  - Internal timer for dedicated baud rate
  - External clock can be used as transfer clock
  - Assorted error detection functions (for parity, frame, and overrun errors)

- I^2C Interface
  - Four channels are incorporated. (ch.3 can be used as two ports.)
  - Master/slave sending and receiving
  - Arbitration function
  - Clock synchronization function
  - Slave address and general call address detection function
  - Detecting transmitting direction function
  - Start condition repeat generation and detection function
  - Bus error detection function
  - 10-bit/7-bit slave address
  - Standard mode (Max 100 kbps)/High speed mode (Max 400 kbps) supported

- Interrupt controller
  - A total of five external interrupt lines are provided (1 nonmaskable interrupt pin ($\overline{NMI}$) and 4 normal interrupt pins (INT3 to INT0).
  - Interrupt from internal peripheral devices.
  - Programmable priorities (16 levels) for all interrupts except the non - maskable interrupt
  - Available for wakeup from STOP mode

- A/D converter
  - 10-bit resolution. 10 channels
  - Successive comparator type, conversion time : approx. 10 µs
  - Conversion modes (Single conversion mode, Scan conversion mode)
  - Startup sources (software and external triggers)

- PPG
  - 4 channels
  - Six-bit down-counter, 16-bit data register with cycle setting buffer
  - Internal clock : Frequency division selected from 1, 4, 16, and 64

- PWC
  - One channel (input) incorporated
  - 16 bits up counter
  - Simple LFP digital filter incorporated

- Multi function timer
  - 4 channels
  - Lowpass filter eliminating noise below the clock setting
  - Capable of pulse width measurement according to fine settings using seven types of clock signals
  - Event count function based on pin input
  - Interval timer function using seven different clocks and one external input clock

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- USB host function
  - USB 1.0 Specification
  - 8 Kbytes of internal RAM for parameters

- USB function
  - USB 1.1 compliant full-speed double buffering
  - CONTROL IN/OUT, BULK IN/OUT, INTERRUPT IN

- OSDC function
  - High-quality OSDC integrated
  - Analog RGB interface (with internal DAC)
  - Digital RGB I/F
  - Internal dot clock generator PLL

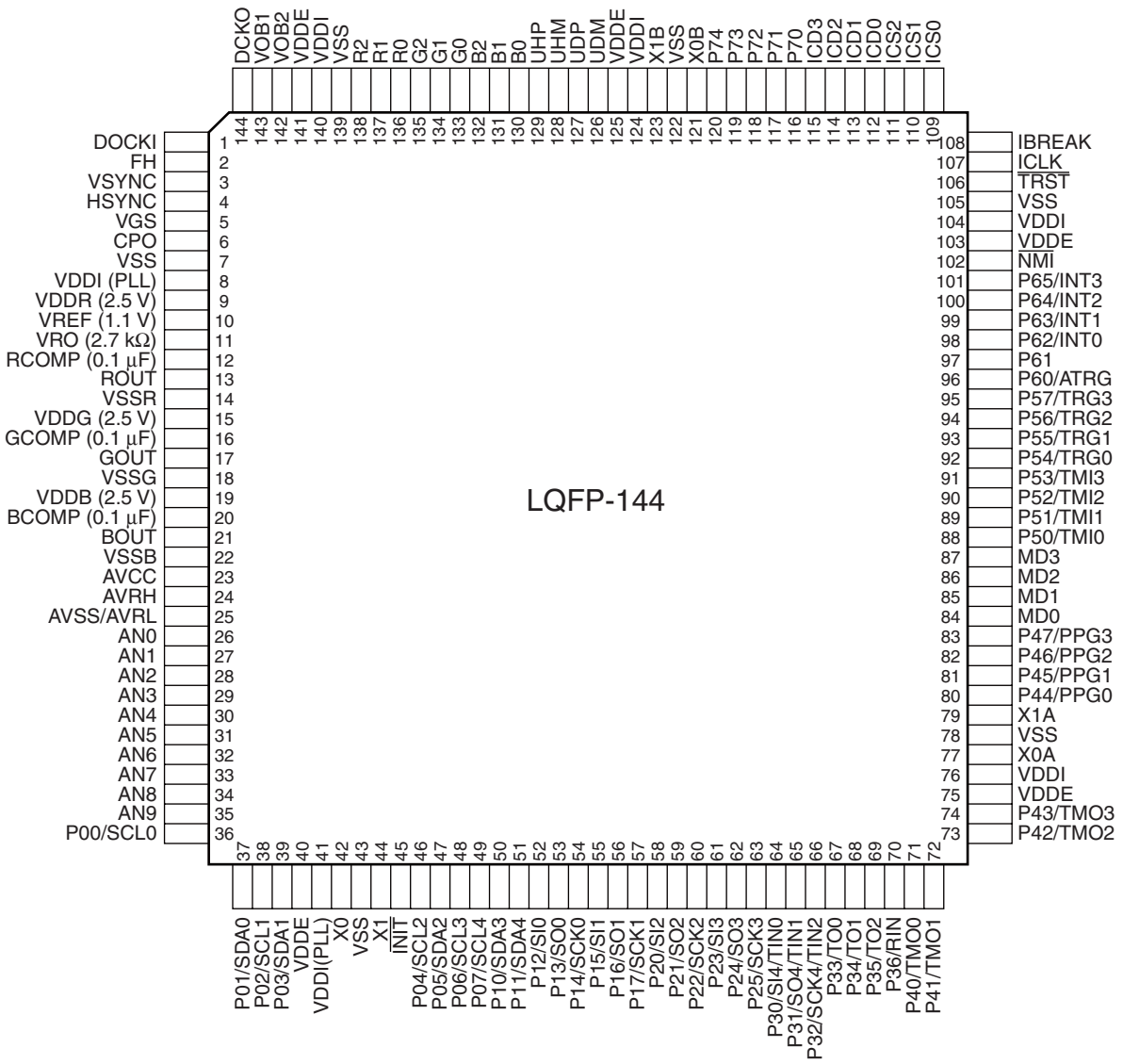
- Other internal times
  - 16-bit PPG timer ch.3 (u-timer)
  - Watch dog timer

- I/O port
  - Max 72 ports

- Other features
  - Internal oscillator circuit as clock source
  - $\overline{\text{INIT}}$ is prepared as a reset terminal.
  - Watchdog timer reset. Software reset.
  - Low power consumption modes supported: Stop mode and Sleep mode
  - Gear function
  - Built-in time base timer
  - Package : LQFP-144, 0.50 mm pitch, 20.0 $\times$ 20.0 mm
  - CMOS technology (0.25 μm)
  - Supply voltage: Dual power supplies at 3.3 V $\pm$ 0.3 V, 2.5 V $\pm$ 0.2 V

■ PIN ASSIGNMENT

(TOP VIEW)



(FPT-144P-M08)

■ PIN DESCRIPTION

Pin no.	Pin name	Circuit type	Description
1	DOCKI	D	Dot clock input
2	FH	D	Vertical synchronous output
3	VSYNC	D	Horizontal synchronous input
4	HSYNC	D	Vertical synchronous input
5	VGS	—	Device Ground
6	CPO	K	Charge pump output
7	VSS	—	Dot clock PLL ground
8	VDDI (PLL)	—	Dot clock PLL power supply
9	VDDR (2.5 V)	—	D/A power supply for R
10	VREF (1.1 V)	K	Voltage reference input
11	VRO (2.7 kΩ)	K	Resistor connection pin
12	RCOMP (0.1 μF)	K	Capacitor connection pin
13	ROUT	K	R output (Analog)
14	VSSR	—	D/A Ground for R
15	VDDG (2.5 V)	—	D/A power supply for G
16	GCOMP (0.1 μF)	K	Capacitor connection pin
17	GOUT	K	G output (Analog)
18	VSSG	—	Device Ground for G
19	VDDB (2.5 V)	—	D/A power supply for B
20	BCOMP (0.1 μF)	K	Capacitor connection pin
21	BOUT	K	B output (Analog)
22	VSSB	—	D/A Ground for B
23	AVCC	—	A/D Power Supply
24	AVRH	—	A/D reference power supply
25	AVSS/AVRL	—	A/D Ground
26	AN0	E	Analog input
27	AN1	E	Analog input
28	AN2	E	Analog input
29	AN3	E	Analog input
30	AN4	E	Analog input
31	AN5	E	Analog input
32	AN6	E	Analog input
33	AN7	E	Analog input
34	AN8	E	Analog input
35	AN9	E	Analog input

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Pin no.	Pin name	Circuit type	Description
36	P00	C	General-purpose port
	SCL0		I²C clock pin
37	P01	C	General-purpose port
	SDA0		I²C Data pin
38	P02	C	General-purpose port
	SCL1		I²C Clock
39	P03	C	General-purpose port
	SDA1		I²C Data pin
40	VDDE	—	3.3 V Power Supply
41	VDDI (PLL)	—	2.5 V Power Supply
42	X0	A	10 MHz oscillation pin
43	VSS	—	Ground
44	X1	A	10 MHz oscillation pin
45	$\overline{\text{INIT}}$	B	Initial (reset) pin
46	P04	C	General-purpose port
	SCL2		I²C clock
47	P05	C	General-purpose port
	SDA2		I²C Data pin
48	P06	N	General-purpose port
	SCL3		I²C clock
49	P07		General-purpose port
	SCL4		I²C clock
50	P10	N	General-purpose port
	SDA3		I²C data pin
51	P11		General-purpose port
	SDA4		I²C data pin
52	P12	C	General-purpose port
	SI0		UART0 serial input
53	P13	C	General-purpose port
	SO0		UART0 serial output
54	P14	C	General-purpose port
	SCK0		UART0 clock input/output
55	P15	C	General-purpose port
	SI1		UART1 serial input
56	P16	C	General-purpose port
	SO1		UART1 serial output

(Continued)

Pin no.	Pin name	Circuit type	Description
57	P17	C	General-purpose port
	SCK1		UART1 clock input/output
58	P20	C	General-purpose port
	SI2		UART2 serial input
59	P21	C	General-purpose port
	SO2		UART2 serial output
60	P22	C	General-purpose port
	SCK2		UART2 clock input/output
61	P23	C	General-purpose port
	SI3		UART3 serial input
62	P24	C	General-purpose port
	SO3		UART3 serial output
63	P25	C	General-purpose port
	SCK3		UART3 clock input/output
64	P30	C	General-purpose port
	SI4		UART4 serial input
	TIN0		Reload timer 0 trigger input
65	P31	C	General-purpose port
	SO4		UART4 serial output
	TIN1		Reload timer 1 trigger input
66	P32	C	General-purpose port
	SCK4		UART4 clock input/output
	TIN2		Reload timer 2 trigger input
67	P33	C	General-purpose port
	TO0		Reload timer 0 output
68	P34	C	General-purpose port
	TO1		Reload timer 1 output
69	P35	C	General-purpose port
	TO2		Reload timer 2 output
70	P36	C	General-purpose port
	RIN		PWC input
71	P40	C	General-purpose port
	TMO0		Multi-function timer 0 output
72	P41	C	General-purpose port
	TMO1		Multi-function timer 1 output

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Pin no.	Pin name	Circuit type	Description
73	P42	C	General-purpose port
	TMO2		Multi-function timer 2 output
74	P43	C	General-purpose port
	TMO3		Multi-function timer 3 output
75	VDDE	—	3.3 V power supply
76	VDDI	—	2.5 V power supply
77	X0A	A	32 kHz oscillation pin
78	VSS	—	Ground
79	X1A	A	32 kHz oscillation pin
80	P44	C	General-purpose port
	PPG0		PPG0 output
81	P45	C	General-purpose port
	PPG1		PPG1 output
82	P46	C	General-purpose port
	PPG2		PPG2 output
83	P47	C	General-purpose port
	PPG3		PPG3 output
84	MD0	F	Mode Pin
85	MD1	F	Mode Pin
86	MD2	F	Mode Pin
87	MD3	F	Mode Pin (ground)
88	P50	C	General-purpose port
	TMI0		Multi-function timer 0 input
89	P51	C	General-purpose port
	TMI1		Multi-function timer 1 input
90	P52	C	General-purpose port
	TMI2		Multi-function timer 2 input
91	P53	C	General-purpose port
	TMI3		Multi-function timer 3 input
92	P54	—	General-purpose port
	TRG0		PPG0 trigger input
93	P55	—	General-purpose port
	TRG1		PPG1 trigger input
94	P56	—	General-purpose port
	TRG2		PPG2 trigger input

(Continued)

Pin no.	Pin name	Circuit type	Description
95	P57	C	General-purpose port
	TRG3		PPG3 trigger input
96	P60	C	General-purpose port
	ATRG		A/D conversion trigger input
97	P61	C	General-purpose port
98	P62	O	General-purpose port
	INT0		External interrupt input 0
99	P63	O	General-purpose port
	INT1		External interrupt input 1
100	P64	O	General-purpose port
	INT2		External interrupt input 2
101	P65	O	General-purpose port
	INT3		External interrupt input 3
102	$\overline{\text{NMI}}$	B	$\overline{\text{NMI}}$ input
103	VDDE	—	3.3 V power supply
104	VDDI	—	2.5 V power supply
105	VSS	—	Ground
106	$\overline{\text{TRST}}$	B	DSU tool reset
107	ICLK	C	DSU clock
108	IBREAK	L	DSU break
109	ICS0	M	DSU status
110	ICS1	M	DSU status
111	ICS2	M	DSU status
112	ICD0	H	DSU data
113	ICD1	H	DSU data
114	ICD2	H	DSU data
115	ICD3	H	DSU data
116	P70	I	General-purpose port
117	P71	C	General-purpose port
118	P72	C	General-purpose port
119	P73	C	General-purpose port
120	P74	H	General-purpose port
121	X0B	A	48 MHz oscillation pin
122	VSS	—	Ground

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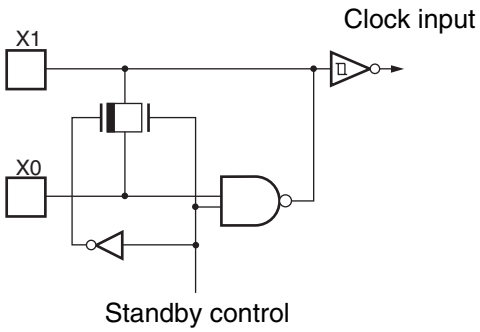
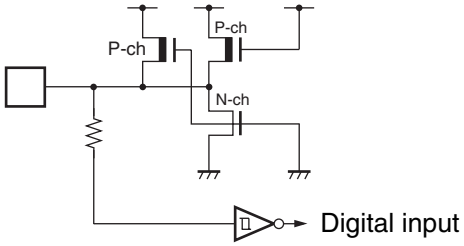
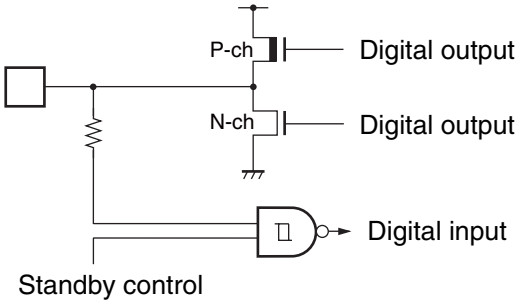
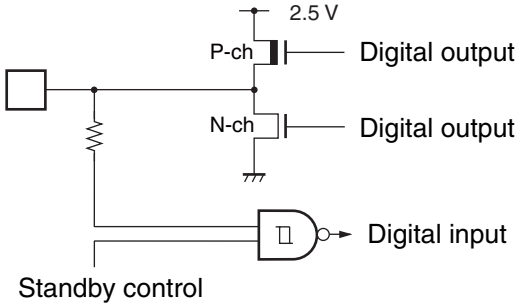
Pin no.	Pin name	Circuit type	Description
123	X1B	A	48 MHz oscillation pin
124	VDDI	—	2.5 V power supply
125	VDDE	—	3.3 V power supply
126	UDM	USB	USB-Function
127	UDP		USB-Function
128	UHM	USB	USB-Host
129	UHP		USB-Host
130	B0	D	RGB digital output
131	B1	D	RGB digital output
132	B2	D	RGB digital output
133	G0	D	RGB digital output
134	G1	D	RGB digital output
135	G2	D	RGB digital output
136	R0	D	RGB digital output
137	R1	D	RGB digital output
138	R2	D	RGB digital output
139	VSS	—	Ground
140	VDDI	—	2.5 V power supply
141	VDDE	—	3.3 V power supply
142	VOB2	D	Semi Transparent color period output
143	VOB1	D	OSD display period output
144	DCKO	D	Dot clock output

■ I/O CIRCUIT TYPE

Type	Circuit type	Remarks
A		Oscillation circuit
B		• CMOS hysteresis input • With pull-up resistance
C		• CMOS level output. • CMOS level hysteresis input • With standby control
D		• 2.5 V CMOS level output. • CMOS level hysteresis input • With standby control

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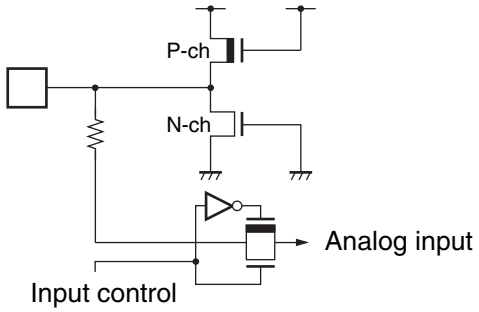
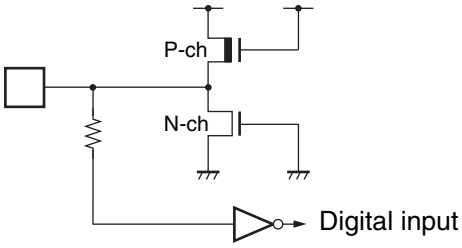
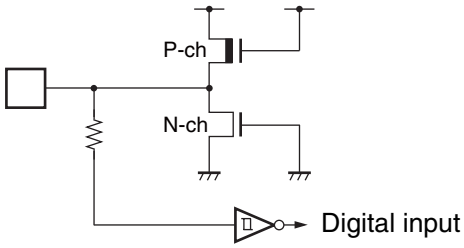
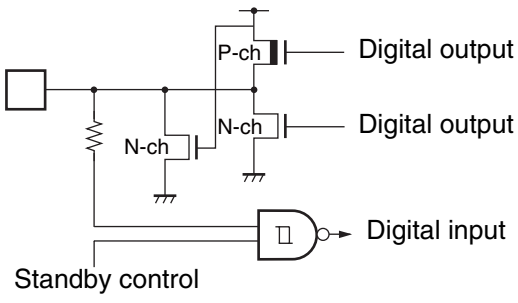
Type	Circuit type	Remarks
E		Analog input with switch
F		• CMOS level input • Without standby control
G		• CMOS level hysteresis input • Without standby control
H		• CMOS level output • Hysteresis input • Standby control provided • Pull-down resistor provided

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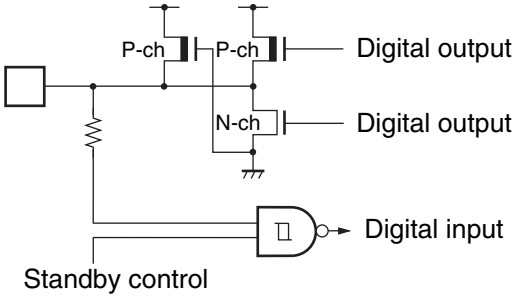
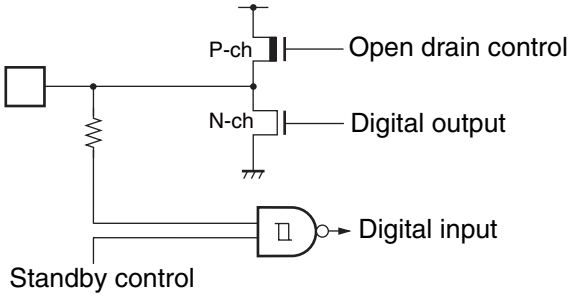
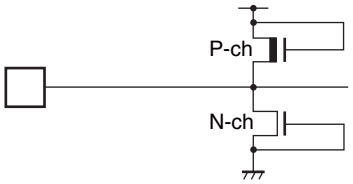
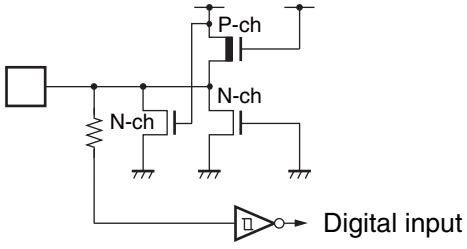
Type	Circuit type	Remarks
I		• CMOS level output • Hysteresis input • Standby control provided • Pull-up resistor provided
J		• Open drain output • CMOS level hysteresis input • With standby control
K		Analog pin
L		• CMOS hysteresis input • With pull-down resistance

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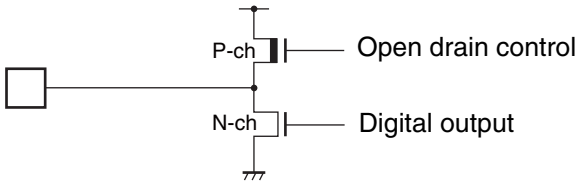
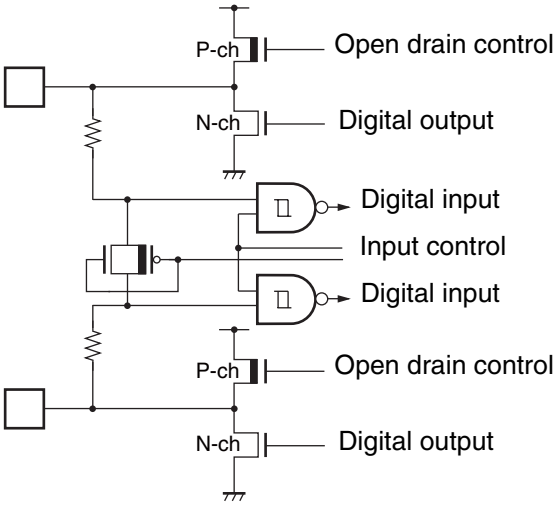
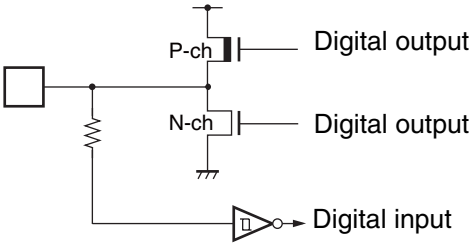
Type	Circuit type	Remarks
M		CMOS level output
N		• Two ports for I²C • CMOS hysteresis input • CMOS output • Stop control provided
O		• CMOS level output • CMOS hysteresis input

■ HANDLING DEVICES

• Preventing Latch-up

Latch-up may occur in a CMOS IC if a voltage greater than VDDE, VDDI or less than V_{SS} is applied to an input or output pin or if an above-rating voltage is applied between power supply and GND pins. A latch-up,if it occurs, significantly increases the power supply current and may cause thermal destruction of an element. When you use a CMOS IC, be very careful not to exceed the maximum rating.

• Treatment of Unused Input Pins

Do not leave an unused input pin open, since it may cause a malfunction. Handle by, for example, using a pull-up or pull-down resistor.

• About Power Supply Pins

If there are multiple power supply and GND pins, from the point of view of device design, pins to be of the same potential are connected the inside of the device to prevent such malfunctioning as latch up. To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the power supply and GND pins to the power supply and ground externally. The power pins should be connected to power supply and GND pins of this device at the lowest possible impedance from the current supply source.
It is also advisable to connect a ceramic bypass capacitor of approximately 0.1μF between power supply and GND pins near this device.

• About Crystal Oscillator Circuit

Noise near the X0 and X1 pin may cause the device to malfunction. When designing a PC board using the device, place the X0 and X1 pins, the crystal (or ceramic) oscillator, and the bypass capacitor leading to the ground as close to one another as possible.
It is strongly recommended to design PC board so that X0 and X1 pins are surrounded by grounding area for stable operation.

• About Mode Pins (MD0 to MD3)

These pins should be connected directly to power supply or GND pins. To prevent the device erroneously switching to test mode due to noise, design the printed circuit board such that the distance between the mode pins and VCC or VSS is as short as possible and the connection impedance is low.

• About Tool Reset Pin ($\overline{\text{TRST}}$)

This pin must input the same signal as that to $\overline{\text{INIT}}$ when the tool is not used. Apply the same treatment to mass-produced products as well.

• Operation at Start-up

A setting initialization reset (INIT) must always be performed via the $\overline{\text{INIT}}$ pin immediately after the power supply is turned on or recycled.
Immediately after the power supply is turned on, hold the Low level input to the $\overline{\text{INIT}}$ pin for the settling time required for the oscillator circuit to take the oscillation stabilization wait time for the oscillator circuit. (For INIT via the $\overline{\text{INIT}}$ pin, the oscillation stabilization wait time setting is initialized to the minimum value.)

• Oscillation Input at Power-ON

When turning the power on, maintain clock input until the device is released from the oscillation stabilization wait state.

• Notes on Power-ON/shut-down

Cautions to take when turning on/off VDDI (2.5 V internal power supply) and VDDE (3.3 V external-pin power supply)

Do not apply VDDE (external) alone continuously (for over an indication of one minute) with VDDI (internal) disconnected not to cause a reliability problem with the LSI.

When VDDE (external) returns from the OFF state to the ON state, the circuit may fail to hold its internal state, for example, due to power supply noise.

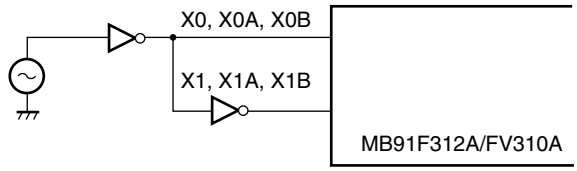
When the power is turned on	VDDI (internal)→ VDDE (external) → Analog → Signal
When the power is turned off	Signal → Analog → VDDE (external) → VDDI (internal)

• Undefined Output on Power-ON

When the power supply is turned on, the output pin may remain indeterminate until the internal power supply becomes stable.

• About the attention when the external clock is used

When the external clock is used, in principle, supply a clock signal to the X0 (X0A, X0B) pin and an opposite-phase clock signal to the X1 (X1A, X1B) pin at the same time. However, In this case. the stop mode must not be used.(This is because, in STOP mode, the X1 (X1A, X1B) pin stops at “H” output.) At 12.5 MHz or less, the device can be used with the clock signal supplied only to the X0 (X0A, X0B) pin.
An example of using the external clock is illustrated below.



[STOP mode (oscillation stop mode) cannot be used.]
External clock usage (normal)

External clock usage (enabled at 12.5 MHz Max.)

Note : The X1 (X1A, X1B) pin must be designed to have a delay within 15 ns, at 10 MHz, from the signal to the X0 (X0A, X0B) pin.

• Restrictions
Common in the MB91310 series

(1) Clock Control Block

Take the oscillation stabilization wait time during Low level input to the $\overline{INIT}$ pin.

(2) Bit Search Module

The 0-detection data register (BSD0), 1-detection data register (BSD1), and transition-detection data register (BSDC) are only word-accessible.

(3) I/O Port

Ports are accessed only in bytes.

(4) Low Power Consumption Mode

To enter the standby mode, use the synchronous standby mode (set with the SYNCS bit as bit 8 in the TBCR, or time-base counter control register) and be sure to use the following sequence:

```
(LDI #value_of_standby, R0)
(LDI #_STCR, R12)
STB R0, @R12            : Write to standby control register (STCR)
LDUB    @R12, R0        : STCR lead for synchronous standby
LDUB    @R12, R0        : Dummy re-lead of STCR
NOP                     : NOP × 5 for timing adjustment
NOP
NOP
NOP
NOP
```

In addition, set the I-flag and the ILM and ICR registers to branch to an interrupt handler when the interrupt handler triggers the microcontroller to return from the standby mode.
Please do not do the following when the monitor debugger is used.

- Set a break point within the above array of instructions
- Single-step the above instructions

(5) Pre-fetch

When accessing a prefetch-enabled little endian area, be sure to use word access (in 32-bit, word length) only. Byte or half-word access results in wrong data read.

(6) Notes on the PS register

As the PS register is processed by some instructions in advance, exception handling below may cause the interrupt handling routine to break when the debugger is used or the display contents of flags in the PS register to be updated.
As the microcontroller is designed to carry out reprocessing correctly upon returning from such an EIT event, it performs operations before and after the EIT as specified in either case.

1. The following operations are performed when (c) the instruction followed by a data event or a DIVOU/DIVOS emulator menu instruction (a) receives a user interrupt or NMI or (b) breaks when single-stepped.

- The D0 and D1 flags are updated in advance.
- An EIT handling routine (user interrupt, NMI, or emulator) is executed.
- Upon returning from the EIT, the DIVOU/DIVOS instruction is executed and the D0 and D1 flags are updated to the same values as in (1).

2. The following operations are performed when the ORCCR/STILM/MOV Ri and PS instructions are executed.

- The PS register is updated in advance.
- An EIT handling routine (user interrupt or NMI) is executed.
- Upon returning from the EIT, the above instructions are executed and the PS register is updated to the same value as in (1).

(7) Watchdog Timer

The watchdog timer built in this model monitors a program to check that it defers a reset within a certain period of time. The watchdog timer resets the CPU if the program runs out of controls, preventing the reset defer function from being executed. Once the function of the watchdog timer is enabled, therefore, the watchdog timer keeps on watching programs until it resets the CPU.
As an exception, the watchdog timer defers a reset automatically under the condition in which the CPU stops program execution.Refer to the watchdog timer function description for the exceptional condition in Hardware manual.
If the system runs out of control and develops the above condition, a watchdog reset may not be generated.
In that case, please reset (INIT) by external $\overline{\text{INIT}}$ terminal.

(8) Notes on using the A/D converter

The MB91310 series contains an A/D converter. Supply power to the AVCC pin at 3.3 V.

Unique to the evaluation chip MB91FV310A

(1) Simultaneous occurrences of a software break and a user interrupt/NMI

If a software break and a user interrupt/NMI occurs simultaneously, the emulator debugger may react as follows.

- The debugger stops pointing to a location other than the programmed break points.
- The halted program is not re - executed correctly.

If this symptom occurs, use a hardware break in place of a hardware break. If you use the monitor debugger, do not set a break point within the relevant array of instructions.

(2) Single-stepping of the RETI instruction

If an interrupt occurs frequently during single stepping, execute only the relevant processing routine repeatedly after single-stepping RETI. This will prevent the main routine and low-interrupt-level programs from being executed. Do not single-step the RETI instruction for avoidance purposes. When the debugging of the relevant interrupt routine becomes unnecessary, perform debugging with that interrupt disabled.

(3) About an Operand Break

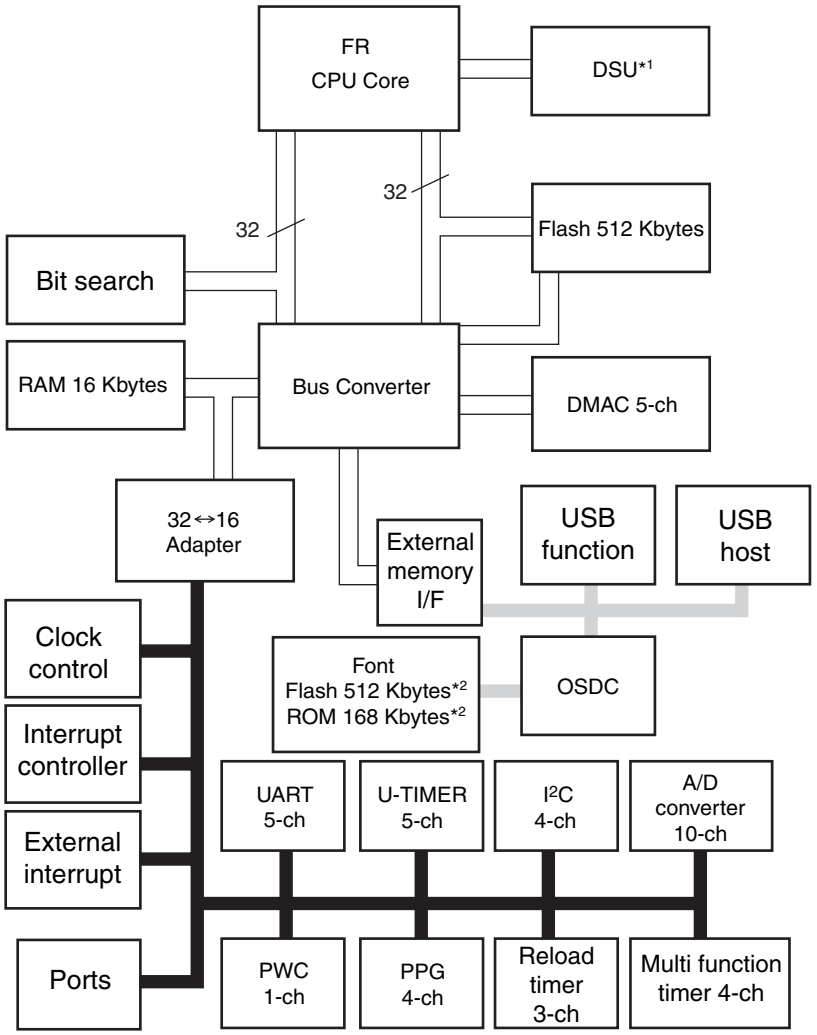
Do not apply a data event break to access to the area containing the address of a stack pointer.

(4) Sample Batch File for Configuration

To debug a program downloaded to internal RAM, be sure to execute the following batch file after executing RESET.

```
# Set MODR (0x7fd)  = Enable In memory + 16-bit External Bus
set mem/byte 0x7fd = 0x5
```

■ BLOCK DIAGRAM



*1 : DSU: MB91FV310A only

*2 : Font ROM : MB91FV310A: Flash 512 Kbytes
: MB91F312A: MASK ROM 168 Kbytes

■ MEMORY SPACE

1. Memory space

The FR family has 4 Gbytes of logical address space (2^{32} addresses) available to the CPU by linear access.

Direct Addressing Areas

The following address space areas are used as I/O areas.
These areas are called direct addressing areas, in which the address of an operand can be specified directly during an instruction.
The size of directly addressable areas depends on the length of the data being accessed as shown below.

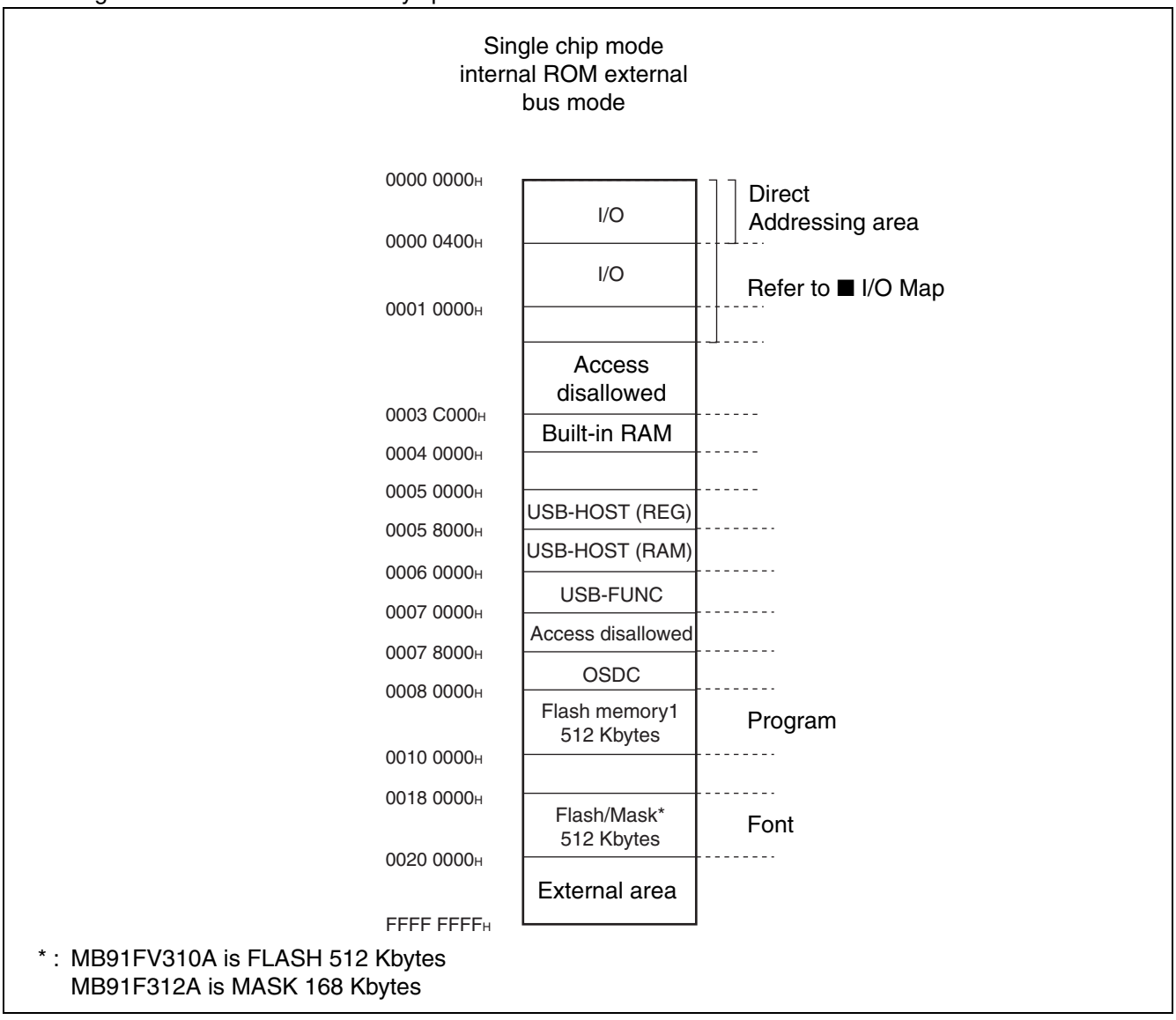
→ byte data access : 000H to 0FFH

→ half word data access : 000H to 1FFH

→ word data access : 000H to 3FFH

2. Memory Map

The figure below shows the memory space of the this item kind.

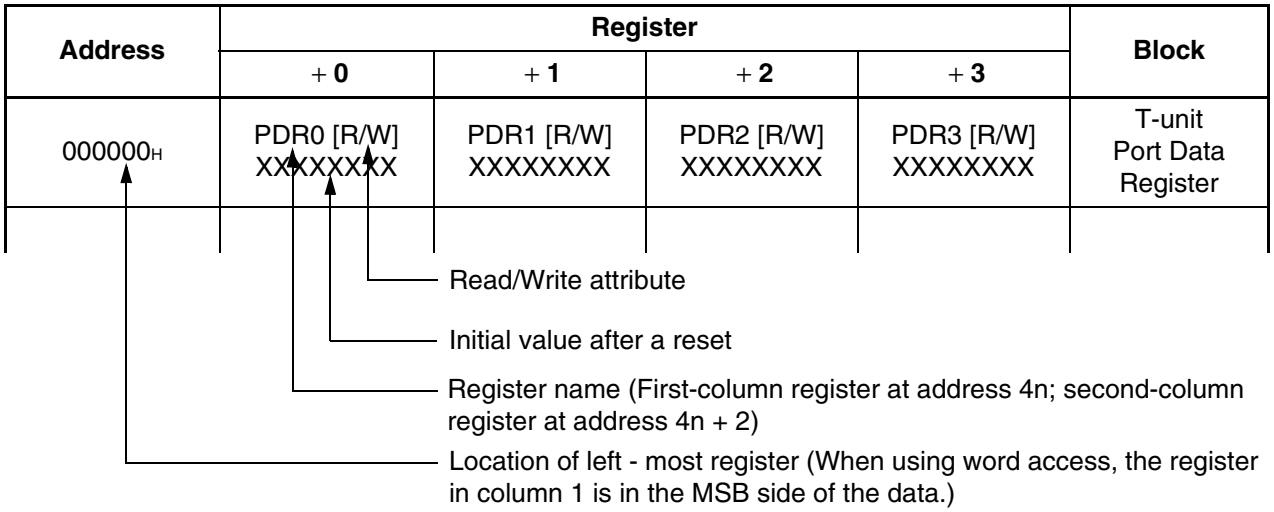


* : MB91FV310A is FLASH 512 Kbytes
MB91F312A is MASK 168 Kbytes

■ I/O MAP

This shows the location of the various peripheral resource registers in the memory space.

[How to read the table]



Note:Initial values of register bits are represented as follows:

- “1” : Initial Value: “1”
- “0” : Initial Value: “0”
- “X” : Initial Value: “X”
- “-” : No physical register at this location

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000000H to 00000FH	—	—	—	—	Reserved
000010H	PDR0 [R/W] XXXXXXXX	PDR1 [R/W] XXXXXXXX	PDR2 [R/W] --XXXXXX	PDR3 [R/W] -XXXXXXX	R-bus Port Data Register
000014H	PDR4 [R/W] XXXXXXXX	PDR5 [R/W] XXXXXXXX	PDR6 [R/W] --XXXXXX	PDR7 [R/W] ---XXXXX	
000018H	—				
00001CH	—				
000020H	ADCTH [R/W] XXXXXX00	ADCTL [R/W] 00000X00	ADCH [R/W] 00000000 00000000		10-bit A/D converter
000024H	ADAT0 [R] XXXXXX00 00000000		ADAT1 [R] XXXXXX00 00000000		
000028H	ADAT2 [R] XXXXXX00 00000000		ADAT3 [R] XXXXXX00 00000000		
00002CH	ADAT4 [R] XXXXXX00 00000000		ADAT5 [R] XXXXXX00 00000000		
000030H	ADAT6 [R] XXXXXX00 00000000		ADAT7 [R] XXXXXX00 00000000		
000034H	ADAT8 [R] XXXXXX00 00000000		ADAT9 [R] XXXXXX00 00000000		
000038H	—				Reserved
00003CH	—				
000040H	EIRR [R/W] 00000000	ENIR [R/W] 00000000	ELVR [R/W] 00000000		Ext int
000044H	DICR [R/W] -------0	HRCL [R/W] 0--11111	—		DLYI/I-unit
000048H	TMRLR0 [W] XXXXXXXX XXXXXXXX		TMR0 [R] XXXXXXXX XXXXXXXX		Reload Timer 0
00004CH	—		TMCSR0 [R/W] ----0000 00000000		
000050H	TMRLR1 [W] XXXXXXXX XXXXXXXX		TMR1 [R] XXXXXXXX XXXXXXXX		Reload Timer 1
000054H	—		TMCSR1 [R/W] ----0000 00000000		
000058H	TMRLR2 [W] XXXXXXXX XXXXXXXX		TMR2 [R] XXXXXXXX XXXXXXXX		Reload Timer 2
00005CH	—		TMCSR2 [R/W] ----0000 00000000		

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000060H	SSR [R/W] 00001-00	SIDR [R/W] XXXXXXXX	SCR [R/W] 00000100	SMR [R/W] 00--0-0-	UART0
000064H	UTIM [R] (UTIMR [W]) 00000000 00000000		DRCL [W] --------	UTIMC [R/W] 0--00001	U-TIMER 0
000068H	SSR [R/W] 00001-00	SIDR [R/W] XXXXXXXX	SCR [R/W] 00000100	SMR [R/W] 00--0-0-	UART1
00006CH	UTIM [R] (UTIMR [W]) 00000000 00000000		DRCL [W] --------	UTIMC [R/W] 0--00001	U-TIMER 1
000070H	SSR [R/W] 00001-00	SIDR [R/W] XXXXXXXX	SCR [R/W] 00000100	SMR [R/W] 00--0-0-	UART2
000074H	UTIM [R] (UTIMR [W]) 00000000 00000000		DRCL [W] --------	UTIMC [R/W] 0--00001	U-TIMER 2
000078H	SSR [R/W] 00001-00	SIDR [R/W] XXXXXXXX	SCR [R/W] 00000100	SMR [R/W] 00--0-0-	UART3
00007CH	UTIM [R] (UTIMR [W]) 00000000 00000000		DRCL [W] --------	UTIMC [R/W] 0--00001	U-TIMER 3
000080H	SSR [R/W] 00001-00	SIDR [R/W] XXXXXXXX	SCR [R/W] 00000100	SMR [R/W] 00--0-0-	UART4
000084H	UTIM [R] (UTIMR [W]) 00000000 00000000		DRCL [W] --------	UTIMC [R/W] 0--00001	U-TIMER 4
000088H	—		—		Reserved
00008CH	—		—		
000090H	PWCCL[R/W] 0000--00	PWCCH[R/W] 00-00000	—		PWC
000094H	PWCD [R] XXXXXXXX XXXXXXXX		—		
000098H	—		—		Reserved
00009CH	—		—		
0000A0H	—		—		
0000A4H	—		—		
0000A8H	—		—		
0000ACH	—		—		
0000B0H	—	—	—	—	
0000B4H	IBCR [R/W] 00000000	IBSR [R/W] 00000000	ITBA [R/W] ------00 00000000		I²C interface ch.0
0000B8H	ITMK [R/W] 00----11 11111111		ISMK [R/W] 01111111	ISBA [R/W] 00000000	
0000BCH	—	IDAR [R/W] 00000000	ICCR [R/W] 0-011111	IDBL [R/W] -------0	
0000C0H	—	—	—	—	Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000C4H	IBCR [R/W] 00000000	IBSR [R/W] 00000000	ITBA [R/W] ------00 00000000		I²C interface ch.1
0000C8H	ITMK [R/W] 00----11 11111111		ISMK [R/W] 01111111	ISBA [R/W] 00000000	
0000CCH	—	IDAR [R/W] 00000000	ICCR [R/W] 0-011111	IDBL [R/W] -------0	
0000D0H	—	—	—	—	Reserved
0000D4H	IBCR [R/W] 00000000	IBSR [R/W] 00000000	ITBA [R/W] ------00 00000000		I²C interface ch.2
0000D8H	ITMK [R/W] 00----11 11111111		ISMK [R/W] 01111111	ISBA [R/W] 00000000	
0000DCH	—	IDAR [R/W] 00000000	ICCR [R/W] 0-011111	IDBL [R/W] -------0	
0000E0H	—	—	—	—	Reserved
0000E4H	IBCR [R/W] 00000000	IBSR [R/W] 00000000	ITBA [R/W] ------00 00000000		I²C interface ch.3
0000E8H	ITMK [R/W] 00----11 11111111		ISMK [R/W] 01111111	ISBA [R/W] 00000000	
0000ECH	—	IDAR [R/W] 00000000	ICCR [R/W] 0-011111	IDBL [R/W] -------0	
0000F0H	T0LPCR [R/W] -----000	T0CCR [R/W] 0-010000	T0TCR [R/W] 00000000	T0R [R/W] ---00000	Multi-function timer
0000F4H	T0DRR [R/W] XXXXXXXX XXXXXXXX		T0CRR [R/W] XXXXXXXX XXXXXXXX		
0000F8H	T1LPCR [R/W] -----000	T1CCR [R/W] 0-000000	T1TCR [R/W] 00000000	T1R [R/W] ---00000	
0000FCH	T1DRR [R/W] XXXXXXXX XXXXXXXX		T1CRR [R/W] XXXXXXXX XXXXXXXX		
000100H	T2LPCR [R/W] -----000	T2CCR [R/W] 0-000000	T2TCR [R/W] 00000000	T2R [R/W] ---00000	
000104H	T2DRR [R/W] XXXXXXXX XXXXXXXX		T2CRR [R/W] XXXXXXXX XXXXXXXX		
000108H	T3LPCR [R/W] -----000	T3CCR [R/W] 0-000000	T3TCR [R/W] 00000000	T3R [R/W] ---00000	
00010CH	T3DRR [R/W] XXXXXXXX XXXXXXXX		T3CRR [R/W] XXXXXXXX XXXXXXXX		
000110H	—	—	—	—	Reserved
000120H	PTMR0 [R] 11111111 11111111		PCSR0 [W] XXXXXXXX XXXXXXXX		PPG0
000124H	PDUT0 [W] XXXXXXXX XXXXXXXX		PCNH0 [R/W] 00000000	PCNL0 [R/W] 00000000	

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000128H	PTMR1 [R] 11111111 11111111		PCSR1 [W] XXXXXXXX XXXXXXXX		PPG1
00012CH	PDUT1 [W] XXXXXXXX XXXXXXXX		PCNH1 [R/W] 00000000	PCNL1 [R/W] 00000000	
000130H	PTMR2 [R] 11111111 11111111		PCSR2 [W] XXXXXXXX XXXXXXXX		PPG2
000134H	PDUT2 [W] XXXXXXXX XXXXXXXX		PCNH2 [R/W] 00000000	PCNL2 [R/W] 00000000	
000138H	PTMR3 [R] 11111111 11111111		PCSR3 [W] XXXXXXXX XXXXXXXX		PPG3
00013CH	PDUT3 [W] XXXXXXXX XXXXXXXX		PCNH3 [R/W] 00000000	PCNL3 [R/W] 00000000	
000140H	—	—	—	—	Reserved
000144H	—	—	—	—	
000148H	—	—	—	—	
00014CH	—	—	—	—	
000150H	—	—	—	—	
000154H	—	—	—	—	
000158H	—	—	—	—	
00015CH	—	—	—	—	
000160H to 0001FCH	—	—	—	—	
000200H	DMACA0 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000204H	DMACB4 [R/W] 00000000 00000000 00000000 00000000				
000208H	DMACA1 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00020CH	DMACB4 [R/W] 00000000 00000000 00000000 00000000				
000210H	DMACA2 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000214H	DMACB4 [R/W] 00000000 00000000 00000000 00000000				
000218H	DMACA3 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00021CH	DMACB4 [R/W] 00000000 00000000 00000000 00000000				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000220H	DMACA4 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000224H	DMACB4 [R/W] 00000000 00000000 00000000 00000000				
000228H	—				
00022CH to 00023CH	—				Reserved
000240H	DMACR [R/W] 0XX00000 XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
000244H to 0002FCH	—				—
000300H to 0003ECH	—				
0003F0H	BSD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit Search Module
0003F4H	BSD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003F8H	BSDC [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003FCH	BSRR [R] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000400H	DDR0 [R/W] 00000000	DDR1 [R/W] 00000000	DDR2 [R/W] --000000	DDR3 [R/W] -0000000	R-bus Port Direction Register
000404H	DDR4 [R/W] 00000000	DDR5 [R/W] 00000000	DDR6 [R/W] --000000	DDR7 [R/W] ---00000	
000408H	—	—	—	—	
00040CH	—	—	—	—	
000410H	PFR0 [R/W] 0--00000	PFR1 [R/W] 00000000	PFR2 [R/W] 000---00	PFR3 [R/W] 00000000	R-bus Port Function Register
000414H	—	—	—	—	
000418H	—	—	—	—	
00041CH	—	—	—	—	
000420H to 00043CH	—				Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000440H	ICR00 [R/W] ---11111	ICR01 [R/W] ---11111	ICR02 [R/W] ---11111	ICR03 [R/W] ---11111	Interrupt Control unit
000444H	ICR04 [R/W] ---11111	ICR05 [R/W] ---11111	ICR06 [R/W] ---11111	ICR07 [R/W] ---11111	
000448H	ICR08 [R/W] ---11111	ICR09 [R/W] ---11111	ICR10 [R/W] ---11111	ICR11 [R/W] ---11111	
00044CH	ICR12 [R/W] ---11111	ICR13 [R/W] ---11111	ICR14 [R/W] ---11111	ICR15 [R/W] ---11111	
000450H	ICR16 [R/W] ---11111	ICR17 [R/W] ---11111	ICR18 [R/W] ---11111	ICR19 [R/W] ---11111	
000454H	ICR20 [R/W] ---11111	ICR21 [R/W] ---11111	ICR22 [R/W] ---11111	ICR23 [R/W] ---11111	
000458H	ICR24 [R/W] ---11111	ICR25 [R/W] ---11111	ICR26 [R/W] ---11111	ICR27 [R/W] ---11111	
00045CH	ICR28 [R/W] ---11111	ICR29 [R/W] ---11111	ICR30 [R/W] ---11111	ICR31 [R/W] ---11111	Interrupt Control unit
000460H	ICR32 [R/W] ---11111	ICR33 [R/W] ---11111	ICR34 [R/W] ---11111	ICR35 [R/W] ---11111	
000464H	ICR36 [R/W] ---11111	ICR37 [R/W] ---11111	ICR38 [R/W] ---11111	ICR39 [R/W] ---11111	
000468H	ICR40 [R/W] ---11111	ICR41 [R/W] ---11111	ICR42 [R/W] ---11111	ICR43 [R/W] ---11111	
00046CH	ICR44 [R/W] ---11111	ICR45 [R/W] ---11111	ICR46 [R/W] ---11111	ICR47 [R/W] ---11111	
000470H to 00047CH	—				—
000480H	RSRR [R/W] 10000000*2	STCR [R/W] 00110011*2	TBCR [R/W] 00XXXX00*1	CTBR [W] XXXXXXXX	Clock Control unit
000484H	CLKR [R/W] 00000000*1	WPR [W] XXXXXXXX	DIVR0 [R/W] 00000011*1	DIVR1 [R/W] 00000000*1	
000488H	—	—	OSCCR [R/W] XXXXXXX0	—	—
00048CH	WPCR [R/W] B 00---000	—	—	—	Clock timer
000490H	OSCR [R/W] B 00---000	—	—	—	Oscillation Stabilization Waiting

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000494H to 0005FCH	—				Reserved
000600H	—	—	—	—	T-unit Port Direction Register
000604H	—	—	—	—	
000608H	—	—	—	—	
00060CH	—	—	—	—	
000610H	—	—	—	—	T-unit Port Function Register
000614H	—	—	—	—	
000618H	—	—	—	—	
00061CH	—	—	—	—	
000620H	—				
000624H	—				
000628H to 00063FH	—				Reserved
000640H	ASR0 [R/W] 00000000 00000000*1		ACR0 [R/W] 1111XX00 00000000*1		T-unit
000644H	ASR1 [R/W] XXXXXXXX XXXXXXXX*1		ACR1 [R/W] XXXXXXXX XXXXXXXX*1		
000648H	ASR2 [R/W] XXXXXXXX XXXXXXXX*1		ACR2 [R/W] XXXXXXXX XXXXXXXX*1		
00064CH	ASR3 [R/W] XXXXXXXX XXXXXXXX*1		ACR3 [R/W] XXXXXXXX XXXXXXXX*1		
000650H	ASR4 [R/W] XXXXXXXX XXXXXXXX*1		ACR4 [R/W] XXXXXXXX XXXXXXXX*1		
000654H	ASR5 [R/W] XXXXXXXX XXXXXXXX*1		ACR5 [R/W] XXXXXXXX XXXXXXXX*1		
000658H	ASR6 [R/W] XXXXXXXX XXXXXXXX*1		ACR6 [R/W] XXXXXXXX XXXXXXXX*1		
00065CH	ASR7 [R/W] XXXXXXXX XXXXXXXX*1		ACR7 [R/W] XXXXXXXX XXXXXXXX*1		
000660H	AWR0 [R/W] 01111111 11111111*1		AWR1 [R/W] XXXXXXXX XXXXXXXX*1		
000664H	AWR2 [R/W] XXXXXXXX XXXXXXXX*1		AWR3 [R/W] XXXXXXXX XXXXXXXX*1		
000668H	AWR4 [R/W] XXXXXXXX XXXXXXXX*1		AWR5 [R/W] XXXXXXXX XXXXXXXX*1		

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
00066C$_H$	AWR6 [R/W] XXXXXXXX XXXXXXXX*1		AWR7 [R/W] XXXXXXXX XXXXXXXX*1		T-unit
000670$_H$	—				
000674$_H$	—				
000678$_H$	IOWR0 [R/W] XXXXXXXX	IOWR1 [R/W] XXXXXXXX	IOWR2 [R/W] XXXXXXXX	—	
00067C$_H$	—				
000680$_H$	CSER [R/W] 00000001	CHER [R/W] 11111111	—	TCR [R/W] 00000000	
000684$_H$	—				
000684$_H$ to 0007F8$_H$	—				Reserved
0007FC$_H$	—	MODR [W] XXXXXXXX	—	—	—
000800$_H$ to 000AFC$_H$	—				Reserved
000B00$_H$	ESTS0 [R/W] X0000000	ESTS1 [R/W] XXXXXXXX	ESTS2 [R] 1XXXXXXX	—	DSU
000B04$_H$	ECTL0 [R/W] 0X000000	ECTL1 [R/W] 00000000	ECTL2 [W] 000X0000	ECTL3 [R/W] 00X00X11	
000B08$_H$	ECNT0 [W] XXXXXXXX	ECNT1 [W] XXXXXXXX	EUSA [W] XXX00000	EDTC [W] 0000XXXX	
000B0C$_H$	EWPT [R] 00000000 00000000		—		
000B10$_H$	EDTR0 [W] XXXXXXXX XXXXXXXX		EDTR1 [W] XXXXXXXX XXXXXXXX		
000B14$_H$ to 000B1C$_H$	—				
000B20$_H$	EIA0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B24$_H$	EIA1 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B28$_H$	EIA2 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B2C$_H$	EIA3 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B30$_H$	EIA4 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000B34H	EIA5 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DSU
000B38H	EIA6 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B3CH	EIA7 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B40H	EDTA [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B44H	EDTM [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B48H	EOA0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B4CH	EOA1 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B50H	EPCR [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B54H	EPSR [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B58H	EIAM0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B5CH	EIAM1 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B60H	EOAM0/EODM0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B64H	EOAM1/EODM1 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B68H	EOD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B6CH	EOD1 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B70H to 000FFCH	—				Reserved
001000H	DMASA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
001004H	DMADA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001008H	DMASA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00100CH	DMADA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
001010H	DMASA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
001014H	DMADA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001018H	DMASA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00101CH	DMADA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001020H	DMASA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001024H	DMADA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001028H to 006FFCH	—				Reserved
007000H	FLCR [R/W] 0110 X000	—			Program Flash I/F
007004H	FLWC [R/W] 0001 0011	—			
007008H to 00707CH	—				Reserved
007080H to 0070FCH	—				Reserved
007100H	FNCR [R/W] 0110 X000	—			Font Flash I/F
007104H	FNWC [R/W] 0001 0011	—			
050000H	HR (Hc Revision) [R] 00000000 00000000 00000001 00010000				USB Host
050004H	HC (Hc Control) [R/W] 00000000 00000000 00000000 00000000				
050008H	HCS (Hc Command Status) [R/W] 00000000 00000000 00000000 00000000				
05000CH	HIS (Hc Interrupt Status) [R/W] 00000000 00000000 00000000 00000000				
050010H	HIE (Hc Interrupt Enable) [R/W] 00000000 00000000 00000000 00000000				
050014H	HID (Hc Interrupt Disable) [R/W] 00000000 00000000 00000000 00000000				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
050018H	HHCCA (Hc HCCA) [R/W] 00000000 00000000 00000000 00000000				USB Host
05000CH	HPCED (Hc Period Current ED) [R/W] 00000000 00000000 00000000 00000000				
050020H	HCHED (Hc Control Head ED) [R/W] 00000000 00000000 00000000 00000000				
050024H	HCCED (Hc Control Current ED) [R/W] 00000000 00000000 00000000 00000000				
050028H	HBHED (Hc Bulk Head ED) [R/W] 00000000 00000000 00000000 00000000				
05002CH	HBCED (Hc Bulk Current ED) [R/W] 00000000 00000000 00000000 00000000				
050030H	HDH (Hc Done Head) [R/W] 00000000 00000000 00000000 00000000				
050034H	HFI (Hc Fm Interval) [R/W] 00000000 00000000 00101110 11011111				
050038H	HFR (Hc Fm Remaining) [R] 00000000 00000000 00000000 00000000				
05003CH	HFN (Hc Fm Number) [R] 00000000 00000000 00000000 00000000				
050040H	HPS (Hc Periodic Start) [R/W] 00000000 00000000 00000000 00000000				
050044H	HLST (Hc LS Threshold) [R/W] 00000000 00000000 00000110 00101000				
050048H	HRDA (Hc Rh Descriptor A) [R/W] 00000001 00000000 00000000 00000010				
05004CH	HRDB (Hc Rh Descriptor B) [R/W] 00000000 00000000 00000000 00000000				
050050H	HRS (Hc Rh Status) [R/W] 00000000 00000000 00000000 000000X0				
050054H	HRPS1 (Hc Rh Port Status[1]) [R/W] 00000000 00000000 00000000 00000X00				
050058H	HRPS2 (Hc Rh Port Status[2]) [R/W] 00000000 00000000 00000000 00000X00				
05005CH to 057FFFH	—				
058000H to 059FFFH	SRAM 8 Kbytes				
05A000H to 05FFFFH	—				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
060000H	FIFO0o [R] XXXXXXXX XXXXXXXX		FIFO0i [W] XXXXXXXX XXXXXXXX		USB Function
060004H	FIFO1 [R] XXXXXXXX XXXXXXXX		FIFO2 [W] XXXXXXXX XXXXXXXX		
060008H	FIFO3 [R] XXXXXXXX XXXXXXXX		—		
06000CH to 06001FH	—				
060020H	—		CONT1 [R/W] XXXXX0XX XXX00000		
060024H	CONT2 [R/W] XXXXXXXX XXX00000		CONT3 [R/W] XXXXXXXX XXX00000		
060028H	CONT4 [R/W] XXXXXXXX XXX00000		CONT5 [R/W] XXXXXXXX XXXX00XX		
06002CH	CONT6 [R/W] XXXXXXXX XXXX00XX		CONT7 [R/W] XXXXXXXX XXX00000		
060030H	CONT8 [R/W] XXXXXXXX XXX00000		CONT9 [R/W] XXXX0000 X000000X		
060034H	CONT10 [R/W] XXXXXXXX 0XXX0000		TTSIZE [R/W] 00010001 00010001		
060038H	TRSIZE [R/W] 00010001 00010001		—		
06003CH	—				
060040H	RSIZE0 [R] XXXXXXXX XXXX0000		—		
060044H	RSIZE1 [R] XXXXXXXX X0000000		—		
060048H to 06005FH	—				
060060H	—		ST1 [R/W] XXXXXX00 00000000		
060064H	—				
060068H	ST2 [R] XXXXXXXX XXX00000		ST3 [R/W] XXXXXXXX XXX00000		
06006CH	ST4 [R/W] XXXXX000 00000000		ST5 [R/W] XXXX0XXX XX000000		

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
060070H to 06FFFBH	—				USB Function
06FFFCH	—	—	RESET [R/W] 00000---	—	
070000H to 077FFFH	—				Reserved
078000H	OSD_VADR [R/W] XXXXXXXX XXXXXXXX		OSD_CD1 [R/W] XXXXXXXX XXXXXXXX		OSDC
078004H	OSD_CD2 [R/W] XXXXXXXX XXXXXXXX		OSD_RCD1 [R/W] XXXXXXXX XXXXXXXX		
078008H	OSD_RCD2 [R/W] XXXXXXXX XXXXXXXX		OSD_SOC1 [R/W] XXXXXXXX 0000XXXX		
07800CH	OSD_SOC2 [R/W] XXXXXXXX XXXXXXXX		OSD_VDPC [R/W] XXXXXXXX XXXXXXXX		
078010H	OSD_HDPC [R/W] XXXXXXXX XXXXXXXX		OSD_CVSC [R/W] XXXXXXXX XXXXXXXX		
078014H	OSD_SBFCC [R/W] XXXXXXXX XXXXXXXX		OSD_THCC [R/W] XXXXXXXX XXXXXXXX		
078018H	OSD_GFCC [R/W] XXXXXXXX XXXXXXXX		OSD_SBCC1 [R/W] XXXXXXXX XXXXXXXX		
07801CH	OSD_SBCC2 [R/W] XXXXXXXX XXXXXXXX		OSD_SPCC1 [R/W] XXXXXXXX XXXXXXXX		
078020H	OSD_SPCC2 [R/W] XXXXXXXX XXXXXXXX		OSD_SPCC3 [R/W] XXXXXXXX XXXXXXXX		
078024H	OSD_SPCC4 [R/W] XXXXXXXX XXXXXXXX		OSD_SYNCC [R/W] XXXXXXXX XXXXXXXX		
078028H	OSD_DCLKC1 [R/W] XXXXXXXX XXXXXXXX		OSD_DCLKC2 [R/W] XXXXXXXX XXXXXXXX		
07802CH	OSD_DCLKC3 [R/W] XXXXXXXX XXXXXXXX		OSD_IOC1 [R/W] XXXXXXXX XXXXXX00		
078030H	OSD_IOC2 [R/W] XXXXXXXX XXXXXXXX		OSD_DPC1 [R/W] XXXXXXXX XXXXXXXX		
078034H	OSD_DPC2 [R/W] XXXXXXXX XXXXXXXX		OSD_DPC3 [R/W] XXXXXXXX XXXXXXXX		
078038H	OSD_DPC4 [R/W] XXXXXXXX XXXXXXXX		OSD_IRC [R/W] XXXXXXXX XXXXXXXX		

(Continued)

(Continued)

Address	Register				Block
	+ **0**	+ **1**	+ **2**	+ **3**	
07803C$_H$	OSD_PLT0 [R/W] XXXXXXXX XXXXXXXX		OSD_PLT1 [R/W] XXXXXXXX XXXXXXXX		OSDC
078040$_H$	OSD_PLT2 [R/W] XXXXXXXX XXXXXXXX		OSD_PLT3 [R/W] XXXXXXXX XXXXXXXX		
078044$_H$	OSD_PLT4 [R/W] XXXXXXXX XXXXXXXX		OSD_PLT5 [R/W] XXXXXXXX XXXXXXXX		
078048$_H$	OSD_PLT6 [R/W] XXXXXXXX XXXXXXXX		OSD_PLT7 [R/W] XXXXXXXX XXXXXXXX		
07804C$_H$	OSD_PLT8 [R/W] XXXXXXXX XXXXXXXX		OSD_PLT9 [R/W] XXXXXXXX XXXXXXXX		
078050$_H$	OSD_PLT10 [R/W] XXXXXXXX XXXXXXXX		OSD_PLT11 [R/W] XXXXXXXX XXXXXXXX		
078054$_H$	OSD_PLT12 [R/W] XXXXXXXX XXXXXXXX		OSD_PLT13 [R/W] XXXXXXXX XXXXXXXX		
078058$_H$	OSD_PLT14 [R/W] XXXXXXXX XXXXXXXX		OSD_PLT15 [R/W] XXXXXXXX XXXXXXXX		
07805C$_H$	OSD_ACT1 [R/W] XXXXXXXX XXXXXXXX		OSD_ACT2 [R/W] XXXXXXXX XXXXXXXX		
078060$_H$ to 07FFFF$_H$	—				Reserved

*1 : The initial value of the register varies with the reset level. The initial value shown is the one after an INIT level reset.

*2 : The initial value of the register varies with the reset level. The initial value shown is the one after an INIT level reset by the $\overline{\text{INIT}}$ pin.

■ INTERRUPT SOURCE, INTERRUPT VECTOR AND INTERRUPT REGISTER ASSIGNMENT

Interrupt source	Interrupt number		Interrupt level	Offset	Address of TBR default	RN
	10	16				
Reset	0	00	—	3FC$_H$	000FFFFC$_H$	—
Mode vector	1	01	—	3F8$_H$	000FFFF8$_H$	—
System reserved	2	02	—	3F4$_H$	000FFFF4$_H$	—
System reserved	3	03	—	3F0$_H$	000FFFF0$_H$	—
System reserved	4	04	—	3EC$_H$	000FFFEC$_H$	—
System reserved	5	05	—	3E8$_H$	000FFFE8$_H$	—
System reserved	6	06	—	3E4$_H$	000FFFE4$_H$	—
Coprocessor absent trap	7	07	—	3E0$_H$	000FFFE0$_H$	—
Coprocessor error trap	8	08	—	3DC$_H$	000FFFDC$_H$	—
INTE instruction	9	09	—	3D8$_H$	000FFFD8$_H$	—
Instruction break exception	10	0A	—	3D4$_H$	000FFFD4$_H$	—
Operand break trap	11	0B	—	3D0$_H$	000FFFD0$_H$	—
Step trace trap	12	0C	—	3CC$_H$	000FFFCC$_H$	—
NMI request (tool)	13	0D	—	3C8$_H$	000FFFC8$_H$	—
Undefined instruction exception	14	0E	—	3C4$_H$	000FFFC4$_H$	—
NMI request	15	0F	15 (F$_H$) fixed	3C0$_H$	000FFFC0$_H$	—
External interrupt 0	16	10	ICR00	3BC$_H$	000FFFBC$_H$	—
External interrupt 1	17	11	ICR01	3B8$_H$	000FFFB8$_H$	—
External interrupt 2	18	12	ICR02	3B4$_H$	000FFFB4$_H$	—
External interrupt 3	19	13	ICR03	3B0$_H$	000FFFB0$_H$	—
External interrupt 4 (USB-function)	20	14	ICR04	3AC$_H$	000FFFAC$_H$	—
External interrupt 5 (USB-Host)	21	15	ICR05	3A8$_H$	000FFFA8$_H$	—
External interrupt 6 (OSDC)	22	16	ICR06	3A4$_H$	000FFFA4$_H$	—
External interrupt 7	23	17	ICR07	3A0$_H$	000FFFA0$_H$	—
Reload timer 0	24	18	ICR08	39C$_H$	000FFF9C$_H$	8
Reload timer 1	25	19	ICR09	398$_H$	000FFF98$_H$	9
Reload timer 2	26	1A	ICR10	394$_H$	000FFF94$_H$	10
UART0(Reception completed)	27	1B	ICR11	390$_H$	000FFF90$_H$	0
UART1(Reception completed)	28	1C	ICR12	38C$_H$	000FFF8C$_H$	1
UART2(Reception completed)	29	1D	ICR13	388$_H$	000FFF88$_H$	2
UART0 (RX completed)	30	1E	ICR14	384$_H$	000FFF84$_H$	3
UART1 (RX completed)	31	1F	ICR15	380$_H$	000FFF80$_H$	4
UART2 (RX completed)	32	20	ICR16	37C$_H$	000FFF7C$_H$	5

(Continued)

Interrupt source	Interrupt number		Interrupt level	Offset	Address of TBR default	RN
	10	16				
DMAC0 (end, error)	33	21	ICR17	378H	000FFF78H	—
DMAC1 (end, error)	34	22	ICR18	374H	000FFF74H	—
DMAC2 (end, error)	35	23	ICR19	370H	000FFF70H	—
DMAC3 (end, error)	36	24	ICR20	36CH	000FFF6CH	—
DMAC4 (end, error)	37	25	ICR21	368H	000FFF68H	—
A/D converter	38	26	ICR22	364H	000FFF64H	—
PPG0	39	27	ICR23	360H	000FFF60H	—
PPG1	40	28	ICR24	35CH	000FFF5CH	—
PPG2	41	29	ICR25	358H	000FFF58H	—
PPG3	42	2A	ICR26	354H	000FFF54H	—
PWC	43	2B	ICR27	350H	000FFF50H	—
System reserved	44	2C	ICR28	34CH	000FFF4CH	—
System reserved	45	2D	ICR29	348H	000FFF48H	—
Main oscillation stabilization	46	2E	ICR30	344H	000FFF44H	—
Timebase timer overflow	47	2F	ICR31	340H	000FFF40H	—
System reserved	48	30	ICR32	33CH	000FFF3CH	—
Clock timer	49	31	ICR33	338H	000FFF38H	—
I²C ch.0	50	32	ICR34	334H	000FFF34H	—
I²C ch.1	51	33	ICR35	330H	000FFF30H	—
I²C ch.2	52	34	ICR36	32CH	000FFF2CH	—
I²C ch.3	53	35	ICR37	328H	000FFF28H	—
UART3(Reception completed)	54	36	ICR38	324H	000FFF24H	—
UART4(Reception completed)	55	37	ICR39	320H	000FFF20H	—
UART3 (RX completed)	56	38	ICR40	31CH	000FFF1CH	—
UART4(Reception completed)	57	39	ICR41	318H	000FFF18H	—
timer0	58	3A	ICR42	314H	000FFF14H	—
timer1	59	3B	ICR43	310H	000FFF10H	—
timer2	60	3C	ICR44	30CH	000FFF0CH	—
timer3	61	3D	ICR45	308H	000FFF08H	—
System reserved	62	3E	ICR46	304H	000FFF04H	—
Delay interrupt source bit	63	3F	ICR47	300H	000FFF00H	—
System reserved (Used by REALOS)	64	40	—	2FCH	000FFEFCH	—
System reserved (Used by REALOS)	65	41	—	2F8H	000FFEF8H	—
System reserved	66	42	—	2F4H	000FFEF4H	—

(Continued)

(Continued)

Interrupt source	Interrupt number		Interrupt level	Offset	Address of TBR default	RN
	10	16				
System reserved	67	43	—	2F0H	000FFEF0H	—
System reserved	68	44	—	2ECH	000FFEECH	—
System reserved	69	45	—	2E8H	000FFEE8H	—
System reserved	70	46	—	2E4H	000FFEE4H	—
System reserved	71	47	—	2E0H	000FFEE0H	—
System reserved	72	48	—	2DCH	000FFEDCH	—
System reserved	73	49	—	2D8H	000FFED8H	—
System reserved	74	4A	—	2D4H	000FFED4H	—
System reserved	75	4B	—	2D0H	000FFED0H	—
System reserved	76	4C	—	2CCH	000FFECCH	—
System reserved	77	4D	—	2C8H	000FFEC8H	—
System reserved	78	4E	—	2C4H	000FFEC4H	—
System reserved	79	4F	—	2C0H	000FFEC0H	—
Used by INT instruction	80 to 255	50 to FF	—	2BCH to 000H	000FFEBCH to 000FFC00H	—

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage	V_{DDE} (3.3 V)	Vss – 0.5	Vss + 4.0	V
	V_{DDI} (2.5 V)	Vss – 0.5	Vss + 3.0	V
Analog power supply voltage	AV_{CC}	Vss – 0.5	Vss + 4.0	V
Input voltage	V_I	Vss – 0.5	Vcc + 0.5	V
Analog pin input voltage	V_{IA}	Vss – 0.5	AVcc + 0.5	V
Output voltage	V_O	Vss – 0.5	Vcc + 0.5	V
Storage temperature	Tstg	– 40	+ 125	°C

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

Parameter	Symbol	Value		Unit
		Min	Max	
Operating temperature	Ta	– 10	+ 70	°C
Power supply voltage	V_{DDE} (3.3 V)	3.00	3.6	V
	V_{DDI} (2.5 V)	2.30	2.70	
Analog power supply voltage	AV_{CC}	3.00	3.60	V

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

3. DC Characteristics

($Ta = -10\ °C$ to $+70\ °C$, $V_{DDE} = 3.3\ V \pm 0.3\ V$, $V_{DDI} = 2.5\ V \pm 0.2\ V$, $Vss = 0\ V$)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Power supply	I_{CC}	ROM product during normal operation Ta = +25 °C, fcp = 40 MHz, fcpp = 20 MHz	—	200	250	mA	MB91F312A Dot clock@90 MHz
				220	270		MB91FV310A Dot clock@90 MHz
	I_{CCS}	Main sleep mode Ta = +25 °C, fcp = 40 MHz, fcpp = 20 MHz	—	150	180	mA	MB91F312A Dot clock PLL STOP
				170	200		MB91FV310A Dot clock PLL STOP
	I_{CCL}	Sub RUN mode Ta = +25 °C, fclk = 32 kHz	—	800	1500	µA	MB91F312A Dot clock PLL stop USB clock stop
				1300	2000		MB91FV310A Dot clock PLL stop USB clock stop
	I_{CCH}	Main stop mode Ta = +25 °C, fclk = 0	—	70	150	µA	MB91F312A
				570	650		MB91FV310A
		Ta = +70 °C, fclk = 0	—	500	2000	µA	MB91F312A
				1000	2500		MB91FV310A
	I_{CCT}	Clock mode Ta = +25 °C, fclk = 32 kHz	—	600	1000	µA	MB91F312A Dot clock PLL stop USB clock stop
				1100	1500		MB91FV310A Dot clock PLL stop USB clock stop
H level input voltage	V_{IH}	*1	$V_{CC} \times 0.8$	—	V_{CC}	V	
L level input voltage	V_{IL}	$V_{CC} = 3.3\ V$*1	V_{SS}	—	$V_{CC} \times 0.2$	V	
		$V_{CC} = 2.5\ V$			$V_{CC} \times 0.15$	V	
H level output voltage	V_{OH}	$V_{DDE} = 3.3\ V$, $I_{OH} = -4\ mA$*2	$V_{CC} - 0.5$	—	V_{CC}	V	
		$V_{DDE} = 2.5\ V$, $I_{OH} = -4\ mA$*3	$V_{CC} - 0.5$	—	V_{CC}	V	
L level output voltage	V_{OL}	$V_{DDE} = 3.3\ V$, $I_{OL} = 4\ mA$*2,*3	V_{SS}	—	0.4	V	
Input leak current	I_{IL}	Ta = +70 °C	−5	—	+5	µA	
I²C bus switch connection resister	RBS	—	—	—	130	Ω	Between SCL3 and SCL4 Between SDA3 and SDA4

*1 : P00 to P07, P10 to P17, P20 to P25, P30 to P36, P40 to P47, P50 to P57, P60 to P65, P70 to P74, DOCKI, HSYNC, VSYNC

*2 : P00 to P07, P10 to P17, P20 to P25, P30 to P36, P40 to P47, P50 to P57, P60 to P65, P70 to P74

*3 : B0 to B2, G0 to B2, R0 to R2, VOB1, VOB2, DCKO, FH

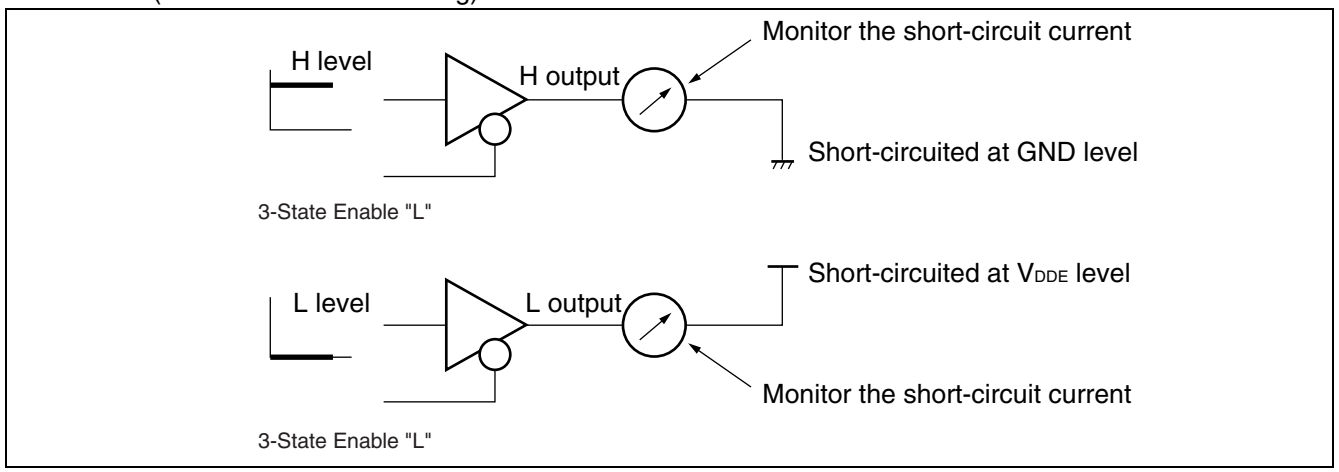
4. USB

(1) DC Characteristics

(Ta = − 10 °C to + 70 °C, V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 2.5 V ± 0.2 V, Vss = 0 V)

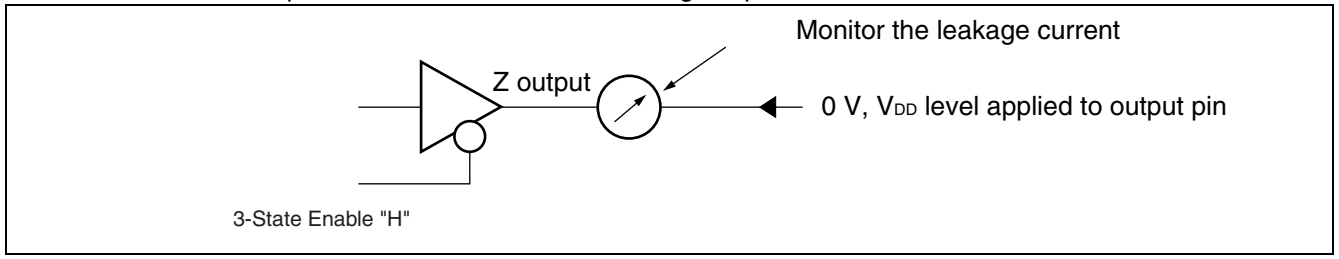
Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
H level output voltage	V_{OH}	—	I_{OH} = − 100 µA	V_{DDE} − 0.2	—	V_{DDE}	V	
Output Level Voltage	V_{OL}	—	I_{OL} = 100 µA	0	—	0.2	V	
H level output current	I_{OH}	—	Full Speed V_{OH} = V_{DDE} − 0.4 V	− 20	—	—	mA	
			Low Speed V_{OH} = V_{DDE} − 0.4 V	− 6	—	—		
L level output current	I_{OL}	—	Full Speed V_{OL} = 0.4 V	20	—	—	mA	
			Low Speed V_{OL} = 0.4 V	6	—	—		
output short circuit current	I_{OS}	—	—	—	—	300	mA	*1
Input leak current	I_{LZ}	—	—	—	—	± 5	µA	*2

*1 : About the output short-circuit current I_{OS}
The output short-circuit current IOS is the maximum current that flows when the output pin is connected to VDDE or VSS (within the maximum rating).



About the output short-circuit current: This is the short-circuit current per differential output pin on one side. As this USB I/O buffer is a differential output, consider both of the two pins.

*2 : About Z leakage current I_{LZ} measurement
The input leakage current I_{LZ} indicates the leakage current that flows when the V_{DDE} or V_{SS} voltage is applied to the bidirectional pin with the USB I/O buffer in a high impedance state.



(2) DC characteristics

Conforming to the USB Specification Revision 1.1.

(Ta = − 10 °C to + 70 °C, V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 2.5 V ± 0.2 V, Vss = 0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
"H" level input voltage (driven)	V_{IH}	2.0	—	V	*1
"L" level input voltage	V_{IL}	—	0.8	V	*1
Differential Input Sensitivity	V_{DI}	0.2	—	V	*2
Differential Common Mode Range	V_{CM}	0.8	2.5	V	*2
"H" level output voltage (driven)	V_{OH}	2.8	3.6	V	*3
"L" level output voltage	V_{OL}	0.0	0.3	V	*3
External Output Signal Crossover Voltage	V_{CRS}	1.3	2.0	V	*4
Bus Pull-Up Resistor on Upstream Port	RPU	1.425	1.575	kΩ	1.5 kΩ ± 5%
Bus Pull-Down Resistor on Downstream Port	RPD	1.425	1.575	kΩ	1.5 kΩ ± 5%
Termination voltage for upstream port pull-up	V_{TERM}	3.0	3.6	V	*5

*1 : About input voltages V_{IH} and V_{IL}

The Single-End-Receiver switching threshold voltage of the USB I/O buffer is set within the range of V_{IL} (Max) = 0.8 V and V_{IH} (Min) = 2.0 V (TTL input standard).

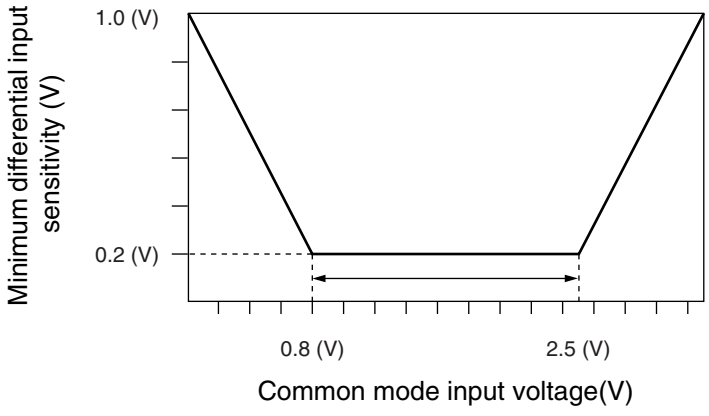
Appropriate hysteresis is provided to reduce noise sensitivity.

*2 : About input voltages V_{DI} and V_{CM}

The Differential-Receiver is used to receive USB differential data signals.

The Differential-Receiver has a differential input sensitivity of 200 mV when the differential data input remains in the range of 0.8 to 2.5 V to the local ground reference level.

The above voltage range is referred to as the common mode input voltage range.



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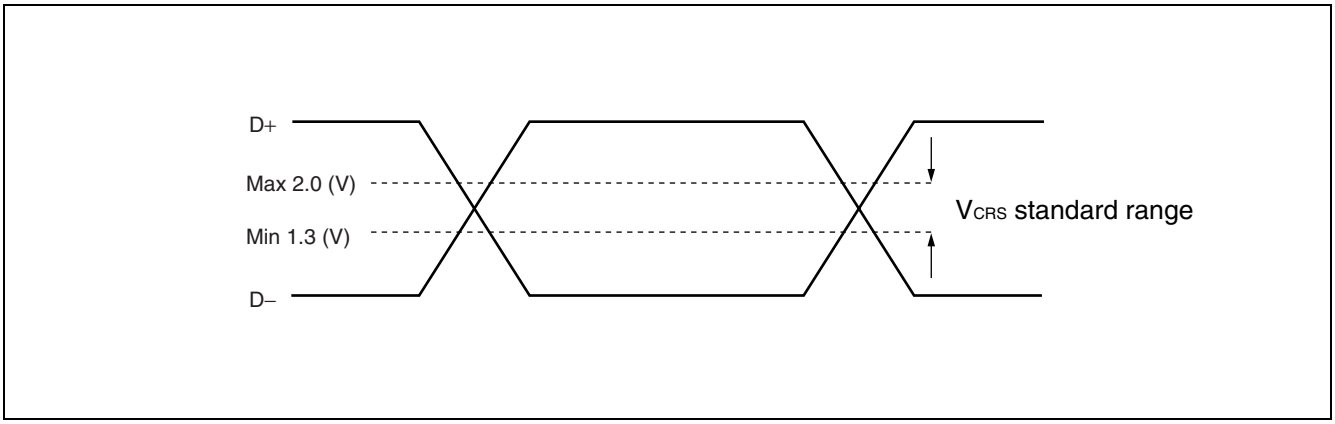
*3 : About output voltages V_{OL} and V_{OH}
The output drive capabilities of the driver are 0.3 V or less in Low-State (V_{OL}) (when 1.5 kΩ is loaded at 3.6 V) and 2.8 V or more in High-State (V_{OH}) (when 15 kΩ is loaded at the ground).

*4 : About output voltages V_{CRS}
The cross voltage of the external differential output signal (D+/D-) of the USB I/O buffer ranges from 1.3 V to 2.0 V.



*5 : About termination V_{TERM}
V_{TERM} represents the pull-up voltage at the upstream port.

5. AC Characteristics

(1) Clock Timing

(Ta = − 10 °C to + 70 °C, V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 2.5 V ± 0.2 V, Vss = 0 V)

Parameter	Symbol	Pin name	Condi-tions	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	fc	X0, X1	—	—	10.135	—	MHz	PLL system (Operation at a maximum internal speed of 40.54 MHz by quadrupling a self-oscillation frequency of 10.135 MHz via PLL)
Internal operating clock frequency	fcp	—	—	2.53	—	40.54	MHz	CPU
	fcpp	—	—	2.53	—	20.27	MHz	Peripheral

(2) Reset

(Ta = − 10 °C to + 70 °C, V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 2.5 V ± 0.2 V, Vss = 0 V)

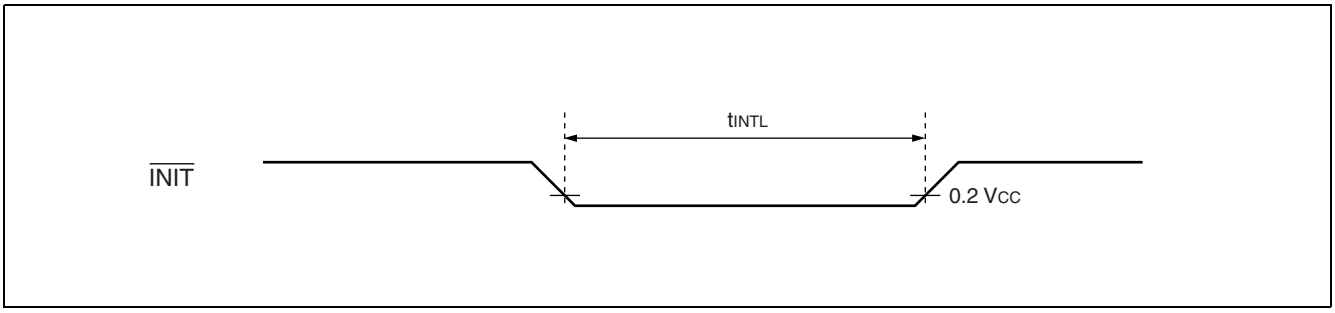
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
INIT input time (at power-on)	t_{INTL}	$\overline{INIT}$	—	*	—	ns
INIT input time (other than at power - on)				$t_{CP} \times 5$	—	ns
INIT input time (stop recovery time)				*	—	ns

* : INIT input time (at power-on)

FAR, CERALOCK : $\phi \times 2^{15}$ or greater recommended

Crystal : $\phi \times 2^{21}$ or greater recommended

ϕ : Power on → X0/X1 period × 2



(3) UART timing

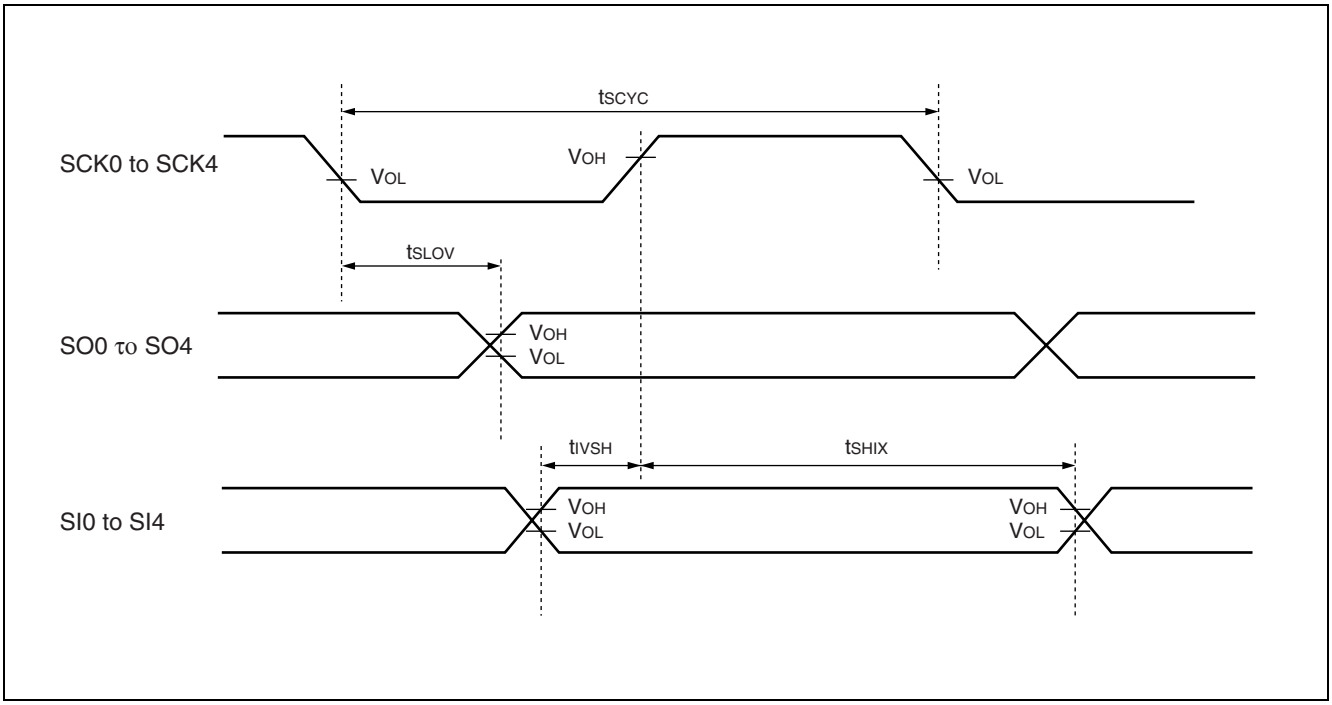
(Ta = − 10 °C to + 70 °C, V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 2.5 V ± 0.2 V, Vss = 0 V)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK4	internal shift lock mode	8 t_{CYCP}*	—	ns
SCK↓ → SO delay time	t_{SLOV}	SCK0 to SCK4 SO0 to SO4		− 80	+ 80	ns
Valid SI →SCK↑	t_{IVSH}	SCK0 to SCK4 SI0 to SI4		100	—	ns
SCK↑ → valid SI hold time	t_{SHIX}	SCK0 to SCK4 SI0 to SI4		60	—	ns
Serial clock H pulse width	t_{SHSL}	SCK0 to SCK4	external shift lock mode	4 t_{CYCP}*	—	ns
Serial clock L pulse width	t_{SLSH}	SCK0 to SCK4		4 t_{CYCP}*	—	ns
SCK↓ → SO delay time	t_{SLOV}	SCK0 to SCK4 SO0 to SO4		—	150	ns
Valid SI →SCK↑	t_{IVSH}	SCK0 to SCK4 SI0 to SI4		60	—	ns
SCK↑ → valid SI hold time	t_{SHIX}	SCK0 to SCK4 SI0 to SI4		60	—	ns

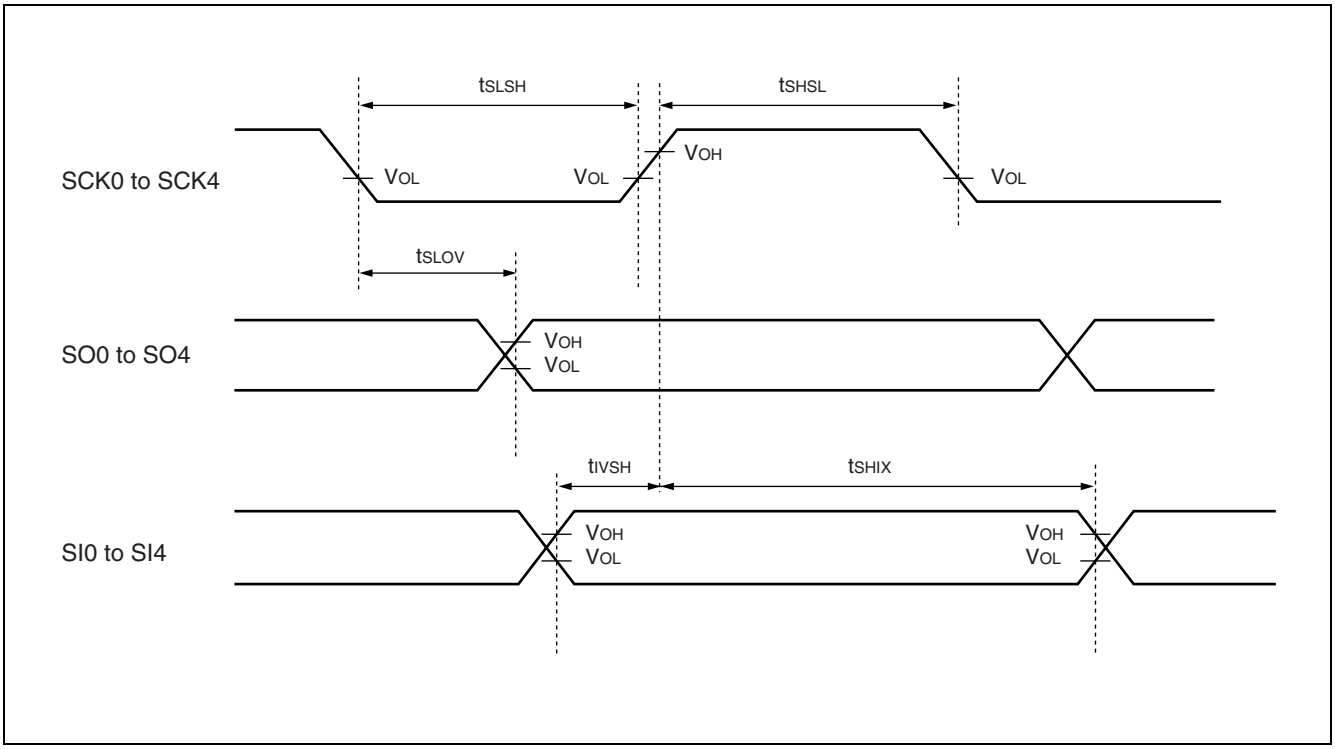
* : t_{CYCP} indicates the peripheral clock cycle time.

Note : AC characteristic in CLK synchronized mode.

• Internal shift clock mode



• External shift clock mode



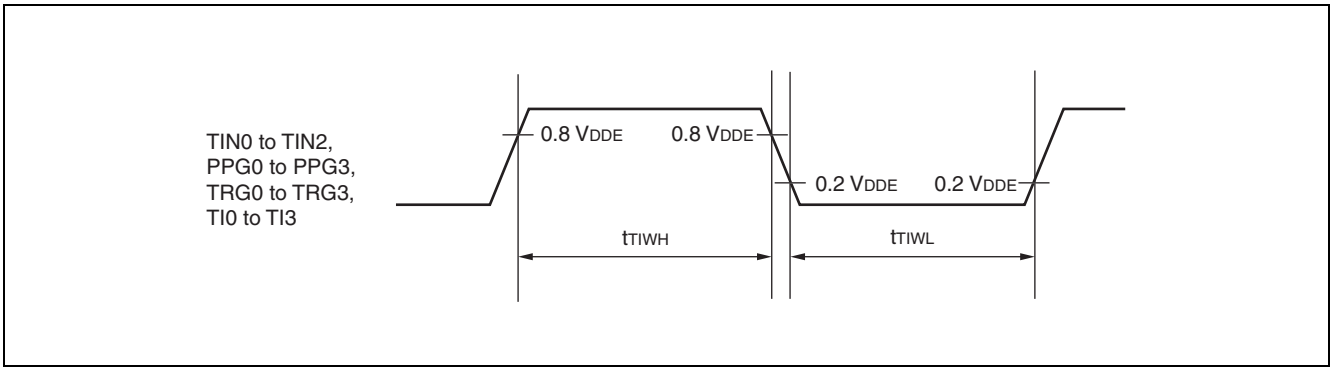
(4) Reload timer clock, PPG timer input, and multi-function timer input timings

(Ta = − 10 °C to + 70 °C, V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 2.5 V ± 0.2 V, Vss = 0 V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH} t_{TIWL}	TIN0 to TIN2 PPG0 to PPG3 TRG0 to TRG3 TI0 to TI3	—	2 t_{CYCP}	—	ns	*1
		INT0 to INT3		3 t_{CYCP}	—	ns	*1
				1.0	—	µs	*2

*1 : t_{CYCP} indicates the peripheral clock cycle time.

*2 : When in stop mode.

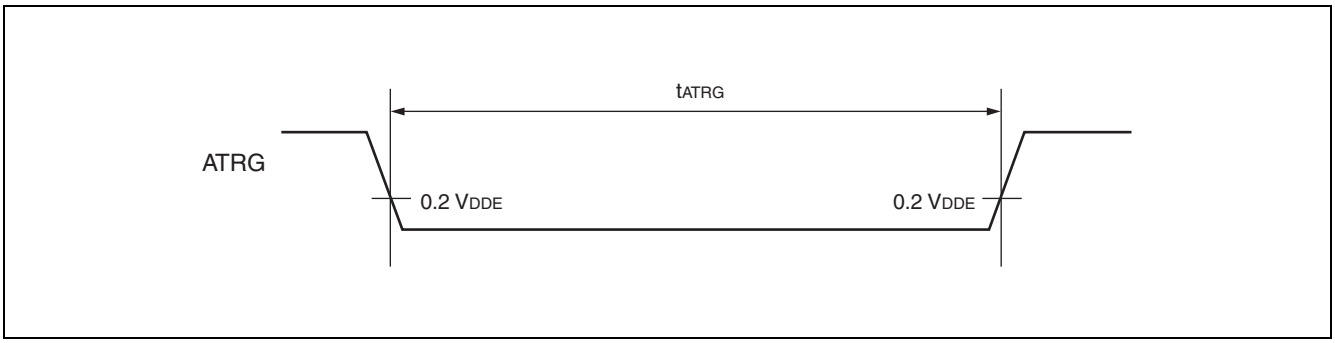


(5) Trigger Input Timing

(Ta = − 10 °C to + 70 °C, V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 2.5 V ± 0.2 V, Vss = 0 V)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
A/D activation trigger input time	t_{ATRG}	ATRG	—	5 t_{CYCP}*	—	ns

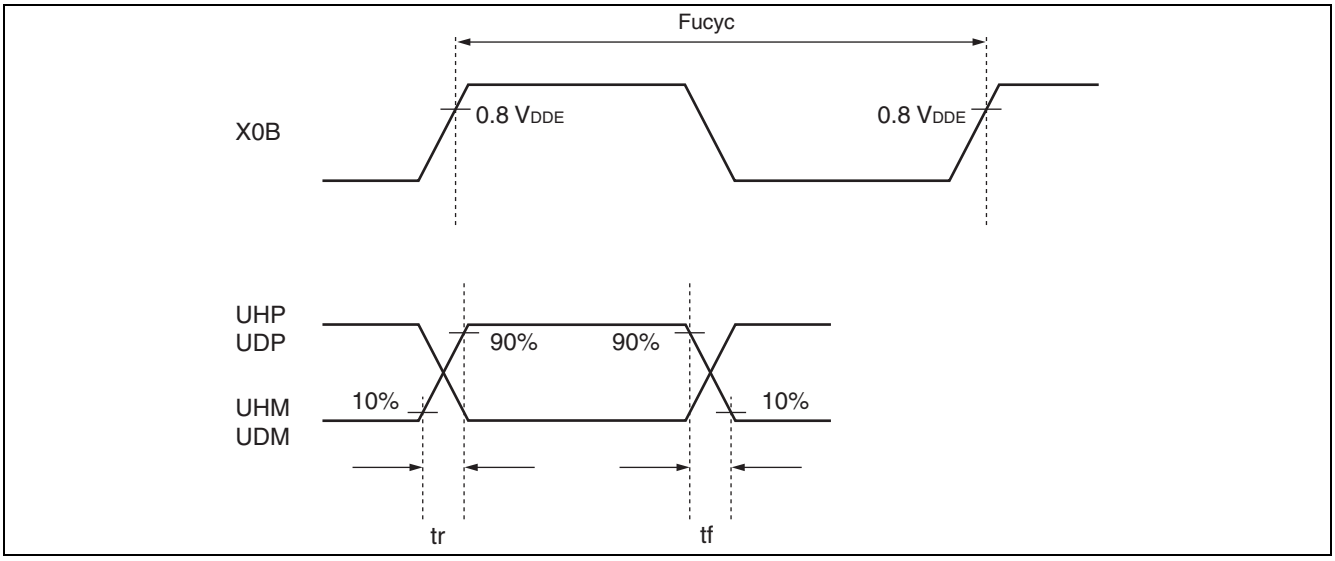
* : t_{CYCP} indicates the peripheral clock cycle time.



(6) USB interface

(Ta = − 10 °C to + 70 °C, V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 2.5 V ± 0.2 V, Vss = 0 V)

Parameter	Symbol	Pin name	Condi-tions	Value			Unit	Remarks
				Min	Typ	Max		
Input clock	Fucyc	X0B, X1B	—	—	48 *1	—	MHz	Self-oscillation at a precision of 500 ppm *1
		X0B						External input at a precision of 500 ppm *1
Rise Time	tr	UHP/UHM UDP/UDM	Full Speed	4	—	20	ns	*2
		UHP/UHM	Low Speed	75	—	300	ns	*2
Fall Time	tf	UHP/UHM UDP/UDM	Full Speed	4	—	20	ns	*2
		UHP/UHM	Low Speed	75	—	300	ns	*2
Differential Rise and Fall Timing Matching	Tfrfm	UHP/UHM UDP/UDM	Full Speed	90	—	111.11	%	*2
		UHP/UHM	Low Speed	80	—	125	%	*2
Driver Output Resistance	Rzdrv	UDP UDM	—	28	—	44	Ω	*3



*1 : The AC characteristics of the USB interface conform to the USB Specification Revision 1.1.

*2 : About driver characteristics tr, tf, and Tfrfm
These represent the rise (tr) and fall (tf) time standards of the differential data signal.
These are defined as times between 10% and 90% of the output signal voltage.
For full-speed buffer, the tr/tf ratio is specified to fall within ± 10% to minimize RFI radiation.

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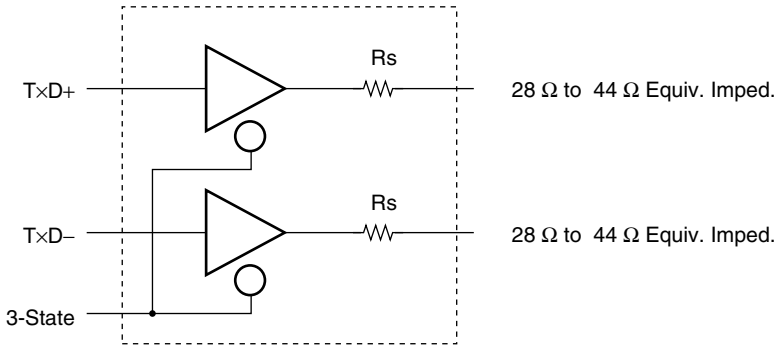
*3 : About driver characteristic ZDRV
USB full-speed connection is made by the twisted pair cable shielded at a characteristic impedance (Z0) of 90 Ω ± 15%. The USB Specification stipulates that the USB driver output impedance be within the range of 28 Ω to 44 Ω. The USB Specification also stipulates that a discrete serial resistor (Rs) be added for balancing purposes while satisfying the above standards.
The output impedance of the USB I/O buffer in this LSI is about 3 Ω to 19 Ω.
As the serial resistor Rs, therefore, a 25 Ω to 30 Ω type (27 Ω type recommended) should be added.



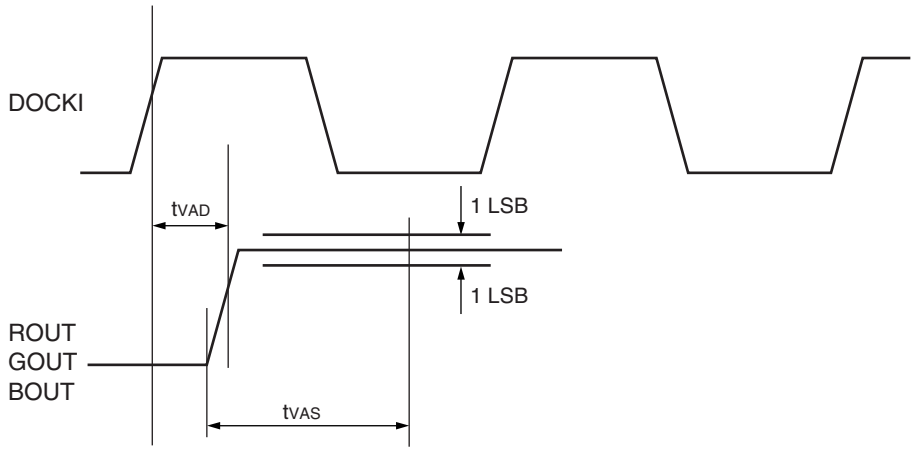
Driver output impedance 3 Ω to 19 Ω
Rs 25 Ω to 30 Ω (recommended value: 27 Ω)

(7) Analog RGB

(Ta = − 10 °C to + 70 °C, V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 2.5 V ± 0.2 V, Vss = 0 V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Analog RGB output delay	t_{VAD}	DOCKI ROUT, GOUT, BOUT	V_{REF} = 1.1 V, V_{DDR} = V_{DDG} = V_{DDB} = 2.5 V, V_{RO} = 2.7 kΩ, RCOMP = GCOMP = BCOMP = 0.1 µF	—	5	—	ns	—
Analog RGB output settling time	t_{VAS}	DOCKI ROUT, GOUT, BOUT		—	10	—	ns	—

• Display signal output timing



(8) Digital RGB

Vertical sync, horizontal sync, and display output control signal input timings

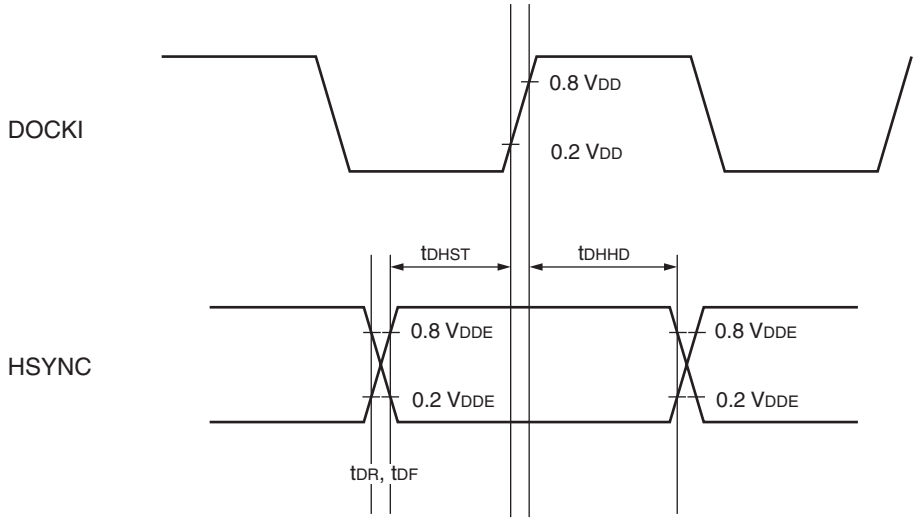
(Ta = − 10 °C to + 70 °C, V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 2.5 V ± 0.2 V, Vss = 0 V)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Horizontal sync signal cycle time	t_{HCYC}	HSYNC	100 + t_{WH}	—	Dot clock	
Horizontal sync signal pulse width	t_{WH}	HSYNC	20	—	Dot clock	*1
			—	6	µs	
Horizontal sync signal setup time	t_{DHST}	HSYNC	4	—	ns	
Horizontal sync signal hold time	t_{DHHD}		0	—	ns	
Vertical sync signal setup time	t_{HVST}	VSYNC	5	1H*2 − 5	Dot clock	
Vertical sync signal hold time	t_{HVHD}		3	—	H*2	
Input sync signal rise/fall time	t_{DR} t_{DF}	HSYNC VSYNC	—	5	ns	

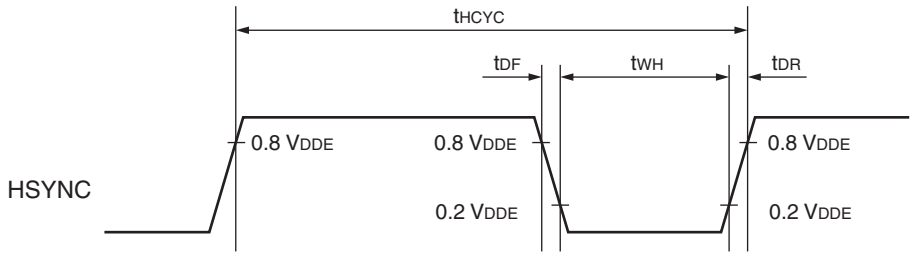
*1 : During the horizontal sync signal pulse period, the device stops its internal OSDC operation, disabling writing to the internal VRAM. Therefore, set the horizontal sync signal pulse width and VRAM write cycle to ensure that: horizontal sync signal pulse width < VRAM write cycle.
Precisely, adjust the command issuance interval not to issue command 2 or command 4 (VRAM write command) more than once in the horizontal sync signal pulse with period.
If the above condition is not satisfied, the device may fail writing to VRAM.

*2 : 1H is assumed to be one horizontal sync signal period.

• Horizontal sync, and display output control signal input timings

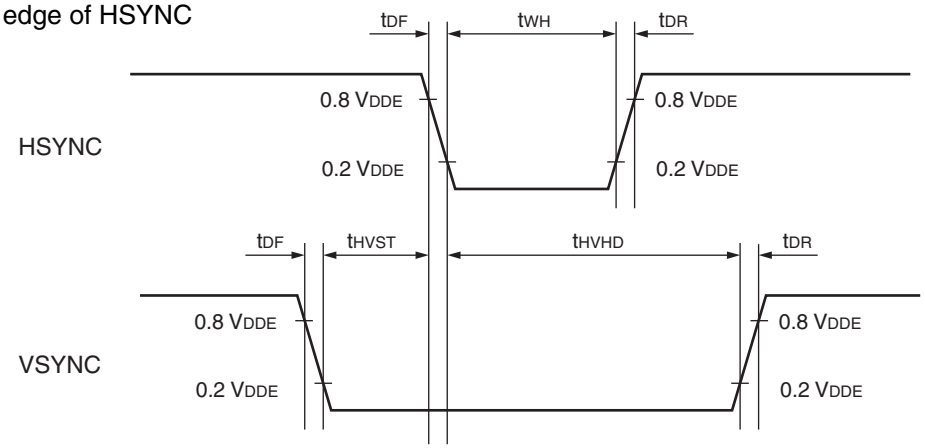


• Horizontal sync signal input

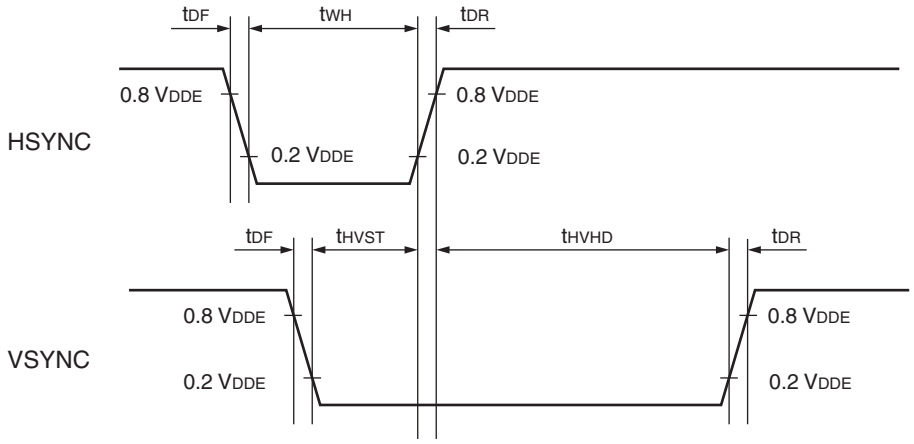


• Vertical sync signal input timing

• Leading edge of HSYNC



•Trailing edge of HSYNC



Display signal timing

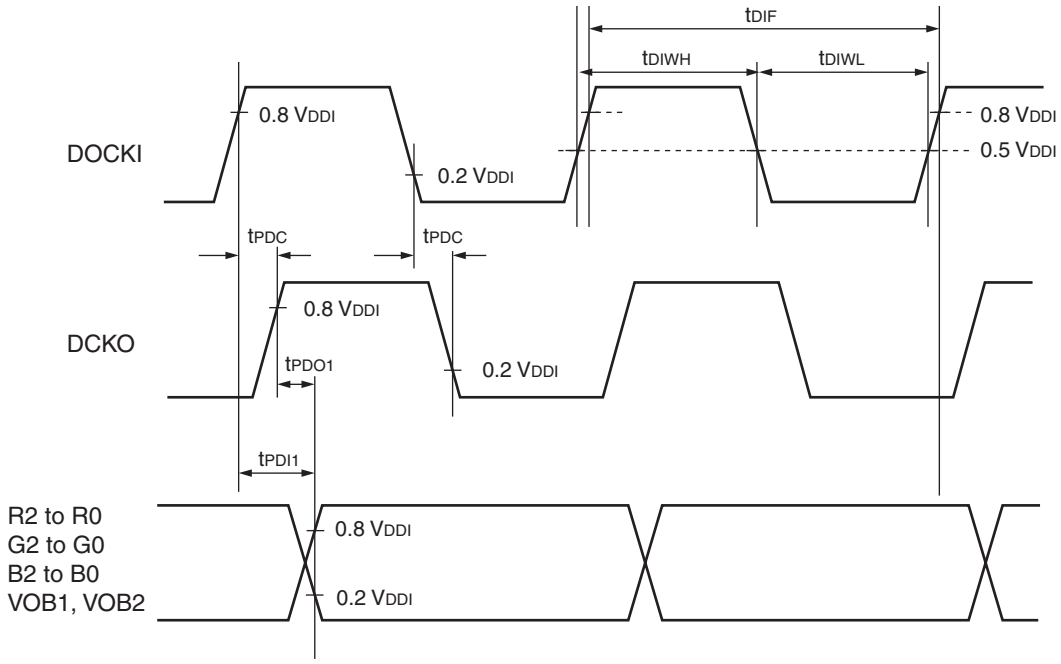
(Ta = − 10 °C to + 70 °C, V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 2.5 V ± 0.2 V, Vss = 0 V)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Dot clock input cycle time	t_{DIF}	DOCKI	11	90	MHz	*1
Dot clock input pulse width	t_{DIWH}	DOCKI	3.5	—	ns	*1
	t_{DIWL}		3.5	—	ns	
Dot clock output delay time 1	t_{PDC}	DCKO	3	8	ns	*2
Display signal output delay time I1	t_{PDI1}	R2 to R0, B2 to B0, G2 to G0, VOB1, VOB2	2	8	ns	*2
Display signal output delay time O1	t_{PDO1}	R2 to R0, B2 to B0, G2 to G0, VOB1, VOB2	− 4	+ 5	ns	*2

*1 : Input a continuous dot clock signal without a break.

*2 : Output load of 16 pF

• Display signal output timing



6. 0.25 µm Technology About the Power-on Sequence for Dual-power-supply Models

- The power supplies must be turned on in the VDDI→VDDE→AVCC, AVRH order and off in the AVCC, AVRH→VDDE→VDDI order.
  When VDDI is turned on earlier, the potential difference between VDDI and VDDE must be within 3.6 V.

- Turn on VDDE before turning on analog power supply AVCC and applying the analog signal.

7. Electrical Characteristics for the A/D Converter

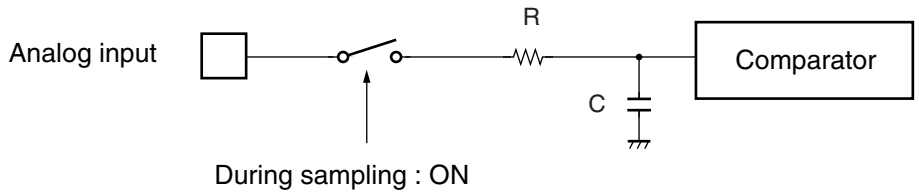
(Ta = − 10 °C to + 70 °C, V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 2.5 V ± 0.2 V, Vss = AV_{SS} = 0 V, AV_{RH} = 3.0 V to 3.6 V)

Parameter	value			Unit	Remarks
	Min	Typ	Max		
Resolution	—	—	10	bit	
Total error*1	− 5.5	—	+ 5.5	LSB	AVcc = 3.3 V, AV_{RH} = 3.3 V (CPU in sleep mode)
Nonlinear error*1	− 3.5	—	+ 3.5	LSB	
Differential linear error*1	− 2.0	—	+ 2.0	LSB	
Zero transition voltage*1	− 4.0	—	+ 6.0	LSB	
Full transition voltage*1	AV_{RH} − 5.5	—	AV_{RH} + 3.0	LSB	
Conversion time	10 *2	—	—	µs	
Power supply current (analog + digital)	—	3.6	—	mA	
	—	—	5	µA	Stop converting
Reference power supply current (between AVRH and AVRL)	—	470	—	µA	AV_{RH} = 3.0 V, AV_{RL} = 0.0 V
	—	—	10	µA	Stop converting
Analog input capacitance	—	40	—	pF	
Interchannel disparity	—	—	4	LSB	

*1 : Measured in the CPU sleep state

*2 : Depends on the clock cycle of the clock signal supplied to peripheral resources.

• Analog input circuit model



	R	C
MB91F312A/MB91FV310A	5 kΩ (Max)	45 pF (Max)

Note : The values are reference values.

■ THE FONT DATA OF STANDARD FONT PRODUCT

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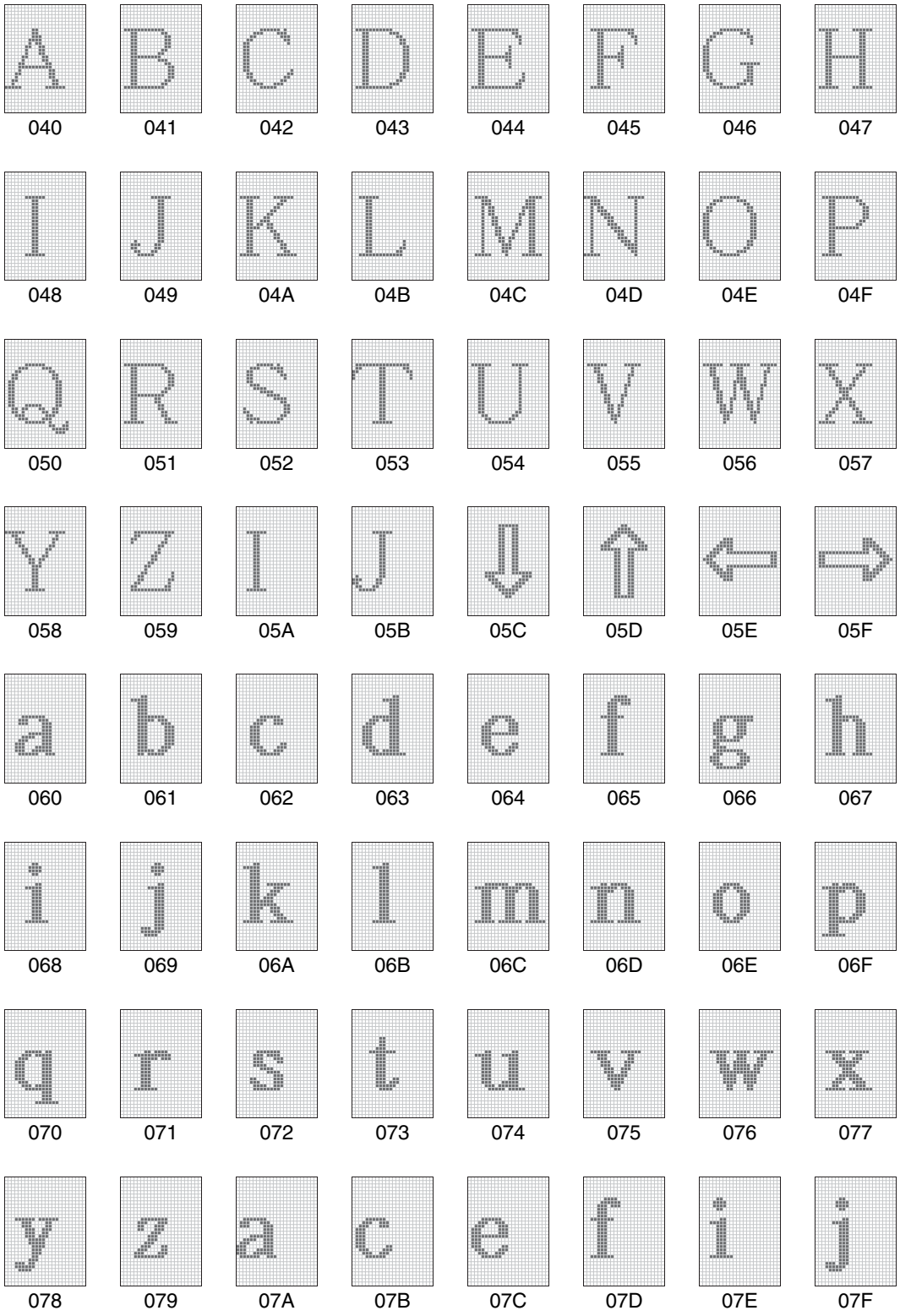
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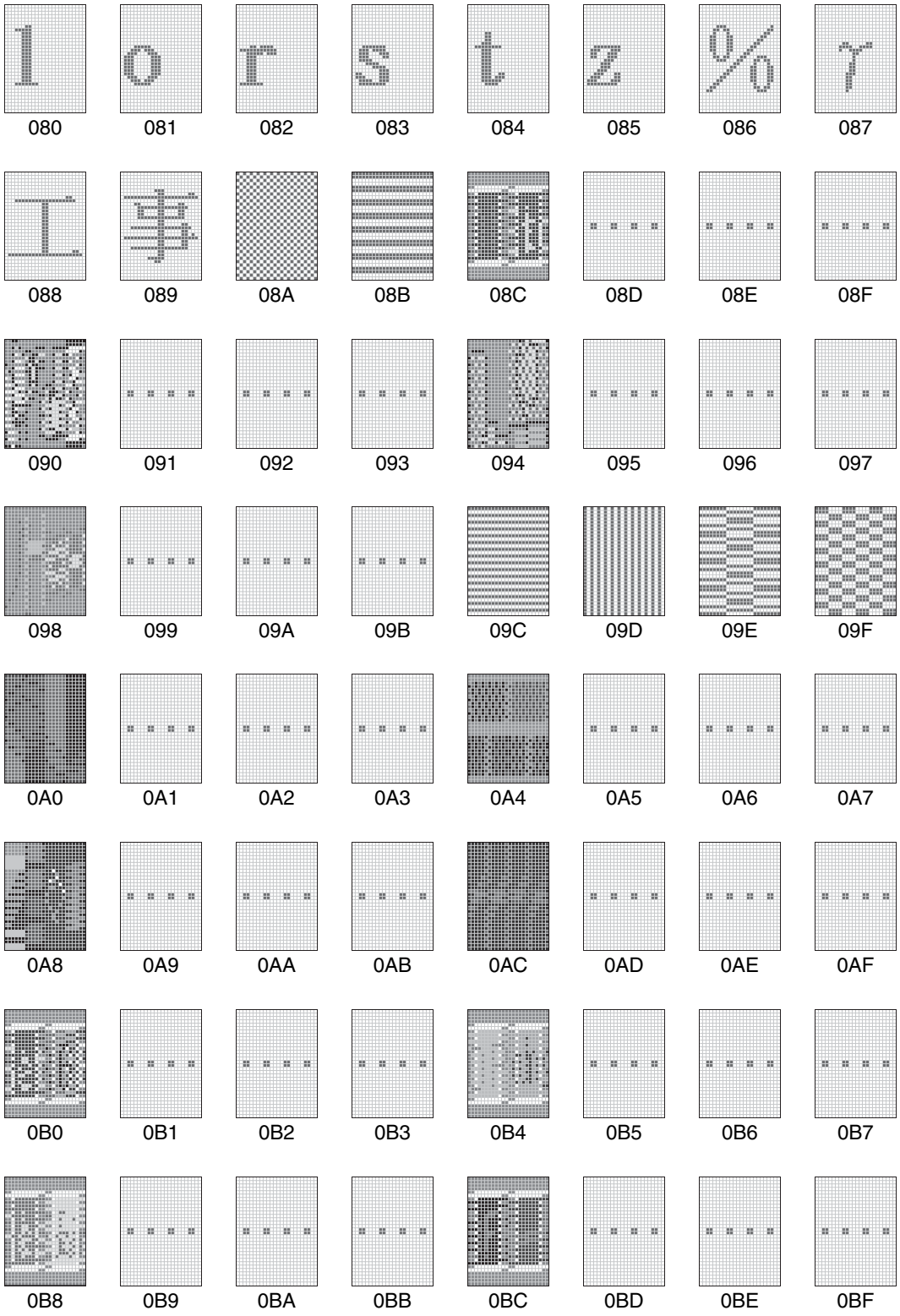
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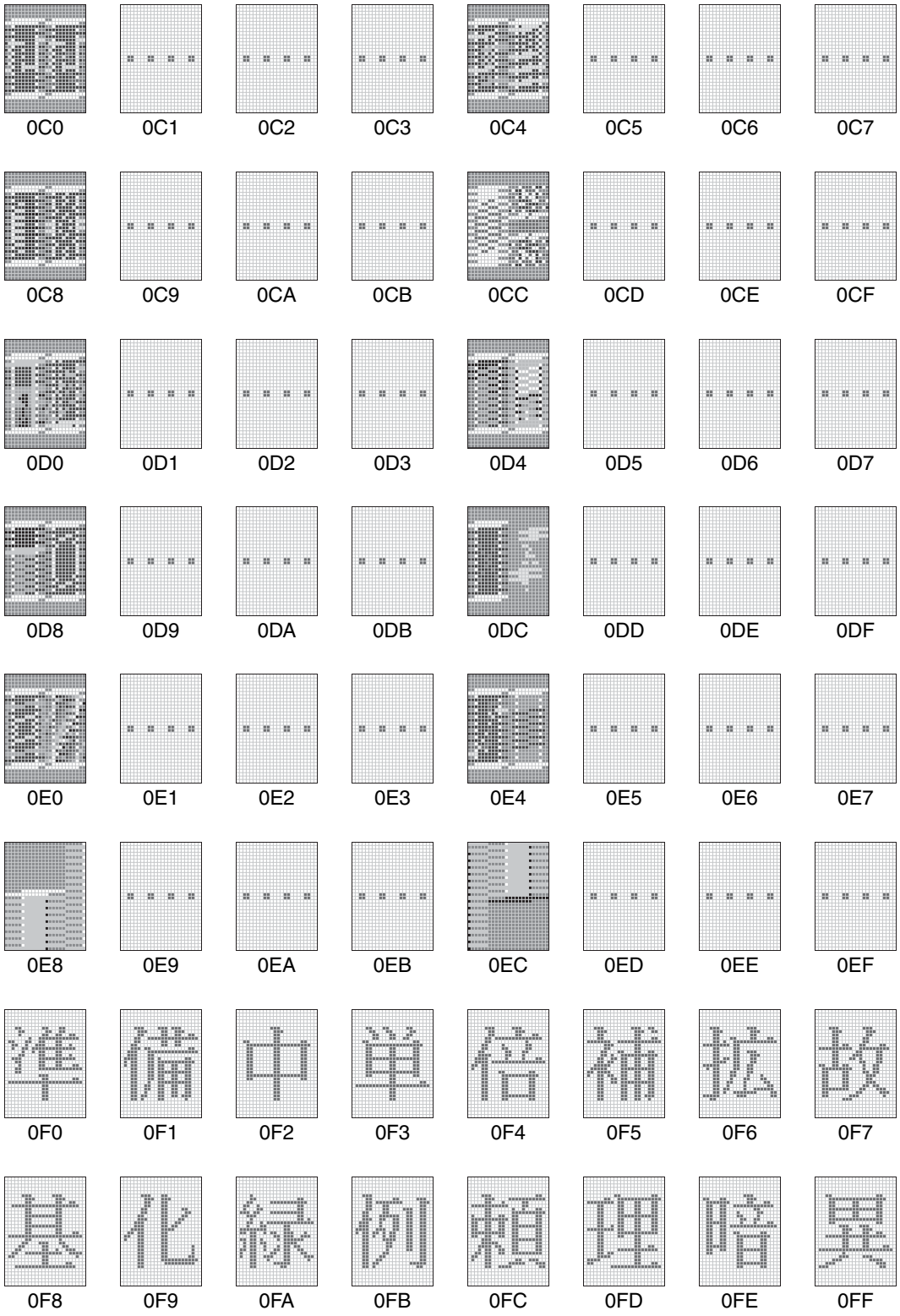
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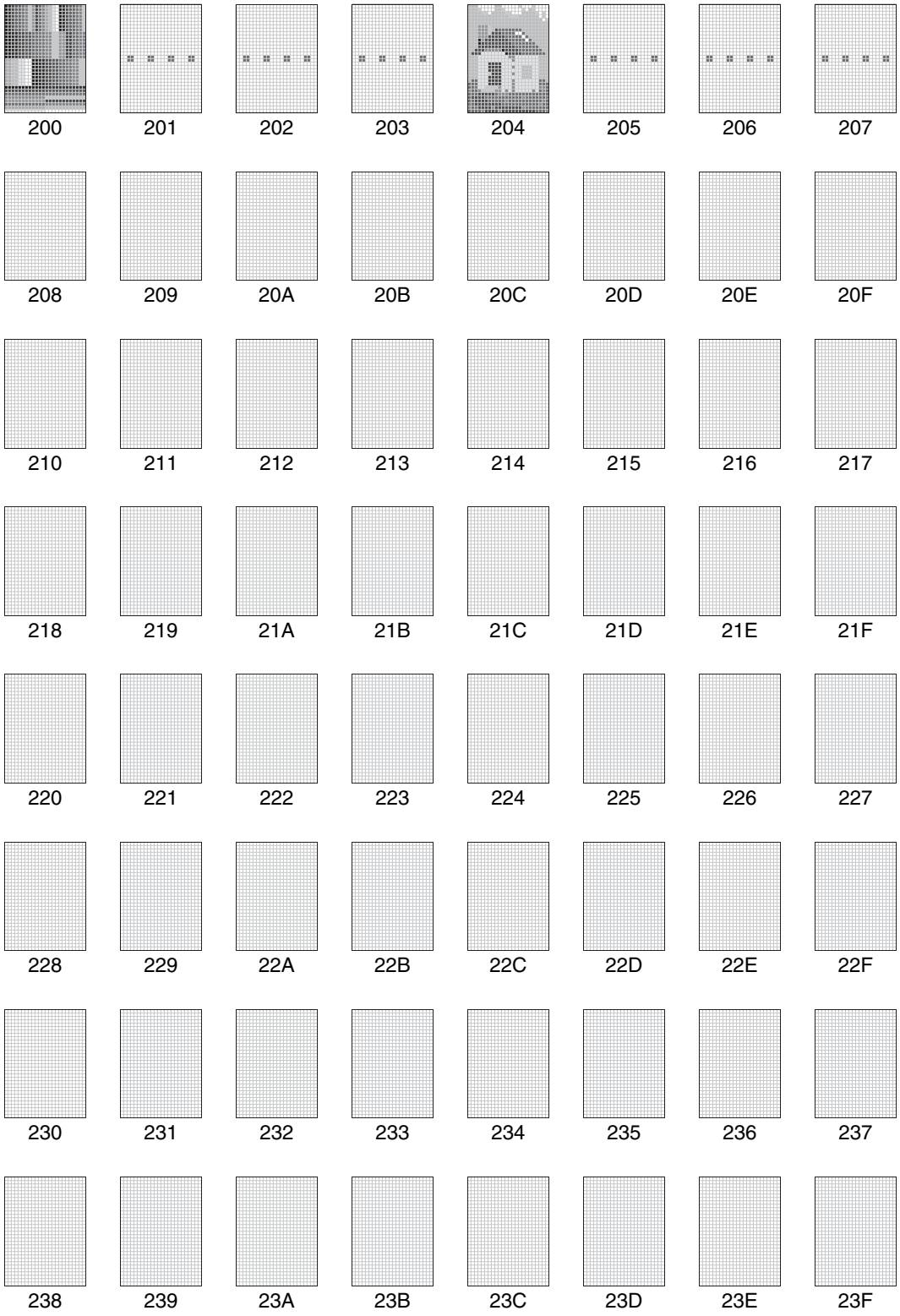
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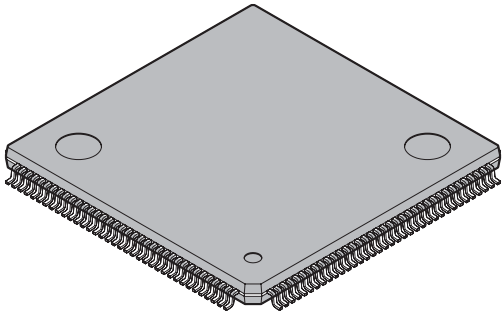
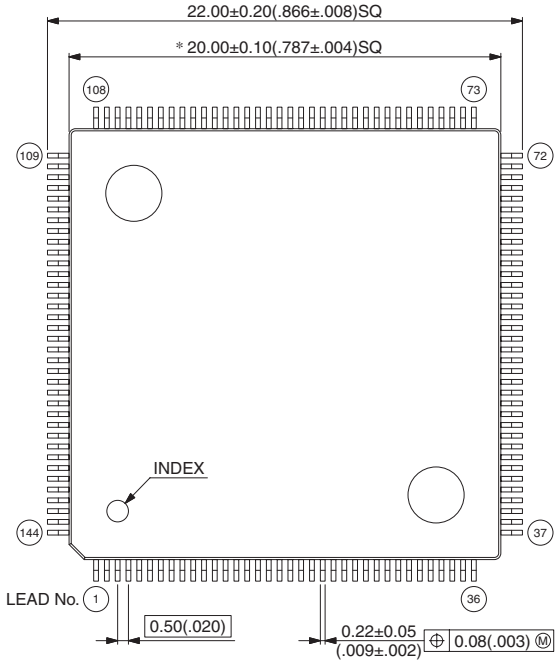
■ ORDERING INFORMATION

Part number	Package	Remarks
MB91F312APFV-1xx-BND-E1	144-pin plastic LQFP (FPT-144P-M08)	Lead Free Package
MB91F312APFV-G-010E1		Standard font product
MB91FV310APFV-ES	144-pin plastic LQFP (FPT-144P-M08)	For development tools

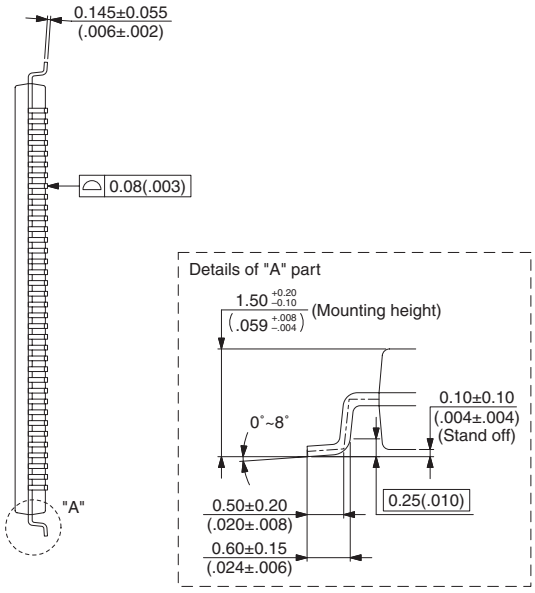
■ PACKAGE DIMENSION

144-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	20.0 × 20.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	1.20g
(FPT-144P-M08)	Code (Reference)	P-LFQFP144-20×20-0.50

144-pin plastic LQFP
(FPT-144P-M08)



Note 1) *:Values do not include resin protrusion.
Resin protrusion is +0.25(.010)Max(each side).
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

■ MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
17	■ HANDLING DEVICES	Changed the " • Notes on Power-ON/shut-down".
20	■ BLOCK DIAGRAM	Added the DSU.
21	■ MEMORY SPACE	Changed the MS to Access disallowed.
27	■ I/O MAP	PFR4 of 000414_H is changed to " – ".
35	■ I/O MAP	Changed the "00060070_H to $0006007D_H$" to "060070_H to $06FFFB_H$".
35	■ I/O MAP	Changed the $0006007E_H$ to $06FFFC_H$. Changed the register
35	■ I/O MAP	Changed the "00060080_H to $00077FFF_H$" to "070000_H to $077FFF_H$".
41	■ I/O MAP	Changed as follows; * 1:P0 to P7, DOCKI, HSYNC, YSYNC →* 1:P00 to P07, P10 to P17, P20 to P25, P30 to P36, P40 to P47, P50 to P57, P60 to P65, P70 to P74, DOCKI, HSYNC, VSYNC * 2:P0 to P7 →* 2:P00 to P07, P10 to P17, P20 to P25, P30 to P36, P40 to P47, P50 to P57, P60 to P65, P70 to P74
48	■ ELECTRICAL CHARACTERISTICS 5. AC Characteristics (4) Reload timer clock, PPG timer input, and multi-function timer input timings	Added the items.
51	(7) Analog RGB	Added the pin name DOCKI.
52, 53	(8) Digital RGB	Changed as follows; VDD → V_{DDE}
54	(8) Digital RGB	Changed as follows; VDD → V_{DDI}
55	6. 0.25 µm Technology About the Power-on Sequence for Dual-power-supply Models	Changed the "6.0.25 µm Technology About the Power-on Sequence for Dual-power-supply Models". Changed the "• Analog input circuit model".
56 to 64	■ THE FONT DATA OF STANDARD FONT PRODUCT	Added the font data.
65	■ ORDERING INFORMATION	Added the part number; MB91F312APFV-G-010E1

The vertical lines marked in the left side of the page show the changes.

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