FUJITSU MICROELECTRONICS
DATA SHEET

DS07-13752-4E

16-bit Microcontrollers

CMOS

F²MC-16LX MB90950 Series

MB90F952JDS/F952MDS/ MB90V950AJAS/V950AMAS

■ DESCRIPTION

The MB90950-series with 2 FULL-CAN interfaces and Flash ROM is especially designed for automotive and other industrial applications. Its main feature are the on-board CAN Interfaces, which conform to V2.0 Part A and Part B, while supporting a very flexible message buffer scheme and so offering more functions than a normal FULL-CAN approach. With the new 0.18 µm CMOS technology, Fujitsu now offers on-chip Flash ROM program memory 256 Kbytes.

The power to the MCU core (1.8 V) is supplied by a built-in regulator circuit, giving these microcontrollers superior performance in terms of power consumption and tolerance to EMI.

Note : F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

For the information for microcontroller supports, see the following web site.

http://edevice.fujitsu.com/micom/en-support/

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■ FEATURES

- **CPU**
  - Instruction system best suited to controller
    - Wide choice of data types (bit, byte, word, and long word)
    - Wide choice of addressing modes (23 types)
    - Enhanced functionality with signed multiply and divide instructions and the RETI instruction
    - Enhanced high-precision computing with 32-bit accumulator
  - Instruction system compatible with high-level language (C language) and multitask
    - Employing system stack pointer
    - Various enhanced pointer indirect instructions
    - Barrel shift instructions
  - Increased processing speed
    4-byte instruction queue
- **Serial interface**
  - UART (LIN/SCI): 7 channels
    - Equipped with full-duplex double buffer
    - Clock-asynchronous or clock-synchronous serial transmission is available
  - I^2C interface: 2 channels
    Up to 400 kbps transfer rate
- **Interrupt controller**
  - Powerful 8-level, 34-condition interrupt feature
  - Up to 16 external interrupts are supported
  - Automatic data transfer function independent of CPU
    Expanded intelligent I/O service function (EI^2OS): up to 16 channels
    DMA function: up to 16 channels
- **I/O ports**
  - General-purpose input/output port (CMOS output) : 82 ports
- **8/10-bit A/D converter: 24 channels**
  - Resolution is selectable between 8-bit and 10-bit.
  - Activation by external trigger input is allowed.
  - Conversion time: 3 μs (at 32-MHz machine clock, including sampling time)
- **8-bit D/A converter: 2 channels**
- **Program patch function**
  Detects address matches against 6 address pointers
- **Timer**
  - Time-base timer, watch timer, watchdog timer: 1 channel
  - 8/16-bit PPG timer: 8-bit × 16 channels, or 16-bit × 8 channels
  - 16-bit reload timer: 4 channels
  - 16-bit input/output timer
    - 16-bit free-run timer: 2 channels
    (FRT0: ICU 0/1/2/3, OCU 0/1/2/3, FRT1: ICU 4/5/6/7, OCU 4/5/6/7)
    - 16-bit input capture: (ICU): 8 channels
    - 16-bit output compare: (OCU): 8 channels

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- **FULL-CAN controller**
  - 2 channels
  - Compliant with Ver2.0A and Ver2.0B CAN specifications
  - 16 built-in message buffers
  - CAN wake-up function
- **Low power consumption (standby) mode**
  - Sleep mode (a mode that halts CPU operating clock)
  - Timebase timer mode (a mode where only the oscillation clock, sub clock, timebase timer and watch timer operate)
  - Watch mode (a mode that operates sub clock and clock timer only)
  - Stop mode (a mode that stops oscillation clock and sub clock)
  - CPU intermittent operation mode
- **Technology**
  0.18 µm CMOS technology

■ PRODUCT LINEUP

Part Number / Parameter	MB90V950AJAS	MB90V950AMAS	MB90F952JDS	MB90F952MDS
Type	Evaluation products		Flash memory products	
CPU	F^2MC-16LX CPU			
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, ×6, ×8, 1/2 when PLL stops) Minimum instruction execution time : 31.25 ns (4 MHz osc. PLL × 8)			
ROM	External		Main 256 Kbytes Satellite 32 Kbytes	
RAM	30 Kbytes		16 Kbytes	
Emulator-specific power supply*1	Yes		—	
FPGA data*2	Rev 050617		—	
Adaptor board*2	MB2147-20 Rev.04C or later		—	
Clock supervisor	Yes	No	Yes	No
Clock calibration unit	Yes	No	Yes	No
Low-voltage/CPU operation detection reset	No (CPU operation detection reset only)	No	Yes	No
Technology	0.35 µm CMOS with built-in power supply regulator		0.18 µm CMOS with built-in power supply regulator + Flash memory with Charge pump for programming voltage	
Operating voltage range	5 V ± 10%		3.0 V to 5.5 V : When normal operating 4.0 V to 5.5 V : When Flash programming 4.5 V to 5.5 V : When using the external bus	
Operating ambient temperature	—		−40 °C to +105 °C	
Package	PGA-299		QFP-100, LQFP-100	
UART	7 channels			
	Wide range of baud rate settings using a dedicated reload timer Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device			
I^2C (400 kbps)	2 channels			
A/D Converter	24 input channels			
	10-bit or 8-bit resolution Conversion time : Min 3 µs include sample time (per one channel)			
16-bit Reload Timer (4 channels)	Operation clock frequency : fsys/2^1, fsys/2^3, fsys/2^5 (fsys = Machine clock frequency) Supports External Event Count function			

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Parameter \ Part Number	MB90V950AJAS	MB90V950AMAS	MB90F952JDS	MB90F952MDS
16-bit I/O Timer (2 channels)	Generates an interrupt signal on overflow Supports Timer Clear when the output compare finds a match Operation clock freq. : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4, fsys/2^5, fsys/2^6, fsys/2^7 (fsys = Machine clock freq.) I/O Timer 0 (clock input FRCK0) corresponds to ICU0/1/2/3, OCU 0/1/2/3 I/O Timer 1 (clock input FRCK1) corresponds to ICU4/5/6/7, OCU 4/5/6/7			
16-bit Output Compare (8 channels)	Generates an interrupt signal when one of the 16-bit I/O timer matches the output compare register A pair of compare registers can be used to generate an output signal.			
16-bit Input Capture (8 channels)	Holds free-run timer on rising edge, falling edge or rising & falling edge Signals an interrupt upon external event			
8/16-bit Programmable Pulse Generator	8 channels (16-bit) /16 channels (8-bit) Sixteen 8-bit reload counters Sixteen 8-bit reload registers for L pulse width Sixteen 8-bit reload registers for H pulse width Supports 8-bit and 16-bit operation modes A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler plus 8-bit reload counter Operating clock freq. : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4 or 128 µs@fosc = 4 MHz (fsys = Machine clock frequency, fosc = Oscillation clock frequency)			
CAN Interface	3 channels		2 channels	
	Conforms to CAN Specification Version 2.0 Part A and B Automatic re-transmission in case of error Automatic transmission in response to Remote Frames Prioritized 16 message buffers for data and ID's Supports multiple messages Flexible configuration of acceptance filtering : Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps			
External Interrupt (16 channels)	Can be used rising edge, falling edge, starting up by H/L level input, external interrupt, expanded intelligent I/O services (EI^{2}OS) and DMA			
D/A converter	2 channels			
Sub clock	Yes	No	Yes	No
I/O Ports	Virtually all external pins can be used as general purpose I/O port All ports are push-pull outputs Bit-wise settable as input/output or peripheral signal Can be configured 8 as CMOS schmitt trigger/ automotive inputs (in blocks of 8 pins) TTL input level settable for external bus (32-pin only for external bus)			

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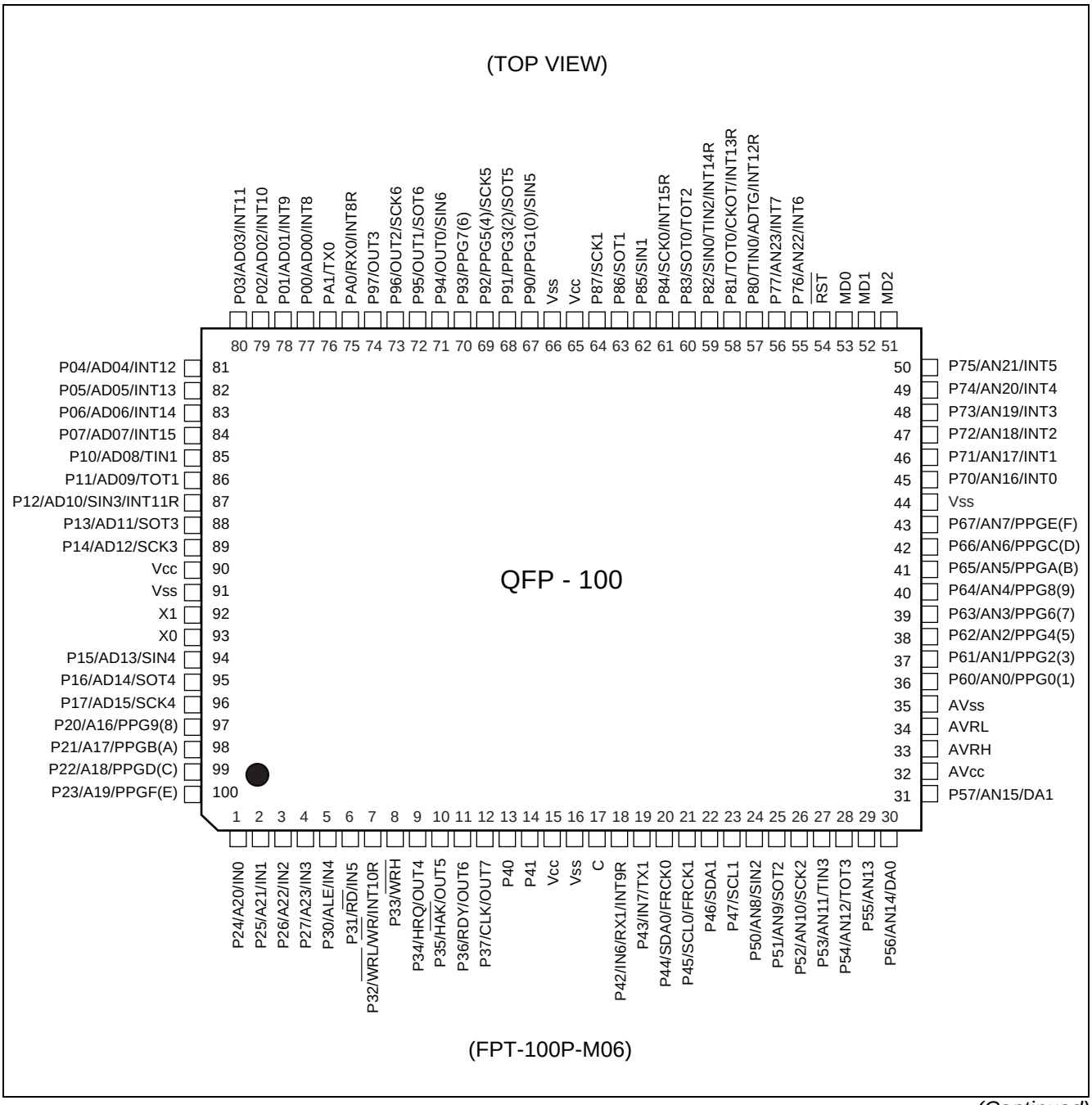
Part Number / Parameter	MB90V950AJAS	MB90V950AMAS	MB90F952JDS	MB90F952MDS
Flash Memory	—		Supports automatic programming, Embedded Algorithm Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Boot block configuration Erase can be performed on each block Block protection with external programming voltage Flash Security Feature for protecting the content of the Flash	

*1 : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01) is used.
Please refer to the Emulator hardware manual for details.

*2 : Customers considering the use of other FPGA data and the adaptor boards should consult with sales representatives.

■ PIN ASSIGNMENTS

- MB90F952JDS, MB90F952MDS



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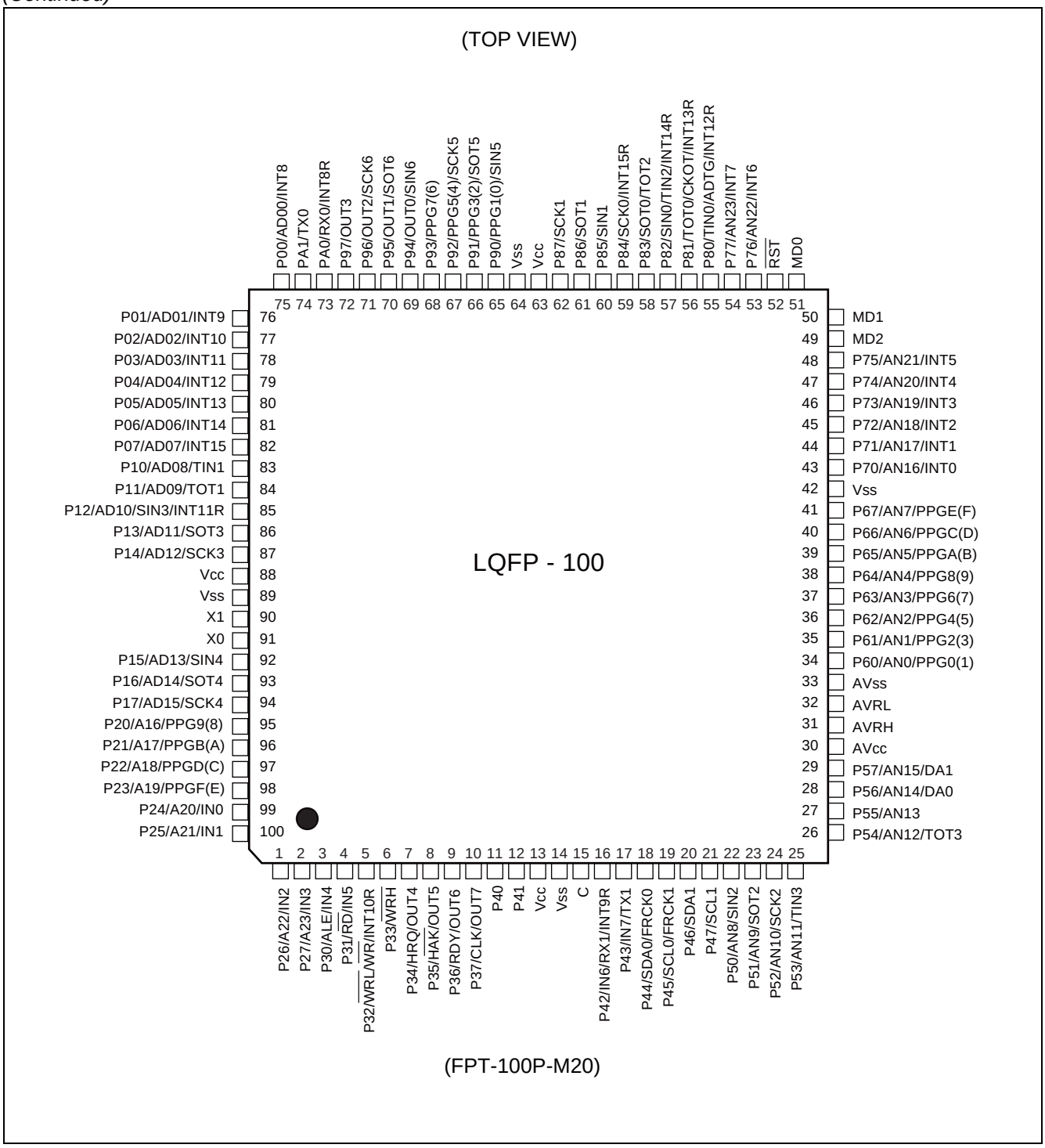

(FPT-100P-M20)

■ PIN DESCRIPTION

Pin No.		Pin name	I/O Circuit type*3	Function
LQFP100*1	QFP100*2			
90	92	X1	A	Oscillation output pin
91	93	X0		Oscillation input pin
52	54	$\overline{RST}$	E	Reset input pin
75 to 82	77 to 84	P00 to P07	G	General purpose I/O ports The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD00 to AD07		I/O pins for 8 lower bits of the external address/data bus. This function is enabled when the external bus is enabled.
		INT8 to INT15		External interrupt request input pins for INT8 to INT15.
83	85	P10	G	General purpose I/O port The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD08		I/O pin of the external address/data bus (AD08). This function is enabled when the external bus is enabled.
		TIN1		Event input pin for the reload timer 1
84	86	P11	G	General purpose I/O port The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD09		I/O pin of the external address/data bus (AD09). This function is enabled when the external bus is enabled.
		TOT1		Output pin for the reload timer 1
85	87	P12	N	General purpose I/O port The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD10		I/O pin of the external address/data bus (AD10). This function is enabled when the external bus is enabled.
		SIN3		Serial data input pin for UART3
		INT11R		External interrupt request input pin for INT11R
86	88	P13	G	General purpose I/O port The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD11		I/O pin of the external address/data bus (AD11). This function is enabled when the external bus is enabled.
		SOT3		Serial data output pin for UART3

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Pin No.		Pin name	I/O Circuit type*3	Function
LQFP100*1	QFP100*2			
87	89	P14	G	General purpose I/O port The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD12		I/O pin of the external address/data bus (AD12). This function is enabled when the external bus is enabled.
		SCK3		Clock I/O pin for UART3
92	94	P15	N	General purpose I/O port The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD13		I/O pin of the external address/data bus (AD13). This function is enabled when the external bus is enabled.
		SIN4		Serial data input pin for UART4
93	95	P16	G	General purpose I/O port The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD14		I/O pin of the external address/data bus (AD14). This function is enabled when the external bus is enabled.
		SOT4		Serial data output pin for UART4
94	96	P17	G	General purpose I/O port The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD15		I/O pin of the external address/data bus (AD15). This function is enabled when the external bus is enabled.
		SCK4		Clock I/O pin for UART4
95 to 98	97 to 100	P20 to P23	G	General purpose I/O ports The register can be set to select whether to use a pull-up resistor.In external bus mode, the pin is enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1.
		A16 to A19		A16 to A19 for output pins of the external address/data bus. When the corresponding bit in the external address output control register (HACR) is 0, the pins are enabled as high address output pins (A16 to A19).
		PPG9, PPGB, PPGD, PPGF		Output pins for PPGs

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Pin No.		Pin name	I/O Circuit type*3	Function
LQFP100*1	QFP100*2			
99, 100, 1, 2	1 to 4	P24 to P27	G	General purpose I/O ports The register can be set to select whether to use a pull-up resistor. In external bus mode, the pin is enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1.
		A20 to A23		A20 to A23 for output pins of the external address/data bus. When the corresponding bit in the external address output control register (HACR) is 0, the pins are enabled as high address output pins (A20 to A23).
		IN0 to IN3		Data sample input pins for input capture ICU0 to ICU3.
3	5	P30	G	General purpose I/O port The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		ALE		Address latch enable output pin. This function is enabled when the external bus is enabled.
		IN4		Data sample input pin for input capture ICU4.
4	6	P31	G	General purpose I/O port The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		$\overline{RD}$		External read strobe output pin for data bus. This function is enabled when the external bus is enabled.
		IN5		Data sample input pin for input capture ICU5.
5	7	P32	G	General purpose I/O port The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the $\overline{WR}$/$\overline{WRL}$ pin output is disabled.
		$\overline{WRL}$/ $\overline{WR}$		Write strobe output pin for the external data bus. This function is enabled when both the external bus and the $\overline{WR}$/$\overline{WRL}$ pin output are enabled. $\overline{WRL}$ is used to write-strobe 8 lower bits of the data bus in 16-bit access while $\overline{WR}$ is used to write-strobe 8 bits of the data bus in 8-bit access.
		INT10R		External interrupt request input pin for INT10R.
6	8	P33	G	General purpose I/O port The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the $\overline{WRH}$ pin output is disabled.
		$\overline{WRH}$		Write strobe output pin for the upper 8 bits of the external data bus. This function is enabled when the external bus is enabled, when the external bus 16-bit mode is selected, and when the $\overline{WRH}$ output pin is enabled.

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Pin No.		Pin name	I/O Circuit type*3	Function
LQFP100*1	QFP100*2			
7	9	P34	G	General purpose I/O port The register can be set to select whether to use a pull-up resistor.This function is enabled either in single-chip mode or when the hold function is disabled.
		HRQ		Hold request input pin. This function is enabled when both the external bus and the hold function are enabled.
		OUT4		Waveform output pin for output compare OCU4.
8	10	P35	G	General purpose I/O port The register can be set to select whether to use a pull-up resistor.This function is enabled either in single-chip mode or when the hold function is disabled.
		$\overline{\text{HAK}}$		Hold acknowledge output pin. This function is enabled when both the external bus and the hold function are enabled.
		OUT5		Waveform output pin for output compare OCU5.
9	11	P36	G	General purpose I/O port The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the external ready function is disabled.
		RDY		Ready input pin. This function is enabled when both the external bus and the external ready function are enabled.
		OUT6		Waveform output pin for output compare OCU6.
10	12	P37	G	General purpose I/O port The register can be set to select whether to use a pull-up resistor.This function is enabled either in single-chip mode or when the clock output is disabled.
		CLK		Clock output pin. This function is enabled when both the external bus and clock output are enabled.
		OUT7		Waveform output pin for output compare OCU7.
11, 12	13, 14	P40, P41	F	General purpose I/O ports
16	18	P42	F	General purpose I/O port
		IN6		Data sample input pin for input capture ICU6.
		RX1		RX input pin for CAN1 Interface
		INT9R		External interrupt request input pin for INT9R.
17	19	P43	F	General purpose I/O port
		IN7		Data sample input pin for input capture ICU7.
		TX1		TX Output pin for CAN1

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Pin No.		Pin name	I/O Circuit type*3	Function
LQFP100*1	QFP100*2			
18	20	P44	H	General purpose I/O port
		SDA0		Serial data I/O pin for I²C 0
		FRCK0		Input pin for the 16-bit I/O Timer 0
19	21	P45	H	General purpose I/O port
		SCL0		Serial clock I/O pin for I²C 0
		FRCK1		Input pin for the 16-bit I/O Timer1
20	22	P46	H	General purpose I/O port
		SDA1		Serial data I/O pin for I²C 1
21	23	P47	H	General purpose I/O port
		SCL1		Serial clock I/O pin for I²C 1
22	24	P50	O	General purpose I/O port
		AN8		Analog input pin for the A/D converter
		SIN2		Serial data input pin for UART2
23	25	P51	I	General purpose I/O port
		AN9		Analog input pin for the A/D converter
		SOT2		Serial data output pin for UART2
24	26	P52	I	General purpose I/O port
		AN10		Analog input pin for the A/D converter
		SCK2		Clock I/O pin for UART2
25	27	P53	I	General purpose I/O port
		AN11		Analog input pin for the A/D converter
		TIN3		Event input pin for the reload timer 3
26	28	P54	I	General purpose I/O port
		AN12		Analog input pin for the A/D converter
		TOT3		Output pin for the reload timer 3
27	29	P55	I	General purpose I/O port
		AN13		Analog input pin for the A/D converter
28, 29	30, 31	P56, P57	J	General purpose I/O ports
		AN14, AN15		Analog input pins for the A/D converter
		DA0,DA1		Analog output pins for the D/A converter

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Pin No.		Pin name	I/O Circuit type*3	Function
LQFP100*1	QFP100*2			
34 to 41	36 to 43	P60 to P67	I	General purpose I/O ports
		AN0 to AN7		Analog input pins for the A/D converter
		PPG0, PPG2, PPG4, PPG6, PPG8, PPGA, PPGC, PPGE		Output pins for PPGs
43 to 48, 53, 54	45 to 50, 55, 56	P70 to P77	I	General purpose I/O ports
		AN16 to AN23		Analog input pins for the A/D converter
		INT0 to INT7		External interrupt request input pins for INT0 to INT7
55	57	P80	F	General purpose I/O port
		TIN0		Event input pin for the reload timer 0
		ADTG		Trigger input pin for the A/D converter
		INT12R		External interrupt request input pin for INT12R
56	58	P81	F	General purpose I/O port
		TOT0		Output pin for the reload timer 0
		CKOT		Output pin for the clock monitor
		INT13R		External interrupt request input pin for INT13R
57	59	P82	M	General purpose I/O port
		SIN0		Serial data input pin for UART0
		TIN2		Event input pin for the reload timer 2
		INT14R		External interrupt request input pin for INT14R
58	60	P83	F	General purpose I/O port
		SOT0		Serial data output pin for UART 0
		TOT2		Output pin for the reload timer 2
59	61	P84	F	General purpose I/O port
		SCK0		Clock I/O pin for UART0
		INT15R		External interrupt request input pin for INT15R
60	62	P85	M	General purpose I/O port
		SIN1		Serial data input pin for UART1
61	63	P86	F	General purpose I/O port
		SOT1		Serial data output pin for UART1

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Pin No.		Pin name	I/O Circuit type*3	Function
LQFP100*1	QFP100*2			
62	64	P87	F	General purpose I/O port
		SCK1		Clock I/O pin for UART1
65	67	P90	M	General purpose I/O port
		PPG1		Output pin for PPGs
		SIN5		Serial data input pin for UART5
66	68	P91	F	General purpose I/O port
		PPG3		Output pin for PPGs
		SOT5		Serial data output pin for UART5
67	69	P92	F	General purpose I/O port
		PPG5		Output pin for PPGs
		SCK5		Clock I/O pin for UART5
68	70	P93	F	General purpose I/O port
		PPG7		Output pin for PPGs
69	71	P94	M	General purpose I/O port
		OUT0		Waveform output pin for output compare for OCU0. This function is enabled when the waveform output is enabled.
		SIN6		Serial data input pin for UART6
70	72	P95	F	General purpose I/O port
		OUT1		Waveform output pin for output compare for OCU1.This function is enabled when the waveform output is enabled.
		SOT6		Serial data output pin for UART6
71	73	P96	F	General purpose I/O port
		OUT2		Waveform output pin for output compare for OCU2. This function is enabled when the waveform output is enabled.
		SCK6		Clock I/O pin for UART6
72	74	P97	F	General purpose I/O port
		OUT3		Waveform output pin for output compare for OCU3. This function is enabled when the waveform output is enabled.
73	75	PA0	F	General purpose I/O port
		RX0		RX input pin for CAN0 Interface. Outputs generated by other functions must be stopped when using the CAN functions.
		INT8R		External interrupt request input pin for INT8R
74	76	PA1	F	General purpose I/O port
		TX0		TX Output pin for CAN0
30	32	AV_{CC}	K	V_{CC} power input pin for the Analog circuit

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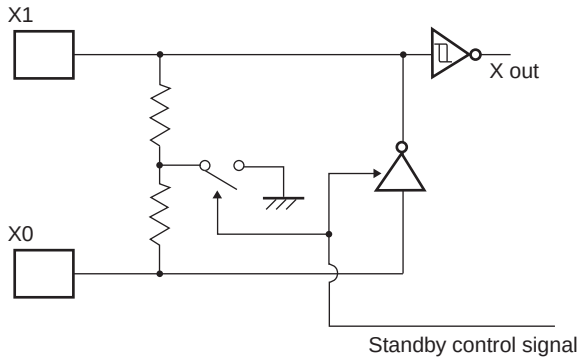
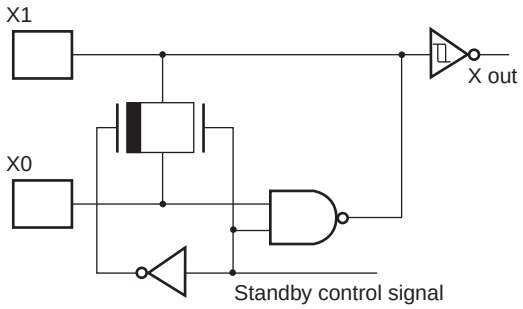
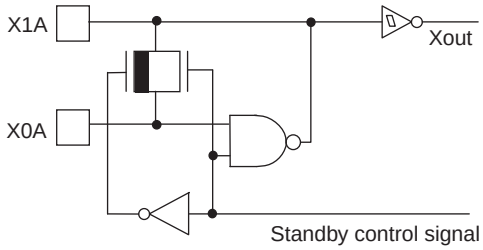
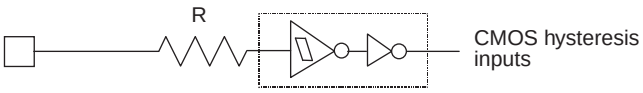
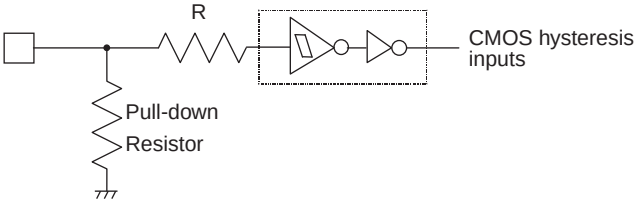
Pin No.		Pin name	I/O Circuit type*3	Function
LQFP100*1	QFP100*2			
31	33	AVRH	L	Reference voltage input pin for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AVRH is applied to AV_{CC}.
32	34	AVRL	K	Lower reference voltage input pin for the A/D Converter
33	35	AV_{SS}	K	V_{SS} power input pin for the Analog circuit
50, 51	52, 53	MD1, MD0	C	Input pins for specifying the operating mode
49	51	MD2	D	Input pin for specifying the operating mode
13, 63, 88	15, 65, 90	V_{CC}	—	Power (3.5 V to 5.5 V) input pins
14, 42, 64, 89	16, 44, 66, 91	V_{SS}	—	Power (0 V) input pins
15	17	C	K	This is the power supply stabilization capacitor. This pin should be connected to a ceramic capacitor with a capacitance greater than or equal to 0.1 μF.

*1 : FPT-100P-M20

*2 : FPT-100P-M06

*3 : For I/O circuit type, refer to “■ I/O CIRCUIT TYPES”.

■ I/O CIRCUIT TYPES

Type	Circuit	Remarks
A		Oscillation circuit High-speed oscillation feedback resistor = approx. 1 MΩ (Flash memory product)
		Oscillation circuit High-speed oscillation feedback resistor = approx. 1 MΩ (Evaluation product)
B		Oscillation circuit Low-speed oscillation feedback resistor = approx. 10 MΩ
C		Evaluation products: CMOS hysteresis input Flash memory products: CMOS input pin
D		Evaluation products: • CMOS hysteresis input • Pull-down resistor value: approx. 50 kΩ Flash memory products: • CMOS input • No pull-down

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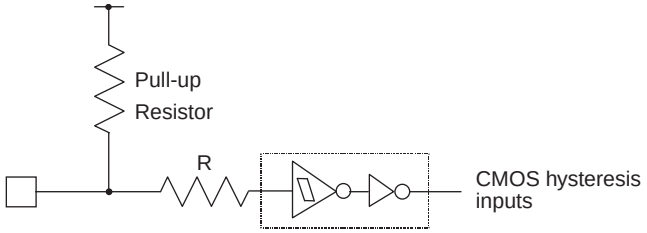
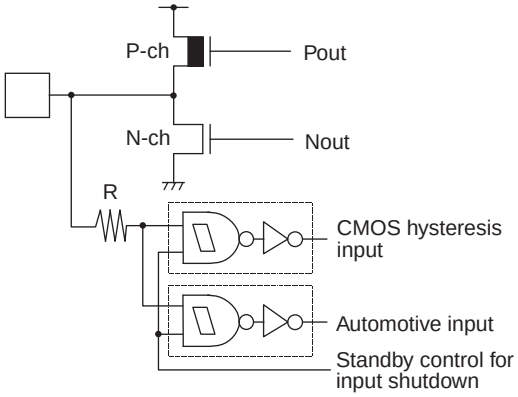
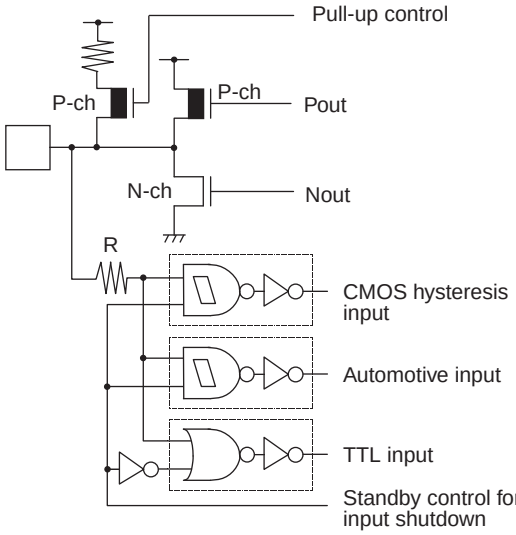
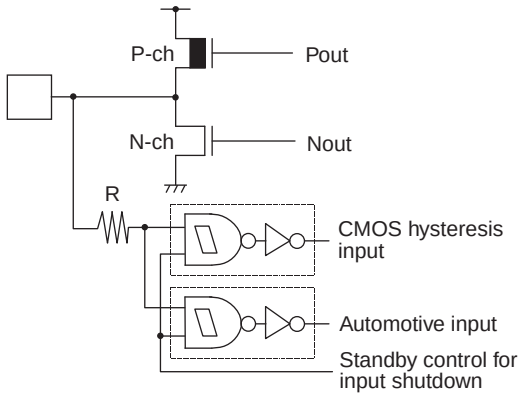
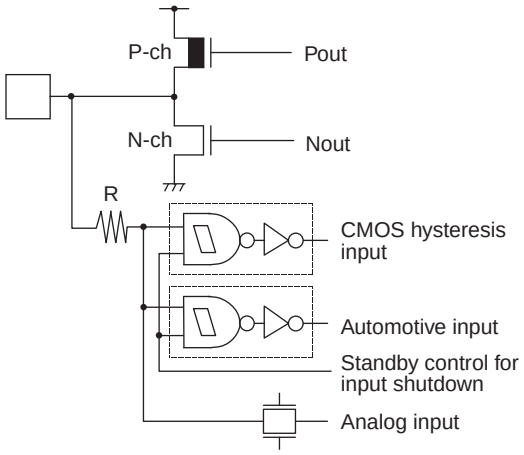
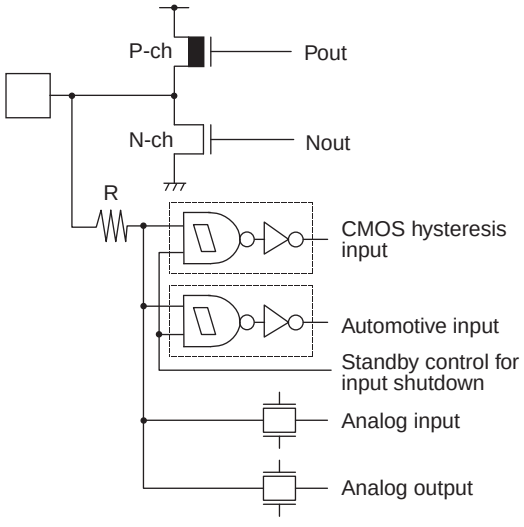
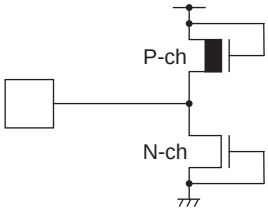
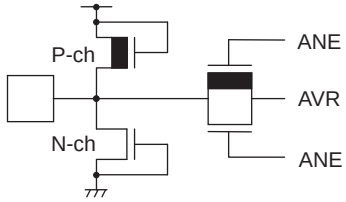
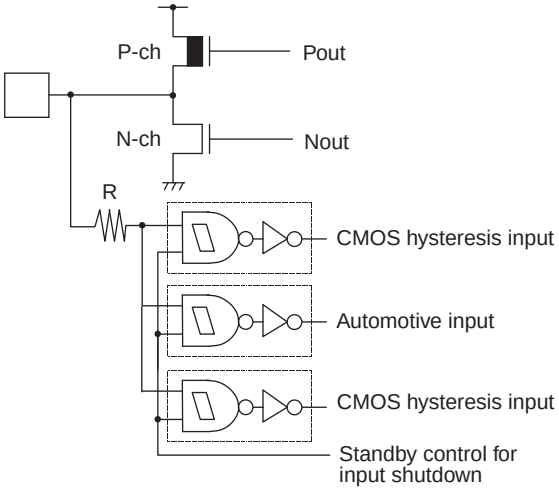
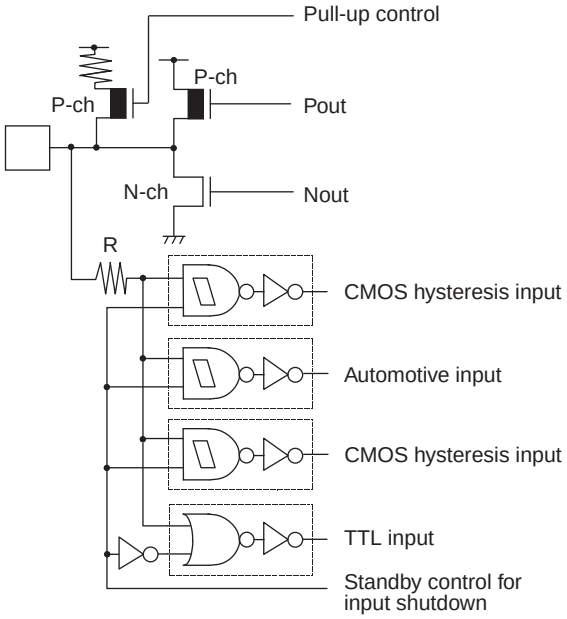
Type	Circuit	Remarks
E		• CMOS hysteresis input • Pull-up resistor value: approx. 50 kΩ
F		• CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) • CMOS hysteresis input (V_{IH} 0.8 V_{CC} V_{IL} 0.2 V_{CC}) (with function to disconnect input during standby) • Automotive input (with function to disconnect input during standby)
G		• CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) • CMOS hysteresis input (V_{IH} 0.8 V_{CC} V_{IL} 0.2 V_{CC}) (with function to disconnect input during standby) • Automotive input (with function to disconnect input during standby) • TTL input (with function to disconnect input during standby) • Programmable pull-up resistor: 50 kΩ approx.

(Continued)

Type	Circuit	Remarks
H		• CMOS level output (I_{OL} = 3 mA, I_{OH} = –3 mA) • CMOS hysteresis input (V_{IH} 0.8 V_{CC} V_{IL} 0.2 V_{CC}) (with function to disconnect input during standby) • Automotive input (with function to disconnect input during standby) • CMOS hysteresis input (V_{IH} 0.7 V_{CC} V_{IL} 0.3 V_{CC}) (with function to disconnect input during standby)
I		• CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) • CMOS hysteresis input (V_{IH} 0.8 V_{CC} V_{IL} 0.2 V_{CC}) (with function to disconnect input during standby) • Automotive input (with function to disconnect input during standby) • A/D converter analog input
J		• CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) • D/A analog output • CMOS hysteresis input (V_{IH} 0.8 V_{CC} V_{IL} 0.2 V_{CC}) (with function to disconnect input during standby) • Automotive input (with function to disconnect input during standby) • A/D converter analog input • D/A converter analog output

(Continued)

Type	Circuit	Remarks
K		Power supply input protection circuit
L		A/D converter reference voltage power supply input pin, with the protection circuit Flash memory devices do not have a protection circuit against V_{CC} for pin AVRH
M		• CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) • CMOS hysteresis input (V_{IH} 0.8 V_{CC} V_{IL} 0.2 V_{CC}) (with function to disconnect input during standby) • Automotive input (with function to disconnect input during standby) • CMOS hysteresis input (V_{IH} 0.7 V_{CC} V_{IL} 0.3 V_{CC}) (with function to disconnect input during standby)
N		• CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) • CMOS hysteresis input (V_{IH} 0.8 V_{CC} V_{IL} 0.2 V_{CC}) (with function to disconnect input during standby) • Automotive input (with function to disconnect input during standby) • TTL input (with function to disconnect input during standby) • CMOS hysteresis input (V_{IH} 0.7 V_{CC} V_{IL} 0.3 V_{CC}) (with function to disconnect input during standby) • Programmable pull-up resistor: 50 kΩ approx

(Continued)

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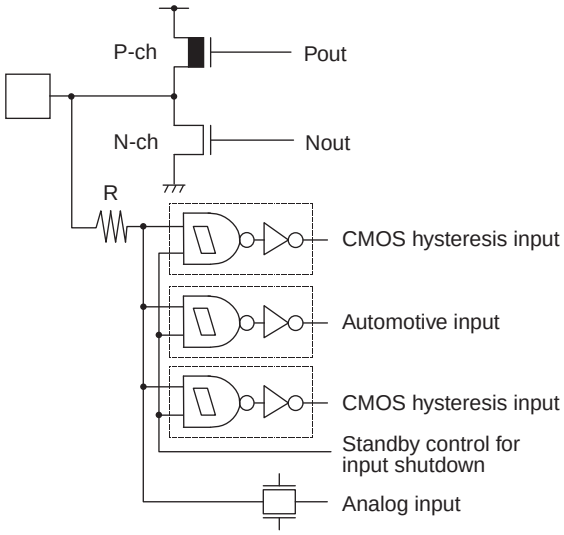
Type	Circuit	Remarks
O		• CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) • CMOS hysteresis input (V_{IH} 0.8 V_{CC} V_{IL} 0.2 V_{CC}) (with function to disconnect input during standby) • Automotive input (with function to disconnect input during standby) • CMOS hysteresis input (V_{IH} 0.7 V_{CC} V_{IL} 0.3 V_{CC}) (with function to disconnect input during standby) • A/D converter analog input

■ HANDLING DEVICES

- **Preventing latch-up**

  CMOS IC chips may suffer latch-up under the following conditions:
  - A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
  - A voltage higher than the rated voltage is applied between V_{CC} and V_{SS} pins.
  - The AV_{CC} power supply is applied before the V_{CC} voltage.

  Latch-up may increase the power supply current drastically, causing thermal damage to the device.

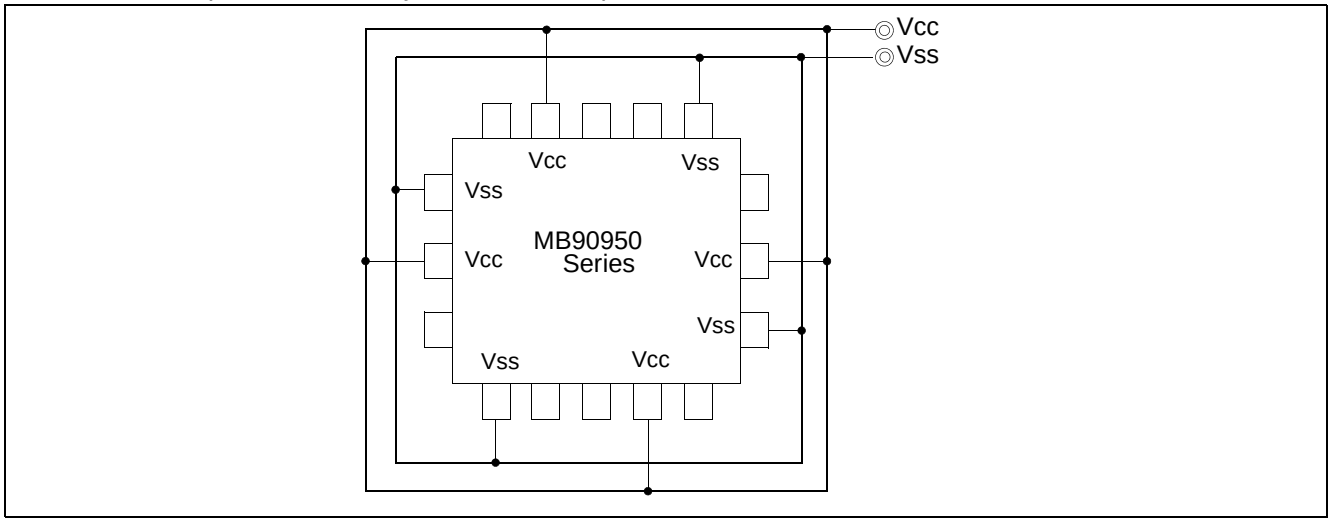
  For the same reason, also be careful not to let the analog power-supply voltage (AV_{CC}, AVRH) exceed the digital power-supply voltage.

- **Handling unused pins**

  Leaving unused input pins open may result in misbehavior or latch-up and possible permanent damage to the device. Therefore they must be pulled up or pulled down through resistors. In this case those resistors should be more than 2 kΩ.

  Unused bidirectional pins should be set to the output state and can be left open, or the input state with the above described connection.

- **Power supply pins (V_{CC}/V_{SS})**
  - If there are multiple V_{CC} and V_{SS} pins, that are designed to be set to the same potential are connected the inside of the device to prevent malfunctions such as latch-up.
    To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the V_{CC} and V_{SS} pins to the power supply and ground externally. Connect V_{CC} and V_{SS} pins to the device from the current supply source at a low impedance.
  - As a measure against power supply noise, connect a capacitor of about 0.1 μF as a bypass capacitor between V_{CC} and V_{SS} pins in the vicinity of V_{CC} and V_{SS} pins of the device



- **Mode Pins (MD0 to MD2)**

  Connect the mode pins directly to V_{CC} or V_{SS} pins. To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the mode pins to V_{CC} or V_{SS} pins and to provide a low-impedance connection.

- **Sequence for Turning On the Power Supply to the A/D Converter and Analog Inputs**

  Make sure to turn on the A/D converter power supply (AV_{CC}, AVRH, AVRL) and analog inputs (AN0 to AN23) after turning-on the digital power supply (V_{CC}).

  Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage does not exceed AVRH or AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable).

- **Pin connection when A/D converter is not used**

  Connect unused pins of A/D converter to $AV_{CC} = V_{CC}$, AV_{SS} = AVRH = AVRL = V_{SS}.

- **Crystal Oscillator Circuit**

  The X0, X1 pins may be possible causes of abnormal operation. Make sure to provide bypass capacitors via the shortest distance from X0, X1 pins and crystal oscillator (or ceramic oscillator) and ground lines, and make sure, to the utmost effort, that the oscillation circuit lines do not cross the lines of other circuits. It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins with a ground area for stabilizing the operation.

  For each of the mass-production products, request an oscillator evaluation from the manufacturer of the oscillator you are using.

- **Pull-up/down resistors**

  The MB90950 Series does not support internal pull-up/down resistors (except for the pull-up resistors built into ports 0 to 3). Use external components where needed.

- **Using external clock**

  The external clock inputs can not be used.

- **Notes on operation in PLL clock mode**

  If PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or the external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

- **Notes on Power-On**

  To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during power-on to 50 µs or more (0.2 V to 2.7 V) .

- **Stabilization of power supply voltage**

  A sudden change in the supply voltage may cause the device to malfunction even within the specified V_{CC} supply voltage operating range. Therefore, the V_{CC} supply voltage should be stabilized.

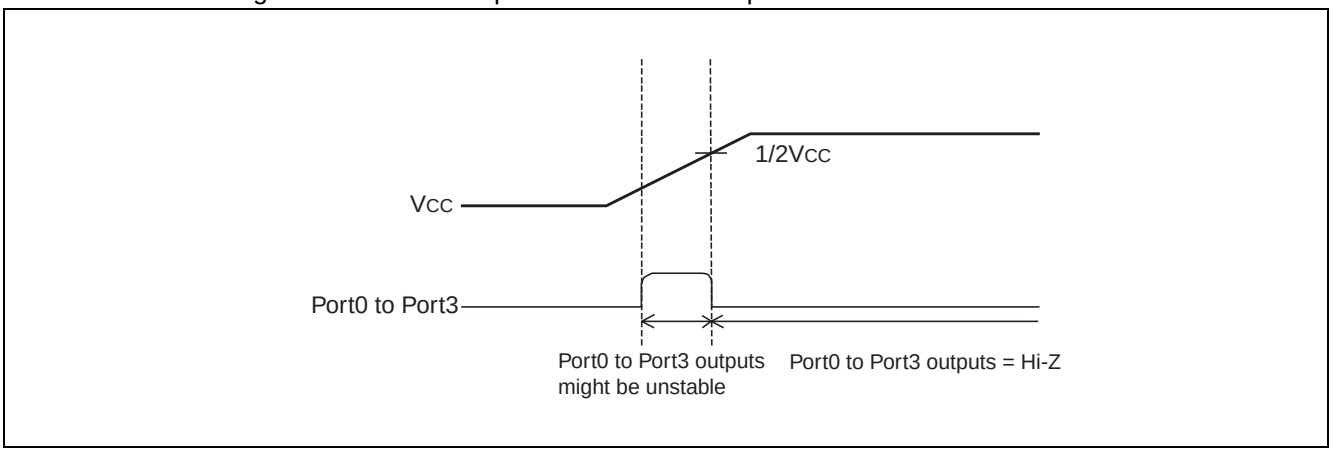
  Stabilize the power supply voltage as follows as a standard level of stabilization.
  - V_{CC} ripple variations (peak-to-peak value) at commercial frequencies (50 Hz/60 Hz) fall below 10% of the standard V_{CC} supply voltage
  - The coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

- **Initialization**

  In the device, there are internal registers which are initialized only by a power-on reset. To initialize these registers, turn on the power again.

- **Port 0 to Port 3 Output During Power-on (External-bus Mode)**

  As shown below, when the power is turned on in External-Bus mode, there is a possibility that output signal of Port 0 to Port 3 might be unstable irrespective of the reset input.



- **Notes on Using the CAN Function**

  To use the CAN function, please set the DIRECT bit of the CAN Direct Mode Register (CDMR) to 1.
  If the DIRECT bit is set to '0' (initial value) only MB90V950AJAS and MB90V950AMAS, wait states will be performed when accessing CAN registers.

Note : Please refer to the Hardware Manual of the MB90950 series for detail of CAN Direct Mode Register.

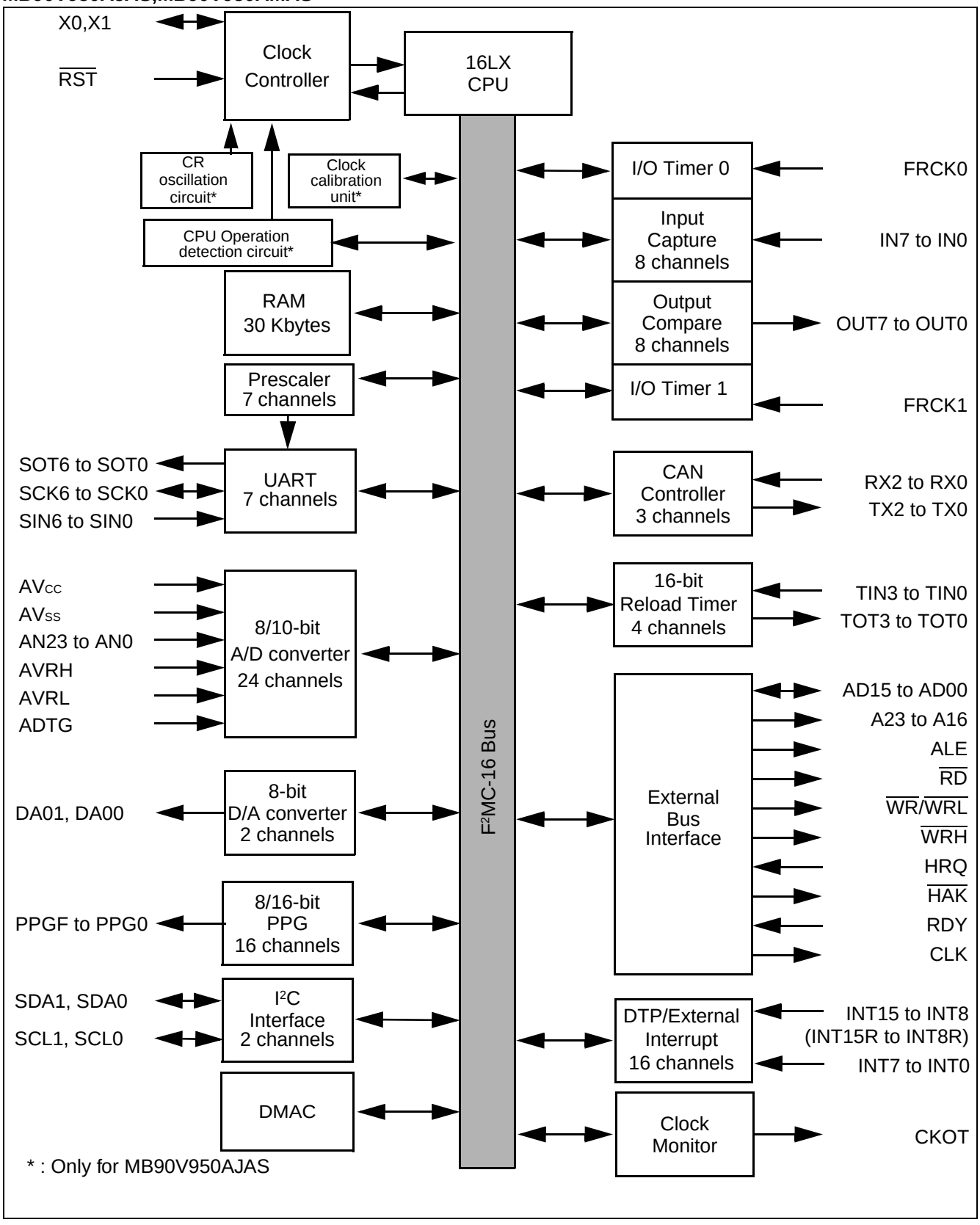
- **Flash Security Function**

  A security bit is located in the area of the Flash memory.
  If protection code 01_H is written in the security bit, the Flash memory is in the protected state by security.
  Therefore please do not write 01_H in this address if you do not use the security function.
  Refer to following table for the address of the security bit.

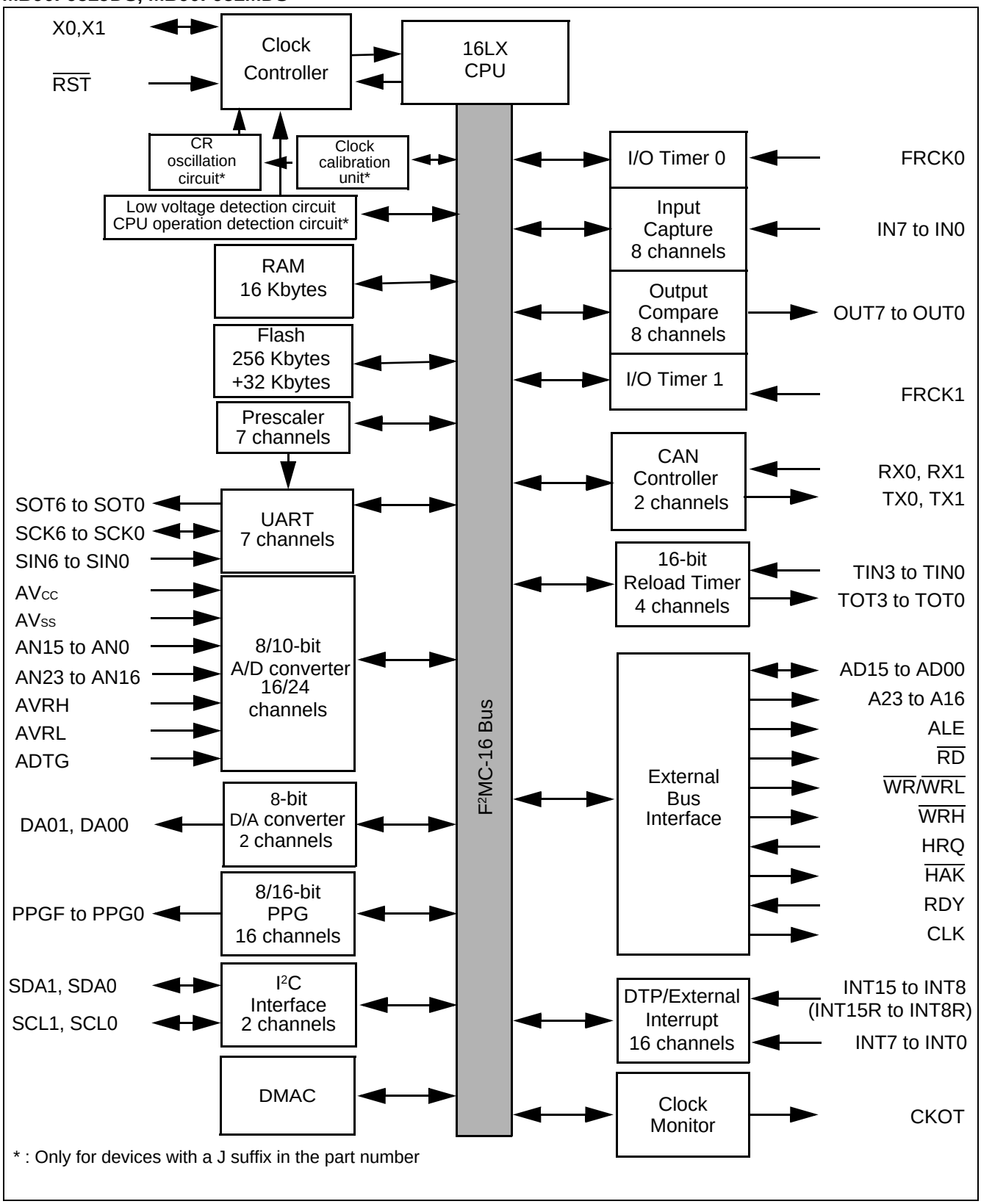
	Flash memory size	Address of the security bit
MB90F952JDS, MB90F952MDS	Embedded 2 Mbits Flash Memory	$FC0001_H$

■ BLOCK DIAGRAMS

MB90V950AJAS,MB90V950AMAS

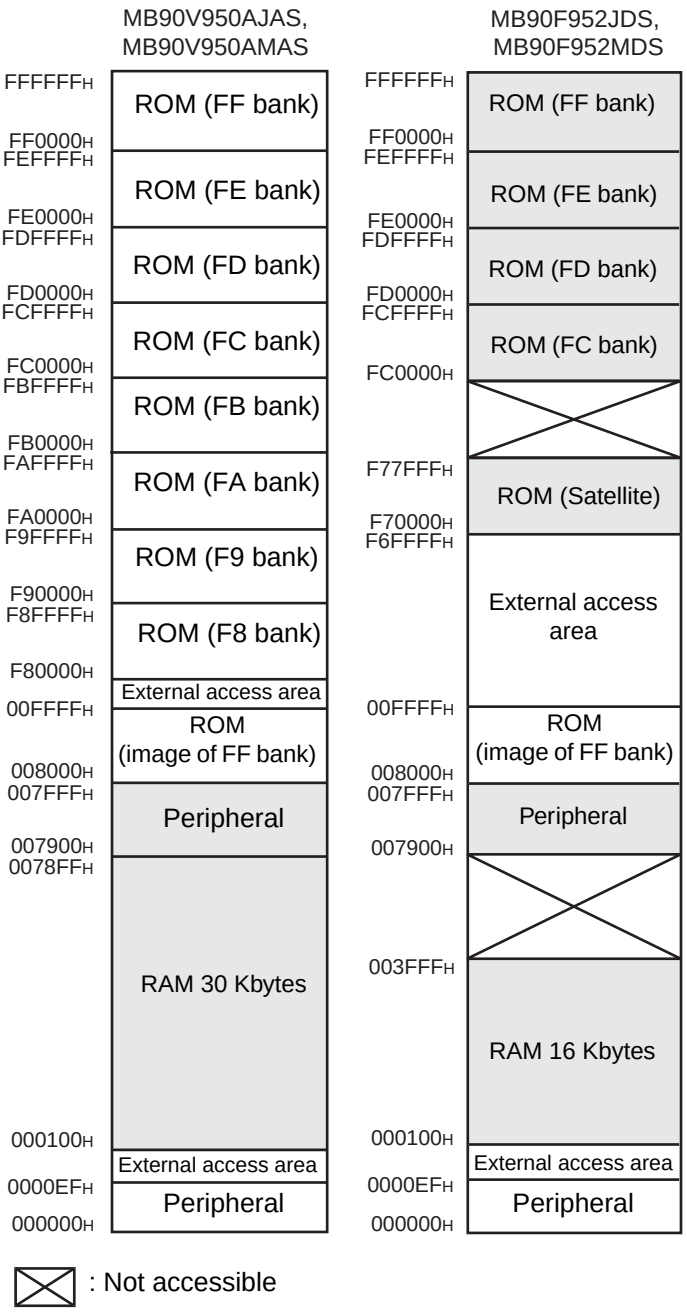


MB90F952JDS, MB90F952MDS



* : Only for devices with a J suffix in the part number

■ MEMORY MAP



Note: An image of the data in the FF bank of ROM is visible in the upper part of bank 00, which makes it possible for the C compiler to use the small memory model. The lower 16 bits of addresses in the FF bank are the same as the lower 16 bits of addresses in the 00 bank so that tables stored in the ROM can be accessed without using the far specifier in the pointer declaration.
For example, when the address 00C000H is accessed, the data at FFC000H in ROM is actually accessed.
The ROM area in bank FF exceeds 32 Kbytes, and its entire image cannot be shown in bank 00.
As a result, the image between FF8000H and FFFFFFH is visible in bank 00, while the image between FF0000H and FF7FFFH is visible only in bank FF.

■ I/O MAP

Address	Register	Abbreviation	Access	Resource name	Initial value
000000H	Port 0 Data Register	PDR0	R/W	Port 0	XXXXXXXXB
000001H	Port 1 Data Register	PDR1	R/W	Port 1	XXXXXXXXB
000002H	Port 2 Data Register	PDR2	R/W	Port 2	XXXXXXXXB
000003H	Port 3 Data Register	PDR3	R/W	Port 3	XXXXXXXXB
000004H	Port 4 Data Register	PDR4	R/W	Port 4	XXXXXXXXB
000005H	Port 5 Data Register	PDR5	R/W	Port 5	XXXXXXXXB
000006H	Port 6 Data Register	PDR6	R/W	Port 6	XXXXXXXXB
000007H	Port 7 Data Register	PDR7	R/W	Port 7	XXXXXXXXB
000008H	Port 8 Data Register	PDR8	R/W	Port 8	XXXXXXXXB
000009H	Port 9 Data Register	PDR9	R/W	Port 9	XXXXXXXXB
00000AH	Port A Data Register	PDRA	R/W	Port A	111111XXB
00000BH	Analog Input Enable Register 5	ADER5	R/W	Port 5, A/D	11111111B
00000CH	Analog Input Enable Register 6	ADER6	R/W	Port 6, A/D	11111111B
00000DH	Analog Input Enable Register 7	ADER7	R/W	Port 7, A/D	11111111B
00000EH	Input Level Select Register 0	ILSR0	R/W	Port 0 to 7	XXXXXXXXB
00000FH	Input Level Select Register 1	ILSR1	R/W	Port 0 to 3, Port 8 to A	XXXX0XXXB
000010H	Port 0 Direction Register	DDR0	R/W	Port 0	00000000B
000011H	Port 1 Direction Register	DDR1	R/W	Port 1	00000000B
000012H	Port 2 Direction Register	DDR2	R/W	Port 2	00000000B
000013H	Port 3 Direction Register	DDR3	R/W	Port 3	00000000B
000014H	Port 4 Direction Register	DDR4	R/W	Port 4	00000000B
000015H	Port 5 Direction Register	DDR5	R/W	Port 5	00000000B
000016H	Port 6 Direction Register	DDR6	R/W	Port 6	00000000B
000017H	Port 7 Direction Register	DDR7	R/W	Port 7	00000000B
000018H	Port 8 Direction Register	DDR8	R/W	Port 8	00000000B
000019H	Port 9 Direction Register	DDR9	R/W	Port 9	00000000B
00001AH	Port A Direction Register	DDRA	R/W	Port A	00000100B
00001BH	Reserved				
00001CH	Port 0 Pull-up Control Register	PUCR0	R/W	Port 0	00000000B
00001DH	Port 1 Pull-up Control Register	PUCR1	R/W	Port 1	00000000B
00001EH	Port 2 Pull-up Control Register	PUCR2	R/W	Port 2	00000000B
00001FH	Port 3 Pull-up Control Register	PUCR3	R/W	Port 3	00000000B

(Continued)

Address	Register	Abbrevia-tion	Access	Resource name	Initial value
000020H	Serial Mode Register 0	SMR0	W, R/W	UART0	00000000B
000021H	Serial Control Register 0	SCR0	W, R/W		00000000B
000022H	Reception/Transmission Data Register 0	RDR0/ TDR0	R/W		00000000B/ 11111111B
000023H	Serial Status Register 0	SSR0	R, R/W		00001000B
000024H	Extended Communication Control Register 0	ECCR0	R, W, R/W		000000XXB
000025H	Extended Status/Control Register 0	ESCR0	R/W		00000X00B
000026H	Baud Rate Generator Register 00	BGR00	R, R/W		00000000B
000027H	Baud Rate Generator Register 01	BGR01	R, R/W		00000000B
000028H	Serial Mode Register 1	SMR1	W, R/W	UART1	00000000B
000029H	Serial Control Register 1	SCR1	W, R/W		00000000B
00002AH	Reception/Transmission Data Register 0	RDR1/ TDR1	R/W		00000000B/ 11111111B
00002BH	Serial Status Register 1	SSR1	R, R/W		00001000B
00002CH	Extended Communication Control Register 1	ECCR1	R, W, R/W		000000XXB
00002DH	Extended Status/Control Register 1	ESCR1	R/W		00000X00B
00002EH	Baud Rate Generator Register 10	BGR10	R, R/W		00000000B
00002FH	Baud Rate Generator Register 11	BGR11	R, R/W		00000000B
000030H	PPG0 Operation Mode Control Register	PPGC0	W, R/W	16-bit PPG0/PPG1	01000111B
000031H	PPG1 Operation Mode Control Register	PPGC1	W, R/W		01000001B
000032H	PPG0/PPG1 Count Clock Select Register	PPG01	R/W		00000010B
000033H	Reserved				
000034H	PPG2 Operation Mode Control Register	PPGC2	W, R/W	16-bit PPG2/PPG3	01000111B
000035H	PPG3 Operation Mode Control Register	PPGC3	W, R/W		01000001B
000036H	PPG2/PPG3 Count Clock Select Register	PPG23	R/W		00000010B
000037H	Reserved				
000038H	PPG4 Operation Mode Control Register	PPGC4	W, R/W	16-bit PPG4/PPG5	01000111B
000039H	PPG5 Operation Mode Control Register	PPGC5	W, R/W		01000001B
00003AH	PPG4/PPG5 Clock Select Register	PPG45	R/W		00000010B
00003BH	Address Detect Control Register 1	PACSR1	R/W	Address Match Detection 1	11000000B
00003CH	PPG6 Operation Mode Control Register	PPGC6	W, R/W	16-bit PPG6/PPG7	01000111B
00003DH	PPG7 Operation Mode Control Register	PPGC7	W, R/W		01000001B
00003EH	PPG6/PPG7 Count Clock Select Register	PPG67	R/W		00000010B
00003FH	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
000040H	PPG8 Operation Mode Control Register	PPGC8	W, R/W	16-bit PPG8/PPG9	01000111B
000041H	PPG9 Operation Mode Control Register	PPGC9	W, R/W		01000001B
000042H	PPG8/PPG9 Count Clock Select Register	PPG89	R/W		00000010B
000043H	Reserved				
000044H	PPGA Operation Mode Control Register	PPGCA	W, R/W	16-bit PPGA/PPGB	01000111B
000045H	PPGB Operation Mode Control Register	PPGCB	W, R/W		01000001B
000046H	PPGA/PPGB Count Clock Select Register	PPGAB	R/W		00000010B
000047H	Reserved				
000048H	PPGC Operation Mode Control Register	PPGCC	W, R/W	16-bit PPGC/PPGD	01000111B
000049H	PPGD Operation Mode Control Register	PPGCD	W, R/W		01000001B
00004AH	PPGC/PPGD Count Clock Select Register	PPGCD	R/W		00000010B
00004BH	Reserved				
00004CH	PPGE Operation Mode Control Register	PPGCE	W, R/W	16-bit PPGE/PPGF	01000111B
00004DH	PPGF Operation Mode Control Register	PPGCF	W, R/W		01000001B
00004EH	PPGE/PPGF Count Clock Select Register	PPGEF	R/W		00000010B
00004FH	Reserved				
000050H	Input Capture Control Status 0/1	ICS01	R/W	Input Capture 0/1	00000000B
000051H	Input Capture Edge 0/1	ICE01	R/W, R		111010XXB
000052H	Input Capture Control Status 2/3	ICS23	R/W	Input Capture 2/3	00000000B
000053H	Input Capture Edge 2/3	ICE23	R		111111XXB
000054H	Input Capture Control Status 4/5	ICS45	R/W	Input Capture 4/5	00000000B
000055H	Input Capture Edge 4/5	ICE45	R		111100XXB
000056H	Input Capture Control Status 6/7	ICS67	R/W	Input Capture 6/7	00000000B
000057H	Input Capture Edge 6/7	ICE67	R/W, R		111000XXB
000058H	Output Compare Control Status 0	OCS0	R/W	Output Compare 0/1	00001100B
000059H	Output Compare Control Status 1	OCS1	R/W		01100000B
00005AH	Output Compare Control Status 2	OCS2	R/W	Output Compare 2/3	00001100B
00005BH	Output Compare Control Status 3	OCS3	R/W		01100000B
00005CH	Output Compare Control Status 4	OCS4	R/W	Output Compare 4/5	00001100B
00005DH	Output Compare Control Status 5	OCS5	R/W		01100000B
00005EH	Output Compare Control Status 6	OCS6	R/W	Output Compare 6/7	00001100B
00005FH	Output Compare Control Status 7	OCS7	R/W		01100000B
000060H	Timer Control Status 0	TMCSR0	R/W	16-bit reload timer 0	00000000B
000061H	Timer Control Status 0	TMCSR0	R/W		11110000B
000062H	Timer Control Status 1	TMCSR1	R/W	16-bit reload timer 1	00000000B
000063H	Timer Control Status 1	TMCSR1	R/W		11110000B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
000064H	Timer Control Status 2	TMCSR2	R/W	16-bit reload timer 2	00000000B
000065H	Timer Control Status 2	TMCSR2	R/W		11110000B
000066H	Timer Control Status 3	TMCSR3	R/W	16-bit reload timer 3	00000000B
000067H	Timer Control Status 3	TMCSR3	R/W		11110000B
000068H	A/D Control Status 0	ADCS0	R/W	A/D Converter	00011110B
000069H	A/D Control Status 1	ADCS1	R/W		00000001B
00006AH	A/D Data 0	ADCR0	R		00000000B
00006BH	A/D Data 1	ADCR1	R		11111100B
00006CH	ADC Setting 0	ADSR0	R/W		00000000B
00006DH	ADC Setting 1	ADSR1	R/W		00000000B
00006EH	Low Voltage/CPU OPeration Detection Reset Control Register	LVRC	R/W	Low Voltage/CPU Operation Detection Reset	00111000B
00006FH	ROM Mirror Function Setting	ROMM	W	ROM Mirror	11111101B
000070H to 00008FH	Reserved for CAN Controller				
000090H to 00009AH	Reserved				
00009BH	DMA Descriptor Channel Specified Register	DCSR	R/W	DMA	00000000B
00009CH	DMA Status Register L	DSRL	R/W		00000000B
00009DH	DMA Status Register H	DSRH	R/W		00000000B
00009EH	Address Detect Control Register 0	PACSR0	R/W	Address Match Detection 0	11000000B
00009FH	Delayed Interrupt Trigger/Release Register	DIRR	R/W	Delayed Interrupt Generation Module	11111110B
0000A0H	Low-power Mode Control Register	LPMCR	W, R/W	Low Power Control Circuit	00011000B
0000A1H	Clock Selection Register	CKSCR	R, R/W	Low Power Control Circuit	11111100B
0000A2H, 0000A3H	Reserved				
0000A4H	DMA Stop Status Register	DSSR	R/W	DMA	00000000B
0000A5H	Automatic Ready Function Select Register	ARSR	W	External Memory Access	00111100B
0000A6H	External Address Output Control Register	HACR	W		00000000B
0000A7H	Bus Control Signal Selection Register	ECSR	W		00000001B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
0000A8H	Watchdog Control Register	WDTC	R, W	Watchdog Timer	X1XXX111B
0000A9H	Time Base Timer Control Register	TBTC	W, R/W	Time Base Timer	11100100B
0000AAH	Watch Timer Control Register	WTC	R, R/W	Watch Timer	1X001000B
0000ABH	Reserved				
0000ACH	DMA Enable Register L	DERL	R/W	DMA	00000000B
0000ADH	DMA Enable Register H	DERH	R/W		00000000B
0000AEH	Flash Control Status Register (Flash memory devices only)	FMCS	R, R/W	Flash Memory	000X0000B
0000AFH	Reserved				
0000B0H	Interrupt Control Register 00	ICR00	W, R/W	Interrupt Control	00000111B
0000B1H	Interrupt Control Register 01	ICR01	W, R/W		00000111B
0000B2H	Interrupt Control Register 02	ICR02	W, R/W		00000111B
0000B3H	Interrupt Control Register 03	ICR03	W, R/W		00000111B
0000B4H	Interrupt Control Register 04	ICR04	W, R/W		00000111B
0000B5H	Interrupt Control Register 05	ICR05	W, R/W		00000111B
0000B6H	Interrupt Control Register 06	ICR06	W, R/W		00000111B
0000B7H	Interrupt Control Register 07	ICR07	W, R/W		00000111B
0000B8H	Interrupt Control Register 08	ICR08	W, R/W		00000111B
0000B9H	Interrupt Control Register 09	ICR09	W, R/W		00000111B
0000BAH	Interrupt Control Register 10	ICR10	W, R/W		00000111B
0000BBH	Interrupt Control Register 11	ICR11	W, R/W		00000111B
0000BCH	Interrupt Control Register 12	ICR12	W, R/W		00000111B
0000BDH	Interrupt Control Register 13	ICR13	W, R/W		00000111B
0000BEH	Interrupt Control Register 14	ICR14	W, R/W		00000111B
0000BFH	Interrupt Control Register 15	ICR15	W, R/W		00000111B
0000C0H	D/A Converter Data 0	DAT0	R/W	D/A Converter	XXXXXXXXB
0000C1H	D/A Converter Data 1	DAT1	R/W		XXXXXXXXB
0000C2H	D/A Control 0	DACR0	R/W		00000000B
0000C3H	D/A Control 1	DACR1	R/W		00000000B
0000C4H, 0000C5H	Reserved				
0000C6H	External Interrupt Enable 0	ENIR0	R/W	DTP/External Interrupt 0	00000000B
0000C7H	External Interrupt Source 0	EIRR0	R/W		XXXXXXXXB
0000C8H	Detection Level Setting 0	ELVR0	R/W		00000000B
0000C9H	Detection Level Setting 0	ELVR0	R/W		00000000B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
0000CA$_H$	External Interrupt Enable 1	ENIR1	R/W	DTP/External Interrupt 1	00000000$_B$
0000CB$_H$	External Interrupt Source 1	EIRR1	R/W		XXXXXXXX$_B$
0000CC$_H$	Detection Level Setting 1	ELVR1	R/W		00000000$_B$
0000CD$_H$	Detection Level Setting 1	ELVR1	R/W		00000000$_B$
0000CE$_H$	External Interrupt Source Select	EISSR	R/W		00000000$_B$
0000CF$_H$	PLL/Sub clock Control Register	PSCCR	W	PLL	11110000$_B$
0000D0$_H$	DMA Buffer Address Pointer L Register	BAPL	R/W	DMA	XXXXXXXX$_B$
0000D1$_H$	DMA Buffer Address Pointer M Register	BAPM	R/W		XXXXXXXX$_B$
0000D2$_H$	DMA Buffer Address Pointer H Register	BAPH	R/W		XXXXXXXX$_B$
0000D3$_H$	DMA Control Register	DMACS	R/W		XXXXXXXX$_B$
0000D4$_H$	I/O Register Address Pointer L Register	IOAL	R/W		XXXXXXXX$_B$
0000D5$_H$	I/O Register Address Pointer H Register	IOAH	R/W		XXXXXXXX$_B$
0000D6$_H$	Data Counter L Register	DCTL	R/W		XXXXXXXX$_B$
0000D7$_H$	Data Counter H Register	DCTH	R/W		XXXXXXXX$_B$
0000D8$_H$	Serial Mode Register 2	SMR2	W, R/W	UART2	00000000$_B$
0000D9$_H$	Serial Control Register 2	SCR2	W, R/W		00000000$_B$
0000DA$_H$	Reception/Transmission Data Register 2	RDR2/ TDR2	R/W		00000000$_B$/ 11111111$_B$
0000DB$_H$	Serial Status Register 2	SSR2	R, R/W		00001000$_B$
0000DC$_H$	Extended Communication Control Register 2	ECCR2	R, W, R/W		000000XX$_B$
0000DD$_H$	Extended Status Control Register 2	ESCR2	R/W		00000X00$_B$
0000DE$_H$	Baud Rate Generator Register 20	BGR20	R, R/W		00000000$_B$
0000DF$_H$	Baud Rate Generator Register 21	BGR21	R, R/W		00000000$_B$
0000E0$_H$ to 0000EF$_H$	Reserved for CAN Controller 2. Refer to "■ CAN CONTROLLERS"				
0000F0$_H$ to 0000FF$_H$	External				
007900$_H$	Reload Register L0	PRLL0	R/W	16-bit PPG0/PPG1	XXXXXXXX$_B$
007901$_H$	Reload Register H0	PRLH0	R/W		XXXXXXXX$_B$
007902$_H$	Reload Register L1	PRLL1	R/W		XXXXXXXX$_B$
007903$_H$	Reload Register H1	PRLH1	R/W		XXXXXXXX$_B$
007904$_H$	Reload Register L2	PRLL2	R/W	16-bit PPG2/PPG3	XXXXXXXX$_B$
007905$_H$	Reload Register H2	PRLH2	R/W		XXXXXXXX$_B$
007906$_H$	Reload Register L3	PRLL3	R/W		XXXXXXXX$_B$
007907$_H$	Reload Register H3	PRLH3	R/W		XXXXXXXX$_B$

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
007908H	Reload Register L4	PRLL4	R/W	16-bit PPG4/PPG5	XXXXXXXXB
007909H	Reload Register H4	PRLH4	R/W		XXXXXXXXB
00790AH	Reload Register L5	PRLL5	R/W		XXXXXXXXB
00790BH	Reload Register H5	PRLH5	R/W		XXXXXXXXB
00790CH	Reload Register L6	PRLL6	R/W	16-bit PPG6/PPG7	XXXXXXXXB
00790DH	Reload Register H6	PRLH6	R/W		XXXXXXXXB
00790EH	Reload Register L7	PRLL7	R/W		XXXXXXXXB
00790FH	Reload Register H7	PRLH7	R/W		XXXXXXXXB
007910H	Reload Register L8	PRLL8	R/W	16-bit PPG8/PPG9	XXXXXXXXB
007911H	Reload Register H8	PRLH8	R/W		XXXXXXXXB
007912H	Reload Register L9	PRLL9	R/W		XXXXXXXXB
007913H	Reload Register H9	PRLH9	R/W		XXXXXXXXB
007914H	Reload Register LA	PRLLA	R/W	16-bit PPGA/PPGB	XXXXXXXXB
007915H	Reload Register HA	PRLHA	R/W		XXXXXXXXB
007916H	Reload Register LB	PRLLB	R/W		XXXXXXXXB
007917H	Reload Register HB	PRLHB	R/W		XXXXXXXXB
007918H	Reload Register LC	PRLLC	R/W	16-bit PPGC/PPGD	XXXXXXXXB
007919H	Reload Register HC	PRLHC	R/W		XXXXXXXXB
00791AH	Reload Register LD	PRLLD	R/W		XXXXXXXXB
00791BH	Reload Register HD	PRLHD	R/W		XXXXXXXXB
00791CH	Reload Register LE	PRLLE	R/W	16-bit PPGE/PPGF	XXXXXXXXB
00791DH	Reload Register HE	PRLHE	R/W		XXXXXXXXB
00791EH	Reload Register LF	PRLLF	R/W		XXXXXXXXB
00791FH	Reload Register HF	PRLHF	R/W		XXXXXXXXB
007920H	Input Capture 0	IPCP0	R	Input Capture 0/1*	00000000B
007921H	Input Capture 0	IPCP0	R		00000000B
007922H	Input Capture 1	IPCP1	R		00000000B
007923H	Input Capture 1	IPCP1	R		00000000B
007924H	Input Capture 2	IPCP2	R	Input Capture 2/3*	00000000B
007925H	Input Capture 2	IPCP2	R		00000000B
007926H	Input Capture 3	IPCP3	R		00000000B
007927H	Input Capture 3	IPCP3	R		00000000B
007928H	Input Capture 4	IPCP4	R	Input Capture 4/5*	00000000B
007929H	Input Capture 4	IPCP4	R		00000000B
00792AH	Input Capture 5	IPCP5	R		00000000B
00792BH	Input Capture 5	IPCP5	R		00000000B

* : The Initial values of MB90V950AJAS and MB90V950AMAS are XXXXXXXXB.

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
00792C$_H$	Input Capture 6	IPCP6	R	Input Capture 6/7*	00000000$_B$
00792D$_H$	Input Capture 6	IPCP6	R		00000000$_B$
00792E$_H$	Input Capture 7	IPCP7	R		00000000$_B$
00792F$_H$	Input Capture 7	IPCP7	R		00000000$_B$
007930$_H$	Output Compare 0	OCCP0	R/W	Output Compare 0/1	XXXXXXXX$_B$
007931$_H$	Output Compare 0	OCCP0	R/W		XXXXXXXX$_B$
007932$_H$	Output Compare 1	OCCP1	R/W		XXXXXXXX$_B$
007933$_H$	Output Compare 1	OCCP1	R/W		XXXXXXXX$_B$
007934$_H$	Output Compare 2	OCCP2	R/W	Output Compare 2/3	XXXXXXXX$_B$
007935$_H$	Output Compare 2	OCCP2	R/W		XXXXXXXX$_B$
007936$_H$	Output Compare 3	OCCP3	R/W		XXXXXXXX$_B$
007937$_H$	Output Compare 3	OCCP3	R/W		XXXXXXXX$_B$
007938$_H$	Output Compare 4	OCCP4	R/W	Output Compare 4/5	XXXXXXXX$_B$
007939$_H$	Output Compare 4	OCCP4	R/W		XXXXXXXX$_B$
00793A$_H$	Output Compare 5	OCCP5	R/W		XXXXXXXX$_B$
00793B$_H$	Output Compare 5	OCCP5	R/W		XXXXXXXX$_B$
00793C$_H$	Output Compare 6	OCCP6	R/W	Output Compare 6/7	XXXXXXXX$_B$
00793D$_H$	Output Compare 6	OCCP6	R/W		XXXXXXXX$_B$
00793E$_H$	Output Compare 7	OCCP7	R/W		XXXXXXXX$_B$
00793F$_H$	Output Compare 7	OCCP7	R/W		XXXXXXXX$_B$
007940$_H$	Timer Data 0	TCDT0	R/W	I/O Timer 0	00000000$_B$
007941$_H$	Timer Data 0	TCDT0	R/W		00000000$_B$
007942$_H$	Timer Control Status 0	TCCSL0	R/W		00000000$_B$
007943$_H$	Timer Control Status 0	TCCSH0	R/W		01100000$_B$
007944$_H$	Timer Data 1	TCDT1	R/W	I/O Timer 1	00000000$_B$
007945$_H$	Timer Data 1	TCDT1	R/W		00000000$_B$
007946$_H$	Timer Control Status 1	TCCSL1	R/W		00000000$_B$
007947$_H$	Timer Control Status 1	TCCSH1	R/W		01100000$_B$
007948$_H$	Timer 0/Reload 0	TMR0/ TMRLR0	R/W	16-bit Reload Timer 0	XXXXXXXX$_B$
007949$_H$			R/W		XXXXXXXX$_B$
00794A$_H$	Timer 1/Reload 1	TMR1/ TMRLR1	R/W	16-bit Reload Timer 1	XXXXXXXX$_B$
00794B$_H$			R/W		XXXXXXXX$_B$
00794C$_H$	Timer 2/Reload 2	TMR2/ TMRLR2	R/W	16-bit Reload Timer 2	XXXXXXXX$_B$
00794D$_H$			R/W		XXXXXXXX$_B$
00794E$_H$	Timer 3/Reload 3	TMR3/ TMRLR3	R/W	16-bit Reload Timer 3	XXXXXXXX$_B$
00794F$_H$			R/W		XXXXXXXX$_B$

* : The Initial values of MB90V950AJAS and MB90V950AMAS are XXXXXXXX$_B$.

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
007950H	Serial Mode Register 3	SMR3	W, R/W	UART3	00000000B
007951H	Serial Control Register 3	SCR3	W, R/W		00000000B
007952H	Reception/Transmission Data Register 3	RDR3/TDR3	R/W		00000000B/ 11111111B
007953H	Serial Status Register 3	SSR3	R, R/W		00001000B
007954H	Extended Communication Control Register 3	ECCR3	R, W, R/W		000000XXB
007955H	Extended Status Control Register 3	ESCR3	R/W		00000X00B
007956H	Baud Rate Generator Register 30	BGR30	R, R/W		00000000B
007957H	Baud Rate Generator Register 31	BGR31	R, R/W		00000000B
007958H	Serial Mode Register 4	SMR4	W, R/W	UART4	00000000B
007959H	Serial Control Register 4	SCR4	W, R/W		00000000B
00795AH	Reception/Transmission Data Register 4	RDR4/TDR4	R/W		00000000B/ 11111111B
00795BH	Serial Status Register 4	SSR4	R, R/W		00001000B
00795CH	Extended Communication Control Register 4	ECCR4	R, W, R/W		000000XXB
00795DH	Extended Status Control Register 4	ESCR4	R/W		00000X00B
00795EH	Baud Rate Generator Register 40	BGR40	R, R/W		00000000B
00795FH	Baud Rate Generator Register 41	BGR41	R, R/W		00000000B
007960H	Clock Supervisor Control Register	CSVCR	R/W	Clock Supervisor	00011100B
007961H to 00796BH	Reserved				
00796CH	Clock Output Enable Register	CLKR	R/W	Clock Monitor	11110000 B
00796DH	Reserved				
00796EH	CAN Direct Mode Register	CDMR	R/W	CAN Clock Sync	11111110 B
00796FH	CAN Switch Register	CANSWR	R/W	CAN 0/1	11111100 B
007970H	I²C Bus Status Register 0	IBSR0	R	I²C Interface 0	00000000B
007971H	I²C Bus Control Register 0	IBCR0	W, R/W		00000000B
007972H	I²C 10-bit Slave Address Register 0	ITBAL0	R/W		00000000B
007973H		ITBAH0	R/W		00000000B
007974H	I²C 10-bit Slave Address Mask Register 0	ITMKL0	R/W		11111111B
007975H		ITMKH0	R/W		00111111B
007976H	I²C 7-bit Slave Address Register 0	ISBA0	R/W		00000000B
007977H	I²C 7-bit Slave Address Mask Register 0	ISMK0	R/W		01111111B
007978H	I²C Data Register 0	IDAR0	R/W		00000000B
007979H, 00797AH	Reserved				

(Continued)

Address	Register	Abbrevia-tion	Access	Resource name	Initial value
00797B$_H$	I^{2}C Clock Control Register 0	ICCR0	R/W	I^{2}C Interface 0	00011111$_B$
00797C$_H$ to 00797F$_H$	Reserved				
007980$_H$	I^{2}C Bus Status Register 1	IBSR1	R	I^{2}C Interface 1	00000000$_B$
007981$_H$	I^{2}C Bus Control Register 1	IBCR1	W, R/W		00000000$_B$
007982$_H$	I^{2}C 10-bit Slave Address Register 1	ITBAL1	R/W		00000000$_B$
007983$_H$		ITBAH1	R/W		00000000$_B$
007984$_H$	I^{2}C 10-bit Slave Address Mask Register 1	ITMKL1	R/W		11111111$_B$
007985$_H$		ITMKH1	R/W		00111111$_B$
007986$_H$	I^{2}C 7-bit Slave Address Register 1	ISBA1	R/W		00000000$_B$
007987$_H$	I^{2}C 7-bit Slave Address Mask Register 1	ISMK1	R/W		01111111$_B$
007988$_H$	I^{2}C Data Register 1	IDAR1	R/W		00000000$_B$
007989$_H$, 00798A$_H$	Reserved				
00798B$_H$	I^{2}C Clock Control Register 1	ICCR1	R/W	I^{2}C Interface1	00011111$_B$
00798C$_H$ to 00798F$_H$	Reserved				
007990$_H$	Serial Mode Register 5	SMR5	W, R/W	UART5	00000000$_B$
007991$_H$	Serial Control Register 5	SCR5	W, R/W		00000000$_B$
007992$_H$	Reception/Transmission Data Register 5	RDR5/ TDR5	R/W		00000000$_B$/ 11111111$_B$
007993$_H$	Serial Status Register 5	SSR5	R, R/W		00001000$_B$
007994$_H$	Extended Communication Control Register 5	ECCR5	R, W, R/W		000000XX$_B$
007995$_H$	Extended Status Control Register 5	ESCR5	R/W		00000X00$_B$
007996$_H$	Baud Rate Generator Register 50	BGR50	R, R/W		00000000$_B$
007997$_H$	Baud Rate Generator Register 51	BGR51	R, R/W		00000000$_B$
007998$_H$	Serial Mode Register 6	SMR6	W, R/W	UART6	00000000$_B$
007999$_H$	Serial Control Register 6	SCR6	W, R/W		00000000$_B$
00799A$_H$	Reception/Transmission Data Register 6	RDR6/ TDR6	R/W		00000000$_B$/ 11111111$_B$
00799B$_H$	Serial Status Register 6	SSR6	R, R/W		00001000$_B$
00799C$_H$	Extended Communication Control Register 6	ECCR6	R, W, R/W		000000XX$_B$
00799D$_H$	Extended Status Control Register 6	ESCR6	R/W		00000X00$_B$
00799E$_H$	Baud Rate Generator Register 60	BGR60	R, R/W		00000000$_B$
00799F$_H$	Baud Rate Generator Register 61	BGR61	R, R/W		00000000$_B$

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
0079A0H	UART Input Level Setting Register	ILSR2	R/W	UART	11111100B
0079A1H	Reserved				
0079A2H	Flash Write Control Register 0	FWR0	R/W	Flash Memory	00000000B
0079A3H	Flash Write Control Register 1	FWR1	R/W	Flash Memory	00000000B
0079A4H to 0079B1H	Reserved				
0079B2H	Low Voltage/CPU Operation Detection Setting Register	LVRS	R/W	Low Voltage/ CPU Operation Detection Reset	10000111B
0079B3H to 0079B7H	Reserved				
0079B8H	Clock Calibration Unit Control	CUCR	R/W	Clock Calibration Unit	00000000B
0079B9H	CR Oscillation Trimming Setting	CRTR	R/W		11110111B
0079BAH	CR Oscillation Timer Data Register	CUTDL	R/W		01010000B
0079BBH		CUTDH	R/W		11000011B
0079BCH	Main Timer Data Register 1	CUTR1L	R		00000000B
0079BDH		CUTR1H	R		00000000B
0079BEH	Main Timer Data Register 2	CUTR2L	R		00000000B
0079BFH		CUTR2H	R		00000000B
0079C0H to 0079DFH	Reserved				
0079E0H	Detect Address Setting 0	PADR0	R/W	Address Match Detection 0	XXXXXXXXB
0079E1H	Detect Address Setting 0	PADR0	R/W		XXXXXXXXB
0079E2H	Detect Address Setting 0	PADR0	R/W		XXXXXXXXB
0079E3H	Detect Address Setting 1	PADR1	R/W		XXXXXXXXB
0079E4H	Detect Address Setting 1	PADR1	R/W		XXXXXXXXB
0079E5H	Detect Address Setting 1	PADR1	R/W		XXXXXXXXB
0079E6H	Detect Address Setting 2	PADR2	R/W	Address Match Detection 0	XXXXXXXXB
0079E7H	Detect Address Setting 2	PADR2	R/W		XXXXXXXXB
0079E8H	Detect Address Setting 2	PADR2	R/W		XXXXXXXXB

(Continued)

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
0079E9H to 0079EFH	Reserved				
0079F0H	Detect Address Setting 3	PADR3	R/W	Address Match Detection 1	XXXXXXXXB
0079F1H	Detect Address Setting 3	PADR3	R/W		XXXXXXXXB
0079F2H	Detect Address Setting 3	PADR3	R/W		XXXXXXXXB
0079F3H	Detect Address Setting 4	PADR4	R/W		XXXXXXXXB
0079F4H	Detect Address Setting 4	PADR4	R/W		XXXXXXXXB
0079F5H	Detect Address Setting 4	PADR4	R/W		XXXXXXXXB
0079F6H	Detect Address Setting 5	PADR5	R/W		XXXXXXXXB
0079F7H	Detect Address Setting 5	PADR5	R/W		XXXXXXXXB
0079F8H	Detect Address Setting 5	PADR5	R/W		XXXXXXXXB
0079F9H to 0079FFH	Reserved				
007A00H to 007AFFH	Reserved for CAN Controller 0. Refer to “■ CAN CONTROLLERS”				
007B00H to 007BFFH	Reserved for CAN Controller 0. Refer to “■ CAN CONTROLLERS”				
007C00H to 007CFFH	Reserved for CAN Controller 1. Refer to “■ CAN CONTROLLERS”				
007D00H to 007DFFH	Reserved for CAN Controller 1. Refer to “■ CAN CONTROLLERS”				
007E00H to 007EFFH	Reserved for CAN Controller 2. Refer to “■ CAN CONTROLLERS”				
007F00H to 007FFFH	Reserved for CAN Controller 2. Refer to “■ CAN CONTROLLERS”				

Notes : • Initial value of “X” represents unknown value.
• Any write access to reserved addresses in I/O map should not be performed. A read access to reserved addresses results in reading “X”.

■ CAN CONTROLLERS

The CAN controller has the following features:

- Conforms to CAN Specification Version 2.0 Part A and B
  - Supports transmission/reception in standard frame and extended frame formats
- Supports transmission of data frames by receiving remote frames
- 16 transmission/reception message buffers
  - 29-bit ID and 8-byte data
  - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
  - Two acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 kbps to 2 Mbps (when input clock is at 16 MHz)

• List of Control Registers (1)

Address			Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2				
000070_H	000080_H	$0000E0_H$	Message Buffer Valid Register	BVALR	R/W	00000000_B 00000000_B
000071_H	000081_H	$0000E1_H$				
000072_H	000082_H	$0000E2_H$	Transmit Request Register	TREQR	R/W	00000000_B 00000000_B
000073_H	000083_H	$0000E3_H$				
000074_H	000084_H	$0000E4_H$	Transmit Cancel Register	TCANR	W	00000000_B 00000000_B
000075_H	000085_H	$0000E5_H$				
000076_H	000086_H	$0000E6_H$	Transmission Complete Register	TCR	R/W	00000000_B 00000000_B
000077_H	000087_H	$0000E7_H$				
000078_H	000088_H	$0000E8_H$	Receive Complete Register	RCR	R/W	00000000_B 00000000_B
000079_H	000089_H	$0000E9_H$				
$00007A_H$	$00008A_H$	$0000EA_H$	Remote Request Receiving Register	RRTRR	R/W	00000000_B 00000000_B
$00007B_H$	$00008B_H$	$0000EB_H$				
$00007C_H$	$00008C_H$	$0000EC_H$	Receive Overrun Register	ROVRR	R/W	00000000_B 00000000_B
$00007D_H$	$00008D_H$	$0000ED_H$				
$00007E_H$	$00008E_H$	$0000EE_H$	Reception Interrupt Enable Register	RIER	R/W	00000000_B 00000000_B
$00007F_H$	$00008F_H$	$0000EF_H$				

• **List of Control Registers (2)**

Address			Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2				
007B00H	007D00H	007F00H	Control Status Register	CSR	R/W, W R/W, R	0XXXX0X1B 00XXX000B
007B01H	007D01H	007F01H				
007B02H	007D02H	007F02H	Last Event Indicator Register	LEIR	R/W	000X0000B XXXXXXXXB
007B03H	007D03H	007F03H				
007B04H	007D04H	007F04H	Receive And Transmit Error Counter	RTEC	R	00000000B 00000000B
007B05H	007D05H	007F05H				
007B06H	007D06H	007F06H	Bit Timing Register	BTR	R/W	11111111B X1111111B
007B07H	007D07H	007F07H				
007B08H	007D08H	007F08H	IDE Register	IDER	R/W	XXXXXXXXB XXXXXXXXB
007B09H	007D09H	007F09H				
007B0AH	007D0AH	007F0AH	Transmit RTR Register	TRTRR	R/W	00000000B 00000000B
007B0BH	007D0BH	007F0BH				
007B0CH	007D0CH	007F0CH	Remote Frame Receive Waiting Register	RFWTR	R/W	XXXXXXXXB XXXXXXXXB
007B0DH	007D0DH	007F0DH				
007B0EH	007D0EH	007F0EH	Transmit Interrupt Enable Register	TIER	R/W	00000000B 00000000B
007B0FH	007D0FH	007F0FH				
007B10H	007D10H	007F10H	Acceptance Mask Select Register	AMSR	R/W	XXXXXXXXB XXXXXXXXB
007B11H	007D11H	007F11H				
007B12H	007D12H	007F12H				XXXXXXXXB XXXXXXXXB
007B13H	007D13H	007F13H				
007B14H	007D14H	007F14H	Acceptance Mask Register 0	AMR0	R/W	XXXXXXXXB XXXXXXXXB
007B15H	007D15H	007F15H				
007B16H	007D16H	007F16H				XXXXXXXXB XXXXXXXXB
007B17H	007D17H	007F17H				
007B18H	007D18H	007F18H	Acceptance Mask Register 1	AMR1	R/W	XXXXXXXXB XXXXXXXXB
007B19H	007D19H	007F19H				
007B1AH	007D1AH	007F1AH				XXXXXXXXB XXXXXXXXB
007B1BH	007D1BH	007F1BH				

• **List of Message Buffers (ID Registers) (1)**

Address			Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2				
007A00H to 007A1FH	007C00H to 007C1FH	007E00H to 007E1FH	General-Purpose Ram	—	R/W	XXXXXXXXB to XXXXXXXXB
007A20H	007C20H	007E20H	ID Register 0	IDR0	R/W	XXXXXXXXB XXXXXXXXB
007A21H	007C21H	007E21H				
007A22H	007C22H	007E22H				XXXXXXXXB XXXXXXXXB
007A23H	007C23H	007E23H				
007A24H	007C24H	007E24H	ID Register 1	IDR1	R/W	XXXXXXXXB XXXXXXXXB
007A25H	007C25H	007E25H				
007A26H	007C26H	007E26H				XXXXXXXXB XXXXXXXXB
007A27H	007C27H	007E27H				
007A28H	007C28H	007E28H	ID Register 2	IDR2	R/W	XXXXXXXXB XXXXXXXXB
007A29H	007C29H	007E29H				
007A2AH	007C2AH	007E2AH				XXXXXXXXB XXXXXXXXB
007A2BH	007C2BH	007E2BH				
007A2CH	007C2CH	007E2CH	ID Register 3	IDR3	R/W	XXXXXXXXB XXXXXXXXB
007A2DH	007C2DH	007E2DH				
007A2EH	007C2EH	007E2EH				XXXXXXXXB XXXXXXXXB
007A2FH	007C2FH	007E2FH				
007A30H	007C30H	007E30H	ID Register 4	IDR4	R/W	XXXXXXXXB XXXXXXXXB
007A31H	007C31H	007E31H				
007A32H	007C32H	007E32H				XXXXXXXXB XXXXXXXXB
007A33H	007C33H	007E33H				
007A34H	007C34H	007E34H	ID Register 5	IDR5	R/W	XXXXXXXXB XXXXXXXXB
007A35H	007C35H	007E35H				
007A36H	007C36H	007E36H				XXXXXXXXB XXXXXXXXB
007A37H	007C37H	007E37H				
007A38H	007C38H	007E38H	ID Register 6	IDR6	R/W	XXXXXXXXB XXXXXXXXB
007A39H	007C39H	007E39H				
007A3AH	007C3AH	007E3AH				XXXXXXXXB XXXXXXXXB
007A3BH	007C3BH	007E3BH				
007A3CH	007C3CH	007E3CH	ID Register 7	IDR7	R/W	XXXXXXXXB XXXXXXXXB
007A3DH	007C3DH	007E3DH				
007A3EH	007C3EH	007E3EH				XXXXXXXXB XXXXXXXXB
007A3FH	007C3FH	007E3FH				

• **List of Message Buffers (ID Registers) (2)**

Address			Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2				
007A40H	007C40H	007E40H	ID Register 8	IDR8	R/W	XXXXXXXXB XXXXXXXXB
007A41H	007C41H	007E41H				
007A42H	007C42H	007E42H				XXXXXXXXB XXXXXXXXB
007A43H	007C43H	007E43H				
007A44H	007C44H	007E44H	ID Register 9	IDR9	R/W	XXXXXXXXB XXXXXXXXB
007A45H	007C45H	007E45H				
007A46H	007C46H	007E46H				XXXXXXXXB XXXXXXXXB
007A47H	007C47H	007E47H				
007A48H	007C48H	007E48H	ID Register 10	IDR10	R/W	XXXXXXXXB XXXXXXXXB
007A49H	007C49H	007E49H				
007A4AH	007C4AH	007E4AH				XXXXXXXXB XXXXXXXXB
007A4BH	007C4BH	007E4BH				
007A4CH	007C4CH	007E4CH	ID Register 11	IDR11	R/W	XXXXXXXXB XXXXXXXXB
007A4DH	007C4DH	007E4DH				
007A4EH	007C4EH	007E4EH				XXXXXXXXB XXXXXXXXB
007A4FH	007C4FH	007E4FH				
007A50H	007C50H	007E50H	ID Register 12	IDR12	R/W	XXXXXXXXB XXXXXXXXB
007A51H	007C51H	007E51H				
007A52H	007C52H	007E52H				XXXXXXXXB XXXXXXXXB
007A53H	007C53H	007E53H				
007A54H	007C54H	007E54H	ID Register 13	IDR13	R/W	XXXXXXXXB XXXXXXXXB
007A55H	007C55H	007E55H				
007A56H	007C56H	007E56H				XXXXXXXXB XXXXXXXXB
007A57H	007C57H	007E57H				
007A58H	007C58H	007E58H	ID Register 14	IDR14	R/W	XXXXXXXXB XXXXXXXXB
007A59H	007C59H	007E59H				
007A5AH	007C5AH	007E5AH				XXXXXXXXB XXXXXXXXB
007A5BH	007C5BH	007E5BH				
007A5CH	007C5CH	007E5CH	ID Register 15	IDR15	R/W	XXXXXXXXB XXXXXXXXB
007A5DH	007C5DH	007E5DH				
007A5EH	007C5EH	007E5EH				XXXXXXXXB XXXXXXXXB
007A5FH	007C5FH	007E5FH				

• **List of Message Buffers (DLC Registers and Data Registers) (1)**

Address			Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2				
007A60H	007C60H	007E60H	DLC Register 0	DLCR0	R/W	XXXXXXXXB
007A61H	007C61H	007E61H				
007A62H	007C62H	007E62H	DLC Register 1	DLCR1	R/W	XXXXXXXXB
007A63H	007C63H	007E63H				
007A64H	007C64H	007E64H	DLC Register 2	DLCR2	R/W	XXXXXXXXB
007A65H	007C65H	007E65H				
007A66H	007C66H	007E66H	DLC Register 3	DLCR3	R/W	XXXXXXXXB
007A67H	007C67H	007E67H				
007A68H	007C68H	007E68H	DLC Register 4	DLCR4	R/W	XXXXXXXXB
007A69H	007C69H	007E69H				
007A6AH	007C6AH	007E6AH	DLC Register 5	DLCR5	R/W	XXXXXXXXB
007A6BH	007C6BH	007E6BH				
007A6CH	007C6CH	007E6CH	DLC Register 6	DLCR6	R/W	XXXXXXXXB
007A6DH	007C6DH	007E6DH				
007A6EH	007C6EH	007E6EH	DLC Register 7	DLCR7	R/W	XXXXXXXXB
007A6FH	007C6FH	007E6FH				
007A70H	007C70H	007E70H	DLC Register 8	DLCR8	R/W	XXXXXXXXB
007A71H	007C71H	007E71H				
007A72H	007C72H	007E72H	DLC Register 9	DLCR9	R/W	XXXXXXXXB
007A73H	007C73H	007E73H				
007A74H	007C74H	007E74H	DLC Register 10	DLCR10	R/W	XXXXXXXXB
007A75H	007C75H	007E75H				
007A76H	007C76H	007E76H	DLC Register 11	DLCR11	R/W	XXXXXXXXB
007A77H	007C77H	007E77H				
007A78H	007C78H	007E78H	DLC Register 12	DLCR12	R/W	XXXXXXXXB
007A79H	007C79H	007E79H				
007A7AH	007C7AH	007E7AH	DLC Register 13	DLCR13	R/W	XXXXXXXXB
007A7BH	007C7BH	007E7BH				
007A7CH	007C7CH	007E7CH	DLC Register 14	DLCR14	R/W	XXXXXXXXB
007A7DH	007C7DH	007E7DH				
007A7EH	007C7EH	007E7EH	DLC Register 15	DLCR15	R/W	XXXXXXXXB
007A7FH	007C7FH	007E7FH				

• **List of Message Buffers (DLC Registers and Data Registers) (2)**

Address			Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2				
007A80H to 007A87H	007C80H to 007C87H	007E80H to 007E87H	Data Register 0 (8 bytes)	DTR0	R/W	XXXXXXXXB to XXXXXXXXB
007A88H to 007A8FH	007C88H to 007C8FH	007E88H to 007E8FH	Data Register 1 (8 bytes)	DTR1	R/W	XXXXXXXXB to XXXXXXXXB
007A90H to 007A97H	007C90H to 007C97H	007E90H to 007E97H	Data Register 2 (8 bytes)	DTR2	R/W	XXXXXXXXB to XXXXXXXXB
007A98H to 007A9FH	007C98H to 007C9FH	007E98H to 007E9FH	Data Register 3 (8 bytes)	DTR3	R/W	XXXXXXXXB to XXXXXXXXB
007AA0H to 007AA7H	007CA0H to 007CA7H	007EA0H to 007EA7H	Data Register 4 (8 bytes)	DTR4	R/W	XXXXXXXXB to XXXXXXXXB
007AA8H to 007AAFH	007CA8H to 007CAFH	007EA8H to 007EAFH	Data Register 5 (8 bytes)	DTR5	R/W	XXXXXXXXB to XXXXXXXXB
007AB0H to 007AB7H	007CB0H to 007CB7H	007EB0H to 007EB7H	Data Register 6 (8 bytes)	DTR6	R/W	XXXXXXXXB to XXXXXXXXB
007AB8H to 007ABFH	007CB8H to 007CBFH	007EB8H to 007EBFH	Data Register 7 (8 bytes)	DTR7	R/W	XXXXXXXXB to XXXXXXXXB
007AC0H to 007AC7H	007CC0H to 007CC7H	007EC0H to 007EC7H	Data Register 8 (8 bytes)	DTR8	R/W	XXXXXXXXB to XXXXXXXXB
007AC8H to 007ACFH	007CC8H to 007CCFH	007EC8H to 007ECFH	Data Register 9 (8 bytes)	DTR9	R/W	XXXXXXXXB to XXXXXXXXB
007AD0H to 007AD7H	007CD0H to 007CD7H	007ED0H to 007ED7H	Data Register 10 (8 bytes)	DTR10	R/W	XXXXXXXXB to XXXXXXXXB
007AD8H to 007ADFH	007CD8H to 007CDFH	007ED8H to 007EDFH	Data Register 11 (8 bytes)	DTR11	R/W	XXXXXXXXB to XXXXXXXXB
007AE0H to 007AE7H	007CE0H to 007CE7H	007EE0H to 007EE7H	Data Register 12 (8 bytes)	DTR12	R/W	XXXXXXXXB to XXXXXXXXB
007AE8H to 007AEFH	007CE8H to 007CEFH	007EE8H to 007EEFH	Data Register 13 (8 bytes)	DTR13	R/W	XXXXXXXXB to XXXXXXXXB

• **List of Message Buffers (DLC Registers and Data Registers) (3)**

Address			Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2				
007AF0H to 007AF7H	007CF0H to 007CF7H	007EF0H to 007EF7H	Data Register 14 (8 bytes)	DTR14	R/W	XXXXXXXXB to XXXXXXXXB
007AF8H to 007AFFH	007CF8H to 007CFFH	007EF8H to 007EFFH	Data Register 15 (8 bytes)	DTR15	R/W	XXXXXXXXB to XXXXXXXXB

■ INTERRUPT FACTORS, INTERRUPT VECTORS, INTERRUPT CONTROL REGISTER

Interrupt cause	EI²OS Support	DMA channel number	Interrupt vector		Interrupt control register	
			Number	Address	Number	Address
Reset	N	—	#08	FFFFDC$_H$	—	—
INT9 instruction	N	—	#09	FFFFD8$_H$	—	—
Exception	N	—	#10	FFFFD4$_H$	—	—
CAN0 RX	N	—	#11	FFFFD0$_H$	ICR00	0000B0$_H$
CAN0 TX/NS	N	—	#12	FFFFCC$_H$		
CAN1 RX/Input Capture 6	Y1	—	#13	FFFFC8$_H$	ICR01	0000B1$_H$
CAN1 TX/NS/Input Capture 7	Y1	—	#14	FFFFC4$_H$		
CAN2 RX / I²C0	N	—	#15	FFFFC0$_H$	ICR02	0000B2$_H$
CAN2 TX / NS / Clock Calibration Unit	N	—	#16	FFFFBC$_H$		
16-bit Reload Timer 0	Y1	0	#17	FFFFB8$_H$	ICR03	0000B3$_H$
16-bit Reload Timer 1	Y1	1	#18	FFFFB4$_H$		
16-bit Reload Timer 2	Y1	2	#19	FFFFB0$_H$	ICR04	0000B4$_H$
16-bit Reload Timer 3	Y1	—	#20	FFFFAC$_H$		
PPG0 / PPG1 / PPG4 / PPG5	N	—	#21	FFFFA8$_H$	ICR05	0000B5$_H$
PPG2 / PPG3 / PPG6 / PPG7	N	—	#22	FFFFA4$_H$		
PPG8 / PPG9 / PPGC / PPGD	N	—	#23	FFFFA0$_H$	ICR06	0000B6$_H$
PPGA / PPGB / PPGE / PPGF	N	—	#24	FFFF9C$_H$		
Time Base Timer	N	—	#25	FFFF98$_H$	ICR07	0000B7$_H$
External Interrupt 0 to 3, 8 to 11	Y1	3	#26	FFFF94$_H$		
Watch Timer	N	—	#27	FFFF90$_H$	ICR08	0000B8$_H$
External Interrupt 4 to 7, 12 to 15	Y1	4	#28	FFFF8C$_H$		
A/D Converter	Y1	5	#29	FFFF88$_H$	ICR09	0000B9$_H$
I/O Timer 0/1	N	—	#30	FFFF84$_H$		
Input Capture 4/5 / I²C1	Y1	6	#31	FFFF80$_H$	ICR10	0000BA$_H$
Output Compare 0/1/4/5	Y1	7	#32	FFFF7C$_H$		
Input Capture 0 to 3	Y1	8	#33	FFFF78$_H$	ICR11	0000BB$_H$
Output Compare 2/3/6/7	Y1	9	#34	FFFF74$_H$		
UART0 RX	Y2	10	#35	FFFF70$_H$	ICR12	0000BC$_H$
UART0 TX	Y1	11	#36	FFFF6C$_H$		
UART1 RX / UART3 RX / UART5 RX	Y2	12	#37	FFFF68$_H$	ICR13	0000BD$_H$
UART1 TX / UART3 TX / UART5 TX	Y1	13	#38	FFFF64$_H$		

(Continued)

(Continued)

Interrupt cause	EI²OS Support	DMA channel number	Interrupt vector		Interrupt control register	
			Number	Address	Number	Address
UART2 RX / UART4 RX / UART6 RX	Y2	14	#39	FFFF60H	ICR14	0000BEH
UART2 TX / UART4 TX / UART6 TX	Y1	15	#40	FFFF5CH		
Flash Memory	N	—	#41	FFFF58H	ICR15	0000BFH
Delayed Interrupt	N	—	#42	FFFF54H		

Y1 : Usable
Y2 : Usable, with EI²OS stop function
N : Unusable

Notes :
- The peripheral resources sharing the ICR register have the same interrupt level.
- When two peripheral resources share the ICR register, only one can use Extended Intelligent I/O Service at a time.
- When either of the two peripheral resources sharing the ICR register specifies Extended Intelligent I/O Service, the other one cannot use interrupts.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	$V_{CC} = AV_{CC}$*2
	AVRH, AVRL	V_{SS} – 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq$ AVRH, $AV_{CC} \geq$ AVRL, AVRH ≥ AVRL
Input voltage*1	V_I	V_{SS} – 0.3	V_{SS} + 6.0	V	*3
Output voltage*1	V_O	V_{SS} – 0.3	V_{SS} + 6.0	V	*3
Maximum Clamp Current	I_{CLAMP}	–4.0	+4.0	mA	*5
Total Maximum Clamp Current	$\Sigma\lvert I_{CLAMP}\rvert$	—	40	mA	*5
“L” level maximum output current	I_{OL}	—	15	mA	*4
“L” level average output current	I_{OLAV}	—	4	mA	*4
“L” level maximum overall output current	ΣI_{OL}	—	100	mA	*4
“L” level average overall output current	ΣI_{OLAV}	—	50	mA	*4
“H” level maximum output current	I_{OH}	—	–15	mA	*4
“H” level average output current	I_{OHAV}	—	–4	mA	*4
“H” level maximum overall output current	ΣI_{OH}	—	–100	mA	*4
“H” level average overall output current	ΣI_{OHAV}	—	–50	mA	*4
Power consumption	P_D	—	430	mW	
Operating temperature	T_A	–40	+105	°C	
		–40	+125	°C	*6
Storage temperature	T_{STG}	–55	+150	°C	

*1: This parameter is based on $V_{SS} = AV_{SS} = 0$ V

*2: Set AV_{CC} and V_{CC} to the same voltage. Make sure that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} when the power is switched on.

*3: V_I and V_O should not exceed V_{CC} + 0.3 V. V_I should not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

*4: Applicable to pins: P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0, PA1

(Continued)

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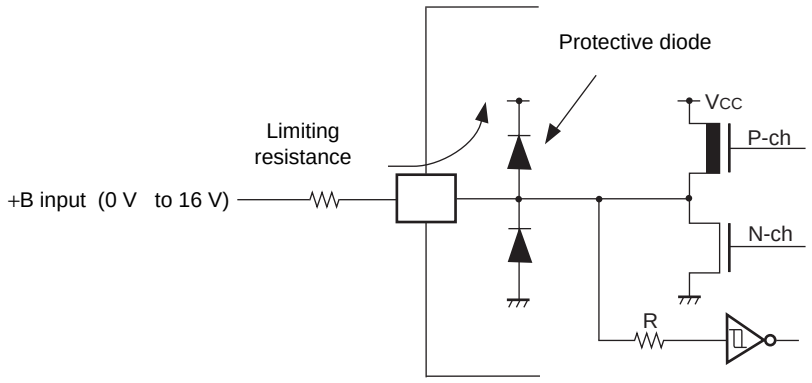
*5: • Applicable to pins: P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P55, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0 to PA1
- Use within recommended operating conditions.
- Use with DC voltage (current)
- The +B signal should always be applied by using a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied, the input current to the microcontroller pin does not exceed the rated value, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Sample recommended circuits:

• Input/output equivalent circuits



*6 : If used exceeding T_A = + 105 °C, please consult with us due to the restricted reliability.
It is ensured to write/erase data to the Flash memory between T_A = − 40 °C and + 105 °C.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

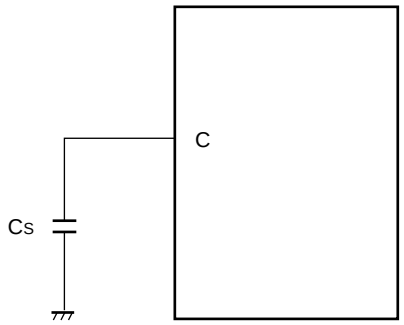
2. Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Power supply voltage	V_{CC}, AV_{CC}	—	3.0	5.0	5.5	V	Under normal operation
			4.5	5.0	5.5	V	When External bus is used.
			3.0	—	5.5	V	Maintains RAM data in stop mode
Smoothing capacitor	C_S	—	0.1	—	1.0	µF	Use a ceramic capacitor or capacitor of better AC characteristics. Capacitor at the V_{CC} should be greater than this capacitor.
Operating temperature	T_A	—	–40	—	+105	°C	MB90F952JDS, MB90F952MDS
			–40	—	+125		*

* : If used exceeding T_A = + 105 °C, please consult with us due to the restricted reliability.
It is ensured to write/erase data to the Flash memory between T_A = – 40 °C and + 105 °C.

C Pin Connection Diagram



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

3. DC Characteristics

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input H voltage (At V_{CC} = 5 V ± 10%)	V_{IHS}	—	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Port inputs if CMOS hysteresis input levels are selected
	V_{IHA}	—	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Port inputs if Automotive input levels are selected
	V_{IHT}	—	—	2.0	—	V_{CC} + 0.3	V	Port inputs if TTL input levels are selected
	V_{IHS}	P12,P15, P44 to P47, P50,P82, P85,P90, P94	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	Port inputs if CMOS hysteresis input levels are selected
	V_{IHR}	$\overline{RST}$	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	$\overline{RST}$ input pin (CMOS hysteresis)
	V_{IHM}	MD0 to MD2	—	V_{CC} – 0.3	—	V_{CC} + 0.3	V	MD input pins
Input L voltage (At V_{CC} = 5 V ± 10%)	V_{ILS}	—	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	Port inputs if CMOS hysteresis input levels are selected
	V_{ILA}	—	—	V_{SS} – 0.3	—	0.5 V_{CC}	V	Port inputs if Automotive input levels are selected
	V_{ILT}	—	—	V_{SS} – 0.3	—	0.8	V	Port inputs if TTL input levels are selected
	V_{ILS}	P12,P15, P44 to P47, P50,P82, P85,P90, P94	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	Port inputs if CMOS hysteresis input levels are selected
	V_{ILR}	$\overline{RST}$	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	$\overline{RST}$ input pin (CMOS hysteresis)
	V_{ILM}	MD0 to MD2	—	V_{SS} – 0.3	—	V_{SS} + 0.3	V	MD input pins
Output H voltage	V_{OH}	Normal outputs	V_{CC} = 4.5 V, I_{OH} = –4.0 mA	V_{CC} – 0.5	—	—	V	
Output H voltage	V_{OHI}	I^2C outputs	V_{CC} = 4.5 V, I_{OH} = –3.0 mA	V_{CC} – 0.5	—	—	V	
Output L voltage	V_{OL}	Normal outputs	V_{CC} = 4.5 V, I_{OL} = 4.0 mA	—	—	0.4	V	
Output L voltage	V_{OLI}	I^2C outputs	V_{CC} = 4.5 V, I_{OL} = 3.0 mA	—	—	0.4	V	

(Continued)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input leak current	I_{IL}	—	V_{CC} = 5.5 V, $V_{SS} < V_I < V_{CC}$	−1	—	+1	µA	
Pull-up resistance	R_{UP}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, $\overline{RST}$	—	25	50	100	kΩ	
Pull-down resistance	R_{DOWN}	MD2	—	25	50	100	kΩ	Except Flash memory devices
Power supply current*	I_{CC}	V_{CC}	V_{CC} = 5.0 V, Internal frequency : 32 MHz, At normal operation.	—	40	50	mA	
			V_{CC} = 5.0 V, Internal frequency : 32 MHz, At writing Flash memory/erasing.	—	50	65	mA	MB90F952JDS, MB90F952MDS
	I_{CCS}		V_{CC} = 5.0 V, Internal frequency : 32 MHz, In Sleep mode.	—	13	23	mA	
	I_{CTS}		V_{CC} = 5.0 V, Internal frequency : 2 MHz, In Main Timer mode	—	0.4	1.0	mA	MB90F952JDS
				—	0.3	0.9		MB90F952MDS
	$I_{CTSPLL6}$		V_{CC} = 5.0 V, Internal frequency : 32 MHz, In PLL Timer mode, external frequency = 4 MHz	—	4	7	mA	
	I_{CCL}		V_{CC} = 5.0 V Internal frequency : 12.5 kHz, In CR sub operation T_A = +25°C	—	170	400	µA	MB90F952JDS
	I_{CCLS}		V_{CC} = 5.0 V Internal frequency : 12.5 kHz, In CR sub sleep T_A = +25°C	—	130	250	µA	MB90F952JDS
	I_{CCT}		V_{CC} = 5.0 V Internal frequency : 12.5 kHz, In CR watch mode T_A = +25°C	—	130	250	µA	MB90F952JDS
	I_{CCH}		V_{CC} = 5.0 V, In Stop mode, T_A = +25°C	—	70	170	µA	MB90F952JDS
				—	25	100		MB90F952MDS

(Continued)

(Continued)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input capacitance	C_{IN}	Other than C, AV_{CC}, AV_{SS}, AVRH, AVRL, V_{CC}, V_{SS}	—	—	5	15	pF	

* : The power supply current is measured with an external clock.

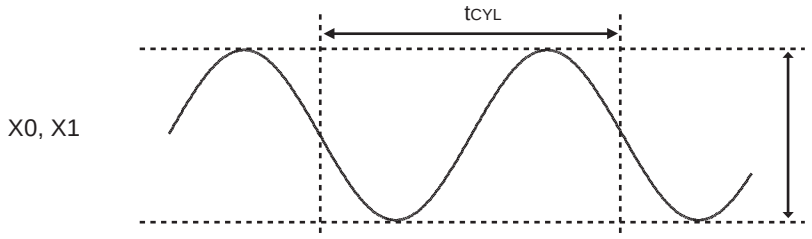
4. AC Characteristics

(1) Clock Timing

(T_A = –40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 32 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	f_C	X0, X1	—	3	—	16	MHz	1/2 multiplied (PLL stopped) When using an oscillation circuit
				4		16		PLL multiplied by 1 When using an oscillation circuit
				4		16		PLL multiplied by 2 When using an oscillation circuit
				4		10		PLL multiplied by 3 When using an oscillation circuit
				4		8		PLL multiplied by 4 When using an oscillation circuit
				4		5		PLL multiplied by 6 When using an oscillation circuit
				4		4		PLL multiplied by 8 When using an oscillation circuit
Clock cycle time	t_{CYL}	X0, X1	—	62.5	—	333	ns	When using an oscillation circuit
Internal operating clock frequency (machine clock)	f_{CP}	—	—	1.5	—	32	MHz	When using main clock
	f_{CPL}	—	—	10.625	12.5	14.375	kHz	When using CR clock
Internal operating clock cycle time (machine clock)	t_{CP}	—	—	31.25	—	666	ns	When using main clock
	t_{CPL}	—	—	69.565	80	94.118	µs	When using CR clock
Internal CR oscillation frequency	f_{CCR}	—	—	85	100	115	kHz	When trimming with the clock calibration unit

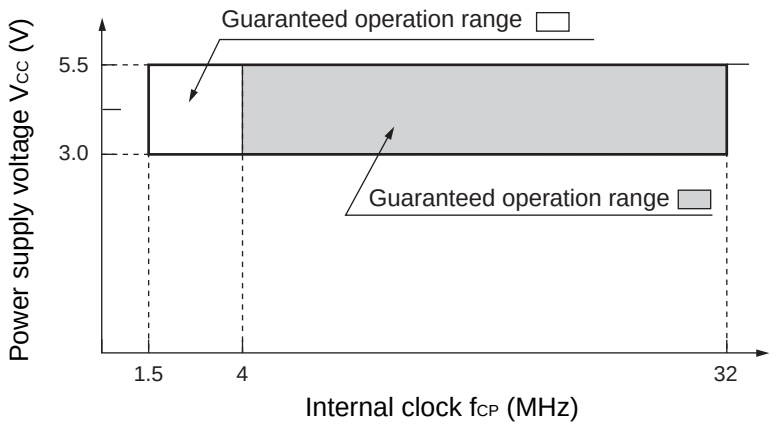
• When oscillation circuit is used



Amplitude:
It varies depending on the external resistance, power rating and the different kind of device.
Reference values: 1 V to 2.5 V

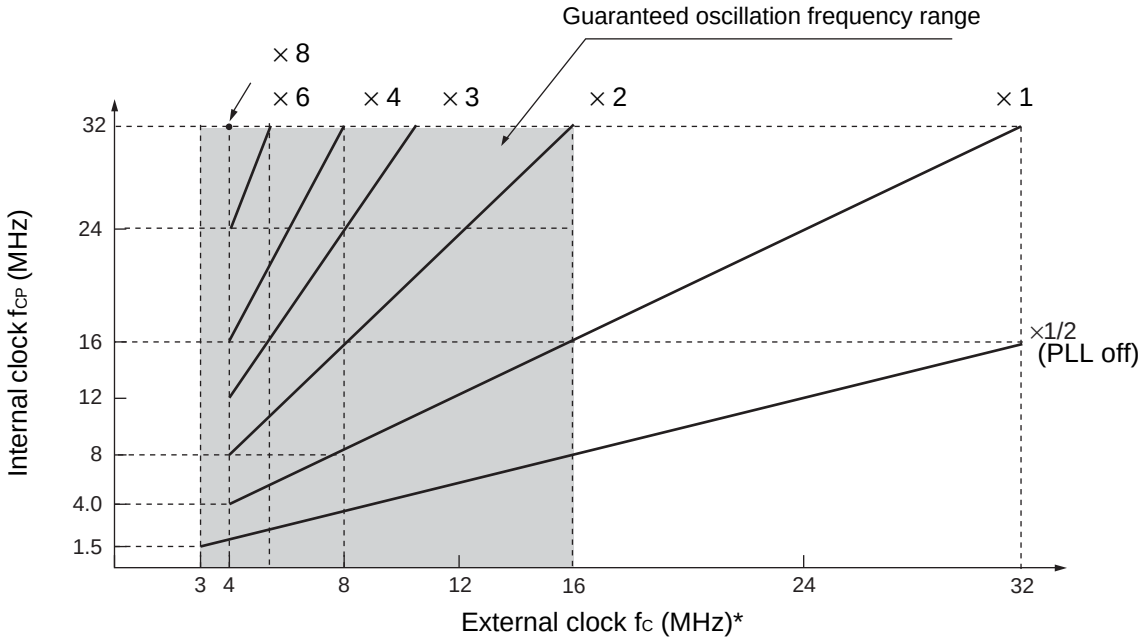
Note: The amplitude of MB90V950AJAS and MB90V950AMAS are the same as V_{CC}.

• Guaranteed PLL operation range



Note: When the power supply voltage is lower than the setting voltage of low voltage detection, MB90F952JDS are reset.

Internal clock f_{CP} — External clock f_C



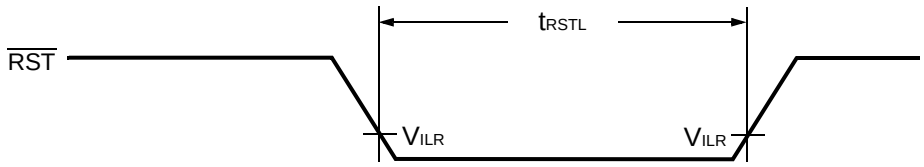
* : When using a crystal oscillator or ceramic oscillator, the maximum oscillation clock frequency is 16 MHz

(2) Reset Standby Input

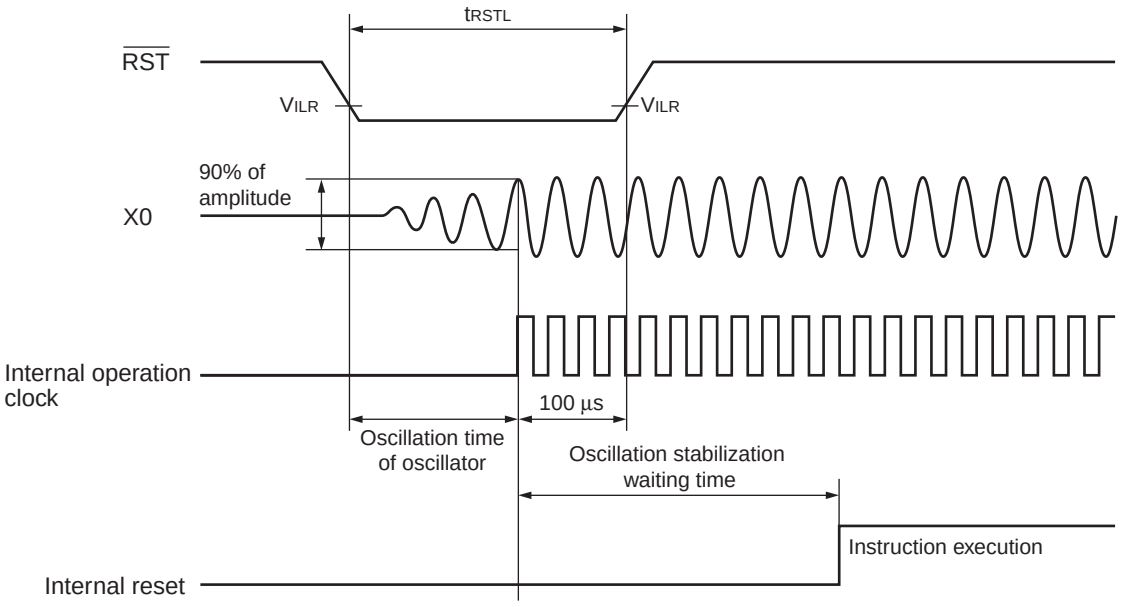
Parameter	Symbol	Pin name	Condi-tions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	—	500	—	ns	Under normal operation
				Oscillation time of oscillator* + 100 µs	—	µs	In Stop mode, Sub Clock mode, Sub Sleep mode and Watch mode
				100	—	µs	In Time Base Timer mode

* : The oscillation time of the oscillator is the time it takes for the amplitude of the oscillations to reach 90%. For crystal oscillators, this time is between several ms and several tens of ms, for ceramic oscillators the time is between several hundred µs and several ms, and for an external clock, the time is 0 ms.

• **Under normal operation:**

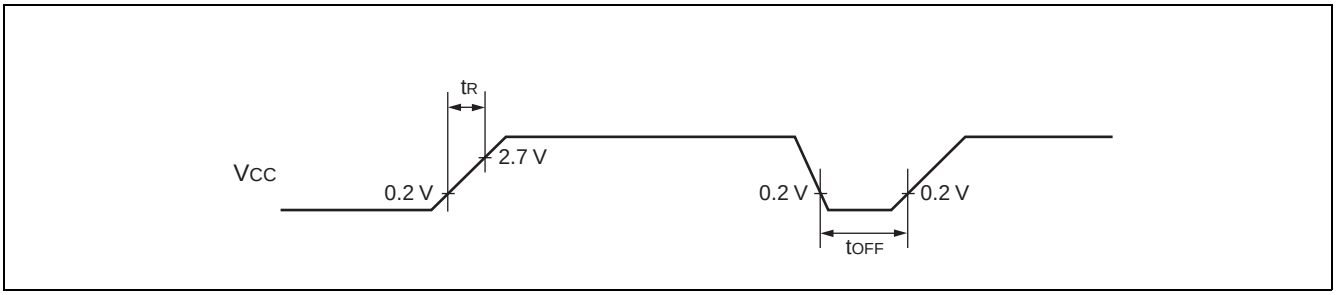


• **In Stop mode, Sub Clock mode, Sub Sleep mode, Watch mode:**

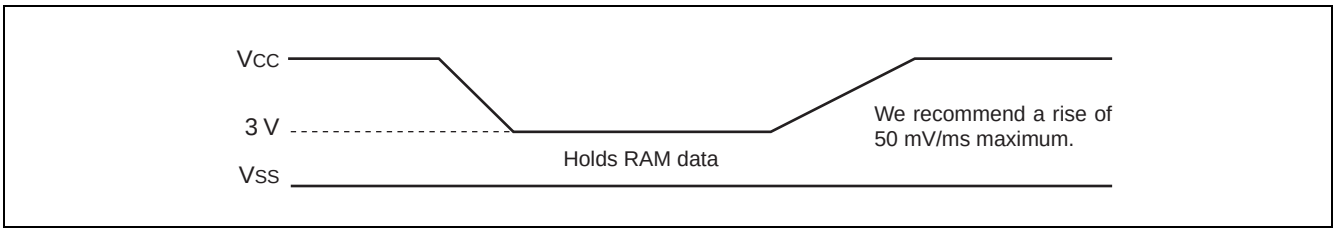


(3) Power On Reset

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Power on rise time	t_R	V_{CC}	—	0.05	30	ms	
Power off time	t_{OFF}	V_{CC}		1	—	ms	Due to repetitive operation



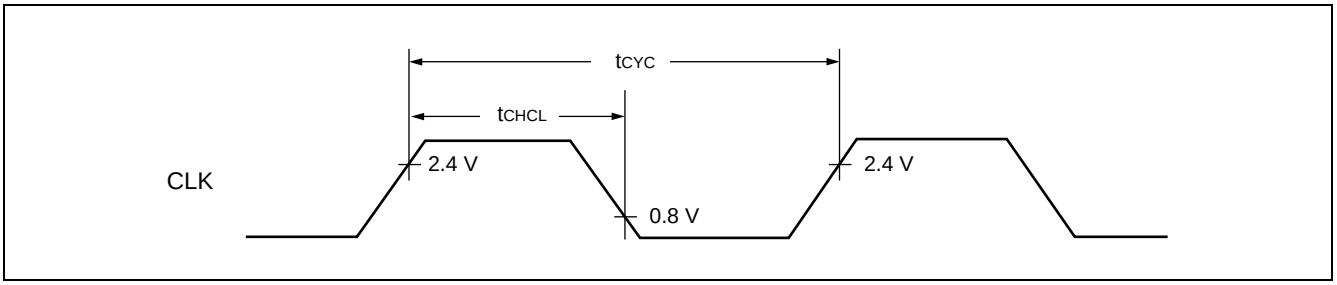
Note: If you change the power supply voltage too rapidly, a power on reset may occur. We recommend that you startup smoothly by restraining voltages when changing the power supply voltage during operation, as shown in the figure below. Perform while not using the PLL clock. However, if voltage drops are within 1 V/s, you can operate while using the PLL clock.



(4) Clock Output Timing

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	CLK	—	tcp*	—	ns	
CLK ↑ → CLK ↓	t_{CHCL}	CLK	—	tcp* / 2 – 15	tcp* / 2 + 15	ns	f_{CP} = 25 MHz
				tcp* / 2 – 20	tcp* / 2 + 20	ns	f_{CP} = 16 MHz

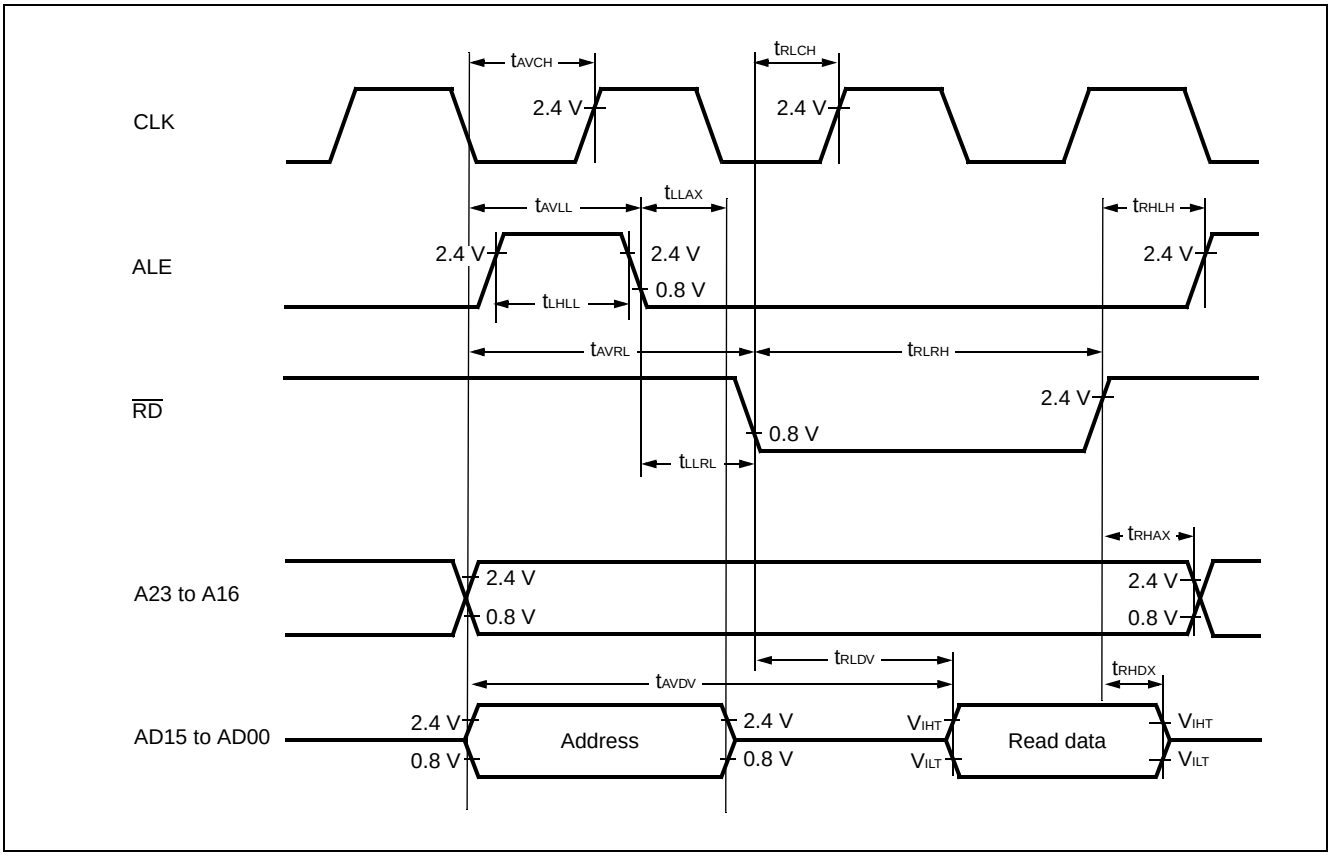
* : tcp is the Internal clock cycle time. Refer to “ (1) Clock Timing”.



(5) Bus Timing (Read)

Parameter	Symbol	Pin name	Condi-tions	Value		Unit	Remarks
				Min	Max		
ALE pulse width	t_{LHLL}	ALE	—	tcp*/ 2 – 15	—	ns	16MHz < fcp ≤ 25 MHz
				tcp*/ 2 – 20	—	ns	8 MHz < fcp ≤ 16 MHz
				tcp*/ 2 – 35	—	ns	fcp ≤ 8 MHz
Valid address → ALE ↓ time	t_{AVLL}	Address, ALE	—	tcp*/ 2 – 17	—	ns	
				tcp*/ 2 – 40	—	ns	fcp ≤ 8 MHz
ALE ↓ → Address valid time	t_{LLAX}	ALE , Address	—	tcp*/ 2 – 15	—	ns	
Valid address → $\overline{RD}$ ↓ time	t_{AVRL}	$\overline{RD}$, Address	—	tcp* – 25	—	ns	
Valid address → Valid data input	t_{AVDV}	Address/ Data	—	—	tcp* / 2 – 55	ns	
				—	tcp* / 2 – 80	ns	fcp ≤ 8 MHz
$\overline{RD}$ pulse width	t_{RLRH}	$\overline{RD}$	—	3 tcp* / 2 – 25	—	ns	16 MHz < fcp ≤ 25 MHz
				3 tcp* / 2 – 20	—	ns	8 MHz < fcp ≤ 16 MHz
$\overline{RD}$ ↓ → Valid data input	t_{RLDV}	$\overline{RD}$, Data	—		3 tcp* / 2 – 55	ns	
					3 tcp* / 2 – 80	ns	fcp ≤ 8 MHz
$\overline{RD}$ ↑ → Data hold time	t_{RHDX}	$\overline{RD}$, Data	—	0	—	ns	
$\overline{RD}$ ↓ → ALE ↑ time	t_{RHLH}	$\overline{RD}$, ALE	—	tcp* / 2 – 15	—	ns	
$\overline{RD}$ ↑ → Address valid time	t_{RHAX}	Address, $\overline{RD}$	—	tcp* / 2 – 10	—	ns	
Valid address → CLK ↑ time	t_{AVCH}	Address, CLK	—	tcp* / 2 – 17	—	ns	
$\overline{RD}$ ↓ → CLK ↑ time	t_{RLCH}	$\overline{RD}$,CLK	—	tcp* / 2 – 17	—	ns	
ALE ↓ → $\overline{RD}$ ↓ time	t_{LLRL}	$\overline{RD}$,ALE	—	tcp* / 2 – 15	—	ns	

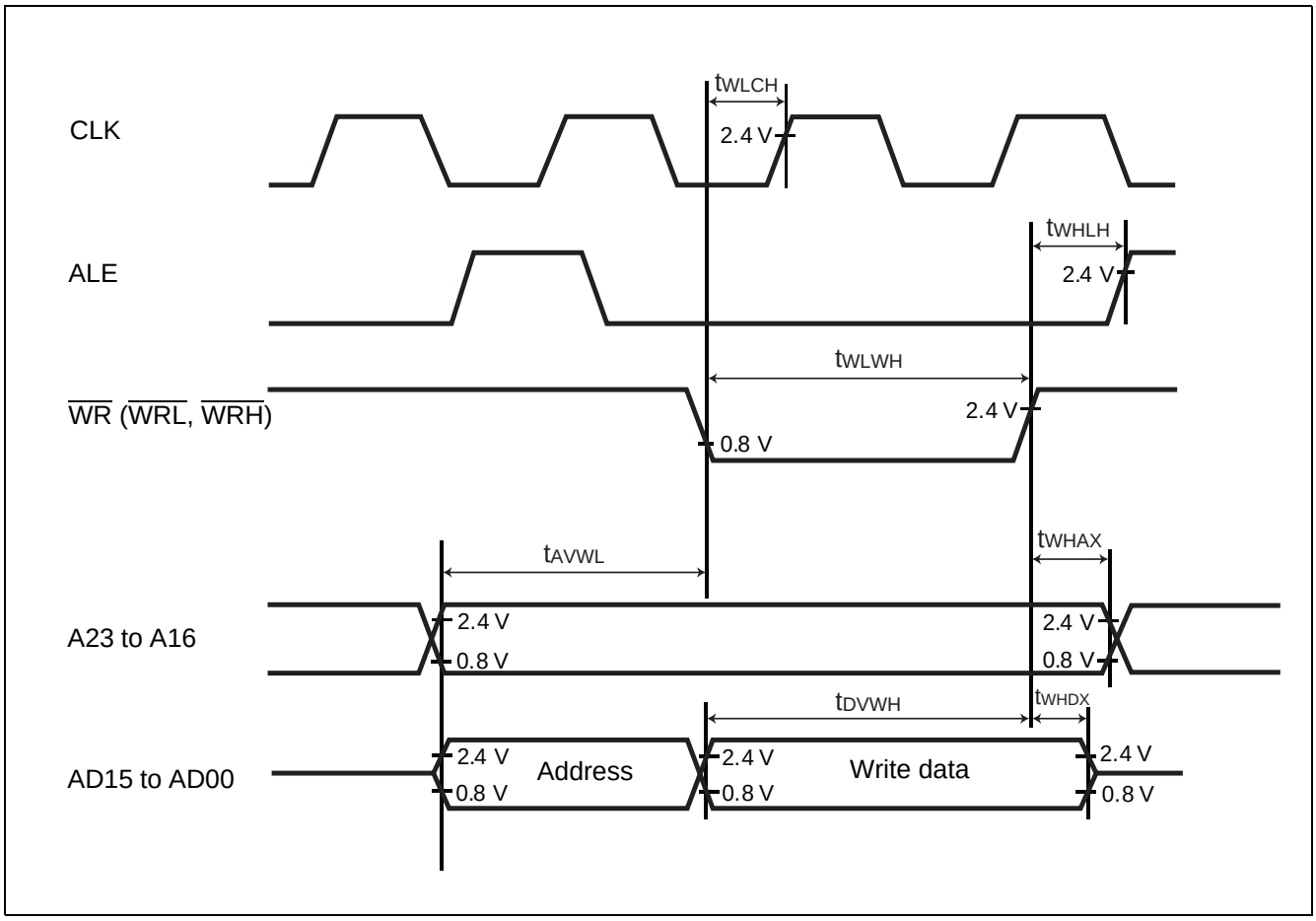
* : tcp is the Internal cycle time. Refer to “(1) Clock Timing”.


CLK
ALE
RD
A23 to A16
AD15 to AD00
tAVCH
tRLCH
2.4 V
tAVLL
tLLAX
tRHLH
tLHLL
0.8 V
tAVRL
tRLRH
tLLRL
tRHAX
tRLDV
tRHDX
tAVDV
Address
Read data
VIHT
VILT

(6) Bus Timing (Write)

Parameter	Symbol	Pin name	Condi-tions	Value		Unit	Remarks
				Min	Max		
Valid address → $\overline{WR}$ ↓ time	t_{AVWL}	Address, $\overline{WR}$	—	tcp* – 15	—	ns	
$\overline{WR}$ pulse width	t_{WLWH}	$\overline{WRL}$, $\overline{WRH}$	—	3 tcp* / 2 – 25	—	ns	16 MHz < fcp ≤ 25 MHz
				3 tcp* / 2 – 20	—	ns	8 MHz < fcp ≤ 16 MHz
Valid data output → $\overline{WR}$ ↑ time	t_{DVWH}	Data, $\overline{WR}$	—	3 tcp* / 2 – 15	—	ns	
$\overline{WR}$ ↑ → Data hold time	t_{WHDX}	$\overline{WR}$, Data	—	10	—	ns	16 MHz < fcp ≤ 25 MHz
				20	—	ns	8 MHz < fcp ≤ 16 MHz
				30	—	ns	fcp ≤ 8 MHz
$\overline{WR}$ ↑ → A ddress valid time	t_{WHAX}	$\overline{WR}$, Address	—	tcp* / 2 – 10	—	ns	
$\overline{WR}$ ↑ → ALE ↑ time	t_{WHLH}	$\overline{WR}$, ALE	—	tcp* / 2 – 15	—	ns	
$\overline{WR}$ ↓ → CLK ↑ time	t_{WLCH}	$\overline{WR}$, CLK	—	tcp* / 2 – 17	—	ns	

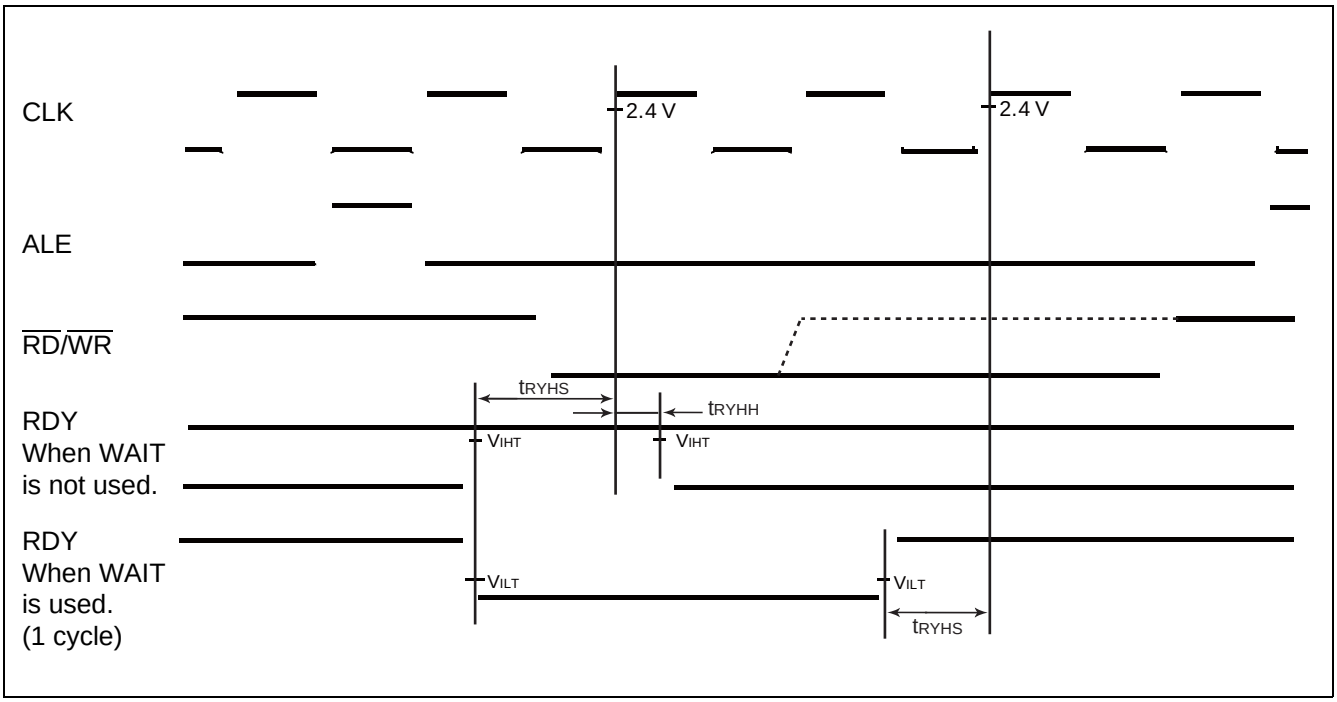
*: tcp is the Internal operating clock cycle time. Refer to “(1) Clock Timing”.


CLK
ALE
WR (WRL, WRH)
A23 to A16
AD15 to AD00
tWLCH
2.4 V
tWHLH
2.4 V
tWLWH
2.4 V
0.8 V
tAVWL
tWHAX
2.4 V
0.8 V
2.4 V
0.8 V
tDVWH
tWHDX
2.4 V
0.8 V
Address
2.4 V
0.8 V
Write data
2.4 V
0.8 V

(7) Ready Input Timing

Parameter	Sym-bol	Pin name	Test Condition	Rated Value		Unit	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY	—	35	—	ns	
				70	—	ns	f_{CP} = 8 MHz
RDY hold time	t_{RYHH}	RDY		0	—	ns	

Note : If the RDY setup time is insufficient, use the auto-ready function.

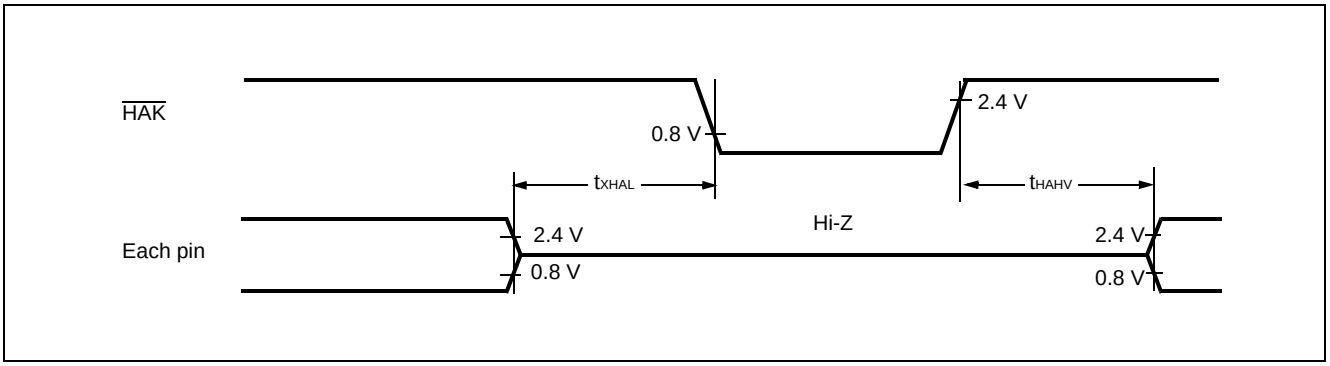


(8) Hold Timing

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Pin floating → $\overline{HAK}$ ↓ time	t_{XHAL}	$\overline{HAK}$	—	30	t_{CP}*	ns
$\overline{HAK}$ ↓ → time → Pin valid time	t_{HAHV}	$\overline{HAK}$		t_{CP}*	2 t_{CP}*	ns

* : tcp is the Internal operating clock cycle time. Refer to “(1) Clock Timing”.

Note : There is more than 1 cycle from when HRQ reads in until the $\overline{HAK}$ is changed.

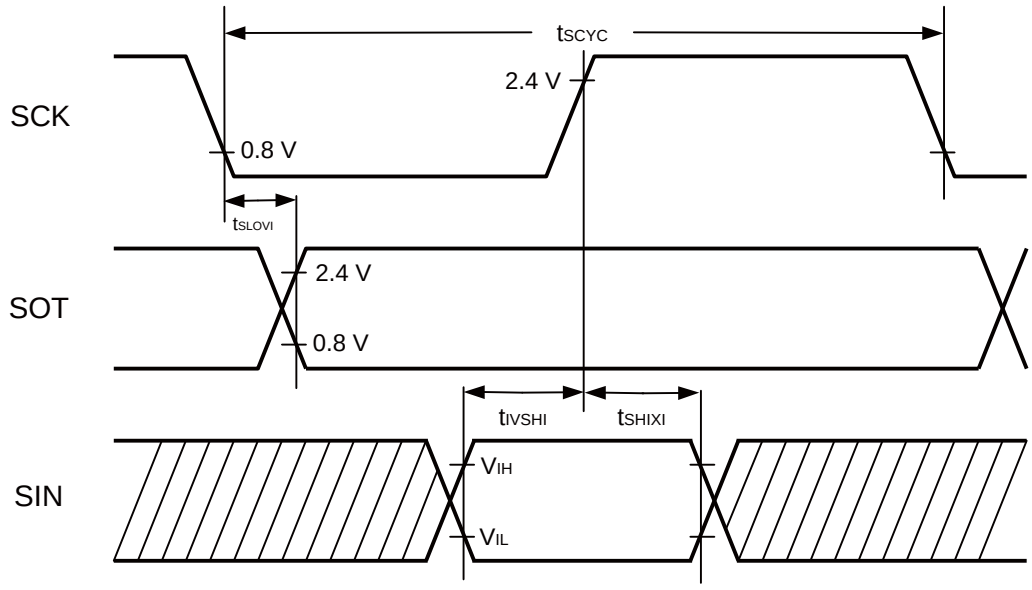


(9) UART

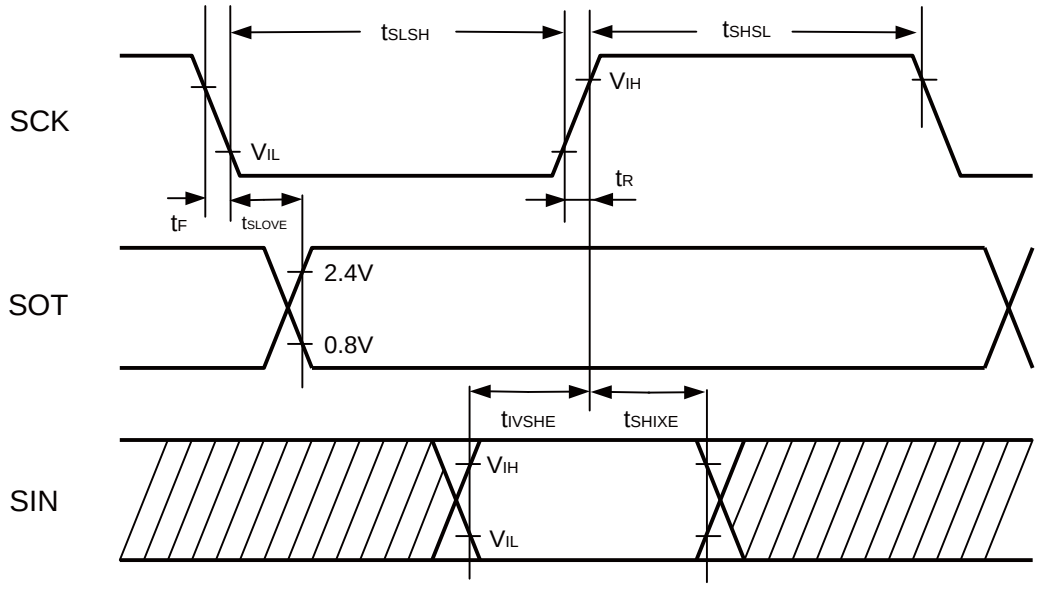
ESCR : SCES = 0, ECCR : SCDE = 0

Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
Serial clock cycle time	t_{SCYC}	Internal shift clock operation C_L = 80 pF + 1 TTL.	5 tcp*	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}		− 50	+ 50	ns
SIN → SCK ↑ setup time	t_{IVSHI}		tcp* + 80	—	ns
SCK ↑ → SIN hold time	t_{SHIXI}		0	—	ns
Serial clock “H” pulse width	t_{SLSH}	External shift clock operation C_L = 80 pF + 1 TTL.	3 tcp* − t_R	—	ns
Serial clock “L” pulse width	t_{SHSL}		tcp* + 10	—	ns
SCK ↓ → SOT delay time	t_{SLOVE}		—	2 tcp* + 60	ns
SIN → SCK ↑ setup time	t_{IVSHE}		30	—	ns
SCK ↑ → SIN hold time	t_{SHIXE}		tcp* + 30	—	ns
SCK fall time	t_F		—	10	ns
SCK rise time	t_R		—	10	ns

*: tcp indicates the machine clock time



Internal Clock Shift Operation

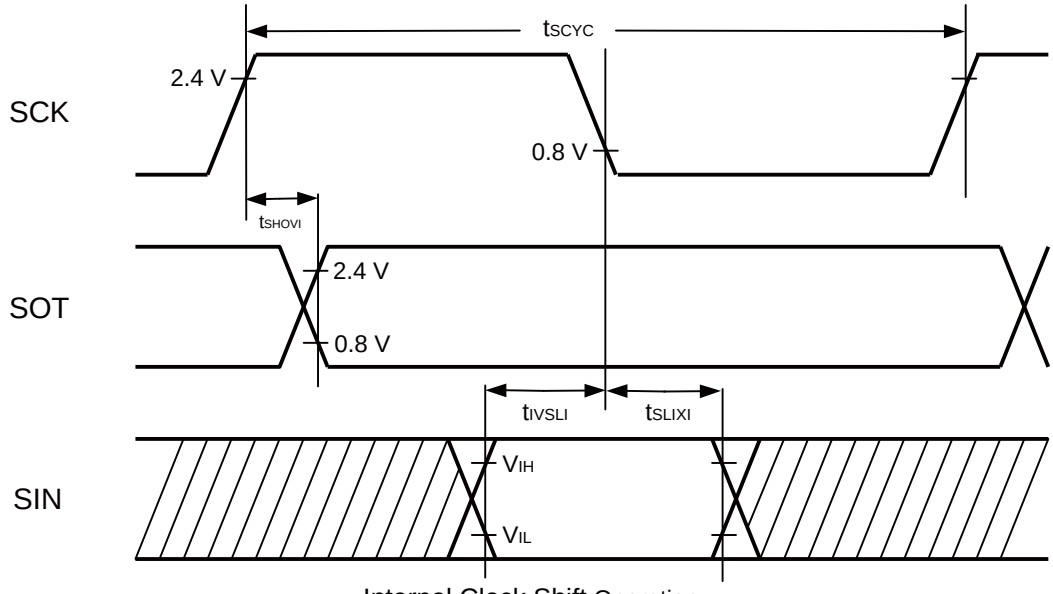


External Clock Shift Operation

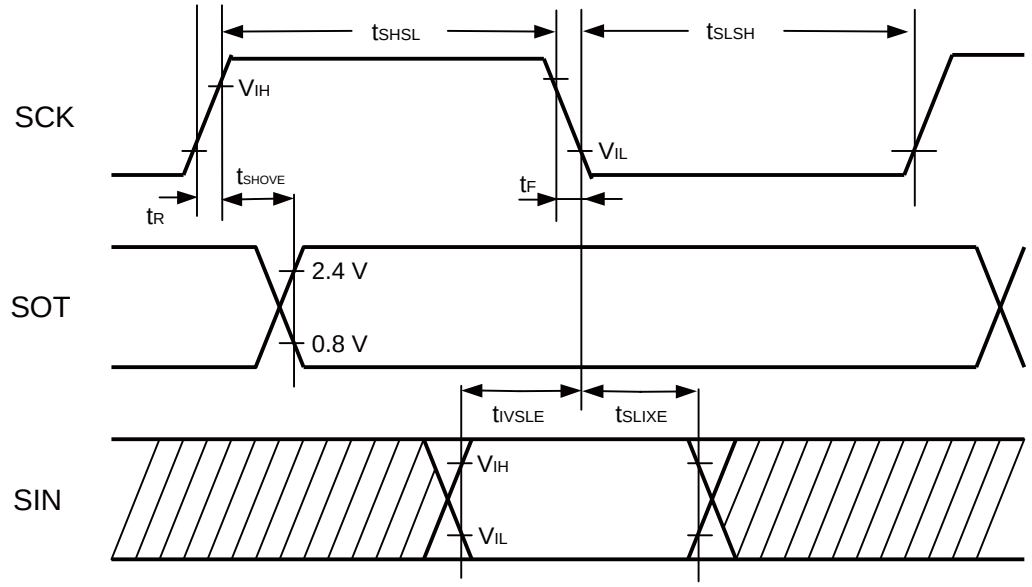
ESCR : SCES = 1, ECCR : SCDE = 0

Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
Serial clock cycle time	t_{SCYC}	Internal shift clock operation C_L = 80 pF + 1 TTL.	5 tcp*	—	ns
SCK ↑ → SOT delay time	t_{SHOVI}		− 50	+ 50	ns
SIN → SCK ↓ setup time	t_{IVSLI}		tcp* + 80	—	ns
SCK ↓ → SIN hold time	t_{SLIXI}		0	—	ns
Serial clock “H” pulse width	t_{SHSL}	External shift clock operation C_L = 80 pF + 1 TTL.	3 tcp* − t_R	—	ns
Serial clock “L” pulse width	t_{SLSH}		tcp* + 10	—	ns
SCK ↑ → SOT delay time	t_{SHOVE}		—	2 tcp* + 60	ns
SIN → SCK ↓ setup time	t_{IVSLE}		30	—	ns
SCK ↓ → SIN hold time	t_{SLIXE}		tcp* + 30	—	ns
SCK fall time	t_F		—	10	ns
SCK rise time	t_R		—	10	ns

*: tcp indicates the machine clock time



Internal Clock Shift Operation

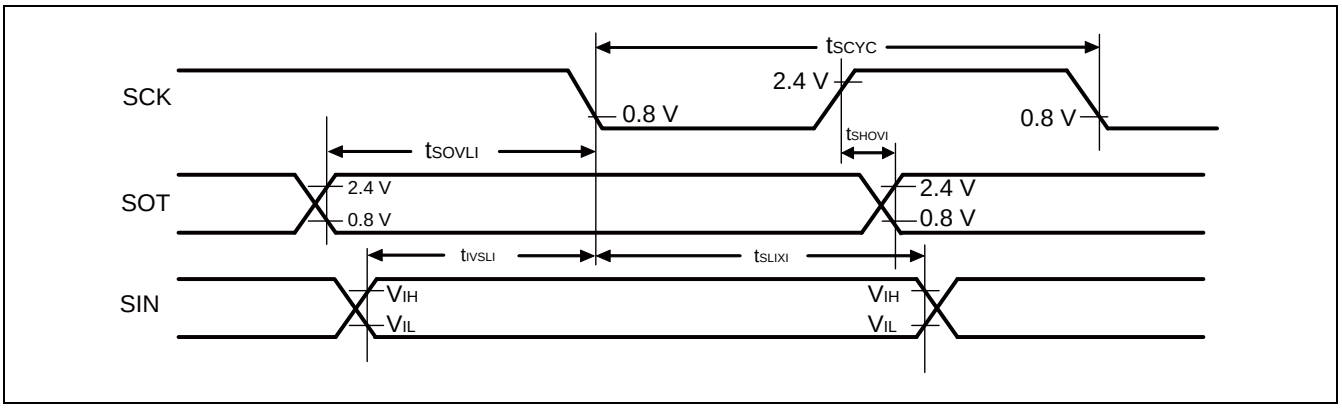


External Clock Shift Operation

ESCR : SCES = 0, ECCR : SCDE = 1

Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
Serial clock cycle time	t_{SCYC}	Internal shift clock operation C_L = 80 pF + 1 TTL.	5 tcp*	—	ns
SCK ↑ → SOT delay time	t_{SHOVI}		− 50	+ 50	ns
SIN → SCK ↓ setup time	t_{IVSLI}		tcp* + 80	—	ns
SCK ↓ → SIN hold time	t_{SLIXI}		0	—	ns
SOT → SCK ↓ delay time	t_{SOVLI}		3 tcp* − 70	—	ns

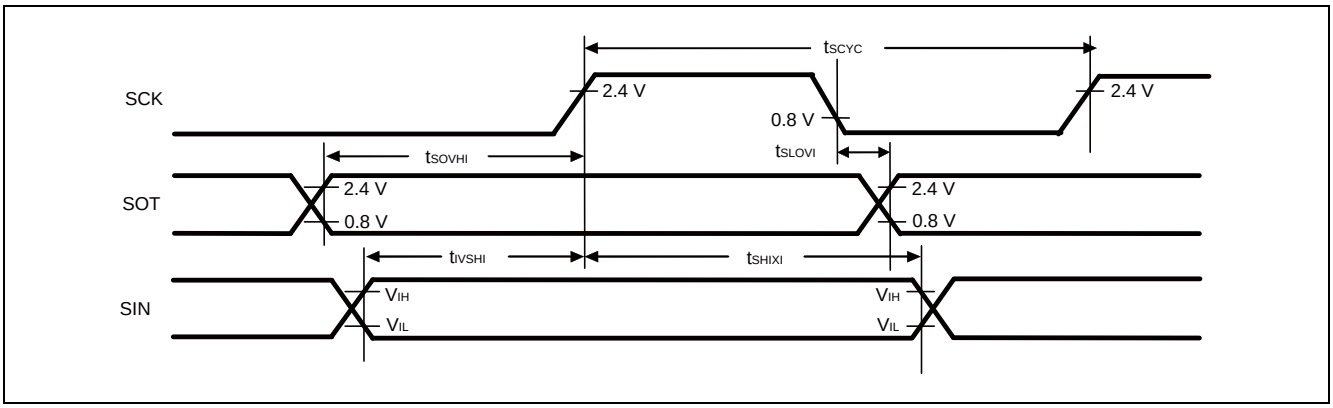
*: tcp indicates the machine clock time



ESCR : SCES = 1, ECCR : SCDE = 1

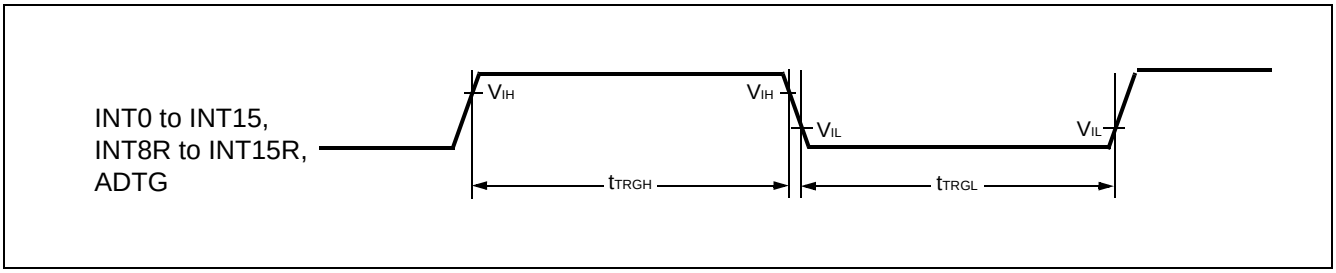
Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
Serial clock cycle time	t_{SCYC}	Internal clock operation C_L = 80 pF + 1 TTL.	5 tcp*	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}		– 50	+ 50	ns
SIN → SCK ↑ setup time	t_{IVSHI}		tcp* + 80	—	ns
SCK ↑ → SIN hold time	t_{SHIXI}		0	—	ns
SOT → SCK ↑ delay time	t_{SOVHI}		3 tcp* – 70	—	ns

*: tcp indicates the machine clock time



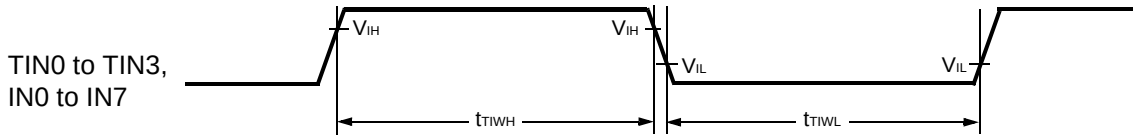
(10) Trigger Input Timing

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Input pulse width	t_{TRGH} t_{TRGL}	INT0 to INT15, INT8R to INT15R, ADTG	—	5 t_{CP}	—	ns



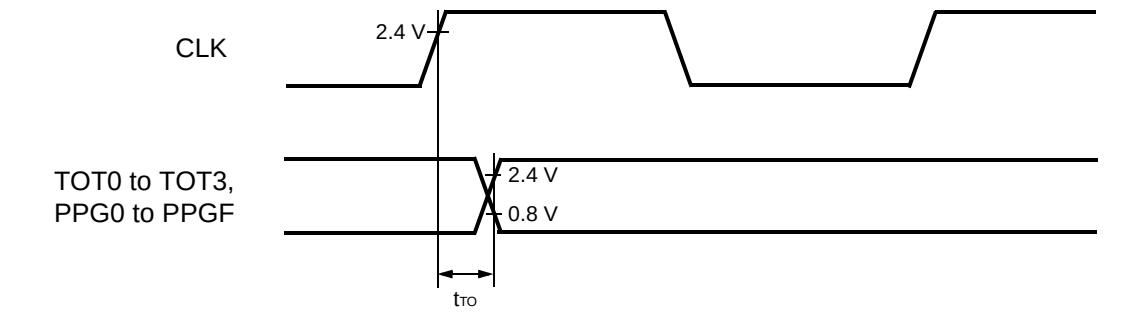
(11) Timer Related Resource Input Timing

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	TIN0 to TIN3, IN0 to IN7	—	4 t_{CP}	—	ns



(12) Timer Related Resource Output Timing

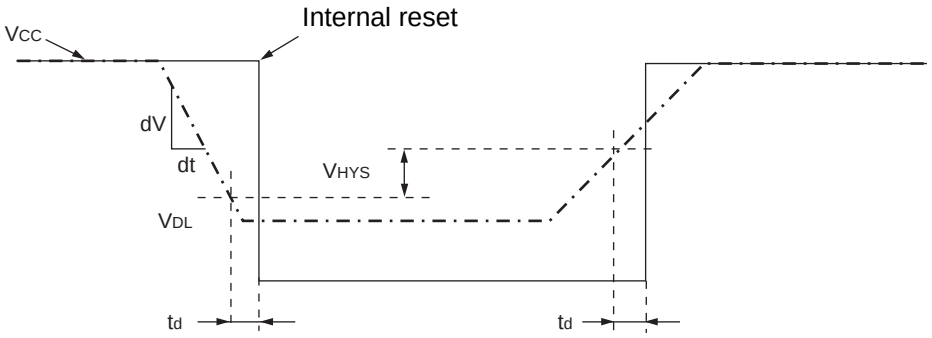
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
CLK ↑ → T_{OUT} change time	t_{TO}	TOT0 to TOT3, PPG0 to PPGF	—	30	—	ns



(13) Low voltage detection

Parameter	Symbol	Pin name	Condi-tions	Value			Unit	Remarks
				Min	Typ	Max		
Detection voltage initial value	V_{DL}	V_{CC}	—	3.8	4.0	4.2	V	During voltage drop
Hysteresis width	V_{HYS}	V_{CC}	—	169	173	177	mV	During voltage rise
Power supply voltage change rate	dV/dt	V_{CC}	—	– 0.1	—	+ 0.1	V/µs	dV/dt at low voltage reset
				– 0.004	—	+ 0.004	V/µs	dV/dt at standard value of low voltage detection/release voltage
Detection delay time	t_d	—	—	—	—	3.2	µs	When | dV/dt | ≤ 0.004 V/µs

Note: The power supply voltage change rate is at 0.004 V/µs<|dv/dt|<0.1 V/µs, a reset may be generated or released after the power supply voltage is passed the detection voltage range.



(14) I²C Timing

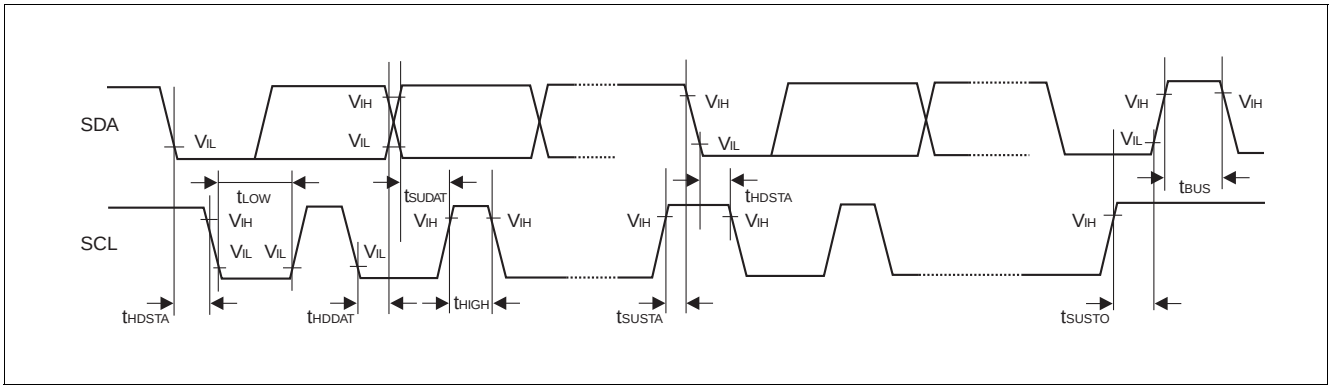
Parameter	Symbol	Conditions	Standard-mode		Fast-mode*1		Unit
			Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	R = 1.7 kΩ, C = 50 pF*2	0	100	0	400	kHz
Hold time (repeated) START condition SDA↓ → SCL ↓	t_{HDSTA}		4.0	—	0.6	—	µs
"L" width of the SCL clock	t_{LOW}		4.7	—	1.3	—	µs
"H" width of the SCL clock	t_{HIGH}		4.0	—	0.6	—	µs
Set-up time (repeated) START condition SCL ↑ → SDA ↓	t_{SUSTA}		4.7	—	0.6	—	µs
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45*3	0	0.9*4	µs
Data set-up time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		250	—	100	—	ns
Set-up time for STOP condition SCL ↑ → SDA ↑	t_{SUSTO}		4.0	—	0.6	—	µs
Bus free time between a STOP and START condition	t_{BUS}		4.7	—	1.3	—	µs

*1: For use at over 100 kHz, set the machine clock to at least 6 MHz.

*2: R,C: Pull-up resistor and load capacitor of the SCL and SDA lines.

*3: The maximum t_{HDDAT} meets the requirement that it does not extend the "L" width (t_{LOW}) of the SCL signal.

*4: A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement $t_{SUDAT} \geq 250$ ns must then be met.

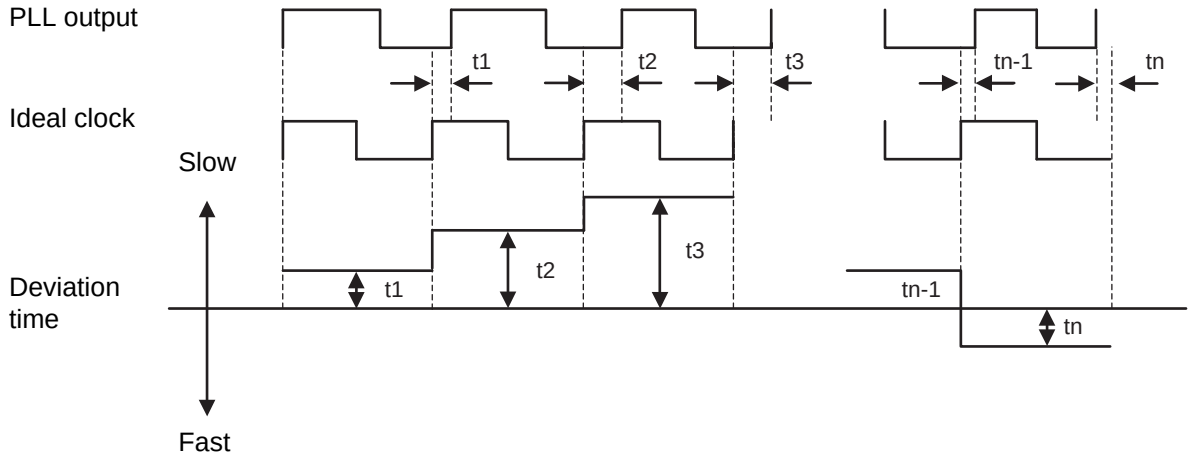


(15) CAN PLL cycle jitter

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
CAN PLL cycle jitter (When locked)	t_{PJ}	—	—	− 10	—	+ 10	ns	F_{CP} = 16 MHz (4 MHz × multiplied by 4) 24 MHz (4 MHz × multiplied by 6) 32 MHz (4 MHz × multiplied by 8)

• CAN PLL cycle jitter

Deviation time from the ideal clock is assured per cycle out of 20, 000 cycles.



5. A/D Converter

(3.0 V ≤ AVRH – AVRL)

Parameter	Symbol	Pin name	Condi-tions	Value			Unit	Remarks
				Min	Typ	Max		
Resolution	—	—	—	—	—	10	bit	
Total error	—	—	—	—	—	±3.0	LSB	
Nonlinearity error	—	—	—	—	—	±2.5	LSB	
Differential nonlinearity error	—	—	—	—	—	±1.9	LSB	
Zero reading voltage	V_{OT}	AN0 to AN23	—	AVRL – 1.5 LSB	AVRL + 0.5 LSB	AVRL + 2.5 LSB	V	
Full scale reading voltage	V_{FST}	AN0 to AN23	—	AVRH – 3.5 LSB	AVRH – 1.5 LSB	AVRH + 0.5 LSB	V	
Compare time	—	—	—	0.66	—	16500	µs	4.5 V ≤ AV_{CC} ≤ 5.5 V
				2.2				3.0 V ≤ AV_{CC} < 4.5 V
Sampling time	—	—	—	0.4	—	∞	µs	4.5 V ≤ AV_{CC} ≤ 5.5 V
				1.0				3.0 V ≤ AV_{CC} < 4.5 V
Analog port input current	I_{AIN}	AN0 to AN23	—	–0.3	—	+0.3	µA	
Analog input voltage range	V_{AIN}	AN0 to AN23	—	AVRL	—	AVRH	V	
Reference voltage range	—	AVRH	—	AVRL + 2.7	—	AV_{CC}	V	
	—	AVRL	—	0	—	AVRH – 2.7	V	
Power supply current	I_A	AV_{CC}	—	—	3.5	7.5	mA	
	I_{AH}	AV_{CC}	—	—	—	5	µA	*
Reference voltage current	I_R	AVRH	—	—	600	900	µA	
	I_{RH}	AVRH	—	—	—	5	µA	*
Offset between input channels	—	AN0 to AN23	—	—	—	4	LSB	

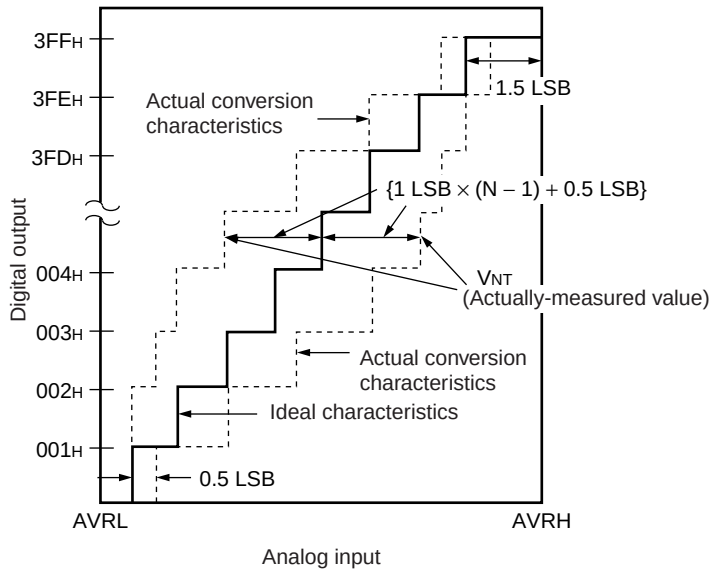
*: If the A/D convertor is not operating, a current when CPU is stopped is applicable (V_{CC} = AV_{CC} = AVRH = 5.0 V) .

Note: The accuracy gets worse as |AVRH – AVRL| becomes smaller.

6. Definition of A/D Converter Terms

Resolution	:	Analog variation that is recognized by the A/D converter.
Non linearity error	:	The deviation between the actual conversion characteristics and a line that joins the zero-transition line (“00 0000 0000” ← → “00 0000 0001”) to the full-scale transition line (“11 1111 1110” ← → “11 1111 1111”) .
Differential linearity error	:	Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.
Total error	:	Difference between the actual value and the ideal value. The total error includes zero transition error, full-scale transition error, and linear error.

Total error



$$\text{Total error of digital output “N”} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\ \text{LSB (Ideal value)} = \frac{\text{AVRH} - \text{AVRL}}{1024}\ [\text{V}]$$

N : Value of the digital output from the A/D converter

V_{OT} (Ideal value) = AVRL + 0.5 LSB [V]

V_{FST} (Ideal value) = AVRH – 1.5 LSB [V]

V_{NT} : A voltage at which the digital output transitions from $(N - 1)_H$ to N_H.

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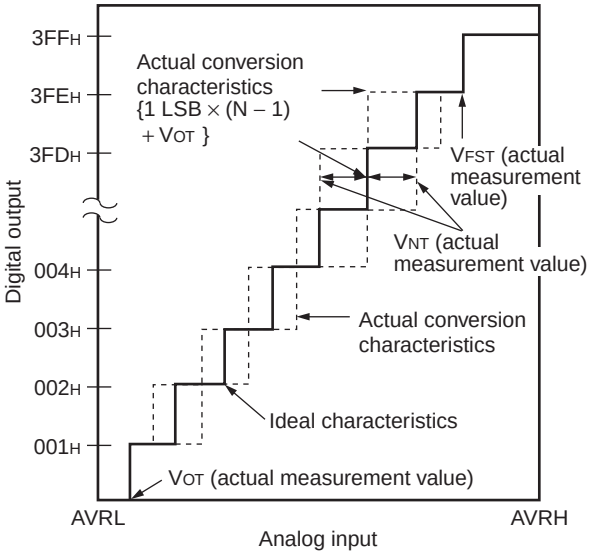
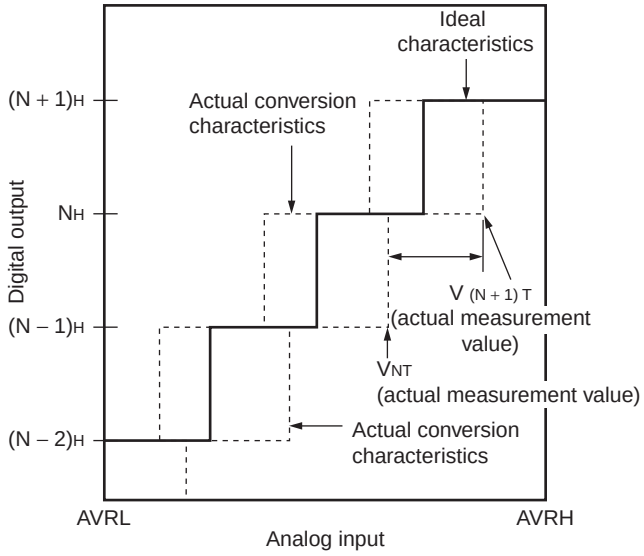
(Continued)

Non linearity error



Differential linearity error



$$\text{Non linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB}\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

N : Value of the digital output from the A/D converter
V_{OT} : Voltage at which digital output transits from “000_H” to “001_H.”
V_{FST} : Voltage at which digital output transits from “$3FE_H$” to “$3FF_H$.”

7. Notes on A/D Converter Section

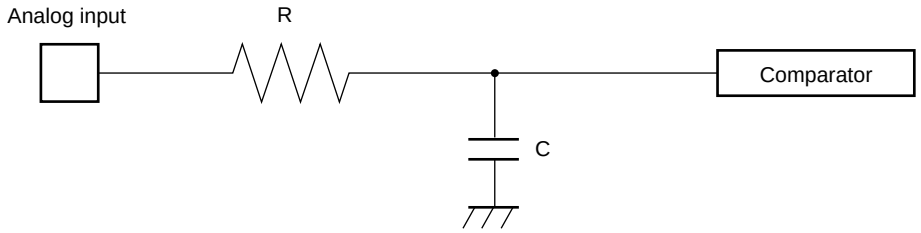
Use the device with external circuits of the following output impedance for analog inputs :

Recommended output impedance of external circuits are : Approx. 4.2 kΩ or lower (4.5 V ≤ AV_{CC} ≤ 5.5 V, sampling period = 0.4 µs)

If an external capacitor is used, in consideration of the capacitive voltage dividing effect between the external capacitor and the internal on-chip capacitor, it is recommended that the capacitance of the external capacitor be several thousand times greater than the capacitance of the internal capacitor.

If the output impedance of the external circuit is too high, a sampling period for an analog voltage may be insufficient.

• Analog input circuit model

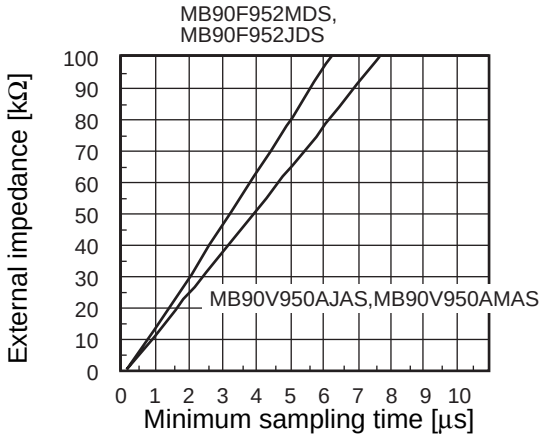


MB90F952JDS/F952MDS	4.5 V ≤ AV_{CC} ≤ 5.5 V : R≒ 4.1 kΩ, C≒ 8.5 pF
	3.0 V ≤ AV_{CC} < 4.5 V : R≒ 10.33 kΩ, C≒ 8.5 pF
MB90V950AJAS/V950AMAS	4.5 V ≤ AV_{CC} ≤ 5.5 V : R≒ 2.52 kΩ, C≒ 10.7 pF

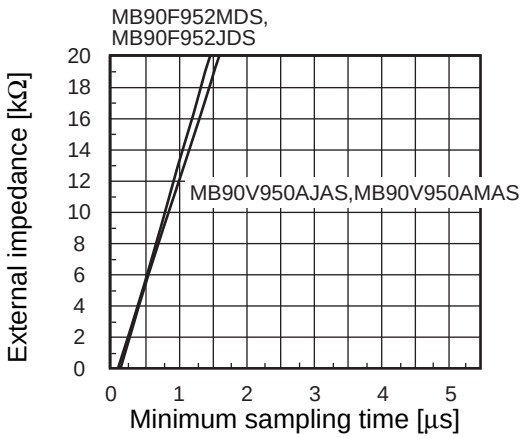
Note : Use the values in the figure only as a guideline.

- The relationship between external impedance and minimum sampling time
  - At 4.5 V ≤ AV_{CC} ≤ 5.5 V

(External impedance = 0 kΩ to 100 kΩ)



(External impedance = 0 kΩ to 20 kΩ)

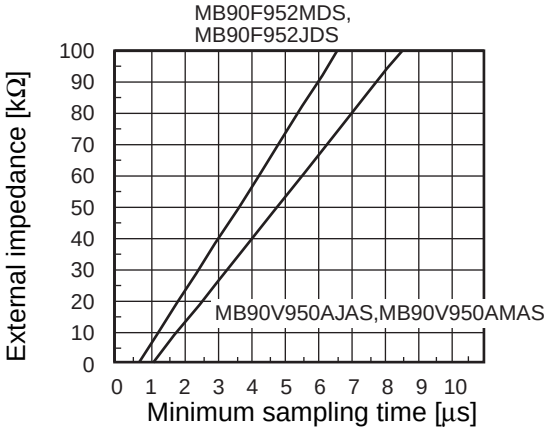


	Minimum sampling time [µs] (4.5 V ≤ AV_{CC} ≤ 5.5 V)		
External impedance [kΩ]	5	10	50
MB90F952MDS,MB90F952JDS	0.54	0.84	3.22
MB90V950AJAS,MB90V950AMAS	0.56	0.94	3.93

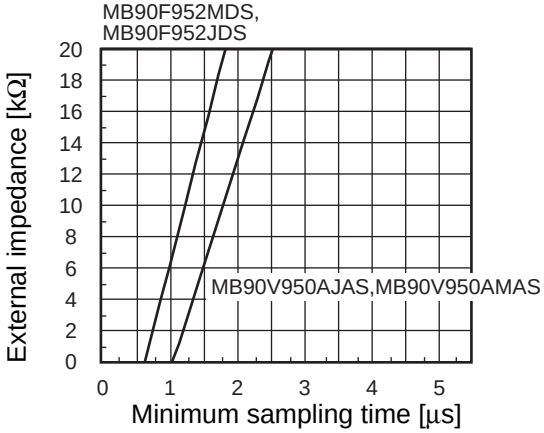
  - At 3.0 V ≤ AV_{CC} < 4.5 V

(MB90V950 is at 4.0 V ≤ AVcc < 4.5 V)

(External impedance = 0 kΩ to 100 kΩ)



(External impedance = 0 kΩ to 20 kΩ)



	Minimum sampling time [µs] (3.0 V ≤ AV_{CC}<4.5 V)		
External impedance [kΩ]	5	10	50
MB90F952MDS,MB90F952JDS	0.91	1.21	3.59
MB90V950AJAS,MB90V950AMAS	1.39	1.77	4.76

- **About errors**

As | AVR – AV_{SS} | becomes smaller, values of relative errors grow larger.

8. Flash Memory Program/Erase Characteristics

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	—	—	0.9	3.6	s	Excludes programming prior to erasure
Chip erase time		—	7.2	28.8	s	Main Flash
		—	3.6	14.4	s	Satellite Flash
Word (16-bit width) programming time		—	15	240	µs	Except for the overhead time of the system
Word (16-bit width) programming time		—	23	370	µs	Except for the overhead time of the system
Program/Erase cycle	T_A > +85 °C	10000	—	—	cycle	
	$T_A \leq$ +85 °C	100000	—	—	cycle	
Flash Data Retention Time	Average T_A = +85 °C	20	—	—	year	*

* : The value was converted into the normalized temperature at +85ÅãC from the results of evaluating the reliability of the technology.

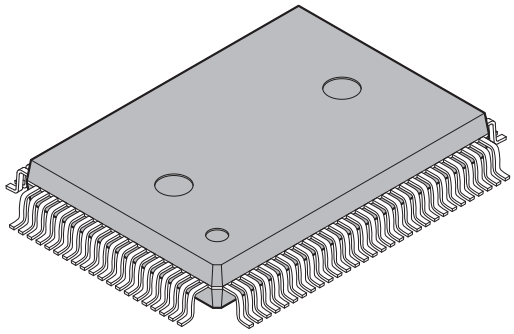
9. D/A Converter

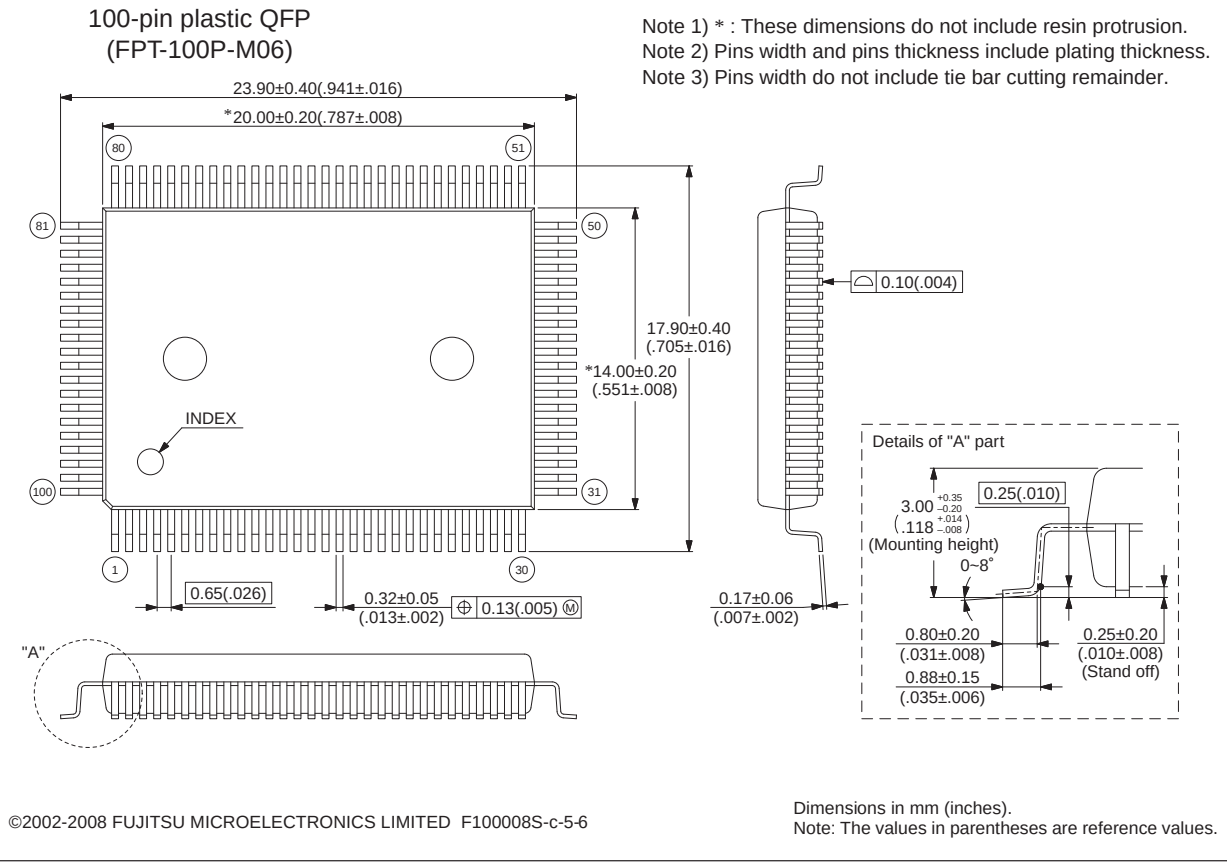
Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Resolution	—	—	—	—	8	—	bit	
Non linearity error	—	—	—	-0.5	—	+0.5	LSB	
Conversion time	—	—	—	0.773	0.787	1.078	µs	C_L = 20 pF
			—	2.490	2.535	3.474		C_L = 100 pF
Output impedance	R_O	DA0, DA1	—	3.19	3.50	4.80	kΩ	
Power supply current	I_A	AV_{CC}	—	—	476	920	µA	
	I_{AH}	AV_{CC}	—	—	—	5	µA	

■ ORDERING INFORMATION

Part number	Package	Remarks
MB90F952JDSPF	100-pin plastic QFP (FPT-100P-M06)	
MB90F952MDSPF		
MB90F952JDSPFV	100-pin plastic LQFP (FPT-100P-M20)	
MB90F952MDSPFV		
MB90V950AMASCR-ES	299-pin ceramic PGA (PGA-299C-A01)	For evaluation
MB90V950AJASCR-ES		

■ PACKAGE DIMENSIONS

100-pin plastic QFP		
	Lead pitch	0.65 mm
	Package width × package length	14.00 × 20.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	3.35 mm MAX
	Code (Reference)	P-QFP100-14×20-0.65
(FPT-100P-M06)		



Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

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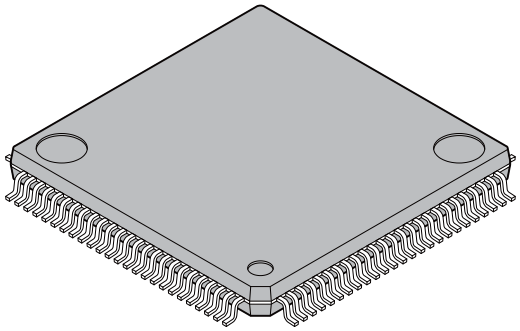
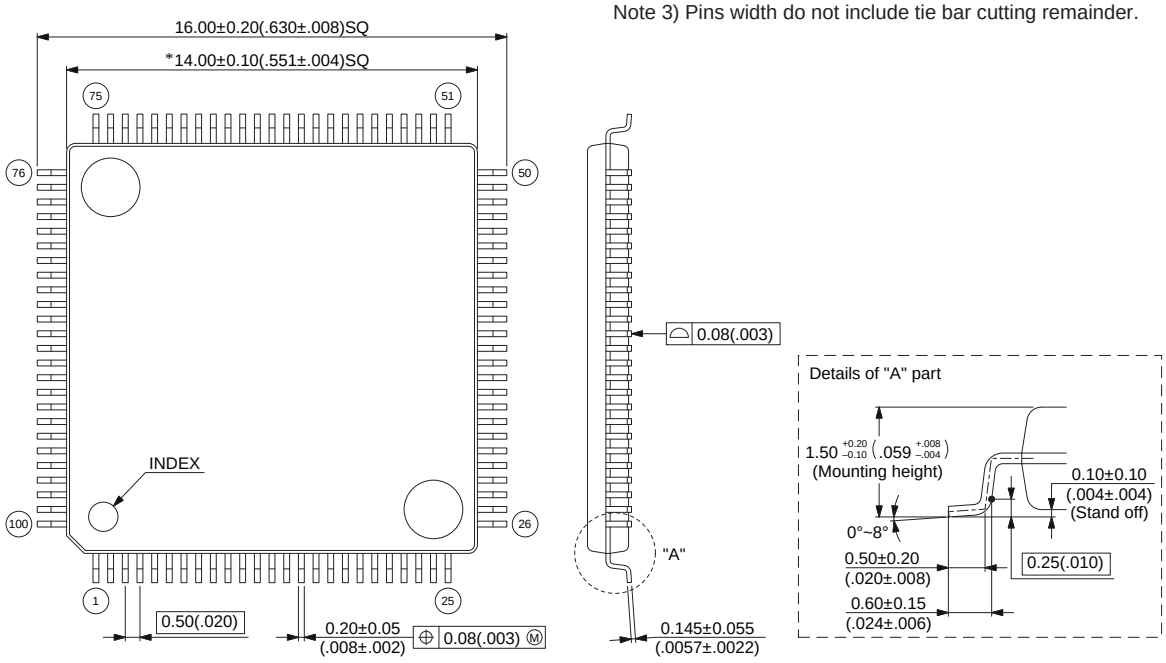
100-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	14.0 mm × 14.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm Max
	Weight	0.65 g
(FPT-100P-M20)	Code (Reference)	P-LFQFP100-14×14-0.50

100-pin plastic LQFP
(FPT-100P-M20)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values

Please confirm the latest Package dimension by following URL.
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■ MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
—	—	Changed the part number; MB90V950MAS→MB90V950AMAS MB90V950JAS→MB90V950AJAS
74	■ ELECTRICAL CHARACTERISTICS 4. AC Characteristics	Added the item “(15) CAN PLL cycle jitter”.

The vertical lines marked in the left side of the page show the changes.

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