

16-bit Microcontroller

CMOS

F²MC-16LX MB90860E Series

MB90867E(S)/F867E(S)/V340E-101/V340E-102

■ DESCRIPTION

The MB90860E series with integrated Flash ROM is a general-purpose Fujitsu 16-bit microcontroller designed for automotive and other industrial applications. By utilizing new 0.35 μm CMOS technology, Fujitsu Microelectronics now offers a 128KBytes of on-chip Flash ROM program memory.

Furthermore, the 3 V power supply of the internal MCU core is supplied by an internal regulator circuit, making this a vastly superior product in terms of reliability and power consumption.

Note : F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

■ FEATURES

• CPU

- Optimal instruction suitable for controller applications
 - Wide range of data types (bit, byte, word, and long word)
 - Wide range of addressing modes (23 types)
 - Enhanced multiplication and division instructions, and enhanced RETI instruction
 - Enhanced high-precision calculations using a 32-bit accumulator
- Instruction set level support for high level languages (C language) and multitask
 - Equipped with a system stack pointer
 - A variety of enhanced pointer indirect instructions
 - Barrel shift instructions
- Increased processing speed
 - 4-byte instruction queue

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The information for microcontroller supports is shown in the following homepage.
Be sure to refer to the "Check Sheet" for the latest cautions on development.

"Check Sheet" is seen at the following support page

"Check Sheet" lists the minimal requirement items to be checked to prevent problems beforehand in system development.

<http://edevic.fujitsu.com/micom/en-support/>

MB90860E Series

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- **Serial interface**

- LIN-UART : 4 channels
 - Equipped with full-duplex double buffer
 - Clock-asynchronous and clock-synchronous serial transmission are available
- I²C interface : 2 channels
 - Up to 400 kbps transfer rate

- **Interrupt controller**

- Powerful interrupt function with 8 levels and 34 sources
- Supports up to 16 external interrupts
- CPU-independent automatic data transfer function
 - Expanded intelligent I/O service function (EI²OS) : up to 16 channels

- **I/O ports**

- General-purpose input/output ports (CMOS output)
 - 80 ports (devices without an S suffix in the part number - devices that support a sub clock)
 - 82 ports (devices with an S suffix in the part number - devices that do not support a sub clock)

- **8/10-bit A/D converter : 24 channels**

- Resolution is selectable between 8-bit and 10-bit.
- Can be activated by an external trigger.
- Conversion time : 3 μ s (at 24-MHz machine clock, including sampling time)

- **Address match detection (program patch) function**

- Address match detection for 6 address pointers

- **Timers**

- Time-base timer, watch timer, watchdog timer : 1 channel
- 8/16-bit PPG timer : 8-bit \times 16 channels or 16-bit \times 8 channels
- 16-bit reload timer : 4 channels
- 16-bit I/O timer
 - 16-bit free run timer : 2 channel (FRT0 : ICU 0/1/2/3, OCU 0/1/2/3, FRT1 : ICU 4/5/6/7, OCU 4/5/6/7)
 - 16-bit input capture (ICU) : 8 channels
 - 16-bit output compare (OCU) : 8 channels

- **Low power consumption (standby) modes**

- Sleep mode (a mode where the CPU operating clock stops)
- Time-base timer mode (a mode where only the oscillator clock, sub clock, time-base timer, and watch timer operate)
- Watch mode (a mode where only the sub clock and watch timer operate)
- Stop mode (a mode where the oscillator clock and sub clock stop)
- CPU blocking operation mode

- **Clock modulator**

- **Technology**

- 0.35 μ m CMOS technology

■ PRODUCT LINEUP

Part Number	MB90867E(S)	MB90F867E(S)	MB90V340E-101/102
CPU	F ² MC-16LX CPU		
Type	MASK ROM product	Flash memory product	Evaluation product
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, ×6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (4 MHz osc. PLL × 6)		
ROM	MASK ROM 128 Kbytes	Flash memory 128 Kbytes	External
RAM	6 Kbytes	6 Kbytes	30 Kbytes
Dedicated power supply for emulator*	—		Yes
Technology	0.35 μm CMOS with on-chip voltage regulator for internal power supply	0.35 μm CMOS with on-chip voltage regulator for internal power supply + Flash memory with on-chip charge pump for programming voltage	0.35 μm CMOS with on-chip voltage regulator for internal power supply
Operating voltage range	3.5 V to 5.5 V : during normal operation (not using A/D converter) 4.0 V to 5.5 V : when using A/D converter/Flash programming 4.5 V to 5.5 V : when using external bus		5 V ± 10%
Temperature range	-40 °C to +105 °C		—
Package	QFP-100, LQFP-100		PGA-299
LIN-UART	4 channels		5 channels
	Wide range of baud rate settings using a dedicated baud rate generator (reload timer) Special synchronous options for adapting to different synchronous serial protocols LIN functionality can operate as either master or slave LIN device		
I ² C (400 kbps)	2 channels		
8/10-bit A/D converter	24 channels		
	10-bit or 8-bit resolution Conversion time : Min 3 μs include sample time (per one channel)		
16-bit reload timer (4 channels)	Operation clock frequency : $f_{sys}/2^1$, $f_{sys}/2^3$, $f_{sys}/2^5$ (f_{sys} = Machine clock frequency) Supports External Event Count function		
16-bit free run timer (2 channels)	Generates an interrupt on overflow Supports Timer Clear when a match with Output Compare (ch.0, ch.4) Operation clock freq. : f_{sys} , $f_{sys}/2^1$, $f_{sys}/2^2$, $f_{sys}/2^3$, $f_{sys}/2^4$, $f_{sys}/2^5$, $f_{sys}/2^6$, $f_{sys}/2^7$ (f_{sys} = Machine clock freq.) Free run Timer 0 (clock input FRCK0) corresponds to ICU 0/1/2/3, OCU 0/1/2/3 Free run Timer 1 (clock input FRCK1) corresponds to ICU 4/5/6/7, OCU 4/5/6/7		
16-bit output compare (8 channels)	Generates an interrupt when the 16-bit free run timer matches the output compare register. Multiple compare registers can be used to generate an output signal.		
16-bit input capture (8 channels)	Captures the value of the 16-bit free run timer and generates an interrupt when triggered by a pin input (rising edge, falling edge, or both rising and falling edges).		

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MB90860E Series

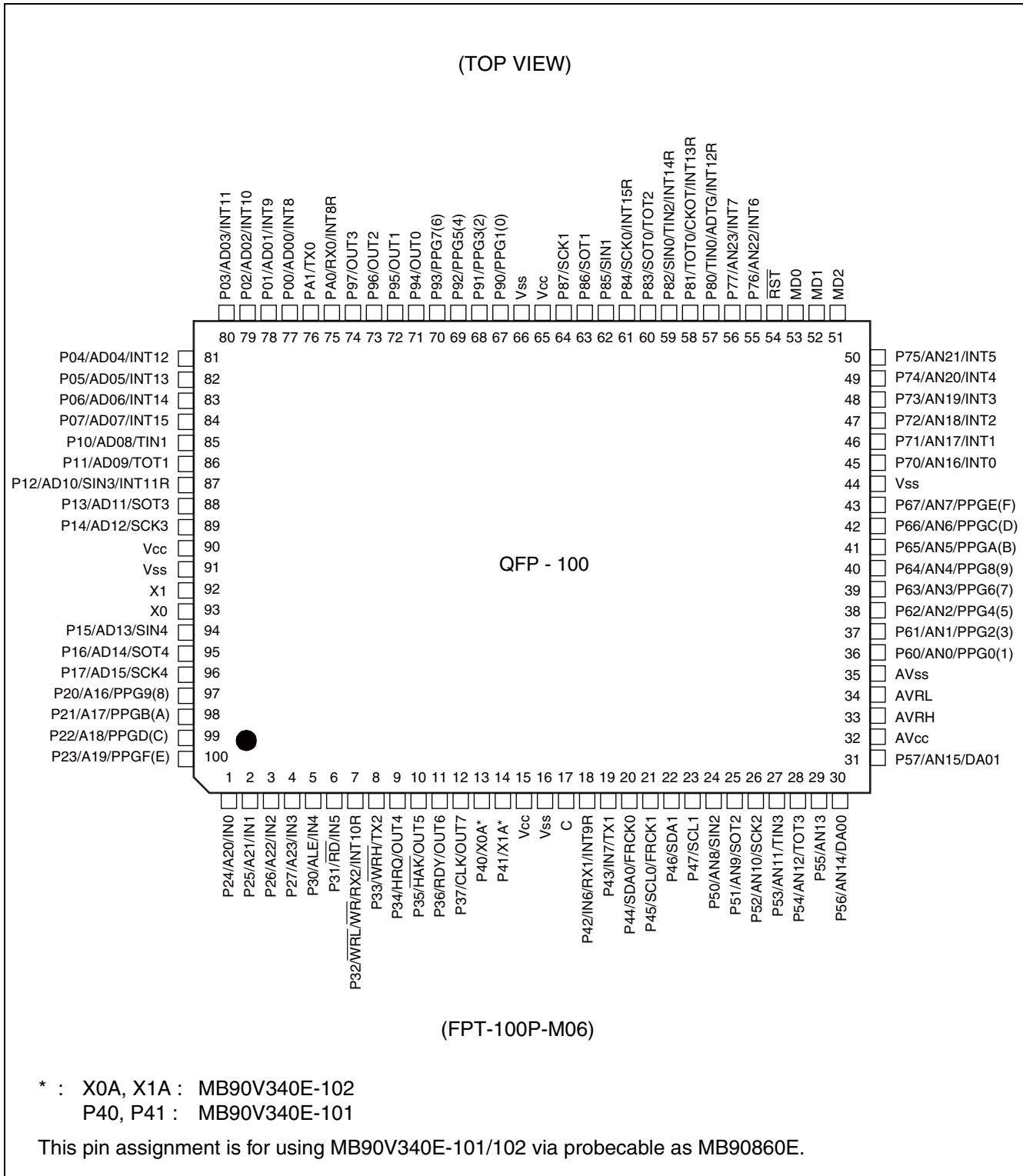
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Part Number Parameter	MB90867E(S)	MB90F867E(S)	MB90V340E-101/102
8/16-bit programmable pulse generator (8 channels)	8 channels (16-bit) or 16 channels (8-bit) 8-bit reload counter × 16 8-bit reload registers for lower part × 16 8-bit reload registers for upper part × 16 Supports 8-bit and 16-bit operating modes A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as an 8-bit prescaler plus an 8-bit reload counter Operation clock freq. : f_{sys} , $f_{sys}/2^1$, $f_{sys}/2^2$, $f_{sys}/2^3$, $f_{sys}/2^4$ or $128 \mu s @ f_{osc} = 4 \text{ MHz}$ (f_{sys} = Machine clock frequency, f_{osc} = Oscillation clock frequency)		
CAN interface	—		3 channels
External interrupt (16 channels)	Can be triggered by rising edge, falling edge, or H/L level inputs, external interrupts can be used by expanded intelligent I/O services (EI ² OS) and DMA		
D/A converter	—		2 channels
Sub clock (maximum 100 kHz)	Devices without 'S' suffix in the part number		Only for MB90V340E-102
I/O ports	Virtually all external pins can be used as general-purpose I/O ports All push-pull outputs Bitwise configurable as input/output or peripheral signal Configurable in blocks of 8 pins as CMOS schmitt trigger or automotive inputs Configurable as TTL input levels for an external bus (only applies to the 32 external bus pins)		
Flash memory	Supports automatic programming, Embedded Algorithm Write/Erase/Erased-Suspend/Resume commands Equipped with a flag indicating completion of the algorithm Number of erase cycles : 10,000 times Data retention time : 20 years Boot block configuration Erase can be performed on each block Block protection with external programming voltage Flash Security Feature for protecting the content of the Flash		—

* : Configured by the jumper switch (TOOL VCC) when the emulator (MB2147-01) is used.
Please refer to the Emulator hardware manual for details.

PIN ASSIGNMENTS

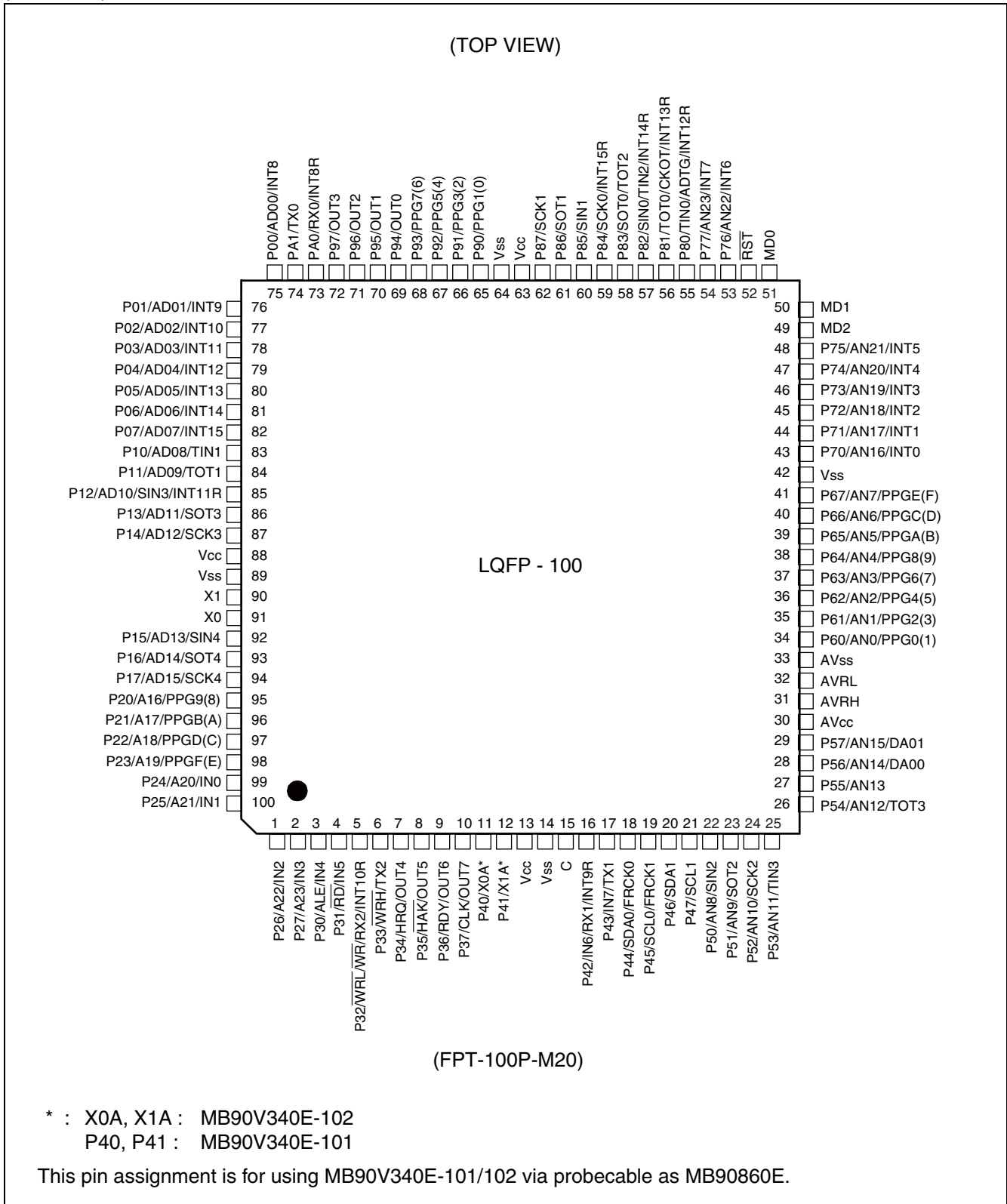
• MB90V340E-101/102



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MB90860E Series

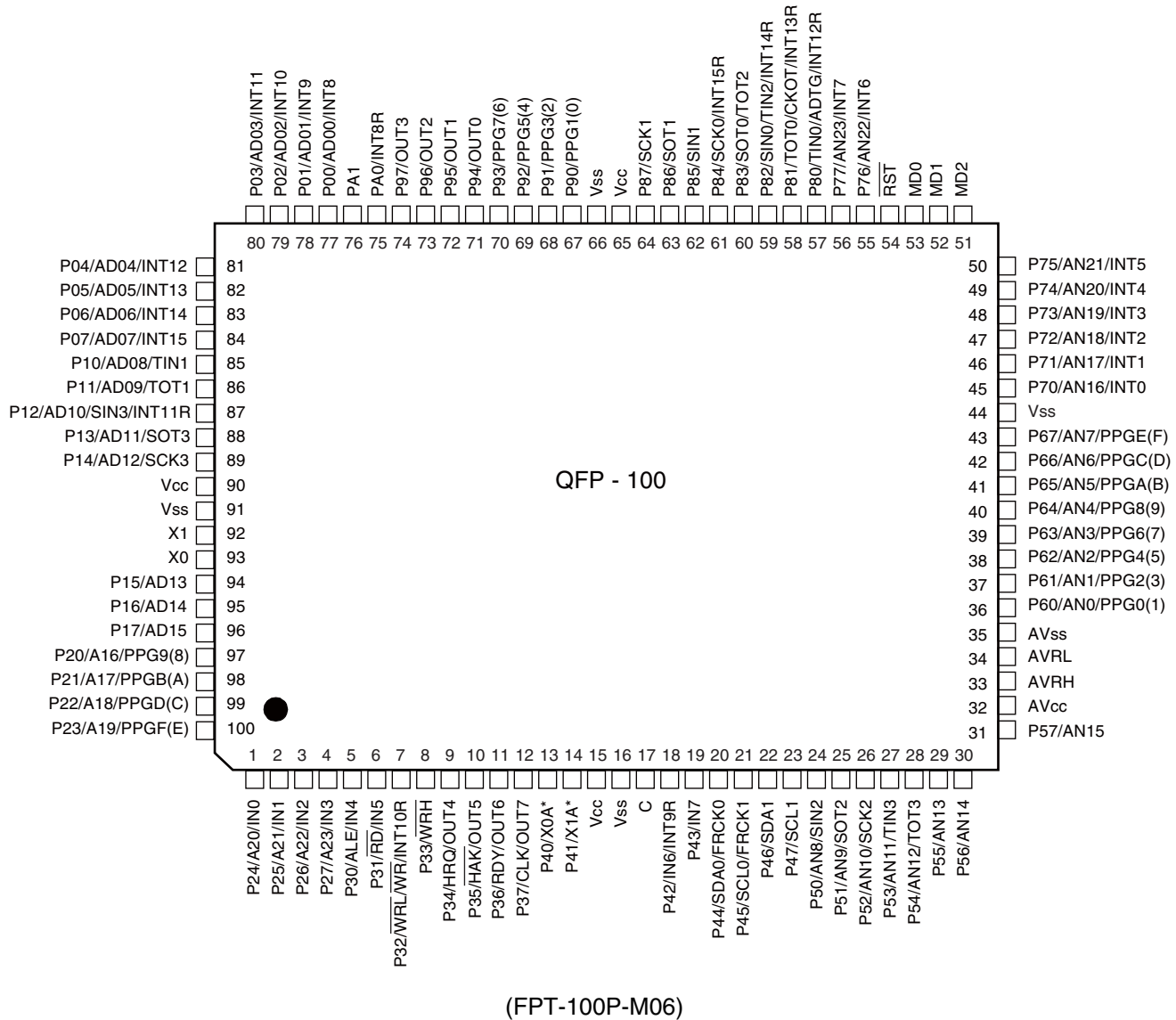
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MB90860E Series

- MB90867E(S)/MB90F867E(S)

(TOP VIEW)



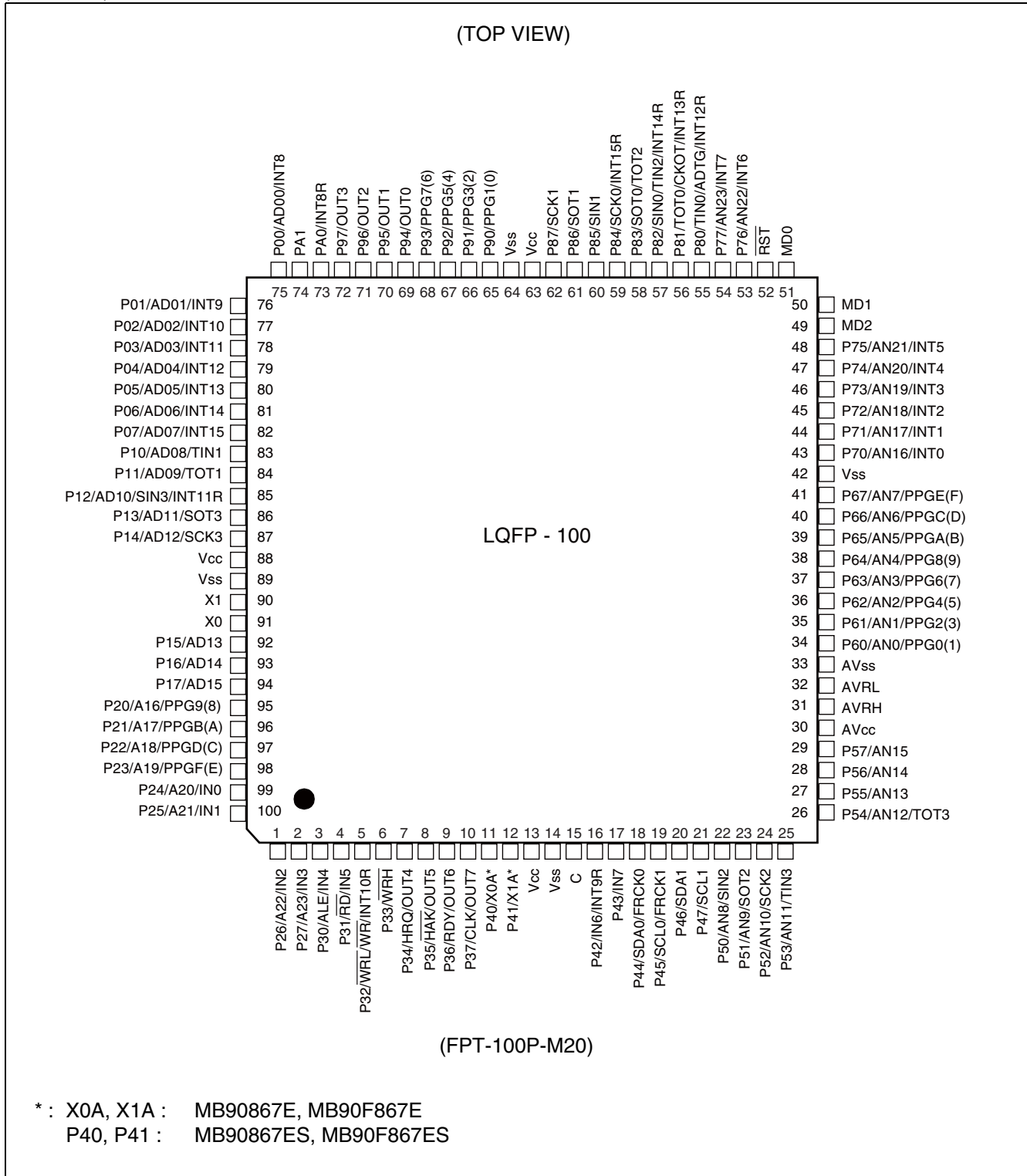
(FPT-100P-M06)

* : X0A, X1A : MB90867E, MB90F867E
 P40, P41 : MB90867ES/MB90F867ES

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MB90860E Series

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■ PIN DESCRIPTION

Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
1 to 4	99 to 2	P24 to P27	G	General-purpose I/O pins. It is possible to select whether or not a pull-up resistance is used by configuring a register. In external bus mode, each pin is enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1.
		A20 to A23		External address bus output pins. When the corresponding bits in the external address output control register (HACR) are 0, the pins are enabled as high address output pins (A20 to A23).
		IN0 to IN3		Trigger input pins for input captures 0 to 3.
5	3	P30	G	General-purpose I/O pin. It is possible to select whether or not a pull-up resistance is used by configuring a register. This function is enabled in single-chip mode.
		ALE		Address latch enable output pin. This function is enabled when the external bus is enabled.
		IN4		Trigger input pin for input capture 4.
6	4	P31	G	General-purpose I/O pin. It is possible to select whether or not a pull-up resistance is used by configuring a register. This function is enabled in single-chip mode.
		\overline{RD}		External read strobe output pin. This function is enabled when the external bus is enabled.
		IN5		Trigger input pin for input capture 5.
7	5	P32	G	General-purpose I/O pin. It is possible to select whether or not a pull-up resistance is used by configuring a register. This function is enabled either in single-chip mode or when the $\overline{WR}/\overline{WRL}$ pin output disabled.
		$\overline{WR} / \overline{WRL}$		Write strobe output pin for the external data bus. This function is enabled when both the external bus and the $\overline{WR}/\overline{WRL}$ pin output are enabled. \overline{WRL} is used as a write strobe output for the lower 8 bits of the data bus in 16-bit access while \overline{WR} is used as the write strobe for the 8 bits of the data bus in 8-bit access.
		INT10R		External interrupt request input pin (sub) .
8	6	P33	G	General-purpose I/O pin. It is possible to select whether or not a pull-up resistance is used by configuring a register. This function is enabled either in single-chip mode or when the \overline{WRH} pin output disabled.
		\overline{WRH}		Write strobe output pin for the upper 8 bits of the external data bus. This function is enabled when the external bus is enabled, and the external bus is in 16-bit mode, and the \overline{WRH} output pin is enabled.

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MB90860E Series

Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
9	7	P34	G	General-purpose I/O pin. It is possible to select whether or not a pull-up resistance is used by configuring a register. This function is enabled either in single-chip mode or when the hold function is disabled.
		HRQ		Hold request input pin. This function is enabled when both the external bus and the hold function are enabled.
		OUT4		Waveform output pin for output compare 4.
10	8	P35	G	General-purpose I/O pin. It is possible to select whether or not a pull-up resistance is used by configuring a register. This function is enabled either in single-chip mode or when the hold function is disabled.
		$\overline{\text{HAK}}$		Hold acknowledge output pin. This function is enabled when both the external bus and the hold function are enabled.
		OUT5		Waveform output pin for output compare 5.
11	9	P36	G	General-purpose I/O pin. It is possible to select whether or not a pull-up resistance is used by configuring a register. This function is enabled either in single-chip mode or when the external ready function is disabled.
		RDY		External ready input pin. This function is enabled when both the external bus and the external ready function are enabled.
		OUT6		Waveform output pin for output compare 6.
12	10	P37	G	General-purpose I/O pin. It is possible to select whether or not a pull-up resistance is used by configuring a register. This function is enabled either in single-chip mode or when clock output is disabled.
		CLK		Clock output pin. This function is enabled when both the external bus and clock output are enabled.
		OUT7		Waveform output pin for output compare 7.
13, 14	11, 12	P40, P41	F	General-purpose I/O pins (devices with an "S" suffix in the part number).
		X0A, X1A	B	Input pins for sub-clock (devices without an "S" suffix in the part number).
15	13	V _{CC}	—	Power (3.5 V to 5.5 V) input pin.
16	14	V _{SS}	—	GND pin.
17	15	C	K	This is the power supply stabilization capacitor pin. It should be connected to a ceramic capacitor with a capacitance of 0.1 μF or higher.
18	16	P42	F	General-purpose I/O pin.
		IN6		Trigger input pin for input capture 6.
		INT9R		External interrupt request input pin (sub) .

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MB90860E Series

Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
19	17	P43	F	General-purpose I/O pin.
		IN7		Trigger input pin for input capture 7.
20	18	P44	H	General-purpose I/O pin.
		SDA0		Serial data I/O pin for I ² C 0.
		FRCK0		Input pin for 16-bit free run timer 0.
21	19	P45	H	General-purpose I/O pin.
		SCL0		Serial clock I/O pin for I ² C 0.
		FRCK1		Input pin for 16-bit free run timer 1.
22	20	P46	H	General-purpose I/O pin.
		SDA1		Serial data I/O pin for I ² C 1.
23	21	P47	H	General-purpose I/O pin.
		SCL1		Serial clock I/O pin for I ² C 1.
24	22	P50	O	General-purpose I/O pin.
		AN8		Analog input pin for the A/D converter.
		SIN2		Serial data input pin for UART2.
25	23	P51	I	General-purpose I/O pin.
		AN9		Analog input pin for the A/D converter.
		SOT2		Serial data output pin for UART2.
26	24	P52	I	General-purpose I/O pin.
		AN10		Analog input pin for the A/D converter.
		SCK2		Clock I/O pin for UART2.
27	25	P53	I	General-purpose I/O pin.
		AN11		Analog input pin for the A/D converter.
		TIN3		Event input pin for reload timer 3.
28	26	P54	I	General-purpose I/O pin.
		AN12		Analog input pin for the A/D converter.
		TOT3		Output pin for reload timer 3.
29	27	P55	I	General-purpose I/O pin.
		AN13		Analog input pin for the A/D converter.
30, 31	28, 29	P56, P57	J	General-purpose I/O pins.
		AN14, AN15		Analog input pin for the A/D converter.
32	30	AV _{CC}	K	Analog power input pin for the A/D converter.

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Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
33	31	AVRH	L	Reference voltage input pin for the A/D converter. This power supply must be turned on or off while a voltage higher than or equal to AVRH is applied to AV _{CC} .
34	32	AVRL	K	Lower reference voltage input pin for the A/D converter.
35	33	AV _{SS}	K	Analog GND pin for the A/D converter.
36 to 43	34 to 41	P60 to P67	I	General-purpose I/O pins.
		AN0 to AN7		Analog input pins for the A/D converter.
		PPG0, 2, 4, 6, 8, A, C, E		PPG output pins.
44	42	V _{SS}	—	GND pin.
45 to 50	43 to 48	P70 to P75	I	General-purpose I/O pins.
		AN16 to AN21		Analog input pins for the A/D converter.
		INT0 to INT5		External interrupt request input pins.
51	49	MD2	D	Input pin for specifying the operating mode.
52, 53	50, 51	MD1, MD0	C	Input pins for specifying the operating mode.
54	52	RST	E	Reset input.
55, 56	53, 54	P76, P77	I	General-purpose I/O pins.
		AN22, AN23		Analog input pins for the A/D converter.
		INT6, INT7		External interrupt request input pins.
57	55	P80	F	General-purpose I/O pin.
		TIN0		Event input pin for reload timer 0.
		ADTG		Trigger input pin for the A/D converter.
		INT12R		External interrupt request input pin (sub) .
58	56	P81	F	General-purpose I/O pin.
		TOT0		Output pin for reload timer 0.
		CKOT		Output pin for the clock monitor.
		INT13R		External interrupt request input pin (sub) .
59	57	P82	M	General-purpose I/O pin.
		SIN0		Serial data input pin for UART0.
		TIN2		Event input pin for reload timer 2.
		INT14R		External interrupt request input pin (sub) .
60	58	P83	F	General-purpose I/O pin.
		SOT0		Serial data output pin for UART0.
		TOT2		Output pin for reload timer 2.

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Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
61	59	P84	F	General-purpose I/O pin.
		SCK0		Clock I/O pin for UART0.
		INT15R		External interrupt request input pin (sub) .
62	60	P85	M	General-purpose I/O pin.
		SIN1		Serial data input pin for UART1.
63	61	P86	F	General-purpose I/O pin.
		SOT1		Serial data output pin for UART1.
64	62	P87	F	General-purpose I/O pin.
		SCK1		Clock I/O pin for UART1.
65	63	V _{CC}	—	Power (3.5 V to 5.5 V) input pins.
66	64	V _{SS}	—	GND pins.
67 to 70	65 to 68	P90 to P93	F	General-purpose I/O pins.
		PPG1, 3, 5, 7		PPG output pins.
71 to 74	69 to 72	P94 to P97	F	General-purpose I/O pins.
		OUT0 to OUT3		Waveform output pins for output compare 0 to 3. This function is enabled when waveform output is enabled.
75	73	PA0	F	General-purpose I/O pin.
		INT8R		External interrupt request input pin (sub) .
76	74	PA1	F	General-purpose I/O pin.
77 to 84	75 to 82	P00 to P07	G	General-purpose I/O pins. It is possible to select whether or not a pull-up resistance is used by configuring a register. This function is enabled in single-chip mode.
		AD00 to AD07		I/O pins for the lower 8 bits of the external address/data bus. This function is enabled when the external bus is enabled.
		INT8 to INT15		External interrupt request input pins.
85	83	P10	G	General-purpose I/O pin. It is possible to select whether or not a pull-up resistance is used by configuring a register. This function is enabled in single-chip mode.
		AD08		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		TIN1		Event input pin for reload timer 1.

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Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
86	84	P11	G	General-purpose I/O pin. It is possible to select whether or not a pull-up resistance is used by configuring a register. This function is enabled in single-chip mode.
		AD09		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		TOT1		Output pin for reload timer 1.
87	85	P12	N	General-purpose I/O pin. It is possible to select whether or not a pull-up resistance is used by configuring a register. This function is enabled in single-chip mode.
		AD10		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		SIN3		Serial data input pin for UART3.
		INT11R		External interrupt request input pin (sub) .
88	86	P13	G	General-purpose I/O pin. It is possible to select whether or not a pull-up resistance is used by configuring a register. This function is enabled in single-chip mode.
		AD11		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		SOT3		Serial data output pin for UART3.
89	87	P14	G	General-purpose I/O pin. It is possible to select whether or not a pull-up resistance is used by configuring a register. This function is enabled in single-chip mode.
		AD12		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		SCK3		Clock I/O pin for UART3.
90	88	V _{CC}	—	Power (3.5 V to 5.5 V) input pin.
91	89	V _{SS}	—	GND pin.
92	90	X1	A	Main clock output pin.
93	91	X0		Main clock input pin.
94	92	P15	G	General-purpose I/O pin. It is possible to select whether or not a pull-up resistance is used by configuring a register. This function is enabled in single-chip mode.
		AD13		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
95	93	P16	G	General-purpose I/O pin. It is possible to select whether or not a pull-up resistance is used by configuring a register. This function is enabled in single-chip mode.
		AD14		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.

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Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
96	94	P17	G	General-purpose I/O pin. It is possible to select whether or not a pull-up resistance is used by configuring a register. This function is enabled in single-chip mode.
		AD15		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
97 to 100	95 to 98	P20 to P23	G	General-purpose I/O pins. It is possible to select whether or not a pull-up resistance is used by configuring a register. In external bus mode, each pin is enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1.
		A16 to A19		Output pins of the external address bus. When the corresponding bit in the external address output control register (HACR) is 0, the pins are enabled as high address output pins (A16 to A19).
		PPG9, B, D, F		PPG output pins.

*1 : FPT-100P-M06

*2 : FPT-100P-M20

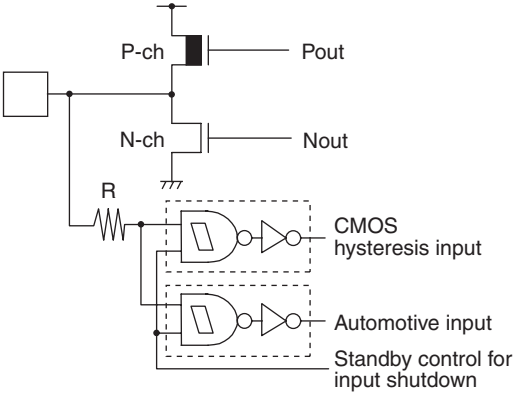
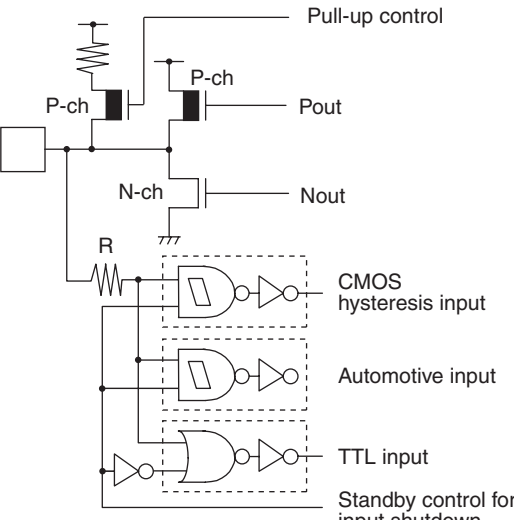
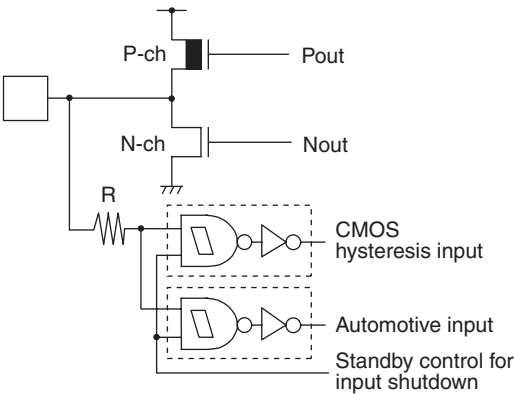
*3 : Refer to "■ I/O CIRCUIT TYPE" for details on the I/O circuit types.

MB90860E Series

■ I/O CIRCUIT TYPE

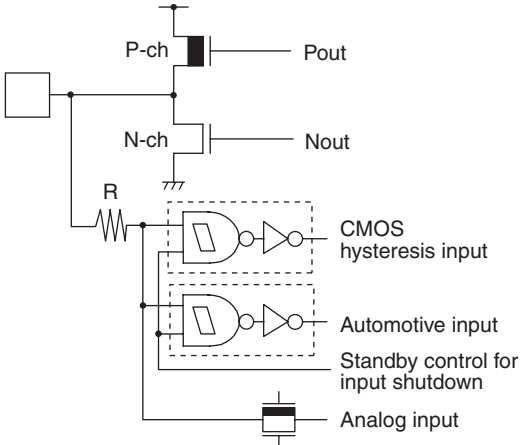
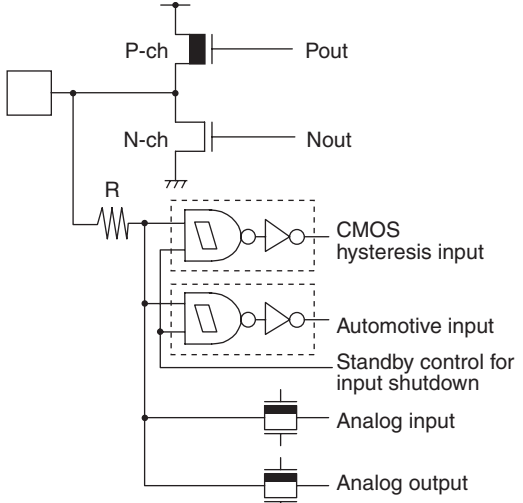
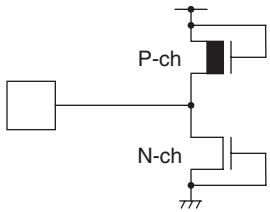
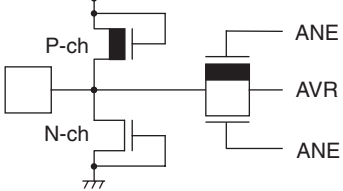
Type	Circuit	Remarks
A		<p>Oscillator circuit</p> <p>High-speed oscillator feedback resistance = approx. 1 MΩ</p>
B		<p>Oscillator circuit</p> <p>Low-speed oscillator feedback resistance = approx. 10 MΩ</p>
C		<ul style="list-style-type: none"> Mask ROM and evaluation device: CMOS hysteresis input pin Flash memory device: CMOS input pin
D		<ul style="list-style-type: none"> Mask ROM and evaluation device: CMOS hysteresis input pin Pull-down resistor value: approx. 50 kΩ Flash memory device: CMOS input pin No pull-down
E		<p>CMOS hysteresis input pin</p> <p>Pull-up resistor value: approx. 50 kΩ</p>

(Continued)

Type	Circuit	Remarks
F	 <p>The diagram shows a CMOS output stage with a P-channel MOSFET (P-ch) and an N-channel MOSFET (N-ch). The P-ch MOSFET is connected to the output terminal Pout, and the N-ch MOSFET is connected to the output terminal Nout. A pull-up resistor R is connected between the input and the P-ch MOSFET gate. The input is connected to three logic blocks: a CMOS hysteresis input (two inverters), an Automotive input (two inverters), and a Standby control for input shutdown (two inverters).</p>	<ul style="list-style-type: none"> • CMOS level output ($I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$) • CMOS hysteresis input (with input shutdown in standby mode) • Automotive input (with input shutdown in standby mode)
G	 <p>The diagram shows a CMOS output stage with a P-channel MOSFET (P-ch) and an N-channel MOSFET (N-ch). The P-ch MOSFET is connected to the output terminal Pout, and the N-ch MOSFET is connected to the output terminal Nout. A pull-up resistor R is connected between the input and the P-ch MOSFET gate. A pull-up control resistor is connected between the input and the P-ch MOSFET drain. The input is connected to four logic blocks: a CMOS hysteresis input (two inverters), an Automotive input (two inverters), a TTL input (NAND gate and two inverters), and a Standby control for input shutdown (two inverters).</p>	<ul style="list-style-type: none"> • CMOS level output ($I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$) • CMOS hysteresis input (with input shutdown in standby mode) • Automotive input (with input shutdown in standby mode) • TTL input (with input shutdown in standby mode) • Programmable pull-up resistor: 50 kΩ approx.
H	 <p>The diagram shows a CMOS output stage with a P-channel MOSFET (P-ch) and an N-channel MOSFET (N-ch). The P-ch MOSFET is connected to the output terminal Pout, and the N-ch MOSFET is connected to the output terminal Nout. A pull-up resistor R is connected between the input and the P-ch MOSFET gate. The input is connected to three logic blocks: a CMOS hysteresis input (two inverters), an Automotive input (two inverters), and a Standby control for input shutdown (two inverters).</p>	<ul style="list-style-type: none"> • CMOS level output ($I_{OL} = 3 \text{ mA}$, $I_{OH} = -3 \text{ mA}$) • CMOS hysteresis input (with input shutdown in standby mode) • Automotive input (with input shutdown in standby mode)

(Continued)

MB90860E Series

Type	Circuit	Remarks
I		<ul style="list-style-type: none"> • CMOS level output ($I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$) • CMOS hysteresis input (with input shutdown in standby mode) • Automotive input (with input shutdown in standby mode) • A/D converter analog input
J		<ul style="list-style-type: none"> • CMOS level output ($I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$) • D/A analog output • CMOS hysteresis input (with input shutdown in standby mode) • Automotive input (with input shutdown in standby mode) • A/D converter analog input
K		Power supply input protection circuit
L		<ul style="list-style-type: none"> • A/D converter reference voltage power supply input pin with protection circuit • Flash devices do not have a protection circuit against V_{CC} for pin AVRH

(Continued)

(Continued)

Type	Circuit	Remarks
M	<p>The diagram shows a P-channel MOSFET (P-ch) and an N-channel MOSFET (N-ch) connected to a common output node. The gates of both MOSFETs are connected to a common input node. This input node is connected to a resistor R and a CMOS input. The CMOS input is connected to an Automotive input. A dashed box labeled 'Standby control for input shutdown' encloses the CMOS and Automotive input stages.</p>	<ul style="list-style-type: none"> • CMOS level output ($I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$) • CMOS input (with input shutdown in standby mode) • Automotive input (with input shutdown in standby mode)
N	<p>The diagram shows a P-channel MOSFET (P-ch) and an N-channel MOSFET (N-ch) connected to a common output node. The gates of both MOSFETs are connected to a common input node. This input node is connected to a pull-up control resistor, a resistor R, and CMOS, Automotive, and TTL inputs. A dashed box labeled 'Standby control for input shutdown' encloses the CMOS and Automotive input stages.</p>	<ul style="list-style-type: none"> • CMOS level output ($I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$) • CMOS input (with input shutdown in standby mode) • Automotive input (with input shutdown in standby mode) • TTL input (with input shutdown in standby mode) <p>Programmable pull-up resistor: 50 kΩ approx</p>
O	<p>The diagram shows a P-channel MOSFET (P-ch) and an N-channel MOSFET (N-ch) connected to a common output node. The gates of both MOSFETs are connected to a common input node. This input node is connected to a resistor R, CMOS, Automotive, and Analog inputs. A dashed box labeled 'Standby control for input shutdown' encloses the CMOS and Automotive input stages.</p>	<ul style="list-style-type: none"> • CMOS level output ($I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$) • CMOS input (with input shutdown in standby mode) • Automotive input (with input shutdown in standby mode) • A/D converter analog input

MB90860E Series

■ HANDLING DEVICES

1. Preventing latch-up

Latch-up may occur in a CMOS IC under the following conditions :

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} and V_{SS} pins.
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

Therefore, be very careful not to apply analog power-supply voltages in excess of the digital power-supply voltages.

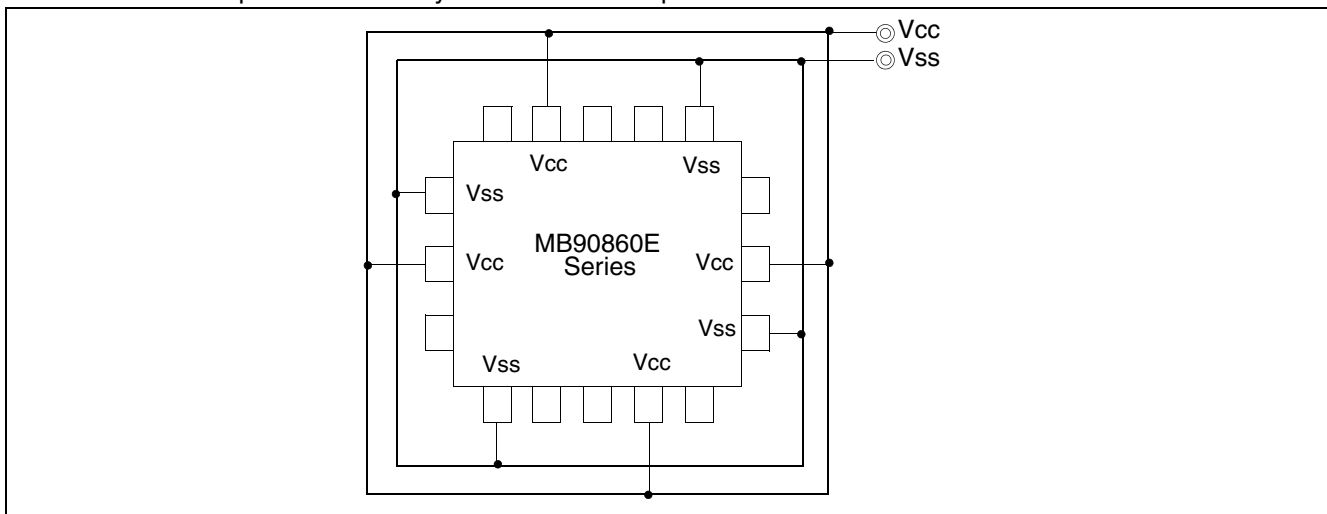
2. Handling unused pins

Leaving unused input pins open may cause malfunctions or permanent damages. Unused input pins must therefore be connected to a pull-up or pull-down resistor, with a resistance of 2 k Ω or more.

Unused bidirectional pins should be set to the output state and can then be left open, or set to the input state and handled as described above.

3. Power supply pins (V_{CC}/V_{SS})

- If there are multiple V_{CC} and V_{SS} pins, from the point of view of device design, pins to be of the same potential are connected the inside of the device to prevent such malfunctioning as latch up. To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the V_{CC} and V_{SS} pins to the power supply and ground externally. Connect V_{CC} and V_{SS} pins to the device from the current supply source at a low impedance.
- As a measure against power supply noise, connect a capacitor of about 0.1 μF as a bypass capacitor between V_{CC} and V_{SS} pins in the vicinity of V_{CC} and V_{SS} pins of the device.



4. Mode pins (MD0 to MD2)

Connect the mode pins directly to the V_{CC} or V_{SS} pins. To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the mode pins to V_{CC} or V_{SS} pins and to provide a low-impedance connection.

5. Sequence for turning on the A/D converter power supply and analog inputs

Make sure to turn on the A/D converter power supply (AV_{CC} , AV_{RH} , AV_{RL}) and analog inputs (AN0 to AN23) after turning on the digital power supply (V_{CC}).

Turn off the digital power after turning off the A/D converter power supply and analog inputs. In this case, make sure that the voltage does not exceed AV_{RH} or AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable).

6. Handling A/D converter pins when the A/D converter is not used

When the A/D converter is not used, connect the pins such that $AV_{CC} = V_{CC}$, $AV_{SS} = AV_{RH} = AV_{RL} = V_{SS}$.

7. Crystal oscillator circuit

Noise near the X0, X1, X0A, and X1A pins can cause the device to malfunction. Design the printed circuit board such that the crystal oscillators (or ceramic oscillators) are as close to the X0 and X1 pins, and X0A and X1A pins as possible, and that the bypass capacitor to ground is as close to the device as possible. Furthermore, try as much as possible to prevent the wiring for these components from crossing over the wiring of other circuitry.

It is highly recommended that the printed circuit board artwork is designed such that the X0, X1 pins and X0A, X1A pins are surrounded by ground plane, as this is expected to produce more stable operation.

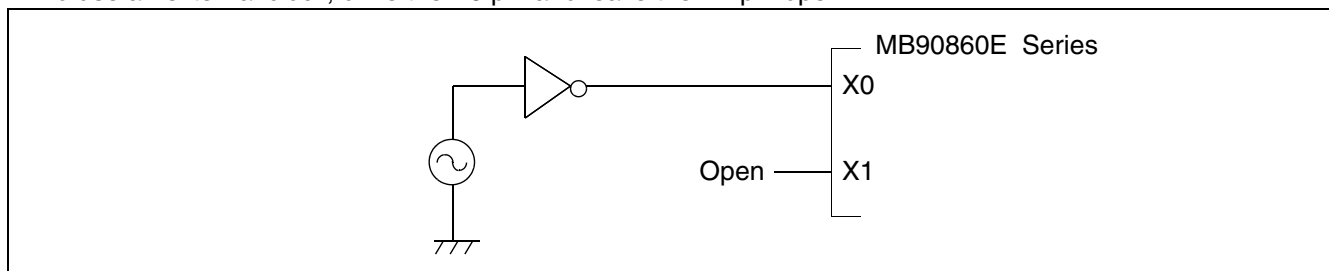
Please request the oscillator manufacturer to evaluate the oscillational characteristics of the crystal and this device.

8. Pull-up/down resistors

The MB90860E series does not support internal pull-up/down resistors (however, port 0 to port 3 have built-in pull-up resistors). Use external components where needed.

9. Using external clock

To use an external clock, drive the X0 pin and leave the X1 pin open.



10. Precautions when not using a sub clock signal

If you do not connect pins X0A and X1A to an oscillator, connect the X0A pin to a pull-down resistance and leave the X1A pin open.

11. Precautions when operating in PLL clock mode

In the MB90860E series, if the oscillator is disconnected or the clock input is stopped while operating in PLL mode, the microcontroller may continue to operate at the free-running frequency of the self-oscillating circuit contained in the PLL. However, operation under these circumstances is not guaranteed.

12. Precautions when turning the power on

To prevent the internal regulator circuit from malfunctioning, ensure that the time over which the voltage rises when the power is turned on is 50 or more μs (0.2 V to 2.7 V)

13. Stabilization of power supply voltage

A sudden change in the supply voltage may cause the device to malfunction even within the specified V_{CC} supply voltage operating range. Therefore, the V_{CC} supply voltage should be stabilized.

As a reference, stabilize the supply voltage by meeting the following standards.

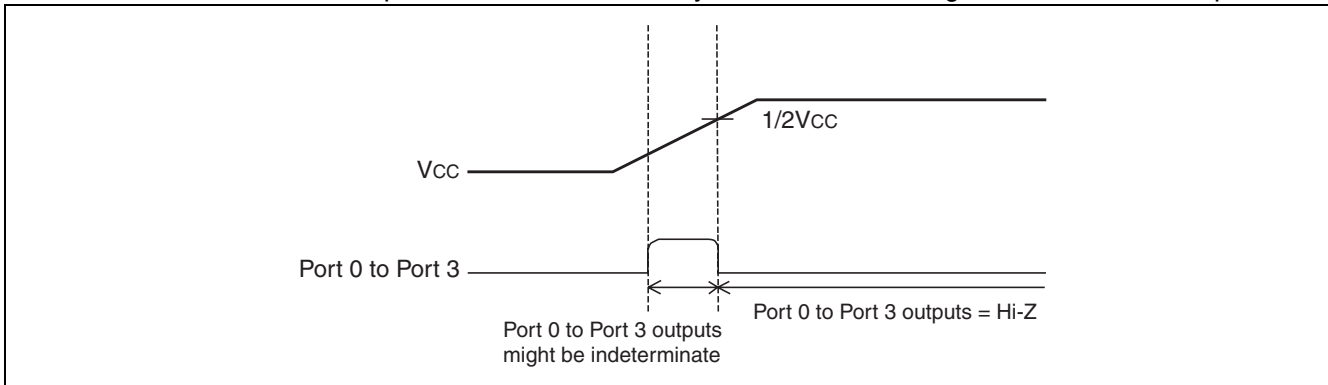
- V_{CC} ripple variations (peak-to-peak value) at commercial frequencies (50 Hz/60 Hz) fall below 10% of the standard V_{CC} supply voltage
- The coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

14. Initialization

The device has internal registers that are only initialized by a power-on reset only. To initialize these registers, turn on the power again.

15. Port 0 to port 3 output during power-on (external bus mode)

In external bus mode, the outputs of Port 0 to Port 3 may be indeterminate regardless of the reset input.



16. Flash security function

The security bit is located in the flash memory area. If protection code 01_H is written to the security bit, the security function is applied to the flash memory.

Therefore do not write 01_H to this address if you do not use the security function.

Please refer to following table for the address of the security bit.

	Flash memory size	Address of security bit
MB90F867E(S)	Embedded 1 Mbit Flash Memory	FE0001 _H

17. Serial communication

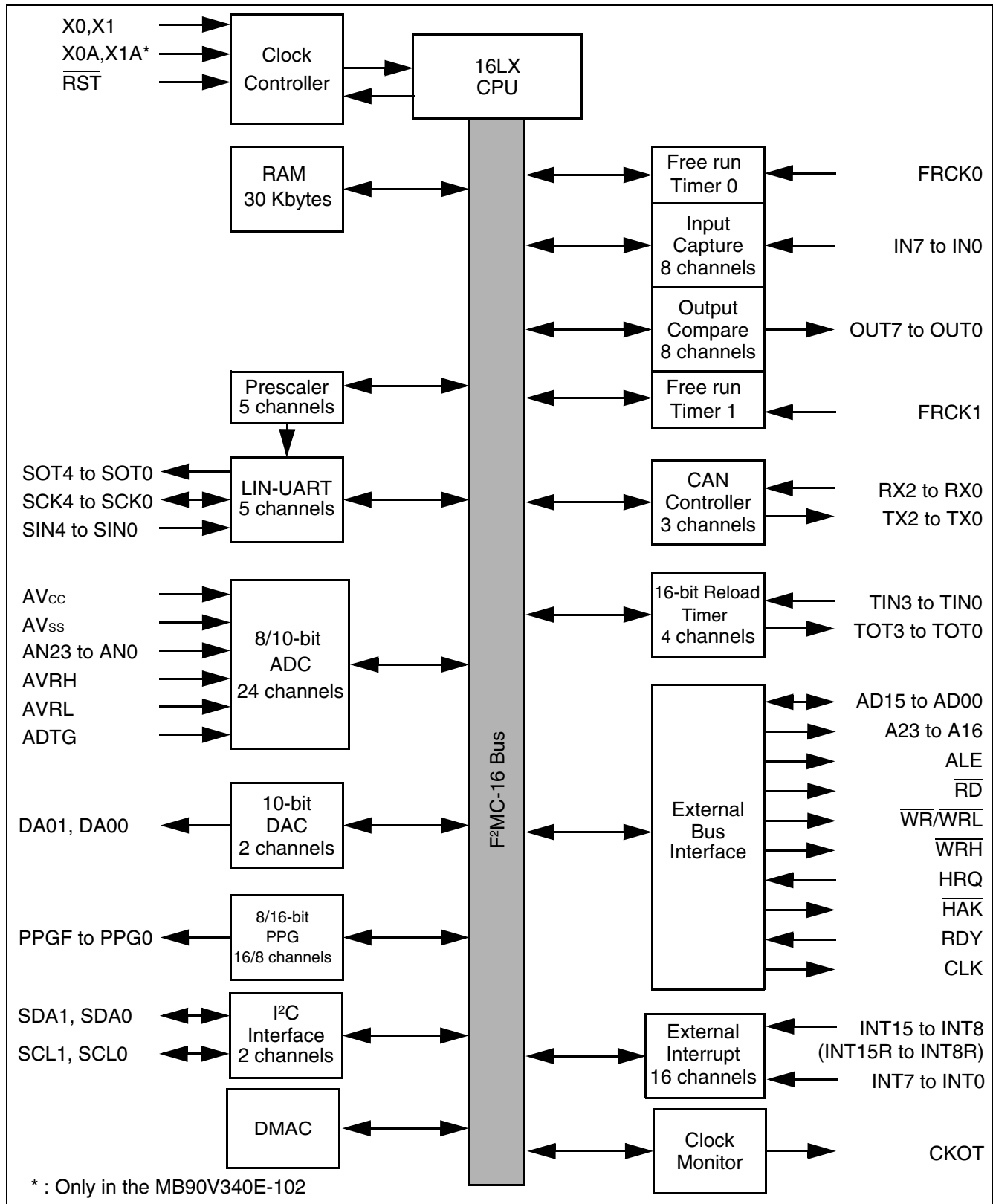
There is a possibility to receive wrong data due to the noise or other causes on the serial communication.

Therefore, design a printed circuit board so as to avoid noise.

Retransmit the data if an error occurs because of applying the checksum to the last data in consideration of receiving wrong data due to the noise.

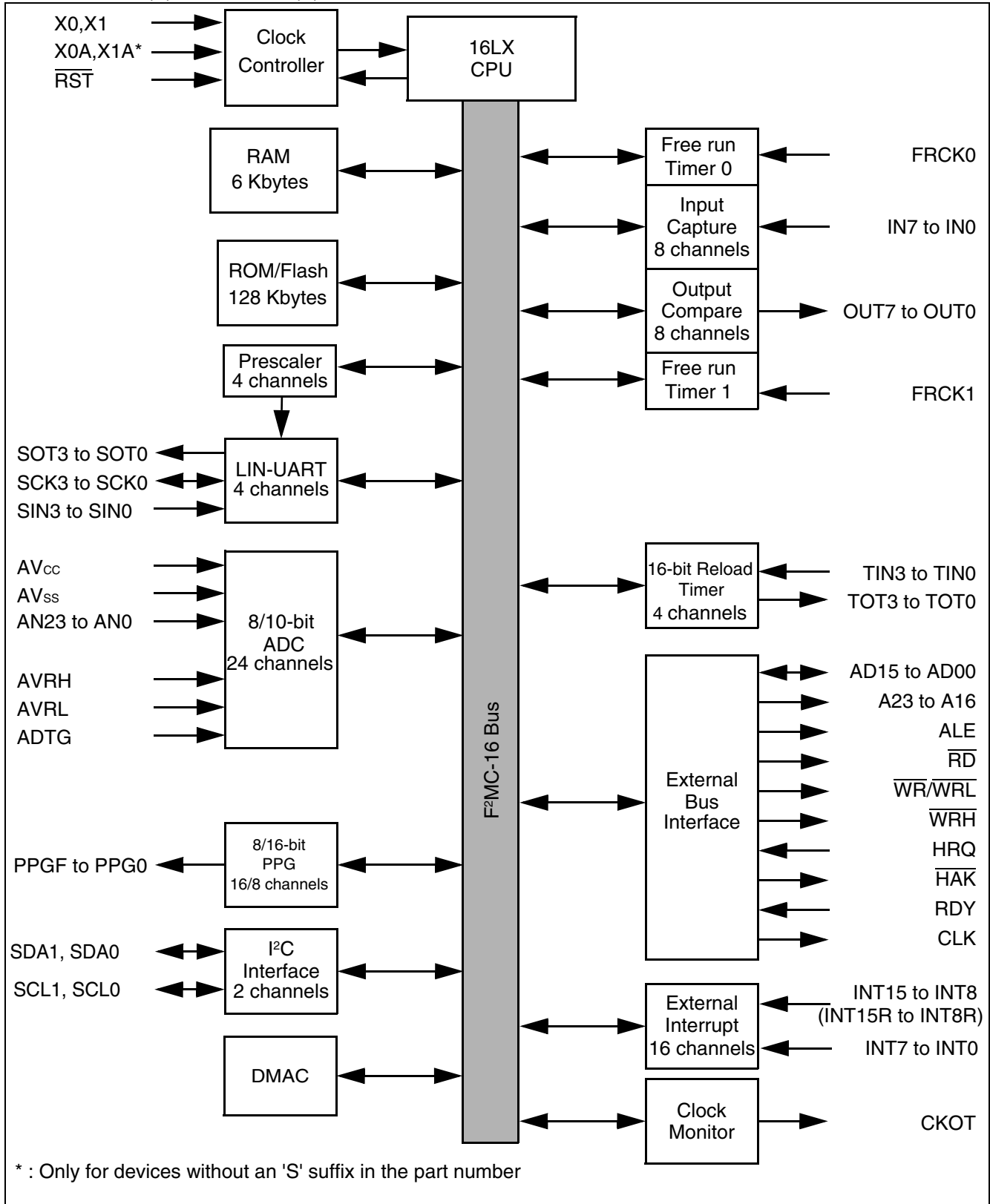
■ BLOCK DIAGRAMS

• MB90V340E-101/102

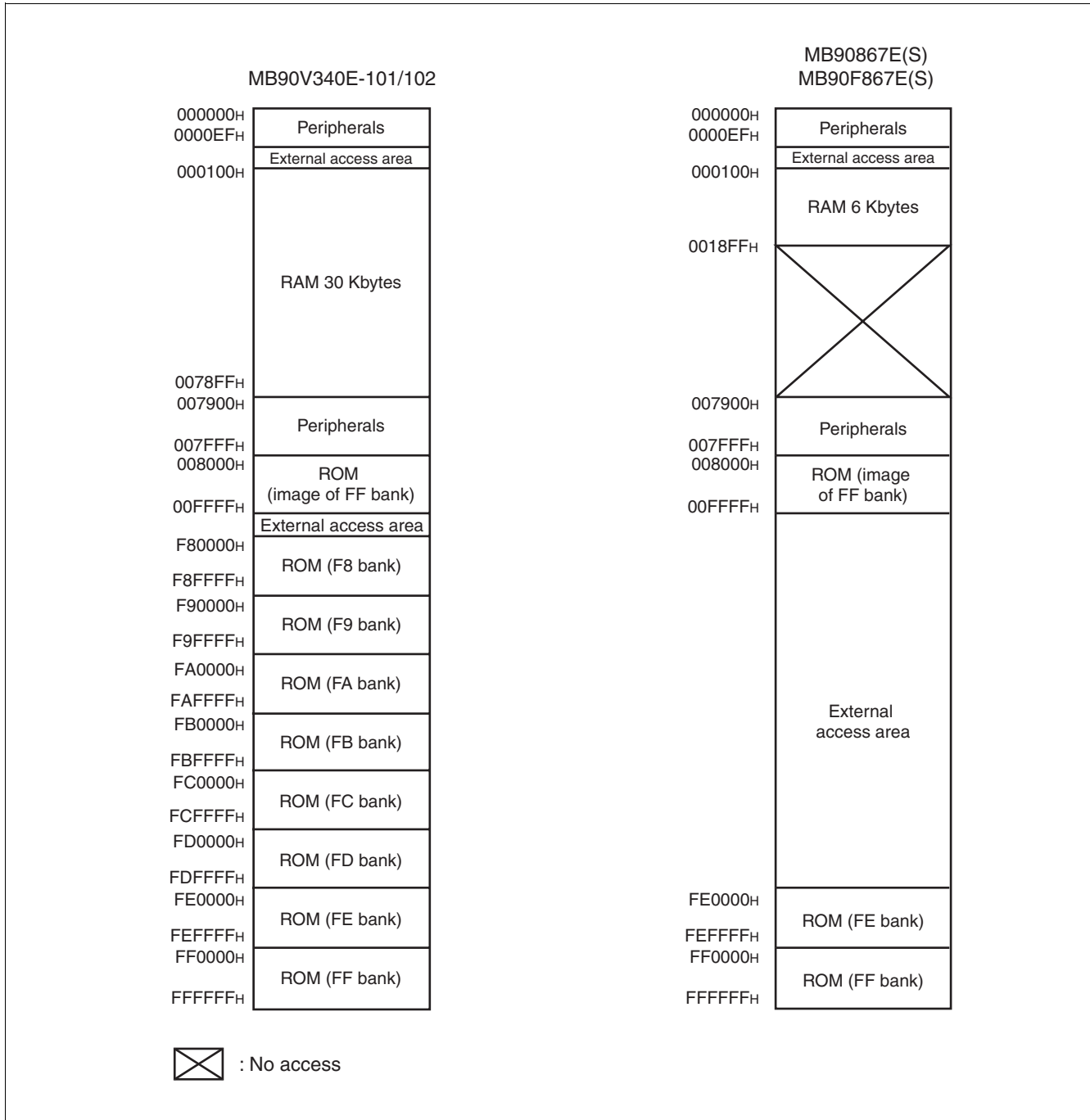


MB90860E Series

• MB90867E(S), MB90F867E(S)



■ MEMORY MAP



Note : An image of the FF bank ROM data is visible in the upper part of bank 00. This makes it possible to use the C compiler small memory model. Because the lower 16 bits of addresses in the 00 bank and the FF bank are the same, tables in ROM can be referenced without using the far specifier in the pointer declarations. For example, an attempt to access 00C000H accesses the value at FFC000H in ROM. The ROM area in bank FF exceeds 32 Kbytes, and therefore, the entire image is not visible in bank 00. The image between FF8000H and FFFFFFFH is visible in bank 00, while the image between FF0000H and FF7FFFH is visible only in bank FF.

MB90860E Series

■ I/O MAP

Address	Register	Abbreviation	Access	Resource name	Initial value
00000H	Port 0 Data Register	PDR0	R/W	Port 0	XXXXXXXX _B
00001H	Port 1 Data Register	PDR1	R/W	Port 1	XXXXXXXX _B
00002H	Port 2 Data Register	PDR2	R/W	Port 2	XXXXXXXX _B
00003H	Port 3 Data Register	PDR3	R/W	Port 3	XXXXXXXX _B
00004H	Port 4 Data Register	PDR4	R/W	Port 4	XXXXXXXX _B
00005H	Port 5 Data Register	PDR5	R/W	Port 5	XXXXXXXX _B
00006H	Port 6 Data Register	PDR6	R/W	Port 6	XXXXXXXX _B
00007H	Port 7 Data Register	PDR7	R/W	Port 7	XXXXXXXX _B
00008H	Port 8 Data Register	PDR8	R/W	Port 8	XXXXXXXX _B
00009H	Port 9 Data Register	PDR9	R/W	Port 9	XXXXXXXX _B
0000AH	Port A Data Register	PDRA	R/W	Port A	XXXXXXXX _B
0000BH	Port 5 Analog Input Enable Register	ADER5	R/W	Port 5, A/D	11111111 _B
0000CH	Port 6 Analog Input Enable Register	ADER6	R/W	Port 6, A/D	11111111 _B
0000DH	Port 7 Analog Input Enable Register	ADER7	R/W	Port 7, A/D	11111111 _B
0000EH	Input Level Select Register 0	ILSR0	R/W	Ports	XXXXXXXX _B
0000FH	Input Level Select Register 1	ILSR1	R/W	Ports	XXXX0XXX _B
00010H	Port 0 Direction Register	DDR0	R/W	Port 0	00000000 _B
00011H	Port 1 Direction Register	DDR1	R/W	Port 1	00000000 _B
00012H	Port 2 Direction Register	DDR2	R/W	Port 2	00000000 _B
00013H	Port 3 Direction Register	DDR3	R/W	Port 3	00000000 _B
00014H	Port 4 Direction Register	DDR4	R/W	Port 4	00000000 _B
00015H	Port 5 Direction Register	DDR5	R/W	Port 5	00000000 _B
00016H	Port 6 Direction Register	DDR6	R/W	Port 6	00000000 _B
00017H	Port 7 Direction Register	DDR7	R/W	Port 7	00000000 _B
00018H	Port 8 Direction Register	DDR8	R/W	Port 8	00000000 _B
00019H	Port 9 Direction Register	DDR9	R/W	Port 9	00000000 _B
0001AH	Port A Direction Register	DDRA	R/W	Port A	0000100 _B
0001BH	Reserved				
0001CH	Port 0 Pull-up Control Register	PUCR0	R/W	Port 0	00000000 _B
0001DH	Port 1 Pull-up Control Register	PUCR1	R/W	Port 1	00000000 _B
0001EH	Port 2 Pull-up Control Register	PUCR2	R/W	Port 2	00000000 _B
0001FH	Port 3 Pull-up Control Register	PUCR3	W, R/W	Port 3	00000000 _B

(Continued)

MB90860E Series

Address	Register	Abbreviation	Access	Resource name	Initial value
000020 _H	Serial Mode Register 0	SMR0	W,R/W	UART0	00000000 _B
000021 _H	Serial Control Register 0	SCR0	W,R/W		00000000 _B
000022 _H	Receive/Transmit Data Register 0	RDR0/ TDR0	R/W		00000000 _B
000023 _H	Serial Status Register 0	SSR0	R,R/W		00001000 _B
000024 _H	Extended Communication Control Register 0	ECCR0	R,W, R/W		000000XX _B
000025 _H	Extended Status/Control Register 0	ESCR0	R/W		00000100 _B
000026 _H	Baud Rate Generator Register 00	BGR00	R/W		00000000 _B
000027 _H	Baud Rate Generator Register 01	BGR01	R/W		00000000 _B
000028 _H	Serial Mode Register 1	SMR1	W,R/W	UART1	00000000 _B
000029 _H	Serial Control Register 1	SCR1	W,R/W		00000000 _B
00002A _H	Receive/Transmit Data Register 1	RDR1/ TDR1	R/W		00000000 _B
00002B _H	Serial Status Register 1	SSR1	R,R/W		00001000 _B
00002C _H	Extended Communication Control Register 1	ECCR1	R,W, R/W		000000XX _B
00002D _H	Extended Status/Control Register 1	ESCR1	R/W		00000100 _B
00002E _H	Baud Rate Generator Register 10	BGR10	R/W		00000000 _B
00002F _H	Baud Rate Generator Register 11	BGR11	R/W		00000000 _B
000030 _H	PPG 0 Operation Mode Control Register	PPGC0	W,R/W	16-bit PPG 0/1	0X000XX1 _B
000031 _H	PPG 1 Operation Mode Control Register	PPGC1	W,R/W		0X000001 _B
000032 _H	PPG 0/PPG 1 Count Clock Select Register	PPG01	R/W		000000X0 _B
000033 _H	Reserved				
000034 _H	PPG 2 Operation Mode Control Register	PPGC2	W,R/W	16-bit PPG 2/3	0X000XX1 _B
000035 _H	PPG 3 Operation Mode Control Register	PPGC3	W,R/W		0X000001 _B
000036 _H	PPG 2/PPG 3 Count Clock Select Register	PPG23	R/W		000000X0 _B
000037 _H	Reserved				
000038 _H	PPG 4 Operation Mode Control Register	PPGC4	W,R/W	16-bit PPG 4/5	0X000XX1 _B
000039 _H	PPG 5 Operation Mode Control Register	PPGC5	W,R/W		0X000001 _B
00003A _H	PPG 4/PPG 5 Clock Select Register	PPG45	R/W		000000X0 _B
00003B _H	Address Detect Control Register 1	PACSR1	R/W	Address Match Detection 1	00000000 _B
00003C _H	PPG 6 Operation Mode Control Register	PPGC6	W,R/W	16-bit PPG 6/7	0X000XX1 _B
00003D _H	PPG 7 Operation Mode Control Register	PPGC7	W,R/W		0X000001 _B
00003E _H	PPG 6/PPG 7 Count Clock Control Register	PPG67	R/W		000000X0 _B
00003F _H	Reserved				

(Continued)

MB90860E Series

Address	Register	Abbreviation	Access	Resource name	Initial value
000040 _H	PPG 8 Operation Mode Control Register	PPGC8	W,R/W	16-bit PPG 8/9	0X000XX1 _B
000041 _H	PPG 9 Operation Mode Control Register	PPGC9	W,R/W		0X000001 _B
000042 _H	PPG 8/PPG 9 Count Clock Control Register	PPG89	R/W		000000X0 _B
000043 _H	Reserved				
000044 _H	PPG A Operation Mode Control Register	PPGCA	W,R/W	16-bit PPG A/B	0X000XX1 _B
000045 _H	PPG B Operation Mode Control Register	PPGCB	W,R/W		0X000001 _B
000046 _H	PPG A/PPG B Count Clock Select Register	PPGAB	R/W		000000X0 _B
000047 _H	Reserved				
000048 _H	PPG C Operation Mode Control Register	PPGCC	W,R/W	16-bit PPG C/D	0X000XX1 _B
000049 _H	PPG D Operation Mode Control Register	PPGCD	W,R/W		0X000001 _B
00004A _H	PPG C/PPG D Count Clock Select Register	PPGCD	R/W		000000X0 _B
00004B _H	Reserved				
00004C _H	PPG E Operation Mode Control Register	PPGCE	W,R/W	16-bit PPG E/F	0X000XX1 _B
00004D _H	PPG F Operation Mode Control Register	PPGCF	W,R/W		0X000001 _B
00004E _H	PPG E/PPG F Count Clock Select Register	PPGEF	R/W		000000X0 _B
00004F _H	Reserved				
000050 _H	Input Capture Control Status 0/1	ICS01	R/W	Input Capture 0/1	00000000 _B
000051 _H	Input Capture Edge 0/1	ICE01	R/W, R		XXX0X0XX _B
000052 _H	Input Capture Control Status 2/3	ICS23	R/W	Input Capture 2/3	00000000 _B
000053 _H	Input Capture Edge 2/3	ICE23	R		XXXXXXXX _B
000054 _H	Input Capture Control Status 4/5	ICS45	R/W	Input Capture 4/5	00000000 _B
000055 _H	Input Capture Edge 4/5	ICE45	R		XXXXXXXX _B
000056 _H	Input Capture Control Status 6/7	ICS67	R/W	Input Capture 6/7	00000000 _B
000057 _H	Input Capture Edge 6/7	ICE67	R/W, R		XXX000XX _B
000058 _H	Output Compare Control Status 0	OCS0	R/W	Output Compare 0/1	0000XX00 _B
000059 _H	Output Compare Control Status 1	OCS1	R/W		0XX00000 _B
00005A _H	Output Compare Control Status 2	OCS2	R/W	Output Compare 2/3	0000XX00 _B
00005B _H	Output Compare Control Status 3	OCS3	R/W		0XX00000 _B
00005C _H	Output Compare Control Status 4	OCS4	R/W	Output Compare 4/5	0000XX00 _B
00005D _H	Output Compare Control Status 5	OCS5	R/W		0XX00000 _B
00005E _H	Output Compare Control Status 6	OCS6	R/W	Output Compare 6/7	0000XX00 _B
00005F _H	Output Compare Control Status 7	OCS7	R/W		0XX00000 _B

(Continued)

MB90860E Series

Address	Register	Abbreviation	Access	Resource name	Initial value
000060 _H	Timer Control Status 0	TMCSR0	R/W	16-bit Reload Timer 0	00000000 _B
000061 _H	Timer Control Status 0	TMCSR0	R/W		XXXX0000 _B
000062 _H	Timer Control Status 1	TMCSR1	R/W	16-bit Reload Timer 1	00000000 _B
000063 _H	Timer Control Status 1	TMCSR1	R/W		XXXX0000 _B
000064 _H	Timer Control Status 2	TMCSR2	R/W	16-bit Reload Timer 2	00000000 _B
000065 _H	Timer Control Status 2	TMCSR2	R/W		XXXX0000 _B
000066 _H	Timer Control Status 3	TMCSR3	R/W	16-bit Reload Timer 3	00000000 _B
000067 _H	Timer Control Status 3	TMCSR3	R/W		XXXX0000 _B
000068 _H	A/D Control Status 0	ADCS0	R/W	A/D Converter	000XXXX0 _B
000069 _H	A/D Control Status 1	ADCS1	R/W		0000000X _B
00006A _H	A/D Data 0	ADCR0	R		00000000 _B
00006B _H	A/D Data 1	ADCR1	R		XXXXXXXX00 _B
00006C _H	ADC Setting 0	ADSR0	R/W		00000000 _B
00006D _H	ADC Setting 1	ADSR1	R/W		00000000 _B
00006E _H	Reserved				
00006F _H	ROM Mirror Function Select	ROMM	W	ROM Mirror	XXXXXXXX1 _B
000070 _H to 00009A _H	Reserved				
00009B _H	DMA Descriptor Channel Selection Register	DCSR	R/W	DMA	00000000 _B
00009C _H	DMA Status L Register	DSRL	R/W		00000000 _B
00009D _H	DMA Status H Register	DSRH	R/W		00000000 _B
00009E _H	Address Detect Control Register 0	PACSR0	R/W	Address Match Detection 0	00000000 _B
00009F _H	Delayed Interrupt Source Generate/ Release Register	DIRR	R/W	Delayed Interrupt	XXXXXXXX0 _B
0000A0 _H	Low-power Mode Control Register	LPMCR	W,R/W	Low Power Control Circuit	00011000 _B
0000A1 _H	Clock Selection Register	CKSCR	R,R/W	Low Power Control Circuit	11111100 _B
0000A2 _H , 0000A3 _H	Reserved				
0000A4 _H	DMA Stop Status Register	DSSR	R/W	DMA	00000000 _B
0000A5 _H	Automatic Ready Function Select Register	ARSR	W	External Memory Access	0011XX00 _B
0000A6 _H	External Address Output Control Register	HACR	W		00000000 _B
0000A7 _H	Bus Control Signal Selection Register	ECSR	W		0000000X _B

(Continued)

MB90860E Series

Address	Register	Abbreviation	Access	Resource name	Initial value
0000A8 _H	Watchdog Control Register	WDTC	R,W	Watchdog Timer	XXXXX111 _B
0000A9 _H	Time Base Timer Control Register	TBTC	W,R/W	Time Base Timer	1XX00100 _B
0000AA _H	Watch Timer Control Register	WTC	R,R/W	Watch Timer	1X001000 _B
0000AB _H	Reserved				
0000AC _H	DMA Enable L Register	DERL	R/W	DMA	00000000 _B
0000AD _H	DMA Enable H Register	DERH	R/W		00000000 _B
0000AE _H	Flash Control Status Register (Flash Devices only. Otherwise reserved)	FMCS	R,R/W	Flash Memory	000X0000 _B
0000AF _H	Reserved				
0000B0 _H	Interrupt Control Register 00	ICR00	W,R/W	Interrupt Control	00000111 _B
0000B1 _H	Interrupt Control Register 01	ICR01	W,R/W		00000111 _B
0000B2 _H	Interrupt Control Register 02	ICR02	W,R/W		00000111 _B
0000B3 _H	Interrupt Control Register 03	ICR03	W,R/W		00000111 _B
0000B4 _H	Interrupt Control Register 04	ICR04	W,R/W		00000111 _B
0000B5 _H	Interrupt Control Register 05	ICR05	W,R/W		00000111 _B
0000B6 _H	Interrupt Control Register 06	ICR06	W,R/W		00000111 _B
0000B7 _H	Interrupt Control Register 07	ICR07	W,R/W		00000111 _B
0000B8 _H	Interrupt Control Register 08	ICR08	W,R/W		00000111 _B
0000B9 _H	Interrupt Control Register 09	ICR09	W,R/W		00000111 _B
0000BA _H	Interrupt Control Register 10	ICR10	W,R/W		00000111 _B
0000BB _H	Interrupt Control Register 11	ICR11	W,R/W		00000111 _B
0000BC _H	Interrupt Control Register 12	ICR12	W,R/W		00000111 _B
0000BD _H	Interrupt Control Register 13	ICR13	W,R/W		00000111 _B
0000BE _H	Interrupt Control Register 14	ICR14	W,R/W		00000111 _B
0000BF _H	Interrupt Control Register 15	ICR15	W,R/W		00000111 _B
0000C0 _H	D/A Converter Data 0 Register	DAT0	R/W	D/A Converter	XXXXXXXX _B
0000C1 _H	D/A Converter Data 1 Register	DAT1	R/W		XXXXXXXX _B
0000C2 _H	D/A Control 0 Register	DACR0	R/W		XXXXXXXX0 _B
0000C3 _H	D/A Control 1 Register	DACR1	R/W		XXXXXXXX0 _B
0000C4 _H , 0000C5 _H	Reserved				
0000C6 _H	External Interrupt Enable 0	ENIR0	R/W	External Interrupt 0	00000000 _B
0000C7 _H	External Interrupt Source 0	EIRR0	R/W		XXXXXXXX _B
0000C8 _H	External Interrupt Level Setting 0	ELVR0	R/W		00000000 _B
0000C9 _H	External Interrupt Level Setting 0	ELVR0	R/W		00000000 _B

(Continued)

MB90860E Series

Address	Register	Abbrevia- tion	Access	Resource name	Initial value
0000CA _H	External Interrupt Enable 1	ENIR1	R/W	External Interrupt 1	00000000 _B
0000CB _H	External Interrupt Source 1	EIRR1	R/W		XXXXXXXX _B
0000CC _H	External Interrupt Level Setting 1	ELVR1	R/W		00000000 _B
0000CD _H	External Interrupt Level Setting 1	ELVR1	R/W		00000000 _B
0000CE _H	External Interrupt Source Select	EISSR	R/W		00000000 _B
0000CF _H	PLL/Sub Clock Control Register	PSCCR	W	PLL	XXXX0000 _B
0000D0 _H	DMA Buffer Address Pointer L Register	BAPL	R/W	DMA	XXXXXXXX _B
0000D1 _H	DMA Buffer Address Pointer M Register	BAPM	R/W		XXXXXXXX _B
0000D2 _H	DMA Buffer Address Pointer H Register	BAPH	R/W		XXXXXXXX _B
0000D3 _H	DMA Control Register	DMACS	R/W		XXXXXXXX _B
0000D4 _H	I/O Register Address Pointer L Register	IOAL	R/W		XXXXXXXX _B
0000D5 _H	I/O Register Address Pointer H Register	IOAH	R/W		XXXXXXXX _B
0000D6 _H	Data Counter L Register	DCTL	R/W		XXXXXXXX _B
0000D7 _H	Data Counter H Register	DCTH	R/W		XXXXXXXX _B
0000D8 _H	Serial Mode Register 2	SMR2	W,R/W	UART2	00000000 _B
0000D9 _H	Serial Control Register 2	SCR2	W,R/W		00000000 _B
0000DA _H	Receive/Transmit Data Register 2	RDR2/ TDR2	R/W		00000000 _B
0000DB _H	Serial Status Register 2	SSR2	R,R/W		00001000 _B
0000DC _H	Extended Communication Control Register 2	ECCR2	R,W, R/W		000000XX _B
0000DD _H	Extended Status Control Register 2	ESCR2	R/W		00000100 _B
0000DE _H	Baud Rate Generator Register 20	BGR20	R/W		00000000 _B
0000DF _H	Baud Rate Generator Register 21	BGR21	R/W		00000000 _B
0000E0 _H to 0000FF _H	External area				
007900 _H	Reload Register L0	PRL0	R/W	16-bit PPG 0/1	XXXXXXXX _B
007901 _H	Reload Register H0	PRLH0	R/W		XXXXXXXX _B
007902 _H	Reload Register L1	PRL1	R/W		XXXXXXXX _B
007903 _H	Reload Register H1	PRLH1	R/W		XXXXXXXX _B
007904 _H	Reload Register L2	PRL2	R/W	16-bit PPG 2/3	XXXXXXXX _B
007905 _H	Reload Register H2	PRLH2	R/W		XXXXXXXX _B
007906 _H	Reload Register L3	PRL3	R/W		XXXXXXXX _B
007907 _H	Reload Register H3	PRLH3	R/W		XXXXXXXX _B

(Continued)

MB90860E Series

Address	Register	Abbreviation	Access	Resource name	Initial value
007908 _H	Reload Register L4	PRL4	R/W	16-bit PPG 4/5	XXXXXXXX _B
007909 _H	Reload Register H4	PRLH4	R/W		XXXXXXXX _B
00790A _H	Reload Register L5	PRL5	R/W		XXXXXXXX _B
00790B _H	Reload Register H5	PRLH5	R/W		XXXXXXXX _B
00790C _H	Reload Register L6	PRL6	R/W	16-bit PPG 6/7	XXXXXXXX _B
00790D _H	Reload Register H6	PRLH6	R/W		XXXXXXXX _B
00790E _H	Reload Register L7	PRL7	R/W		XXXXXXXX _B
00790F _H	Reload Register H7	PRLH7	R/W		XXXXXXXX _B
007910 _H	Reload Register L8	PRL8	R/W	16-bit PPG 8/9	XXXXXXXX _B
007911 _H	Reload Register H8	PRLH8	R/W		XXXXXXXX _B
007912 _H	Reload Register L9	PRL9	R/W		XXXXXXXX _B
007913 _H	Reload Register H9	PRLH9	R/W		XXXXXXXX _B
007914 _H	Reload Register LA	PRLA	R/W	16-bit PPG A/B	XXXXXXXX _B
007915 _H	Reload Register HA	PRLHA	R/W		XXXXXXXX _B
007916 _H	Reload Register LB	PRLB	R/W		XXXXXXXX _B
007917 _H	Reload Register HB	PRLHB	R/W		XXXXXXXX _B
007918 _H	Reload Register LC	PRLC	R/W	16-bit PPG C/D	XXXXXXXX _B
007919 _H	Reload Register HC	PRLHC	R/W		XXXXXXXX _B
00791A _H	Reload Register LD	PRLD	R/W		XXXXXXXX _B
00791B _H	Reload Register HD	PRLHD	R/W		XXXXXXXX _B
00791C _H	Reload Register LE	PRLLE	R/W	16-bit PPG E/F	XXXXXXXX _B
00791D _H	Reload Register HE	PRLHE	R/W		XXXXXXXX _B
00791E _H	Reload Register LF	PRLLE	R/W		XXXXXXXX _B
00791F _H	Reload Register HF	PRLHF	R/W		XXXXXXXX _B
007920 _H	Input Capture 0	IPCP0	R	Input Capture 0/1	XXXXXXXX _B
007921 _H	Input Capture 0	IPCP0	R		XXXXXXXX _B
007922 _H	Input Capture 1	IPCP1	R		XXXXXXXX _B
007923 _H	Input Capture 1	IPCP1	R		XXXXXXXX _B
007924 _H	Input Capture 2	IPCP2	R	Input Capture 2/3	XXXXXXXX _B
007925 _H	Input Capture 2	IPCP2	R		XXXXXXXX _B
007926 _H	Input Capture 3	IPCP3	R		XXXXXXXX _B
007927 _H	Input Capture 3	IPCP3	R		XXXXXXXX _B
007928 _H	Input Capture 4	IPCP4	R	Input Capture 4/5	XXXXXXXX _B
007929 _H	Input Capture 4	IPCP4	R		XXXXXXXX _B
00792A _H	Input Capture 5	IPCP5	R		XXXXXXXX _B
00792B _H	Input Capture 5	IPCP5	R		XXXXXXXX _B

(Continued)

MB90860E Series

Address	Register	Abbreviation	Access	Resource name	Initial value
00792C _H	Input Capture 6	IPCP6	R	Input Capture 6/7	XXXXXXXX _B
00792D _H	Input Capture 6	IPCP6	R		XXXXXXXX _B
00792E _H	Input Capture 7	IPCP7	R		XXXXXXXX _B
00792F _H	Input Capture 7	IPCP7	R		XXXXXXXX _B
007930 _H	Output Compare 0	OCCP0	R/W	Output Compare 0/1	XXXXXXXX _B
007931 _H	Output Compare 0	OCCP0	R/W		XXXXXXXX _B
007932 _H	Output Compare 1	OCCP1	R/W		XXXXXXXX _B
007933 _H	Output Compare 1	OCCP1	R/W		XXXXXXXX _B
007934 _H	Output Compare 2	OCCP2	R/W	Output Compare 2/3	XXXXXXXX _B
007935 _H	Output Compare 2	OCCP2	R/W		XXXXXXXX _B
007936 _H	Output Compare 3	OCCP3	R/W		XXXXXXXX _B
007937 _H	Output Compare 3	OCCP3	R/W		XXXXXXXX _B
007938 _H	Output Compare 4	OCCP4	R/W	Output Compare 4/5	XXXXXXXX _B
007939 _H	Output Compare 4	OCCP4	R/W		XXXXXXXX _B
00793A _H	Output Compare 5	OCCP5	R/W		XXXXXXXX _B
00793B _H	Output Compare 5	OCCP5	R/W		XXXXXXXX _B
00793C _H	Output Compare 6	OCCP6	R/W	Output Compare 6/7	XXXXXXXX _B
00793D _H	Output Compare 6	OCCP6	R/W		XXXXXXXX _B
00793E _H	Output Compare 7	OCCP7	R/W		XXXXXXXX _B
00793F _H	Output Compare 7	OCCP7	R/W		XXXXXXXX _B
007940 _H	Timer Data 0	TCDT0	R/W	Free-run Timer 0	00000000 _B
007941 _H	Timer Data 0	TCDT0	R/W		00000000 _B
007942 _H	Timer Control Status 0	TCCSL0	R/W		00000000 _B
007943 _H	Timer Control Status 0	TCCSH0	R/W		0XXXXXXXX _B
007944 _H	Timer Data 1	TCDT1	R/W	Free-run Timer 1	00000000 _B
007945 _H	Timer Data 1	TCDT1	R/W		00000000 _B
007946 _H	Timer Control Status 1	TCCSL1	R/W		00000000 _B
007947 _H	Timer Control Status 1	TCCSH1	R/W		0XXXXXXXX _B
007948 _H	Timer 0/Reload 0	TMR0/	R/W	16-bit Reload Timer 0	XXXXXXXX _B
007949 _H		TMRLR0	R/W		XXXXXXXX _B
00794A _H	Timer 1/Reload 1	TMR1/	R/W	16-bit Reload Timer 1	XXXXXXXX _B
00794B _H		TMRLR1	R/W		XXXXXXXX _B
00794C _H	Timer 2/Reload 2	TMR2/	R/W	16-bit Reload Timer 2	XXXXXXXX _B
00794D _H		TMRLR2	R/W		XXXXXXXX _B
00794E _H	Timer 3/Reload 3	TMR3/	R/W	16-bit Reload Timer 3	XXXXXXXX _B
00794F _H		TMRLR3	R/W		XXXXXXXX _B

(Continued)

MB90860E Series

Address	Register	Abbreviation	Access	Resource name	Initial value
007950 _H	Serial Mode Register 3	SMR3	W,R/W	UART3	00000000 _B
007951 _H	Serial Control Register 3	SCR3	W,R/W		00000000 _B
007952 _H	Receive/Transmit Data Register 3	RDR3/ TDR3	R/W		00000000 _B
007953 _H	Serial Status Register 3	SSR3	R,R/W		00001000 _B
007954 _H	Extended Communication Control Register 3	ECCR3	R,W, R/W		000000XX _B
007955 _H	Extended Status Control Register	ESCR3	R/W		00000100 _B
007956 _H	Baud Rate Generator Register 30	BGR30	R/W		00000000 _B
007957 _H	Baud Rate Generator Register 31	BGR31	R/W		00000000 _B
007958 _H	Serial Mode Register 4	SMR4	W,R/W	UART4	00000000 _B
007959 _H	Serial Control Register 4	SCR4	W,R/W		00000000 _B
00795A _H	Receive/Transmit Data Register 4	RDR4/ TDR4	R/W		00000000 _B
00795B _H	Serial Status Register 4	SSR4	R,R/W		00001000 _B
00795C _H	Extended Communication Control Register 4	ECCR4	R,W, R/W		000000XX _B
00795D _H	Extended Status Control Register	ESCR4	R/W		00000100 _B
00795E _H	Baud Rate Generator Register 40	BGR40	R/W		00000000 _B
00795F _H	Baud Rate Generator Register 41	BGR41	R/W		00000000 _B
007960 _H to 00796B _H	Reserved				
00796C _H	Clock Output Enable Register	CLKR	R/W	Clock Monitor	XXXX0000 _B
00796D _H to 00796F _H	Reserved				
007970 _H	I ² C Bus Status Register 0	IBSR0	R	I ² C Interface 0	00000000 _B
007971 _H	I ² C bus Control Register 0	IBCR0	W,R/W		00000000 _B
007972 _H	I ² C 10-bit Slave Address Register 0	ITBAL0	R/W		00000000 _B
007973 _H		ITBAH0	R/W		00000000 _B
007974 _H	I ² C 10-bit Slave Address Mask Register 0	ITMKL0	R/W		11111111 _B
007975 _H		ITMKH0	R/W		00111111 _B
007976 _H	I ² C 7-bit Slave Address Register 0	ISBA0	R/W		00000000 _B
007977 _H	I ² C 7-bit Slave Address Mask Register 0	ISMK0	R/W		01111111 _B
007978 _H	I ² C Data Register 0	IDAR0	R/W	00000000 _B	
007979 _H , 00797A _H	Reserved				

(Continued)

MB90860E Series

Address	Register	Abbreviation	Access	Resource name	Initial value
00797B _H	I ² C Clock Control Register 0	ICCR0	R/W	I ² C Interface 0	00011111 _B
00797C _H to 00797F _H	Reserved				
007980 _H	I ² C Bus Status Register 1	IBSR1	R	I ² C Interface 1	00000000 _B
007981 _H	I ² C Bus Control Register 1	IBCR1	W,R/W		00000000 _B
007982 _H	I ² C 10-bit Slave Address Register 1	ITBAL1	R/W		00000000 _B
007983 _H		ITBAH1	R/W		00000000 _B
007984 _H	I ² C 10-bit Slave Address Mask Register 1	ITMKL1	R/W		11111111 _B
007985 _H		ITMKH1	R/W		00111111 _B
007986 _H	I ² C 7-bit Slave Address Register 1	ISBA1	R/W		00000000 _B
007987 _H	I ² C 7-bit Slave Address Mask Register 1	ISMK1	R/W		01111111 _B
007988 _H	I ² C Data Register 1	IDAR1	R/W		00000000 _B
007989 _H , 00798A _H	Reserved				
00798B _H	I ² C Clock Control Register 1	ICCR1	R/W	I ² C Interface 1	00011111 _B
00798C _H to 0079C1 _H	Reserved				
0079C2 _H	Clock Modulator Control Register	CMCR	R, R/W	Clock Modulator	0001X000 _B
0079C3 _H to 0079DF _H	Reserved				
0079E0 _H	Detect Address Setting 0	PADR0	R/W	Address Match Detection 0	XXXXXXXX _B
0079E1 _H	Detect Address Setting 0	PADR0	R/W		XXXXXXXX _B
0079E2 _H	Detect Address Setting 0	PADR0	R/W		XXXXXXXX _B
0079E3 _H	Detect Address Setting 1	PADR1	R/W		XXXXXXXX _B
0079E4 _H	Detect Address Setting 1	PADR1	R/W		XXXXXXXX _B
0079E5 _H	Detect Address Setting 1	PADR1	R/W		XXXXXXXX _B
0079E6 _H	Detect Address Setting 2	PADR2	R/W		XXXXXXXX _B
0079E7 _H	Detect Address Setting 2	PADR2	R/W		XXXXXXXX _B
0079E8 _H	Detect Address Setting 2	PADR2	R/W		XXXXXXXX _B
0079E9 _H to 0079EF _H	Reserved				

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MB90860E Series

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Address	Register	Abbrevia- tion	Access	Resource name	Initial value
0079F0 _H	Detect Address Setting 3	PADR3	R/W	Address Match Detection 1	XXXXXXXX _B
0079F1 _H	Detect Address Setting 3	PADR3	R/W		XXXXXXXX _B
0079F2 _H	Detect Address Setting 3	PADR3	R/W		XXXXXXXX _B
0079F3 _H	Detect Address Setting 4	PADR4	R/W		XXXXXXXX _B
0079F4 _H	Detect Address Setting 4	PADR4	R/W		XXXXXXXX _B
0079F5 _H	Detect Address Setting 4	PADR4	R/W		XXXXXXXX _B
0079F6 _H	Detect Address Setting 5	PADR5	R/W		XXXXXXXX _B
0079F7 _H	Detect Address Setting 5	PADR5	R/W		XXXXXXXX _B
0079F8 _H	Detect Address Setting 5	PADR5	R/W		XXXXXXXX _B
0079F9 _H to 007FFF _H	Reserved				

- Notes :
- Initial value of “X” represents undefined value.
 - Do not write to the reserved areas in the I/O map. Reading from reserved addresses will return undefined values.

■ INTERRUPT SOURCES, INTERRUPT VECTORS, INTERRUPT CONTROL REGISTER

Interrupt source	EI ² OS clear	DMA ch number	Interrupt vector		Interrupt control register	
			Number	Address	Number	Address
Reset	N	—	#08	FFFFDC _H	—	—
INT9 instruction	N	—	#09	FFFFD8 _H	—	—
Exception	N	—	#10	FFFFD4 _H	—	—
(Reserved)	N	—	#11	FFFFD0 _H	ICR00	0000B0 _H
(Reserved)	N	—	#12	FFFFCC _H		
Input Capture 6	Y1	—	#13	FFFFC8 _H	ICR01	0000B1 _H
Input Capture 7	Y1	—	#14	FFFFC4 _H		
I ² C0	N	—	#15	FFFFC0 _H	ICR02	0000B2 _H
(Reserved)	N	—	#16	FFFFBC _H		
16-bit Reload Timer 0	Y1	0	#17	FFFFB8 _H	ICR03	0000B3 _H
16-bit Reload Timer 1	Y1	1	#18	FFFFB4 _H		
16-bit Reload Timer 2	Y1	2	#19	FFFFB0 _H	ICR04	0000B4 _H
16-bit Reload Timer 3	Y1	—	#20	FFFFAC _H		
PPG 0/1/4/5	N	—	#21	FFFFA8 _H	ICR05	0000B5 _H
PPG 2/3/6/7	N	—	#22	FFFFA4 _H		
PPG 8/9/C/D	N	—	#23	FFFFA0 _H	ICR06	0000B6 _H
PPG A/B/E/F	N	—	#24	FFFF9C _H		
Time Base Timer	N	—	#25	FFFF98 _H	ICR07	0000B7 _H
External Interrupt 0 to 3, 8 to 11	Y1	3	#26	FFFF94 _H		
Watch Timer	N	—	#27	FFFF90 _H	ICR08	0000B8 _H
External Interrupt 4 to 7, 12 to 15	Y1	4	#28	FFFF8C _H		
8/10-bit A/D Converter	Y1	5	#29	FFFF88 _H	ICR09	0000B9 _H
Free-run Timer 0, Free-run Timer 1	N	—	#30	FFFF84 _H		
Input Capture 4/5, I ² C1	Y1	6	#31	FFFF80 _H	ICR10	0000BA _H
Output Compare 0/1/4/5	Y1	7	#32	FFFF7C _H		
Input Capture 0 to 3	Y1	8	#33	FFFF78 _H	ICR11	0000BB _H
Output Compare 2/3/6/7	Y1	9	#34	FFFF74 _H		
UART 0 Reception	Y2	10	#35	FFFF70 _H	ICR12	0000BC _H
UART 0 Transmission	Y1	11	#36	FFFF6C _H		
UART 1 Reception / UART 3 Reception	Y2	12	#37	FFFF68 _H	ICR13	0000BD _H
UART 1 Transmission / UART 3 Transmission	Y1	13	#38	FFFF64 _H		

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MB90860E Series

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Interrupt source	EI ² OS clear	DMA ch number	Interrupt vector		Interrupt control register	
			Number	Address	Number	Address
UART 2 Reception / UART 4 Reception	Y2	14	#39	FFFF60 _H	ICR14	0000BE _H
UART 2 Transmission / UART 4 Transmission	Y1	15	#40	FFFF5C _H		
Flash Memory	N	—	#41	FFFF58 _H	ICR15	0000BF _H
Delayed interrupt	N	—	#42	FFFF54 _H		

Y1 : Usable

Y2 : Usable, with EI²OS stop function

N : Unusable

- Notes :
- Peripheral resources that share an ICR register have the same interrupt level.
 - When two peripheral resources share an ICR register, only one can use Extended Intelligent I/O Service at a time.
 - When either of the two peripheral resources sharing an ICR register specifies Extended Intelligent I/O Service, the other one cannot use interrupts.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	
	AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$V_{CC} = AV_{CC}$ *2
	AV_{RH} , AV_{RL}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$AV_{CC} \geq AV_{RH}$, $AV_{CC} \geq AV_{RL}$, $AV_{RH} \geq AV_{RL}$
Input voltage*1	V_I	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*3
Output voltage*1	V_O	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*3
Maximum clamp current	I_{CLAMP}	-4.0	+4.0	mA	*5
Total maximum clamp current	$\Sigma I_{CLAMP} $	—	40	mA	*5
“L” level maximum output current	I_{OL}	—	15	mA	*4
“L” level average output current	I_{OLAV}	—	4	mA	*4
“L” level maximum overall output current	ΣI_{OL}	—	100	mA	*4
“L” level average overall output current	ΣI_{OLAV}	—	50	mA	*4
“H” level maximum output current	I_{OH}	—	-15	mA	*4
“H” level average output current	I_{OHAV}	—	-4	mA	*4
“H” level maximum overall output current	ΣI_{OH}	—	-100	mA	*4
“H” level average overall output current	ΣI_{OHAV}	—	-50	mA	*4
Power consumption	P_D	—	340	mW	
Operating temperature	T_A	-40	+105	°C	
Storage temperature	T_{STG}	-55	+150	°C	

*1 : This parameter is based on $V_{SS} = AV_{SS} = 0$ V.

*2 : Set AV_{CC} and V_{CC} to the same voltage. Make sure that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} when the power is switched on.

*3 : V_I and V_O must not exceed $V_{CC} + 0.3$ V. V_I must not exceed the specified ratings. However if the maximum current to/from an input is limited by some means using external components, the I_{CLAMP} rating supersedes the V_I rating.

*4 : Applicable to pins : P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0, and PA1

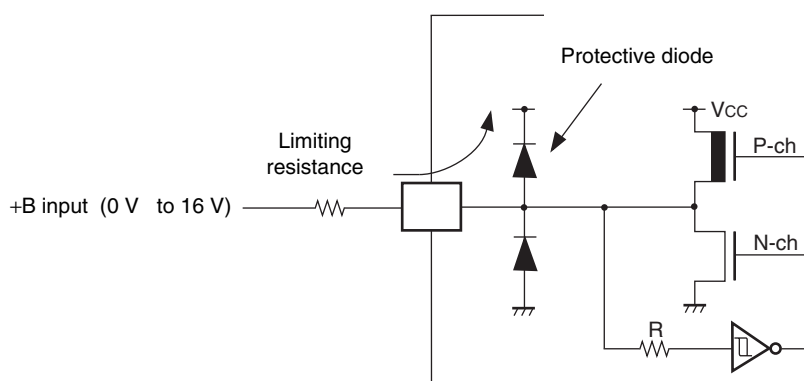
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MB90860E Series

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- *5 :
- Applicable to pins: P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57 (evaluation device : P50 to P55) , P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0, and PA1
 - Use within recommended operating conditions.
 - Use at DC voltage (current)
 - The +B signal should always be applied by placing a limiting resistance between the +B signal and the microcontroller.
 - The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed the rated values, either instantaneously or for prolonged periods.
 - Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
 - Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , power may be supplied through the +B pin, resulting in incomplete operation of the microcontroller.
 - Note that if the +B input is applied during power-on, the power supplied via the +B pin may result in the supply voltage being insufficient to activate the power-on reset.
 - Care must be taken not to leave +B input pins open.
 - Sample recommended circuits:

- Input/output equivalent circuits



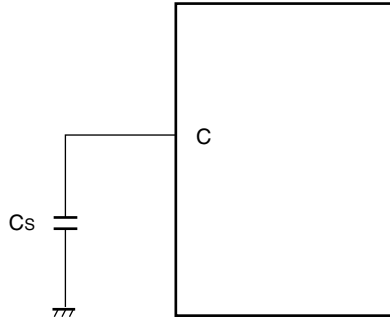
WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

($V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC} , AV_{CC}	4.0	5.0	5.5	V	During normal operation
		3.5	5.0	5.5	V	During normal operation, when not using the A/D converter and not Flash programming.
		4.5	5.0	5.5	V	When using an external bus
		3.0	—	5.5	V	Maintains RAM data in stop mode
Smoothing capacitor	C_S	0.1	—	1.0	μF	Use a ceramic capacitor or a capacitor with similar AC characteristics. The bypass capacitor used on the V_{CC} pin should have a greater capacitance than this capacitor.
Operating temperature	T_A	-40	—	+105	$^{\circ}\text{C}$	

- C Pin Connection Diagram



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges.

Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

MB90860E Series

3. DC Characteristics

($T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input H voltage (At $V_{CC} = 5\text{ V} \pm 10\%$)	V_{IHS}	—	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	Port inputs if CMOS hysteresis input levels are selected (except P12, P44, P45, P46, P47, P50, P82, P85)
	V_{IHA}	—	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	Port inputs if automotive input levels are selected
	V_{IHT}	—	—	2.0	—	$V_{CC} + 0.3$	V	Port inputs if TTL input levels are selected
	V_{IHS}	—	—	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	P12, P50, P82, P85 inputs if CMOS input levels are selected
	V_{IHI}	—	—	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	P44, P45, P46, P47 inputs if CMOS hysteresis input levels are selected
	V_{IHR}	—	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	$\overline{\text{RST}}$ input pin (CMOS hysteresis)
	V_{IHM}	—	—	$V_{CC} - 0.3$	—	$V_{CC} + 0.3$	V	MD input pin
Input L voltage (At $V_{CC} = 5\text{ V} \pm 10\%$)	V_{ILS}	—	—	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	Port inputs if CMOS hysteresis input levels are selected (except P12, P44, P45, P46, P47, P50, P82, P85)
	V_{ILA}	—	—	$V_{SS} - 0.3$	—	$0.5 V_{CC}$	V	Port inputs if automotive input levels are selected
	V_{ILT}	—	—	$V_{SS} - 0.3$	—	0.8	V	Port inputs if TTL input levels are selected
	V_{ILS}	—	—	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	P12, P50, P82, P85 inputs if CMOS input levels are selected
	V_{ILI}	—	—	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	P44, P45, P46, P47 inputs if CMOS hysteresis input levels are selected
	V_{ILR}	—	—	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	$\overline{\text{RST}}$ input pin (CMOS hysteresis)
	V_{ILM}	—	—	$V_{SS} - 0.3$	—	$V_{SS} + 0.3$	V	MD input pin
Output H voltage	V_{OH}	Normal outputs	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -4.0\text{ mA}$	$V_{CC} - 0.5$	—	—	V	
Output H voltage	V_{OHI}	I ² C current outputs	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -3.0\text{ mA}$	$V_{CC} - 0.5$	—	—	V	
Output L voltage	V_{OL}	Normal outputs	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 4.0\text{ mA}$	—	—	0.4	V	
Output L voltage	V_{OLI}	I ² C current outputs	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 3.0\text{ mA}$	—	—	0.4	V	

(Continued)

MB90860E Series

(Continued)

($T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input leak current	I_{IL}	—	$V_{CC} = 5.5\text{ V}$, $V_{SS} < V_i < V_{CC}$	-1	—	+1	μA	
Pull-up resistance	R_{UP}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, \overline{RST}	—	25	50	100	$\text{k}\Omega$	
Pull-down resistance	R_{DOWN}	MD2	—	25	50	100	$\text{k}\Omega$	Except Flash devices
Power supply current*	I_{CC}	V_{CC}	$V_{CC} = 5.0\text{ V}$, Internal frequency : 24 MHz, during normal operation.	—	55	70	mA	
			$V_{CC} = 5.0\text{ V}$, Internal frequency : 24 MHz, when writing FLASH memory.	—	70	85	mA	Flash devices
			$V_{CC} = 5.0\text{ V}$, Internal frequency : 24 MHz, when erasing FLASH memory.	—	75	90	mA	Flash devices
	I_{CCS}		$V_{CC} = 5.0\text{ V}$, Internal frequency : 24 MHz, in Sleep mode.	—	25	35	mA	
	I_{CTS}		$V_{CC} = 5.0\text{ V}$, Internal frequency : 2 MHz, in Main Timer mode	—	0.3	0.8	mA	
	$I_{CTSPLL6}$		$V_{CC} = 5.0\text{ V}$, Internal frequency : 24 MHz, in PLL Timer mode, external frequency = 4 MHz	—	4	7	mA	
	I_{CCL}		$V_{CC} = 5.0\text{ V}$ Internal frequency : 8 kHz, during sub operation $T_A = +25\text{ }^\circ\text{C}$	—	70	140	μA	
	I_{CCLS}		$V_{CC} = 5.0\text{ V}$ Internal frequency : 8 kHz, during sub sleep $T_A = +25\text{ }^\circ\text{C}$	—	20	50	μA	
	I_{CCT}		$V_{CC} = 5.0\text{ V}$ Internal frequency : 8 kHz, in watch mode $T_A = +25\text{ }^\circ\text{C}$	—	10	35	μA	
I_{CCH}	$V_{CC} = 5.0\text{ V}$, in Stop mode, $T_A = +25\text{ }^\circ\text{C}$	—	7	25	μA			
Input capacitance	C_{IN}	Other than C, AV_{CC} , AV_{SS} , $AVRH$, $AVRL$, V_{CC} , V_{SS}	—	—	5	15	pF	

* : Power supply currents were measured under test conditions using an external clock.

MB90860E Series

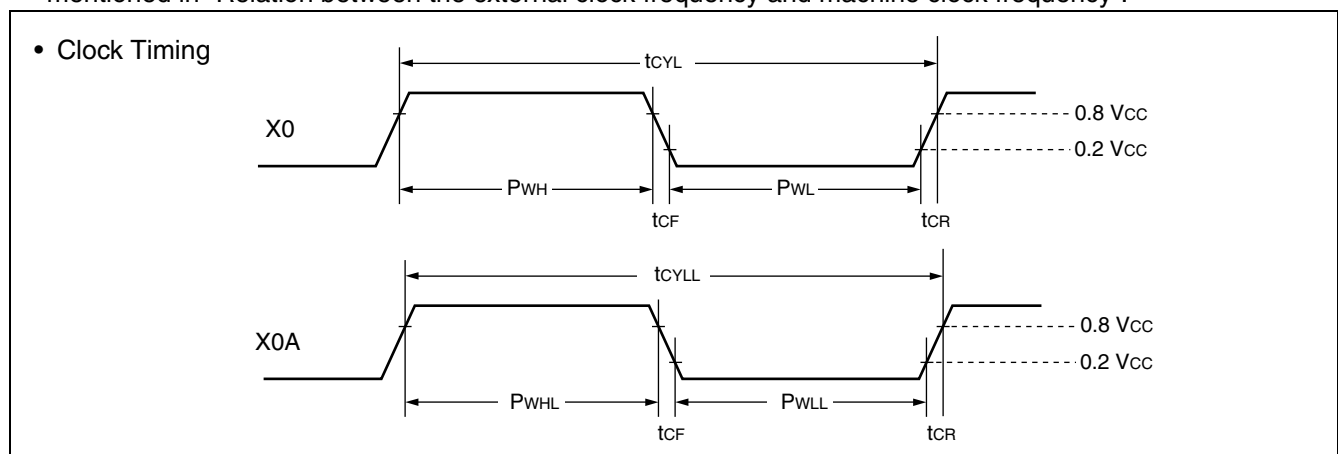
4. AC Characteristics

(1) Clock Timing

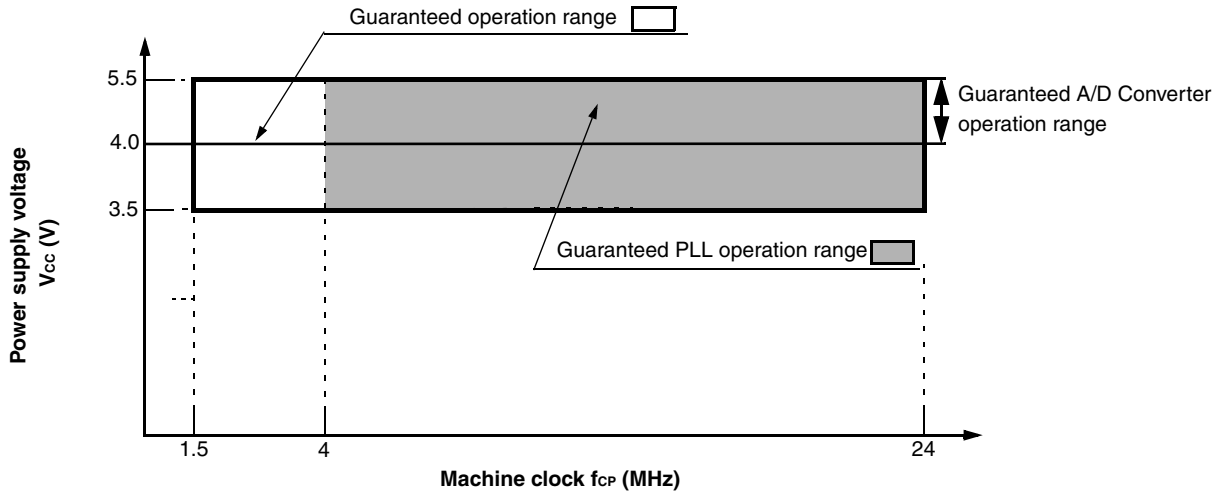
($T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f _c	X0, X1	3	—	16	MHz	1/2 (at PLL stop) When using an oscillator circuit
			4	—	16	MHz	PLL multiplied by 1 When using an oscillator circuit*
			4	—	12	MHz	PLL multiplied by 2 When using an oscillator circuit*
			4	—	8	MHz	PLL multiplied by 3 When using an oscillator circuit*
			4	—	6	MHz	PLL multiplied by 4 When using an oscillator circuit*
			—	—	4	MHz	PLL multiplied by 6 When using an oscillator circuit*
	f _{CL}	X0A, X1A	—	32.768	100	kHz	When using an external clock
Clock cycle time	t _{CYL}	X0, X1	62.5	—	333	ns	When using an oscillator circuit
		X0, X1	41.67	—	333	ns	When using an external clock
	t _{CYLL}	X0A, X1A	10	30.5	—	μs	
Input clock pulse width	P _{WH} , P _{WL}	X0	10	—	—	ns	Duty ratio is about 30% to 70%.
	P _{WHL} , P _{WLL}	X0A	5	15.2	—	μs	
Input clock rise and fall time	t _{CR} , t _{CF}	X0	—	—	5	ns	When using external clock
Internal operating clock frequency (machine clock)	f _{CP}	—	1.5	—	24	MHz	When using main clock
	f _{CPL}	—	—	8.192	50	kHz	When using sub clock
Internal operating clock cycle time (machine clock)	t _{CP}	—	41.67	—	666	ns	When using main clock
	t _{CPL}	—	20	122.1	—	μs	When using sub clock

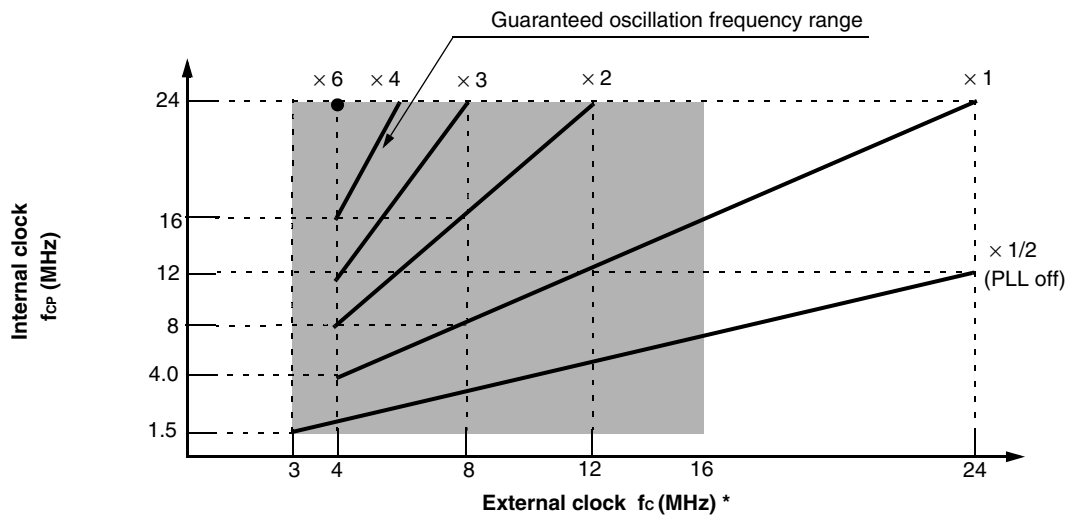
* : When selecting the PLL clock, the range of clock frequency is limited. Use this product within the range as mentioned in "Relation between the external clock frequency and machine clock frequency".



• Guaranteed PLL operation range



Guaranteed operation range of MB90860E series



* : When using a crystal oscillator or a ceramic oscillator, the maximum oscillation clock frequency is 16 MHz

MB90860E Series

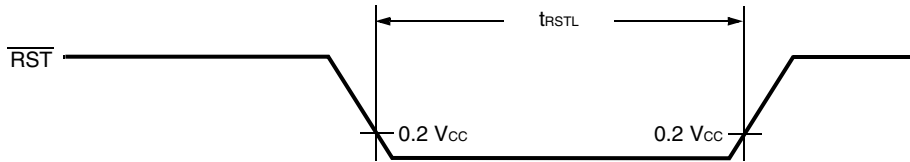
(2) Reset Standby Input

($T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$)

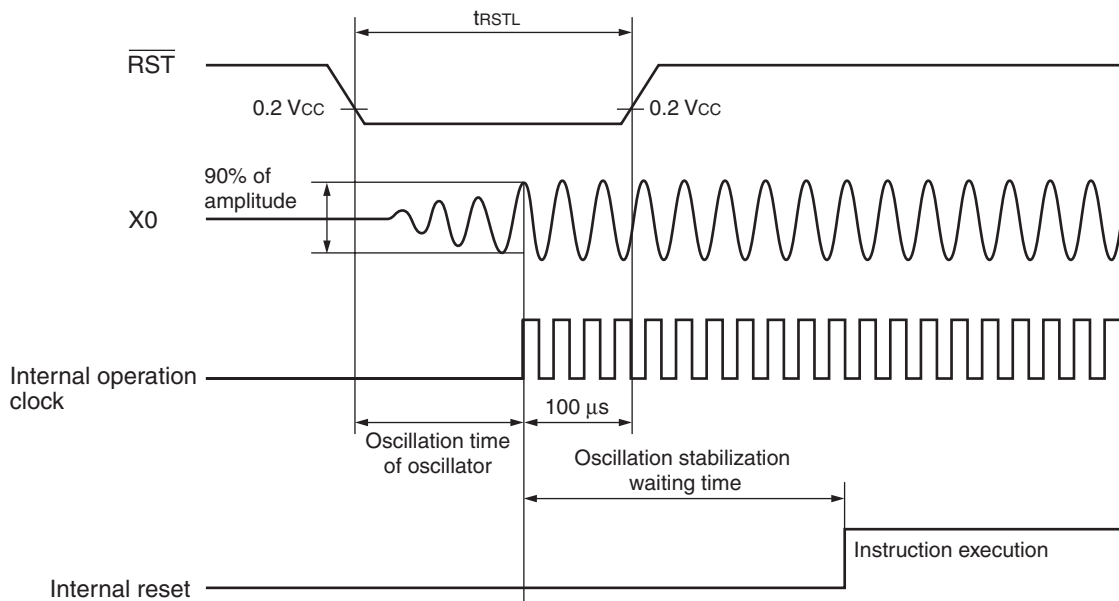
Parameter	Symbol	Pin	Value		Unit	Remarks	
			Min	Max			
Reset input time	t_{RSTL}	\overline{RST}	500	—	ns	During normal operation	
			Oscillation time of oscillator* + 100 μs		—	μs	In Stop mode, Sub Clock mode, Sub Sleep mode and Watch mode
			100	—	μs	In Time Timer mode	

* : The oscillation time of the oscillator is the time it takes for the amplitude to reach 90%. In crystal oscillators, the oscillation time is between several ms and to tens of ms. In crystal oscillators, the oscillation time is between hundreds of μs to several ms. For an external clock, the oscillation time is 0 ms.

During normal operation:



In Stop mode, Sub Clock mode, Sub Sleep mode, Watch mode, Power-on:



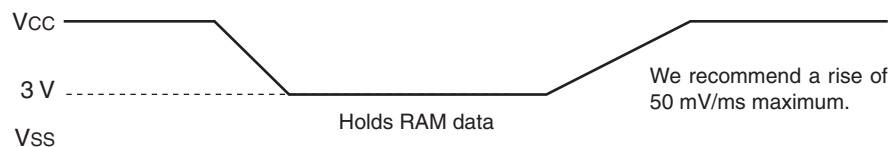
(3) Power On Reset

($T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Power on rise time	t_R	V_{CC}	—	0.05	30	ms	
Power off time	t_{OFF}	V_{CC}	—	1	—	ms	Waiting time until power-on



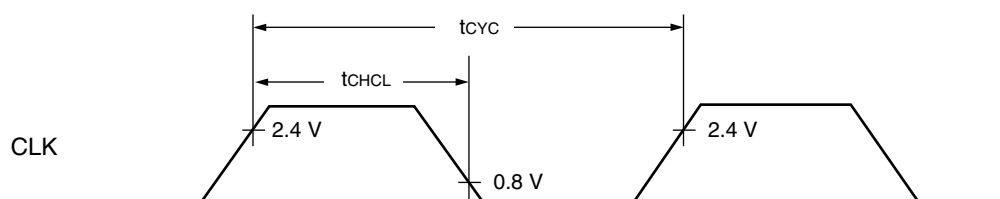
If you change the power supply voltage too rapidly, a power on reset may occur. If the power supply voltage is varied while the device is operating, it is recommended that variation be limited such that the supply voltage rises smoothly as shown in the following diagram. The supply voltage should be changed while the PLL clock is not being used. However, the device can be operated while the PLL is being used if the rate of change is less than 1 V/s.



(4) Clock Output Timing

($T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $f_{CP} \leq 24\text{ MHz}$)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	CLK	—	62.5	—	ns	$f_{CP} = 16\text{ MHz}$
				41.67	—	ns	$f_{CP} = 24\text{ MHz}$
CLK $\uparrow \rightarrow$ CLK \downarrow	t_{CHCL}	CLK	—	20	—	ns	$f_{CP} = 16\text{ MHz}$
				13	—	ns	$f_{CP} = 24\text{ MHz}$

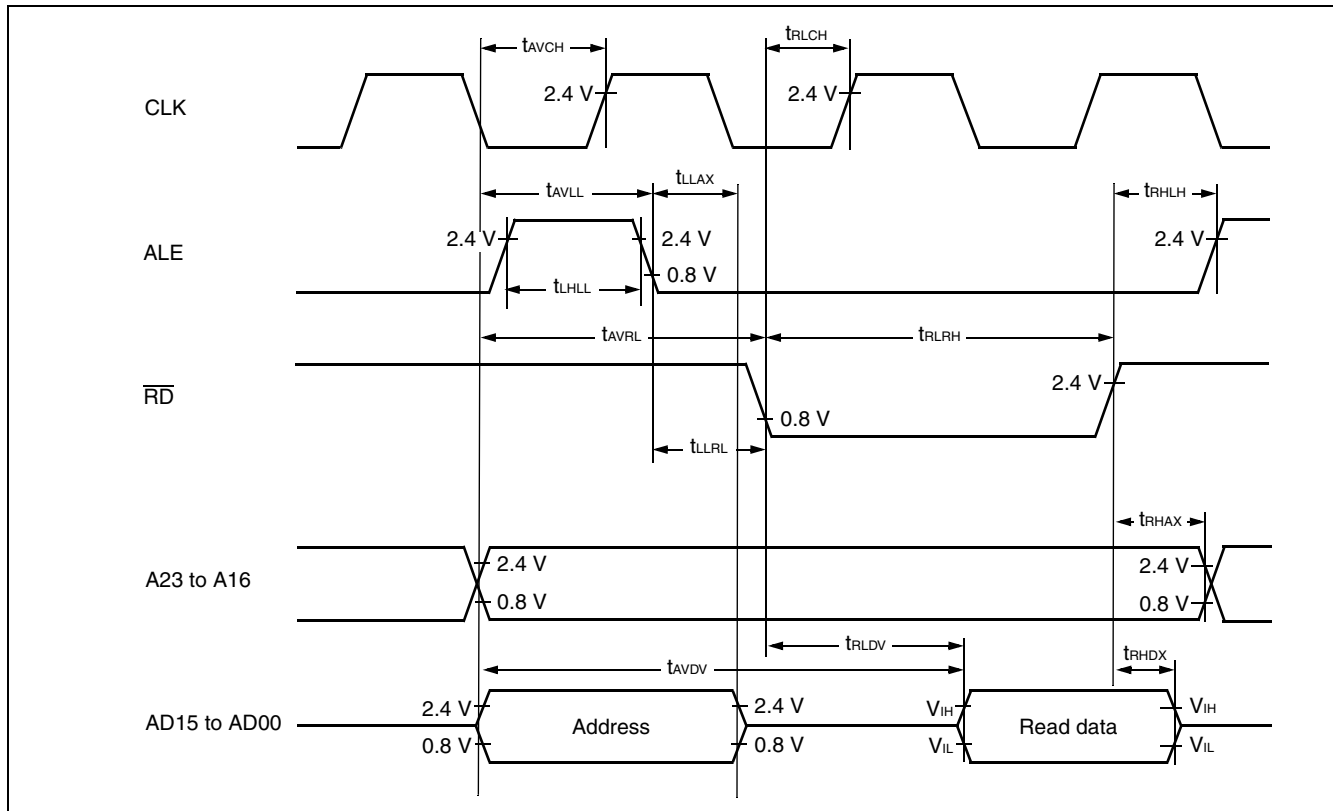


MB90860E Series

(5) Bus Timing (Read)

($T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $f_{CP} \leq 24\text{ MHz}$)

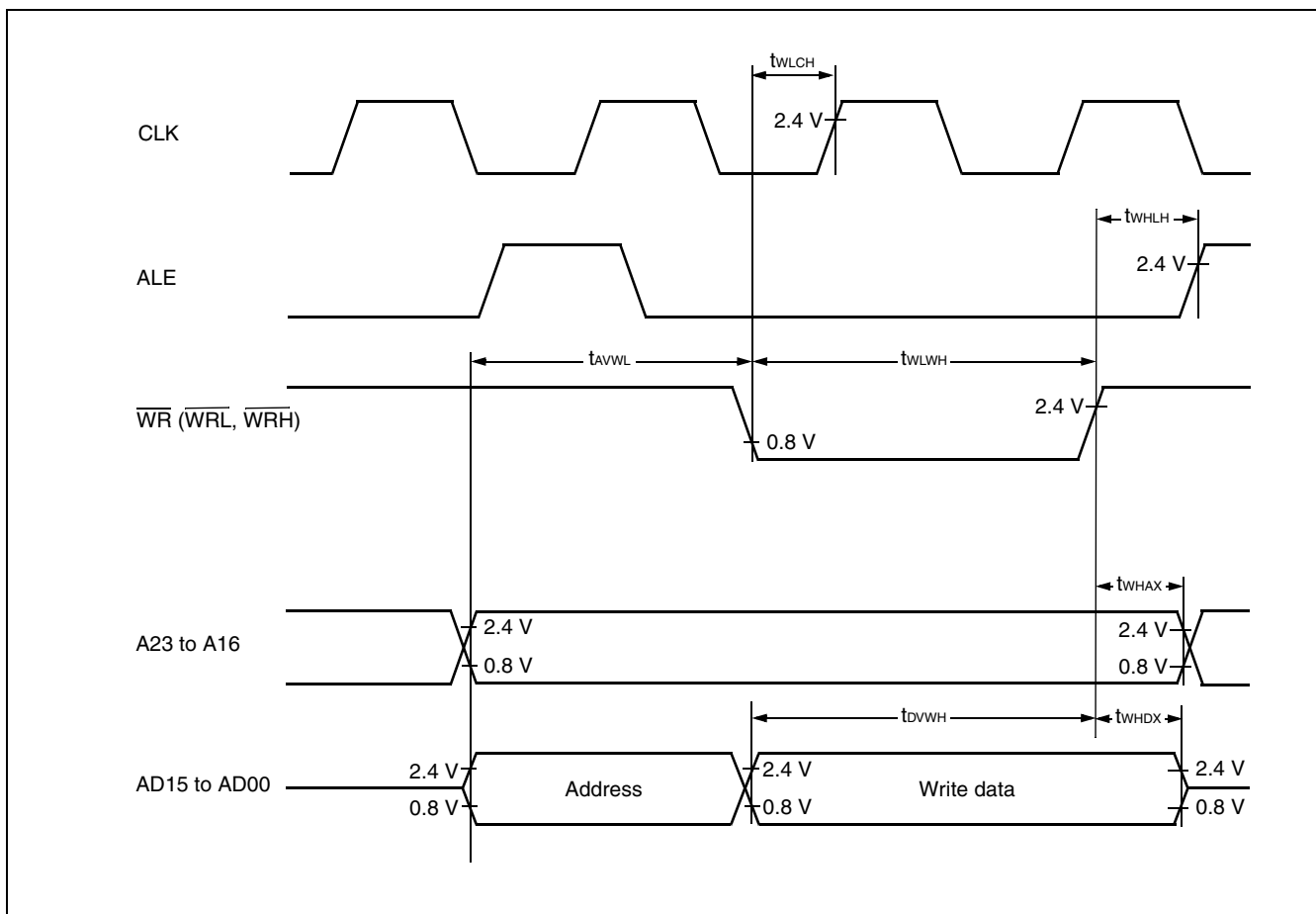
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
ALE pulse width	t_{LHLL}	ALE	—	$t_{CP}/2 - 10$	—	ns
Valid address \rightarrow ALE \downarrow time	t_{AVLL}	ALE, A23 to A16, AD15 to AD00		$t_{CP}/2 - 20$	—	ns
ALE \downarrow \rightarrow Address valid time	t_{LLAX}	ALE, AD15 to AD00		$t_{CP}/2 - 15$	—	ns
Valid address \rightarrow \overline{RD} \downarrow time	t_{AVRL}	A23 to A16, AD15 to AD00, \overline{RD}		$t_{CP} - 15$	—	ns
Valid address \rightarrow Valid data input	t_{AVDV}	A23 to A16, AD15 to AD00		—	$5 t_{CP}/2 - 60$	ns
\overline{RD} pulse width	t_{RLRH}	\overline{RD}		$3 t_{CP}/2 - 20$	—	ns
\overline{RD} \downarrow \rightarrow Valid data input	t_{RLDV}	\overline{RD} , AD15 to AD00		—	$3 t_{CP}/2 - 50$	ns
\overline{RD} \uparrow \rightarrow Data hold time	t_{RHDX}	\overline{RD} , AD15 to AD00		0	—	ns
\overline{RD} \uparrow \rightarrow ALE \uparrow time	t_{RHLH}	\overline{RD} , ALE		$t_{CP}/2 - 15$	—	ns
\overline{RD} \uparrow \rightarrow Address valid time	t_{RHAX}	\overline{RD} , A23 to A16		$t_{CP}/2 - 10$	—	ns
Valid address \rightarrow CLK \uparrow time	t_{AVCH}	A23 to A16, AD15 to AD00, CLK		$t_{CP}/2 - 16$	—	ns
\overline{RD} \downarrow \rightarrow CLK \uparrow time	t_{RLCH}	\overline{RD} , CLK		$t_{CP}/2 - 15$	—	ns
ALE \downarrow \rightarrow \overline{RD} \downarrow time	t_{LLRL}	ALE, \overline{RD}		$t_{CP}/2 - 15$	—	ns



(6) Bus Timing (Write)

($T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $f_{CP} \leq 24\text{ MHz}$)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Valid address $\rightarrow \overline{WR} \downarrow$ time	t_{AVWL}	A23 to A16, AD15 to AD00, \overline{WR}	—	$t_{CP} - 15$	—	ns
\overline{WR} pulse width	t_{WLWH}	\overline{WR}		$3 t_{CP} / 2 - 20$	—	ns
Valid data output $\rightarrow \overline{WR} \uparrow$ time	t_{DVWH}	AD15 to AD00, \overline{WR}		$3 t_{CP} / 2 - 20$	—	ns
$\overline{WR} \uparrow \rightarrow$ Data hold time	t_{WHDX}	AD15 to AD00, \overline{WR}		15	—	ns
$\overline{WR} \uparrow \rightarrow$ Address valid time	t_{WHAX}	A23 to A16, \overline{WR}		$t_{CP} / 2 - 10$	—	ns
$\overline{WR} \uparrow \rightarrow$ ALE \uparrow time	t_{WHLH}	\overline{WR} , ALE		$t_{CP} / 2 - 15$	—	ns
$\overline{WR} \downarrow \rightarrow$ CLK \uparrow time	t_{WLCH}	\overline{WR} , CLK		$t_{CP} / 2 - 15$	—	ns



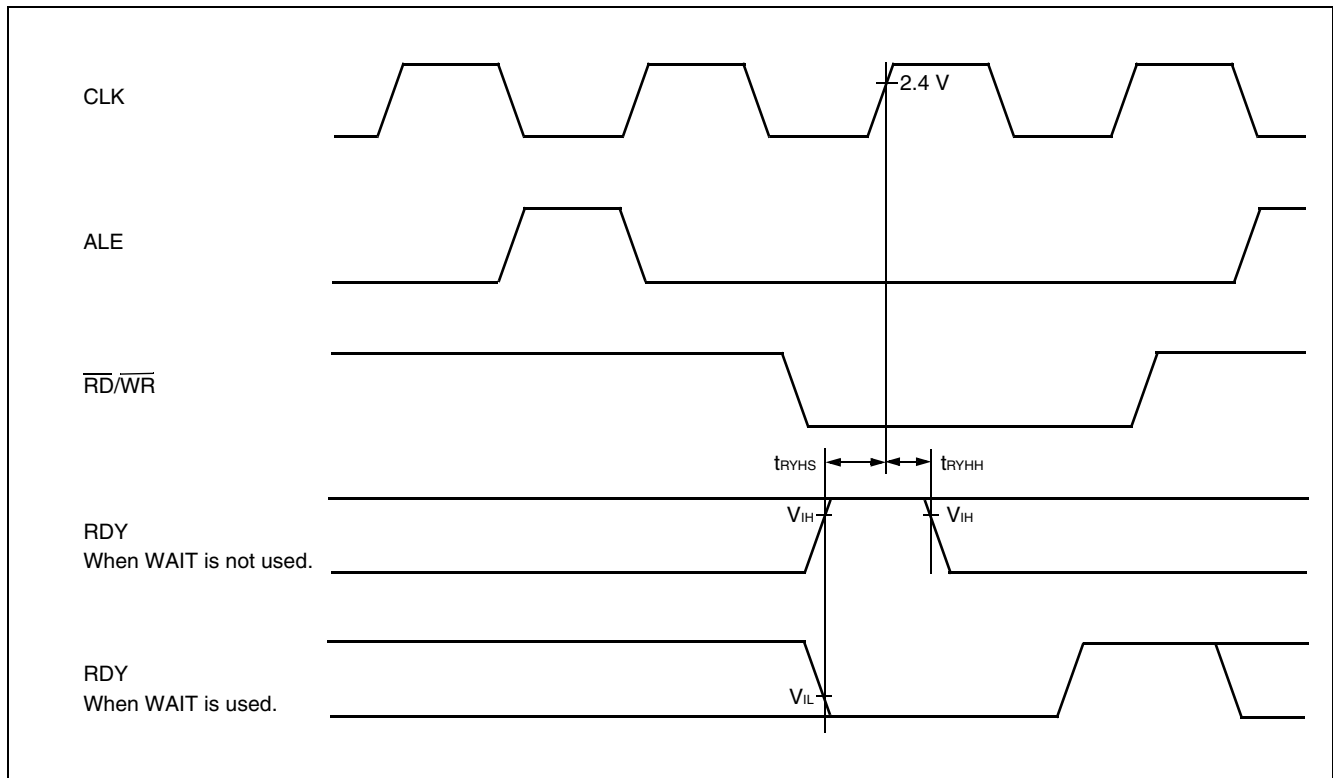
MB90860E Series

(7) Ready Input Timing

($T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $f_{CP} \leq 24\text{ MHz}$)

Parameter	Symbol	Pin	Condition	Rated Value		Units	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY	—	45	—	ns	$f_{CP} = 16\text{ MHz}$
				32	—	ns	$f_{CP} = 24\text{ MHz}$
RDY hold time	t_{RYHH}	RDY	—	0	—	ns	

Note : If the RDY setup time is insufficient, use the auto-ready function.

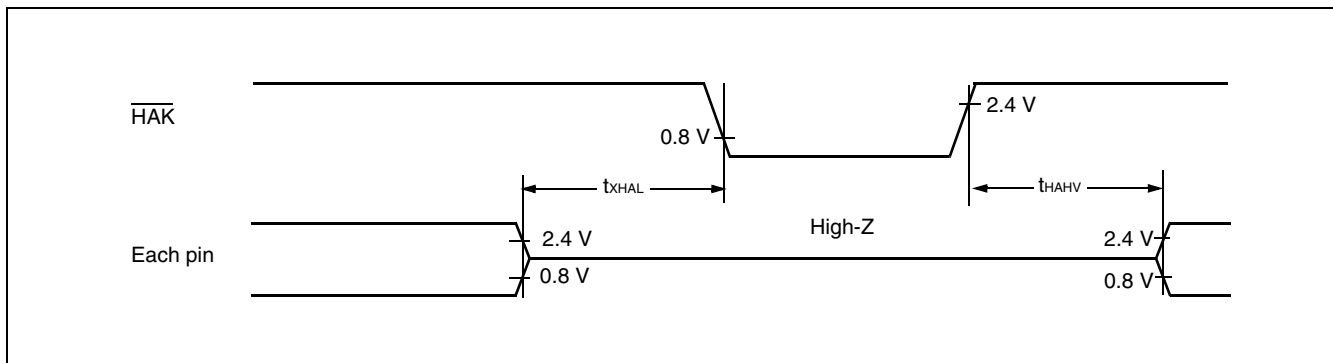


(8) Hold Timing

($T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $f_{CP} \leq 24\text{ MHz}$)

Parameter	Symbol	Pin	Condition	Value		Units
				Min	Max	
Pin floating $\rightarrow \overline{\text{HAK}} \downarrow$ time	t_{XHAL}	$\overline{\text{HAK}}$	—	30	t_{CP}	ns
$\overline{\text{HAK}} \uparrow$ time \rightarrow Pin valid time	t_{HAHV}	$\overline{\text{HAK}}$		t_{CP}	$2 t_{CP}$	ns

Note : It takes at least one machine clock cycle from when an HRQ is accepted until $\overline{\text{HAK}}$ changes.



MB90860E Series

(9) LIN-UART0/1/2/3

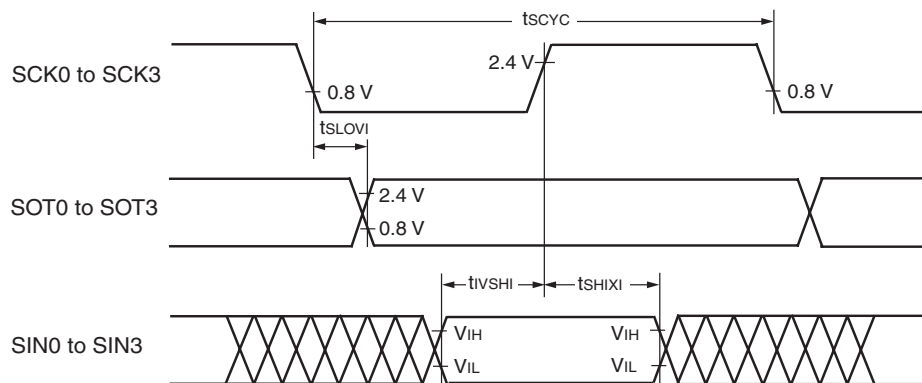
- Bit setting: ESCR:SCES = 0, ECCR:SCDE = 0

($T_A = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = 0\text{ V}$)

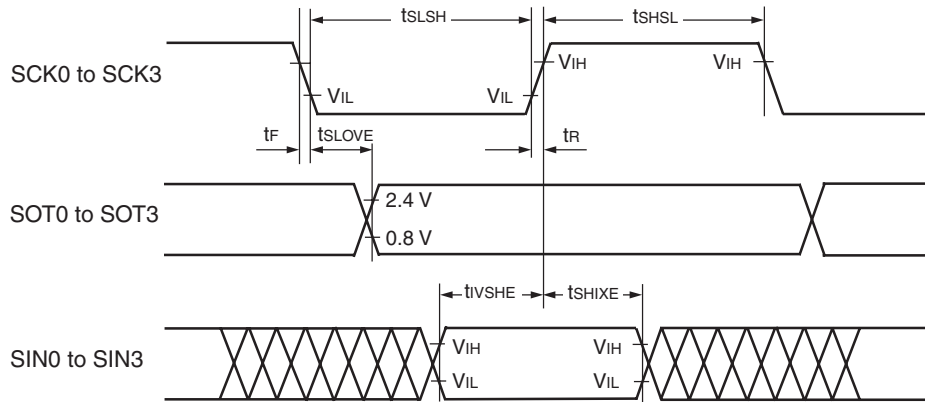
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal shift clock mode output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$.	$5 t_{CP}$	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK0 to SCK3 SOT0 to SOT3		-50	+50	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK0 to SCK3 SIN0 to SIN3		$t_{CP} + 80$	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXI}	SCK0 to SCK3 SIN0 to SIN3		0	—	ns
Serial clock “L” pulse width	t_{SHSL}	SCK0 to SCK3	External shift clock mode output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$.	$3 t_{CP} - t_R$	—	ns
Serial clock “H” pulse width	t_{SLSH}	SCK0 to SCK3		$t_{CP} + 10$	—	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCK0 to SCK3 SOT0 to SOT3		—	$2 t_{CP} + 60$	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCK0 to SCK3 SIN0 to SIN3		30	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXE}	SCK0, SCK1, SIN0 to SIN3		$t_{CP} + 30$	—	ns
SCK fall time	t_F	SCK0 to SCK3		—	10	ns
SCK rise time	t_R	SCK0 to SCK3		—	10	ns

- Notes :
- AC characteristic in CLK synchronized mode.
 - C_L is load capacity value of pins when testing.
 - t_{CP} is internal operating clock cycle time (machine clock) . Refer to “ (1) Clock Timing”.

• Internal Shift Clock Mode



• External Shift Clock Mode



• Bit setting: ESCR:SCES = 1, ECCR:SCDE = 0

($T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = 0\text{ V}$)

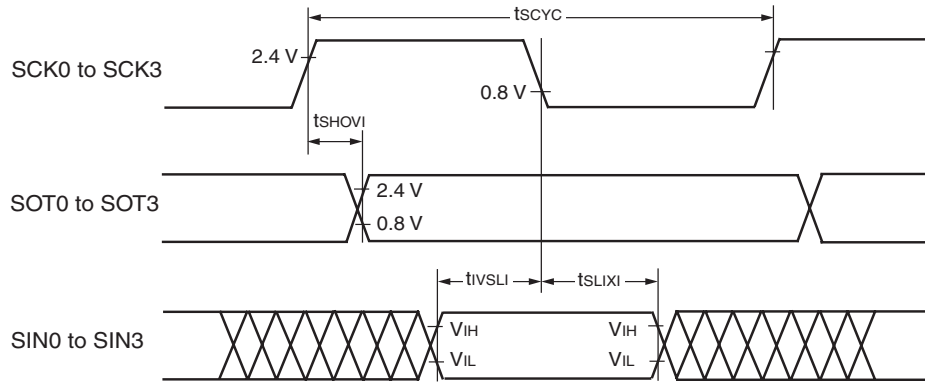
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal shift clock mode output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$.	$5 t_{CP}$	—	ns
SCK \uparrow \rightarrow SOT delay time	t_{SHOVI}	SCK0 to SCK3 SOT0 to SOT3		-50	+50	ns
Valid SIN \rightarrow SCK \downarrow	t_{IVSLI}	SCK0 to SCK3 SIN0 to SIN3		$t_{CP} + 80$	—	ns
SCK \downarrow \rightarrow Valid SIN hold time	t_{SLIXI}	SCK0 to SCK3 SIN0 to SIN3		0	—	ns
Serial clock "H" pulse width	t_{SHSL}	SCK0 to SCK3	External shift clock mode output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$.	$3 t_{CP} - t_R$	—	ns
Serial clock "L" pulse width	t_{SLSH}	SCK0 to SCK3		$t_{CP} + 10$	—	ns
SCK \uparrow \rightarrow SOT delay time	t_{SHOVE}	SCK0 to SCK3 SOT0 to SOT3		—	$2 t_{CP} + 60$	ns
Valid SIN \rightarrow SCK \downarrow	t_{IVSLE}	SCK0 to SCK3 SIN0 to SIN3		30	—	ns
SCK \downarrow \rightarrow Valid SIN hold time	t_{SLIXE}	SCK0 to SCK3 SIN0 to SIN3		$t_{CP} + 30$	—	ns
SCK fall time	t_F	SCK0 to SCK3		—	10	ns
SCK rise time	t_R	SCK0 to SCK3		—	10	ns

Notes : • C_L is load capacity value of pins when testing.

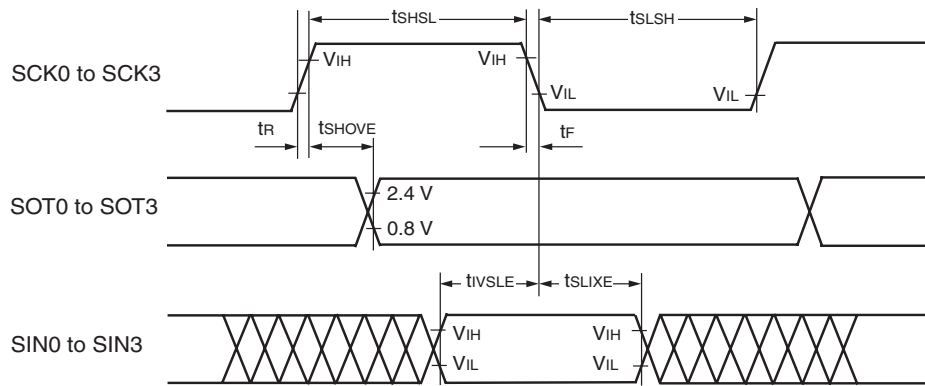
• t_{CP} is internal operating clock cycle time (machine clock) . Refer to "(1) Clock Timing".

MB90860E Series

• Internal Shift Clock Mode



• External Shift Clock Mode



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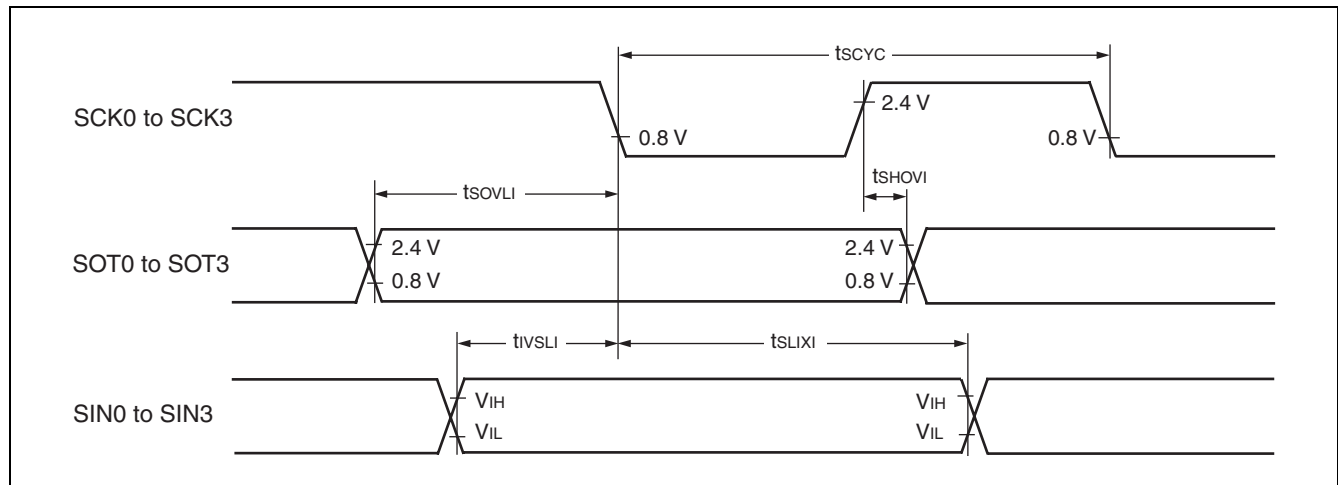
- Bit setting: ESCR:SCES = 0, ECCR:SCDE = 1

($T_A = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$.	$5 t_{CP}$	—	ns
SCK \uparrow \rightarrow SOT delay time	t_{SHOVI}	SCK0 to SCK3 SOT0 to SOT3		-50	+50	ns
Valid SIN \rightarrow SCK \downarrow	t_{IVSLI}	SCK0 to SCK3 SIN0 to SIN3		$t_{CP} + 80$	—	ns
SCK \downarrow \rightarrow Valid SIN hold time	t_{SLIXI}	SCK0 to SCK3 SIN0 to SIN3		0	—	ns
SOT \rightarrow SCK \downarrow delay time	t_{SOVLI}	SCK0 to SCK3 SOT0 to SOT3		$3 t_{CP} - 70$	—	ns

Notes : • C_L is load capacity value of pins when testing.

- t_{CP} is internal operating clock cycle time (machine clock) . Refer to “ (1) Clock Timing”.



MB90860E Series

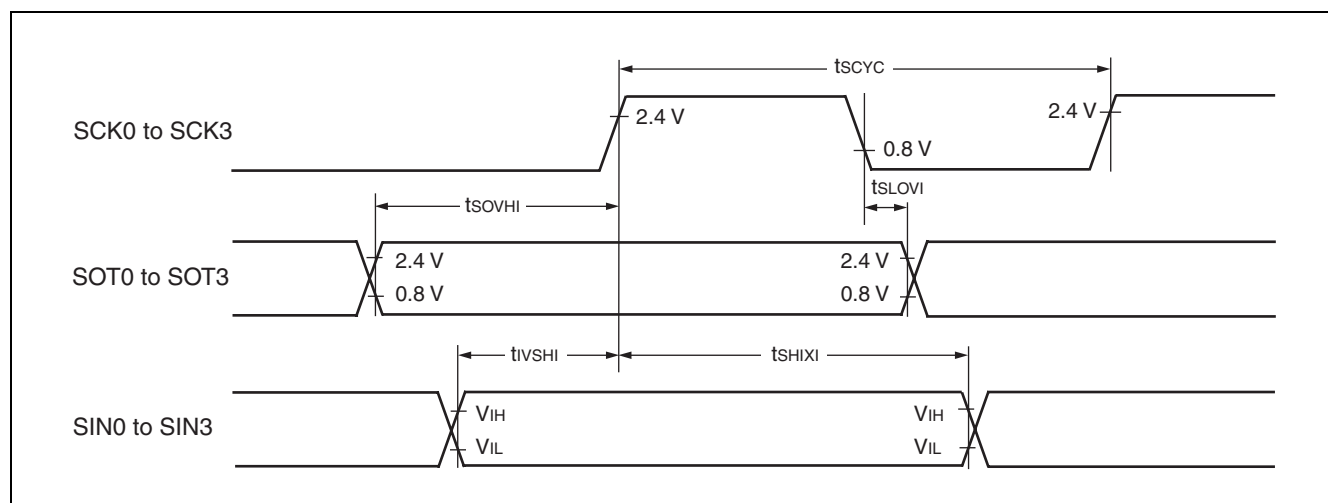
- Bit setting: ESCR:SCES = 1, ECCR:SCDE = 1

($T_A = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$.	$5 t_{CP}$	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK0 to SCK3 SOT0 to SOT3		-50	+50	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK0 to SCK3 SIN0 to SIN3		$t_{CP} + 80$	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXI}	SCK0 to SCK3 SIN0 to SIN3		0	—	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCK0 to SCK3 SOT0 to SOT3		$3 t_{CP} - 70$	—	ns

Notes : • C_L is load capacity value of pins when testing.

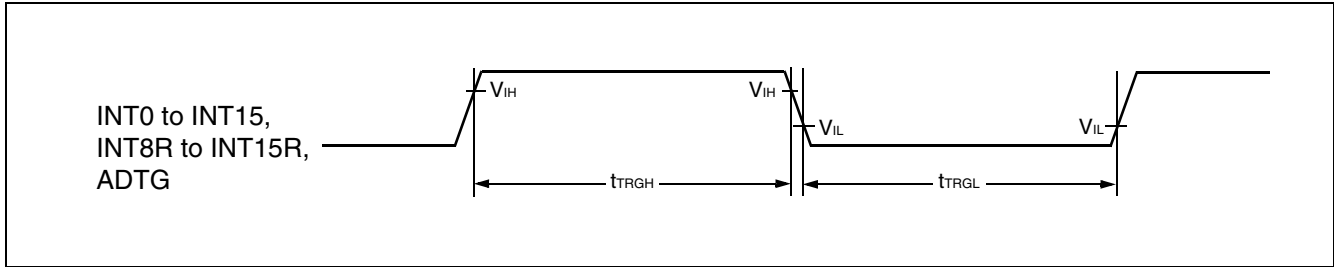
- t_{CP} is internal operating clock cycle time (machine clock) . Refer to “(1) Clock Timing”.



(10) Trigger Input Timing

($T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TRGH} t_{TRGL}	INT0 to INT15, INT8R to INT15R, ADTG	—	5 t_{CP}	—	ns

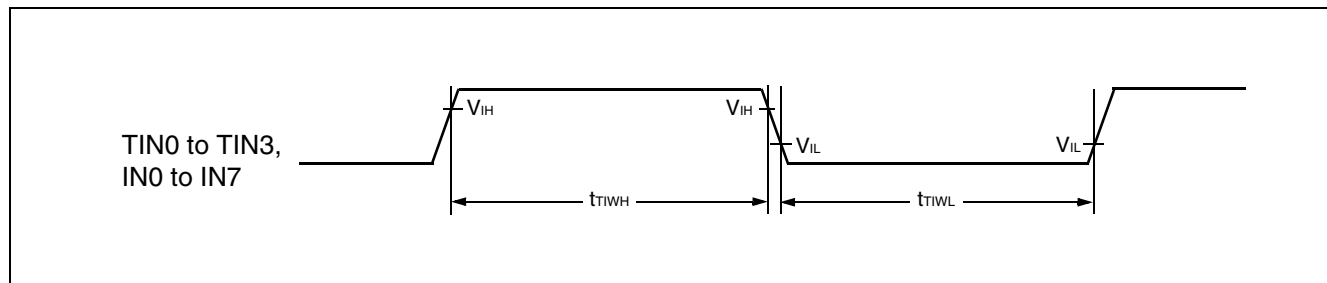


MB90860E Series

(11) Timer Related Resource Input Timing

($T_A = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = 0\text{ V}$)

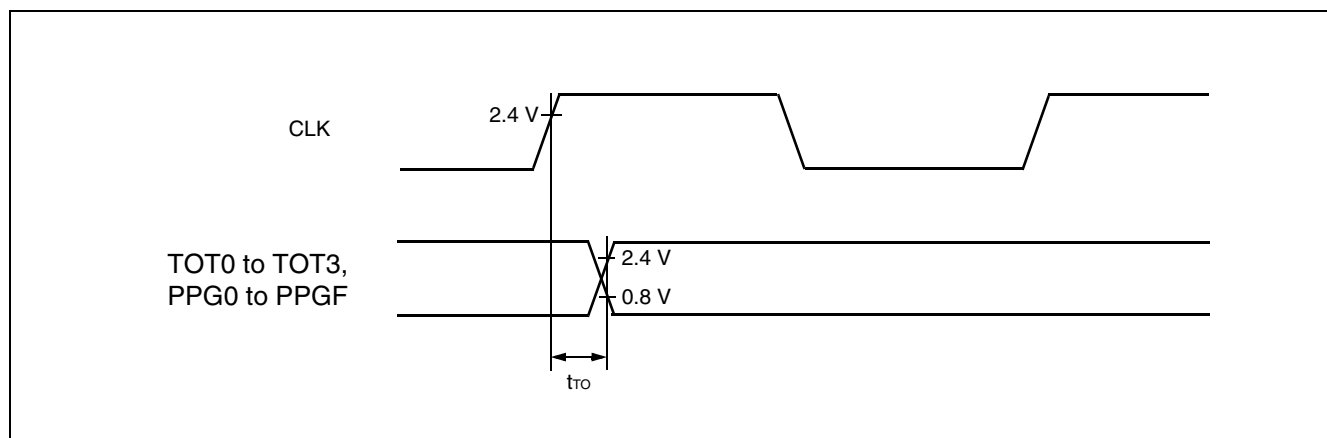
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH}	TIN0 to TIN3, IN0 to IN7	—	4 t_{CP}	—	ns
	t_{TIWL}					



(12) Timer Related Resource Output Timing

($T_A = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
CLK \uparrow \rightarrow T_{OUT} change time	t_{TO}	TOT0 to TOT3, PPG0 to PPGF	—	30	—	ns



(13) I²C Timing

(T_A = -40°C to +105°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V)

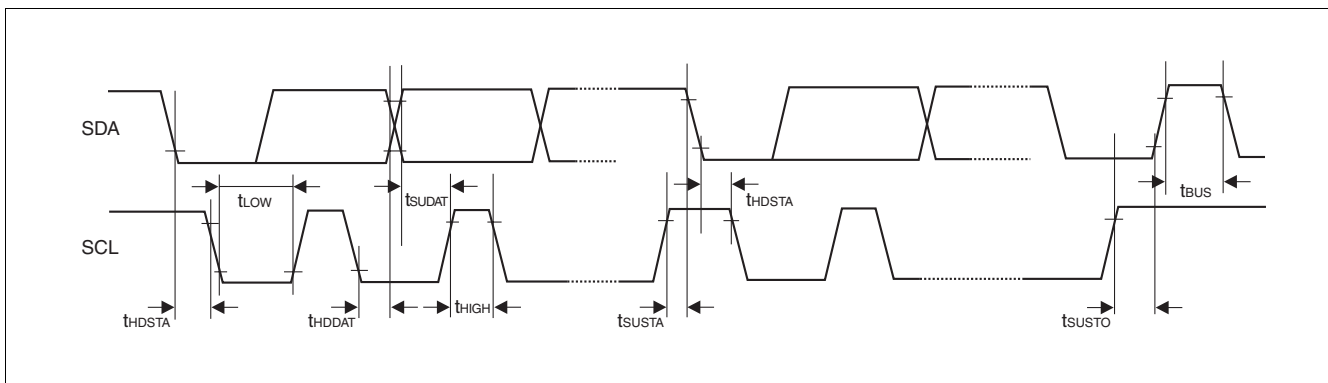
Parameter	Symbol	Condition	Standard-mode		Fast-mode* ¹		Unit
			Min	Max	Min	Max	
SCL clock frequency	f _{SCL}	R = 1.7 kΩ, C = 50 pF* ²	0	100	0	400	kHz
Hold time (repeated) START condition SDA ↓ → SCL ↓	t _{HDSTA}		4.0	—	0.6	—	μs
“L” width of the SCL clock	t _{LOW}		4.7	—	1.3	—	μs
“H” width of the SCL clock	t _{HIGH}		4.0	—	0.6	—	μs
Set-up time for a repeated START condition SCL ↑ → SDA ↓	t _{SUSTA}		4.7	—	0.6	—	μs
Data hold time SCL ↓ → SDA ↓ ↑	t _{HDDAT}		0	3.45* ³	0	0.9* ⁴	μs
Data set-up time SDA ↓ ↑ → SCL ↑	t _{SUDAT}		250	—	100	—	ns
Set-up time for STOP condition SCL ↑ → SDA ↑	t _{SUSTO}		4.0	—	0.6	—	μs
Bus free time between a STOP and START condition	t _{BUS}	4.7	—	1.3	—	μs	

*1 : For use at over 100 kHz, set the machine clock to at least 6 MHz.

*2 : R,C : Pull-up resistance and load capacitance of the SCL and SDA lines.

*3 : The maximum t_{HDDAT} must be satisfied if the device does not extend the “L” width (t_{LOW}) of the SCL signal.

*4 : A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement t_{SUDAT} ≥ 250 ns must then be met.



MB90860E Series

5. A/D Converter

($T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$, $3.0\text{ V} \leq AV_{RH} - AV_{RL}$, $V_{CC} = AV_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

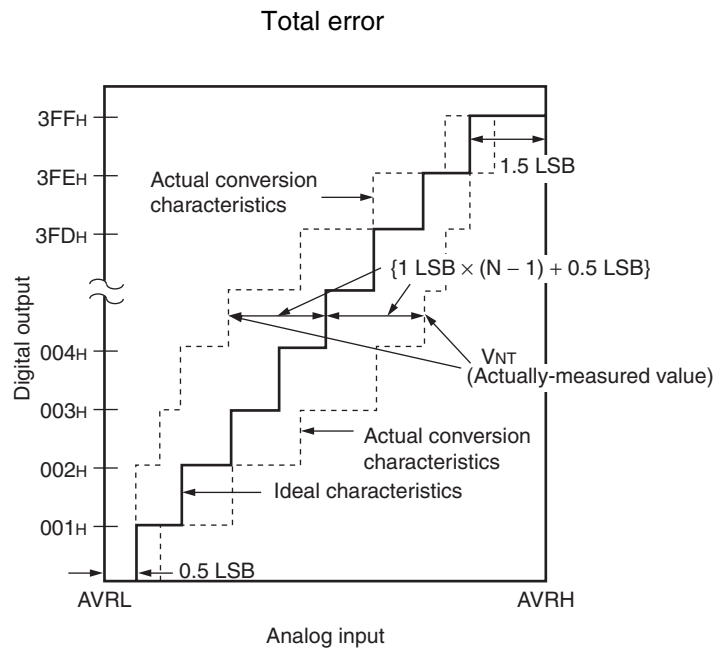
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	—	—	± 3.0	LSB	
Nonlinearity error	—	—	—	—	± 2.5	LSB	
Differential nonlinearity error	—	—	—	—	± 1.9	LSB	
Zero reading voltage	V_{OT}	AN0 to AN23	$AV_{RL} - 1.5 \times \text{LSB}$	$AV_{RL} + 0.5 \times \text{LSB}$	$AV_{RL} + 2.5 \times \text{LSB}$	V	
Full scale reading voltage	V_{FST}	AN0 to AN23	$AV_{RH} - 3.5 \times \text{LSB}$	$AV_{RH} - 1.5 \times \text{LSB}$	$AV_{RH} + 0.5 \times \text{LSB}$	V	
Compare time	—	—	1.0	—	16500	μs	$4.5\text{ V} \leq AV_{CC} \leq 5.5\text{ V}$
			2.0				$4.0\text{ V} \leq AV_{CC} < 4.5\text{ V}$
Sampling time	—	—	0.5	—	∞	μs	$4.5\text{ V} \leq AV_{CC} \leq 5.5\text{ V}$
			1.2				$4.0\text{ V} \leq AV_{CC} < 4.5\text{ V}$
Analog port input current	I_{AIN}	AN0 to AN23	-0.3	—	+0.3	μA	
Analog input voltage	V_{AIN}	AN0 to AN23	AV_{RL}	—	AV_{RH}	V	
Reference voltage	—	AV_{RH}	$AV_{RL} + 2.7$	—	AV_{CC}	V	
	—	AV_{RL}	0	—	$AV_{RH} - 2.7$	V	
Power supply current	I_A	AV_{CC}	—	3.5	7.5	mA	
	I_{AH}	AV_{CC}	—	—	5	μA	*
Reference voltage current	I_R	AV_{RH}	—	600	900	μA	
	I_{RH}	AV_{RH}	—	—	5	μA	*
Variation between input channels	—	AN0 to AN23	—	—	4	LSB	

* : This is the current when the A/D converter is not being operated, and the CPU is stopped ($V_{CC} = AV_{CC} = AV_{RH} = 5.0\text{ V}$).

Note : The relative error increases as $AV_{RH} - AV_{RL}$ becomes smaller.

6. Definition of A/D Converter Terms

- Resolution : Analog variation that is recognized by an A/D converter.
- Non linearity error : Deviation of the actual conversion characteristics from a line that connects the zero transition point (“00 0000 0000” ← → “00 0000 0001”) to the full-scale transition point (“11 1111 1110” ← → “11 1111 1111”) .
- Differential linearity error : Deviation from the ideal value of the input voltage required to change the output code by LSB.
- Total error : Difference between the actual value and the ideal value. The total error includes zero transition error, full-scale transition error, and linear error.



$$\text{Total error of digital output "N"} = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + 0.5 \text{ LSB}\}}{1 \text{ LSB}} \text{ [LSB]}$$

$$1 \text{ LSB (Ideal value)} = \frac{AVRH - AVRL}{1024} \text{ [V]}$$

N : A/D converter digital output value

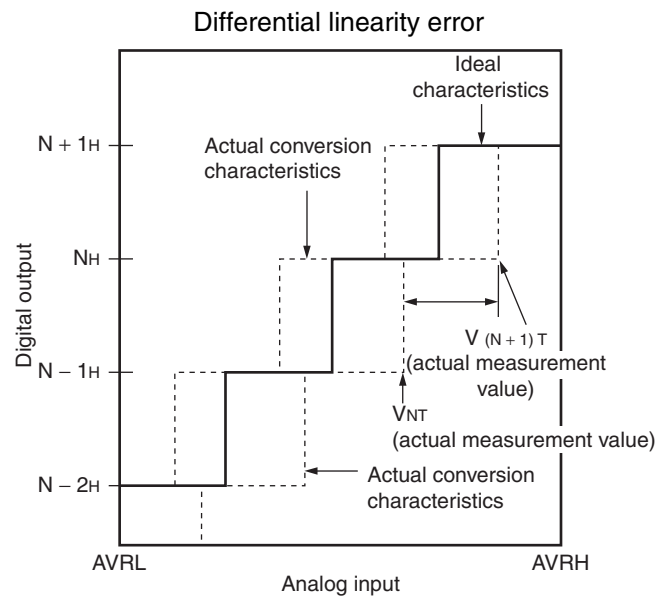
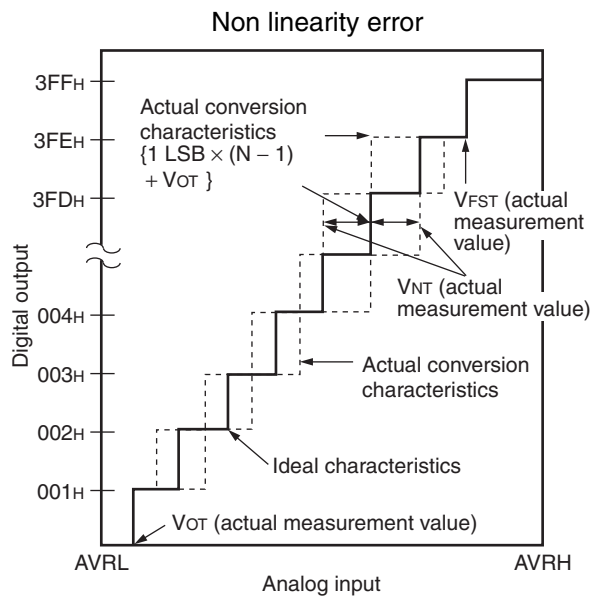
$$V_{OT} \text{ (Ideal value)} = AVRL + 0.5 \text{ LSB [V]}$$

$$V_{FST} \text{ (Ideal value)} = AVRH - 1.5 \text{ LSB [V]}$$

V_{NT} : The voltage at which the digital output changes from $(N - 1)_H$ to N_H .

(Continued)

(Continued)



$$\text{Non linearity error of digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + V_{OT}\}}{1 \text{ LSB}} \text{ [LSB]}$$

$$\text{Differential linearity error of digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}} - 1 \text{ LSB [LSB]}$$

$$1 \text{ LSB} = \frac{V_{FST} - V_{OT}}{1022} \text{ [V]}$$

N : A/D converter digital output value

V_{OT} : The voltage at which the digital output changes from “000_H” to “001_H.”

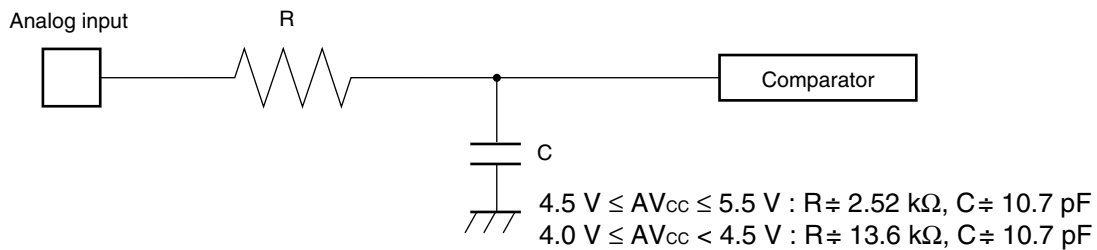
V_{FST} : The voltage at which the digital output changes from “3FE_H” to “3FF_H.”

7. Notes on A/D Converter Unit

Use the device such that the output impedance of the external circuits attached to the analog inputs satisfy the following conditions.

- It is recommended that the output impedance of external circuits are approx. 1.5 kΩ or lower (4.0 V ≤ AV_{CC} ≤ 5.5 V, sampling period = 0.5 μs)
- If an external capacitor is used, in consideration of the capacitive voltage division effect between the external capacitor and the internal on-chip capacitor, it is recommended that the capacitance of the external capacitor is several thousand times greater than the internal capacitor.
- If the output impedance of the external circuit is too high, the sampling period for the analog voltage may be insufficient.

• Analog input circuit model



Note : The values shown in this figure are reference values.

8. Flash Memory Program/Erase Characteristics

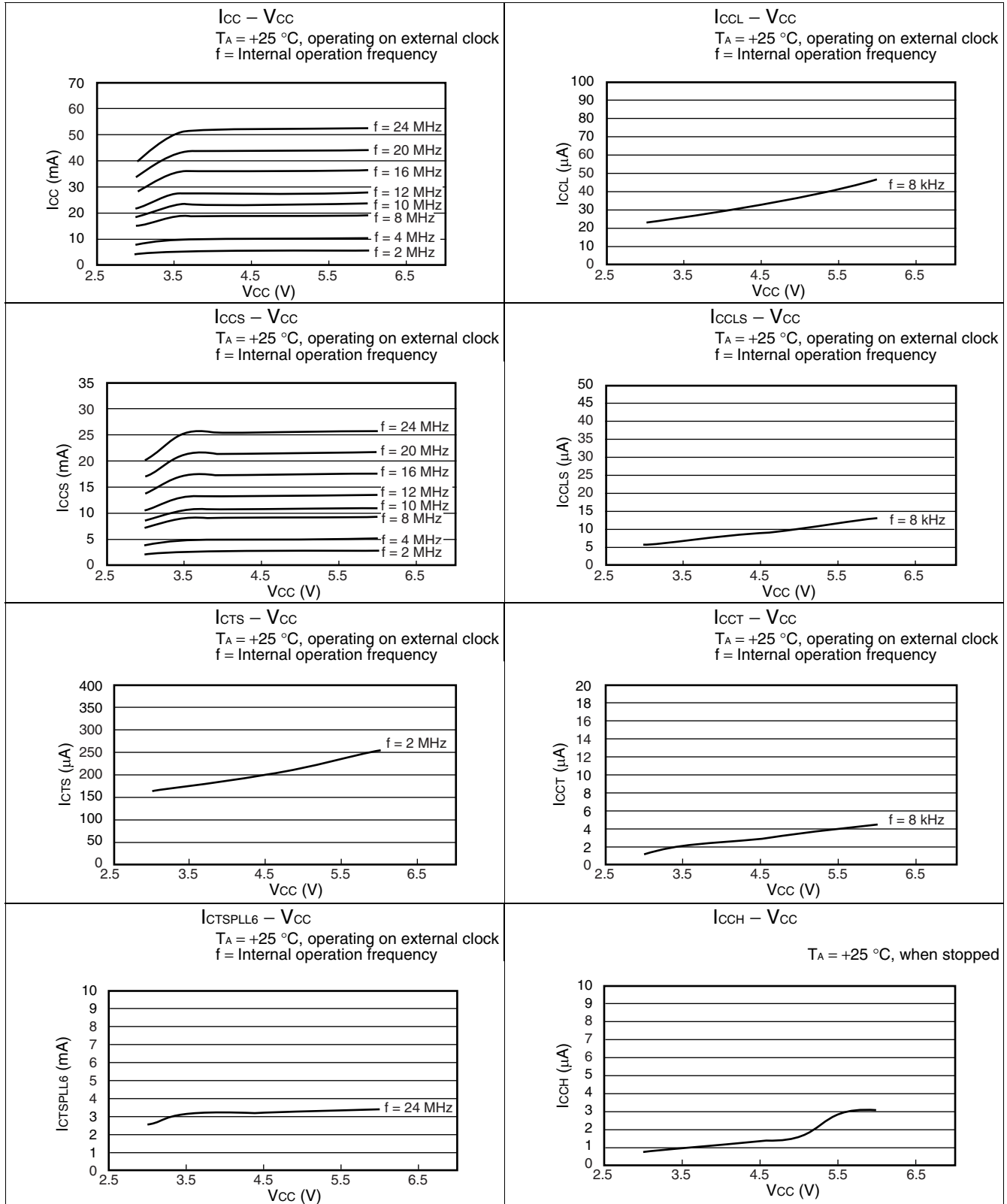
Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	T _A = +25 °C V _{CC} = 5.0 V	—	1	15	s	Excludes programming prior to erasure
Chip erase time		—	9	—	s	Excludes programming prior to erasure
Word (16-bit width) programming time		—	16	3600	μs	Except for the over head time of the system
Number of program/erase cycles	—	10000	—	—	cycle	
Flash data retention time	Average T _A = +85 °C	20	—	—	Year	*

* : This value is the result of evaluating the reliability of the technology (using Arrhenius equation to translate high temperature measurements into normalized value at +85 °C) .

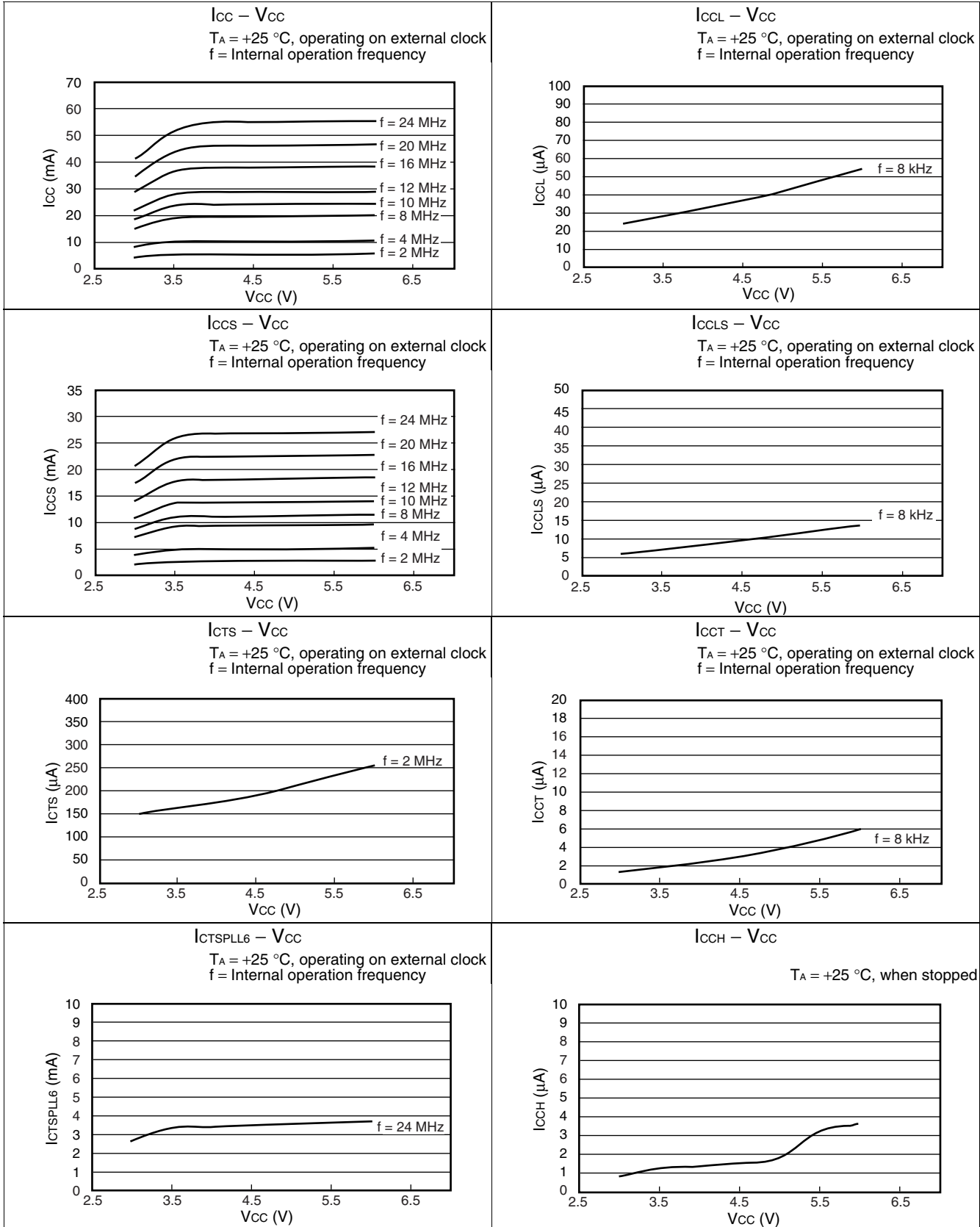
MB90860E Series

EXAMPLE CHARACTERISTICS

- MB90F867E, MB90F867ES

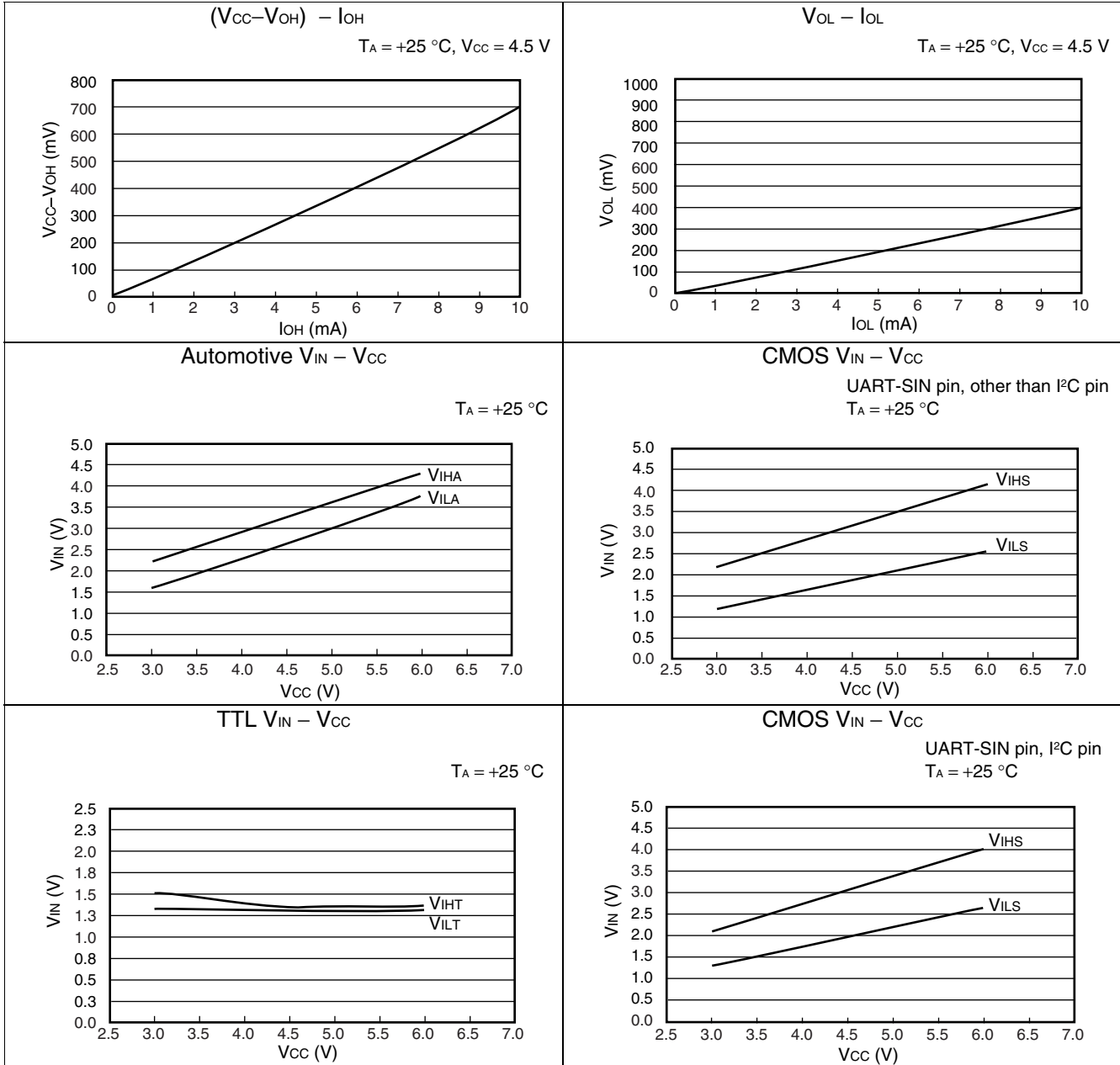


• MB90867E, MB90867ES



MB90860E Series

- I/O characteristics

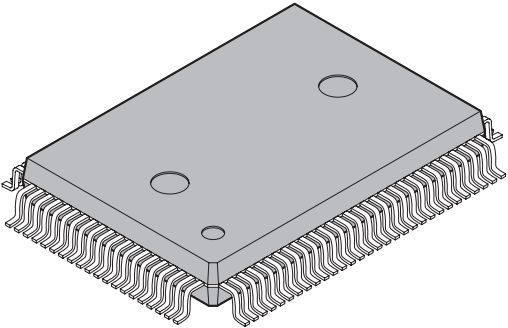


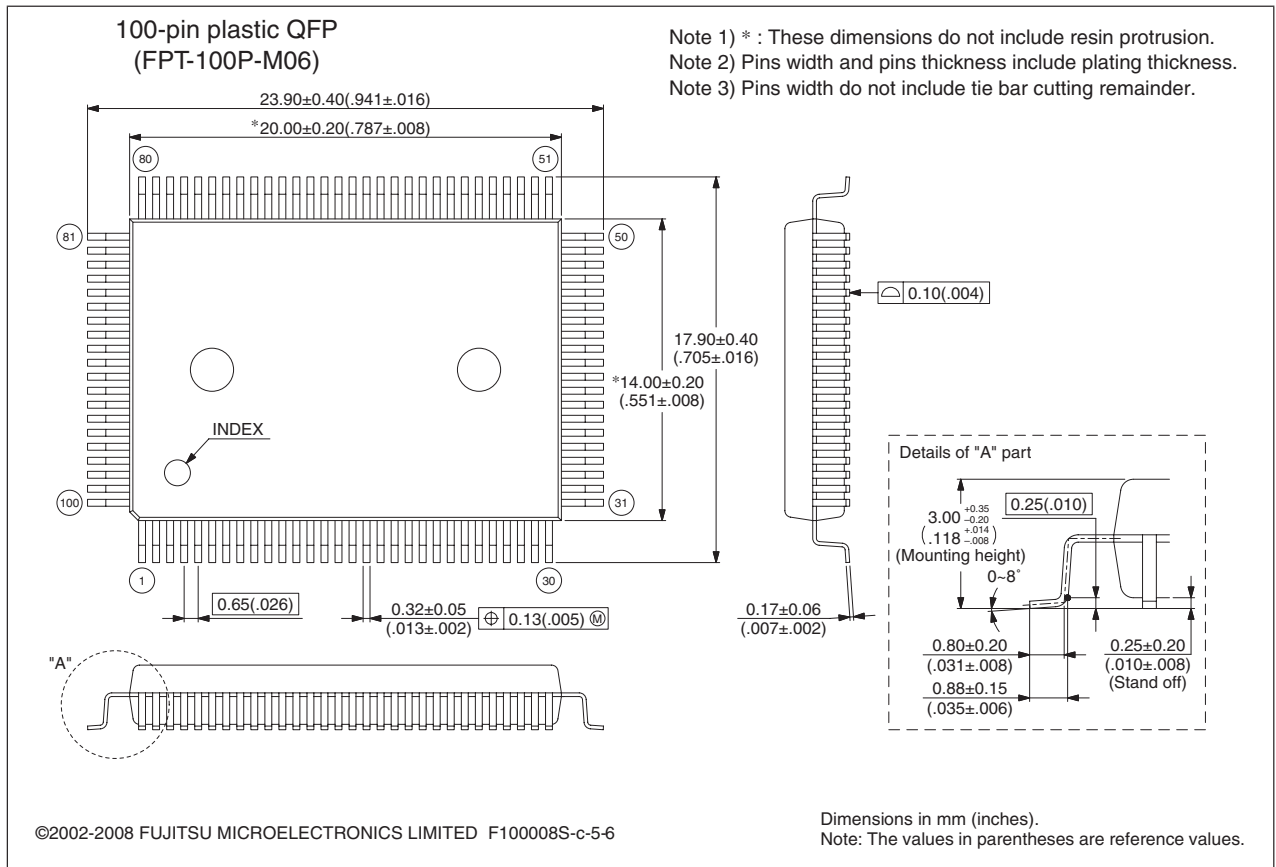
■ ORDERING INFORMATION

Part number	Package	Remarks
MB90F867EPF	100-pin plastic QFP (FPT-100P-M06)	Flash memory product
MB90F867ESPF		
MB90F867EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90F867ESPMC		
MB90867EPF	100-pin plastic QFP (FPT-100P-M06)	MASK ROM product
MB90867ESPF		
MB90867EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90867ESPMC		
MB90V340E-101CR	299-pin ceramic PGA (PGA-299C-A01)	Evaluation product
MB90V340E-102CR		

MB90860E Series

PACKAGE DIMENSIONS

<p>100-pin plastic QFP</p>  <p>(FPT-100P-M06)</p>	Lead pitch	0.65 mm
	Package width × package length	14.00 × 20.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	3.35 mm MAX
	Code (Reference)	P-QFP100-14×20-0.65

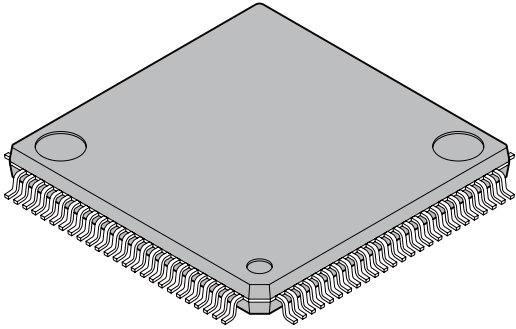


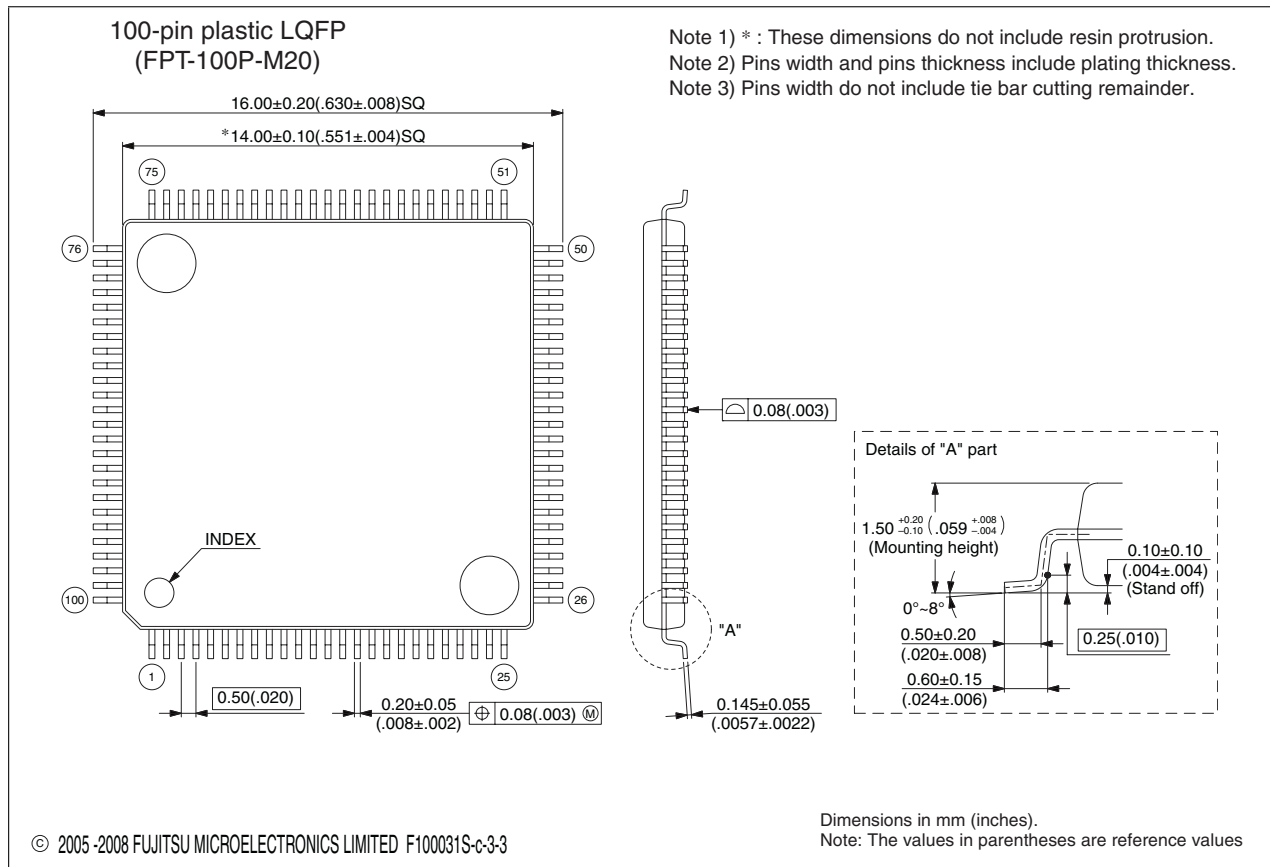
Please confirm the latest Package dimension by following URL.
<http://edevic.fujitsu.com/package/en-search/>

(Continued)

MB90860E Series

(Continued)

<p>100-pin plastic LQFP</p>  <p>(FPT-100P-M20)</p>	Lead pitch	0.50 mm
	Package width × package length	14.0 mm × 14.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm Max
	Weight	0.65 g
	Code (Reference)	P-LFQFP100-14×14-0.50



Please confirm the latest Package dimension by following URL.
<http://edevice.fujitsu.com/package/en-search/>

MB90860E Series

■ MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
—	—	Changed the package. FPT-100P-M05 → FPT-100P-M20
60	■ ELECTRICAL CHARACTERISTICS 5. A/D Converter	Changed the items for “Zero reading voltage” and “Full scale reading voltage”.
67	■ ORDERING INFORMATION	Changed the part numbers; MB90867EPFV → MB90367EPMC MB90867ESPFV → MB90867ESPMC MB90F867EPFV → MB90F867EPMC MB90F867ESPFV → MB90F867ESPMC MB90V340E-101 → MB90V340E-101CR MB90V340E-102 → MB90V340E-102CR
69	■ PACKAGE DIMENSIONS	Changed the package's figure. FPT-100P-M05 → FPT-100P-M20

The vertical lines marked in the left side of the page show the changes.

MEMO

MB90860E Series

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