

# 16-bit Proprietary Microcontroller

CMOS

## F<sup>2</sup>MC-16LX MB90370 Series

### MB90372/F372/V370

#### ■ DESCRIPTION

The MB90370 series is a line of general-purpose, 16-bit microcontrollers designed for those applications which require high-speed real-time processing. The instruction set is designed to be optimized for controller applications which inheriting the AT architecture of F<sup>2</sup>MC-16LX family and allow a wide range of control tasks to be processed efficiently at high speed.

A built-in LPC interface, serial IRQ and PS/2 interface simplifies communication with host CPU and PS/2 devices in computer system. Moreover, SMBus compliant I<sup>2</sup>C, comparator for battery control and A/D converter implements the smart battery control. With these features, the MB90370 series matches itself as keyboard controller with smart battery control.

While inheriting the AT architecture of the F<sup>2</sup>MC\* family, the instruction set for the F<sup>2</sup>MC-16LX CPU core of the MB90370 series incorporates additional instructions for high-level languages, supports extended addressing modes, and contains enhanced multiplication and division instructions as well as a substantial collection of improved bit manipulation instructions. In addition, the MB90370 series has an on-chip 32-bit accumulator which enables processing of long-word data.

\* : F<sup>2</sup>MC is the abbreviation of FUJITSU Flexible Microcontroller.

For the information for microcontroller supports, see the following web site.

<http://edevice.fujitsu.com/micom/en-support/>

## ■ FEATURES

- **Clock**
  - Embedded PLL clock multiplication circuit
  - Operating clock (PLL clock) can be selected from divided-by-2 of oscillation or one to four times the oscillation (at oscillation of 4 MHz to 16 MHz) .
  - Minimum instruction execution time of 62.5 ns (at oscillation of 4 MHz, four times the PLL clock, operation at V<sub>cc</sub> of 3.3 V)
- **CPU addressing space of 16M bytes**
  - Internal 24-bit addressing
- **Instruction set optimized for controller applications**
  - Rich data types (bit, byte, word, long word)
  - Rich addressing mode (23 types)
  - High code efficiency
  - Enhanced precision calculation realized by the 32-bit accumulator
- **Instruction set designed for high level language (C) and multi-task operations**
  - Adoption of system stack pointer
  - Enhanced pointer indirect instructions
  - Barrel shift instructions
- **Program patch function (2 address pointer)**
- **Improved execution speed**
  - 4-byte instruction queue
- **Powerful interrupt function**
  - Priority level programmable : 8 levels
  - 32 factors of stronger interrupt function
- **Automatic data transmission function independent of CPU operation**
  - Extended intelligent I/O service function (EI<sup>2</sup>OS)
  - Maximum 16 channels
- **Low-power consumption (standby) mode**
  - Sleep mode (mode in which CPU operating clock is stopped)
  - Timebase timer mode (mode in which operations other than timebase timer and watch timer are stopped)
  - Stop mode (mode in which all oscillations are stopped)
  - CPU intermittent operation mode
  - Watch mode
- **Package**
  - LQFP-144 (FPT-144P-M12 : 0.4 mm pitch)
- **Process**
  - CMOS technology

# MB90370 Series

## ■ PRODUCT LINEUP

Part number Parameter	MB90V370	MB90F372	MB90372
Classification	—	Flash type ROM	Mask ROM
ROM size	—	64K Bytes	
RAM size	15.7K Bytes	6K Bytes	
CPU function	Number of instruction : 351 Minimum execution time : 62.5 ns / 4 MHz (PLL × 4) Addressing mode : 23 Data bit length : 1, 8, 16 bits Maximum memory space : 16M Bytes		
I/O port	I/O port (N-channel) : 16 I/O port (CMOS) : 72 I/O port (CMOS with pull-up control) : 32 Total : 120		
16-bit reload timer	Reload timer : 4 channels Reload mode, single-shot mode or event count mode selectable		
16-bit PPG timer	PPG timer : 3 channels PWM mode or single-shot mode selectable		
Bit decoder	Bit decoder : 1 channel		
Parity generator	Parity generator : 1 channel Selectable odd/even parity		
PS/2 interface	PS/2 interface : 3 channels 4 selectable sampling clocks		
LPC interface	LPC bus interface : 1 channel Universal peripheral Interface : 4 channels GA20 output control : for UPI channel 0 only Data buffer array : 48 bytes		
LPC Standby (able to work in Stop/Time-base timer/ Watch mode)	Yes	No	No
Serial IRQ controller	Serial IRQ request : 6 channels LPC clock monitor / control		
UART	With full-duplex double buffer (variable data length) Clock asynchronized or clock synchronized transmission (with start and stop bits) can be selectively used		
I <sup>2</sup> C	I <sup>2</sup> C (SMBus compliant) : 1 channel Support I <sup>2</sup> C bus of Philips and the SMBus proposed by Intel Selectable packet error check Timeout detection function		
PC Arbitration under a particular condition*2	No	No	No

(Continued)

# MB90370 Series

(Continued)

Part number	MB90V370	MB90F372	MB90372
Parameter			
Multi-address I <sup>2</sup> C	Multi-address I <sup>2</sup> C (SMBus compliant) : 1 channel Support I <sup>2</sup> C bus of Philips and the SMBus proposed by Intel Selectable packet error check Timeout detection function 6 addresses support ALERT function		
Bridge circuit	Three bus connection routes can be switched by I <sup>2</sup> C / multi-address I <sup>2</sup> C		
Comparator	A comparator that can change the hysteresis width is contained Battery voltage, mounting/dismounting and instantaneous interruption can be detected Parallel and serial charging/discharging		
External interrupt	6 independent channels Selectable causes : Rise/fall edge, fall edge, "L" level or "H" level		
Key-on wake-up interrupt	8 independent channels Causes : "L" level		
8/10-bit A/D converter	8/10-bit resolution : 12 channels Conversion time : Less than 6.13 μs (16 MHz internal clock)		
8-bit D/A converter	8-bit resolution : 2 channels		
LCD controller/driver	Up to 9 SEG × 4 COM Selectable LCD output or CMOS I/O port		
Low-power consumption	Stop mode / Sleep mode / CPU intermittent operation mode / Watch mode		
Process	CMOS		
Package	PGA256	LQFP-144 (FPT-144P-M12 : 0.4 mm pitch)	
Operating voltage	3.0 V to 3.6 V @ 16 MHz *1		

\*1 : Varies with conditions such as the operating frequency (see Section "■ ELECTRICAL CHARACTERISTICS"), Assurance for the MB90V370 is given only for operation with a tool at power supply voltage of 3.0 V to 3.6 V, an operating temperature of 0 °C to +25 °C, and an operating frequency of 1 MHz to 16 MHz.

\*2 : I<sup>2</sup>C can detect the arbitration lost when another I<sup>2</sup>C starts another communication at the same time.

## ■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB90V370	MB90F372	MB90372
PGA256	○	X	X
FPT-144P-M12	X	○	○

○ : Available

X : Not available

Note : For more information about each package, see Section "■ PACKAGE DIMENSIONS".

## ■ DIFFERENCES AMONG PRODUCTS

### Memory size

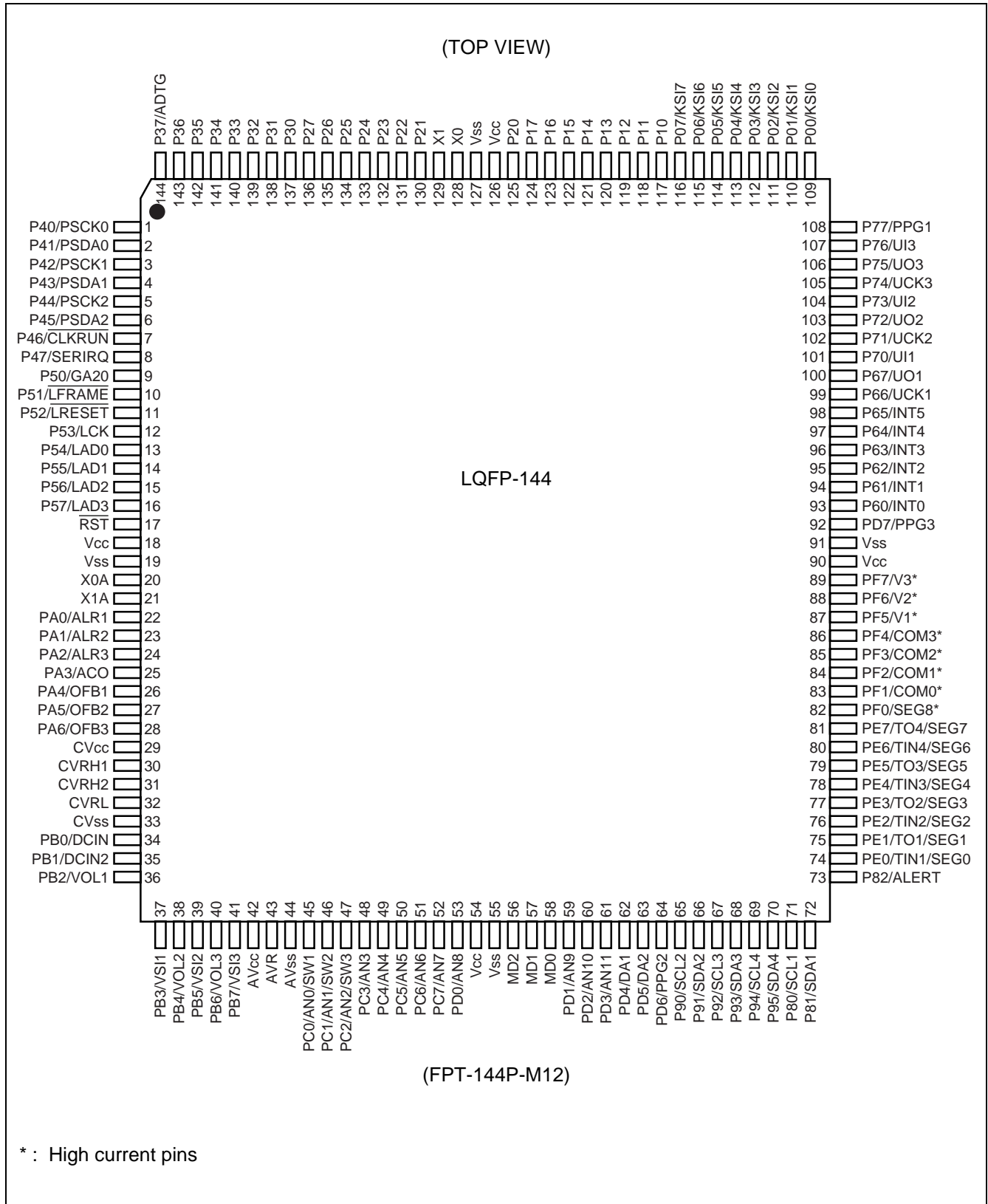
In evaluation with an evaluation product, note the difference between the evaluation product and the product actually used. The following items must be taken into consideration.

- The MB90V370 does not have an internal ROM, however, operations equivalent to chips with an internal ROM can be evaluated by using a dedicated development tool, enabling selection of ROM size by settings of the development tool.
- In the MB90V370, images from FF4000<sub>H</sub> to FFFFFFF<sub>H</sub> are mapped to bank 00, and FF0000<sub>H</sub> to FF3FFF<sub>H</sub> are mapped to bank FF only. (This setting can be changed by the development tool configuration.)
- In the MB90372/F372, images from FF4000<sub>H</sub> to FFFFFFF<sub>H</sub> are mapped to bank 00, and FF0000<sub>H</sub> to FF3FFF<sub>H</sub> are mapped to bank FF only.

# MB90370 Series

## PIN ASSIGNMENT

• MB90372/F372



## ■ PIN DESCRIPTION

Pin no. LQFP-144	Pin name	I/O circuit	Pin status during reset	Function
128, 129	X0, X1	A	Oscillating	Main oscillation pins.
20, 21	X0A, X1A	A	Oscillating	Sub-clock oscillation pins.
17	$\overline{\text{RST}}$	B	Reset input	External reset input pin.
58, 57, 56	MD0 to MD2	C	Mode input	Input pin for operation mode specification. Connect this pin directly to Vcc or Vss.
109 to 116	P00 to P07	D	Port input	General-purpose I/O ports.
	KSI0 to KSI7			Can be used as key-on wake-up interrupt input channel 0 to channel 7. Input is enabled when 1 is set in EICR : EN0 to EN7 in standby mode.
117 to 124	P10 to P17	E		General-purpose I/O ports.
125, 130 to 136	P20 to P27	E		General-purpose I/O ports.
137 to 143	P30 to P36	E		General-purpose I/O ports.
144	P37	E		General-purpose I/O ports.
	ADTG			External trigger input pin (ADTG) for the A/D converter.
1	P40	F		General-purpose N-ch open-drain I/O port.
	PSCK0			Serial clock I/O pin for PS/2 interface channel 0. This function is selected when PS/2 interface channel 0 is enabled.
2	P41	F		General-purpose N-ch open-drain I/O port.
	PSDA0			Serial data I/O pin for PS/2 interface channel 0. This function is selected when PS/2 interface channel 0 is enabled.
3	P42	F		General-purpose N-ch open-drain I/O port.
	PSCK1			Serial clock I/O pin for PS/2 interface channel 1. This function is selected when PS/2 interface channel 1 is enabled.
4	P43	F		General-purpose N-ch open-drain I/O port.
	PSDA1			Serial data I/O pin for PS/2 interface channel 1. This function is selected when PS/2 interface channel 1 is enabled.
5	P44	F		General-purpose N-ch open-drain I/O port.
	PSCK2			Serial clock I/O pin for PS/2 interface channel 2. This function is selected when PS/2 interface channel 2 is enabled.
6	P45	F		General-purpose N-ch open-drain I/O port.
	PSDA2			Serial data I/O pin for PS/2 interface channel 2. This function is selected when PS/2 interface channel 2 is enabled.
7	P46	G		General-purpose N-ch open-drain I/O port.
	$\overline{\text{CLKRUN}}$		LPC clock status / restart request I/O pin for serial IRQ controller. This function is selected when serial IRQ and LPC clock restart request is enabled.	

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# MB90370 Series

Pin no. LQFP-144	Pin name	I/O circuit	Pin status during reset	Function
8	P47	H	Port input	General-purpose I/O port.
	SERIRQ			Serial IRQ data I/O pin for serial IRQ controller. This function is selected when serial IRQ is enabled.
9	P50	H		General-purpose I/O port.
	GA20			GA20 output for LPC interface. This function is selected when GA20 function is enabled.
10	P51	H		General-purpose I/O port.
	$\overline{\text{LFRAME}}$			LFRAME input for LPC interface. This function is selected when LPC interface is enabled.
11	P52	H		General-purpose I/O port.
	$\overline{\text{LRESET}}$			Reset input for LPC interface. This function is selected when LPC interface is enabled.
12	P53	H		General-purpose I/O port.
	LCK			Clock input for LPC interface. This function is selected when LPC interface is enabled.
13 to 16	P54 to P57	H		General-purpose I/O ports.
	LAD0 to LAD3			Address/Data I/O for LPC interface. This function is selected when LPC interface is enabled.
93 to 98	P60 to P65	I		General-purpose I/O ports.
	INT0 to INT5			Can be used as DTP/external interrupt request input channel 0 to 5. Input is enabled when 1 is set in ENIR : EN0 to EN5 in standby mode.
99	P66	I		General-purpose I/O port.
	UCK1			Serial clock I/O pin for UART channel 1. This function is enabled when UART channel 1 enables clock output.
100	P67	I	General-purpose I/O port.	
	UO1		Serial data output pin for UART channel 1. This function is enabled when UART channel 1 enables data output.	
101	P70	I	General-purpose I/O port.	
	UI1		Serial data input pin for UART channel 1. While UART channel 1 is operating for input, the input of this pin is used as required and must not be used for any other input.	
102	P71	I	General-purpose I/O port.	
	UCK2		Serial clock I/O pin for UART channel 2. This function is enabled when UART channel 2 enables clock output.	

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# MB90370 Series

Pin no. LQFP-144	Pin name	I/O circuit	Pin status during reset	Function
103	P72	I	Port input	General-purpose I/O port.
	UO2			Serial data output pin for UART channel 2. This function is enabled when UART channel 2 enables data output.
104	P73	I		General-purpose I/O port.
	UI2			Serial data input pin for UART channel 2. While UART channel 2 is operating for input, the input of this pin is used as required and must not be used for any other input.
105	P74	I		General-purpose I/O port.
	UCK3			Serial clock I/O pin for UART channel 3. This function is enabled when UART channel 3 enables clock output.
106	P75	I		General-purpose I/O port.
	UO3			Serial data output pin for UART channel 3. This function is enabled when UART channel 3 enables data output.
107	P76	I		General-purpose I/O port.
	UI3			Serial data input pin for UART channel 3. While UART channel 3 is operating for input, the input of this pin is used as required and must not be used for any other input.
108	P77	I		General-purpose I/O port.
	PPG1			Output pin for PPG channel 1. This function is enabled when PPG channel 1 output is enabled.
71	P80	T		General-purpose N-ch open-drain I/O port.
	SCL1			Serial clock I/O pin for multi-address I <sup>2</sup> C.
72	P81	T		General-purpose N-ch open-drain I/O port.
	SDA1			Serial data I/O pin for multi-address I <sup>2</sup> C.
73	P82	J		General-purpose N-ch open-drain I/O port.
	ALERT			ALERT output pin for multi-address I <sup>2</sup> C.
65	P90	T		General-purpose N-ch open-drain I/O port.
	SCL2			Serial clock I/O pin for bridge circuit.
66	P91	T		General-purpose N-ch open-drain I/O port.
	SDA2			Serial data I/O pin for bridge circuit.
67	P92	T		General-purpose N-ch open-drain I/O port.
	SCL3			Serial clock I/O pin for bridge circuit.
68	P93	T	General-purpose N-ch open-drain I/O port.	
	SDA3		Serial data I/O pin for bridge circuit.	

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# MB90370 Series

Pin no. LQFP-144	Pin name	I/O circuit	Pin status during reset	Function
69	P94	T	Port input	General-purpose N-ch open-drain I/O port.
	SCL4			Serial clock I/O pin for bridge circuit.
70	P95	T		General-purpose N-ch open-drain I/O port.
	SDA4			Serial data I/O pin for bridge circuit.
22 to 24	PA0 to PA2	H		General-purpose I/O ports.
	ALR1 to ALR3			Alarm signal output when battery 1 to 3 run down in comparator circuit.
25	PA3	H		General-purpose I/O port.
	ACO			AC power set signal output in comparator circuit.
26 to 28	PA4 to PA6	H		General-purpose I/O ports.
	OFB1 to OFB3			Battery 1 to 3 discharge control signal output in comparator circuit.
34, 35	PB0 to PB1	K		General-purpose I/O ports.
	DCIN to DCIN2			AC power monitoring input in comparator circuit.
36	PB2	K		General-purpose I/O port.
	VOL1			Battery 1 power instantaneous interruption monitoring input in comparator circuit.
37	PB3	K	General-purpose I/O port.	
	VSI1		Battery 1 indicator monitoring input in comparator circuit.	
38	PB4	K	General-purpose I/O port.	
	VOL2		Battery 2 power instantaneous interruption monitoring input in comparator circuit.	
39	PB5	K	General-purpose I/O port.	
	VSI2		Battery 2 indicator monitoring input in comparator circuit.	
40	PB6	K	General-purpose I/O port.	
	VOL3		Battery 3 power instantaneous interruption monitoring input in comparator circuit.	
41	PB7	K	General-purpose I/O port.	
	VSI3		Battery 3 indicator monitoring input in comparator circuit.	
45 to 47	PC0 to PC2	L	Comparator input or A/D input	General-purpose I/O ports.
	SW1 to SW3		Battery 1 to 3 mount / dismount detection input in comparator circuit.	
	AN0 to AN2		A/D converter analog input pin 0 to 2. This function is enabled when the analog input specification is enabled (ADER1) .	

(Continued)

# MB90370 Series

Pin no. LQFP-144	Pin name	I/O circuit	Pin status during reset	Function
48 to 52	PC3 to PC7	M	A/D input	General-purpose I/O ports.
	AN3 to AN7			A/D converter analog input pin 3 to 7. This function is enabled when the analog input specification is enabled (ADER1) .
53, 59 to 61	PD0 to PD3	M		General-purpose I/O ports.
	AN8 to AN11			A/D converter analog input pin 8 to 11. This function is enabled when the analog input specification is enabled (ADER2) .
62, 63	PD4, PD5	N	Port input	General-purpose I/O ports.
	DA1, DA2			D/A converter analog output 1 to 2. This function is selected when D/A converter is enabled.
64, 92	PD6, PD7	H		General-purpose I/O ports.
	PPG2, PPG3			Output pin for PPG channel 2 to 3. This function is selected when PPG channel 2 to 3 output is enabled.
74	PE0	O	General-purpose I/O port.	
	SEG0		Segment output pin for LCD controller/driver. This function is selected when LCD segment output is enabled.	
	TIN1		External clock input pin for reload timer 1.	
75	PE1	O	General-purpose I/O port.	
	SEG1		Segment output pin for LCD controller/driver. This function is selected when LCD segment output is enabled.	
	TO1		Event output pin for reload timer 1.	
76	PE2	O	General-purpose I/O port.	
	SEG2		Segment output pin for LCD controller/driver. This function is selected when LCD segment output is enabled.	
	TIN2		External clock input pin for reload timer 2.	
77	PE3	O	General-purpose I/O port.	
	SEG3		Segment output pin for LCD controller/driver. This function is selected when LCD segment output is enabled.	
	TO2		Event output pin for reload timer 2.	
78	PE4	O	General-purpose I/O port.	
	SEG4		Segment output pin for LCD controller/driver. This function is selected when LCD segment output is enabled.	
	TIN3		External clock input pin for reload timer 3.	
79	PE5	O	General-purpose I/O port.	
	SEG5		Segment output pin for LCD controller/driver. This function is selected when LCD segment output is enabled.	
	TO3		Event output pin for reload timer 3.	

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# MB90370 Series

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Pin no. LQFP-144	Pin name	I/O circuit	Pin status during reset	Function
80	PE6	O	Port input	General-purpose I/O port.
	SEG6			Segment output pin for LCD controller/driver. This function is selected when LCD segment output is enabled.
	TIN4			External clock input pin for reload timer 4.
81	PE7	O		General-purpose I/O port.
	SEG7			Segment output pin for LCD controller/driver. This function is selected when LCD segment output is enabled.
	TO4			Event output pin for reload timer 4.
82	PF0	P		General-purpose I/O port.
	SEG8			Segment output pin for LCD controller/driver. This function is selected when LCD segment output is enabled.
83 to 86	PF1 to PF4	P		General-purpose I/O port.
	COM0 to COM3			COM output pin for LCD controller/driver. This function is selected when LCD COM output is enabled.
87 to 89	PF5 to PF7	Q	Power input	General-purpose I/O port.
	V1 to V3			Power input pin for LCD controller/driver. This function is selected when external voltage divider is enabled.
42	AV <sub>cc</sub>	R	Power input	V <sub>cc</sub> power input pin for analog circuits.
43	AVR	S		V <sub>ref+</sub> input pin for the A/D converter. This voltage must not exceed V <sub>cc</sub> . V <sub>ref-</sub> is fixed to AV <sub>SS</sub> .
44	AV <sub>ss</sub>	R		V <sub>ss</sub> power input pin for analog circuits.
29	CV <sub>cc</sub>	R	Power input	V <sub>cc</sub> power input pin for analog circuits.
30	CVRH1	R		Standard power input pin of the comparator.
31	CVRH2	R		
32	CVRL	R		
33	CV <sub>ss</sub>	R		
19, 55, 91, 127	V <sub>ss</sub>	–	Power input	Power (0 V) input pin.
18, 54, 90, 126	V <sub>cc</sub>	–		Power (3.3 V) input pin.

## I/O CIRCUIT TYPE

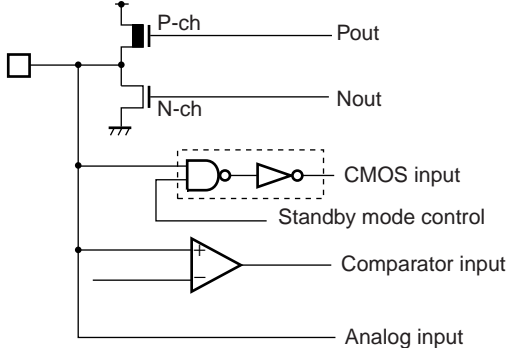
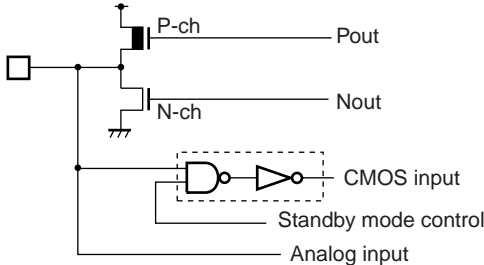
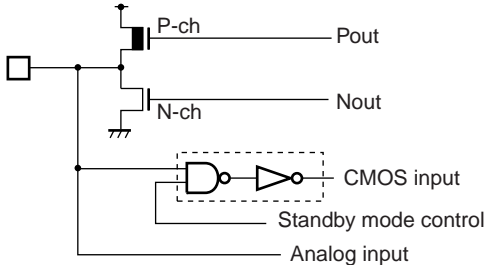
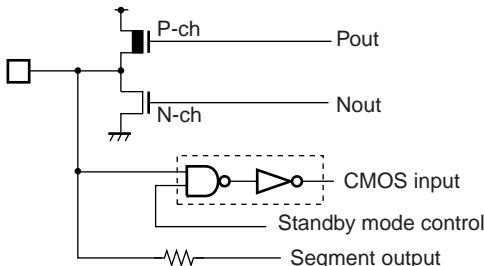
Type	Circuit	Remarks
A		<p>Main/Sub clock (main/sub clock crystal oscillator)</p> <ul style="list-style-type: none"> <li>• High-rate oscillation feedback resistor of approximately 1 MΩ</li> <li>• Low-rate oscillation feedback resistor of approximately 10 MΩ</li> </ul>
B		<ul style="list-style-type: none"> <li>• Hysteresis input</li> <li>• Pull-up resistor approximately 50 kΩ</li> </ul>
C		<ul style="list-style-type: none"> <li>• Hysteresis input</li> </ul>
D		<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• Hysteresis input</li> <li>• Selectable pull-up resistor approximately 50 kΩ</li> <li>• <math>I_{OL} = 4 \text{ mA}</math></li> </ul>
E		<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• CMOS input</li> <li>• Selectable pull-up resistor approximately 50 kΩ</li> <li>• <math>I_{OL} = 4 \text{ mA}</math></li> </ul>
F		<ul style="list-style-type: none"> <li>• N-ch open-drain output</li> <li>• Hysteresis input</li> <li>• <math>I_{OL} = 4 \text{ mA}</math></li> <li>• 5 V tolerant</li> </ul>

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# MB90370 Series

Type	Circuit	Remarks
G		<ul style="list-style-type: none"> <li>• N-ch open-drain output</li> <li>• CMOS input</li> <li>• <math>I_{OL} = 4 \text{ mA}</math></li> </ul>
H		<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• CMOS input</li> <li>• <math>I_{OL} = 4 \text{ mA}</math></li> </ul>
I		<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• Hysteresis input</li> <li>• <math>I_{OL} = 4 \text{ mA}</math></li> </ul>
J		<ul style="list-style-type: none"> <li>• N-ch open-drain output</li> <li>• CMOS input</li> <li>• <math>I_{OL} = 4 \text{ mA}</math></li> <li>• 5 V tolerant</li> </ul>
K		<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• CMOS input</li> <li>• Comparator input</li> <li>• <math>I_{OL} = 4 \text{ mA}</math></li> </ul>

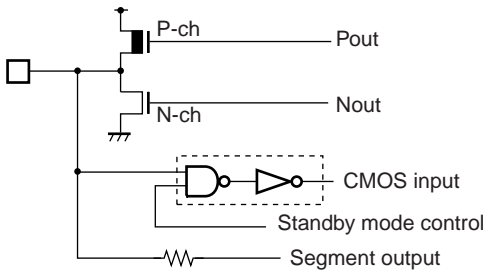
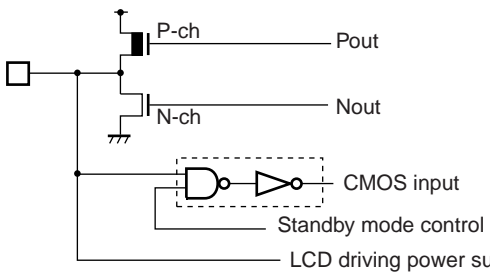
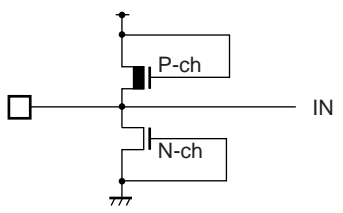
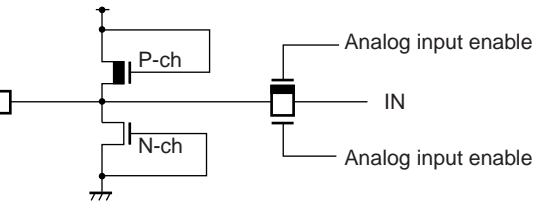
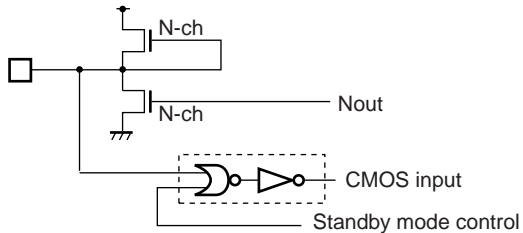
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Type	Circuit	Remarks
L		<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• CMOS input</li> <li>• Comparator input</li> <li>• A/D analog input</li> <li>• <math>I_{OL} = 4 \text{ mA}</math></li> </ul>
M		<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• CMOS input</li> <li>• A/D analog input</li> <li>• <math>I_{OL} = 4 \text{ mA}</math></li> </ul>
N		<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• CMOS input</li> <li>• D/A analog output</li> <li>• <math>I_{OL} = 4 \text{ mA}</math></li> </ul>
O		<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• CMOS input</li> <li>• Segment output</li> <li>• <math>I_{OL} = 4 \text{ mA}</math></li> </ul>

(Continued)

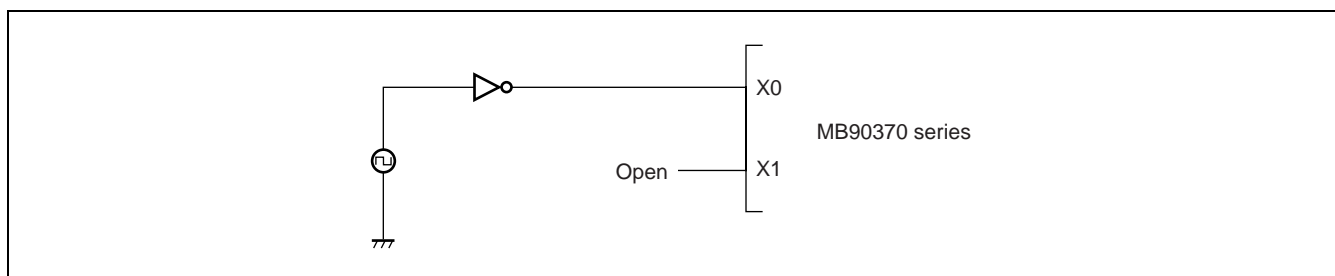
# MB90370 Series

(Continued)

Type	Circuit	Remarks
P		<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• CMOS input</li> <li>• Segment output</li> <li>• <math>I_{OL} = 12 \text{ mA}</math></li> </ul>
Q		<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• CMOS input</li> <li>• LCD driving power supply</li> <li>• <math>I_{OL} = 12 \text{ mA}</math></li> </ul>
R		<ul style="list-style-type: none"> <li>• Power supply input protection circuit</li> </ul>
S		<ul style="list-style-type: none"> <li>• A/D converter reference voltage (AVR) input pin with protection circuit</li> </ul>
T		<ul style="list-style-type: none"> <li>• N-ch open-drain output</li> <li>• CMOS input</li> <li>• <math>I_{OL} = 4 \text{ mA}</math></li> <li>• 5 V tolerant</li> </ul>

## ■ HANDLING DEVICES

- Be sure that the maximum rated voltage is not exceeded (latch-up prevention) .  
A latch-up may occur on a CMOS IC if a voltage higher than  $V_{CC}$  or lower than  $V_{SS}$  is applied to an input or output pin other than medium-to-high voltage pins. A latch-up may also occur if a voltage higher than the rating is applied between  $V_{CC}$  and  $V_{SS}$ . A latch-up causes a rapid increase in the power supply current, which can result in thermal damage to an element. Take utmost care that the maximum rated voltage is not exceeded. When turning the power on or off to analog circuits, be sure that the analog supply voltages ( $AV_{CC}$ ,  $CV_{CC}$ ,  $AVR$ ,  $CVRH1$ ,  $CVRH2$  and  $CVRL$ ) and analog input voltage do not exceed the digital supply voltage ( $V_{CC}$ ) .
- Stabilize the supply voltages  
Even within the operation guarantee range of the  $V_{CC}$  supply voltage, a malfunction can be caused if the supply voltage undergoes a rapid change. For voltage stabilization guidelines, the  $V_{CC}$  ripple fluctuations (P-P value) at commercial frequencies (50 Hz to 60 Hz) should be suppressed to 10% or less of the reference  $V_{CC}$  value. During a momentary change such as when switching a supply voltage, voltage fluctuations should also be suppressed so that the transient fluctuation rate is 0.1 V/ms or less.
- Power-on  
To prevent a malfunction in the built-in voltage drop circuit, secure 50  $\mu$ s (between 0.2 V and 1.8 V) or more for the voltage rise time during power-on.
- Treatment of unused input pins  
An unused input pin may cause a malfunction if it is left open. Every unused input pin should be pulled up or down.
- Treatment of A/D converter, D/A converter and comparator power pin  
When the A/D converter, D/A converter and comparator is not used, connect the pins as follows :  $AV_{CC} = CV_{CC} = V_{CC}$ ,  $AV_{SS} = AVR = CV_{SS} = CVRL = CVRH1 = CVRH2 = V_{SS}$ .
- Notes on external clock  
When an external clock is used, the oscillation stabilization wait time is required at power-on reset or at cancellation of sub-clock mode or stop mode. As shown in diagram below, when an external clock is used, connect only the X0 pin and leave the X1 pin open.

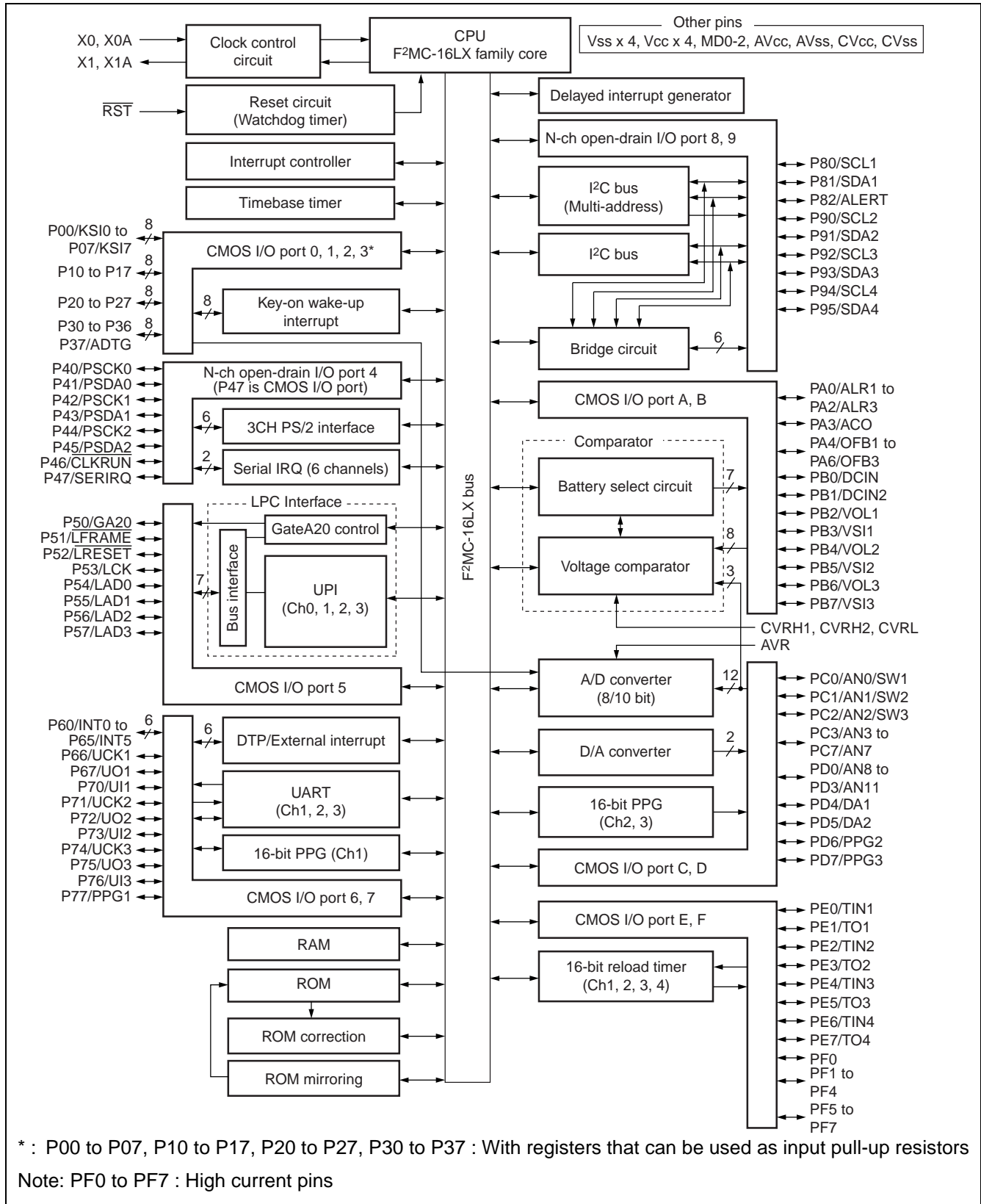


- Power supply pins  
When a device has two or more  $V_{CC}$  or  $V_{SS}$  pins, the pins that should have equal potential are connected within the device in order to prevent a latch-up or other malfunction. To reduce extraneous emission, to prevent a malfunction of the strobe signal due to an increase in the group level, and to maintain the local output current rating, connect all these power supply pins to an external power supply and ground them.  
The current source should be connected to the  $V_{CC}$  and  $V_{SS}$  pins of the device with minimum impedance. It is recommended that a bypass capacitor of about 0.1  $\mu$ F be connected near the terminals between  $V_{CC}$  and  $V_{SS}$ .

- Analog power-on sequence of A/D converter, D/A converter and comparator  
The power to the A/D converter, D/A converter and comparator ( $AV_{CC}$ ,  $CV_{CC}$ , AVR, CVRH1, CVRH2 and CVRL) and analog inputs (AN0 to AN11, VOL1 to VOL3, VSI1 to VSI3, SW1 to SW3, DCIN and DCIN2) must be turned on after the power to the digital circuits ( $V_{CC}$ ) is turned on. When turning off the power, turn off the power to the digital circuits ( $V_{CC}$ ) after turning off the power to the A/D converter, D/A converter, comparator and analog inputs. When the power is turned on or off, AVR should not exceed  $AV_{CC}$ . And CVRH1, CVRH2 and CVRL should not exceed  $CV_{CC}$ . Also, when a pin that is used for A/D analog input is used as an input port, the input voltage should not exceed  $AV_{CC}$ . And when comparator analog input is also used as an input port, the input voltage should not exceed  $CV_{CC}$ . (The power to the analog circuits and the power to the digital circuits can be simultaneously turned on or off.)
- Caution on Operations during PLL Clock Mode  
If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

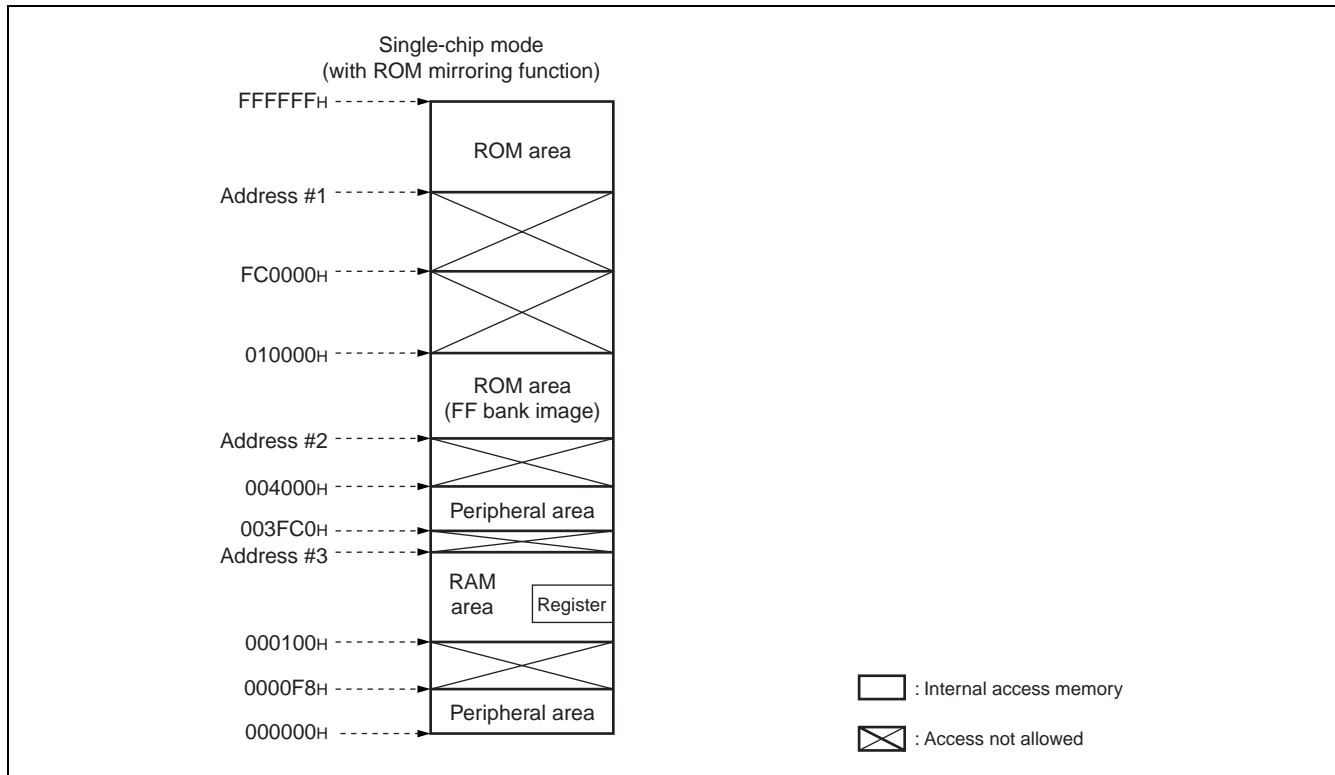
## ■ BLOCK DIAGRAM

• MB90372/F372/V370



# MB90370 Series

## MEMORY MAP



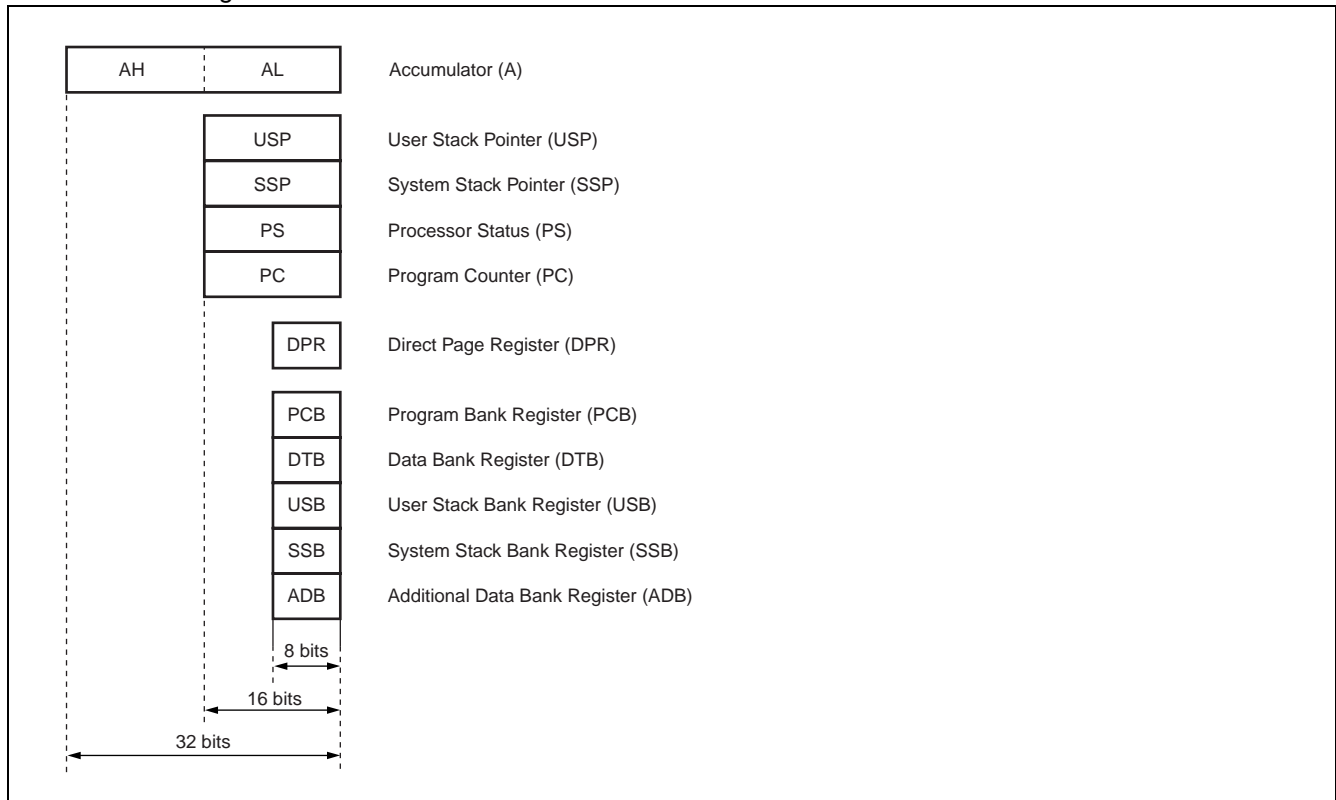
Model	Address #1	Address #2	Address #3
MB90372	FF0000H	004000H	001900H
MB90F372	FF0000H	004000H	001900H
MB90V370	FF0000H*	004000H*	003FC0H

\* : The MB90V370 does not contain ROM. Assume that the development tool uses these area for its ROM decode areas.

Note : ROM data in the FF bank can be seen as an image in the higher 00 bank to validate the small model C compiler. Because addresses of the 16 low-order bits in the FF bank are the same, the table in ROM can be referenced without the “far” specification. For example, when 00C000H is accessed, the contents of ROM at FFC000H are actually accessed. The ROM area in the FF bank exceeds 48 kilobytes, and all areas cannot be seen as images in the 00 bank. Because ROM data from FF4000H to FFFFFFFH is seen as an image at 004000H to 00FFFFH, the ROM data table should be stored in the area from FF4000H to FFFFFFFH.

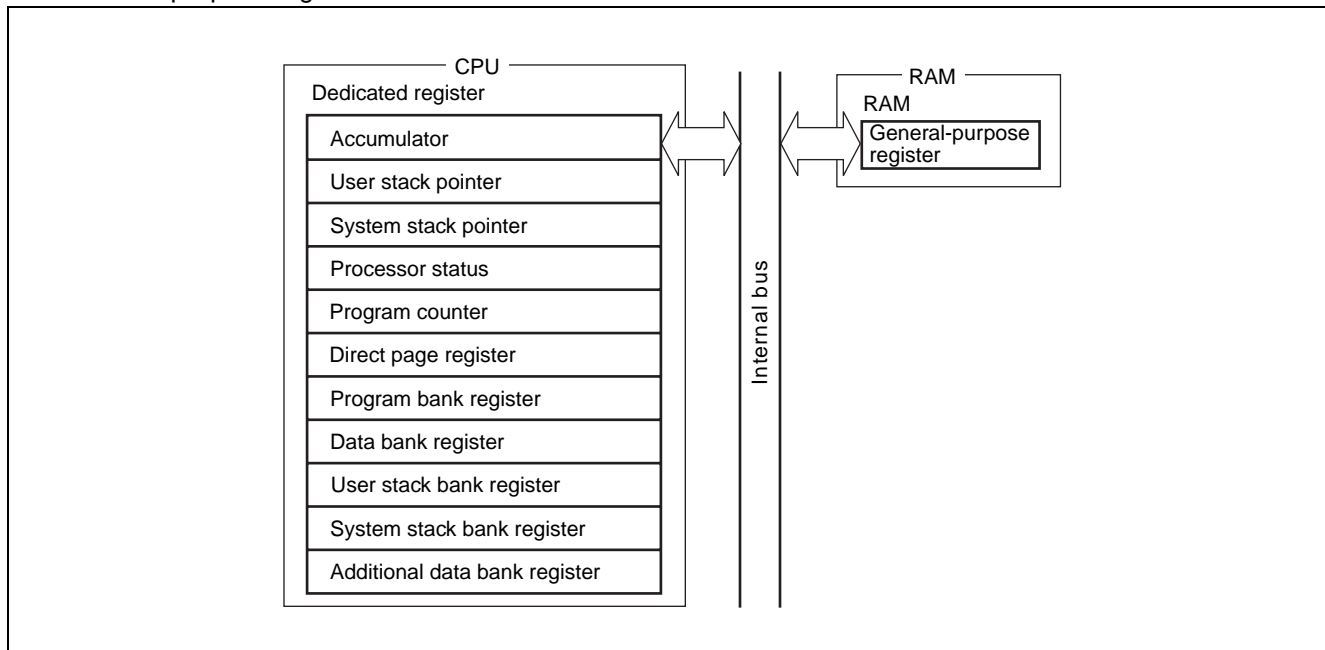
## ■ F<sup>2</sup>MC-16LX CPU PROGRAMMING MODEL

- Dedicated registers

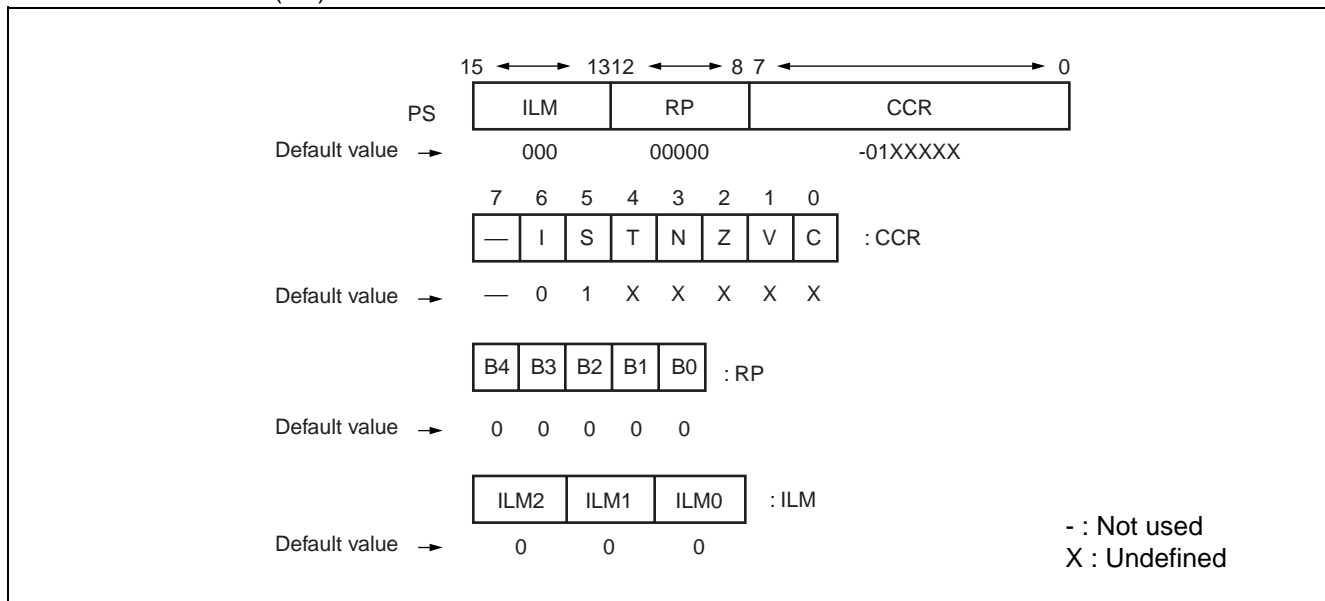


# MB90370 Series

- General-purpose registers



- Processor status (PS)



## ■ I/O MAP

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
000000 <sub>H</sub>	PDR0	Port 0 data register	R/W	R/W	Port 0	XXXXXXXX <sub>B</sub>
000001 <sub>H</sub>	PDR1	Port 1 data register	R/W	R/W	Port 1	XXXXXXXX <sub>B</sub>
000002 <sub>H</sub>	PDR2	Port 2 data register	R/W	R/W	Port 2	XXXXXXXX <sub>B</sub>
000003 <sub>H</sub>	PDR3	Port 3 data register	R/W	R/W	Port 3	XXXXXXXX <sub>B</sub>
000004 <sub>H</sub>	PDR4	Port 4 data register	R/W	R/W	Port 4	X1111111 <sub>B</sub>
000005 <sub>H</sub>	PDR5	Port 5 data register	R/W	R/W	Port 5	XXXXXXXX <sub>B</sub>
000006 <sub>H</sub>	PDR6	Port 6 data register	R/W	R/W	Port 6	XXXXXXXX <sub>B</sub>
000007 <sub>H</sub>	PDR7	Port 7 data register	R/W	R/W	Port 7	XXXXXXXX <sub>B</sub>
000008 <sub>H</sub>	PDR8	Port 8 data register	R/W	R/W	Port 8	----111 <sub>B</sub>
000009 <sub>H</sub>	PDR9	Port 9 data register	R/W	R/W	Port 9	--111111 <sub>B</sub>
00000A <sub>H</sub>	PDRA	Port A data register	R/W	R/W	Port A	-XXXXXXXX <sub>B</sub>
00000B <sub>H</sub>	PDRB	Port B data register	R/W	R/W	Port B	XXXXXXXX <sub>B</sub>
00000C <sub>H</sub>	PDRC	Port C data register	R/W	R/W	Port C	XXXXXXXX <sub>B</sub>
00000D <sub>H</sub>	PDRD	Port D data register	R/W	R/W	Port D	XXXXXXXX <sub>B</sub>
00000E <sub>H</sub>	PDRE	Port E data register	R/W	R/W	Port E	XXXXXXXX <sub>B</sub>
00000F <sub>H</sub>	PDRF	Port F data register	R/W	R/W	Port F	XXXXXXXX <sub>B</sub>
000010 <sub>H</sub>	DDR0	Port 0 direction register	R/W	R/W	Port 0	00000000 <sub>B</sub>
000011 <sub>H</sub>	DDR1	Port 1 direction register	R/W	R/W	Port 1	00000000 <sub>B</sub>
000012 <sub>H</sub>	DDR2	Port 2 direction register	R/W	R/W	Port 2	00000000 <sub>B</sub>
000013 <sub>H</sub>	DDR3	Port 3 direction register	R/W	R/W	Port 3	00000000 <sub>B</sub>
000014 <sub>H</sub>	DDR4	Port 4 direction register	R/W	R/W	Port 4	0----- <sub>B</sub>
000015 <sub>H</sub>	DDR5	Port 5 direction register	R/W	R/W	Port 5	00000000 <sub>B</sub>
000016 <sub>H</sub>	DDR6	Port 6 direction register	R/W	R/W	Port 6	00000000 <sub>B</sub>
000017 <sub>H</sub>	DDR7	Port 7 direction register	R/W	R/W	Port 7	00000000 <sub>B</sub>
000018 <sub>H</sub>	PGDR	Parity generator data register	R/W	R/W	Parity generator	XXXXXXXX <sub>B</sub>
000019 <sub>H</sub>	PGCSR	Parity generator control status register	R/W	R/W		X-----0 <sub>B</sub>
00001A <sub>H</sub>	DDRA	Port A direction register	R/W	R/W	Port A	-0000000 <sub>B</sub>
00001B <sub>H</sub>	DDRB	Port B direction register	R/W	R/W	Port B	00000000 <sub>B</sub>
00001C <sub>H</sub>	DDRC	Port C direction register	R/W	R/W	Port C	00000000 <sub>B</sub>
00001D <sub>H</sub>	DDRD	Port D direction register	R/W	R/W	Port D	00000000 <sub>B</sub>
00001E <sub>H</sub>	DDRE	Port E direction register	R/W	R/W	Port E	00000000 <sub>B</sub>
00001F <sub>H</sub>	DDRF	Port F direction register	R/W	R/W	Port F	00000000 <sub>B</sub>

(Continued)

# MB90370 Series

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
000020 <sub>H</sub>	SMR1	Serial mode register 1	R/W	R/W	UART1	00000-00 <sub>B</sub>
000021 <sub>H</sub>	SCR1	Serial control register 1	R/W	R/W		00000100 <sub>B</sub>
000022 <sub>H</sub>	SIDR1/ SODR1	Input data register 1 / Output data register 1	R/W	R/W		XXXXXXXX <sub>B</sub>
000023 <sub>H</sub>	SSR1	Serial status register 1	R/W	R/W		00001000 <sub>B</sub>
000024 <sub>H</sub>	M2CR1	Mode 2 control register 1	R/W	R/W		----1000 <sub>B</sub>
000025 <sub>H</sub>	CDCR1	Clock division control register 1	R/W	R/W	Communication prescaler 1	0---0000 <sub>B</sub>
000026 <sub>H</sub>	ENIR	Interrupt / DTP enable register	R/W	R/W	DTP/external interrupt	--000000 <sub>B</sub>
000027 <sub>H</sub>	EIRR	Interrupt / DTP cause register	R/W	R/W		--XXXXXXXX <sub>B</sub>
000028 <sub>H</sub>	ELVR	Request level setting register	R/W	R/W		00000000 <sub>B</sub>
000029 <sub>H</sub>			R/W	R/W		----0000 <sub>B</sub>
00002A <sub>H</sub>	ADER1	Analog input enable register 1	R/W	R/W	Port C, A/D	11111111 <sub>B</sub>
00002B <sub>H</sub>	ADER2	Analog input enable register 2	R/W	R/W	Port D, A/D	----1111 <sub>B</sub>
00002C <sub>H</sub>	BRSR	Bridge circuit selection register	R/W	R/W	Bridge circuit	--000000 <sub>B</sub>
00002D <sub>H</sub>	ADC0	A/D control register	R/W	R/W	8/10-bit A/D converter	00000000 <sub>B</sub>
00002E <sub>H</sub>	ADCR0	A/D data register	R	R		XXXXXXXX <sub>B</sub>
00002F <sub>H</sub>	ADCR1		R/W	R/W		00000-XX <sub>B</sub>
000030 <sub>H</sub>	ADCS0	A/D control status register	R/W	R/W		00----- <sub>B</sub>
000031 <sub>H</sub>	ADCS1		R/W	R/W		00000000 <sub>B</sub>
000032 <sub>H</sub>	SICRL	Serial interrupt request register	R/W	R/W		Serial IRQ
000033 <sub>H</sub>	SICRH	Serial interrupt control register	R/W	R/W	00000000 <sub>B</sub>	
000034 <sub>H</sub>	SIFR1	Serial interrupt frame number register 1	R/W	R/W	--000000 <sub>B</sub>	
000035 <sub>H</sub>	SIFR2	Serial interrupt frame number register 2	R/W	R/W	--000000 <sub>B</sub>	
000036 <sub>H</sub>	SIFR3	Serial interrupt frame number register 3	R/W	R/W	--000000 <sub>B</sub>	
000037 <sub>H</sub>	SIFR4	Serial interrupt frame number register 4	R/W	R/W	--000000 <sub>B</sub>	

(Continued)

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
000038 <sub>H</sub>	PDCRL1	PPG1 down counter register	—	R	16-bit PPG timer (CH1)	11111111 <sub>B</sub>
000039 <sub>H</sub>	PDCRH1		—	R		11111111 <sub>B</sub>
00003A <sub>H</sub>	PCSRL1	PPG1 period setting register	—	W		XXXXXXXX <sub>B</sub>
00003B <sub>H</sub>	PCSRH1		—	W		XXXXXXXX <sub>B</sub>
00003C <sub>H</sub>	PDUTL1	PPG1 duty setting register	—	W		XXXXXXXX <sub>B</sub>
00003D <sub>H</sub>	PDUTH1		—	W		XXXXXXXX <sub>B</sub>
00003E <sub>H</sub>	PCNTL1	PPG1 control status register	R/W	R/W		--000000 <sub>B</sub>
00003F <sub>H</sub>	PCNTH1		R/W	R/W		00000000 <sub>B</sub>
000040 <sub>H</sub>	PDCRL2	PPG2 down counter register	—	R	16-bit PPG timer (CH2)	11111111 <sub>B</sub>
000041 <sub>H</sub>	PDCRH2		—	R		11111111 <sub>B</sub>
000042 <sub>H</sub>	PCSRL2	PPG2 period setting register	—	W		XXXXXXXX <sub>B</sub>
000043 <sub>H</sub>	PCSRH2		—	W		XXXXXXXX <sub>B</sub>
000044 <sub>H</sub>	PDUTL2	PPG2 duty setting register	—	W		XXXXXXXX <sub>B</sub>
000045 <sub>H</sub>	PDUTH2		—	W		XXXXXXXX <sub>B</sub>
000046 <sub>H</sub>	PCNTL2	PPG2 control status register	R/W	R/W		--000000 <sub>B</sub>
000047 <sub>H</sub>	PCNTH2		R/W	R/W		00000000 <sub>B</sub>
000048 <sub>H</sub>	PDCRL3	PPG3 down counter register	—	R	16-bit PPG timer (CH3)	11111111 <sub>B</sub>
000049 <sub>H</sub>	PDCRH3		—	R		11111111 <sub>B</sub>
00004A <sub>H</sub>	PCSRL3	PPG3 period setting register	—	W		XXXXXXXX <sub>B</sub>
00004B <sub>H</sub>	PCSRH3		—	W		XXXXXXXX <sub>B</sub>
00004C <sub>H</sub>	PDUTL3	PPG3 duty setting register	—	W		XXXXXXXX <sub>B</sub>
00004D <sub>H</sub>	PDUTH3		—	W		XXXXXXXX <sub>B</sub>
00004E <sub>H</sub>	PCNTL3	PPG3 control status register	R/W	R/W		--000000 <sub>B</sub>
00004F <sub>H</sub>	PCNTH3		R/W	R/W		00000000 <sub>B</sub>
000050 <sub>H</sub>	PSCR0	PS/2 interface control register 0	R/W	R/W	3-channel PS/2 interface	0--00000 <sub>B</sub>
000051 <sub>H</sub>	PSSR0	PS/2 interface status register 0	R/W	R/W		00000000 <sub>B</sub>
000052 <sub>H</sub>	PSCR1	PS/2 interface control register 1	R/W	R/W		0--00000 <sub>B</sub>
000053 <sub>H</sub>	PSSR1	PS/2 interface status register 1	R/W	R/W		00000000 <sub>B</sub>
000054 <sub>H</sub>	PSCR2	PS/2 interface control register 2	R/W	R/W		0--00000 <sub>B</sub>
000055 <sub>H</sub>	PSSR2	PS/2 interface status register 2	R/W	R/W		00000000 <sub>B</sub>
000056 <sub>H</sub>	PSDR0	PS/2 interface data register 0	R/W	R/W		00000000 <sub>B</sub>
000057 <sub>H</sub>	PSDR1	PS/2 interface data register 1	R/W	R/W		00000000 <sub>B</sub>
000058 <sub>H</sub>	PSDR2	PS/2 interface data register 2	R/W	R/W		00000000 <sub>B</sub>
000059 <sub>H</sub>	PSMR	PS/2 interface mode register	R/W	R/W		----0000 <sub>B</sub>

(Continued)

# MB90370 Series

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
00005A <sub>H</sub>	DAT0	D/A converter data register 0	R/W	R/W	D/A converter	XXXXXXXX <sub>B</sub>
00005B <sub>H</sub>	DAT1	D/A converter data register 1	R/W	R/W		XXXXXXXX <sub>B</sub>
00005C <sub>H</sub>	DACR0	D/A control register 0	R/W	R/W		-----0 <sub>B</sub>
00005D <sub>H</sub>	DACR1	D/A control register 1	R/W	R/W		-----0 <sub>B</sub>
00005E <sub>H</sub>	UPAL1	UPI1 address register (lower)	R/W	R/W	LPC interface	XXXXXXXX <sub>B</sub>
00005F <sub>H</sub>	UPAH1	UPI1 address register (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
000060 <sub>H</sub>	UPAL2	UPI2 address register (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>
000061 <sub>H</sub>	UPAH2	UPI2 address register (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
000062 <sub>H</sub>	UPAL3	UPI3 address register (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>
000063 <sub>H</sub>	UPAH3	UPI3 address register (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
000064 <sub>H</sub>	UPCL	UPI control register (lower)	R/W	R/W		00000000 <sub>B</sub>
000065 <sub>H</sub>	UPCH	UPI control register (upper)	R/W	R/W		-000-000 <sub>B</sub>
000066 <sub>H</sub>	UPDI0/ UPDO0	UPI0 data input register / data output register	R/W	R/W		XXXXXXXX <sub>B</sub>
000067 <sub>H</sub>	UPS0	UPI0 status register	R/W	R/W		00000000 <sub>B</sub>
000068 <sub>H</sub>	UPDI1/ UPDO1	UPI1 data input register / data output register	R/W	R/W		XXXXXXXX <sub>B</sub>
000069 <sub>H</sub>	UPS1	UPI1 status register	R/W	R/W		00000000 <sub>B</sub>
00006A <sub>H</sub>	UPDI2/ UPDO2	UPI2 data input register / data output register	R/W	R/W		XXXXXXXX <sub>B</sub>
00006B <sub>H</sub>	UPS2	UPI2 status register	R/W	R/W		00000000 <sub>B</sub>
00006C <sub>H</sub>	UPDI3/ UPDO3	UPI3 data input register / data output register	R/W	R/W		XXXXXXXX <sub>B</sub>
00006D <sub>H</sub>	UPS3	UPI3 status register	R/W	R/W		00000000 <sub>B</sub>
00006E <sub>H</sub>	LCR	LPC control register	R/W	R/W		----000 <sub>B</sub>
00006F <sub>H</sub>	ROMM	ROM mirroring function selection register	W	W	ROM mirroring function	-----01 <sub>B</sub>
000070 <sub>H</sub>	TMCSRL1	Timer control status register CH1 (lower)	R/W	R/W	16-bit reload timer (CH1)	00000000 <sub>B</sub>
000071 <sub>H</sub>	TMCSRH1	Timer control status register CH1 (upper)	R/W	R/W		----0000 <sub>B</sub>
000072 <sub>H</sub>	TMR1/ TMRD1	16-bit timer/reload register CH1	—	R/W		XXXXXXXX <sub>B</sub>
000073 <sub>H</sub>			—	R/W		XXXXXXXX <sub>B</sub>

(Continued)

# MB90370 Series

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value	
000074 <sub>H</sub>	TMCSRL2	Timer control status register CH2 (lower)	R/W	R/W	16-bit reload timer (CH2)	00000000 <sub>B</sub>	
000075 <sub>H</sub>	TMCSRH2	Timer control status register CH2 (upper)	R/W	R/W		----0000 <sub>B</sub>	
000076 <sub>H</sub>	TMR2/ TMRD2	16-bit timer/reload register CH2	—	R/W		XXXXXXXX <sub>B</sub>	
000077 <sub>H</sub>			—	R/W		XXXXXXXX <sub>B</sub>	
000078 <sub>H</sub>	TMCSRL3	Timer control status register CH3 (lower)	R/W	R/W	16-bit reload timer (CH3)	00000000 <sub>B</sub>	
000079 <sub>H</sub>	TMCSRH3	Timer control status register CH3 (upper)	R/W	R/W		----0000 <sub>B</sub>	
00007A <sub>H</sub>	TMR3/ TMRD3	16-bit timer/reload register CH3	—	R/W		XXXXXXXX <sub>B</sub>	
00007B <sub>H</sub>			—	R/W		XXXXXXXX <sub>B</sub>	
00007C <sub>H</sub>	TMCSRL4	Timer control status register CH4 (lower)	R/W	R/W	16-bit reload timer (CH4)	00000000 <sub>B</sub>	
00007D <sub>H</sub>	TMCSRH4	Timer control status register CH4 (upper)	R/W	R/W		----0000 <sub>B</sub>	
00007E <sub>H</sub>	TMR4/ TMRD4	16-bit timer/reload register CH4	—	R/W		XXXXXXXX <sub>B</sub>	
00007F <sub>H</sub>			—	R/W		XXXXXXXX <sub>B</sub>	
000080 <sub>H</sub>	IBCRL	I <sup>2</sup> C bus control register (lower)	R/W	R/W	I <sup>2</sup> C	----0000 <sub>B</sub>	
000081 <sub>H</sub>	IBCRH	I <sup>2</sup> C bus control register (upper)	R/W	R/W		00000000 <sub>B</sub>	
000082 <sub>H</sub>	IBSRL	I <sup>2</sup> C bus status register (lower)	R	R		00000000 <sub>B</sub>	
000083 <sub>H</sub>	IBSRH	I <sup>2</sup> C bus status register (upper)	R/W	R/W		--000000 <sub>B</sub>	
000084 <sub>H</sub>	IDAR	I <sup>2</sup> C data register	R/W	R/W		XXXXXXXX <sub>B</sub>	
000085 <sub>H</sub>	IADR	I <sup>2</sup> C address register	R/W	R/W		-XXXXXXXX <sub>B</sub>	
000086 <sub>H</sub>	ICCR	I <sup>2</sup> C clock control register	R/W	R/W		0-000000 <sub>B</sub>	
000087 <sub>H</sub>	ITCR	I <sup>2</sup> C timeout control register	R/W	R/W		-0-000000 <sub>B</sub>	
000088 <sub>H</sub>	ITOC	I <sup>2</sup> C timeout clock register	R/W	R/W		00000000 <sub>B</sub>	
000089 <sub>H</sub>	ITOD	I <sup>2</sup> C timeout data register	R/W	R/W		00000000 <sub>B</sub>	
00008A <sub>H</sub>	ISTO	I <sup>2</sup> C slave timeout register	R/W	R/W		00000000 <sub>B</sub>	
00008B <sub>H</sub>	IMTO	I <sup>2</sup> C master timeout register	R/W	R/W		00000000 <sub>B</sub>	
00008C <sub>H</sub>	RDR0	Port 0 pull-up resistor setting register	R/W	R/W		Port 0	00000000 <sub>B</sub>
00008D <sub>H</sub>	RDR1	Port 1 pull-up resistor setting register	R/W	R/W		Port 1	00000000 <sub>B</sub>
00008E <sub>H</sub>	RDR2	Port 2 pull-up resistor setting register	R/W	R/W	Port 2	00000000 <sub>B</sub>	
00008F <sub>H</sub>	RDR3	Port 3 pull-up resistor setting register	R/W	R/W	Port 3	00000000 <sub>B</sub>	

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(Continued)

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
000090 <sub>H</sub> to 9D <sub>H</sub>	Prohibited area					
00009E <sub>H</sub>	PACSR	Program address detect control status register	R/W	R/W	ROM correction	----0000 <sub>B</sub>
00009F <sub>H</sub>	DIRR	Delayed interrupt cause / clear register	R/W	R/W	Delayed interrupt	-----0 <sub>B</sub>
0000A0 <sub>H</sub>	LPMCR	Low-power consumption mode register	R/W	R/W	Low-power consumption control register	00011000 <sub>B</sub>
0000A1 <sub>H</sub>	CKSCR	Clock selection register	R/W	R/W		11111100 <sub>B</sub>
0000A2 <sub>H</sub> to A7 <sub>H</sub>	Prohibited area					
0000A8 <sub>H</sub>	WDTC	Watchdog control register	R/W	R/W	Watchdog timer	X-XXX111 <sub>B</sub>
0000A9 <sub>H</sub>	TBTC	Timebase timer control register	R/W	R/W	Timebase timer	1--00100 <sub>B</sub>
0000AA <sub>H</sub>	WTC	Watch timer control register	R/W	R/W	Watch timer	10001000 <sub>B</sub>
0000AB <sub>H</sub>	Prohibited area					
0000AC <sub>H</sub>	EICR	Wake-up interrupt control register	R/W	R/W	Wake-up interrupt	00000000 <sub>B</sub>
0000AD <sub>H</sub>	EIFR	Wake-up interrupt flag register	R/W	R/W		-----0 <sub>B</sub>
0000AE <sub>H</sub>	FMCS	Flash memory control status register	R/W	R/W	Flash memory interface circuit	00010000 <sub>B</sub>
0000AF <sub>H</sub>	Prohibited area					
0000B0 <sub>H</sub>	ICR00	Interrupt control register 00	R/W	R/W	Interrupt controller	00000111 <sub>B</sub>
0000B1 <sub>H</sub>	ICR01	Interrupt control register 01	R/W	R/W		00000111 <sub>B</sub>
0000B2 <sub>H</sub>	ICR02	Interrupt control register 02	R/W	R/W		00000111 <sub>B</sub>
0000B3 <sub>H</sub>	ICR03	Interrupt control register 03	R/W	R/W		00000111 <sub>B</sub>
0000B4 <sub>H</sub>	ICR04	Interrupt control register 04	R/W	R/W		00000111 <sub>B</sub>
0000B5 <sub>H</sub>	ICR05	Interrupt control register 05	R/W	R/W		00000111 <sub>B</sub>
0000B6 <sub>H</sub>	ICR06	Interrupt control register 06	R/W	R/W		00000111 <sub>B</sub>
0000B7 <sub>H</sub>	ICR07	Interrupt control register 07	R/W	R/W		00000111 <sub>B</sub>
0000B8 <sub>H</sub>	ICR08	Interrupt control register 08	R/W	R/W		00000111 <sub>B</sub>
0000B9 <sub>H</sub>	ICR09	Interrupt control register 09	R/W	R/W		00000111 <sub>B</sub>
0000BA <sub>H</sub>	ICR10	Interrupt control register 10	R/W	R/W		00000111 <sub>B</sub>

(Continued)

# MB90370 Series

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value	
0000BB <sub>H</sub>	ICR11	Interrupt control register 11	R/W	R/W	Interrupt controller	00000111 <sub>B</sub>	
0000BC <sub>H</sub>	ICR12	Interrupt control register 12	R/W	R/W		00000111 <sub>B</sub>	
0000BD <sub>H</sub>	ICR13	Interrupt control register 13	R/W	R/W		00000111 <sub>B</sub>	
0000BE <sub>H</sub>	ICR14	Interrupt control register 14	R/W	R/W		00000111 <sub>B</sub>	
0000BF <sub>H</sub>	ICR15	Interrupt control register 15	R/W	R/W		00000111 <sub>B</sub>	
0000C0 <sub>H</sub>	MBCRL	MI <sup>2</sup> C bus control register (lower)	R/W	R/W	MI <sup>2</sup> C	----0000 <sub>B</sub>	
0000C1 <sub>H</sub>	MBCRH	MI <sup>2</sup> C bus control register (upper)	R/W	R/W		00000000 <sub>B</sub>	
0000C2 <sub>H</sub>	MBSRL	MI <sup>2</sup> C bus status register (lower)	R	R		00000000 <sub>B</sub>	
0000C3 <sub>H</sub>	MBSRH	MI <sup>2</sup> C bus status register (upper)	R/W	R/W		--000000 <sub>B</sub>	
0000C4 <sub>H</sub>	MDAR	MI <sup>2</sup> C data register	R/W	R/W		XXXXXXXX <sub>B</sub>	
0000C5 <sub>H</sub>	MALR	MI <sup>2</sup> C alert register	R/W	R/W		----0000 <sub>B</sub>	
0000C6 <sub>H</sub>	MADR1	MI <sup>2</sup> C address register 1	R/W	R/W		-XXXXXXXX <sub>B</sub>	
0000C7 <sub>H</sub>	MADR2	MI <sup>2</sup> C address register 2	R/W	R/W		-XXXXXXXX <sub>B</sub>	
0000C8 <sub>H</sub>	MADR3	MI <sup>2</sup> C address register 3	R/W	R/W		-XXXXXXXX <sub>B</sub>	
0000C9 <sub>H</sub>	MADR4	MI <sup>2</sup> C address register 4	R/W	R/W		-XXXXXXXX <sub>B</sub>	
0000CA <sub>H</sub>	MADR5	MI <sup>2</sup> C address register 5	R/W	R/W		-XXXXXXXX <sub>B</sub>	
0000CB <sub>H</sub>	MADR6	MI <sup>2</sup> C address register 6	R/W	R/W		-XXXXXXXX <sub>B</sub>	
0000CC <sub>H</sub>	MCCR	MI <sup>2</sup> C clock control register	R/W	R/W		0-000000 <sub>B</sub>	
0000CD <sub>H</sub>	MTCR	MI <sup>2</sup> C timeout control register	R/W	R/W		-0-00000 <sub>B</sub>	
0000CE <sub>H</sub>	MTOC	MI <sup>2</sup> C timeout clock register	R/W	R/W		00000000 <sub>B</sub>	
0000CF <sub>H</sub>	MTOD	MI <sup>2</sup> C timeout data register	R/W	R/W		00000000 <sub>B</sub>	
0000D0 <sub>H</sub>	MSTO	MI <sup>2</sup> C slave timeout register	R/W	R/W		00000000 <sub>B</sub>	
0000D1 <sub>H</sub>	MMTO	MI <sup>2</sup> C master timeout register	R/W	R/W		00000000 <sub>B</sub>	
0000D2 <sub>H</sub>	SMR2	Serial mode register 2	R/W	R/W		UART2	0000-00 <sub>B</sub>
0000D3 <sub>H</sub>	SCR2	Serial control register 2	R/W	R/W			00000100 <sub>B</sub>
0000D4 <sub>H</sub>	SIDR2/ SODR2	Input data register 2 / output data register 2	R/W	R/W	XXXXXXXX <sub>B</sub>		
0000D5 <sub>H</sub>	SSR2	Status register 2	R/W	R/W	00001000 <sub>B</sub>		
0000D6 <sub>H</sub>	M2CR2	Mode 2 control register 2	R/W	R/W	----1000 <sub>B</sub>		
0000D7 <sub>H</sub>	CDCR2	Clock division control register 2	R/W	R/W	Communication prescaler 2	0---0000 <sub>B</sub>	

(Continued)

# MB90370 Series

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
0000D8 <sub>H</sub>	COCRL	Comparator control register (lower)	R/W	R/W	Voltage comparator	--000000 <sub>B</sub>
0000D9 <sub>H</sub>	COCRH	Comparator control register (upper)	R/W	R/W		00011111 <sub>B</sub>
0000DA <sub>H</sub>	COSRL1	Comparator status register 1 (lower)	R/W	R/W		00000000 <sub>B</sub>
0000DB <sub>H</sub>	COSRH1	Comparator status register 1 (upper)	R/W	R/W		--000000 <sub>B</sub>
0000DC <sub>H</sub>	CICRL	Comparator interrupt control register (lower)	R/W	R/W		00000000 <sub>B</sub>
0000DD <sub>H</sub>	CICRH	Comparator interrupt control register (upper)	R/W	R/W		--000000 <sub>B</sub>
0000DE <sub>H</sub>	COSRL2	Comparator status register 2 (lower)	R	R		XXXXXXXX <sub>B</sub>
0000DF <sub>H</sub>	COSRH2	Comparator status register 2 (upper)	R	R		--XXXXXXXX <sub>B</sub>
0000E0 <sub>H</sub>	CIER	Comparator input enable register	R/W	R/W		---11111 <sub>B</sub>
0000E1 <sub>H</sub>	BDR	Bit data register	R/W	R/W		Bit decoder
0000E2 <sub>H</sub>	BRRL	Bit result register (lower)	R	R	XXXXXXXX <sub>B</sub>	
0000E3 <sub>H</sub>	BRRH	Bit result register (upper)	R	R	XXXXXXXX <sub>B</sub>	
0000E4 <sub>H</sub>	SMR3	Serial mode register 3	R/W	R/W	UART3	00000-00 <sub>B</sub>
0000E5 <sub>H</sub>	SCR3	Serial control register 3	R/W	R/W		00000100 <sub>B</sub>
0000E6 <sub>H</sub>	SIDR3/ SODR3	Input data register 3 / output data register 3	R/W	R/W		XXXXXXXX <sub>B</sub>
0000E7 <sub>H</sub>	SSR3	Status register 3	R/W	R/W		00001000 <sub>B</sub>
0000E8 <sub>H</sub>	M2CR3	Mode 2 control register 3	R/W	R/W		----1000 <sub>B</sub>
0000E9 <sub>H</sub>	CDCR3	Clock division control register 3	R/W	R/W	Communication prescaler 3	0---0000 <sub>B</sub>
0000EA <sub>H</sub>	PDL3	Port 3 data latch register	R/W	R/W	Port 3 data latch	00000000 <sub>B</sub>
0000EB <sub>H</sub> to ED <sub>H</sub>	Prohibited area					
0000EE <sub>H</sub>	LCRL	LCD control register 0	R/W	R/W	LCD controller / driver	00010000 <sub>B</sub>
0000EF <sub>H</sub>	LCRH	LCD control register 1	R/W	R/W		00000000 <sub>B</sub>
0000F0 <sub>H</sub> to F4 <sub>H</sub>	VRAM	LCD display RAM	R/W	—		XXXXXXXX <sub>B</sub>
0000F5 <sub>H</sub> to F7 <sub>H</sub>	Prohibited area					
0000F8 <sub>H</sub> to FF <sub>H</sub>	External area					

(Continued)

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
001FF0H	PADR0	Program address detection register 0	R/W	R/W	ROM correction	XXXXXXXX <sub>B</sub>
001FF1H		Program address detection register 1	R/W	R/W		XXXXXXXX <sub>B</sub>
001FF2H		Program address detection register 2	R/W	R/W		XXXXXXXX <sub>B</sub>
001FF3H	PADR1	Program address detection register 3	R/W	R/W		XXXXXXXX <sub>B</sub>
001FF4H		Program address detection register 4	R/W	R/W		XXXXXXXX <sub>B</sub>
001FF5H		Program address detection register 5	R/W	R/W		XXXXXXXX <sub>B</sub>
003FC0H	UDRL0	UP data register 0 (lower)	R/W	R/W	LPC data buffer array	XXXXXXXX <sub>B</sub>
003FC1H	UDRH0	UP data register 0 (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FC2H	UDRL1	UP data register 1 (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FC3H	UDRH1	UP data register 1 (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FC4H	UDRL2	UP data register 2 (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FC5H	UDRH2	UP data register 2 (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FC6H	UDRL3	UP data register 3 (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FC7H	UDRH3	UP data register 3 (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FC8H	UDRL4	UP data register 4 (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FC9H	UDRH4	UP data register 4 (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FCAH	UDRL5	UP data register 5 (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FCBH	UDRH5	UP data register 5 (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FCC <sub>H</sub>	UDRL6	UP data register 6 (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FCD <sub>H</sub>	UDRH6	UP data register 6 (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FCE <sub>H</sub>	UDRL7	UP data register 7 (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FCF <sub>H</sub>	UDRH7	UP data register 7 (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FD0 <sub>H</sub>	UDRL8	UP data register 8 (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FD1 <sub>H</sub>	UDRH8	UP data register 8 (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>
003FD2 <sub>H</sub>	UDRL9	UP data register 9 (lower)	R/W	R/W	XXXXXXXX <sub>B</sub>	
003FD3 <sub>H</sub>	UDRH9	UP data register 9 (upper)	R/W	R/W	XXXXXXXX <sub>B</sub>	

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(Continued)

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value	
003FD4 <sub>H</sub>	UDRLA	UP data register A (lower)	R/W	R/W	LPC data buffer array	XXXXXXXX <sub>B</sub>	
003FD5 <sub>H</sub>	UDRHA	UP data register A (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>	
003FD6 <sub>H</sub>	UDRLB	UP data register B (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>	
003FD7 <sub>H</sub>	UDRHB	UP data register B (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>	
003FD8 <sub>H</sub>	UDRLC	UP data register C (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>	
003FD9 <sub>H</sub>	UDRHC	UP data register C (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>	
003FDA <sub>H</sub>	UDRLD	UP data register D (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>	
003FDB <sub>H</sub>	UDRHD	UP data register D (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>	
003FDC <sub>H</sub>	UDRLE	UP data register E (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>	
003FDD <sub>H</sub>	UDRHE	UP data register E (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>	
003FDE <sub>H</sub>	UDRLF	UP data register F (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>	
003FDF <sub>H</sub>	UDRHF	UP data register F (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>	
003FE0 <sub>H</sub>	DNDL0	DOWN data register 0 (lower)	R	R		XXXXXXXX <sub>B</sub>	
003FE1 <sub>H</sub>	DNDH0	DOWN data register 0 (upper)	R	R		XXXXXXXX <sub>B</sub>	
003FE2 <sub>H</sub>	DNDL1	DOWN data register 1 (lower)	R	R		XXXXXXXX <sub>B</sub>	
003FE3 <sub>H</sub>	DNDH1	DOWN data register 1 (upper)	R	R		XXXXXXXX <sub>B</sub>	
003FE4 <sub>H</sub>	DNDL2	DOWN data register 2 (lower)	R	R		XXXXXXXX <sub>B</sub>	
003FE5 <sub>H</sub>	DNDH2	DOWN data register 2 (upper)	R	R		XXXXXXXX <sub>B</sub>	
003FE6 <sub>H</sub>	DNDL3	DOWN data register 3 (lower)	R	R		XXXXXXXX <sub>B</sub>	
003FE7 <sub>H</sub>	DNDH3	DOWN data register 3 (upper)	R	R		XXXXXXXX <sub>B</sub>	
003FE8 <sub>H</sub>	DNDL4	DOWN data register 4 (lower)	R	R		XXXXXXXX <sub>B</sub>	
003FE9 <sub>H</sub>	DNDH4	DOWN data register 4 (upper)	R	R		XXXXXXXX <sub>B</sub>	
003FEA <sub>H</sub>	DNDL5	DOWN data register 5 (lower)	R	R		XXXXXXXX <sub>B</sub>	
003FEB <sub>H</sub>	DNDH5	DOWN data register 5 (upper)	R	R		XXXXXXXX <sub>B</sub>	
003FEC <sub>H</sub>	DNDL6	DOWN data register 6 (lower)	R	R		XXXXXXXX <sub>B</sub>	
003FED <sub>H</sub>	DNDH6	DOWN data register 6 (upper)	R	R		XXXXXXXX <sub>B</sub>	
003FEE <sub>H</sub>	DNDL7	DOWN data register 7 (lower)	R	R		XXXXXXXX <sub>B</sub>	
003FEF <sub>H</sub>	DNDH7	DOWN data register 7 (upper)	R	R		XXXXXXXX <sub>B</sub>	
003FF0 <sub>H</sub>	DBAAL	Data buffer array address register (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>	
003FF1 <sub>H</sub>	DBAAH	Data buffer array address register (upper)	R/W	R/W		XXXXXXXX <sub>B</sub>	
003FF2 <sub>H</sub> to 003FFF <sub>H</sub>	Prohibited area						

- **Meaning of abbreviations used for reading and writing**

R/W : Read and write enabled

R : Read-only

W : Write-only

- **Explanation of initial values**

0 : The bit is initialized to 0.

1 : The bit is initialized to 1.

X : The initial value of the bit is undefined.

- : The bit is not used. Its initial value is undefined.

- **Instruction using IO addressing e.g. MOV A, io, is not supported for registers area 003FC0<sub>H</sub> to 003FFF<sub>H</sub>.**

# MB90370 Series

## ■ INTERRUPT FACTORS, INTERRUPT VECTORS, INTERRUPT CONTROL REGISTER

Interrupt cause	EPOS support	Interrupt vector		Interrupt control register		Priority*2	
		Number	Address	ICR	Address		
Reset	X	#08	08H	FFFFDC <sub>H</sub>	—	<div style="display: flex; align-items: center; justify-content: center;"> <span style="margin-right: 5px;">High</span> </div> <div style="display: flex; align-items: center; justify-content: center; margin-top: 200px;"> <span style="margin-left: 5px;">Low</span> </div>	
INT9 instruction	X	#09	09H	FFFFD8 <sub>H</sub>	—		
Exception processing	X	#10	0AH	FFFFD4 <sub>H</sub>	—		
A/D converter conversion termination	○	#11	0BH	FFFFD0 <sub>H</sub>	ICR00		0000B0 <sub>H</sub> *1
Timebase timer	△	#12	0CH	FFFFCC <sub>H</sub>			
UPI0 IBF / LPC reset	△	#13	0DH	FFFFC8 <sub>H</sub>	ICR01		0000B1 <sub>H</sub> *1
UPI1 IBF	△	#14	0EH	FFFFC4 <sub>H</sub>			
UPI2 IBF	△	#15	0FH	FFFFC0 <sub>H</sub>	ICR02		0000B2 <sub>H</sub> *1
UPI3 IBF	△	#16	10H	FFFFBC <sub>H</sub>			
DTP/ext. interrupt channels 0/1 detection	○	#17	11H	FFFFB8 <sub>H</sub>	ICR03		0000B3 <sub>H</sub> *1
DTP/ext. interrupt channels 2/3 detection	○	#18	12H	FFFFB4 <sub>H</sub>			
DTP/ext. interrupt channels 4/5 detection	○	#19	13H	FFFFB0 <sub>H</sub>	ICR04		0000B4 <sub>H</sub> *1
Wake-up interrupt detection	△	#20	14H	FFFFAC <sub>H</sub>			
UPI0/1/2/3 OBE	△	#21	15H	FFFA8 <sub>H</sub>	ICR05		0000B5 <sub>H</sub> *2
16-bit PPG timer 1	○	#22	16H	FFFA4 <sub>H</sub>			
PS/2 interface 0/1	△	#23	17H	FFFA0 <sub>H</sub>	ICR06		0000B6 <sub>H</sub> *1
PS/2 interface 2	△	#24	18H	FFFF9C <sub>H</sub>			
Watch timer	△	#25	19H	FFFF98 <sub>H</sub>	ICR07		0000B7 <sub>H</sub> *1
I <sup>2</sup> C transfer complete / bus error	△	#26	1AH	FFFF94 <sub>H</sub>			
16-bit PPG timer 2/3	○	#27	1BH	FFFF90 <sub>H</sub>	ICR08		0000B8 <sub>H</sub> *1
Voltage comparator 1	△	#28	1CH	FFFF8C <sub>H</sub>			
MI <sup>2</sup> C transfer complete / bus error	△	#29	1DH	FFFF88 <sub>H</sub>	ICR09		0000B9 <sub>H</sub> *1
Voltage comparator 2	△	#30	1EH	FFFF84 <sub>H</sub>			
I <sup>2</sup> C timeout / standby wake-up	△	#31	1FH	FFFF80 <sub>H</sub>	ICR10		0000BA <sub>H</sub> *1
16-bit reload timer 1/2 underflow	○	#32	20H	FFFF7C <sub>H</sub>			
MI <sup>2</sup> C timeout / standby wake-up	△	#33	21H	FFFF78 <sub>H</sub>	ICR11		0000BB <sub>H</sub> *1
16-bit reload timer 3/4 underflow	○	#34	22H	FFFF74 <sub>H</sub>			
UART1 receive	◎	#35	23H	FFFF70 <sub>H</sub>	ICR12		0000BC <sub>H</sub> *1
UART1 send	△	#36	24H	FFFF6C <sub>H</sub>			
UART2 receive	◎	#37	25H	FFFF68 <sub>H</sub>	ICR13		0000BD <sub>H</sub> *1
UART2 send	△	#38	26H	FFFF64 <sub>H</sub>			
UART3 receive	◎	#39	27H	FFFF60 <sub>H</sub>	ICR14		0000BE <sub>H</sub> *1
UART3 send	△	#40	28H	FFFF5C <sub>H</sub>			
Flash memory status	△	#41	29H	FFFF58 <sub>H</sub>	ICR15		0000BF <sub>H</sub> *1
Delayed interrupt generator module	△	#42	2AH	FFFF54 <sub>H</sub>			

- : Can be used and interrupt request flag is cleared by EI<sup>2</sup>OS interrupt clear signal.
- × : Cannot be used.
- ◎ : Can be used and support the EI<sup>2</sup>OS stop request.
- △ : Can be used.

- \*1 :
- For peripheral functions that share the ICR register, the interrupt level will be the same.
  - If the extended intelligent I/O service is to be used with a peripheral function that shares the ICR register with another peripheral function, the service can be started by either of the function. And if EI<sup>2</sup>OS clear is supported, both interrupt request flags for the two interrupt causes are cleared by EI<sup>2</sup>OS interrupt clear signal. It is recommended to mask either of the interrupt request during the use of EI<sup>2</sup>OS.
  - EI<sup>2</sup>OS service cannot be started multiple times simultaneously. Interrupt other than the operating interrupt is masked during EI<sup>2</sup>OS operation. It is recommended to mask either of the interrupt requests during the use of EI<sup>2</sup>OS.

- \*2 : This priority is applied when interrupts of the same level occur simultaneously.

## ■ PERIPHERAL RESOURCES

### 1. Low-power Consumption Control Circuit

The MB90370 series has the following CPU operating mode selected by the configuration of an operating clock and clock operation control.

#### • Clock Mode

- PLL clock mode  
In this mode, a PLL clock that is a multiple of the oscillation clock (HCLK) is used to operate the CPU and peripheral functions.
- Main clock mode  
In this mode, the main clock, with the oscillation clock (HCLK) frequency divided by 2 is used to operate the CPU and peripheral functions. In the main clock mode, the PLL multiplier circuit is inactive.
- Sub-clock mode  
In this mode, the sub-clock, with the sub-clock (SCLK) frequency divided by 4 is used to operate the CPU and peripheral functions. In the sub-clock mode, the main clock and PLL multiplier circuit are inactive.

#### • CPU Intermittent Operating Mode

In this mode, the CPU is operated intermittently while high-speed clock pulses are supplied to peripheral functions, thereby reducing power consumption. In this mode, intermittent clock pulses are supplied only to the CPU while it is accessing a register, internal memory, or peripheral function.

#### • Standby Mode

In this mode, the low-power consumption control circuit stops supplying the clock to the CPU (sleep mode) or the CPU and peripheral functions (timebase timer mode) or stops the oscillation clock itself (stop mode), thereby reducing power consumption.

- PLL sleep mode  
The PLL sleep mode is activated to stop the CPU operating clock in the PLL clock mode. Components excluding the CPU operate on the PLL clock.
- Main sleep mode  
The main sleep mode is activated to stop the CPU operating clock in the main clock mode. Components excluding the CPU operate on the main clock.
- Sub-sleep mode  
The sub-sleep mode is activated to stop the CPU operating clock in the sub-clock mode. Components excluding the CPU operate on the divided-by-four sub-clock.
- Timebase timer mode  
The timebase timer mode causes the operation of functions, excluding the oscillation clock, timebase timer, and watch timer, to stop. All functions other than the timebase timer and watch timer are inactivated.
- Watch mode and main watch mode  
The watch mode and main watch mode operates the watch timer only. The sub-clock operates but the main clock and PLL multiplier circuit stop.
- Stop mode  
The stop mode causes the oscillation to stop. All functions are inactivated.

Note : Because the stop mode turns the oscillation clock off, data can be retained by the lowest power consumption.

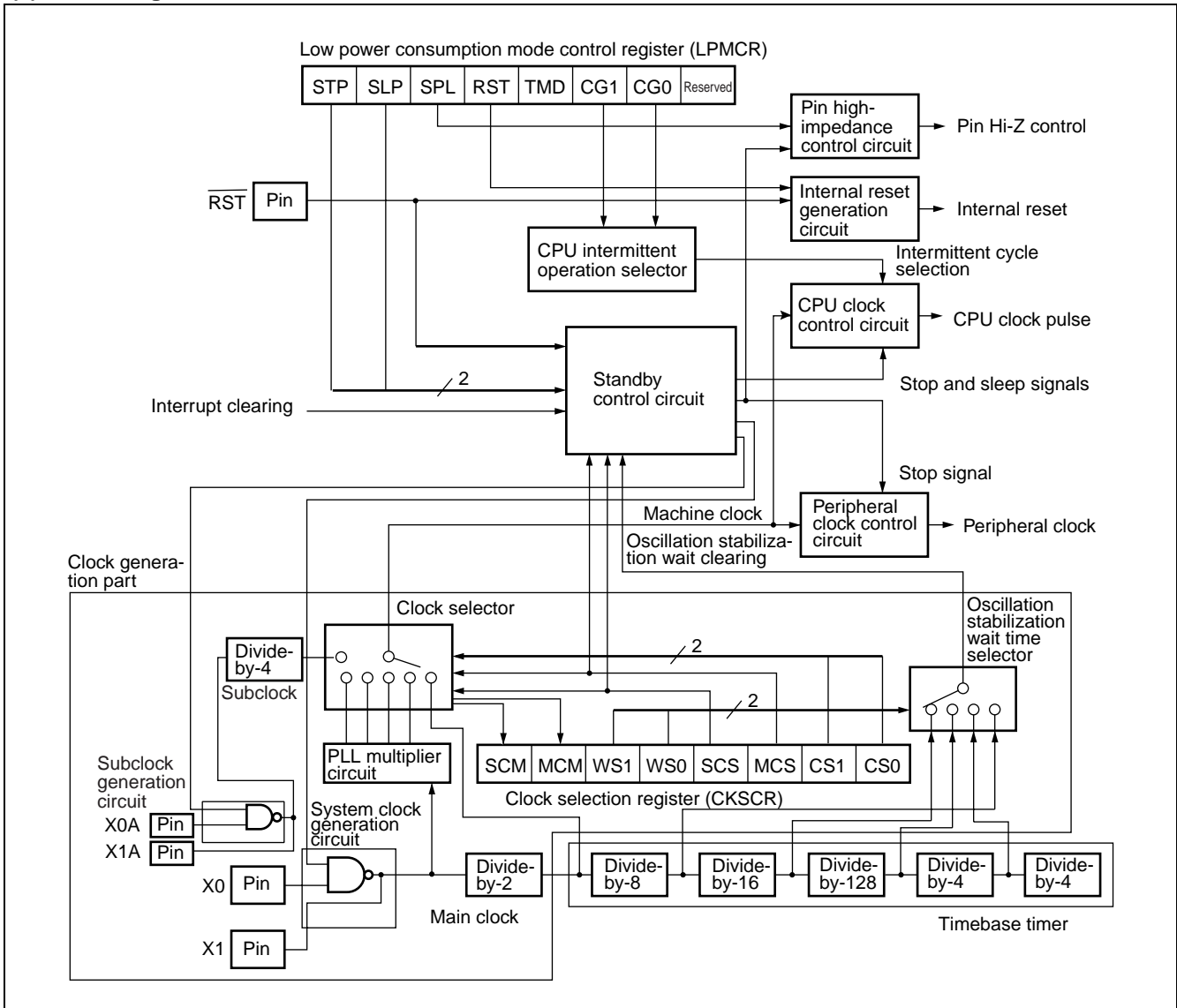
## (1) Register configuration

Clock Selection Register									
Address : 0000A1H	15	14	13	12	11	10	9	8	⇐ Bit number CKSCR
	SCM	MCM	WS1	WS0	SCS	MCS	CS1	CS0	
Read/write	⇒ R	⇒ R	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	
Initial value	⇒ 1	⇒ 1	⇒ 1	⇒ 1	⇒ 1	⇒ 1	⇒ 0	⇒ 0	

Lower Power Consumption Mode Control Register									
Address : 0000A0H	7	6	5	4	3	2	1	0	⇐ Bit number LPMCR
	STP	SLP	SPL	RST	TMD	CG1	CG0	Reserved	
Read/write	⇒ W	⇒ W	⇒ R/W	⇒ W	⇒ W	⇒ R/W	⇒ R/W	⇒ R/W	
Initial value	⇒ 0	⇒ 0	⇒ 0	⇒ 1	⇒ 1	⇒ 0	⇒ 0	⇒ 0	

## (2) Block diagram



# MB90370 Series

## 2. I/O Ports

### (1) Outline of I/O ports

Each I/O port outputs data from the CPU to the I/O pins or inputs signals from the I/O pins to the CPU as directed by the port data register (PDR). Each CMOS I/O port can also designate the direction of a data flow (input or output) at the I/O pins in bit units using the port data direction register (DDR). Or N-channel open-drain port can designate the direction of a data flow (input or output) at the I/O pins in bit units using the port data register (PDR). The function of each port and the resources using it are described below:

- Port 0 : General-purpose I/O port/resource (Key-on wake-up interrupt)
- Port 1 : General-purpose I/O port
- Port 2 : General-purpose I/O port
- Port 3 : General-purpose I/O port/resource (A/D converter external trigger)
- Port 4 : General-purpose I/O port/resource (PS/2 interface / serial IRQ controller)
- Port 5 : General-purpose I/O port/resource (LPC interface)
- Port 6 : General-purpose I/O port/resource (DTP / UART1)
- Port 7 : General-purpose I/O port/resource (UART1 / UART2 / UART3 / PPG1)
- Port 8 : General-purpose I/O port/resource (Multi-address I<sup>2</sup>C)
- Port 9 : General-purpose I/O port/resource (I<sup>2</sup>C / Multi-address I<sup>2</sup>C)
- Port A : General-purpose I/O port/resource (Comparator)
- Port B : General-purpose I/O port/resource (Comparator)
- Port C : General-purpose I/O port/resource (Comparator / A/D converter)
- Port D : General-purpose I/O port/resource (A/D converter / D/A converter / PPG2 / PPG3)
- Port E : General-purpose I/O port/resource (Reload timer1 to 4 / LCD controller)
- Port F : General-purpose I/O port/resource (LCD controller)

### (2) Register configuration

Register	Read/Write	Address	Initial value
Port 0 data register (PDR0)	R/W	000000H	XXXXXXXX <sub>B</sub>
Port 1 data register (PDR1)	R/W	000001H	XXXXXXXX <sub>B</sub>
Port 2 data register (PDR2)	R/W	000002H	XXXXXXXX <sub>B</sub>
Port 3 data register (PDR3)	R/W	000003H	XXXXXXXX <sub>B</sub>
Port 4 data register (PDR4)	R/W	000004H	X1111111 <sub>B</sub>
Port 5 data register (PDR5)	R/W	000005H	XXXXXXXX <sub>B</sub>
Port 6 data register (PDR6)	R/W	000006H	XXXXXXXX <sub>B</sub>
Port 7 data register (PDR7)	R/W	000007H	XXXXXXXX <sub>B</sub>
Port 8 data register (PDR8)	R/W	000008H	----111 <sub>B</sub>
Port 9 data register (PDR9)	R/W	000009H	--111111 <sub>B</sub>
Port A data register (PDRA)	R/W	00000AH	-XXXXXXXX <sub>B</sub>
Port B data register (PDRB)	R/W	00000BH	XXXXXXXX <sub>B</sub>
Port C data register (PDRC)	R/W	00000CH	XXXXXXXX <sub>B</sub>
Port D data register (PDRD)	R/W	00000DH	XXXXXXXX <sub>B</sub>
Port E data register (PDRE)	R/W	00000EH	XXXXXXXX <sub>B</sub>

(Continued)

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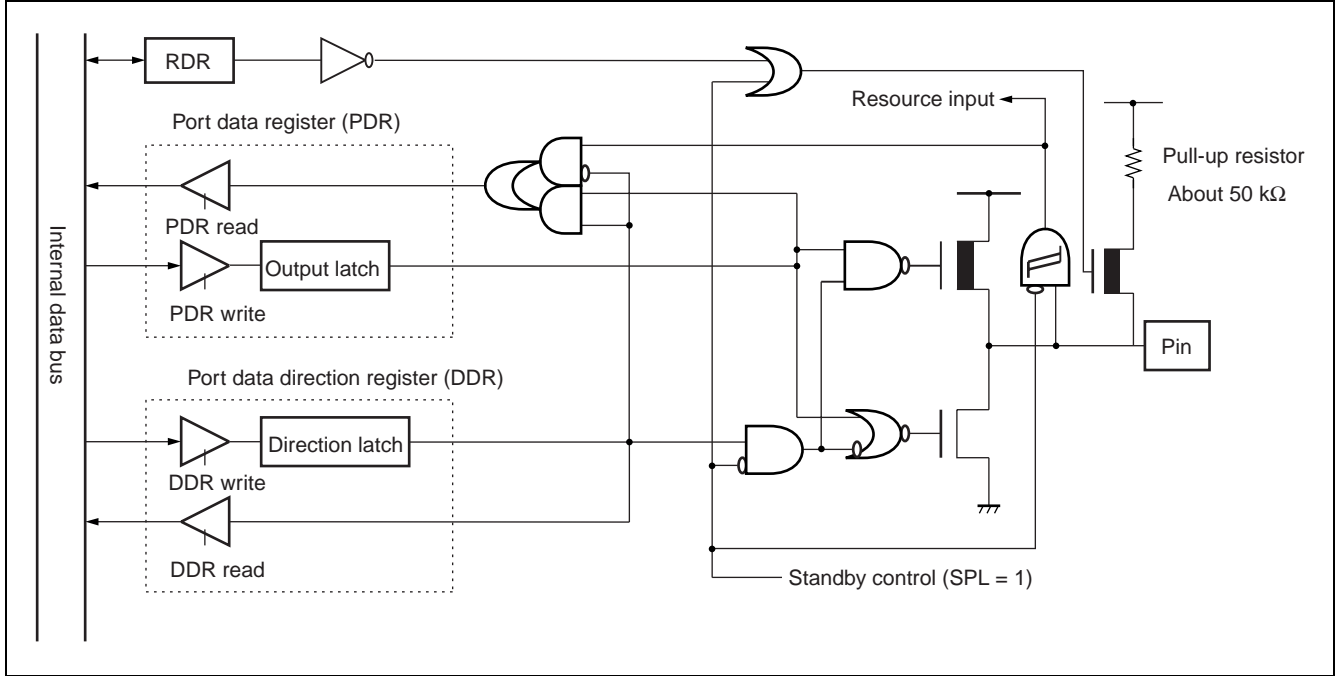
Register	Read/Write	Address	Initial value
Port F data register (PDRF)	R/W	00000FH	XXXXXXXX <sub>B</sub>
Port 0 data direction register (DDR0)	R/W	000010H	00000000 <sub>B</sub>
Port 1 data direction register (DDR1)	R/W	000011H	00000000 <sub>B</sub>
Port 2 data direction register (DDR2)	R/W	000012H	00000000 <sub>B</sub>
Port 3 data direction register (DDR3)	R/W	000013H	00000000 <sub>B</sub>
Port 4 data direction register (DDR4)	R/W	000014H	0----- <sub>B</sub>
Port 5 data direction register (DDR5)	R/W	000015H	00000000 <sub>B</sub>
Port 6 data direction register (DDR6)	R/W	000016H	00000000 <sub>B</sub>
Port 7 data direction register (DDR7)	R/W	000017H	00000000 <sub>B</sub>
Port A data direction register (DDRA)	R/W	00001AH	-0000000 <sub>B</sub>
Port B data direction register (DDRB)	R/W	00001BH	00000000 <sub>B</sub>
Port C data direction register (DDRC)	R/W	00001CH	00000000 <sub>B</sub>
Port D data direction register (DDRD)	R/W	00001DH	00000000 <sub>B</sub>
Port E data direction register (DDRE)	R/W	00001EH	00000000 <sub>B</sub>
Port F data direction register (DDRF)	R/W	00001FH	00000000 <sub>B</sub>
Analog data input enable register (ADER1)	R/W	00002AH	11111111 <sub>B</sub>
Analog data input enable register (ADER2)	R/W	00002BH	----1111 <sub>B</sub>
Comparator input enable register (CIER)	R/W	0000E0H	---11111 <sub>B</sub>
LCD control register 1 (LCRH)	R/W	0000EFH	00000000 <sub>B</sub>
Port 0 pull-up resistor setting register (RDR0)	R/W	00008CH	00000000 <sub>B</sub>
Port 1 pull-up resistor setting register (RDR1)	R/W	00008DH	00000000 <sub>B</sub>
Port 2 pull-up resistor setting register (RDR2)	R/W	00008EH	00000000 <sub>B</sub>
Port 3 pull-up resistor setting register (RDR3)	R/W	00008FH	00000000 <sub>B</sub>
Port 3 data latch register (PDL3)	R/W	0000EAH	00000000 <sub>B</sub>

R/W : Read/write enabled  
 X : Undefined  
 - : Not used

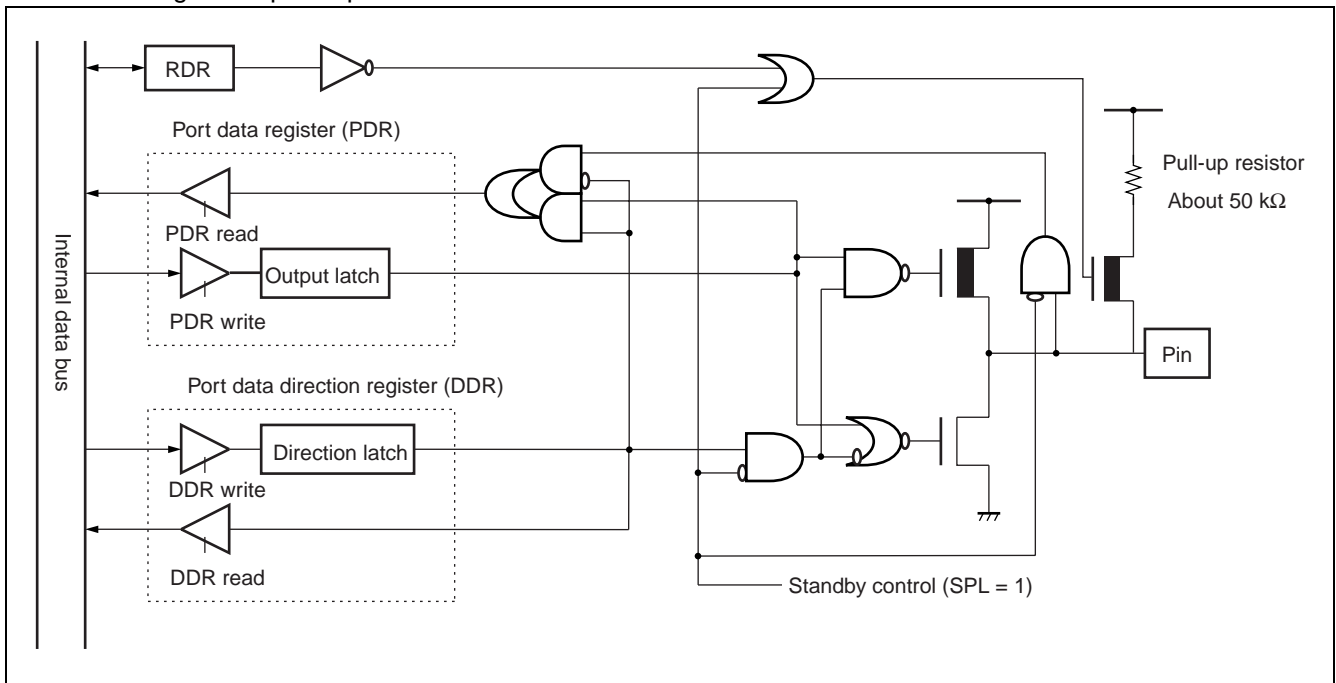
# MB90370 Series

## (3) Block diagram of I/O ports

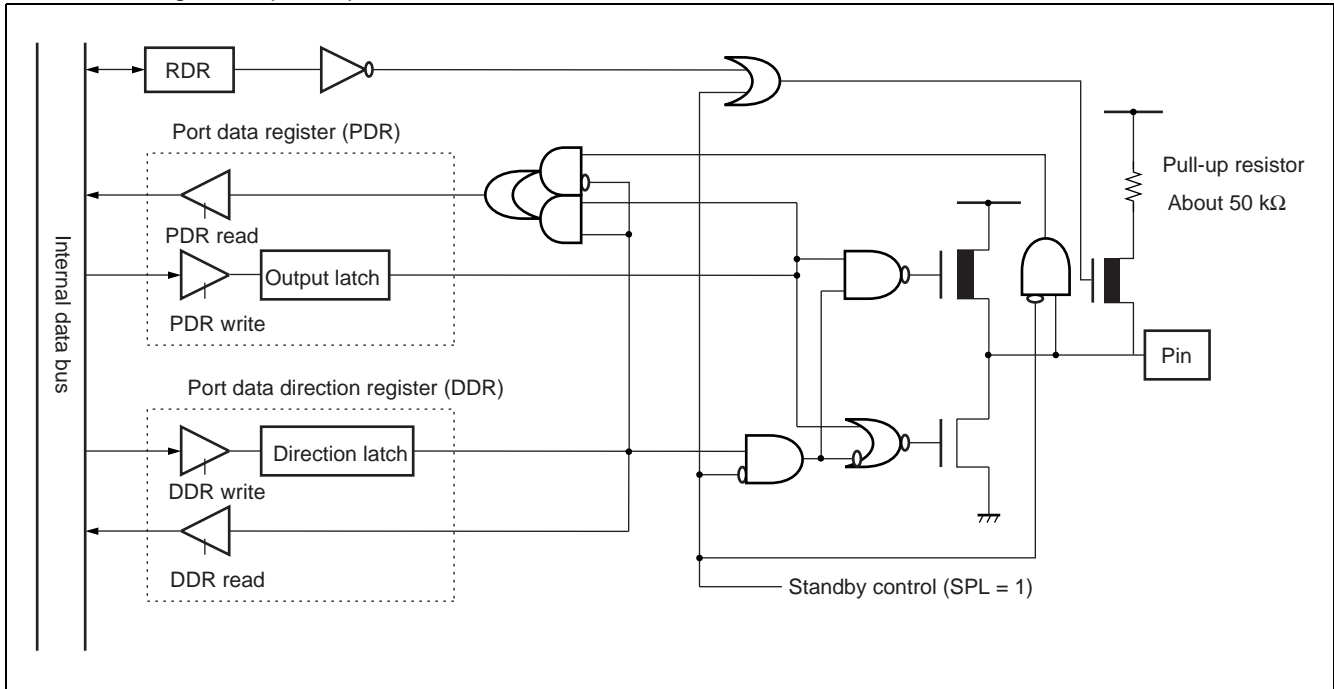
- Block diagram of port 0 pins



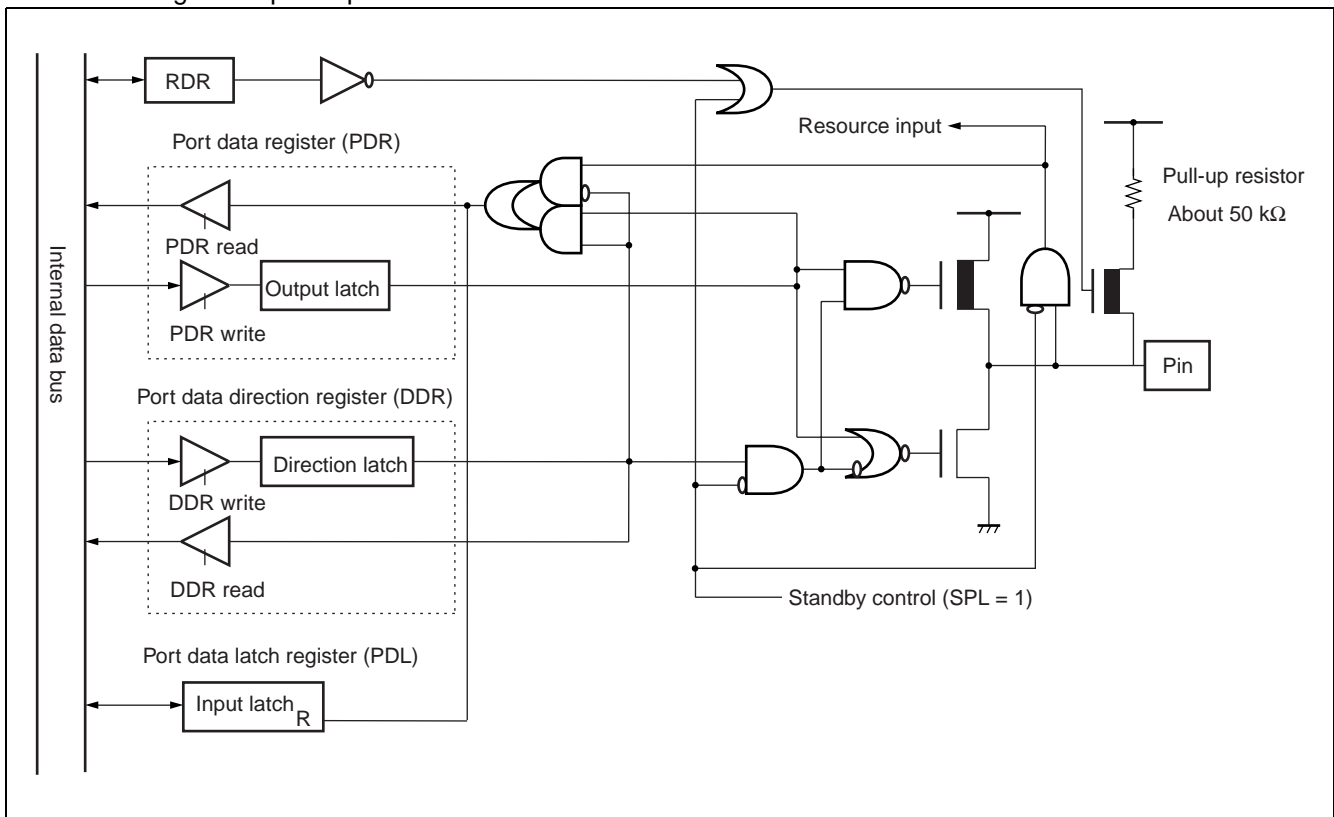
- Block diagram of port 1 pins



• Block diagram of port 2 pins

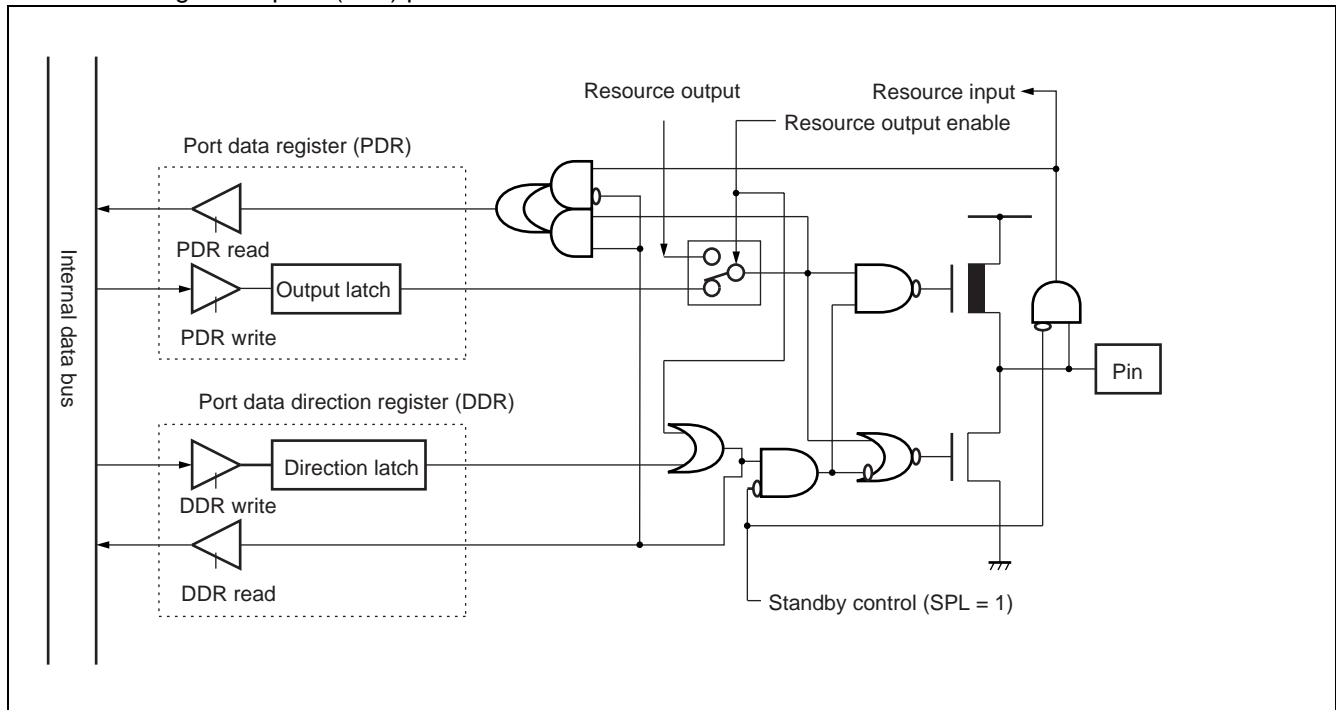


• Block diagram of port 3 pins

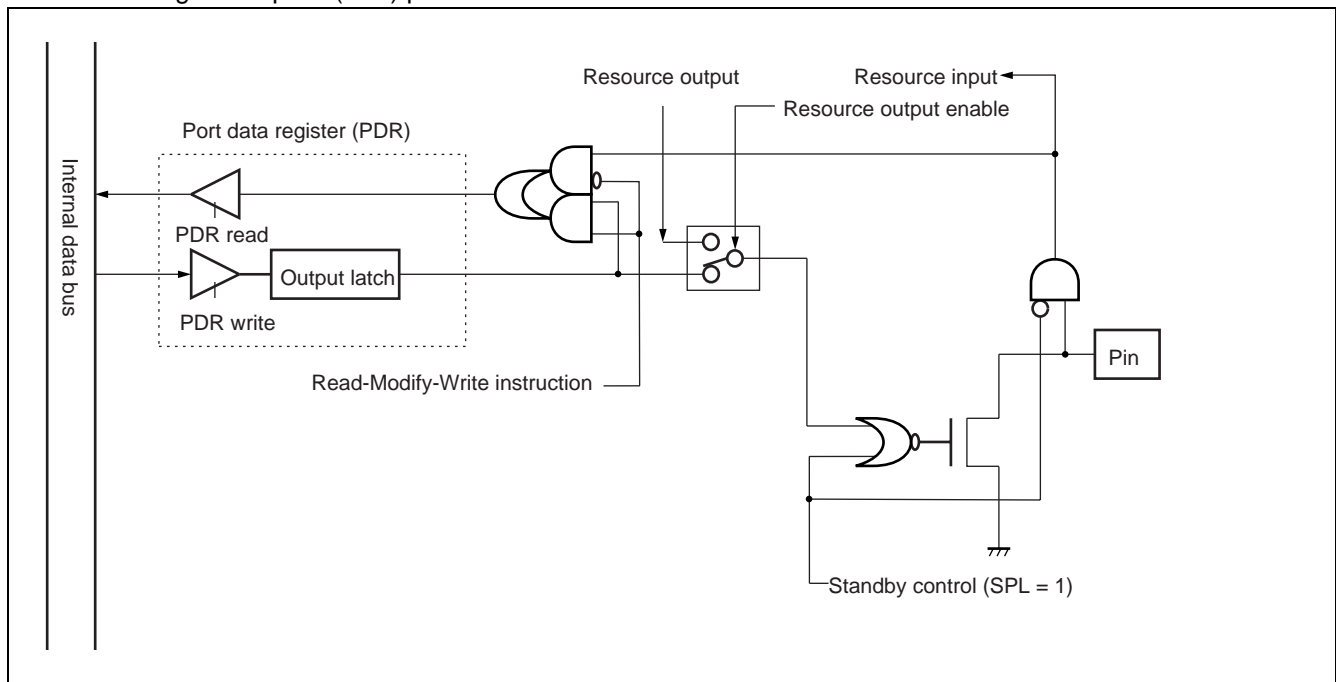


# MB90370 Series

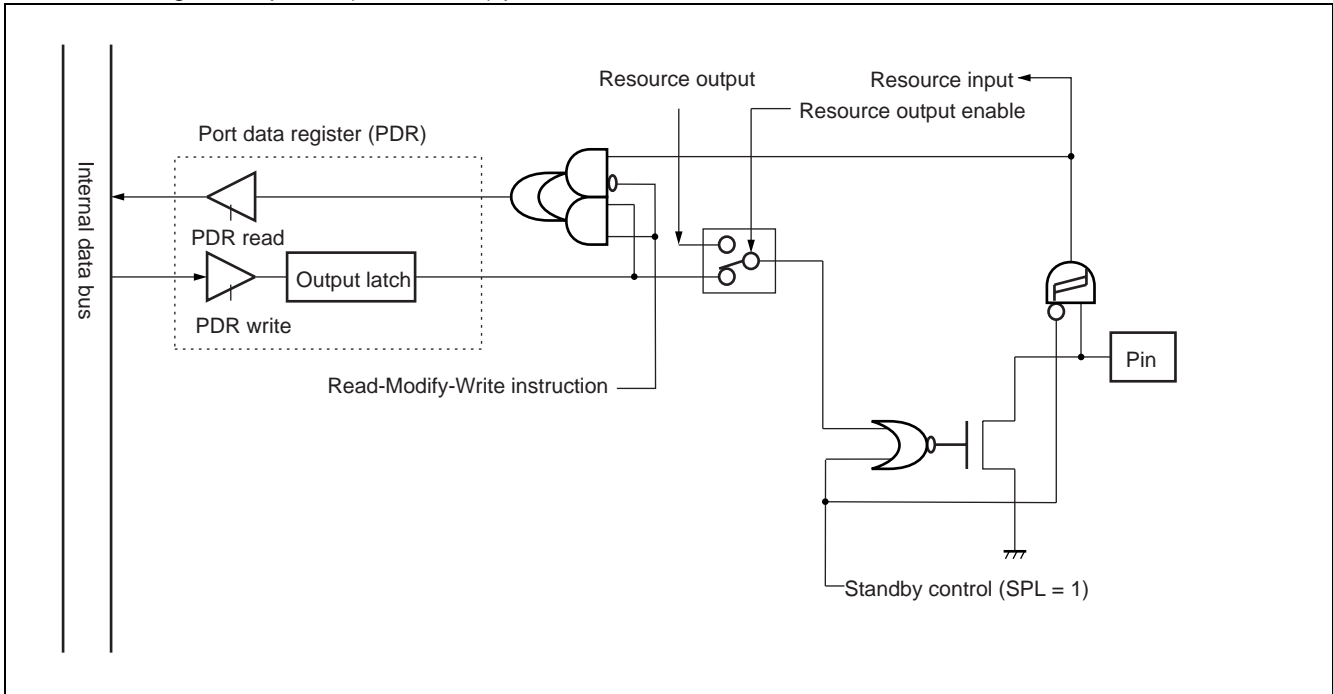
- Block diagram of port (P47) pin



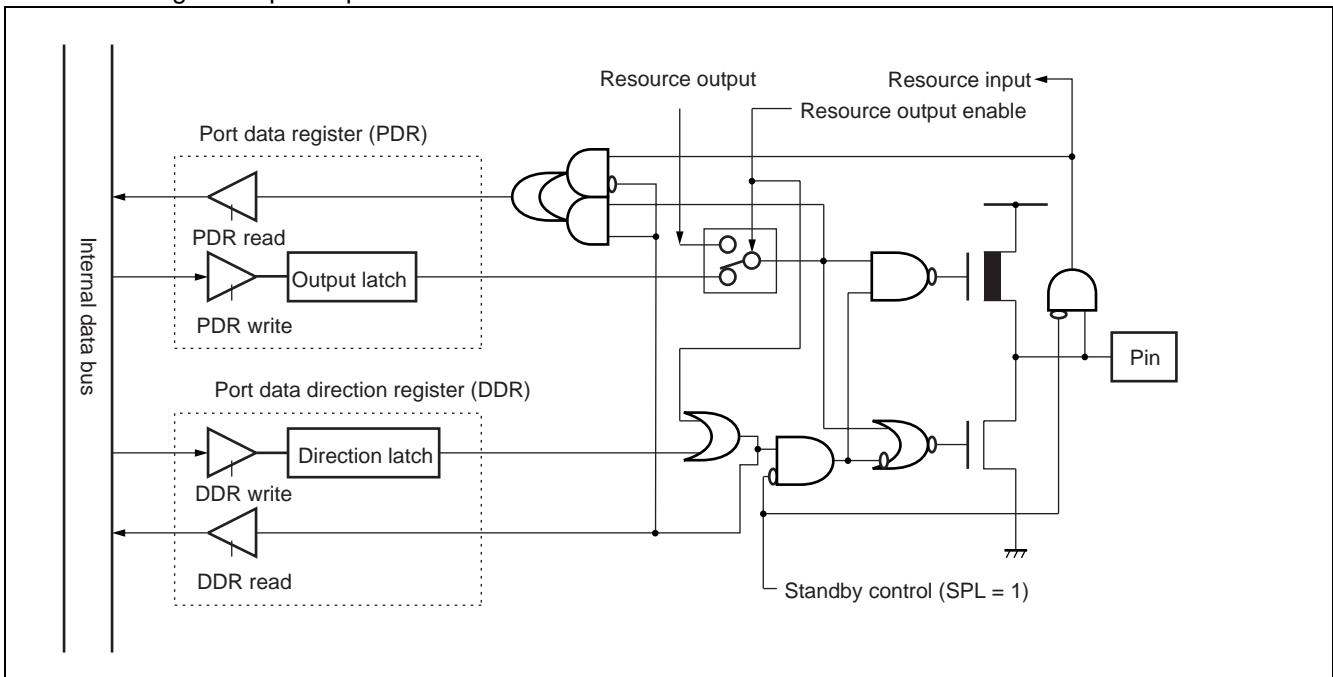
- Block diagram of port (P46) pin



- Block diagram of port 4 (P45 to P40) pins

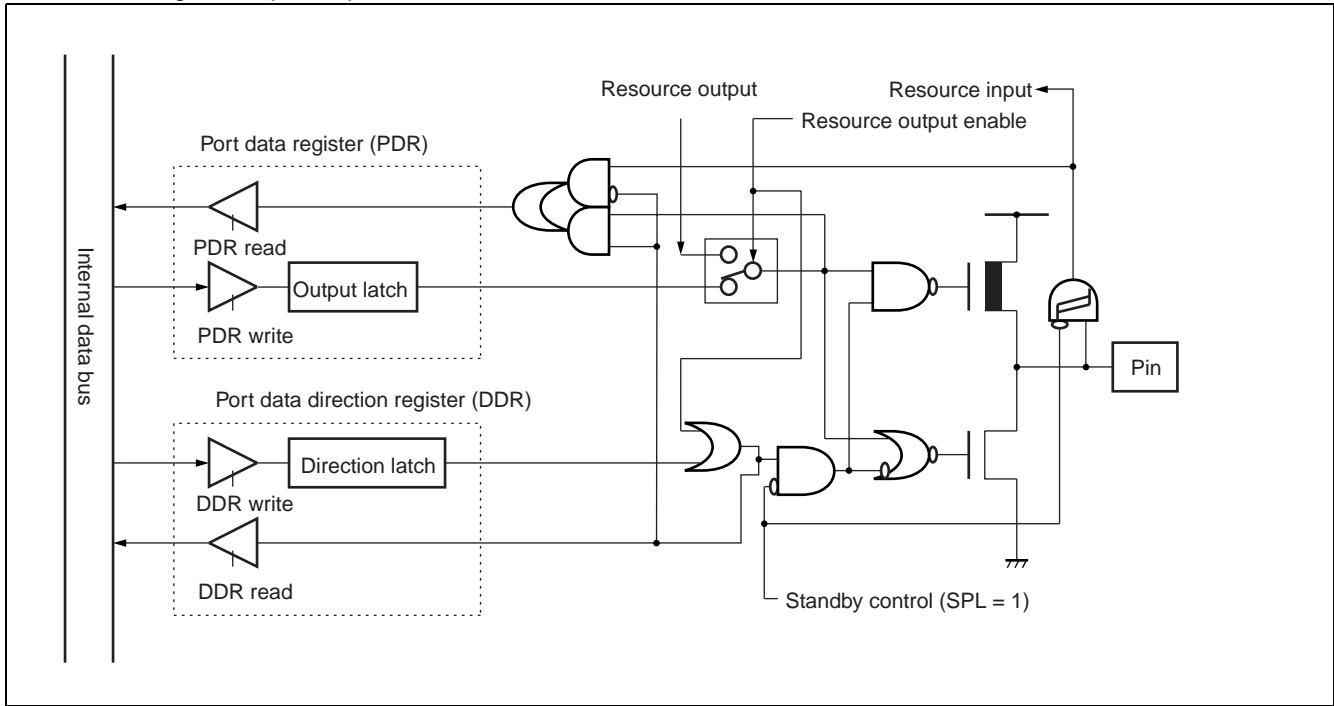


- Block diagram of port 5 pins

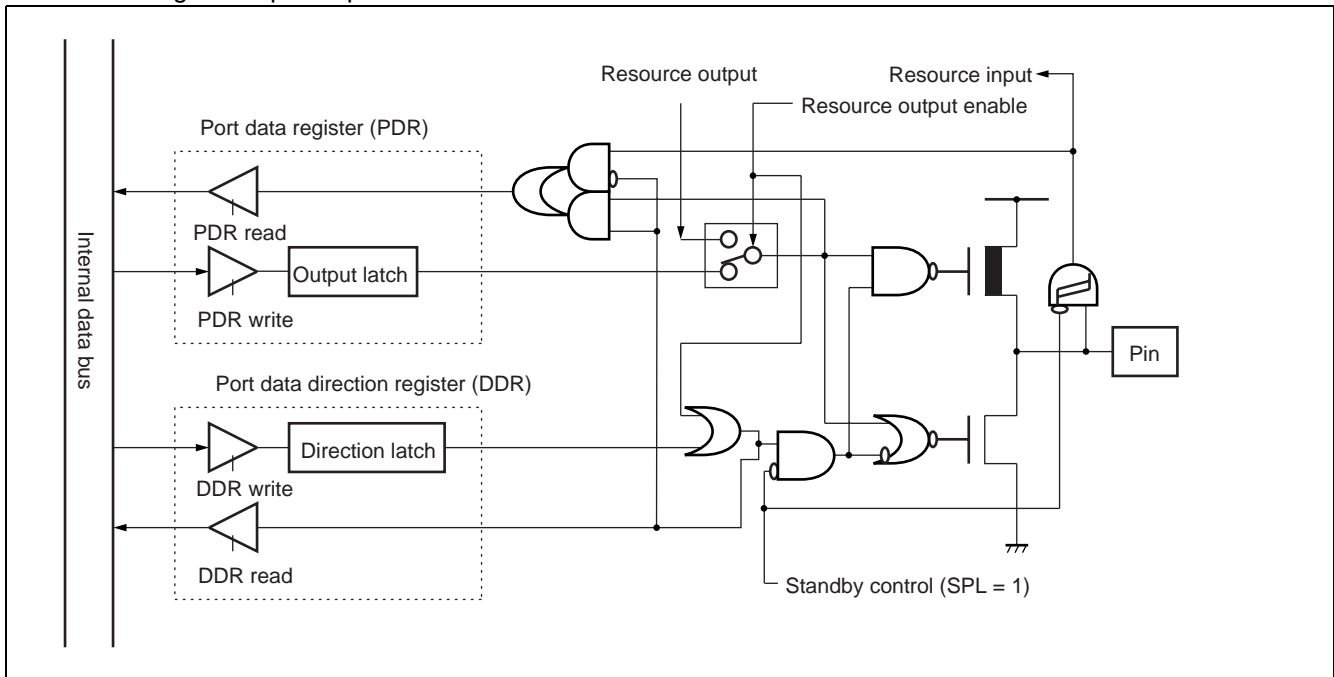


# MB90370 Series

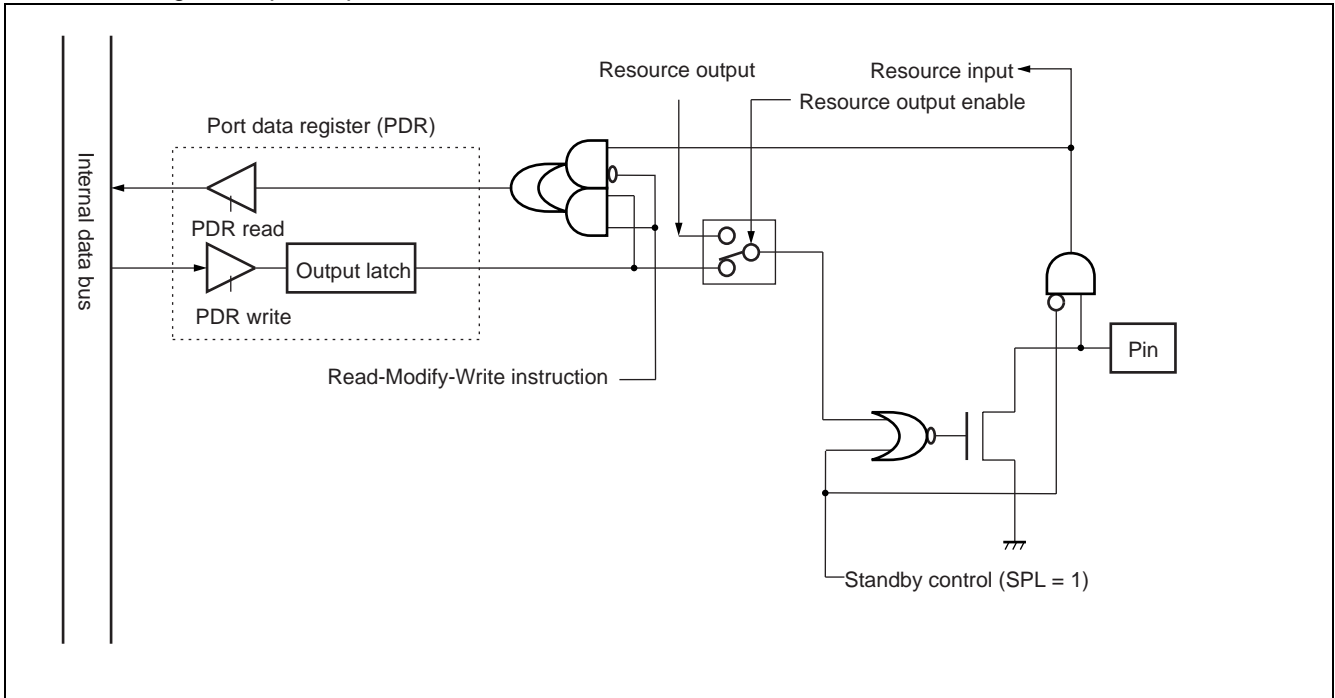
- Block diagram of port 6 pins



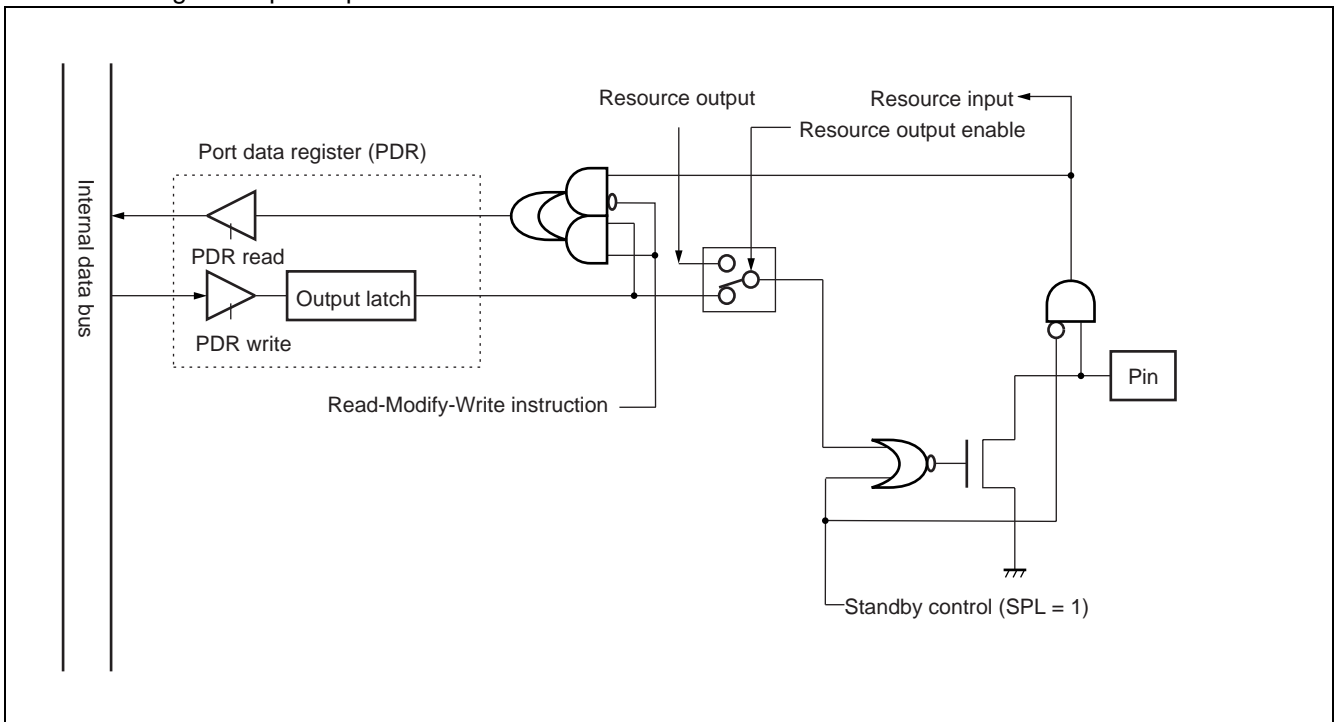
- Block diagram of port 7 pins



- Block diagram of port 8 pins

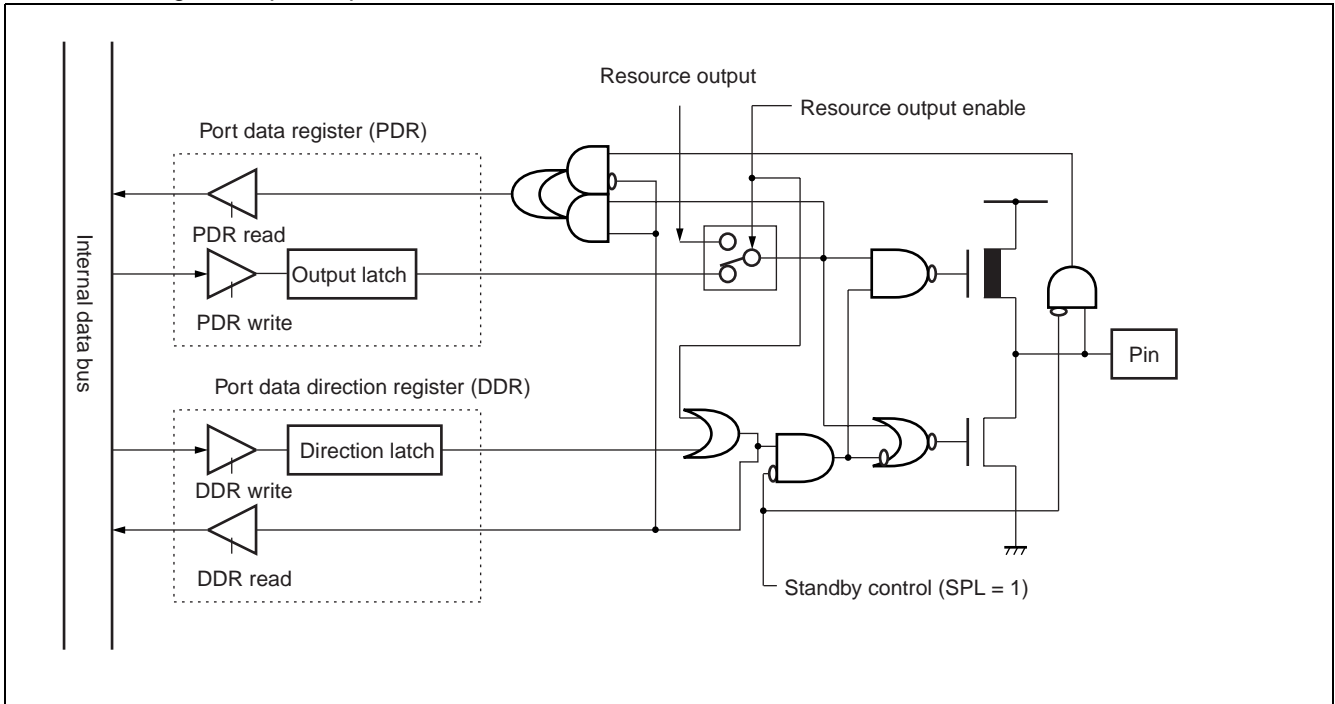


- Block diagram of port 9 pins

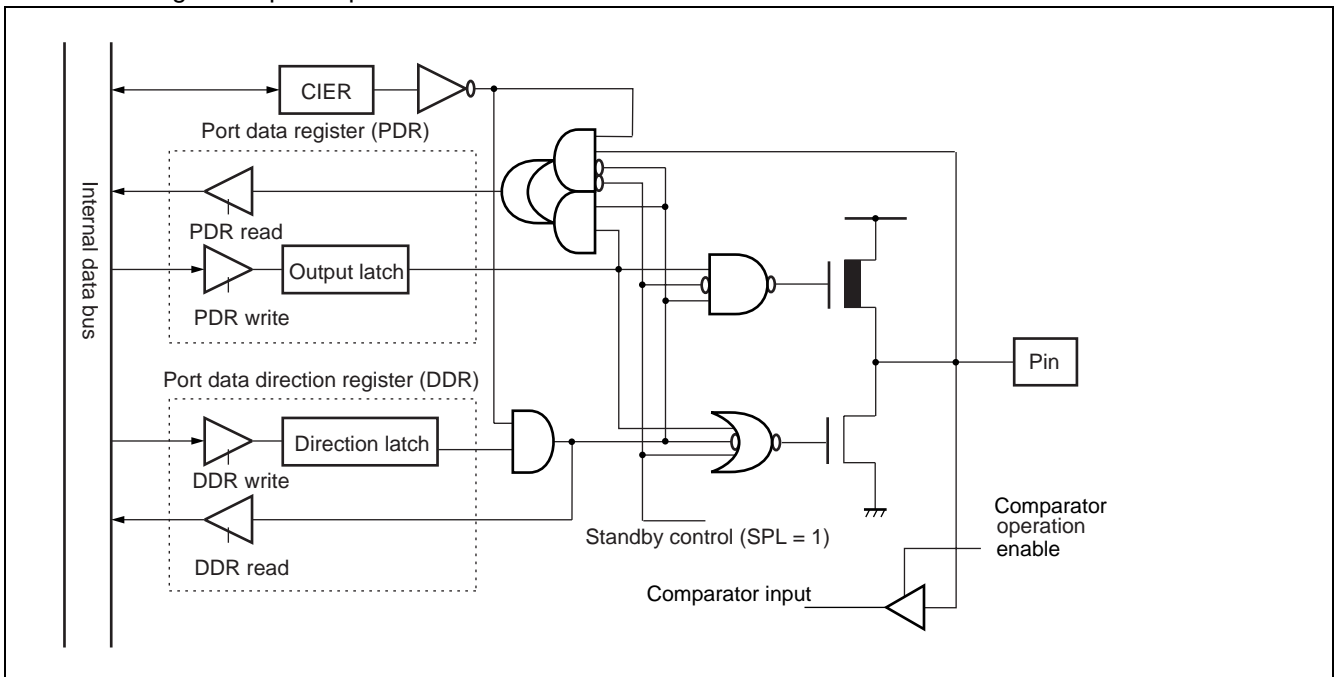


# MB90370 Series

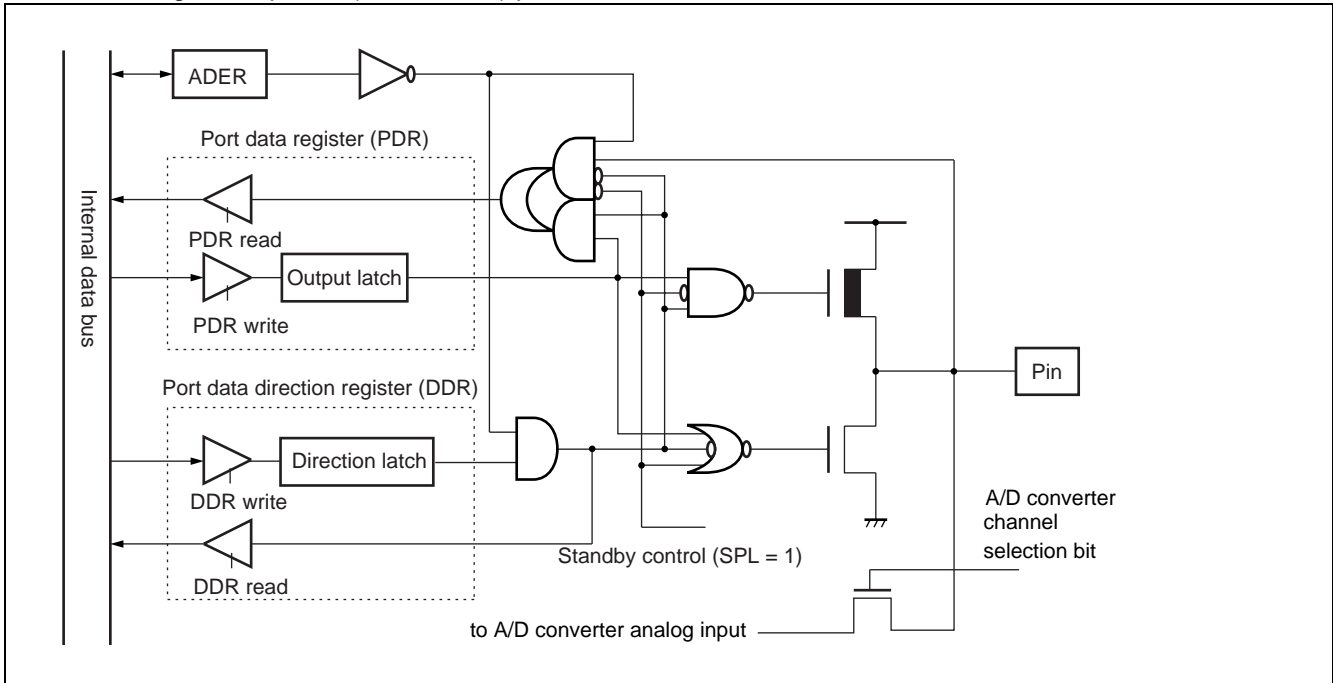
- Block diagram of port A pins



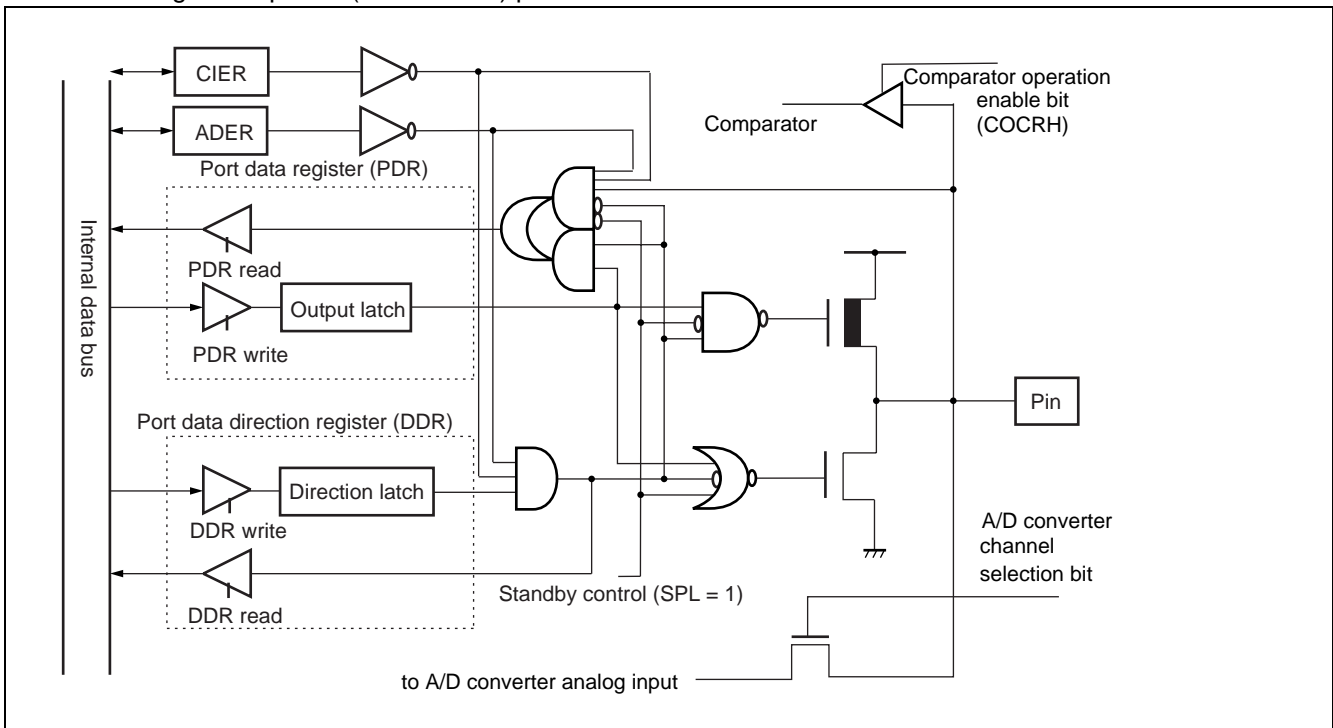
- Block diagram of port B pins



• Block diagram of port C (PC7 to PC3) pins

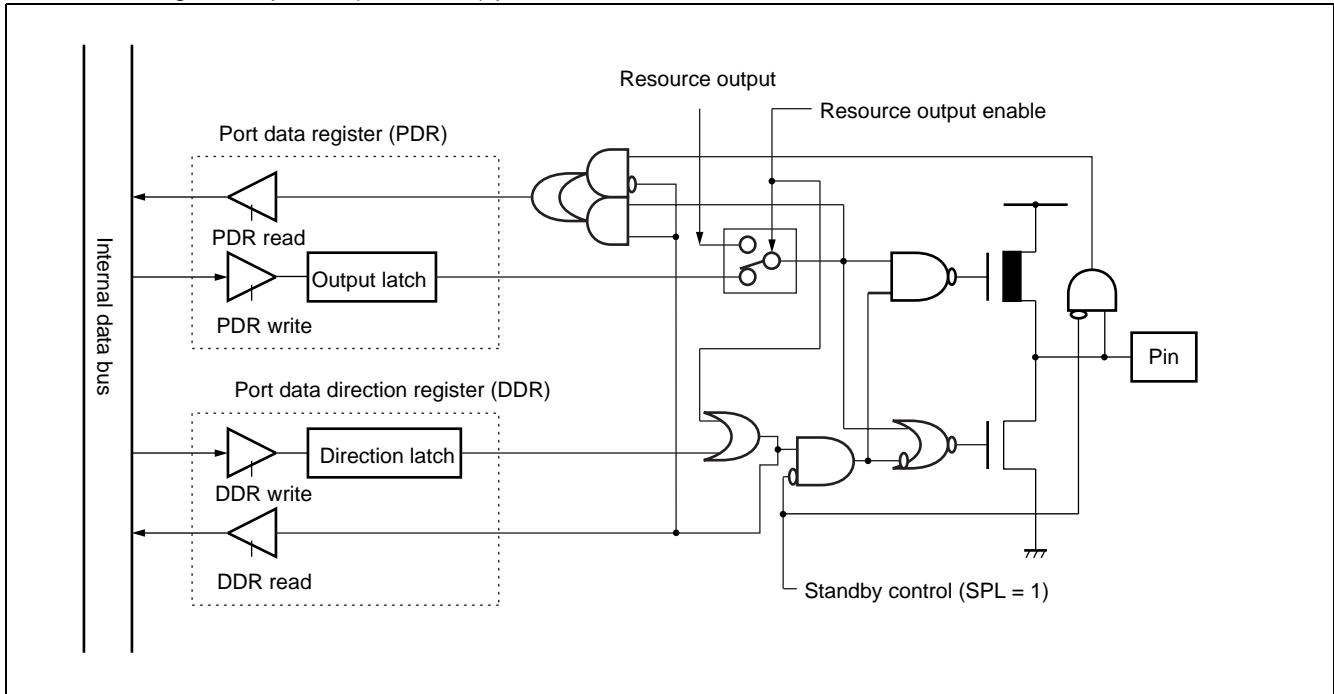


• Block diagram of port C (PC2 to PC0) pins

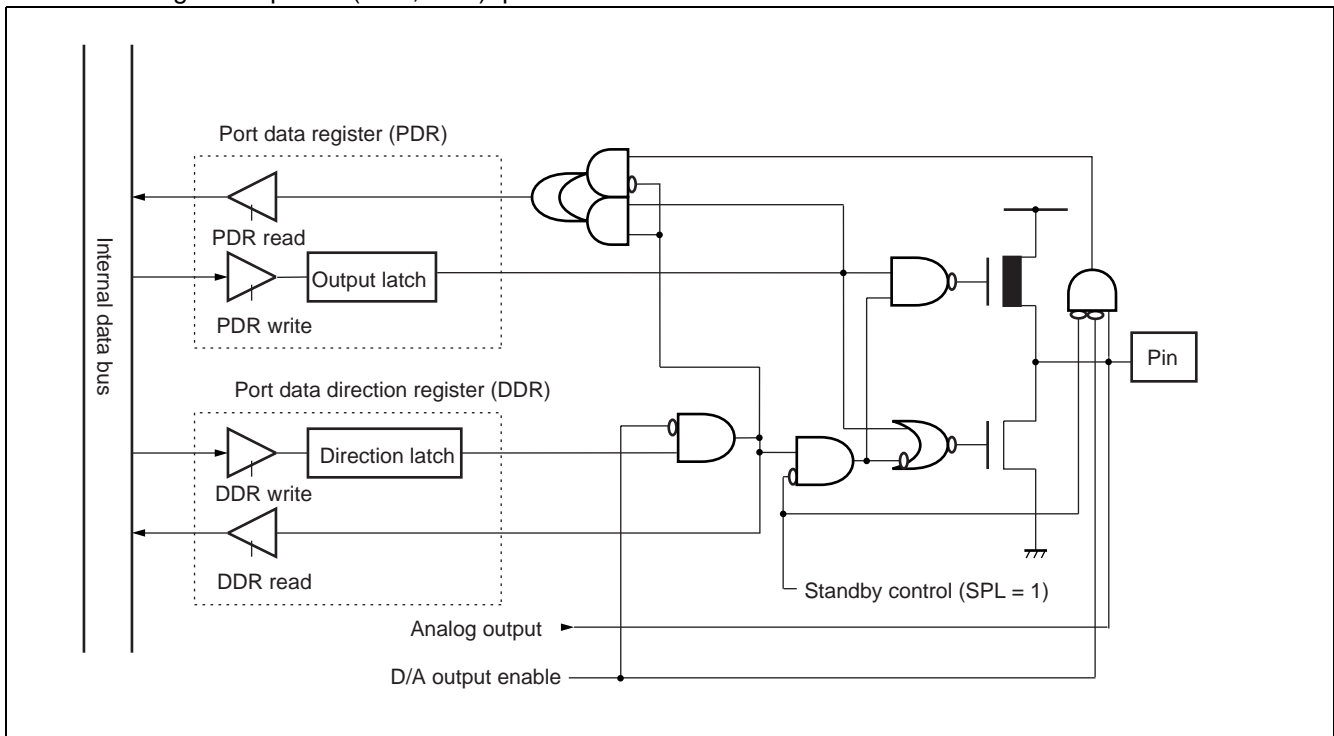


# MB90370 Series

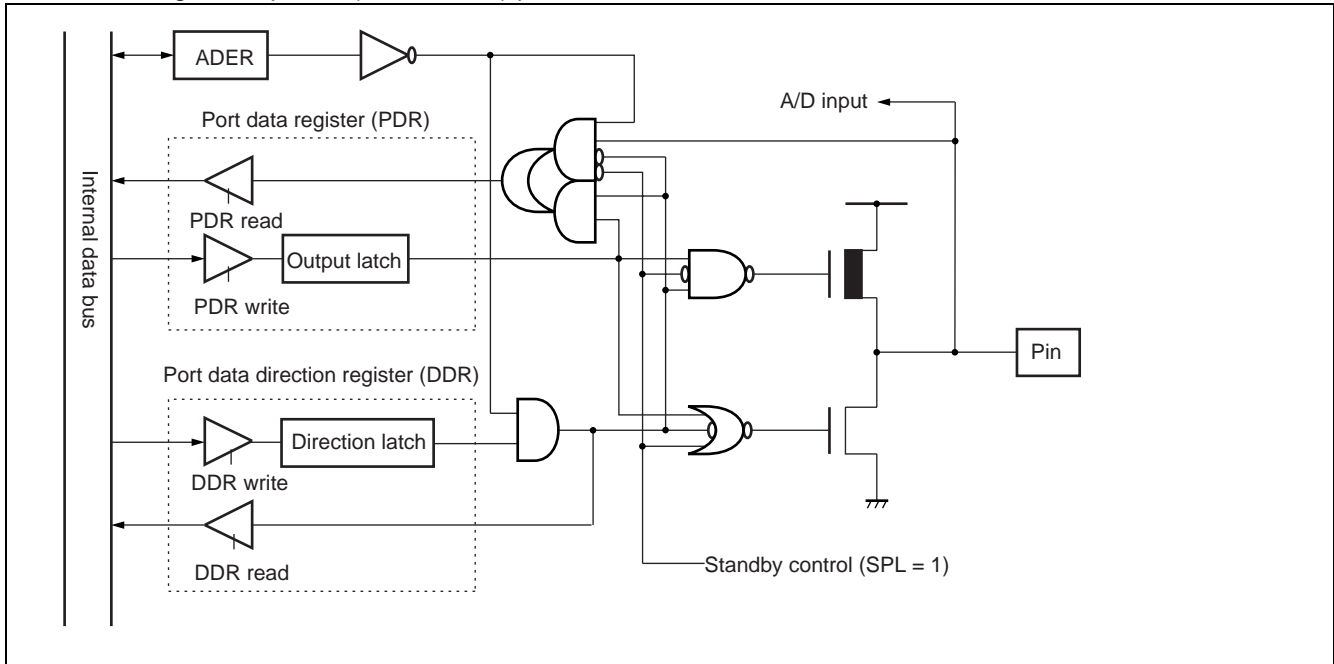
- Block diagram of port D (PD7, PD6) pins



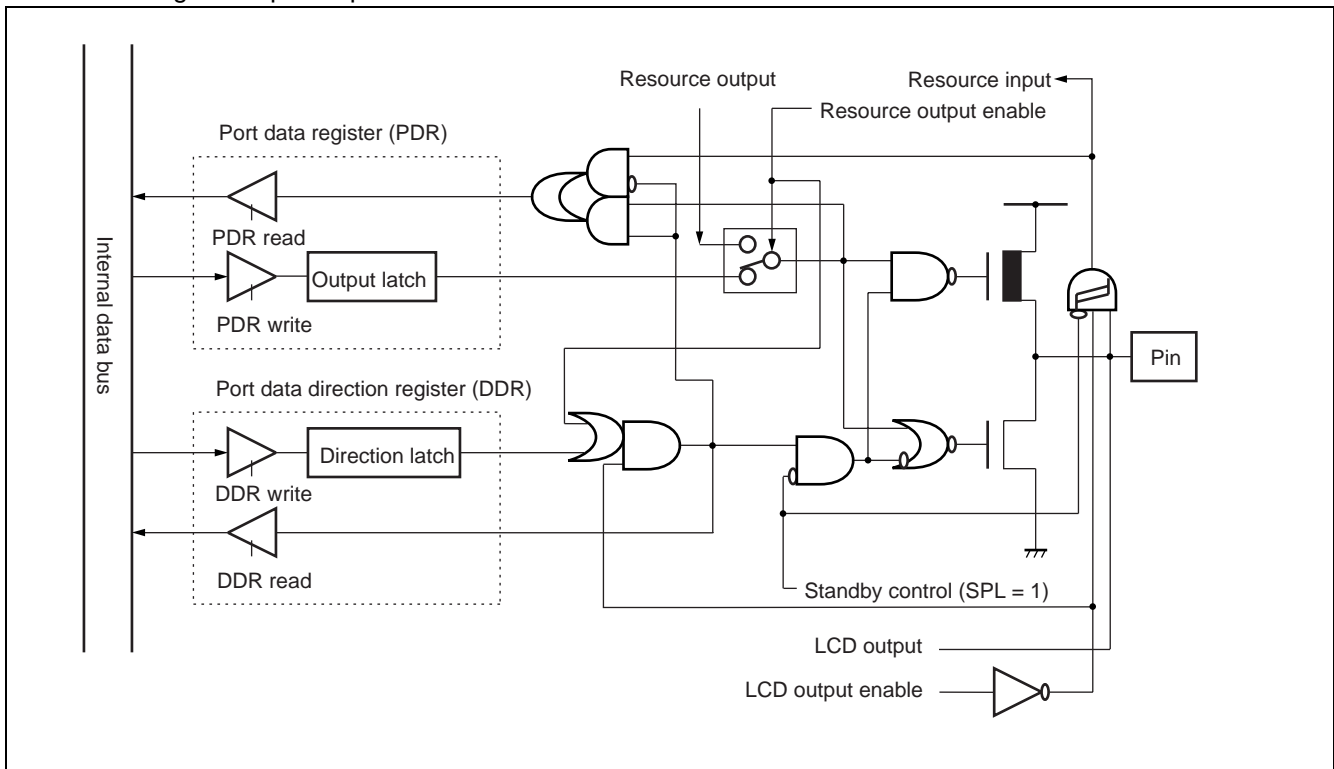
- Block diagram of port D (PD5, PD4) pins



- Block diagram of port D (PD3 to PD0) pins

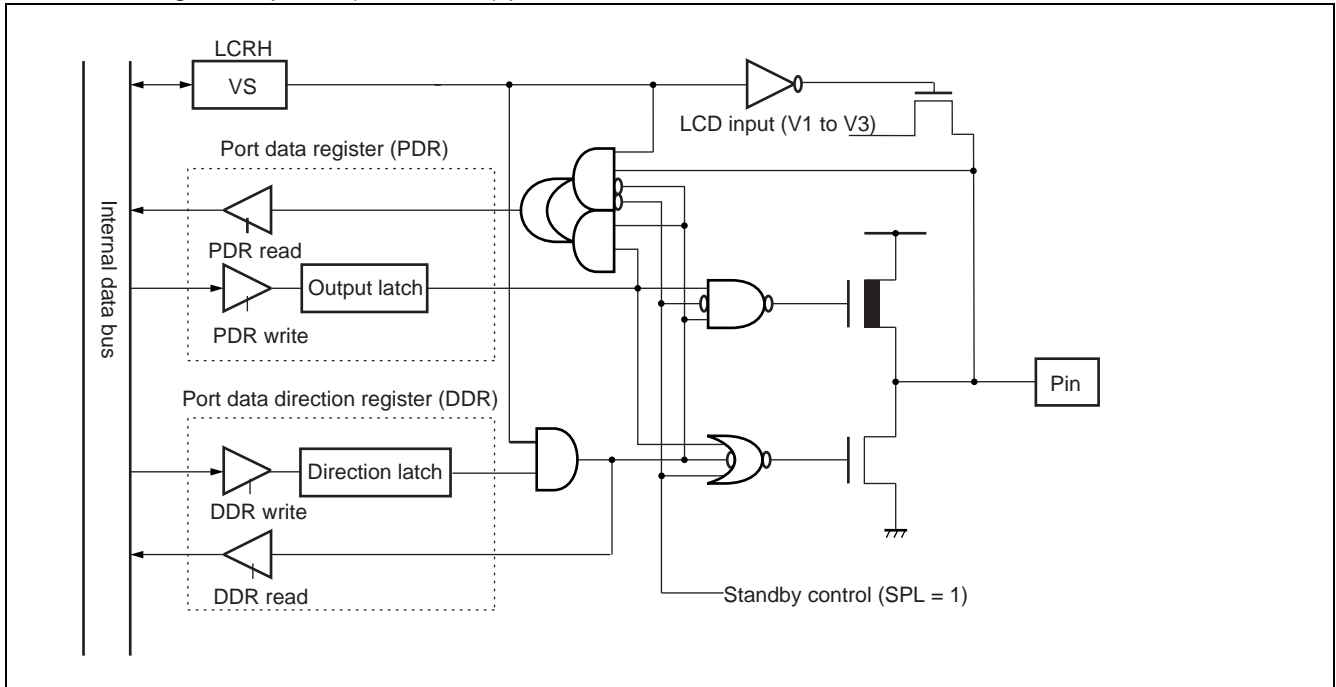


- Block diagram of port E pins

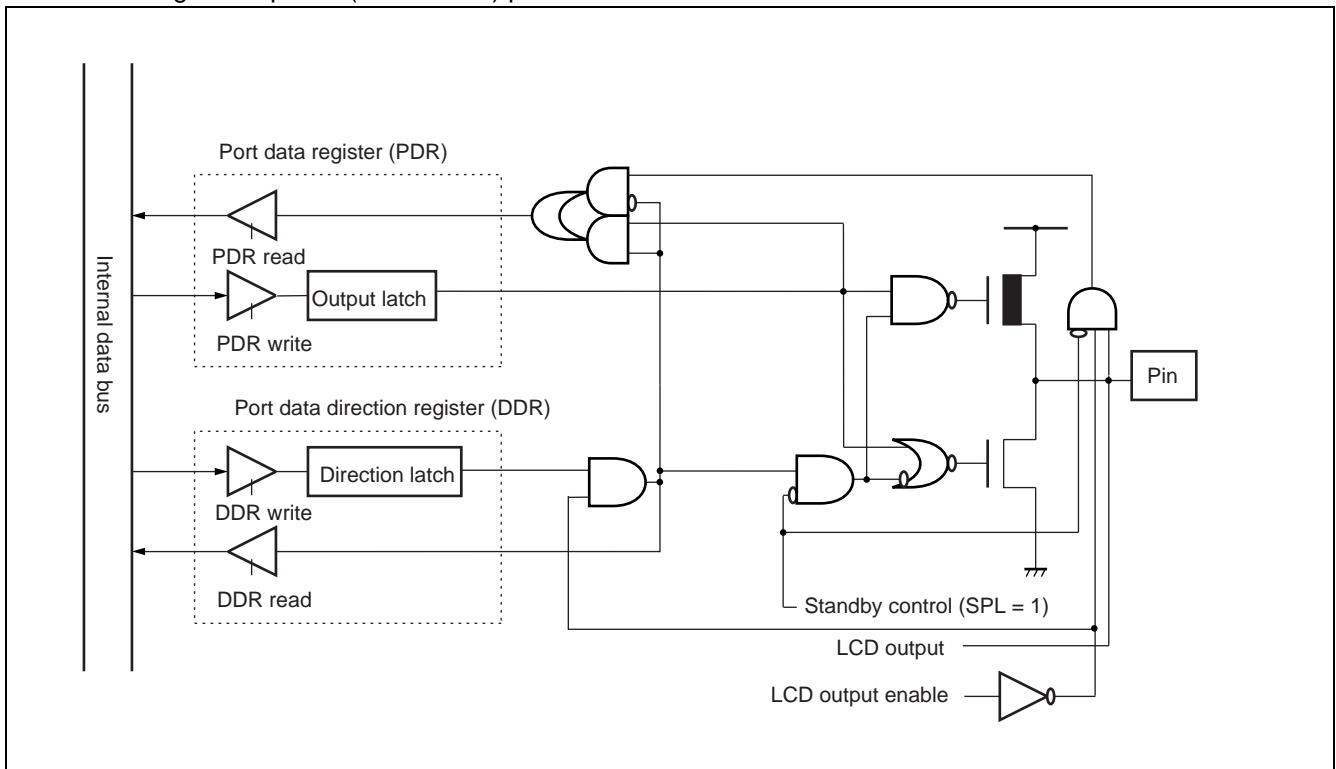


# MB90370 Series

- Block diagram of port F (PF7 to PF5) pins



- Block diagram of port F (PF4 to PF0) pins



## 3. Timebase timer

The timebase timer is an 18-bit free-running counter (timebase counter) that counts up in synchronization with the internal count clock (one-half of the source oscillation) .

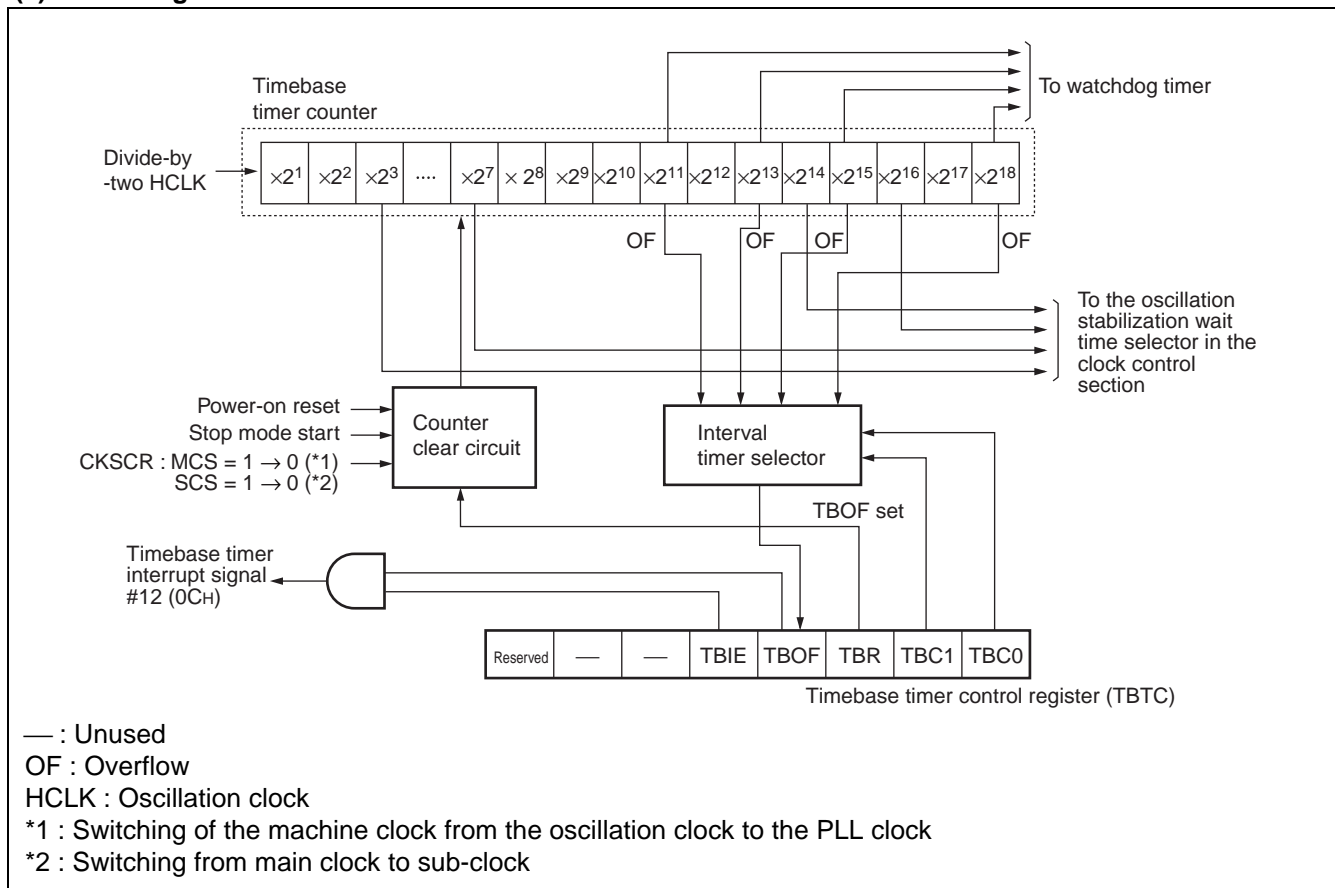
Features of timebase timer :

- Interrupt generated when counter overflow
- EI<sup>2</sup>OS supported
- Interval timer function :  
An interrupt generated at four different time intervals
- Clock supply function :  
Four different clocks can be selected as watchdog timer's count clock.  
Supply clock for oscillation stabilization

### (1) Register configuration

Timebase Timer Control Register									Bit number
Address : 0000A9H	15	14	13	12	11	10	9	8	⇐ TBTC
Read/write	⇒ R/W	—	—	R/W	R/W	R/W	R/W	R/W	
Initial value	⇒ 1	—	—	0	0	1	0	0	

### (2) Block diagram of timebase timer



## 4. Watchdog timer

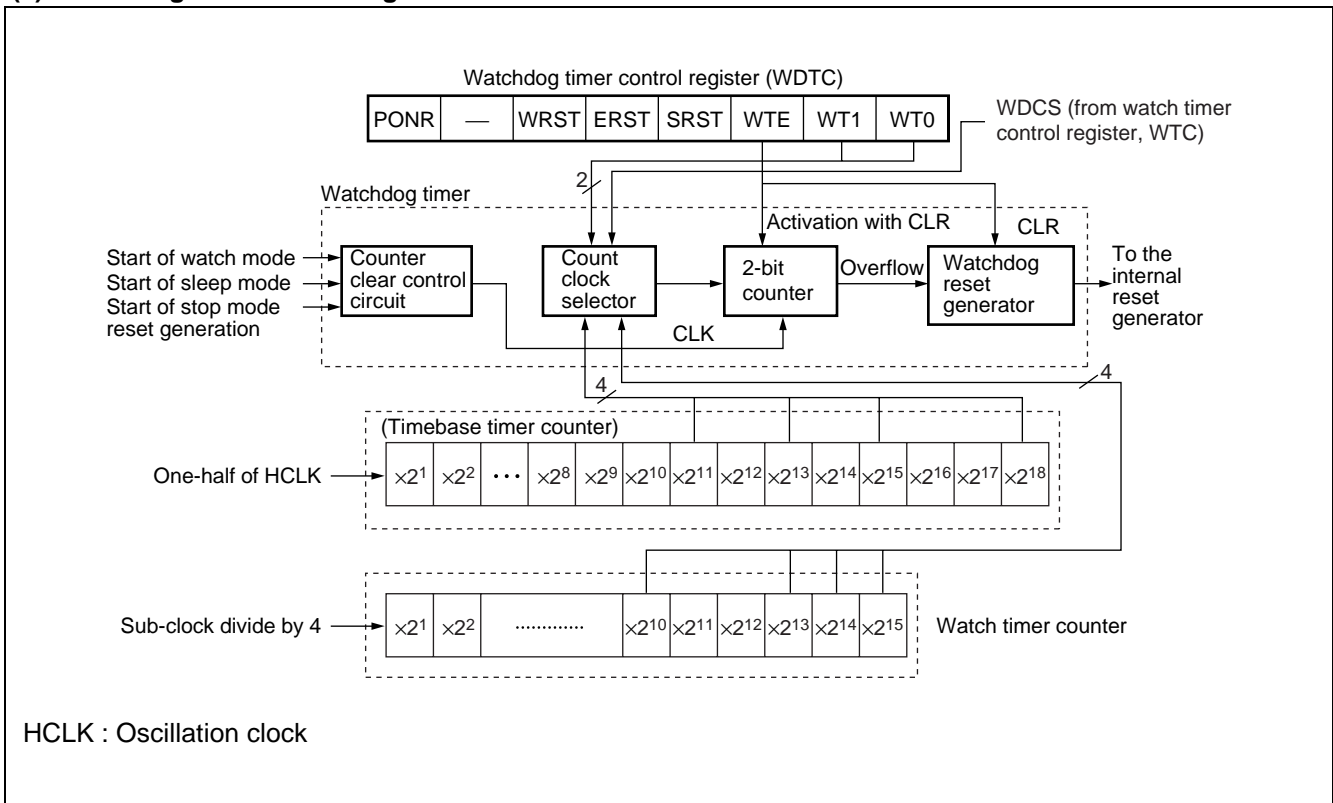
The watchdog timer is a 2-bit counter that uses the timebase timer's supply clock as the count clock. After activation, if the watchdog timer is not cleared within a given period, the CPU will be reset.

- Features of watchdog timer :
  - Reset CPU at four different time intervals
  - Status bits to indicate the reset causes

### (1) Register configuration of watchdog timer

Watchdog Timer Control Register								Bit number	
Address : 0000A8H	7	6	5	4	3	2	1	0	WDTC
	PONR	—	WRST	ERST	SRST	WTE	WT1	WT0	
Read/write	R	—	R	R	R	W	W	W	
Initial value	X	—	X	X	X	1	1	1	

### (2) Block diagram of watchdog timer



## 5. Watch timer

The watch timer is a 15-bit timer that uses sub-clocks and can generate an interval interrupt. It can also be used as the watchdog timer clock source and sub-clock oscillation wait time.

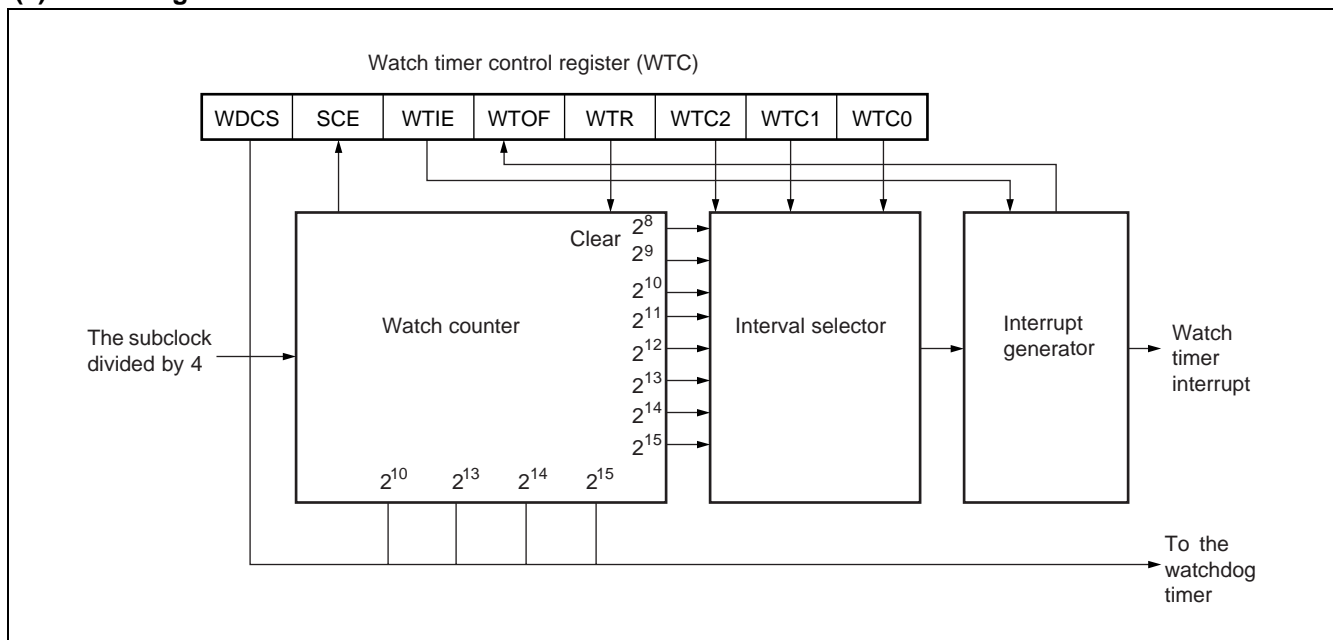
Features of the watch timer :

- Provides the watchdog timer clock source
- Sub-clock oscillation stabilization wait timer function
- Interval timer function that generates interrupts in a given cycle

### (1) Register configuration of watch timer

Watch Timer Control Register										Bit number
Address : 0000AAH		7	6	5	4	3	2	1	0	↔
		WDCS	SCE	WTIE	WTOF	WTR	WTC2	WTC1	WTC0	WTC
Read/write	↔	R/W	R	R/W	R/W	W	R/W	R/W	R/W	
Initial value	↔	1	0	0	0	1	0	0	0	

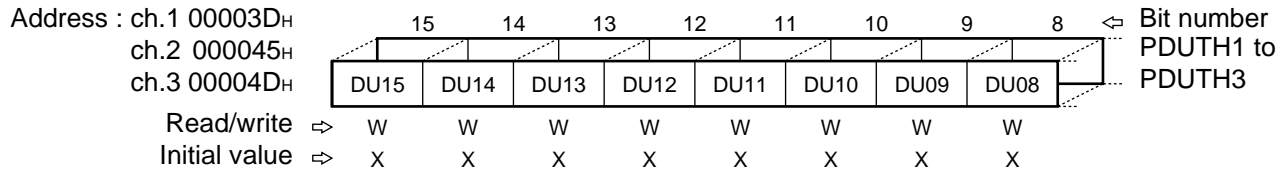
### (2) Block diagram of watch timer



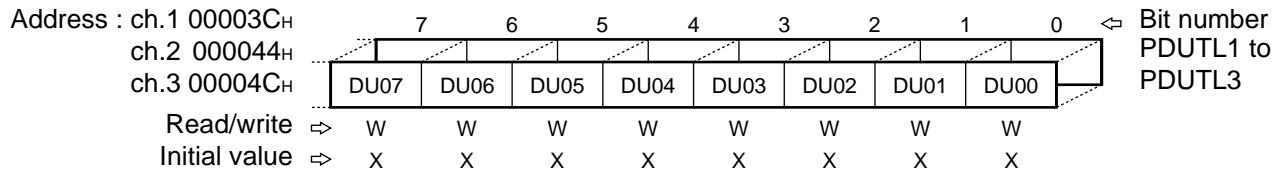


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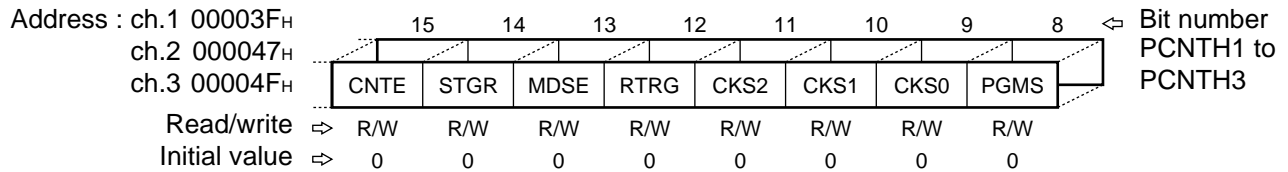
### PPG Duty Setting Buffer Register (Upper)



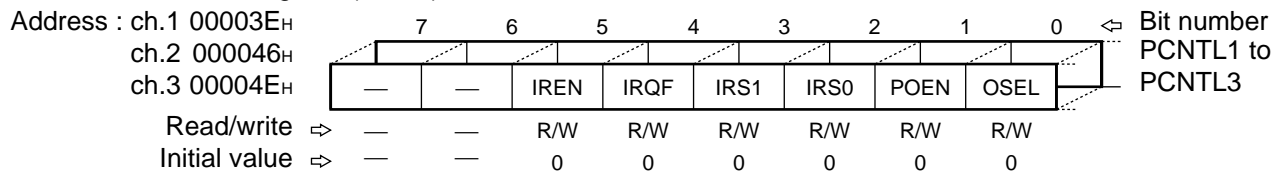
### PPG Duty Setting Buffer Register (Lower)



### PPG Control Status Register (Upper)

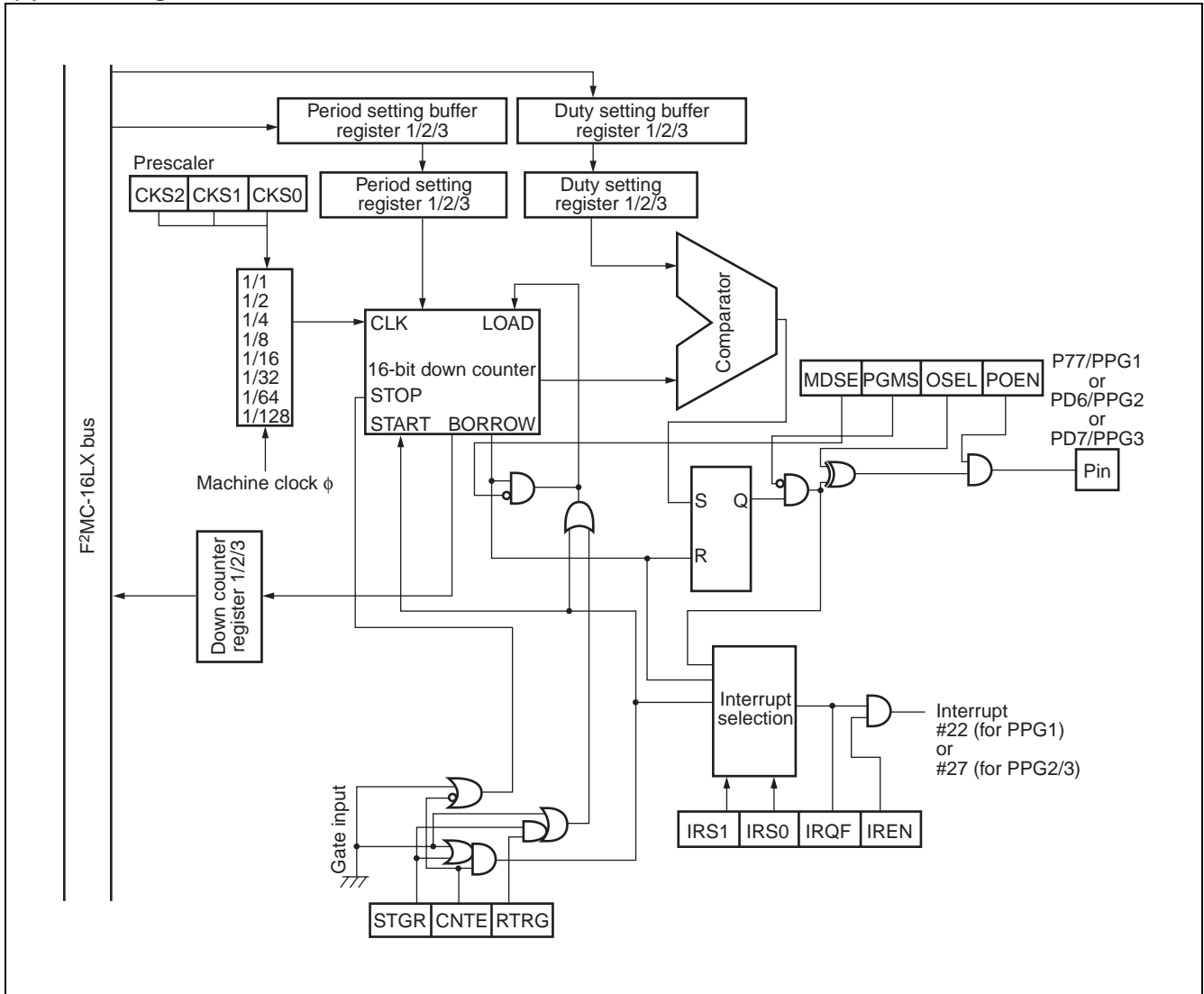


### PPG Control Status Register (Lower)



Note : Registers PDCR1 to PDCR3, PCSR1 to PCSR3 and PDUT1 to PDUT3 are word access only.

## (2) Block diagram of PPG timer



## 7. 16-bit reload timer (× 4)

The 16-bit reload timer provides two operating modes, internal clock mode and event count mode. In each operating mode, the 16-bit down counter can be reloaded (reload mode) or stopped when underflow (one-shot mode).

Output pins TO1 to TO4 are able to output different waveform according to the counter operating mode. TO1 to TO4 toggles when counter underflow if counter is operated as reload mode. TO1 to TO4 output specified level (“H” or “L”) when counter is counting if the counter is in one-shot mode.

Features of the 16-bit reload timer :

- Interrupt generated when timer underflow
- EI²OS supported
- Internal clock operating mode :  
Three internal count clocks can be selected.  
Counter can be activated by software or external trigger (signal at TIN1 to TIN4 pin).  
Counter can be reloaded or stopped when underflow after activated.
- Event count operating mode :  
Counter counts down by one when specified edge at TIN1 to TIN4 pin.  
Counter can be reloaded or stopped when underflow.

### (1) Register configuration of reload timer

Timer Control Status Register (Upper)

Address : ch.1 000071H

ch.2 000075H

ch.3 000079H

ch.4 00007DH

15	14	13	12	11	10	9	8	↔
—	—	—	—	CSL1	CSL0	MOD2	MOD1	

Bit number  
TMCSRH1 to  
TMCSRH4

Read/write ↗ — — — — R/W R/W R/W R/W  
Initial value ↗ — — — — 0 0 0 0

Timer Control Status Register (Lower)

Address : ch.1 000070H

ch.2 000074H

ch.3 000078H

ch.4 00007CH

7	6	5	4	3	2	1	0	↔
MOD0	OUTE	OUTL	RELD	INTE	UF	CNTE	TRG	

Bit number  
TMCSRL1 to  
TMCSRL4

Read/write ↗ R/W R/W R/W R/W R/W R/W R/W  
Initial value ↗ 0 0 0 0 0 0 0 0

16-bit Timer Register / 16-bit Reload Register (Upper)

Address : ch.1 000073H

ch.2 000077H

ch.3 00007BH

ch.4 00007FH

15	14	13	12	11	10	9	8	↔
D15	D14	D13	D12	D11	D10	D09	D08	

Bit number  
TMR1 to TMR4/  
TMRD1 to  
TMRD4

Read/write ↗ R/W R/W R/W R/W R/W R/W R/W R/W  
Initial value ↗ X X X X X X X X

16-bit Timer Register / 16-bit Reload Register (Lower)

Address : ch.1 000072H

ch.2 000076H

ch.3 00007AH

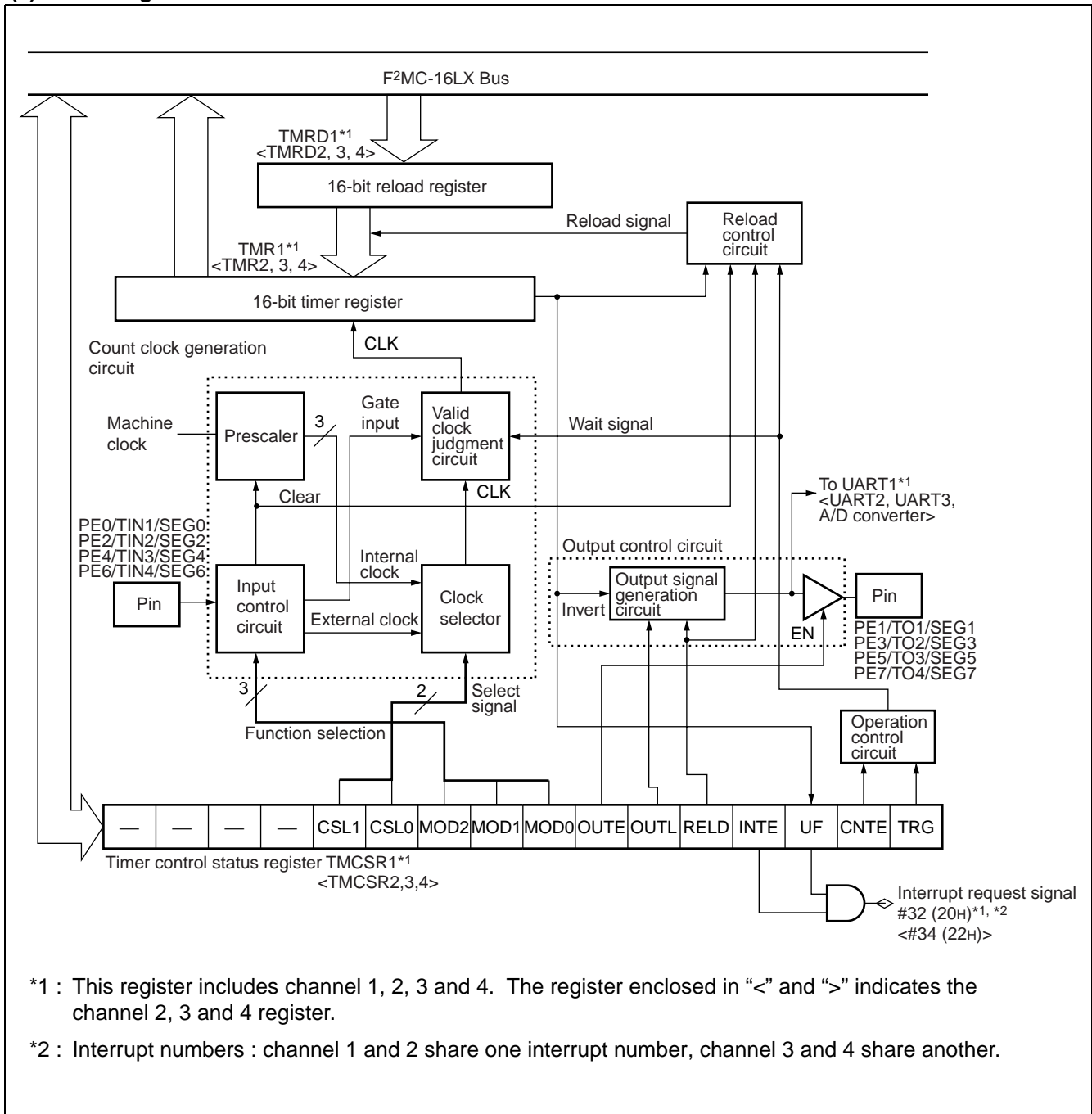
ch.4 00007EH

7	6	5	4	3	2	1	0	↔
D07	D06	D05	D04	D03	D02	D01	D00	

Bit number  
TMR1 to TMR4/  
TMRD1 to  
TMRD4

Read/write ↗ R/W R/W R/W R/W R/W R/W R/W R/W  
Initial value ↗ X X X X X X X X

## (2) Block diagram of reload timer



\*1 : This register includes channel 1, 2, 3 and 4. The register enclosed in “<” and “>” indicates the channel 2, 3 and 4 register.

\*2 : Interrupt numbers : channel 1 and 2 share one interrupt number, channel 3 and 4 share another.

## 8. I<sup>2</sup>C

The I<sup>2</sup>C (Inter IC Bus) interface is a simple structure bidirectional bus consisting of two wires : a serial data line (SDA) and a serial clock line (SCL) . Among the devices connected with these two wires, information is transmitted to one another. By recognizing the unique address of each device, it can operate as a transmitting or receiving device in accordance with the function of each device. Among these devices, the master/slave relation is established.

The I<sup>2</sup>C interface can connect two or more devices to the bus provided the upper limit of the bus capacitance does not exceed 400 pF. It is a full-fledged multi-master bus equipped with collision detection and communication adjustment procedures designed to avoid the destruction of data if two or more masters attempt to start data transfer simultaneously.

The communication adjustment procedure permits only one master to control the bus when two or more masters attempt to control the bus so that messages are not lost or the contents of messages are not changed. Multi-master means that multiple masters attempt to control the bus simultaneously without losing messages.

This I<sup>2</sup>C interface includes MCU standby mode wake-up function, and a CRC-8 calculator that performs automatic Packet Error Code (PEC) generation and verification.

### (1) Register configuration of I<sup>2</sup>C

I <sup>2</sup> C Bus Control Register (Lower)									
Address : 000080 <sub>H</sub>	7	6	5	4	3	2	1	0	↔ Bit number IBCRL
	—	—	—	—	RES	PECE	LBT	WUE	
Read/write	↔ —	↔ —	↔ —	↔ —	R/W	R/W	R/W	R/W	
Initial value	↔ —	↔ —	↔ —	↔ —	0	0	0	0	
I <sup>2</sup> C Bus Control Register (Upper)									
Address : 000081 <sub>H</sub>	15	14	13	12	11	10	9	8	↔ Bit number IBCRH
	BER	BEIE	SCC	MSS	ACK	GCAA	INTE	INT	
Read/write	↔ R/W	↔ R/W	↔ R/W	↔ R/W	↔ R/W	↔ R/W	↔ R/W	↔ R/W	
Initial value	↔ 0	↔ 0	↔ 0	↔ 0	↔ 0	↔ 0	↔ 0	↔ 0	
I <sup>2</sup> C Bus Status Register (Lower)									
Address : 000082 <sub>H</sub>	7	6	5	4	3	2	1	0	↔ Bit number IBSRL
	BB	RSC	AL	LRB	TRX	AAS	GCA	FBT	
Read/write	↔ R	↔ R	↔ R	↔ R	↔ R	↔ R	↔ R	↔ R	
Initial value	↔ 0	↔ 0	↔ 0	↔ 0	↔ 0	↔ 0	↔ 0	↔ 0	
I <sup>2</sup> C Bus Status Register (Upper)									
Address : 000083 <sub>H</sub>	15	14	13	12	11	10	9	8	↔ Bit number IBSRH
	—	—	PMATCH	WUF	TDR	TCR	MTR	STR	
Read/write	↔ —	↔ —	↔ R	↔ R/W	↔ R/W	↔ R/W	↔ R/W	↔ R/W	
Initial value	↔ —	↔ —	↔ 0	↔ 0	↔ 0	↔ 0	↔ 0	↔ 0	
I <sup>2</sup> C Data Register									
Address : 000084 <sub>H</sub>	7	6	5	4	3	2	1	0	↔ Bit number IDAR
	D7	D6	D5	D4	D3	D2	D1	D0	
Read/write	↔ R/W	↔ R/W	↔ R/W	↔ R/W	↔ R/W	↔ R/W	↔ R/W	↔ R/W	
Initial value	↔ X	↔ X	↔ X	↔ X	↔ X	↔ X	↔ X	↔ X	

(Continued)

# MB90370 Series

(Continued)

## I<sup>2</sup>C Address Register

	15	14	13	12	11	10	9	8	↔	Bit number
Address : 000085H	—	A6	A5	A4	A3	A2	A1	A0		IADR
Read/write	↔	—	R/W	R/W	R/W	R/W	R/W	R/W		
Initial value	↔	—	X	X	X	X	X	X		

## I<sup>2</sup>C Clock Control Register

	7	6	5	4	3	2	1	0	↔	Bit number
Address : 000086H	DMBP	—	EN	CS4	CS3	CS2	CS1	CS0		ICCR
Read/write	↔	R/W	—	R/W	R/W	R/W	R/W	R/W		
Initial value	↔	0	—	0	0	0	0	0		

## I<sup>2</sup>C Timeout Control Register

	15	14	13	12	11	10	9	8	↔	Bit number
Address : 000087H	—	AAC	—	TOE	EXT	TS2	TS1	TS0		ITCR
Read/write	↔	—	R/W	—	R/W	R/W	R/W	R/W		
Initial value	↔	—	0	—	0	0	0	0		

## I<sup>2</sup>C Timeout Clock Register

	7	6	5	4	3	2	1	0	↔	Bit number
Address : 000088H	C7	C6	C5	C4	C3	C2	C1	C0		ITOC
Read/write	↔	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
Initial value	↔	0	0	0	0	0	0	0		

## I<sup>2</sup>C Timeout Data Register

	15	14	13	12	11	10	9	8	↔	Bit number
Address : 000089H	D7	D6	D5	D4	D3	D2	D1	D0		ITOD
Read/write	↔	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
Initial value	↔	0	0	0	0	0	0	0		

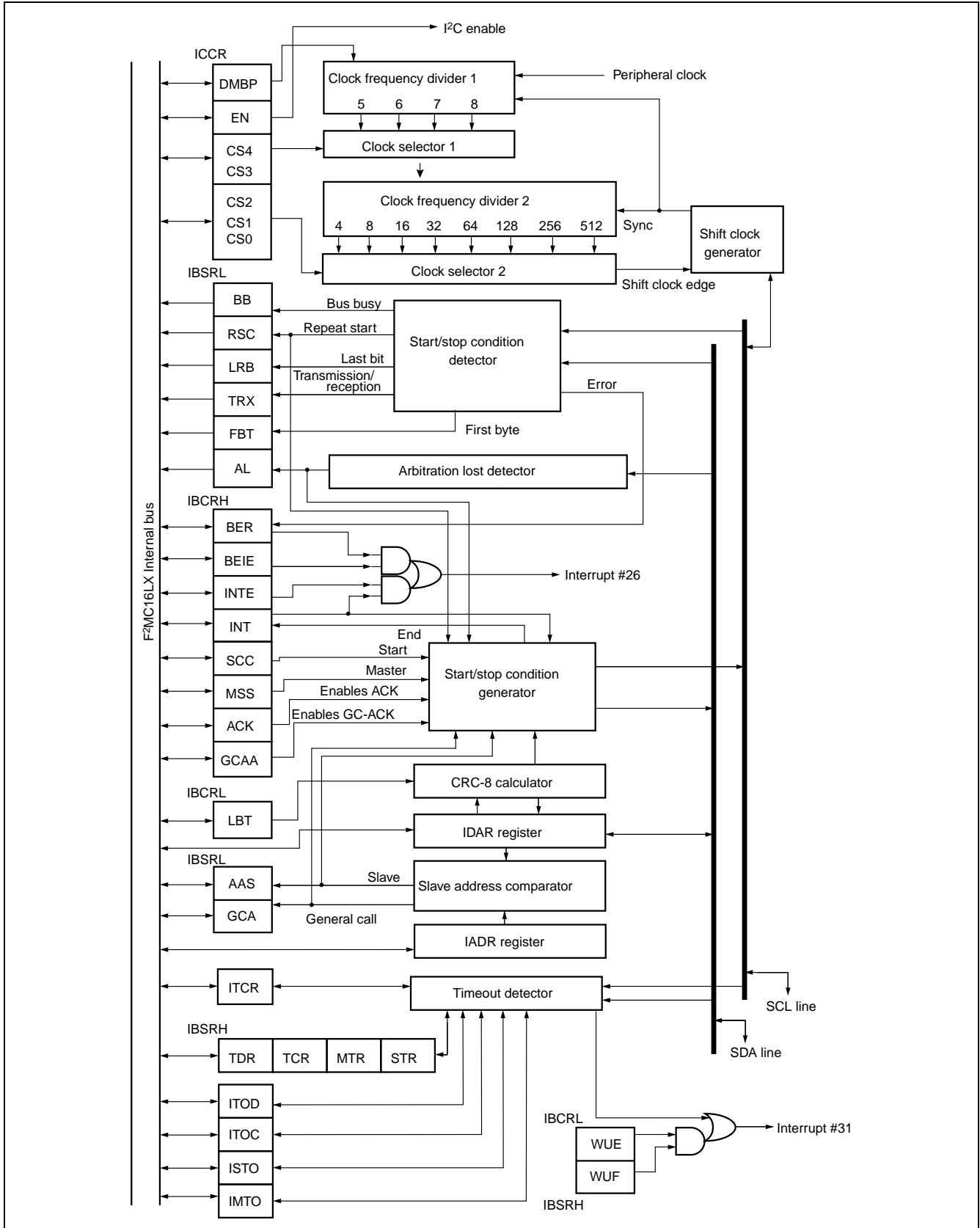
## I<sup>2</sup>C Slave Timeout Register

	7	6	5	4	3	2	1	0	↔	Bit number
Address : 00008AH	S6	S6	S5	S4	S3	S2	S1	S0		ISTO
Read/write	↔	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
Initial value	↔	0	0	0	0	0	0	0		

## I<sup>2</sup>C Master Timeout Register

	15	14	13	12	11	10	9	8	↔	Bit number
Address : 00008BH	M7	M6	M5	M4	M3	M2	M1	M0		IMTO
Read/write	↔	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
Initial value	↔	0	0	0	0	0	0	0		

## (2) Block diagram of I<sup>2</sup>C



# MB90370 Series

## 9. I<sup>2</sup>C

The Multi-address I<sup>2</sup>C (Inter IC Bus) interface is a simple structure bidirectional bus consisting of two wires : a serial data line (SDA) and a serial clock line (SCL) . Among the devices connected with these two wires, information is transmitted to one another. By recognizing the unique address of each device, it can operate as a transmitting or receiving device in accordance with the function of each device. Among these devices, the master/slave relation is established.

The Multi-address I<sup>2</sup>C interface can connect two or more devices to the bus provided the upper limit of the bus capacitance does not exceed 400 pF. It is a full-fledged multi-master bus equipped with collision detection and communication adjustment procedures designed to avoid the destruction of data if two or more masters attempt to start data transfer simultaneously. This macro provides 6 addresses to implement the multi-address function.

The communication adjustment procedure permits only one master to control the bus when two or more masters attempt to control the bus so that messages are not lost or the contents of messages are not changed. Multi-master means that multiple masters attempt to control the bus simultaneously without losing messages.

This Multi-address I<sup>2</sup>C interface includes MCU standby mode wake-up function, and a CRC-8 calculator that performs automatic Packet Error Code (PEC) generation and verification.

### (1) Register configuration of I<sup>2</sup>C

Multi-address I <sup>2</sup> C Bus Control Register (Lower)									
Address : 0000C0 <sub>H</sub>	7	6	5	4	3	2	1	0	↔ Bit number MBCRL
	—	—	—	—	RES	PECE	LBT	WUE	
Read/write	↔ —	↔ —	↔ —	↔ —	R/W	R/W	R/W	R/W	
Initial value	↔ —	↔ —	↔ —	↔ —	0	0	0	0	
Multi-address I <sup>2</sup> C Bus Control Register (Upper)									
Address : 0000C1 <sub>H</sub>	15	14	13	12	11	10	9	8	↔ Bit number MBCRH
	BER	BEIE	SCC	MSS	ACK	GCAA	INTE	INT	
Read/write	↔ R/W	↔ R/W	↔ R/W	↔ R/W	↔ R/W	↔ R/W	↔ R/W	↔ R/W	
Initial value	↔ 0	↔ 0	↔ 0	↔ 0	↔ 0	↔ 0	↔ 0	↔ 0	
Multi-address I <sup>2</sup> C Bus Status Register (Lower)									
Address : 0000C2 <sub>H</sub>	7	6	5	4	3	2	1	0	↔ Bit number MBSRL
	BB	RSC	AL	LRB	TRX	AAS	GCA	FBT	
Read/write	↔ R	↔ R	↔ R	↔ R	↔ R	↔ R	↔ R	↔ R	
Initial value	↔ 0	↔ 0	↔ 0	↔ 0	↔ 0	↔ 0	↔ 0	↔ 0	
Multi-address I <sup>2</sup> C Bus Status Register (Upper)									
Address : 0000C3 <sub>H</sub>	15	14	13	12	11	10	9	8	↔ Bit number MBSRH
	—	—	PMATCH	WUF	TDR	TCR	MTR	STR	
Read/write	↔ —	↔ —	↔ R	↔ R/W	↔ R/W	↔ R/W	↔ R/W	↔ R/W	
Initial value	↔ —	↔ —	↔ 0	↔ 0	↔ 0	↔ 0	↔ 0	↔ 0	
Multi-address I <sup>2</sup> C Data Register									
Address : 0000C4 <sub>H</sub>	7	6	5	4	3	2	1	0	↔ Bit number MDAR
	D7	D6	D5	D4	D3	D2	D1	D0	
Read/write	↔ R/W	↔ R/W	↔ R/W	↔ R/W	↔ R/W	↔ R/W	↔ R/W	↔ R/W	
Initial value	↔ X	↔ X	↔ X	↔ X	↔ X	↔ X	↔ X	↔ X	

(Continued)

## Multi-address I<sup>2</sup>C Alert Register

Address : 0000C5 <sub>H</sub>	15	14	13	12	11	10	9	8	Bit number MALR
	—	—	—	—	ARAE	ARO	ARF	AEN	
Read/write	⇒ —	⇒ —	⇒ —	⇒ —	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	
Initial value	⇒ —	⇒ —	⇒ —	⇒ —	⇒ 0	⇒ 0	⇒ 0	⇒ 0	

## Multi-address I<sup>2</sup>C Address Register 1/3/5

Address ch1 : 0000C6 <sub>H</sub>	7	6	5	4	3	2	1	0	Bit number MADR1/3/5
Address ch3 : 0000C8 <sub>H</sub>	—	A6	A5	A4	A3	A2	A1	A0	
Address ch5 : 0000CA <sub>H</sub>	—	A6	A5	A4	A3	A2	A1	A0	
Read/write	⇒ —	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	
Initial value	⇒ —	⇒ X	⇒ X	⇒ X	⇒ X	⇒ X	⇒ X	⇒ X	

## Multi-address I<sup>2</sup>C Address Register 2/4/6

Address ch2 : 0000C7 <sub>H</sub>	15	14	13	12	11	10	9	8	Bit number MADR2/4/6
Address ch4 : 0000C9 <sub>H</sub>	—	A6	A5	A4	A3	A2	A1	A0	
Address ch6 : 0000CB <sub>H</sub>	—	A6	A5	A4	A3	A2	A1	A0	
Read/write	⇒ —	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	
Initial value	⇒ —	⇒ X	⇒ X	⇒ X	⇒ X	⇒ X	⇒ X	⇒ X	

## Multi-address I<sup>2</sup>C Clock Control Register

Address : 0000CC <sub>H</sub>	7	6	5	4	3	2	1	0	Bit number MCCR
	DMBP	—	EN	CS4	CS3	CS2	CS1	CS0	
Read/write	⇒ R/W	⇒ —	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	
Initial value	⇒ 0	⇒ —	⇒ 0	⇒ 0	⇒ 0	⇒ 0	⇒ 0	⇒ 0	

## Multi-address I<sup>2</sup>C Timeout Control Register

Address : 0000CD <sub>H</sub>	15	14	13	12	11	10	9	8	Bit number MTCR
	—	AAC	—	TOE	EXT	TS2	TS1	TS0	
Read/write	⇒ —	⇒ R/W	⇒ —	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	
Initial value	⇒ —	⇒ 0	⇒ —	⇒ 0	⇒ 0	⇒ 0	⇒ 0	⇒ 0	

## Multi-address I<sup>2</sup>C Timeout Clock Register

Address : 0000CE <sub>H</sub>	7	6	5	4	3	2	1	0	Bit number MTOC
	C7	C6	C5	C4	C3	C2	C1	C0	
Read/write	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	
Initial value	⇒ 0	⇒ 0	⇒ 0	⇒ 0	⇒ 0	⇒ 0	⇒ 0	⇒ 0	

## Multi-address I<sup>2</sup>C Timeout Data Register

Address : 0000CF <sub>H</sub>	15	14	13	12	11	10	9	8	Bit number MTOD
	D7	D6	D5	D4	D3	D2	D1	D0	
Read/write	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	
Initial value	⇒ 0	⇒ 0	⇒ 0	⇒ 0	⇒ 0	⇒ 0	⇒ 0	⇒ 0	

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# MB90370 Series

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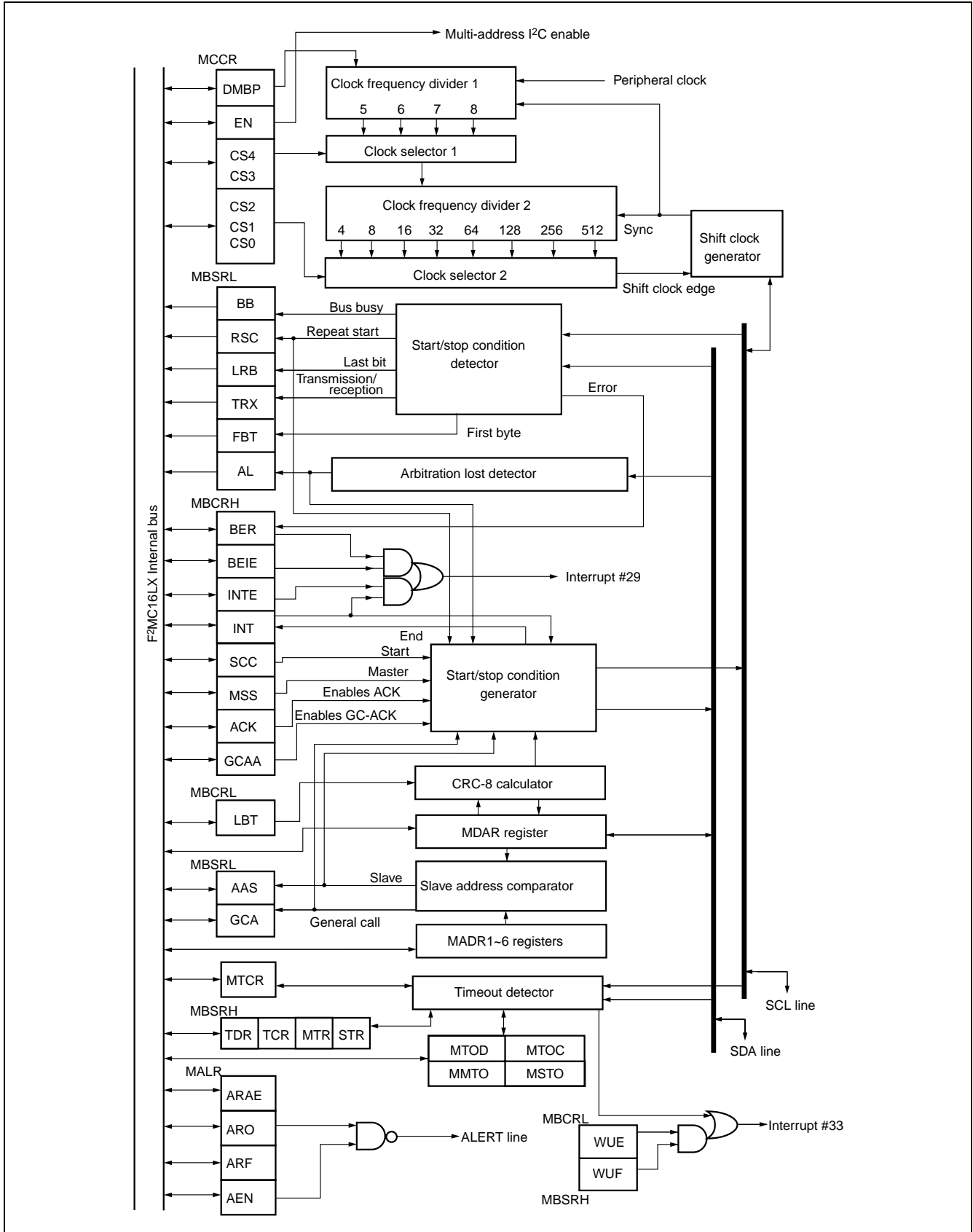
## Multi-address I<sup>2</sup>C Slave Timeout Register

	7	6	5	4	3	2	1	0	⇐ Bit number MSTO
Address : 0000D0 <sub>H</sub>	S6	S6	S5	S4	S3	S2	S1	S0	
Read/write	⇒ R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	⇒ 0	0	0	0	0	0	0	0	

## Multi-address I<sup>2</sup>C Master Timeout Register

	15	14	13	12	11	10	9	8	⇐ Bit number MMTO
Address : 0000D1 <sub>H</sub>	M7	M6	M5	M4	M3	M2	M1	M0	
Read/write	⇒ R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	⇒ 0	0	0	0	0	0	0	0	

## (2) Block diagram of MI<sup>2</sup>C



# MB90370 Series

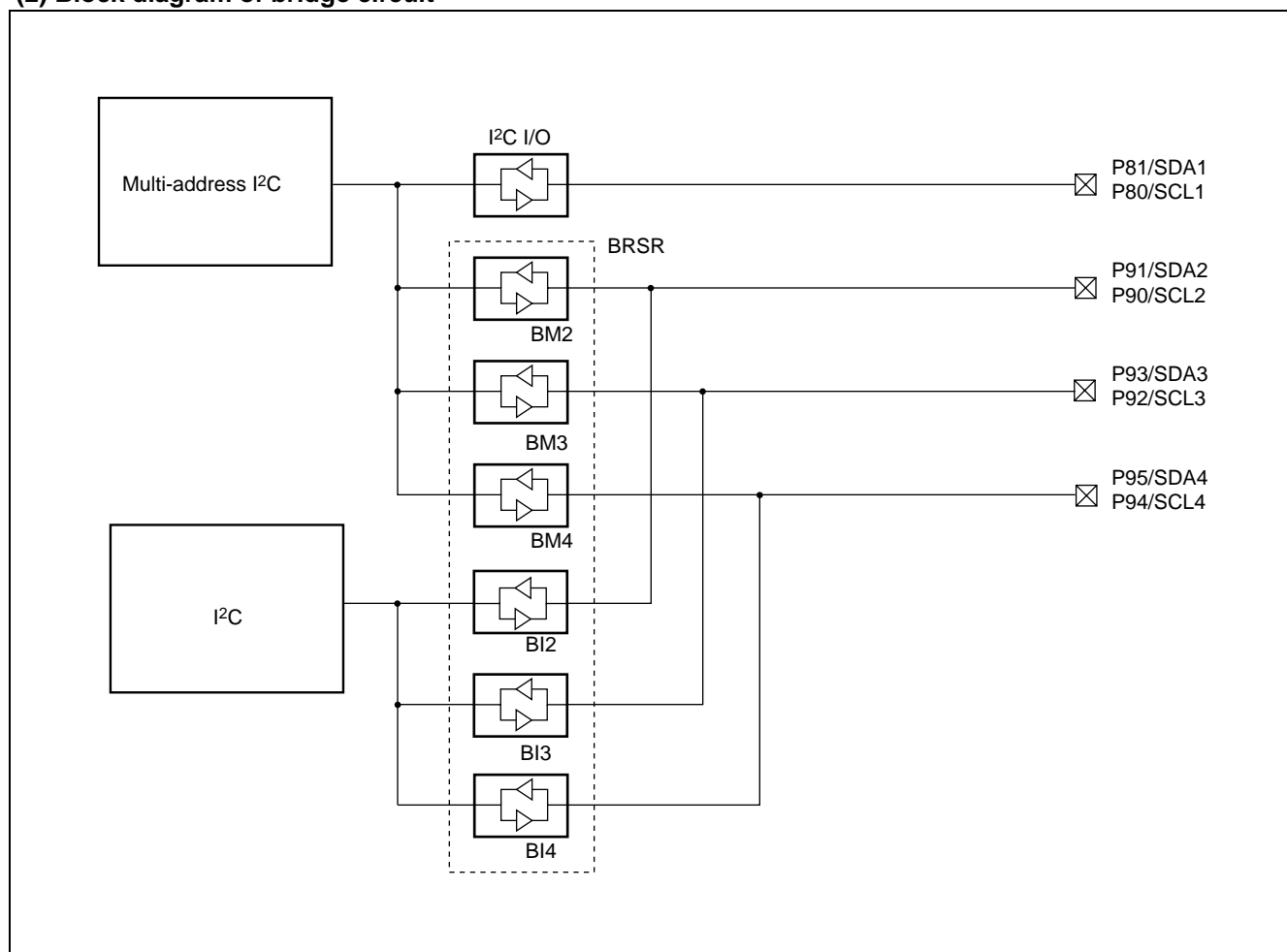
## 10. Bridge circuit

The bridge circuit can switch the I/O path of each port to I<sup>2</sup>C or Multi-address I<sup>2</sup>C.

### (1) Register configuration of bridge circuit

Bridge Circuit Selection Register								Bit number		
Address : 00002C <sub>H</sub>	7	6	5	4	3	2	1	0	↔	BRSR
	—	—	BM4	BI4	BM3	BI3	BM2	BI2		
Read/write	⇒	—	R/W	R/W	R/W	R/W	R/W	R/W		
Initial value	⇒	—	0	0	0	0	0	0		

### (2) Block diagram of bridge circuit



## 11. Comparator

This comparator circuit monitors voltage of up to three batteries and automatically controls electric discharge. Either parallel discharge or sequential discharge can be selected.

- **Parallel discharge control**  
In parallel discharge control, all batteries are allowed to discharge when power is not being supplied from the AC adapter.
- If power is being supplied from the AC adapter, the permission/prohibition of discharge for batteries is controlled by software.
- **Sequential discharge control**  
In sequential discharge control, the comparator controls discharge in a specified order, while monitoring intermittent interruption of power, voltage level, and mount/dismount of batteries, when power is not being supplied from the AC adapter.
- If power is being supplied from the AC adapter, the permission/prohibition of discharge for batteries is controlled by software.
- Up to three batteries can be controlled, and the order of discharge can be selected.
- The affect of intermittent interruption of power is automatically filtered.
- Mount/dismount of batteries is automatically detected and discharge is controlled.
- Battery voltage is monitored, and if battery voltage is below the specified voltage, a change over to the next battery is automatically done.

## (1) Register configuration of comparator

Comparator Control Register (Lower)									Bit number COCRL
Address : 0000D8H	7	6	5	4	3	2	1	0	
	—	—	BOF3	BOF2	BOF1	SPM2	SPM1	SPM0	
Read/write	⇒ —	⇒ —	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	
Initial value	⇒ —	⇒ —	⇒ 0	⇒ 0	⇒ 0	⇒ 0	⇒ 0	⇒ 0	
Comparator Control Register (Upper)									Bit number COCRH
Address : 0000D9H	15	14	13	12	11	10	9	8	
	SPL3	SPL2	SPL1	B3	B2	B1	DC2	DC1	
Read/write	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	
Initial value	⇒ 0	⇒ 0	⇒ 1	⇒ 1	⇒ 1	⇒ 1	⇒ 1	⇒ 1	
Comparator Status Register 1 (Lower)									Bit number COSRL1
Address : 0000DAH	7	6	5	4	3	2	1	0	
	COR8	COR7	COR6	COR5	COR4	COR3	COR2	COR1	
Read/write	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	
Initial value	⇒ 0	⇒ 0	⇒ 0	⇒ 0	⇒ 0	⇒ 0	⇒ 0	⇒ 0	
Comparator Status Register 1 (Upper)									Bit number COSRH1
Address : 0000DBH	15	14	13	12	11	10	9	8	
	—	—	SWR3	SWR2	SWR1	VAR3	VAR2	VAR1	
Read/write	⇒ —	⇒ —	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	
Initial value	⇒ —	⇒ —	⇒ 0	⇒ 0	⇒ 0	⇒ 0	⇒ 0	⇒ 0	
Comparator Interrupt Control Register (Lower)									Bit number CICRL
Address : 0000DCH	7	6	5	4	3	2	1	0	
	CEN8	CEN7	CEN6	CEN5	CEN4	CEN3	CEN2	CEN1	
Read/write	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	
Initial value	⇒ 0	⇒ 0	⇒ 0	⇒ 0	⇒ 0	⇒ 0	⇒ 0	⇒ 0	

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## Comparator Interrupt Control Register (Upper)

	15	14	13	12	11	10	9	8	Bit number
Address : 0000DD <sub>H</sub>	—	—	SEN3	SEN2	SEN1	VEN3	VEN2	VEN1	CICRH
Read/write	⇒ —	⇒ —	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	
Initial value	⇒ —	⇒ —	⇒ 0	⇒ 0	⇒ 0	⇒ 0	⇒ 0	⇒ 0	

## Comparator Status Register 2 (Lower)

	7	6	5	4	3	2	1	0	Bit number
Address : 0000DE <sub>H</sub>	COS8	COS7	COS6	COS5	COS4	COS3	COS2	COS1	COSRL2
Read/write	⇒ R	⇒ R	⇒ R	⇒ R	⇒ R	⇒ R	⇒ R	⇒ R	
Initial value	⇒ X	⇒ X	⇒ X	⇒ X	⇒ X	⇒ X	⇒ X	⇒ X	

## Comparator Status Register 2 (Upper)

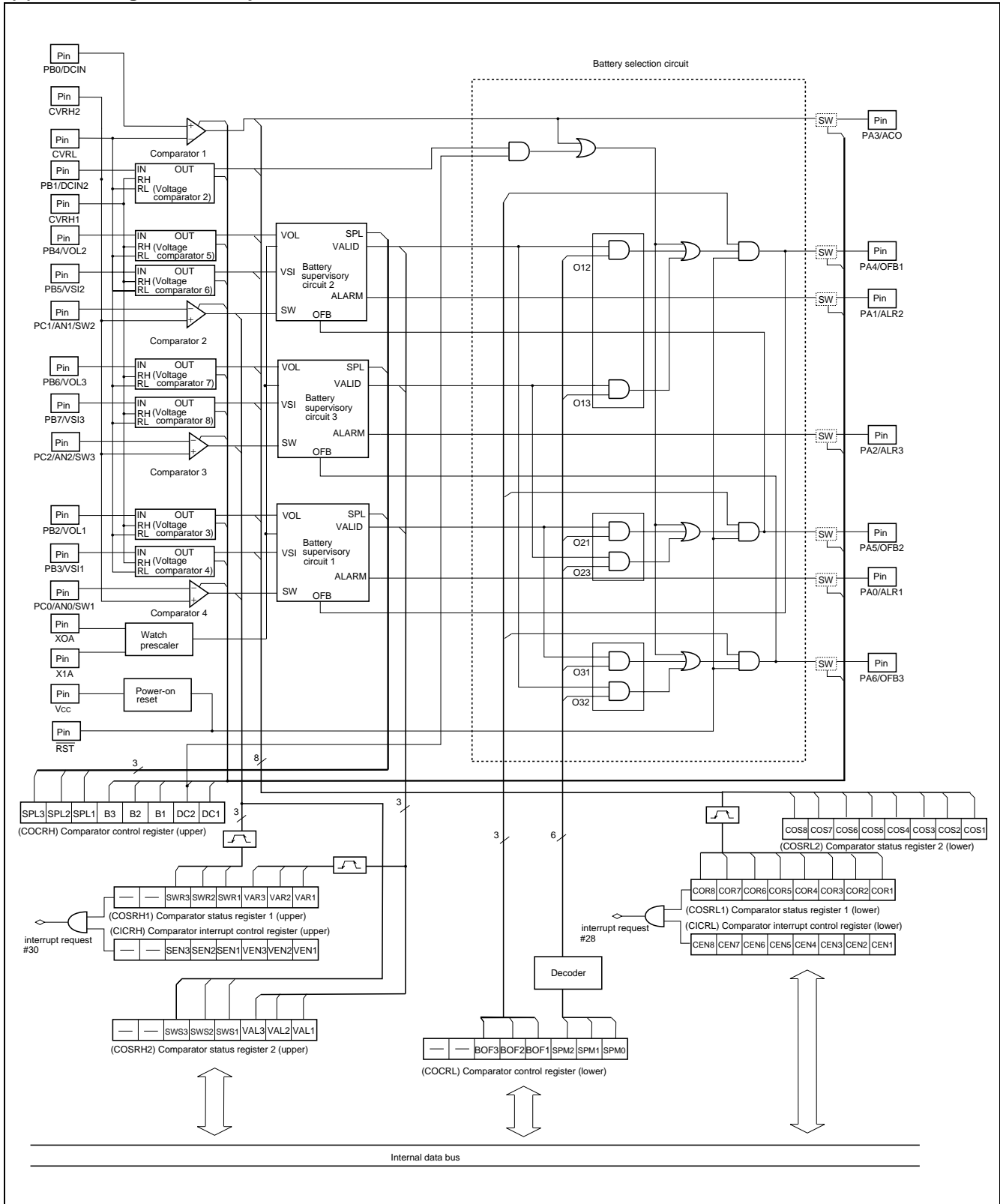
	15	14	13	12	11	10	9	8	Bit number
Address : 0000DF <sub>H</sub>	—	—	SWS3	SWS2	SWS1	VAL3	VAL2	VAL1	COSRH2
Read/write	⇒ —	⇒ —	⇒ R	⇒ R	⇒ R	⇒ R	⇒ R	⇒ R	
Initial value	⇒ —	⇒ —	⇒ X	⇒ X	⇒ X	⇒ X	⇒ X	⇒ X	

## Comparator Input Enable Register

	7	6	5	4	3	2	1	0	Bit number
Address : 0000E0 <sub>H</sub>	—	—	—	BIE3	BIE2	BIE1	DIE2	DIE1	CIER
Read/write	⇒ —	⇒ —	⇒ —	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	
Initial value	⇒ —	⇒ —	⇒ —	⇒ 1	⇒ 1	⇒ 1	⇒ 1	⇒ 1	

# MB90370 Series

## (2) Block diagram of comparator



## 12. UART (× 3)

The UART (Universal Asynchronous Receiver Transmitter) is a serial I/O port for asynchronous (start-stop) communication or clock-synchronous communication.

The UART has the following features :

- Full-duplex double buffering
- Capable of asynchronous (start-stop bit) and CLK-synchronous communications
- Support for the multiprocessor mode
- Various method of baud rate generation :
  - External clock input possible
  - Internal clock (a clock supplied from 16-bit reload timer can be used)
  - Embedded dedicated baud rate generator

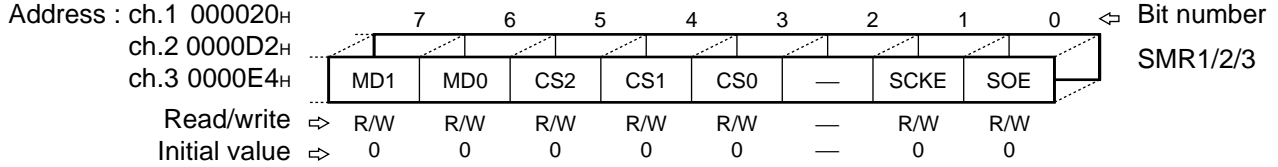
Operation	Baud rate
Asynchronous	76923 / 38461 / 19230 / 9615 / 500K / 250K bps
CLK synchronous	16M / 8M / 4M / 2M / 1M / 500K bps

- Error detection functions (parity, framing, overrun)
- NRZ (Non Return to Zero) signal format
- Interrupt request :
  - Receive interrupt (receive complete, receive error detection)
  - Transmit interrupt (transmission complete)
  - Transmit / receive conforms to extended intelligent I/O service (EI<sup>2</sup>OS)

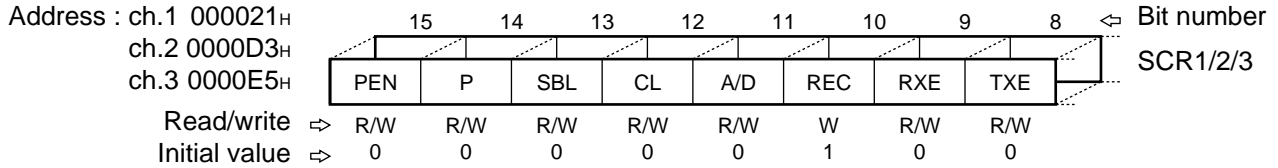
# MB90370 Series

## (1) Register configuration of UART

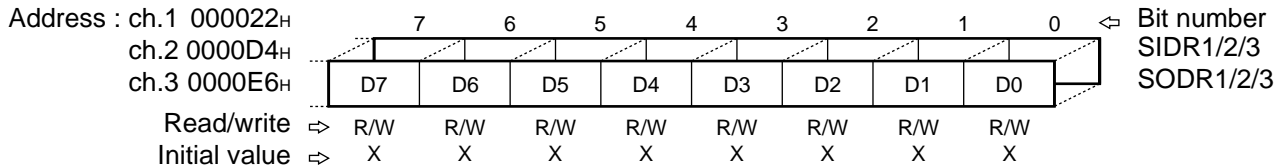
### Serial Mode Register



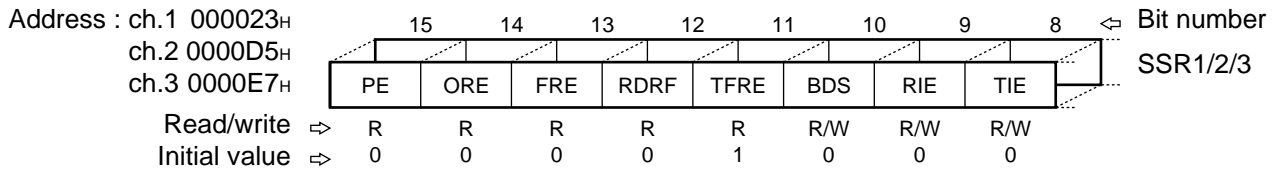
### Serial Control Register



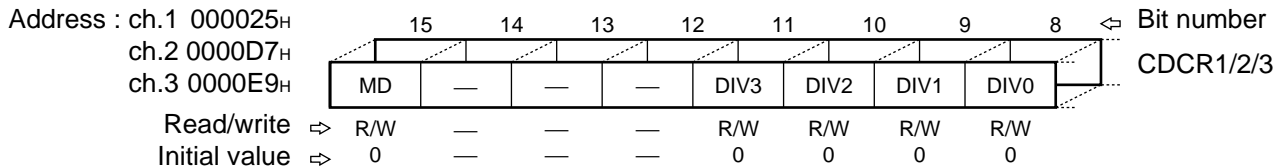
### UART Input Data Register / Output Data Register



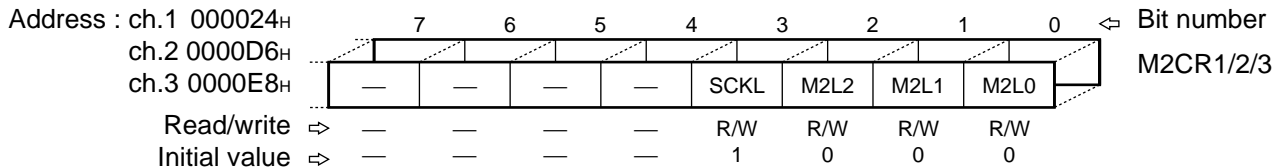
### UART Status Register



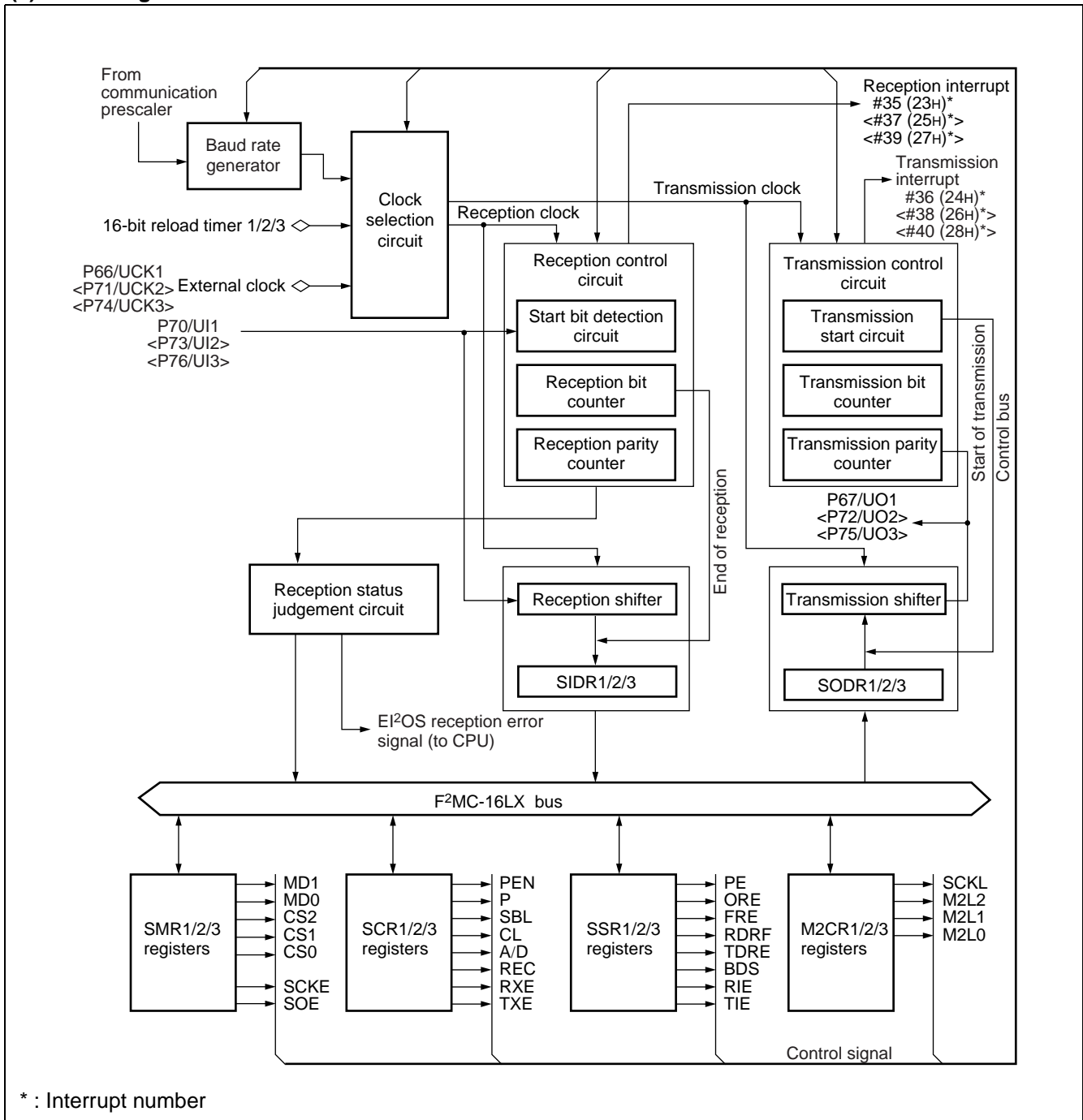
### Clock Division Control Register



### Mode 2 Control Register



## (2) Block diagram of UART



## 13. LCD controller/driver

The LCD (Liquid Crystal Display) controller/driver function displays the contents of a display data memory directly to the LCD panel by segment and common outputs.

- Up to nine segment outputs (SEG0 to SEG8) and four common outputs (COM0 to COM3) may be used.
- Built-in display RAM.
- Three selectable duty ratios (1/2, 1/3, and 1/4) . However, not all duty ratios are available with all bias settings.
- Either the main or sub-clock can be selected as the drive clock.
- LCD can be driven directly.

Table below shows the duty ratios available with each bias setting.

Part number	Bias	1/2 duty ratio	1/3 duty ratio	1/4 duty ratio
MB90370 series	1/2 bias	○	X	X
	1/3 bias	X	○	○

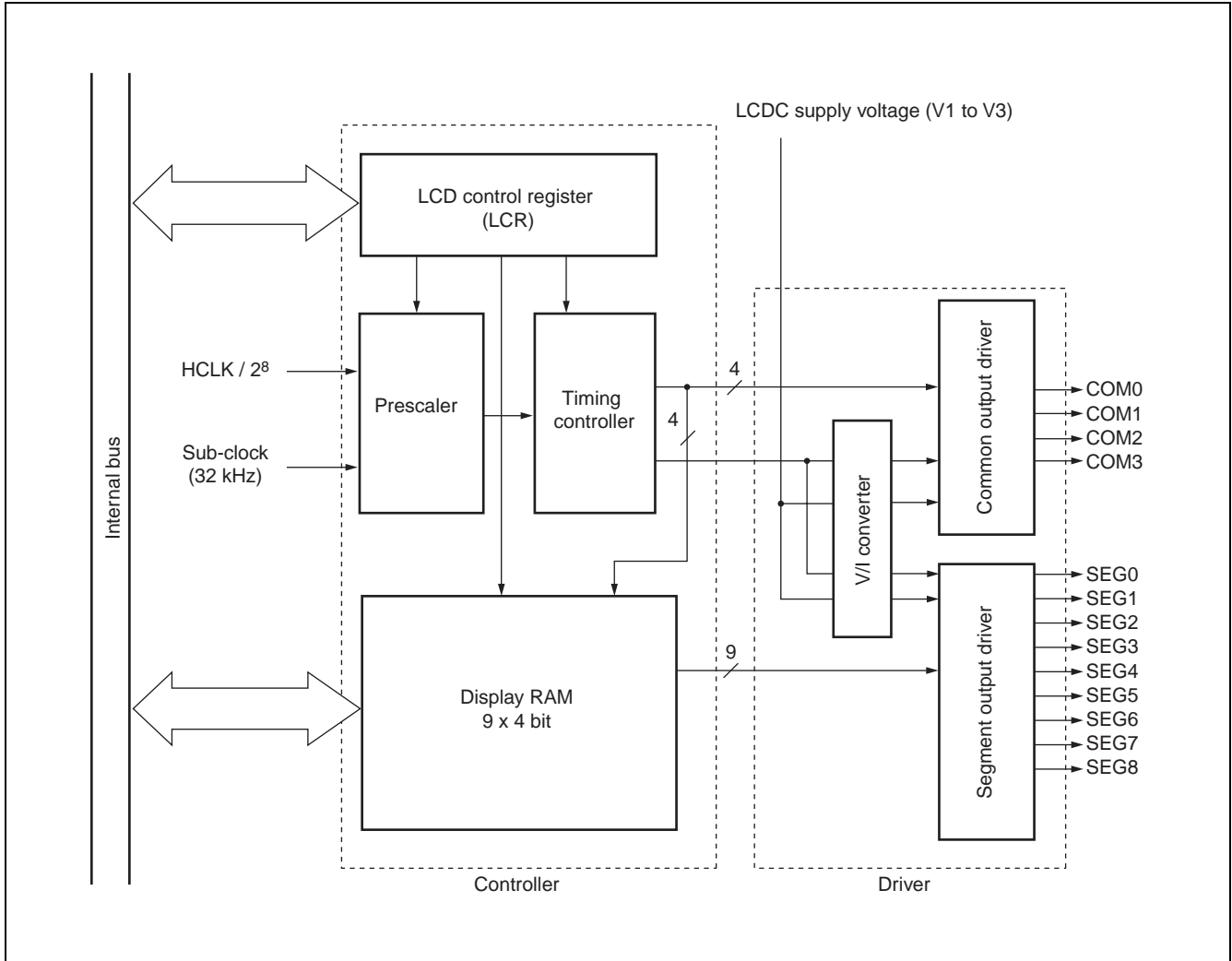
○ : Recommended mode

X : Do not use

### (1) Register configuration of LCD

LCD Control Register (Upper)								Bit number LCRH	
Address : 0000EF <sub>H</sub>	15	14	13	12	11	10	9		8
	SS4	VS	CS1	CS0	SS3	SS2	SS1		SS0
Read/write	⇒ R/W	R/W	R/W	R/W	R/W	R/W	R/W		R/W
Initial value	⇒ 0	0	0	0	0	0	0	0	
LCD Control Register (Lower)								Bit number LCRL	
Address : 0000EE <sub>H</sub>	7	6	5	4	3	2	1		0
	CSS	LCEN	VSEL	BK	MS1	MS0	FP1		FP0
Read/write	⇒ R/W	R/W	R/W	R/W	R/W	R/W	R/W		R/W
Initial value	⇒ 0	0	0	1	0	0	0	0	

## (2) Block diagram of LCD



# MB90370 Series

## 14. A/D converter

The A/D (Analog to Digital) converter converts the analog voltage input to an analog input pin (input voltage) to a digital value.

The converter has the following features :

- The minimum conversion time is 6.13  $\mu$ s (for a machine clock of 16 MHz; includes the sampling time) .
- The minimum sampling time is 3.75  $\mu$ s (for a machine clock of 16 MHz) .
- The converter uses the RC-type successive approximation conversion method with a sample and hold circuit.
- A resolution of 10 bits or 8 bits can be selected.
- Up to twelve channels for analog input pins can be selected by a program.
- Various conversion modes :
  - Single conversion mode : Selectively convert one channel.
  - Scan conversion mode : Continuously convert multiple channels. Maximum of 12 selectable channels.
  - Continuous conversion mode : Repeatedly convert specified channels.
  - Stop conversion mode : Convert one channel then halt until the next activation. (Enables synchronization of the conversion start timing.)
- At the end of A/D conversion, an interrupt request can be generated and EI<sup>2</sup>OS can be activated.
- In the interrupt-enabled state, the conversion data protection function prevents any part of the data from being lost through continuous conversion.
- The conversion can be activated by software, 16-bit reload timer 4 (rise edge) and ADTG.

### (1) Register configuration of A/D converter

Analog Input Enable Register 2									
Address : 00002B <sub>H</sub>	15	14	13	12	11	10	9	8	⇐ Bit number ADER2
	—	—	—	—	ADE11	ADE10	ADE9	ADE8	
Read/write	⇐ —	⇐ —	⇐ —	⇐ —	R/W	R/W	R/W	R/W	
Initial value	⇐ —	⇐ —	⇐ —	⇐ —	1	1	1	1	
Analog Input Enable Register 1									
Address : 00002A <sub>H</sub>	7	6	5	4	3	2	1	0	⇐ Bit number ADER1
	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0	
Read/write	⇐ R/W	⇐ R/W	⇐ R/W	⇐ R/W	⇐ R/W	⇐ R/W	⇐ R/W	⇐ R/W	
Initial value	⇐ 1	⇐ 1	⇐ 1	⇐ 1	⇐ 1	⇐ 1	⇐ 1	⇐ 1	
A/D Control Status Register 1									
Address : 000031 <sub>H</sub>	15	14	13	12	11	10	9	8	⇐ Bit number ADCS1
	BUSY	INT	INTE	PAUS	STS1	STS0	STRT	RESV	
Read/write	⇐ R/W	⇐ R/W	⇐ R/W	⇐ R/W	⇐ R/W	⇐ R/W	⇐ W	⇐ R/W	
Initial value	⇐ 0	⇐ 0	⇐ 0	⇐ 0	⇐ 0	⇐ 0	⇐ 0	⇐ 0	
A/D Control Status Register 0									
Address : 000030 <sub>H</sub>	7	6	5	4	3	2	1	0	⇐ Bit number ADCS0
	MD1	MD0	—	—	—	—	—	—	
Read/write	⇐ R/W	⇐ R/W	⇐ —	⇐ —	⇐ —	⇐ —	⇐ —	⇐ —	
Initial value	⇐ 0	⇐ 0	⇐ —	⇐ —	⇐ —	⇐ —	⇐ —	⇐ —	

(Continued)



## 15. D/A converter

The D/A (Digital to Analog) converter is used to generate an analog output from an 8-bit digital input. By setting the enable bit in the D/A control register (DACR) to 1, it will enable the corresponding D/A output channel. Hence, setting this bit to 0 will disable that channel.

If D/A output is disabled, the analog switch inserted to the output of each D/A converter channel in series is turned off. In the D/A converter, the bit is cleared to 0 and the direct-current path is shut off. The above is also true in the stop mode.

The output voltage of the D/A converter ranges from 0 V to  $255/256 \times AV_{CC}$ .

The D/A converter output does not have the internal buffer amplifier. The analog switch ( $= 100 \Omega$ ) is inserted to the output in series. To apply load to the output externally, estimate a sufficient stabilization time.

Table below lists the theoretical values of output voltage of the D/A converter.

Value written to DA07 to DA00 and DA17 to DA10	Theoretical value of output voltage
00 <sub>H</sub>	$0/256 \times AV_{CC} (= 0 \text{ V})$
01 <sub>H</sub>	$1/256 \times AV_{CC}$
02 <sub>H</sub>	$2/256 \times AV_{CC}$
:	:
FD <sub>H</sub>	$253/256 \times AV_{CC}$
FE <sub>H</sub>	$254/256 \times AV_{CC}$
FF <sub>H</sub>	$255/256 \times AV_{CC}$

## (1) Register configuration of D/A converter

D/A converter register 1

Address : 00005B <sub>H</sub>	15	14	13	12	11	10	9	8	Bit number DAT1
	DA17	DA16	DA15	DA14	DA13	DA12	DA11	DA10	
Read/write	↔ R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	↔ X	X	X	X	X	X	X	X	

D/A converter register 0

Address : 00005A <sub>H</sub>	7	6	5	4	3	2	1	0	Bit number DAT0
	DA07	DA06	DA05	DA04	DA03	DA02	DA01	DA00	
Read/write	↔ R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	↔ X	X	X	X	X	X	X	X	

D/A control register 1

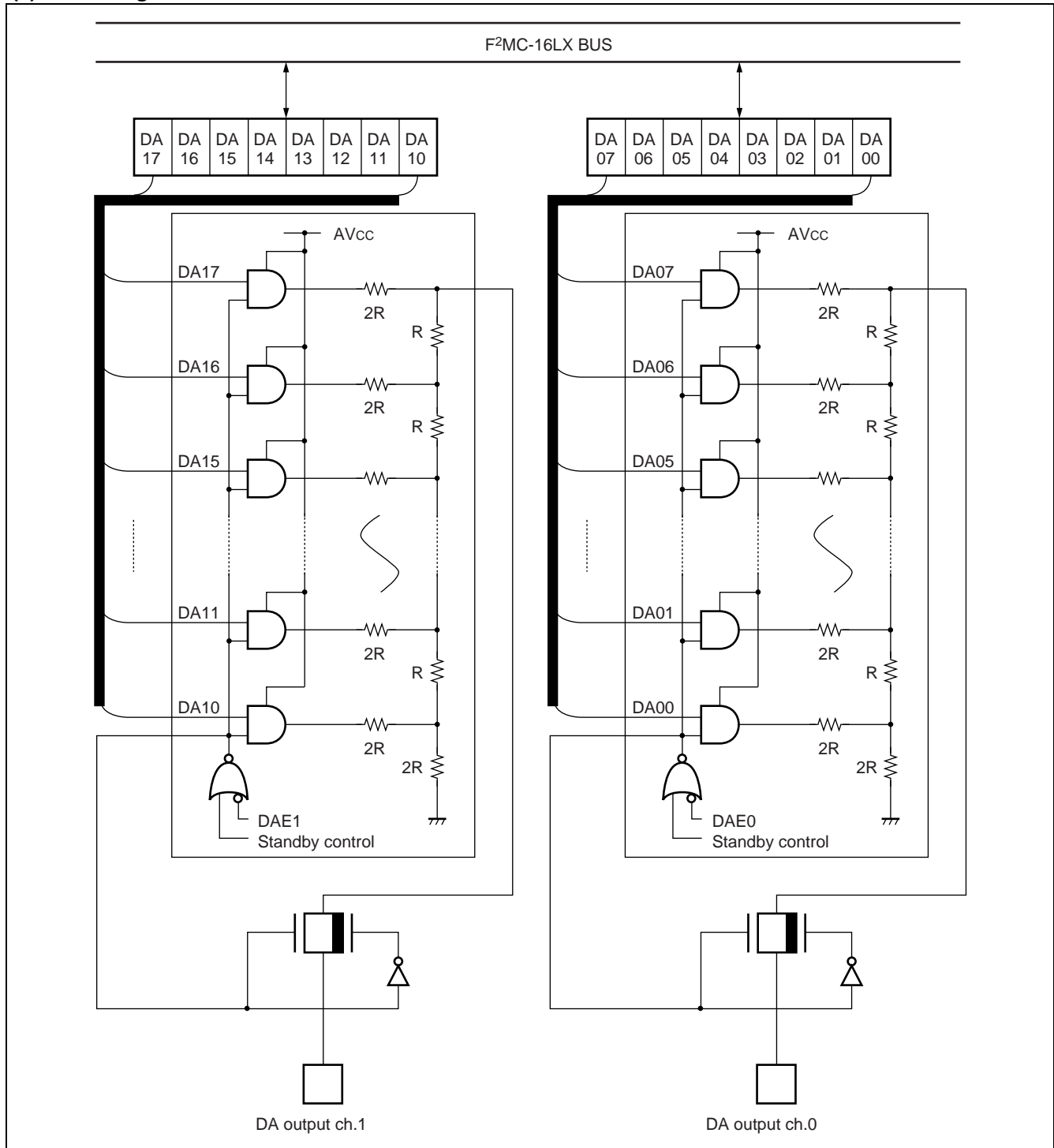
Address : 00005D <sub>H</sub>	15	14	13	12	11	10	9	8	Bit number DACR1
	—	—	—	—	—	—	—	DAE1	
Read/write	↔ —	—	—	—	—	—	—	R/W	
Initial value	↔ —	—	—	—	—	—	—	0	

D/A control register 0

Address : 00005C <sub>H</sub>	7	6	5	4	3	2	1	0	Bit number DACR0
	—	—	—	—	—	—	—	DAE0	
Read/write	↔ —	—	—	—	—	—	—	R/W	
Initial value	↔ —	—	—	—	—	—	—	0	

# MB90370 Series

(2) Block diagram of D/A converter



## 16. LPC interface

The LPC (Low Pin Count) interface consists of an LPC bus interface, universal parallel interface (UPI × 4 channels) , gate address A20 function and LPC data buffer array. By using the LPC bus interface and UPI, data can be exchanged with an external host CPU synchronously via an external LPC bus.

- **LPC bus interface**

The LPC bus interface provides direct access of host CPU to UPI.

- It supports I/O read and I/O write cycle only. Other cycle types will be ignored.
- It supports LPC clock running at 33 MHz.

- **Universal parallel interface, UPI × 4 channels**

The UPI is used to exchange parallel data to serial data in LPC bus with host CPU.

- An 8-bit data will be transmitted or received.
- A buffer function is available for independent input and output.
- The I/O buffer status can be output externally through LPC bus interface.

- **Gate address A20 function for UPI channel 0**

The GA20 (Gate Address A20) is intended to implement the memory management in a PC architecture. This allows the access to the extended memory needed by the operating system. On-chip logic is provided to speed up the generation of GA20.

- **Data buffer array**

The data buffer array is consisted of 32 bytes UP data register and 16 bytes DOWN data register to speed up the data transfer between MCU and external host through LPC bus.

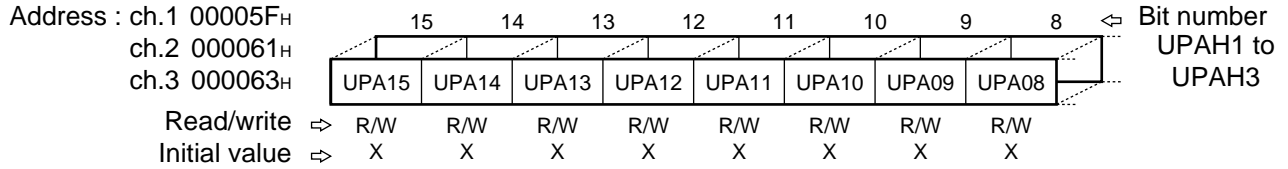
### (1) Register configuration of LPC bus interface register

LPC Control Register								Bit number	
Address : 00006E <sub>H</sub>	7	6	5	4	3	2	1	0	⇐ LCR
	—	—	—	—	—	LRF	LRIE	LPE	
Read/write	⇒ —	⇒ —	⇒ —	⇒ —	⇒ —	R/W	R/W	R/W	
Initial value	⇒ —	⇒ —	⇒ —	⇒ —	⇒ —	0	0	0	

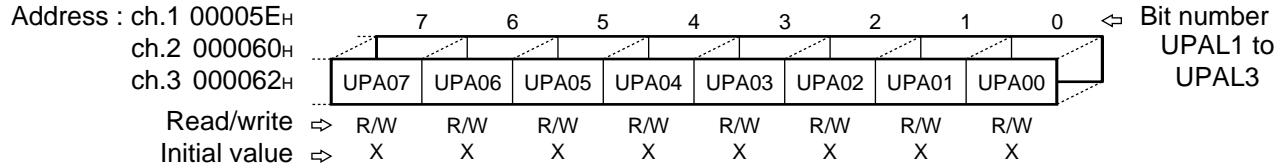
# MB90370 Series

## (2) Register configuration of UPI registers

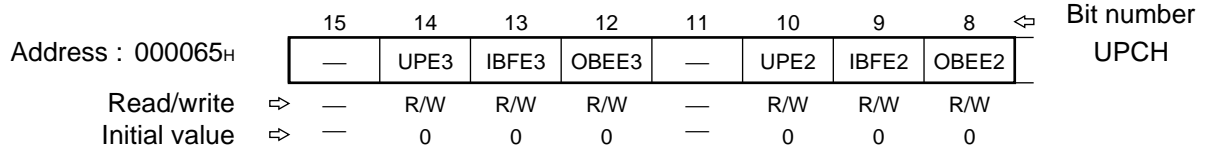
### UPI Address Register (Upper)



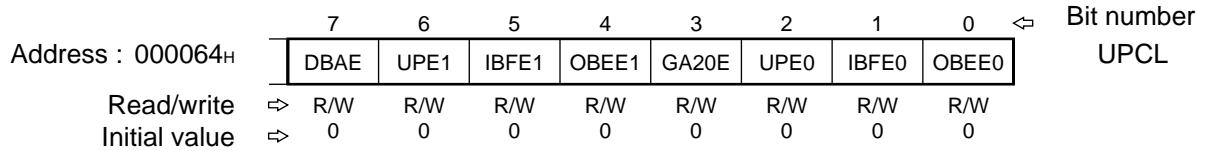
### UPI Address Register (Lower)



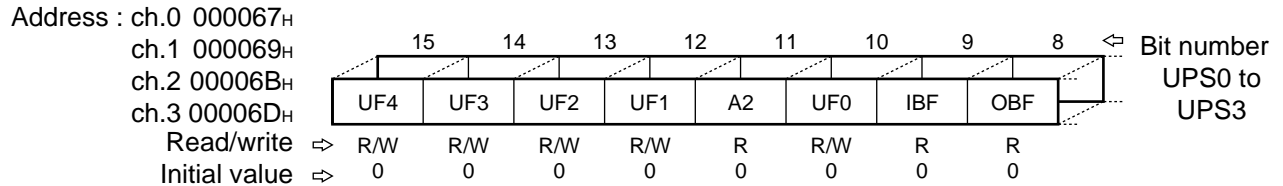
### UPI Control Register (Upper)



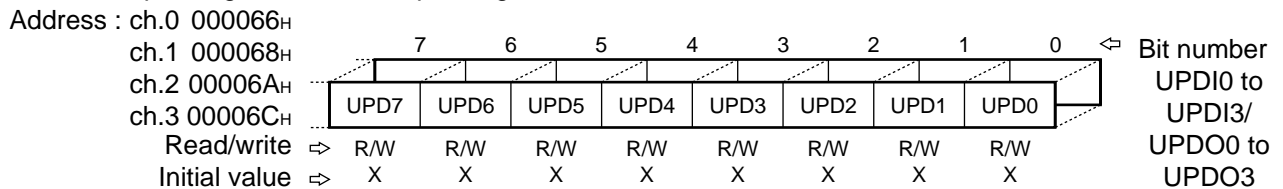
### UPI Control Register (Lower)



### UPI Status Register



### UPI Data Input Register / Data Output Register



## (3) Register configuration of LPC data buffer registers

### Data Buffer Array Address Register (Upper)

Address : 003FF1H	15	14	13	12	11	10	9	8	⇐ Bit number DBAAH
	DA15	DA14	DA13	DA12	DA11	DA10	DA09	DA08	
Read/write	⇨ R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	⇨ X	X	X	X	X	X	X	X	

### Data Buffer Array Address Register (Lower)

Address : 003FF0H	7	6	5	4	3	2	1	0	⇐ Bit number DBAAL
	DA07	DA06	DA05	DA04	DA03	DA02	DA01	DA00	
Read/write	⇨ R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	⇨ X	X	X	X	X	X	X	X	

### UP Data Register (upper)

Address : ch.0 003FC1H ch.1 003FC3H to ch.F 003FDFH	15	14	13	12	11	10	9	8	⇐ Bit number UDRH0 to UDRHF
	UP15	UP14	UP13	UP12	UP11	UP10	UP09	UP08	
Read/write	⇨ R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	⇨ X	X	X	X	X	X	X	X	

### UP Data Register (lower)

Address : ch.0 003FC0H ch.1 003FC2H to ch.F 003FDEH	7	6	5	4	3	2	1	0	⇐ Bit number UDRL0 to UDRLF
	UP07	UP06	UP05	UP04	UP03	UP02	UP01	UP00	
Read/write	⇨ R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	⇨ X	X	X	X	X	X	X	X	

### DOWN Data Register (upper)

Address : ch.0 003FE1H ch.1 003FE3H to ch.7 003FEFH	15	14	13	12	11	10	9	8	⇐ Bit number DNDH0 to DNDH7
	DN15	DN14	DN13	DN12	DN11	DN10	DN09	DN08	
Read/write	⇨ R	R	R	R	R	R	R	R	
Initial value	⇨ X	X	X	X	X	X	X	X	

### DOWN Data Register (lower)

Address : ch.0 003FE0H ch.1 003FE2H to ch.7 003FEEH	7	6	5	4	3	2	1	0	⇐ Bit number DNDL0 to DNDL7
	DN07	DN06	DN05	DN04	DN03	DN02	DN01	DN00	
Read/write	⇨ R	R	R	R	R	R	R	R	
Initial value	⇨ X	X	X	X	X	X	X	X	

(Continued)

# MB90370 Series

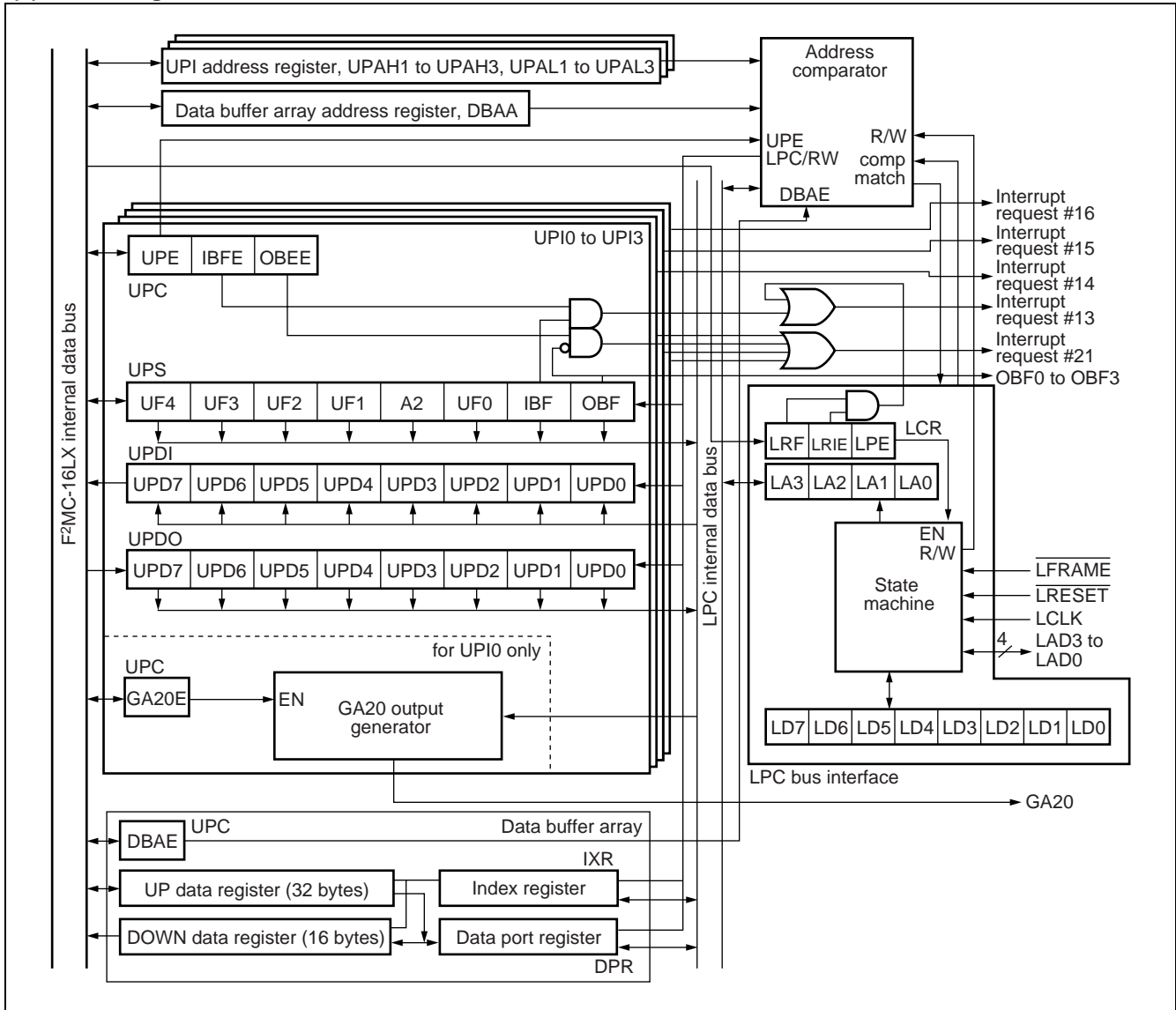
(Continued)

Index Register								Bit number	
Address :	7	6	5	4	3	2	1	0	IXR
—	—	—	IX05	IX04	IX03	IX02	IX01	IX00	
Read/write	⇒ —	⇒ —	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	
Initial value	⇒ —	⇒ —	⇒ 0	⇒ 0	⇒ 0	⇒ 0	⇒ 0	⇒ 0	

Data Port Register								Bit number	
Address :	7	6	5	4	3	2	1	0	DPR
—	DP07	DP06	DP05	DP04	DP03	DP02	DP01	DP00	
Read/write	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	
Initial value	⇒ X	⇒ X	⇒ X	⇒ X	⇒ X	⇒ X	⇒ X	⇒ X	

## (4) Block diagram of LPC interface



## 17. Serial IRQ controller

The serial IRQ controller consists of a 6-channel serial IRQ control circuit and an LPC clock monitor / control circuit. By using this serial IRQ controller, host interrupt requests can be transferred serially through a single signal wire (SERIRQ) , synchronized with the LPC clock.

### 6-channel serial IRQ control circuit

- The 6-channel serial IRQ control circuit consists of a serial interrupt control register (SICR) , 4 serial interrupt frame number registers (SIFR1 to SIFR4) , a protocol state machine and a serial interrupt data latch and output control.
- For channel 0A, 0B and 1 to 3, if SICR : OBE bit (OBF controlled enable bit) = 0, then serial IRQ can be controlled by software setting of SICR : IRR bit. If SICR : OBE bit = 1, then software control is disabled and serial IRQ is controlled by OBF flag (Output buffer full flag) from LPC UPI0 to UPI3.
- For channel 4, serial IRQ can be controlled by software setting of SICR : IRR bit.
- For channel 0A and 0B, additional enable bit (SICR : EN0A/0B bit) can be used to latch and keep the OBF0 or IRR0A/0B bit status.
- The serial interrupt data latch transfers serial IRQs serially according to their frame number. The frame number for channel 0A is fixed to "IRQ1", for channel 0B is fixed to "IRQ12", and the frame number for channel 1 to channel 4 are software programmable (IRQ1 to IRQ15, and IRQ21 to IRQ31) by setting the SIFR1 to SIFR4.
- By monitoring the SERIRQ and the LPC clock pin, the protocol state machine can detect the START frame condition. Then it starts counting the DATA frame and transfers its serial IRQs through SERIRQ. Finally it can switch to continuous/quiet mode operation by determine the STOP frame condition.
- The serial interrupt output control support both continuous and quiet mode operation. In continuous mode operation, only the host can initiate the serial IRQs transfer; In quiet mode operation, both the host and slave (e.g. the serial IRQ controller) can initiate the serial IRQs transfer.

### LPC clock monitor / control circuit

- The LPC clock monitor / control circuit consists of a clock-run monitor / control circuit. By monitoring the clock-run pin ( $\overline{\text{CLKRUN}}$ ) , the clock monitor / control circuit can determine whether the host has stopped LPC clock in quiet mode operation or not. If LPC clock is stopped and the controller wants to initiate the serial IRQs transfer, then it can request the host to restart the LPC clock by controlling the  $\overline{\text{CLKRUN}}$  pin.

## (1) Register configuration of serial IRQ controller

### Serial Interrupt Control Register (Lower)

Address : 000032H	7	6	5	4	3	2	1	0	⇐ Bit number SICRL
	EN0B	EN0A	IRR4	IRR3	IRR2	IRR1	IRR0B	IRR0A	
Read/write	⇔ R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	⇔ 0	0	0	0	0	0	0	0	

### Serial Interrupt Control Register (Upper)

Address : 000033H	15	14	13	12	11	10	9	8	⇐ Bit number SICRH
	IRQEN	RSEN	BUSY	OBE3	OBE2	OBE1	OBE0B	OBE0A	
Read/write	⇔ R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	
Initial value	⇔ 0	0	0	0	0	0	0	0	

### Serial Interrupt Frame Number Register 1

Address : 000034H	7	6	5	4	3	2	1	0	⇐ Bit number SIFR1
	—	—	LV1	FR14	FR13	FR12	FR11	FR10	
Read/write	⇔ —	—	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	⇔ —	—	0	0	0	0	0	0	

### Serial Interrupt Frame Number Register 2

Address : 000035H	15	14	13	12	11	10	9	8	⇐ Bit number SIFR2
	—	—	LV2	FR24	FR23	FR22	FR21	FR20	
Read/write	⇔ —	—	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	⇔ —	—	0	0	0	0	0	0	

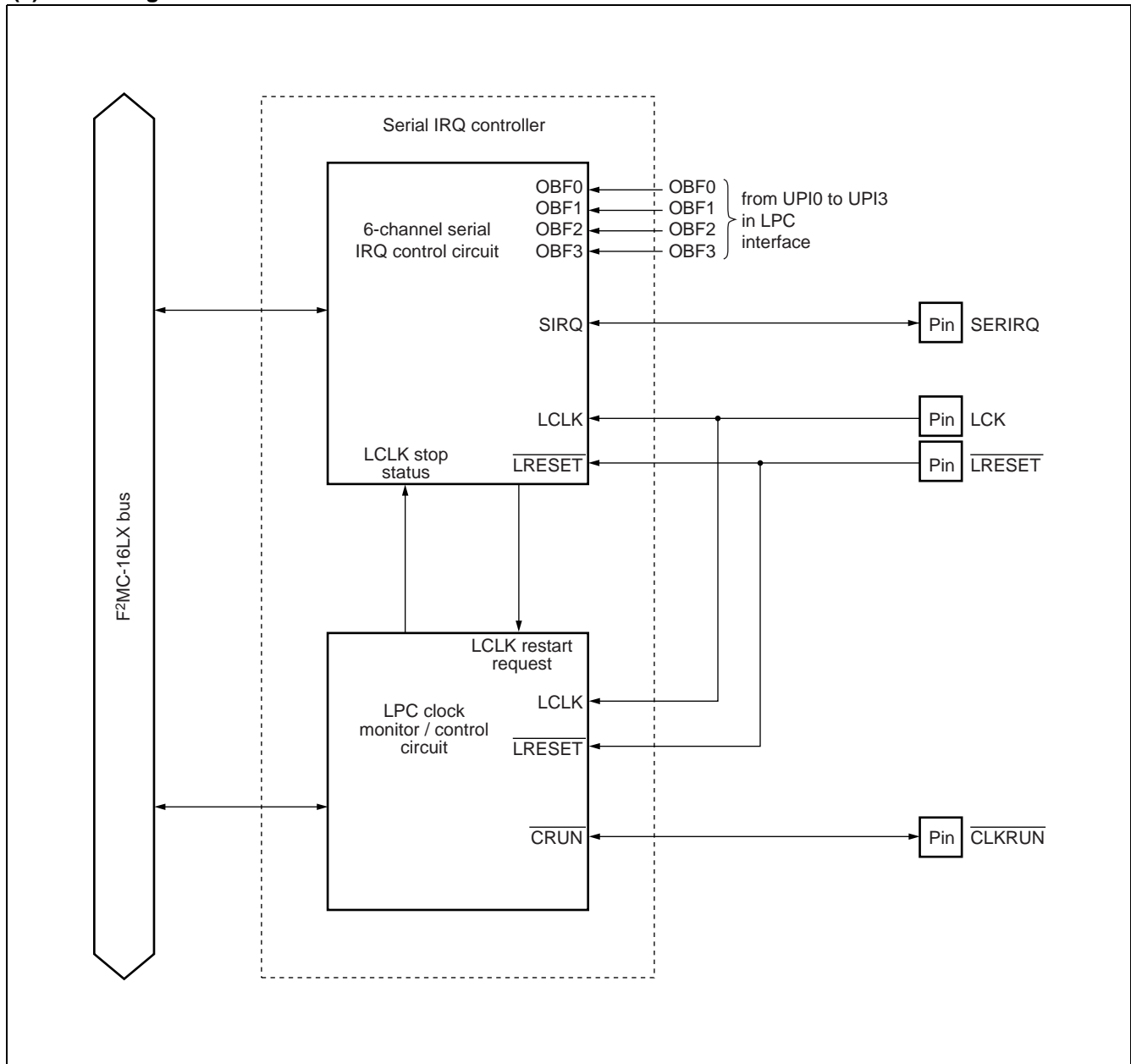
### Serial Interrupt Frame Number Register 3

Address : 000036H	7	6	5	4	3	2	1	0	⇐ Bit number SIFR3
	—	—	LV3	FR34	FR33	FR32	FR31	FR30	
Read/write	⇔ —	—	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	⇔ —	—	0	0	0	0	0	0	

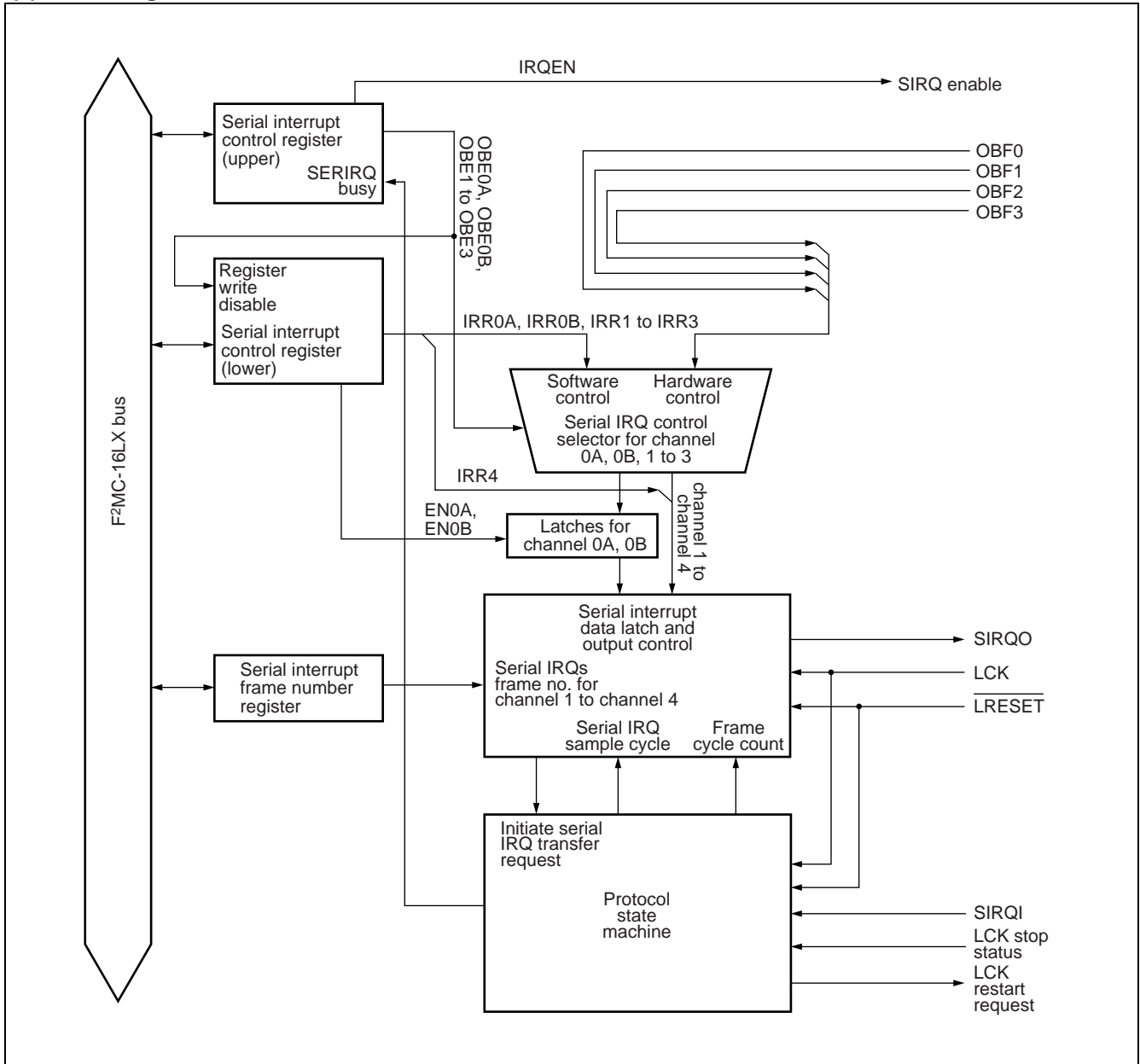
### Serial Interrupt Frame Number Register 4

Address : 000037H	15	14	13	12	11	10	9	8	⇐ Bit number SIFR4
	—	—	LV4	FR44	FR43	FR42	FR41	FR40	
Read/write	⇔ —	—	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	⇔ —	—	0	0	0	0	0	0	

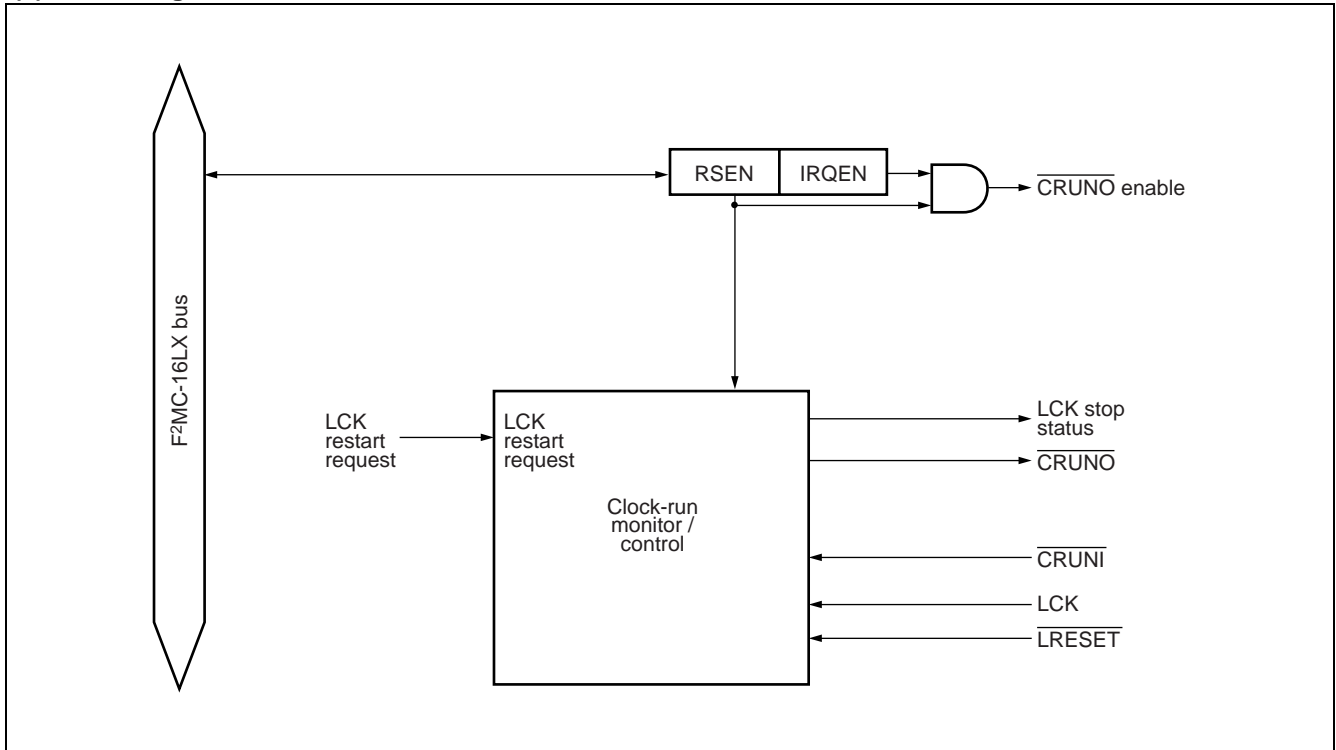
## (2) Block diagram of the serial IRQ controller



## (3) Block diagram of the 6-channel serial IRQ control circuit



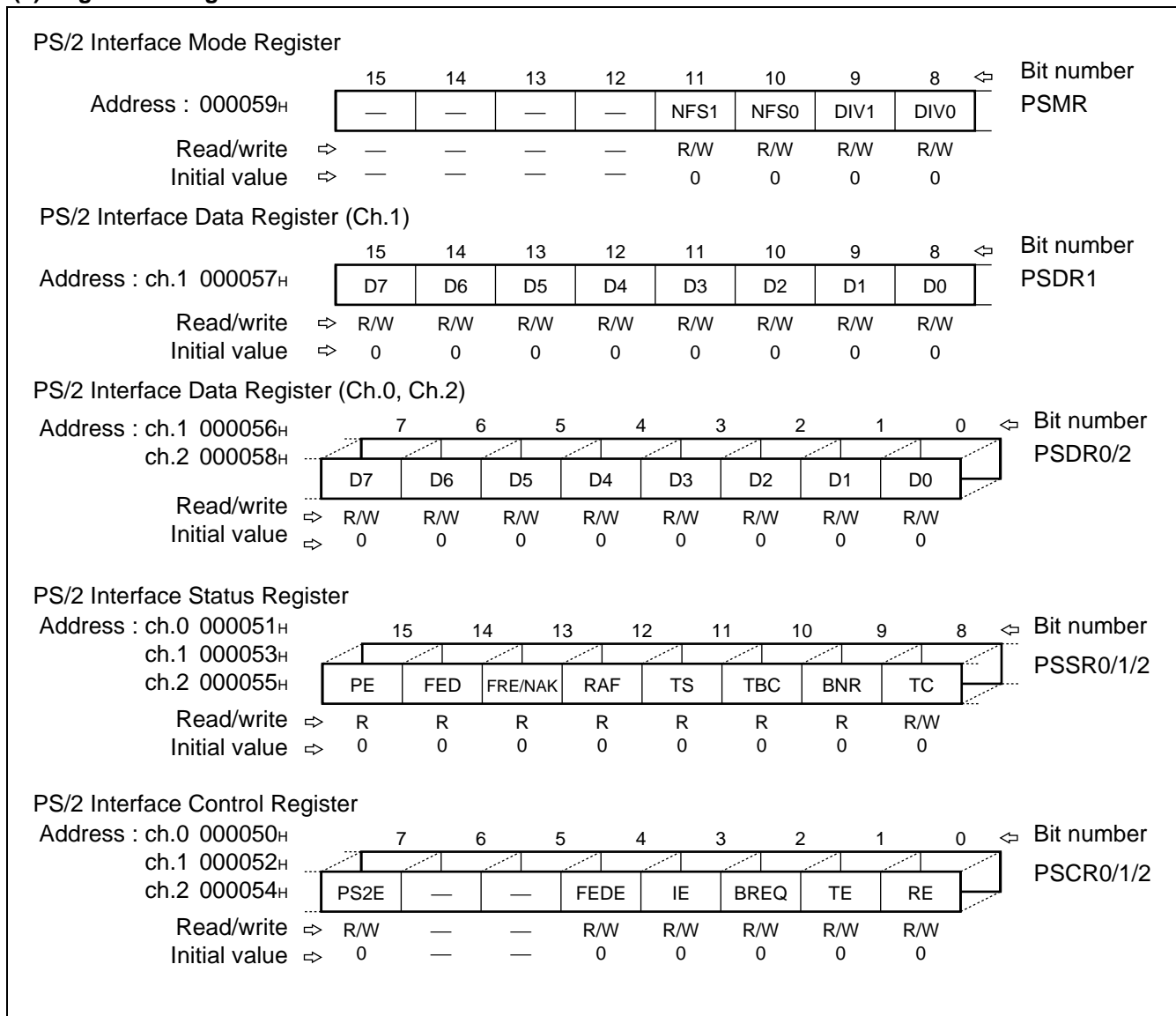
## (4) Block diagram of the LPC clock monitor / control circuit



## 18. 3-channel PS/2 interface

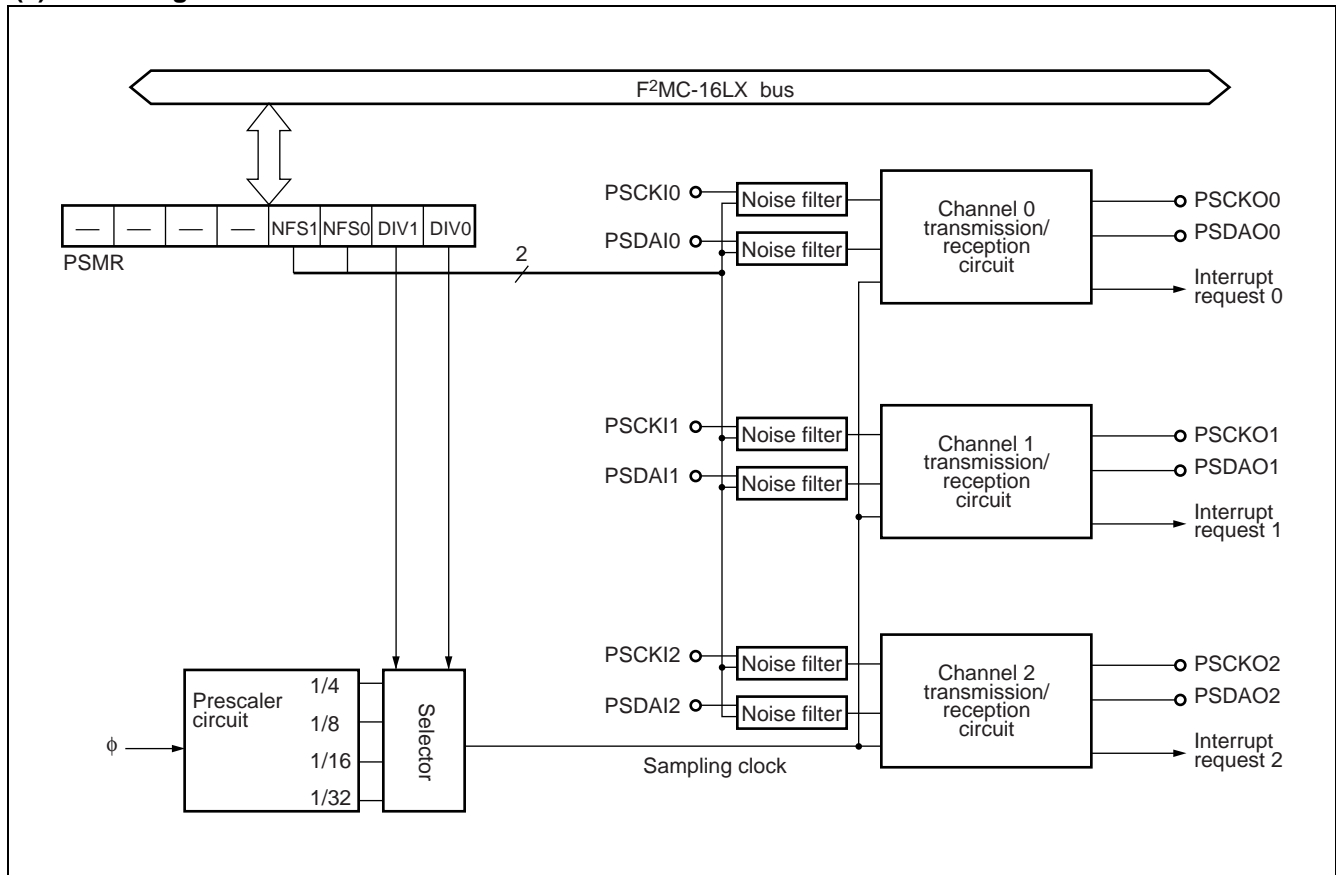
The 3-channel PS/2 interface consists of 3 individual channels of PS/2 interface that can be operated concurrently. PS/2 interface is a two wires, bidirectional serial bus providing economical way for data exchange between host (keyboard controller) and device (keyboard / mouse, etc) .

### (1) Register configuration of 3-channel PS/2 interface

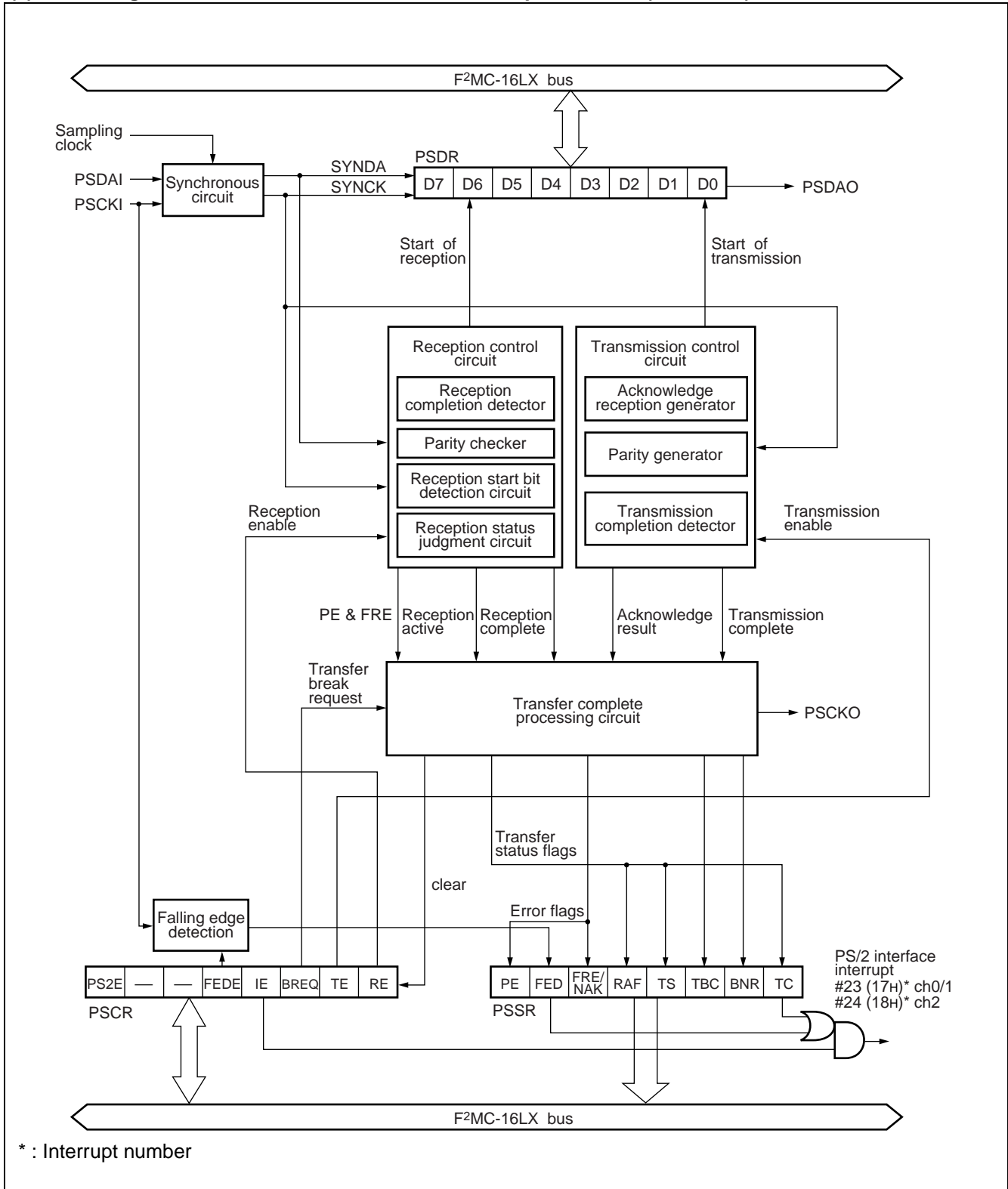


# MB90370 Series

(2) Block diagram of 3-channel PS/2 interface



## (3) Block diagram of PS/2 interface transmission/reception circuit (1 channel)



# MB90370 Series

## 19. Parity generator

The parity generator is a simple circuit that generates odd / even parity based on the input data. It consists of a parity generator data register (PGDR) , an odd / even parity generation logic and a parity generator control status register (PGCSR) .

An 8-bit data can be loaded into PGDR, then the parity generator will generate odd / even parity based on the input data. Either odd or even parity can be generated by setting the PGCSR.

For odd parity generation, if the number of “1”s in the PGDR is even number, then the parity bit in PGCSR will be set to “1”, otherwise the parity bit will be set to “0”.

For even parity generation, if the number of “1”s in the PGDR is even number, then the parity bit in PGCSR will be set to “0”, otherwise the parity bit will be set to “1”.

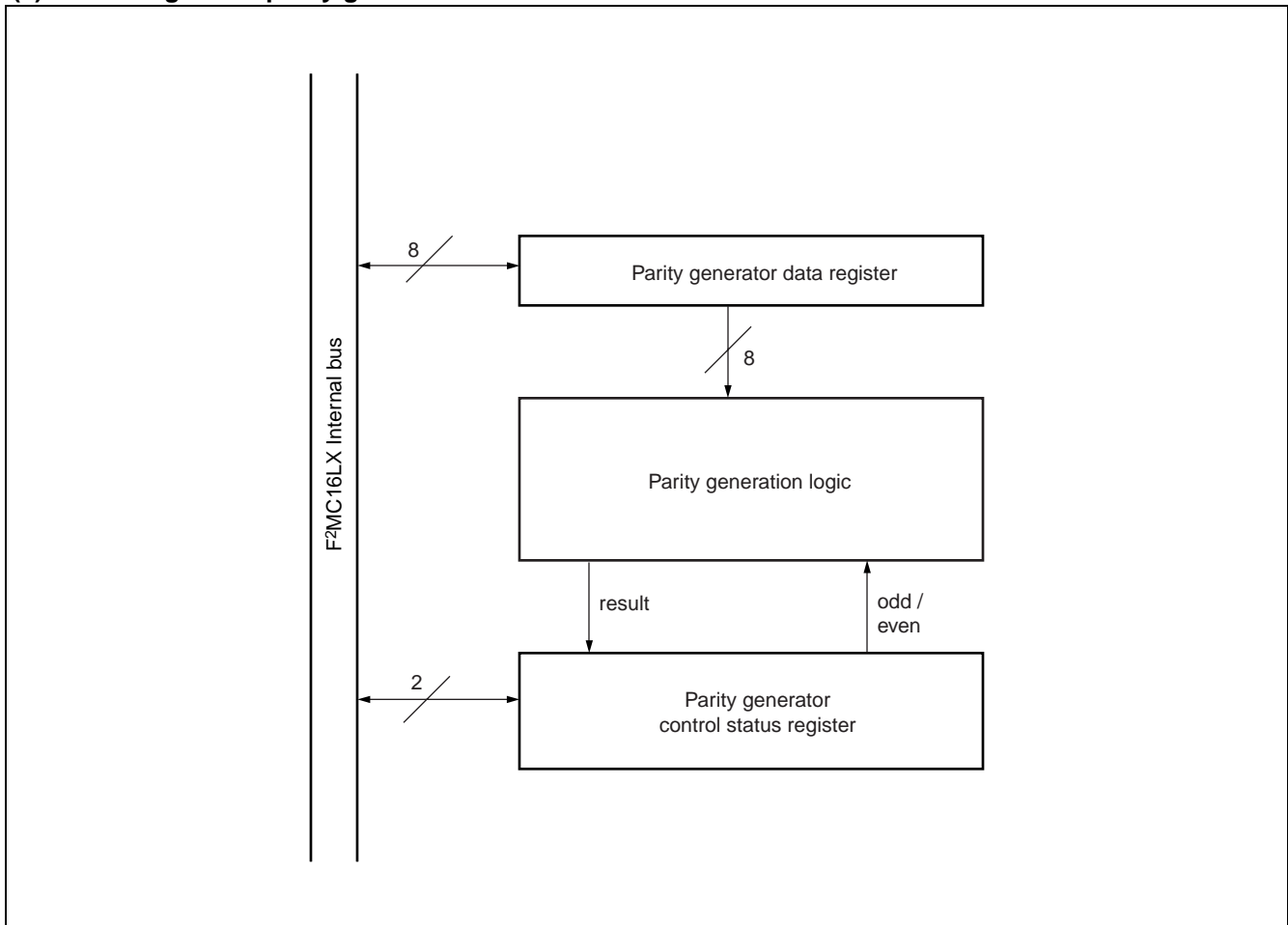
Table shows some examples of odd / even parity generation.

Input data	Parity bit (odd parity)	Parity bit (even parity)
0000 0000 <sub>B</sub>	1	0
0101 0101 <sub>B</sub>	1	0
1000 0000 <sub>B</sub>	0	1
1010 1011 <sub>B</sub>	0	1

### (1) Register configuration of parity generator

Parity Generator Data Register									
Address : 000018 <sub>H</sub>	7	6	5	4	3	2	1	0	⇐ Bit number PGDR
	D7	D6	D5	D4	D3	D2	D1	D0	
Read/write ⇨	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value ⇨	X	X	X	X	X	X	X	X	
Parity Generator Control Status Register									
Address : 000019 <sub>H</sub>	15	14	13	12	11	10	9	8	⇐ Bit number PGCSR
	PRTY	—	—	—	—	—	—	PSEL	
Read/write ⇨	R	—	—	—	—	—	—	R/W	
Initial value ⇨	X	—	—	—	—	—	—	0	

## (2) Block diagram of parity generator



# MB90370 Series

## 20. Bit decoder

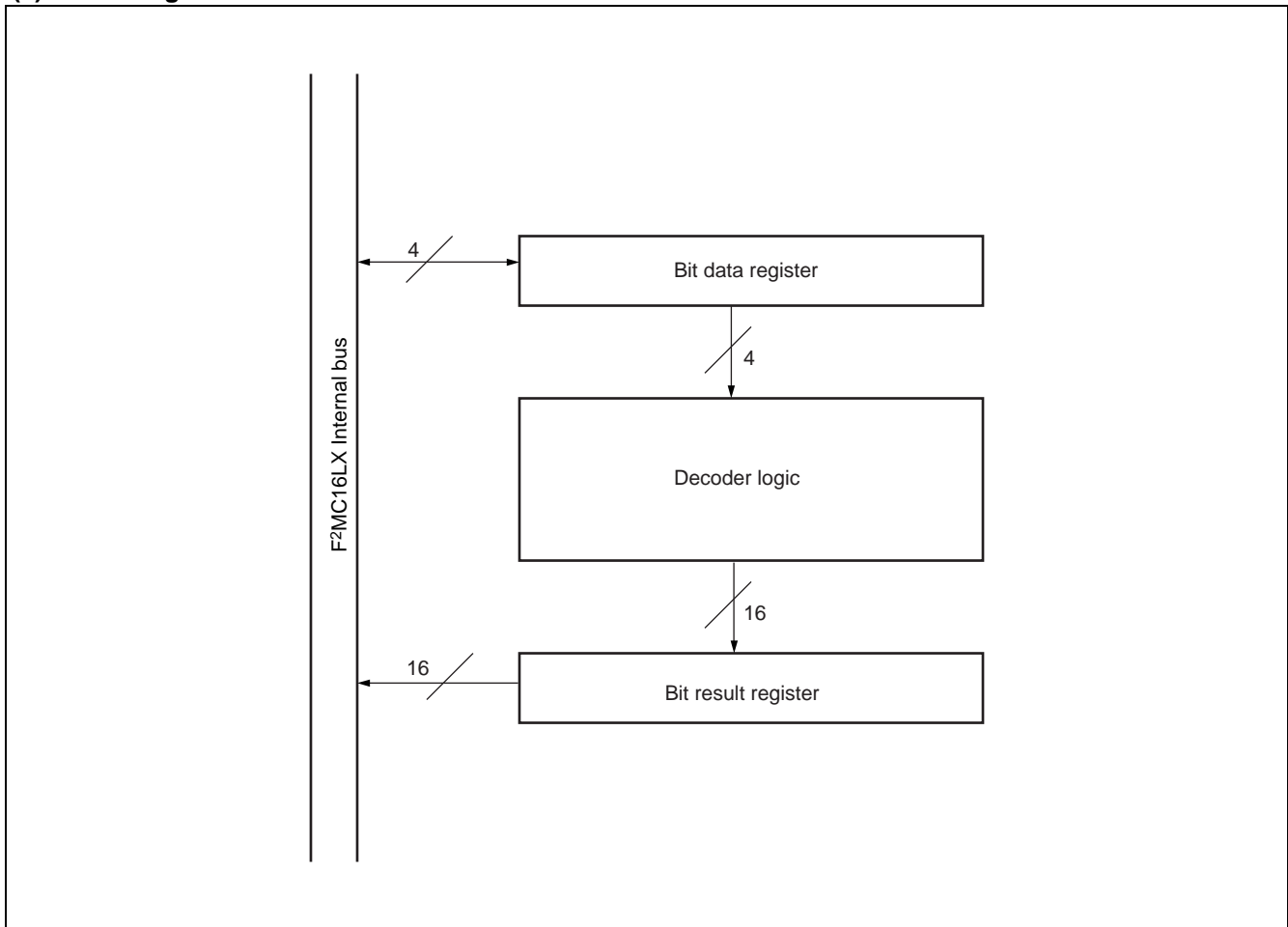
The bit decoder is a simple one-hot decoder that can be used together with the keyscan inputs. It consists of a bit data register (BDR) , a decoder logic and a bit result register (BRR) . A 4-bit encoded data can be loaded into BDR, then the decoder logic will decode the data and store the 16-bit resulted data into BRR. A table below shows the decoder's logic.

4-bit encoded data	16-bit resulted data
0H	0000 0000 0000 0001 <sub>B</sub>
1H	0000 0000 0000 0010 <sub>B</sub>
2H	0000 0000 0000 0100 <sub>B</sub>
3H	0000 0000 0000 1000 <sub>B</sub>
4H	0000 0000 0001 0000 <sub>B</sub>
5H	0000 0000 0010 0000 <sub>B</sub>
6H	0000 0000 0100 0000 <sub>B</sub>
7H	0000 0000 1000 0000 <sub>B</sub>
8H	0000 0001 0000 0000 <sub>B</sub>
9H	0000 0010 0000 0000 <sub>B</sub>
AH	0000 0100 0000 0000 <sub>B</sub>
BH	0000 1000 0000 0000 <sub>B</sub>
CH	0001 0000 0000 0000 <sub>B</sub>
DH	0010 0000 0000 0000 <sub>B</sub>
EH	0100 0000 0000 0000 <sub>B</sub>
FH	1000 0000 0000 0000 <sub>B</sub>

### (1) Register configuration of bit decoder

Bit Data Register										
Address : 0000E1H	15	14	13	12	11	10	9	8	↔	Bit number BDR
	—	—	—	—	D3	D2	D1	D0		
Read/write	⇒	—	—	—	R/W	R/W	R/W	R/W		
Initial value	⇒	—	—	—	X	X	X	X		
Bit Result Register (Upper)										
Address : 0000E3H	15	14	13	12	11	10	9	8	↔	Bit number BRRH
	R15	R14	R13	R12	R11	R10	R9	R8		
Read/write	⇒	R	R	R	R	R	R	R		
Initial value	⇒	X	X	X	X	X	X	X		
Bit Result Register (Lower)										
Address : 0000E2H	7	6	5	4	3	2	1	0	↔	Bit number BRRL
	R7	R6	R5	R4	R3	R2	R1	R0		
Read/write	⇒	R	R	R	R	R	R	R		
Initial value	⇒	X	X	X	X	X	X	X		

## (2) Block diagram of bit decoder



## 21. Wake-up interrupt

The wake-up interrupt circuit detects the signals of the “L” levels input to the external interrupt pins and to generate interrupt request to the CPU. These interrupts can wake up the CPU from standby mode.

Wake-up interrupt pins : 8 pins (P00/KSI0 to P07/KSI7) .

Wake-up interrupt sources : “L” level signal input to a wake-up interrupt pin.

Interrupt control : Enables or disables to input wake-up interrupt controlled by wake-up interrupt control register (EICR) .

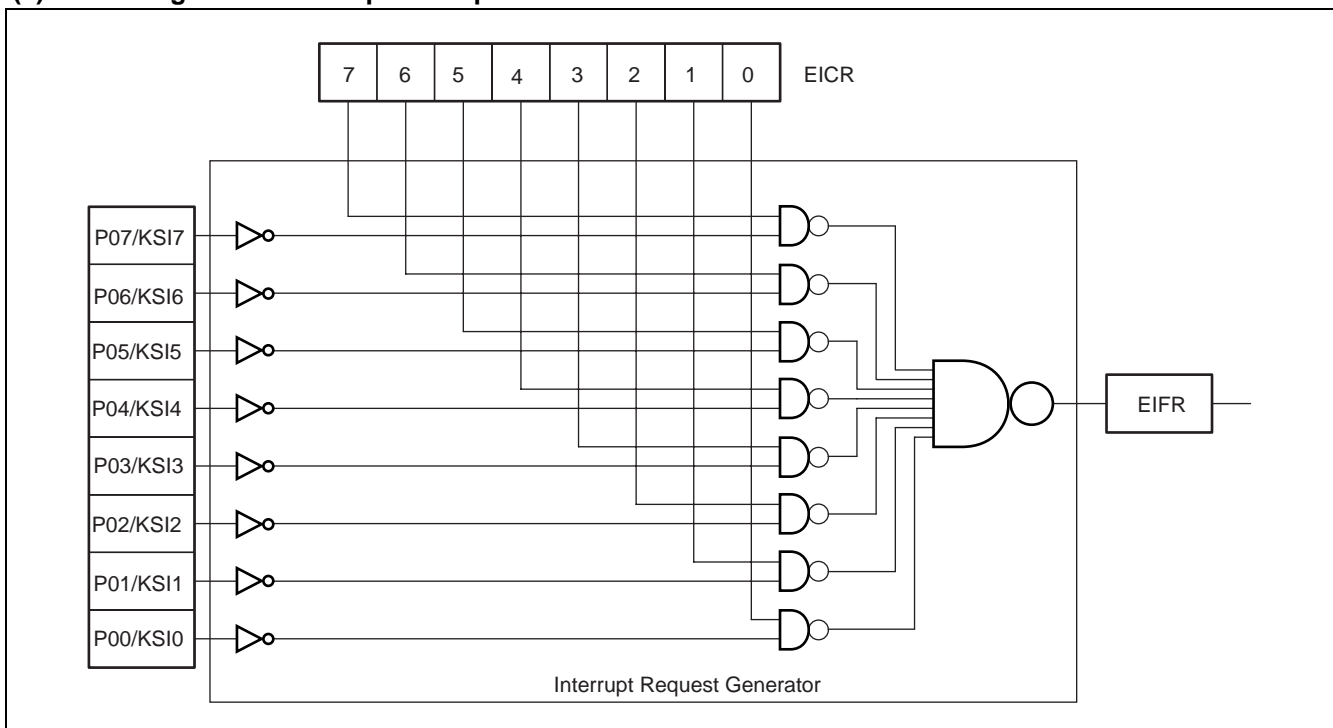
Interrupt flag : IRQ flag bit of wake-up interrupt flag register (EIFR) . Flag set when there is an IRQ.

Interrupt request : Interrupt request #20 is generated if any enabled external interrupt pin goes LOW.

### (1) Register configuration of wake-up interrupt

Wake-up Interrupt Flag Register										
Address : 0000AD <sub>H</sub>	15	14	13	12	11	10	9	8	↔	Bit number EIFR
	—	—	—	—	—	—	—	WIF		
Read/write	⇒	—	—	—	—	—	—	R/W		
Initial value	⇒	—	—	—	—	—	—	0		
Wake-up Interrupt Control Register										
Address : 0000AC <sub>H</sub>	7	6	5	4	3	2	1	0	↔	Bit number EICR
	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0		
Read/write	⇒	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	⇒	0	0	0	0	0	0	0	0	

### (2) Block diagram of wake-up interrupt



## 22. DTP/External interrupts

The DTP (Data Transfer Peripheral) /external interrupt circuit is activated by the signal supplied to a DTP/external interrupt pin. The CPU accepts the signal using the same as procedure used for normal hardware interrupts and generates external interrupts or activates the extended intelligent I/O service (EI<sup>2</sup>OS) .

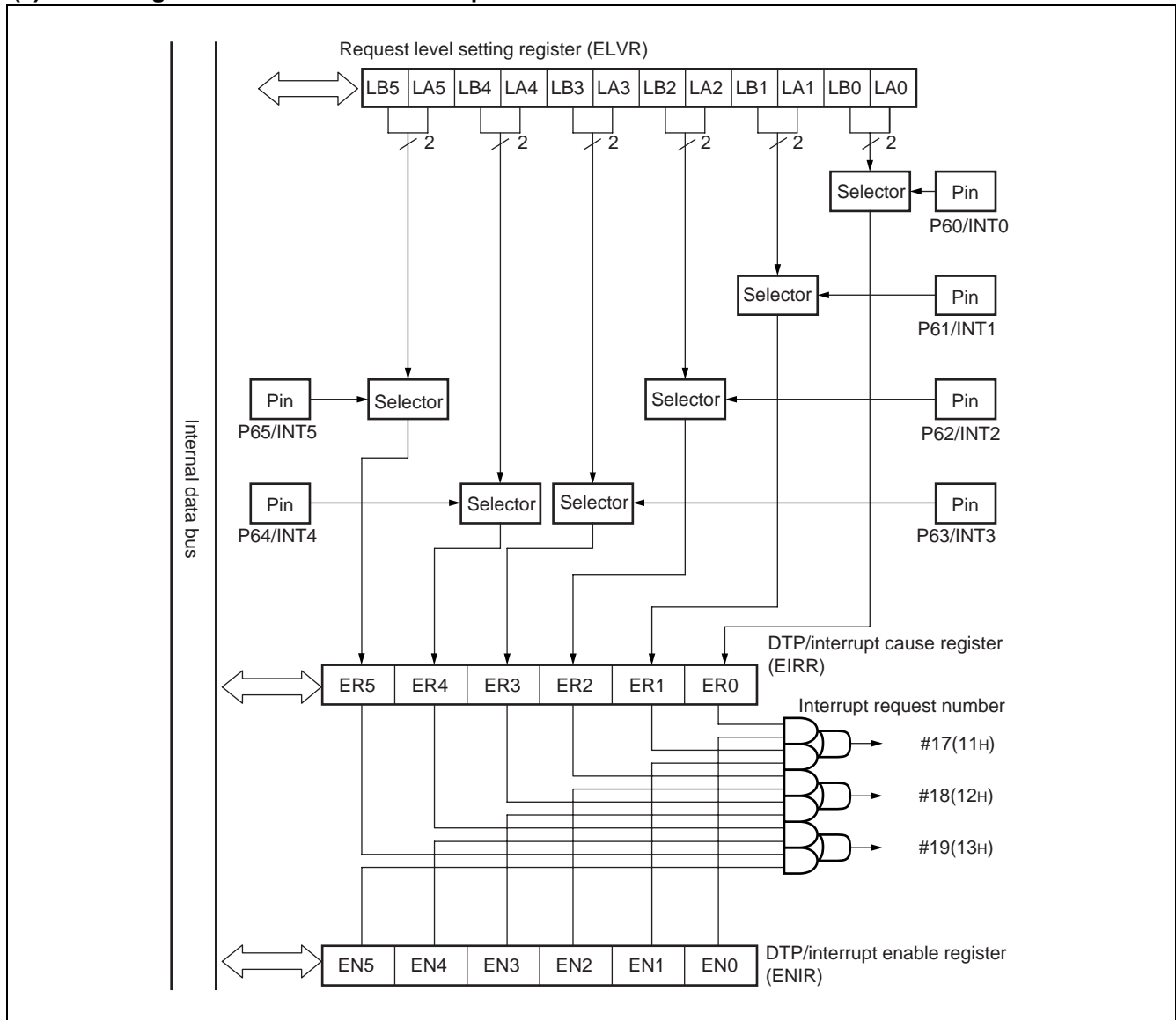
Features of DTP/External interrupt :

- Total 6 external interrupt channels
- Two request levels (“H” and “L”) are provided for the intelligent I/O service.
- Four request levels (rise/fall edge, fall edge, “H” level and “L” level) are provided for external interrupt requests .

### (1) Register configuration

DTP/Interrupt Source Register									
Address : 000027H	15	14	13	12	11	10	9	8	Bit number EIRR
	—	—	ER5	ER4	ER3	ER2	ER1	ER0	
Read/write	⇒ —	⇒ —	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	
Initial value	⇒ —	⇒ —	⇒ 0	⇒ 0	⇒ 0	⇒ 0	⇒ 0	⇒ 0	
DTP/Interrupt Enable Register									
Address : 000026H	7	6	5	4	3	2	1	0	Bit number ENIR
	—	—	EN5	EN4	EN3	EN2	EN1	EN0	
Read/write	⇒ —	⇒ —	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	
Initial value	⇒ —	⇒ —	⇒ 0	⇒ 0	⇒ 0	⇒ 0	⇒ 0	⇒ 0	
Request Level Setting Register (Upper)									
Address : 000029H	15	14	13	12	11	10	9	8	Bit number ELVRH
	—	—	—	—	LB5	LA5	LB4	LA4	
Read/write	⇒ —	⇒ —	⇒ —	⇒ —	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	
Initial value	⇒ —	⇒ —	⇒ —	⇒ —	⇒ 0	⇒ 0	⇒ 0	⇒ 0	
Request Level Setting Register (Lower)									
Address : 000028H	7	6	5	4	3	2	1	0	Bit number ELVRL
	LB3	LA3	LB2	LA2	LB1	LA1	LB0	LA0	
Read/write	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R/W	
Initial value	⇒ 0	⇒ 0	⇒ 0	⇒ 0	⇒ 0	⇒ 0	⇒ 0	⇒ 0	

## (2) Block diagram of DTP/External interrupts



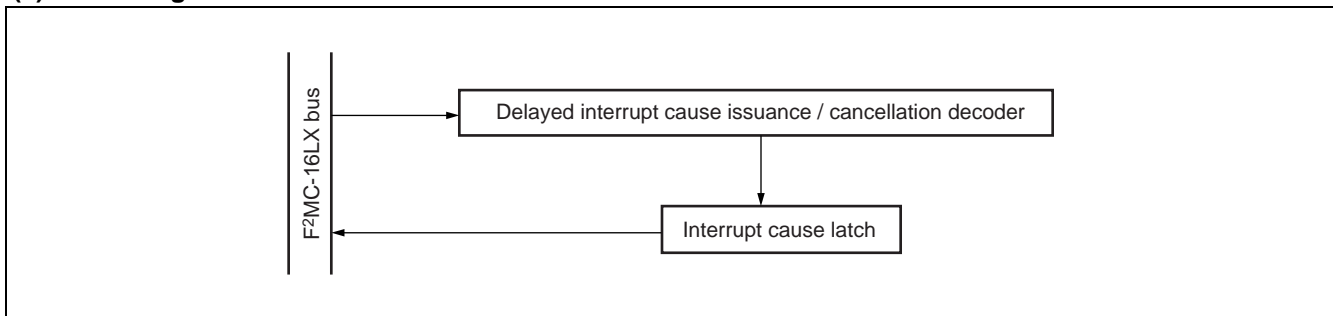
## 23. Delayed interrupt generation module

The delayed interrupt generation module is used to generate a task switching interrupt. Interrupt requests to the F<sup>2</sup>MC-16LX CPU can be generated and cleared by software using this module.

### (1) Register configuration

Delayed Interrupt Generator Module Register									Bit number
Address : 00009F <sub>H</sub>	15	14	13	12	11	10	9	8	DIRR
Read/write	⇒	—	—	—	—	—	—	R/W	
Initial value	⇒	—	—	—	—	—	—	0	

### (2) Block diagram



## 24. ROM correction function

When an address matches the value set in the address detection register, the instruction code to be loaded into the CPU is forced to be replaced with the INT9 instruction code (01H) . When executing a set instruction, the CPU executes the INT9 instruction. The ROM correction function is implemented by processing using the INT9 interrupt routine.

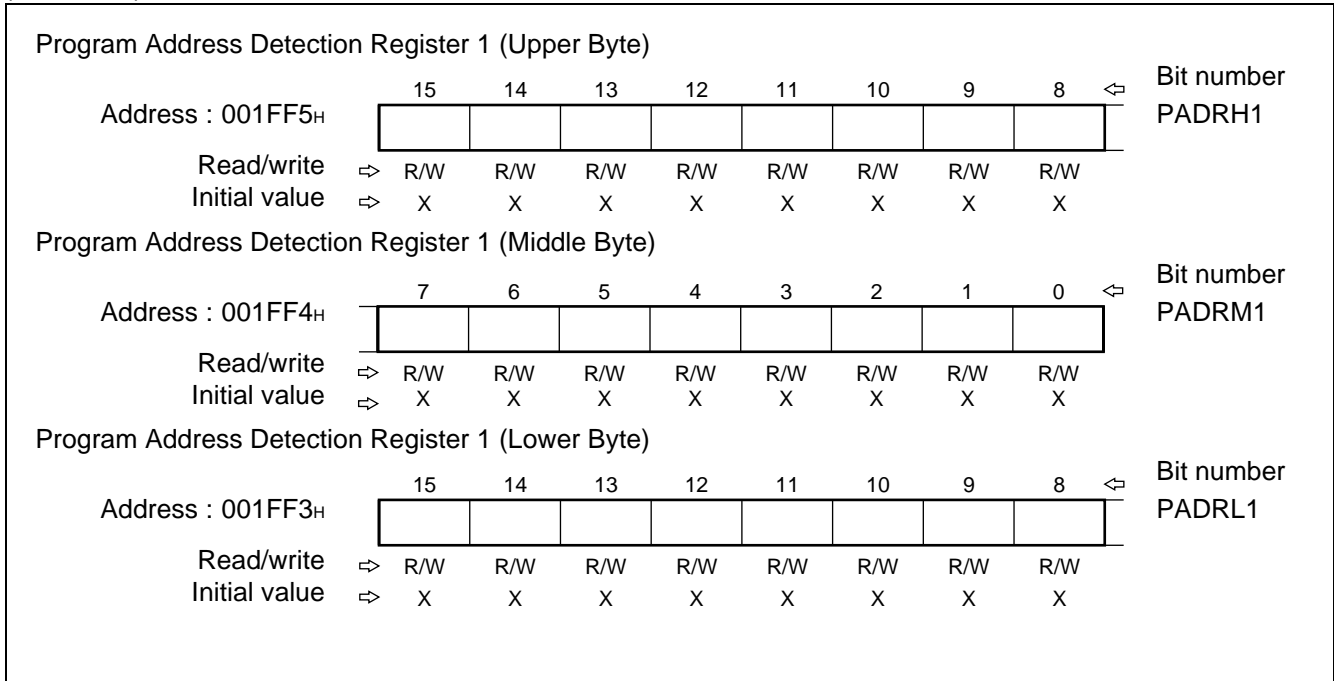
The device contains two address detection registers, each provided with a compare enable bit. When the value set in the address detection register matches an address and the interrupt enable bit is "1", the instruction code to be loaded into the CPU is forced to be replaced with the INT9 instruction code.

### (1) Register configuration

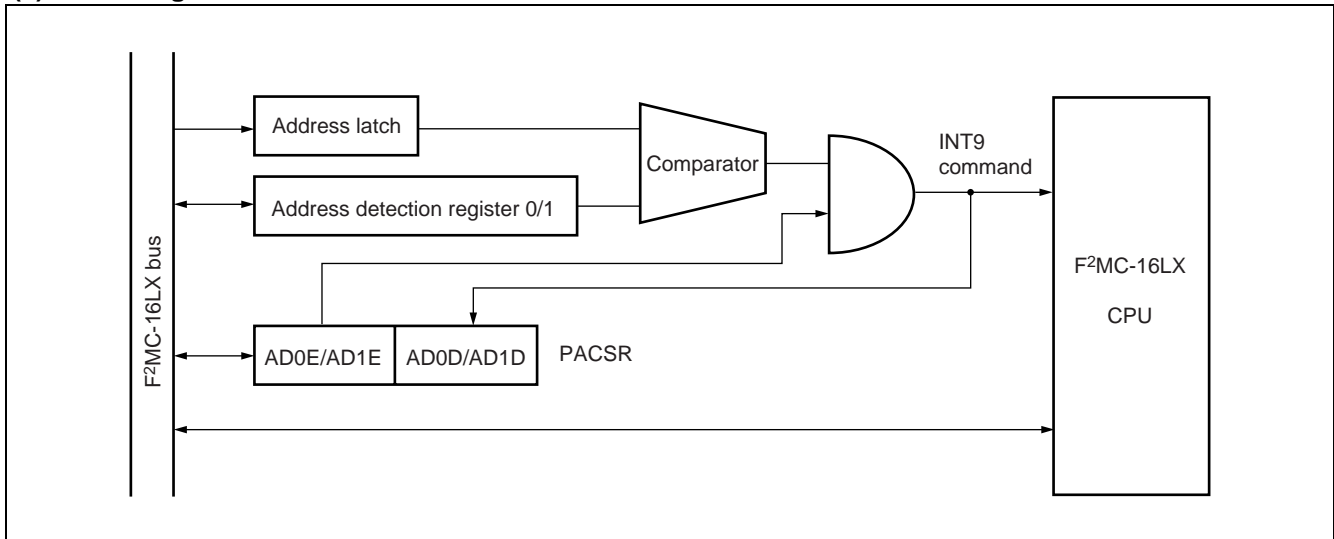
Program Address Detection Control / Status Register									
Address : 00009EH	7	6	5	4	3	2	1	0	⇐ Bit number PACSR
	—	—	—	—	AD1E	AD1D	AD0E	AD0D	
Read/write	⇐ —	⇐ —	⇐ —	⇐ —	⇐ R/W	⇐ R/W	⇐ R/W	⇐ R/W	
Initial value	⇐ —	⇐ —	⇐ —	⇐ —	⇐ 0	⇐ 0	⇐ 0	⇐ 0	
Program Address Detection Register 0 (Upper Byte)									
Address : 001FF2H	7	6	5	4	3	2	1	0	⇐ Bit number PADRH0
Read/write	⇐ R/W	⇐ R/W	⇐ R/W	⇐ R/W	⇐ R/W	⇐ R/W	⇐ R/W	⇐ R/W	
Initial value	⇐ X	⇐ X	⇐ X	⇐ X	⇐ X	⇐ X	⇐ X	⇐ X	
Program Address Detection Register 0 (Middle Byte)									
Address : 001FF1H	15	14	13	12	11	10	9	8	⇐ Bit number PADRM0
Read/write	⇐ R/W	⇐ R/W	⇐ R/W	⇐ R/W	⇐ R/W	⇐ R/W	⇐ R/W	⇐ R/W	
Initial value	⇐ X	⇐ X	⇐ X	⇐ X	⇐ X	⇐ X	⇐ X	⇐ X	
Program Address Detection Register 0 (Lower Byte)									
Address : 001FF0H	7	6	5	4	3	2	1	0	⇐ Bit number PADRL0
Read/write	⇐ R/W	⇐ R/W	⇐ R/W	⇐ R/W	⇐ R/W	⇐ R/W	⇐ R/W	⇐ R/W	
Initial value	⇐ X	⇐ X	⇐ X	⇐ X	⇐ X	⇐ X	⇐ X	⇐ X	

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(Continued)



## (2) Block diagram



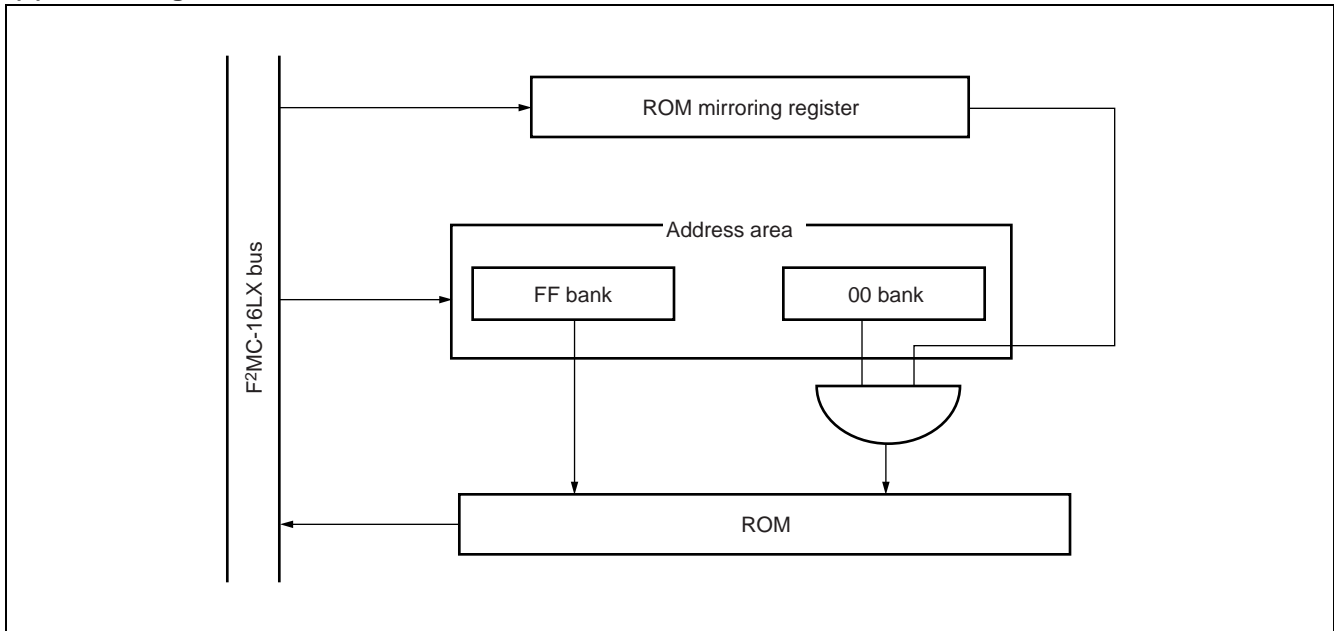
## 25. ROM mirroring function selection module

The ROM mirroring function selection module can select what the FF bank allocated the ROM sees through the 00 bank according to register settings.

### (1) Register configuration

ROM Mirror Function Selection Register								Bit number	
Address : 0006FH	15	14	13	12	11	10	9	8	ROMM
Read/write	⇒	—	—	—	—	—	—	—	W
Initial value	⇒	—	—	—	—	—	—	—	1

### (2) Block diagram



## 26. 512K bit flash memory

The 512K bit flash memory is allocated in the FF<sub>H</sub> banks on the CPU memory map. Like masked ROM, flash memory is read-accessible and program-accessible to the CPU using the flash memory interface circuit. The flash memory can be programmed/erased by the instruction from the CPU via the flash memory interface circuit. The flash memory can therefore be reprogrammed (updated) while still on the circuit board under integrated CPU control, allowing program code and data to be improved efficiently. Note that sector operations such as “enable sector protect” cannot be used.

Features of 512K bit flash memory :

- 64 Kwords × 8 bits / 32 Kwords × 16 bits (16 K + 8 K + 8 K + 32 K) sector configuration
- Automatic program algorithm (same as the Embedded Algorithm : MBM29F400TA)
- Installation of the deletion temporary stop/delete restart function
- Write/delete completion detected by the data polling or toggle bit
- Write/delete completion detected by the CPU interrupt
- Compatibility with the JEDEC standard-type command
- Each sector deletion can be executed (Sectors can be freely combined) .
- Number of write/delete operations 10,000 times guaranteed

### (1) Register configuration

Flash Memory Control Status Register									Bit number FMCS
Address : 0000AE <sub>H</sub>	7	6	5	4	3	2	1	0	
	INTE	RDYINT	WE	RDY	Reserved	LPM1	Reserved	LPM0	
Read/write	⇒ R/W	⇒ R/W	⇒ R/W	⇒ R	⇒ W	⇒ R/W	⇒ W	⇒ R/W	
Initial value	⇒ 0	⇒ 0	⇒ 0	⇒ 1	⇒ 0	⇒ 0	⇒ 0	⇒ 0	

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## (2) Sector configuration of 512K bits flash memory

The 512K bits flash memory has the sector configuration illustrated below. The addresses in the illustration are the upper and lower addresses of each sector.

When accessed from the CPU, SA0 and SA1 to SA3 are allocated in the FF bank registers, respectively.

Flash memory	CPU address	*Writer address
SA3 (16 Kbytes)	FFFFFFH	7FFFFH
	FFC000H	7C000H
SA2 (8 Kbytes)	FFBFFFH	7BFFFH
	FFA000H	7A000H
SA1 (8 Kbytes)	FF9FFFH	79FFFH
	FF8000H	78000H
SA0 (32 Kbytes)	FF7FFFH	77FFFH
	FF0000H	70000H

\* : Writer addresses correspond to CPU addresses when data is programmed in flash memory by a parallel writer. Writer addresses are used to program/erase data using a general-purpose writer.

## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Ratings

( $V_{SS} = AV_{SS} = CV_{SS} = 0.0\text{ V}$ )

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage	$V_{CC}$	$V_{SS} - 0.3$	$V_{SS} + 4.0$	V	
	$CV_{CC}$	$V_{SS} - 0.3$	$V_{SS} + 4.0$	V	$V_{CC} \geq CV_{CC}$ *1
	$AV_{CC}$	$V_{SS} - 0.3$	$V_{SS} + 4.0$	V	$V_{CC} \geq AV_{CC}$ *1
A/D converter reference input voltage	AVR	$V_{SS} - 0.3$	$V_{SS} + 4.0$	V	$AV_{CC} \geq AVR$ , $AVR \geq AV_{SS}$
Comparator reference input voltage	CVRH1 CVRH2 CVRL	$V_{SS} - 0.3$	$V_{SS} + 4.0$	V	$CV_{CC} \geq CVRH1$ , $CVRH1 \geq CV_{SS}$ $CV_{CC} \geq CVRH2$ , $CVRH2 \geq CV_{SS}$ $CV_{CC} \geq CVRL$ , $CVRL \geq CV_{SS}$
LCD power supply voltage	V1 to V3	$V_{SS} - 0.3$	$V_{SS} + 4.0$	V	V1 to V3 must not exceed $V_{CC}$
Input voltage	$V_{I1}$	$V_{SS} - 0.3$	$V_{SS} + 4.0$	V	All pins except P40 to P45, P80 to P82, P90 to P95 *2
	$V_{I2}$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	P40 to P45, P80 to P82, P90 to P95
Output voltage	$V_O$	$V_{SS} - 0.3$	$V_{SS} + 4.0$	V	*2
Maximum clamp current	$I_{CLAMP}$	-2.0	+2.0	mA	*4
Total maximum clamp current	$\Sigma I_{CLAMP} $	—	20	mA	*4
“L” level maximum output current	$I_{OL1}$	—	10	mA	All pins except PF0 to PF7*3
	$I_{OL2}$	—	20	mA	PF0 to PF7*3
“L” level average output current	$I_{OLAV1}$	—	4	mA	All pins except PF0 to PF7 Average output current = operating current $\times$ operating efficiency
	$I_{OLAV2}$	—	12	mA	PF0 to PF7 Average output current = operating current $\times$ operating efficiency
“L” level total maximum output current	$\Sigma I_{OL}$	—	100	mA	
“L” level total average output current	$\Sigma I_{OLAV}$	—	50	mA	Average output current = operating current $\times$ operating efficiency
“H” level maximum output current	$I_{OH}$	—	-10	mA	*3
“H” level average output current	$I_{OHAV}$	—	-3	mA	Average output current = operating current $\times$ operating efficiency
“H” level total maximum output current	$\Sigma I_{OH}$	—	-100	mA	
“H” level total average output current	$\Sigma I_{OHAV}$	—	-50	mA	Average output current = operating current $\times$ operating efficiency

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# MB90370 Series

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( $V_{SS} = AV_{SS} = CV_{SS} = 0.0\text{ V}$ )

Parameter	Symbol	Rting		Unit	Remarks
		Min	Max		
Power consumption	$P_D$	—	200	mW	
Operating temperature	$T_A$	-40	+85	°C	
Storage temperature	$T_{stg}$	-55	+150	°C	

\*1 : Set  $AV_{CC}$ ,  $CV_{CC}$  and  $V_{CC}$  at the same voltage. Take care so that AVR, CVRH1, CVRH2 and CVRL do not exceed  $V_{CC} + 0.3\text{ V}$  when the power is turned on.

\*2 :  $V_i$  and  $V_o$  shall never exceed  $V_{CC} + 0.3\text{ V}$ .  $V_i$  should not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the  $I_{CLAMP}$  rating supersedes the  $V_i$  rating.

\*3 : The maximum output current is a peak value for a corresponding pin.

\*4 : Applicable to pins : P00 to P07, P10 to P17, P20 to P27, P30 to P37, P47, P50 to P57, P60 to P67, P70 to P77, PA0 to PA6, PC3 to PC7, PD0 to PD3, PD6, PD7

Use within recommended operating conditions.

Use at DC voltage (current) .

The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.

The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.

Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the  $V_{CC}$  pin, and this may affect other devices.

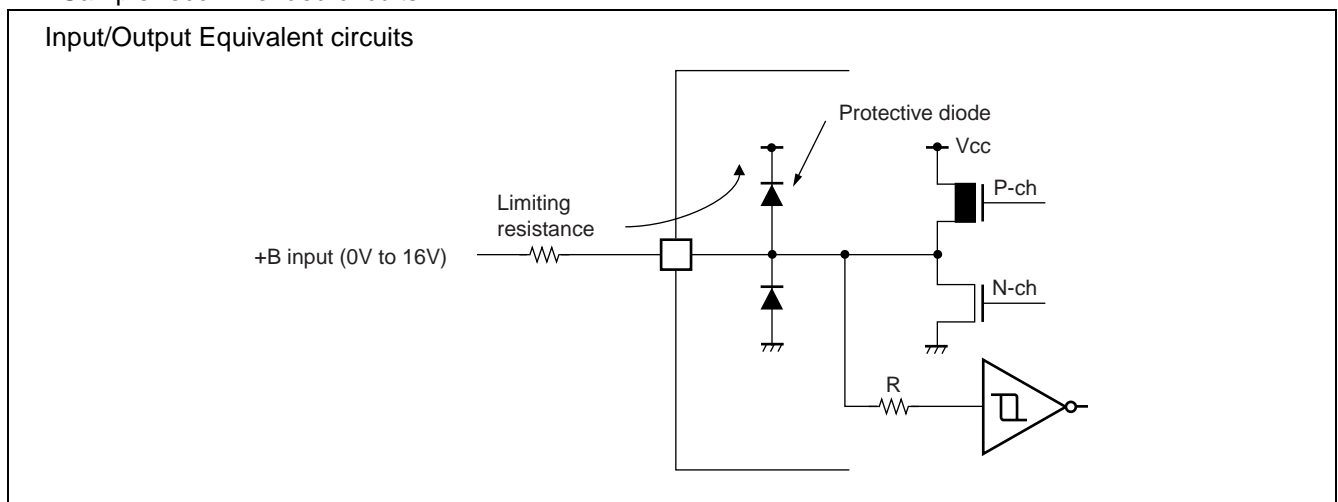
Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0V) , the power supply is provided from the pins, so that incomplete operation may result.

Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.

Care must be taken not to leave the +B input pin open.

Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal input.

Sample recommended circuits :



**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## 2. Recommended Operating Conditions

( $V_{SS} = AV_{SS} = CV_{SS} = 0.0\text{ V}$ )

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage *1	$V_{CC}$	3.0	3.6	V	Normal operation assurance range
	$CV_{CC}$	3.3	3.6	V	
	$V_{CC}$	1.8	3.6	V	Retains the RAM state in stop mode
A/D converter reference input voltage *2	AVR	0	$AV_{CC}$	V	Normal operation assurance range
LCD power supply voltage	V1 to V3	$V_{SS}$	$V_{CC}$	V	V1 to V3 pins (The optimum value is dependent on the LCD element in use.)
Operating temperature	$T_A$	-40	+85	°C	

\*1 : Set  $AV_{CC}$ ,  $CV_{CC}$  and  $V_{CC}$  at the same voltage.

\*2 : Take care so that AVR, CVRH1, CVRH2 and CVRL do not exceed  $V_{CC} + 0.3\text{ V}$  when power is turned on.

**WARNING:** The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

# MB90370 Series

## 3. DC Characteristics

( $V_{CC} = AV_{CC} = CV_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = CV_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	$V_{IH}$	P10 to P17 P20 to P27 P30 to P37 P46, P47 P50 to P57 PA0 to PA6 PB0 to PB7 PC0 to PC7 PD0 to PD7 PF0 to PF7	—	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	CMOS input pins
	$V_{IHS}$	P00 to P07 P60 to P67 P70 to P77 PE0 to PE7 RST		$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	CMOS hysteresis input pins
	$V_{IHS5}$	P40 to P45		$0.8 V_{CC}$	—	$V_{SS} + 5.5$	V	5 V tolerant CMOS hysteresis input pins
	$V_{IH5}$	P82		$0.7 V_{CC}$	—	$V_{SS} + 5.5$	V	5 V tolerant CMOS input pin
	$V_{IHSM}$	P80, P81 P90 to P95		2.1	—	$V_{SS} + 5.5$	V	SMbus input pins
	$V_{IHM}$	MD0 to MD2		$V_{CC} - 0.3$	—	$V_{CC} + 0.3$	V	Mode pins
"L" level input voltage	$V_{IL}$	P10 to P17 P20 to P27 P30 to P37 P46, P47 P50 to P57 P82 PA0 to PA6 PB0 to PB7 PC0 to PC7 PD0 to PD7 PF0 to PF7	—	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	CMOS input pins
	$V_{ILS}$	P00 to P07 P40 to P45 P60 to P67 P70 to P77 PE0 to PE7 RST		$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	CMOS hysteresis input pins

(Continued)

# MB90370 Series

( $V_{CC} = AV_{CC} = CV_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = CV_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
“L” level input voltage	$V_{ILSM}$	P80, P81 P90 to P95	—	$V_{SS} - 0.3$	—	0.8	V	SMBus input pins
	$V_{ILM}$	MD0 to MD2		$V_{SS} - 0.3$	—	$V_{SS} + 0.3$	V	Mode pins
Open-drain output pin application voltage	$V_{D5}$	P40 to P45 P80 to P82 P90 to P95	—	$V_{SS} - 0.3$	—	$V_{SS} + 5.5$	V	
	$V_D$	P46		$V_{SS} - 0.3$	—	$V_{CC} + 0.3$	V	
“H” level output voltage	$V_{OH1}$	All port pins except P40 to P46 P80 to P82 P90 to P95 PF0 to PF7	$V_{CC} = 3.0\text{ V}$ $I_{OH1} = -4.0\text{ mA}$	$V_{CC} - 0.5$	—	—	V	
	$V_{OH2}$	PF0 to PF7	$V_{CC} = 3.0\text{ V}$ $I_{OH2} = -8.0\text{ mA}$	$V_{CC} - 0.5$	—	—	V	
“L” level output voltage	$V_{OL1}$	All port pins except PF0 to PF7	$I_{OL1} = 4.0\text{ mA}$	—	—	0.4	V	
	$V_{OL2}$	PF0 to PF7	$I_{OL2} = 12.0\text{ mA}$	—	—	0.4	V	
Input leakage current (High-Z output leakage current)	$I_{IL}$	All input pins	$V_{CC} = 3.3\text{ V}$ , $V_{SS} < V_i < V_{CC}$	-5	—	+5	$\mu\text{A}$	
Open-drain output leakage current	$I_{LEAK}$	P40 to P46 P80 to P82 P90 to P95	—	—	—	5	$\mu\text{A}$	
Power supply current*	$I_{CC}$	$V_{CC}$	$V_{CC} = 3.3\text{ V}$ , Internal operation at 16 MHz	—	37	45	mA	MB90F372
				—	30	35	mA	MB90372
	$I_{CCS}$		$V_{CC} = 3.3\text{ V}$ , Internal operation at 16 MHz, In sleep mode	—	15	20	mA	
	$I_{CCL}$		$V_{CC} = 3.3\text{ V}$ , External 32 kHz, Internal operation at 8 kHz, In sub-clock mode, $T_A = +25\text{ }^\circ\text{C}$	—	23	80	$\mu\text{A}$	

(Continued)

# MB90370 Series

( $V_{CC} = AV_{CC} = CV_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = CV_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*	I <sub>CCLS</sub>	V <sub>CC</sub>	V <sub>CC</sub> = 3.3 V, External 32 kHz, Internal operation at 8 kHz, In sub-clock sleep mode, T <sub>A</sub> = +25 °C	—	10	50	μA	
	I <sub>CCWAT</sub>		V <sub>CC</sub> = 3.3 V, External 32 kHz, Internal operation at 8 kHz, In watch mode, T <sub>A</sub> = +25 °C	—	1.5	30	μA	
	I <sub>CCCT</sub>		V <sub>CC</sub> = 3.3 V, Internal operation at 16 MHz, In timebase timer mode	—	1.3	2	mA	
	I <sub>CCCH</sub>		V <sub>CC</sub> = 3.3 V, In stop mode, T <sub>A</sub> = +25 °C	—	1	20	μA	
Input capacitance	C <sub>IN</sub>	All input pins except V <sub>CC</sub> , AV <sub>CC</sub> , CV <sub>CC</sub> , V <sub>SS</sub> , AV <sub>SS</sub> , CV <sub>SS</sub>	—	—	5	15	pF	
LCD divided resistance	R <sub>LCD</sub>	—	Between V <sub>CC</sub> and V3 at V <sub>CC</sub> = 3.3 V	100	200	400	kΩ	
			Between V3 and V2	50	100	200		
			Between V2 and V1 Between V1 and V <sub>SS</sub> at V <sub>CC</sub> = 3.3 V					
COM0 to COM3 output impedance	R <sub>VCOM</sub>	COM0 to COM3	V1 to V3 = 3.3 V	—	—	5	kΩ	
SEG0 to SEG8 output impedance	R <sub>VSEG</sub>	SEG0 to SEG8		—	—	5	kΩ	
LCD leakage current	L <sub>LCDL</sub>	V1 to V3 COM0 to COM3 SEG0 to SEG8	—	—	—	±1	μA	

(Continued)

(Continued)

( $V_{CC} = AV_{CC} = CV_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$ ,  $V_{SS} = AV_{SS} = CV_{SS} = 0.0 \text{ V}$ ,  $T_A = -40 \text{ }^\circ\text{C to } +85 \text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Pull-up resistance	$R_{UP}$	P00 to P07 P10 to P17 P20 to P27 P30 to P37 $\overline{RST}$	—	25	50	100	k $\Omega$	
Pull-down resistance	$R_{DOWN}$	MD2	—	25	50	100	k $\Omega$	MB90V370, MB90372 only

\* : The power supply current is measured with an external clock.

# MB90370 Series

## 4. AC Characteristics

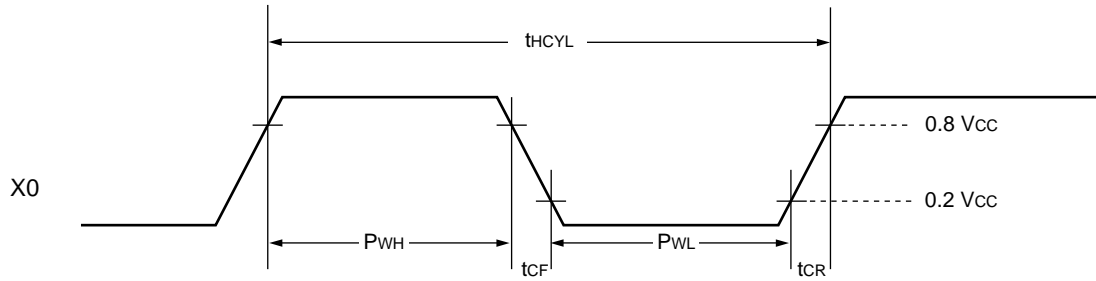
### (1) Clock Timings

( $V_{CC} = AV_{CC} = CV_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = CV_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

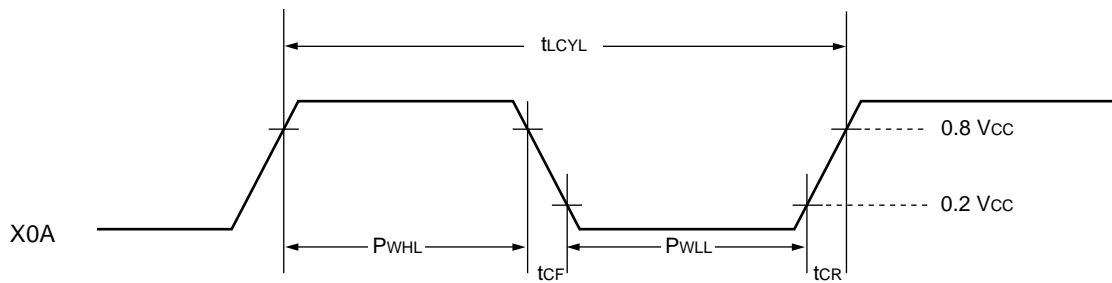
Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F <sub>CH</sub>	X0, X1	—	3	—	16	MHz	Crystal oscillator
	F <sub>CH</sub>	X0, X1		3	—	16	MHz	External clock
	F <sub>CH</sub>	X0, X1		8	—	16	MHz	PLL multiplied by 1*
				4	—	8	MHz	PLL multiplied by 2*
				3	—	5.33	MHz	PLL multiplied by 3*
				3	—	4	MHz	PLL multiplied by 4*
F <sub>CL</sub>	X0A, X1A	—		32.768	—	kHz		
Clock cycle time	t <sub>H CYL</sub>	X0, X1		31.25	—	333	ns	
	t <sub>L CYL</sub>	X0A, X1A		—	30.5	—	μs	
Input clock pulse width	P <sub>WH</sub> P <sub>WL</sub>	X0		5	—	—	ns	Recommend duty ratio of 30% to 70%
	P <sub>WHL</sub> P <sub>WLL</sub>	X0A		—	15.2	—	μs	Recommend duty ratio of 30% to 70%
Input clock rise/fall time	t <sub>CR</sub> t <sub>CF</sub>	X0		—	—	5	ns	External clock operation
Internal operating clock frequency	f <sub>CP</sub>	—	1.5	—	16	MHz	Main clock operation	
	f <sub>LCP</sub>	—	—	8.192	—	kHz	Sub-clock operation	
Internal operating clock cycle time	t <sub>CP</sub>	—	62.5	—	666	ns	Main clock operation	
	t <sub>LCP</sub>	—	—	122.1	—	μs	Sub-clock operation	

\* : When selecting the PLL clock, the range of clock frequency is limited. Use this product within range as mentioned in “Relationship between oscillating frequency and internal operating clock frequency” of “• PLL operation guarantee range”.

X0, X1 clock timing

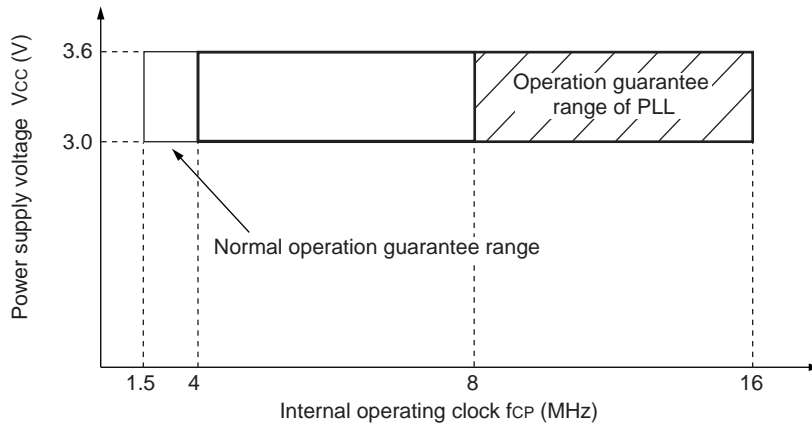


X0A, X1A clock timing

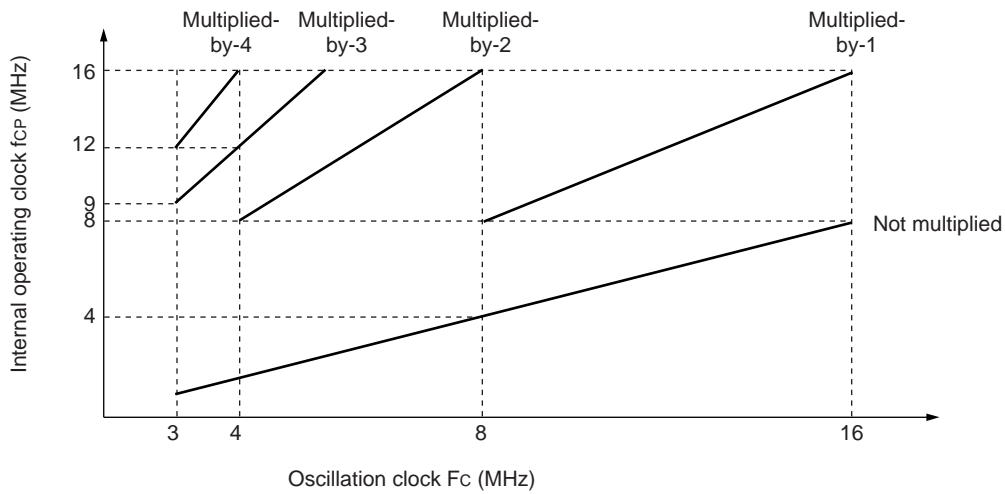


- PLL operation guarantee range

Relationship between internal operating clock frequency and power supply voltage



Relationship between oscillating frequency and internal operating clock frequency



The AC ratings are measured for the following measurement reference voltages :

- Input signal waveform

Hysteresis input pin

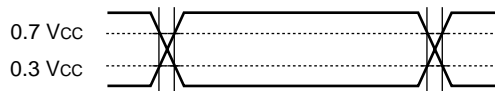


- Output signal waveform

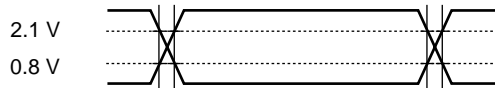
Output pin



CMOS input pin



SMbus input pin



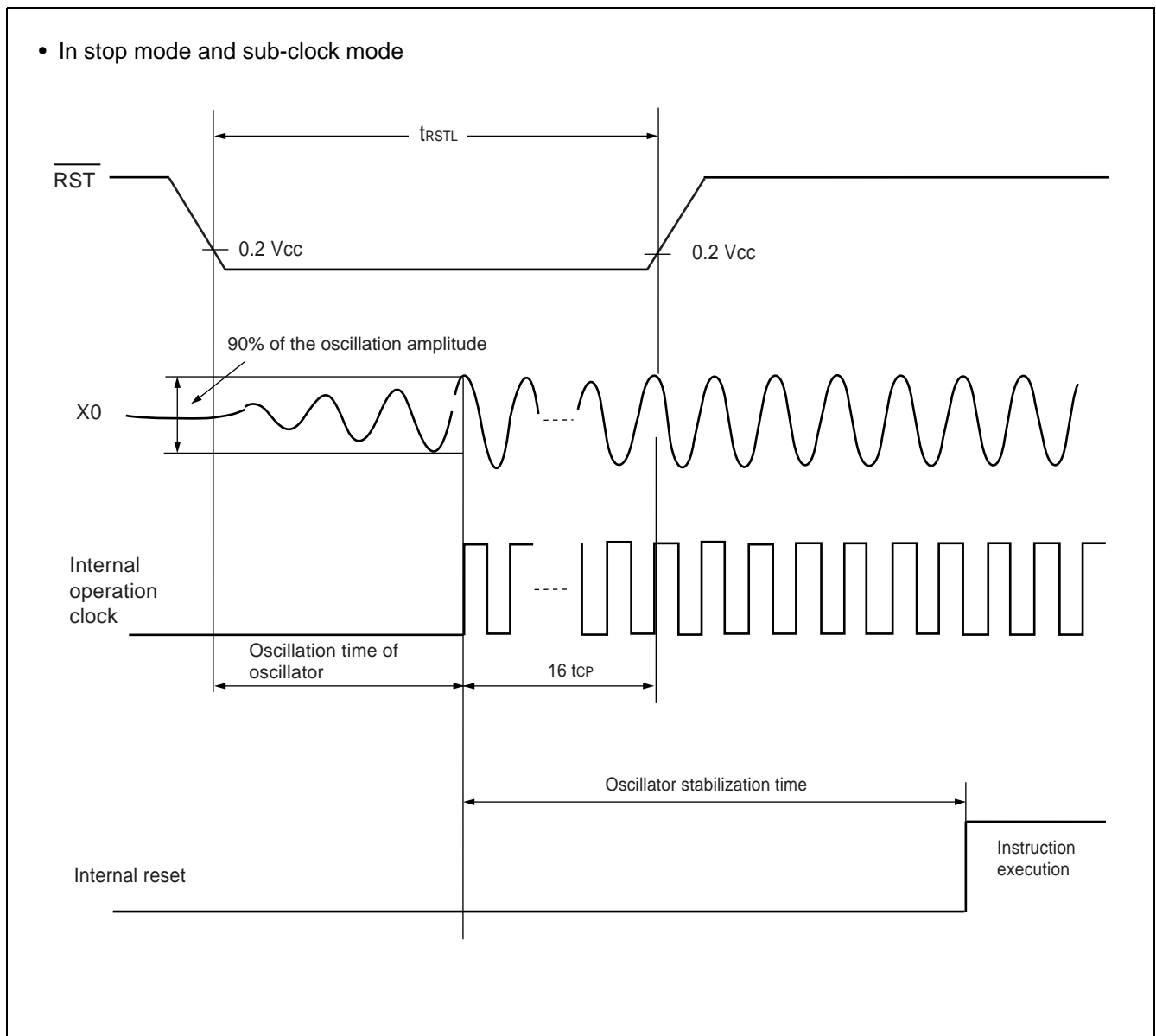
# MB90370 Series

## (2) Reset Input Timing

( $V_{CC} = AV_{CC} = CV_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = CV_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Reset input time	$t_{RSTL}$	$\overline{RST}$	—	16 $t_{CP}$	—	ns	Normal operation
				Oscillation time of oscillator* + 16 $t_{CP}$	—	ms	In stop mode and sub-clock mode

\* : Oscillation time of oscillator is the time to reach to 90% of the oscillation amplitude from stand still. In the crystal oscillator, the oscillation time is between several ms to tens of ms. In ceramic oscillator, the oscillation time is between hundreds of  $\mu\text{s}$  to several ms. In the external clock, the oscillation time is 0 ms.



## (3) Power-on Reset

( $V_{CC} = AV_{CC} = CV_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = CV_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Power supply rise time	$t_R$	$V_{CC}^*$	—	—	50	ms	
Power supply cut-off time	$t_{OFF}$	$V_{CC}^*$	—	1	—	ms	Due to repeated operations

\* :  $V_{CC}$  must be kept lower than 0.2 V before power-on.

Notes : • The above values are used for causing a power-on reset.

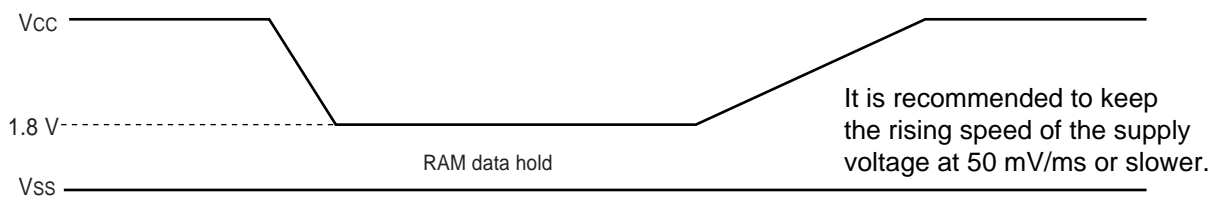
Some registers in the device are initialized only upon a power-on reset. To initialize these registers, turn on the power supply using the above values.

- Make sure that power supply rises within the selected oscillation stabilization time. If the power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.



Sudden changes in the power supply voltage may cause a power-on reset.

To change the power supply voltage while the device is in operation, it is recommended to raise the voltage smoothly to suppress fluctuations as shown below. In this case, change the supply voltage with the PLL clock not used. If the voltage drop is 1 V or fewer per second, however, you can use the PLL clock.



# MB90370 Series

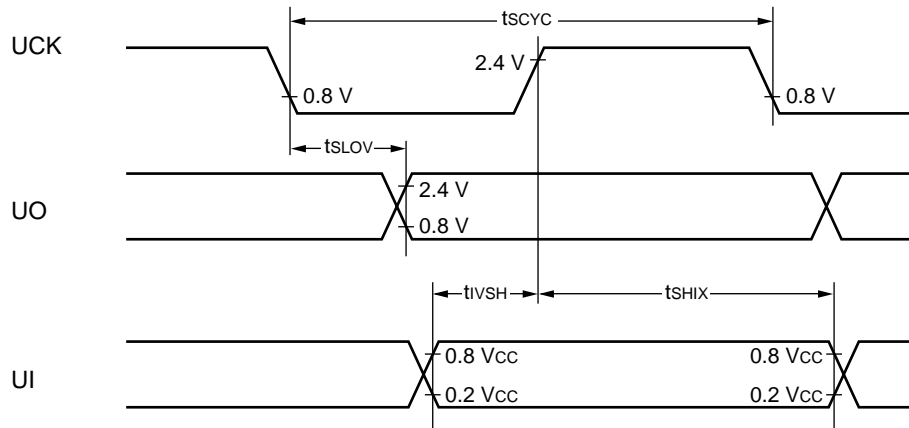
## (4) UART1 to UART3

( $V_{CC} = AV_{CC} = CV_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = CV_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ °C to }+85\text{ °C}$ )

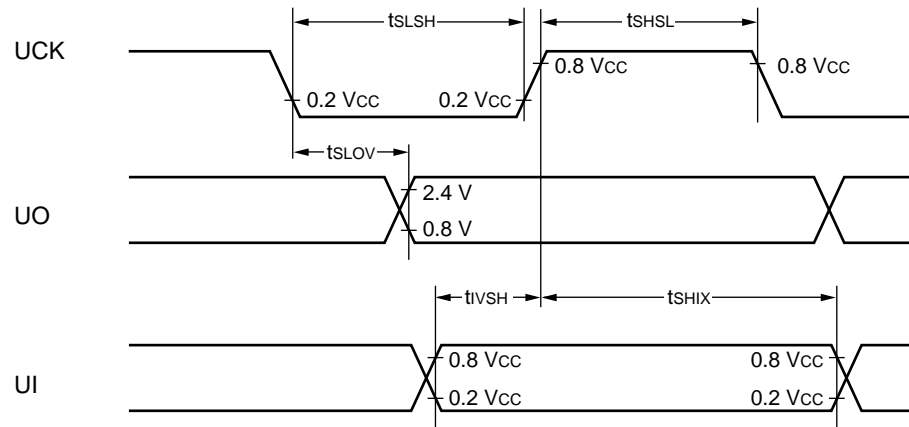
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	$t_{SCYC}$	UCK1 to UCK3	$C_L = 80\text{ pF} + 1\text{ TTL}$ for an output pin of internal shift clock mode	$4 t_{CP}$	—	ns	
UCK ↓ → UO delay time	$t_{SLOV}$	UCK1 to UCK3 UO1 to UO3		-80	+80	ns	
Valid UI → UCK ↑	$t_{IVSH}$	UCK1 to UCK3 UI1 to UI3		100	—	ns	
UCK ↑ → valid UI hold time	$t_{SHIX}$	UCK1 to UCK3 UI1 to UI3		$t_{CP}$	—	ns	
Serial clock "H" pulse width	$t_{SHSL}$	UCK1 to UCK3	$C_L = 80\text{ pF} + 1\text{ TTL}$ for an output pin of external shift clock mode	$2 t_{CP}$	—	ns	
Serial clock "L" pulse width	$t_{SLSH}$	UCK1 to UCK3		$2 t_{CP}$	—	ns	
UCK ↓ → UO delay time	$t_{SLOV}$	UCK1 to UCK3 UO1 to UO3		—	150	ns	
Valid UI → UCK ↑	$t_{IVSH}$	UCK1 to UCK3 UI1 to UI3		60	—	ns	
UCK ↑ → valid UI hold time	$t_{SHIX}$	UCK1 to UCK3 UI1 to UI3		60	—	ns	

- Notes :
- These are AC ratings in the CLK synchronous mode.
  - $C_L$  is the load capacitance value connected to pins while testing.
  - $t_{CP}$  is the internal operating clock cycle time.

- Internal shift clock mode



- External shift clock mode

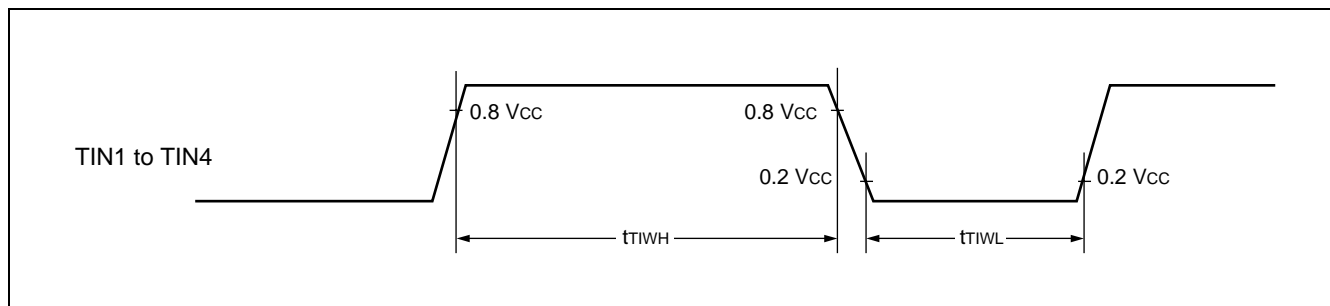


# MB90370 Series

## (5) Resources Input Timing

( $V_{CC} = AV_{CC} = CV_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = CV_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

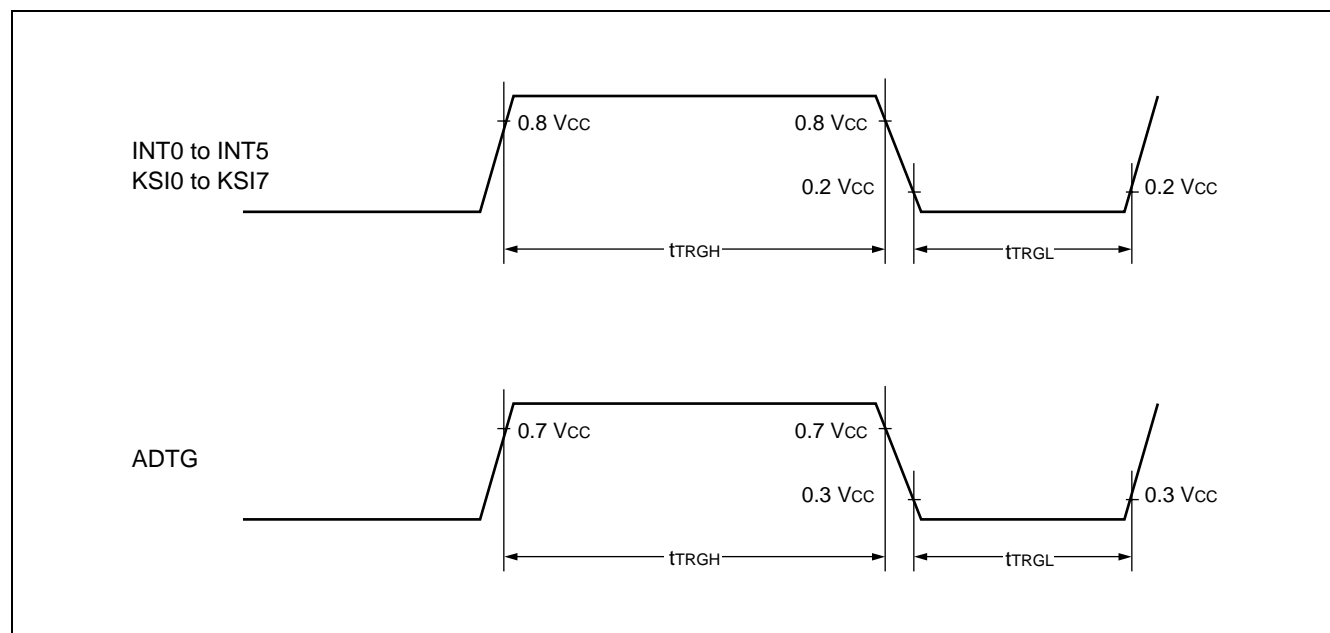
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Timer input pulse width	$t_{TIWH}$ $t_{TIWL}$	TIN1 to TIN4	—	$4 t_{CP}$	—	ns	



## (6) Trigger Input Timing

( $V_{CC} = AV_{CC} = CV_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = CV_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	$t_{TRGH}$	ADTG	—	$5 t_{CP}$	—	ns	Normal operation
	$t_{TRGL}$	INT0 to INT5 KSI0 to KSI7		1	—	$\mu\text{s}$	Stop mode



## (7) I<sup>2</sup>C / MI<sup>2</sup>C Timing

(V<sub>CC</sub> = AV<sub>CC</sub> = CV<sub>CC</sub> = 3.0 V to 3.6 V, V<sub>SS</sub> = AV<sub>SS</sub> = CV<sub>SS</sub> = 0.0 V, T<sub>A</sub> = -40 °C to +85 °C)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Start condition output	t <sub>STA</sub>	SCL SDA	t <sub>CP</sub> (m × n/2 - 1) - 20	t <sub>CP</sub> (m × n/2 - 1) + 20	ns	Master mode
Stop condition output	t <sub>STO</sub>	SCL SDA	t <sub>CP</sub> (m × n/2 + 3) - 20	t <sub>CP</sub> (m × n/2 + 3) + 20	ns	Master mode
Start condition detect	t <sub>STA</sub>	SCL SDA	t <sub>CP</sub> + 40	—	ns	
Stop condition detect	t <sub>STO</sub>	SCL SDA	t <sub>CP</sub> + 40	—	ns	
Restart condition output	t <sub>STASU</sub>	SCL SDA	t <sub>CP</sub> (m × n/2 + 3) - 20	t <sub>CP</sub> (m × n/2 + 3) + 20	ns	Master mode
Restart condition detect	t <sub>STASU</sub>	SCL SDA	t <sub>CP</sub> + 40	—	ns	
SCL output "L" width	t <sub>LOW</sub>	SCL	t <sub>CP</sub> × m × n/2 - 20	t <sub>CP</sub> × m × n/2 + 20	ns	Master mode
SCL output "H" width	t <sub>HIGH</sub>	SCL	t <sub>CP</sub> (m × n/2 + 2) - 20	t <sub>CP</sub> (m × n/2 + 2) + 20	ns	Master mode
SDA output delay	t <sub>DO</sub>	SDA	t <sub>CP</sub> × 3 - 20	t <sub>CP</sub> × 3 + 20	ns	
SDA output setup time after interrupt	t <sub>DOSU</sub> *3	SDA	t <sub>CP</sub> × m × n/2 - 20	—	ns	*1
			t <sub>CP</sub> × 4 - 20	—	ns	*2
SCL input "L" pulse	t <sub>LOW</sub>	SCL	t <sub>CP</sub> × 3 + 40	—	ns	
SCL input "H" pulse	t <sub>HIGH</sub>	SCL	t <sub>CP</sub> + 40	—	ns	
SDA output setup time	t <sub>SU</sub>	SDA	40	—	ns	
SDA hold time	t <sub>HO</sub>	SDA	0	—	ns	

\*1 : At the stop condition or transferring of next byte.

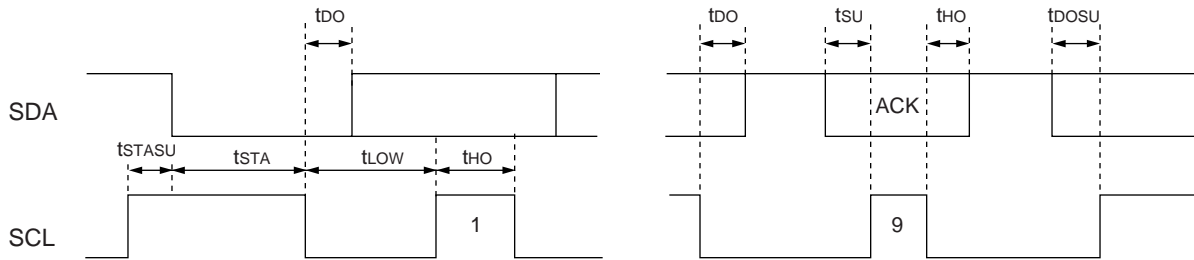
\*2 : After setting register bit IBCRH : SCC/MBCRH : SCC at restart.

\*3 : t<sub>DOSU</sub> is longer than the "L" width of SCL.

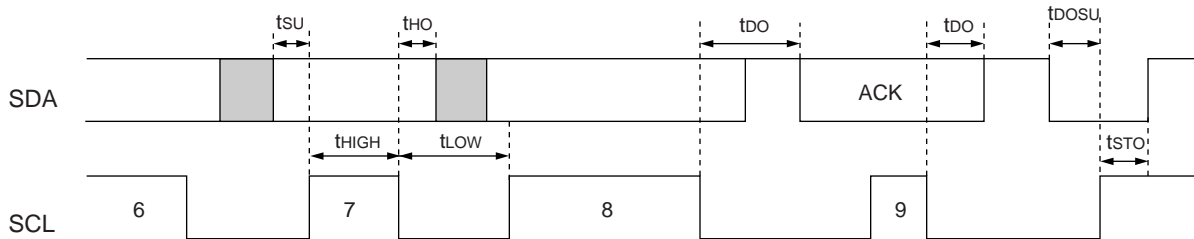
Notes : • t<sub>CP</sub> is the internal operating clock cycle time.

- m is the setting bit of shift clock oscillation defined in the "ICCR register (CS4, CS3)" and "MCCR register (CS4, CS3)". Please refer to the hardware manual for details.
- n is the setting bit of shift clock oscillation defined in the "ICCR register (CS2 to CS0)" and "MCCR register (CS2 to CS0)". Please refer to the hardware manual for details.
- SDA and SCL output value is specified on condition that the rise/fall time is "0 ns".

- Data transmit (master / slave)



- Data receive (master / slave)

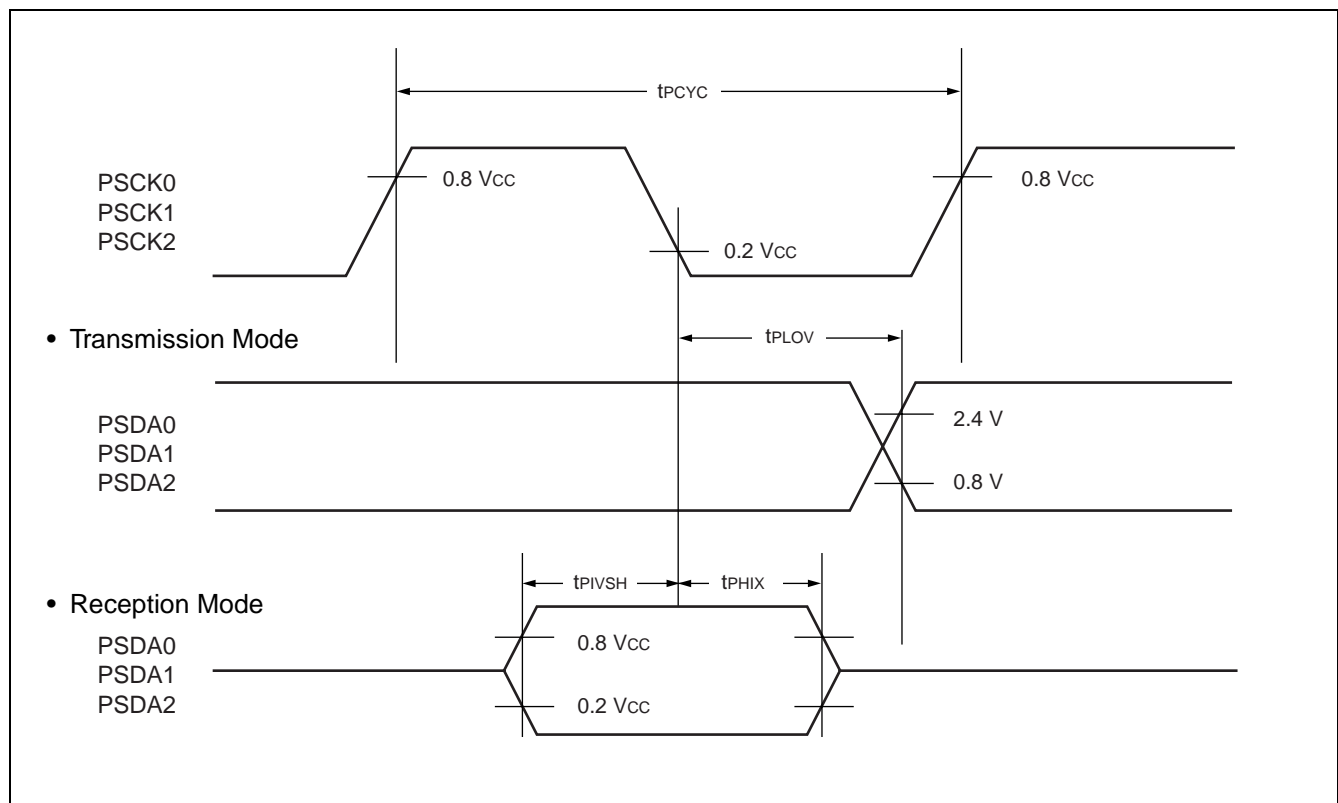


## (8) PS/2 Interface Timing

( $V_{CC} = AV_{CC} = CV_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
PSCK clock cycle time	$t_{PCYC}$	PSCK0 to PSCK2 PSDA0 to PSDA2	—	$4 t_{CP}$	—	—	ns	
PSCK $\downarrow \rightarrow$ PSDA	$t_{PLOV}$	PSCK0 to PSCK2 PSDA0 to PSDA2	Transmission Mode	$2 t_{CP}$	—	—	ns	
Valid PSDA $\rightarrow$ PSCK $\downarrow$	$t_{PIVSH}$	PSCK0 to PSCK2 PSDA0 to PSDA2	Reception Mode	$1 t_{CP}$	—	—	ns	
PSCK $\downarrow \rightarrow$ valid PSDA hold time	$t_{PHIX}$	PSCK0 to PSCK2 PSDA0 to PSDA2		$1 t_{CP}$	—	—	ns	
PSCK clock "H" pulse width	$t_{PHSL}$	PSCK0 to PSCK2 PSDA0 to PSDA2	—	$2 t_{CP}$	—	—	ns	
PSCK clock "L" pulse width	$t_{PLSH}$	PSCK0 to PSCK2 PSDA0 to PSDA2		$2 t_{CP}$	—	—	ns	

Note :  $t_{CP}$  is the internal operating clock cycle time.



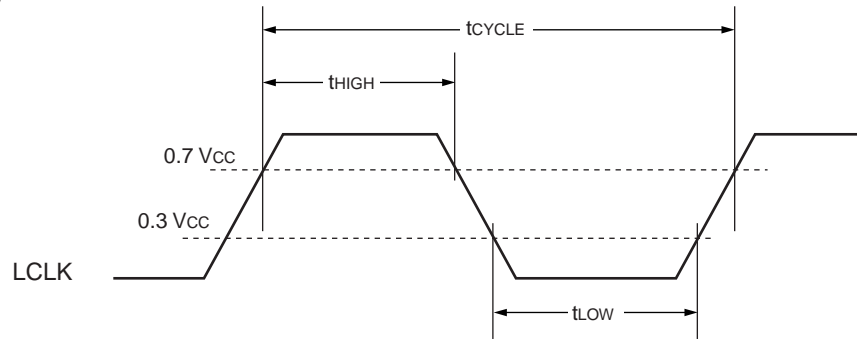
# MB90370 Series

## (9) LPC Timing

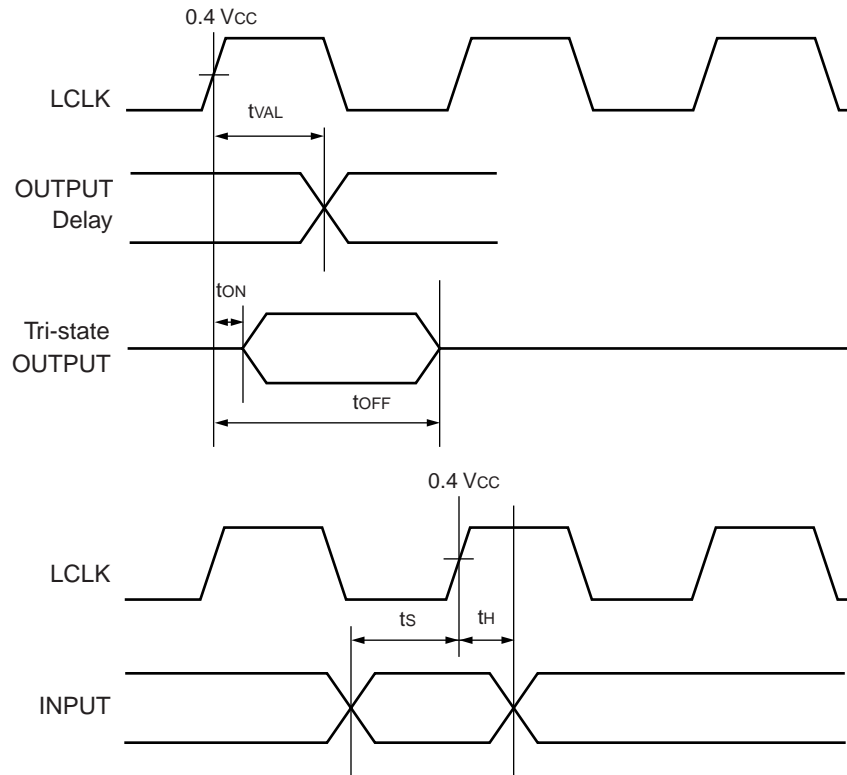
( $V_{CC} = AV_{CC} = CV_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = CV_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
LCLK cycle time	$t_{\text{CYCLE}}$	—	—	30	—	—	ns	
LCLK high time	$t_{\text{HIGH}}$	—	—	12	—	—	ns	
LCLK low time	$t_{\text{LOW}}$	—	—	12	—	—	ns	

LCLK AC timing



LAD,  $\overline{\text{LFRAME}}$ , GA20 AC timing



# MB90370 Series

## 5. A/D Converter Electrical Characteristics

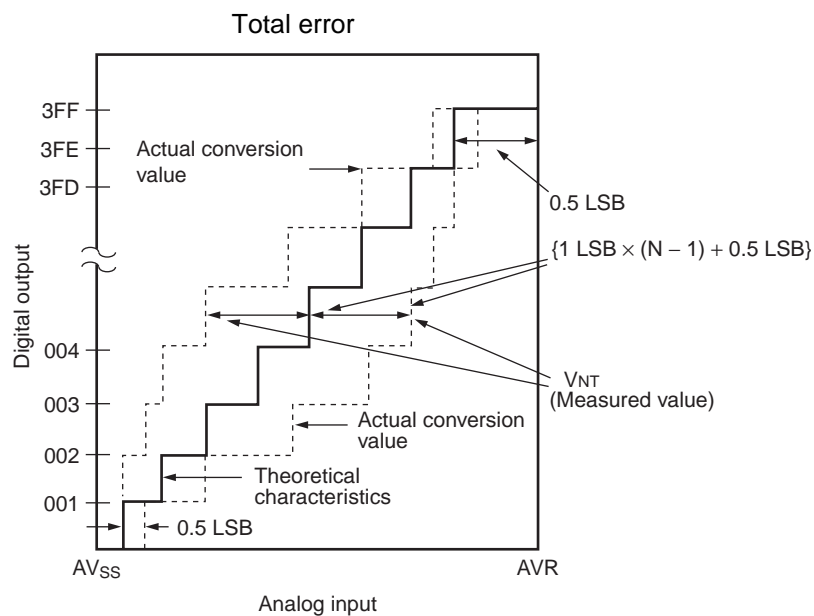
( $2.7\text{ V} \leq \text{AVR} - \text{AV}_{\text{SS}}, V_{\text{CC}} = \text{AV}_{\text{CC}} = \text{CV}_{\text{CC}} = 3.0\text{ V}$  to  $3.6\text{ V}$ ,  $V_{\text{SS}} = \text{AV}_{\text{SS}} = \text{CV}_{\text{SS}} = 0.0\text{ V}$ ,  $T_{\text{A}} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ )

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	—	—	$\pm 3.0$	LSB	
Non-linear error	—	—	—	—	$\pm 2.5$	LSB	
Differential linearity error	—	—	—	—	$\pm 1.9$	LSB	
Zero transition voltage	$V_{\text{OT}}$	AN0 to AN11	$\text{AV}_{\text{SS}} - 1.5\text{ LSB}$	$\text{AV}_{\text{SS}} + 0.5\text{ LSB}$	$\text{AV}_{\text{SS}} + 5.5\text{ LSB}$	V	For MB90V370
					$\text{AV}_{\text{SS}} + 2.5\text{ LSB}$		For MB90F372/372
Full-scale transition voltage	$V_{\text{FST}}$	AN0 to AN11	$\text{AVR} - 3.5\text{ LSB}$	$\text{AVR} - 1.5\text{ LSB}$	$\text{AVR} + 0.5\text{ LSB}$	V	
Conversion time	—	—	3.1	—	—	$\mu\text{s}$	Actual value is specified as a sum of values specified in ADCR0 : CT1, CT0 and ADCR0 : ST1, ST0. Be sure that the setting value is greater than the Min value.
Sampling period	—	—	2	—	—	$\mu\text{s}$	Actual value is specified in ADCR0 : ST1, ST0 bits. Be sure that the setting value is greater than the Min value.
Analog port input current	$I_{\text{AIN}}$	AN0 to AN11	—	0.1	10	$\mu\text{A}$	
Analog input voltage	$V_{\text{AIN}}$	AN0 to AN11	$\text{AV}_{\text{SS}}$	—	AVR	V	
Reference voltage	—	AVR	$\text{AV}_{\text{SS}} + 2.7$	—	$\text{AV}_{\text{CC}}$	V	
Power supply current	$I_{\text{A}}$	$\text{AV}_{\text{CC}}$	—	1.4	6.4	mA	
	$I_{\text{AH}}$		—	—	5	$\mu\text{A}$	*
Reference voltage supply current	$I_{\text{R}}$	AVR	—	94	300	$\mu\text{A}$	
	$I_{\text{RH}}$		—	—	5	$\mu\text{A}$	*
Offset between channels	—	AN0 to AN11	—	—	4	LSB	

\* : The current when the A/D converter is not operating or the CPU is in stop mode (for  $V_{\text{CC}} = \text{AV}_{\text{CC}} = \text{AVR} = 3.0\text{ V}$ ) .

## 6. A/D Converter Glossary

- Resolution : Analog changes that are identifiable with the A/D converter.
- Linearity error : The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1110” ↔ “11 1111 1111”) from actual conversion characteristics.
- Differential linearity error : The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value.
- Total error : The total error is defined as a difference between the actual value and the theoretical value, which includes zero-transition error/full-scale transition error and linearity error.



$$\text{Total error for digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + 0.5 \text{ LSB}\}}{1 \text{ LSB}} \text{ [LSB]}$$

$$1 \text{ LSB} = (\text{Theoretical value}) \frac{AVR - AV_{SS}}{1024} \text{ [V]}$$

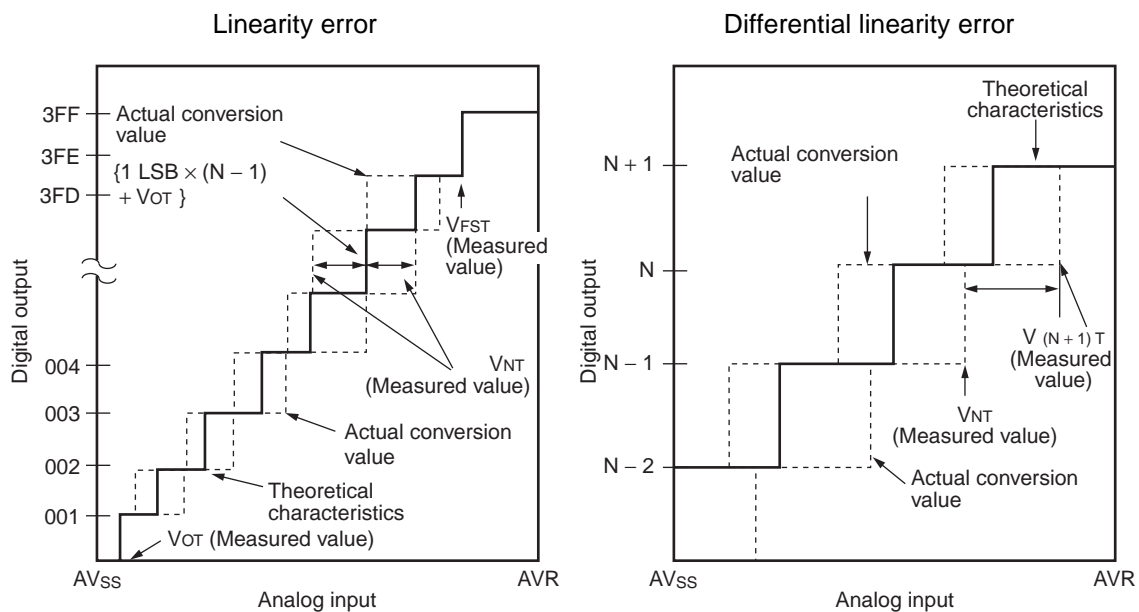
$$V_{OT} (\text{Theoretical value}) = AV_{SS} + 0.5 \text{ LSB [V]}$$

$$V_{FST} (\text{Theoretical value}) = AVR - 1.5 \text{ LSB [V]}$$

$V_{NT}$  : Voltage at a transition of digital output from (N - 1) to N

(Continued)

(Continued)



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + V_{OT}\}}{1 \text{ LSB}} \quad [\text{LSB}]$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}} - 1 \quad [\text{LSB}]$$

$$1 \text{ LSB} = \frac{V_{FST} - V_{OT}}{1022} \quad [\text{V}]$$

$V_{OT}$  : Voltage at transition of digital output from "000<sub>H</sub>" to "001<sub>H</sub>"

$V_{FST}$  : Voltage at transition of digital output from "3FE<sub>H</sub>" to "3FF<sub>H</sub>"

## 7. Notes on Using A/D Converter

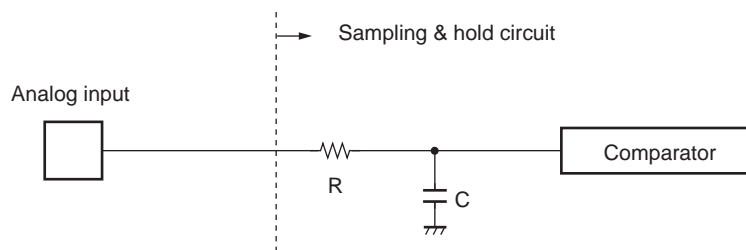
Select the output impedance value for the external circuit of analog input according to the following conditions.

Output impedance values of the external circuit of 4 kΩ or lower are recommended.

When capacitors are connected to external pins, the capacitance of several thousand times the internal capacitor value is recommended to minimized the effect of voltage distribution between the external capacitor and internal capacitor.

When the output impedance of the external circuit is too high, the sampling period for analog voltages may not be sufficient.

- Equipment of analog input circuit model



R : about 1.9 kΩ  
C : about 32.3 pF

Note : Listed values must be considered as standards.

- Error

The smaller the  $|AVR - AV_{SS}|$  is, the greater the error would become relatively.

## 8. D/A Electrical Characteristics

( $V_{CC} = AV_{CC} = CV_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = CV_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ °C to }+85\text{ °C}$ )

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Resolution	—	—	—	—	8	—	bit	
Differential linearity error	—	—		—	—	±0.9	LSB	
Non-linearity error	—	—		—	—	±1.5	LSB	
Conversion time	—	—		—	0.6	—	μs	*
Analog output impedance	—	—		2.0	2.9	3.8	kΩ	
Power supply	$I_{DVR}$	$AV_{CC}$		—	—	460	μA	
Current	$I_{DVRs}$	$AV_{CC}$		—	0.1	—	μA	D/A stops

\* : With load capacitance is 20 pF.

# MB90370 Series

## 9. Comparator Electrical Characteristics

( $V_{CC} = AV_{CC} = CV_{CC} = 3.3 \text{ V to } 3.6 \text{ V}$ ,  $V_{SS} = AV_{SS} = CV_{SS} = 0.0 \text{ V}$ ,  $T_A = -40 \text{ }^\circ\text{C to } +85 \text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Reference voltage	—	CVRH2	—	1.1	—	2.9	V	
		CVRH1		CVRL	—	2.9	V	
		CVRL		1.1	—	CVRH1	V	
Reference voltage supply current	$I_{CR}$	CVRH2 CVRH1 CVRL	—	—	—	$\pm 1$	$\mu\text{A}$	
Comparator supply current	$I_{CV}$	$CV_{CC}$	—	—	—	50	$\mu\text{A}$	active
				—	—	10	$\mu\text{A}$	inactive
Analog input voltage	$V_{IH}$	DCIN DCIN2 VOL1 to VOL3 VSI1 to VSI3	—	$CV_{SS}$	—	$CV_{CC}$	V	

## 10. Serial IRQ Electrical Characteristics

( $V_{CC} = AV_{CC} = CV_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$ ,  $V_{SS} = AV_{SS} = CV_{SS} = 0.0 \text{ V}$ ,  $T_A = -40 \text{ }^\circ\text{C to } +85 \text{ }^\circ\text{C}$ )

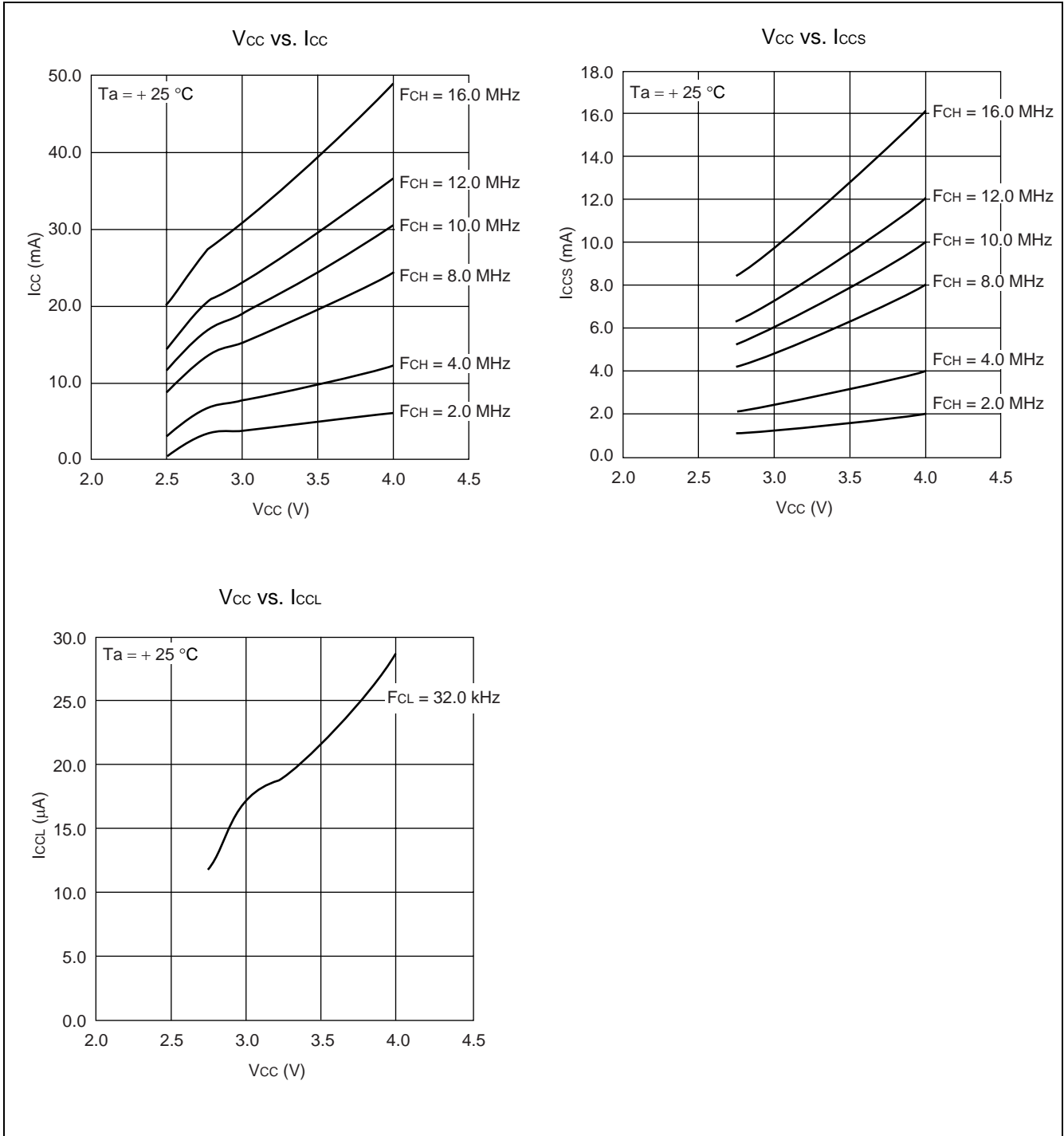
Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	$V_{IH}$	—	—	$0.7V_{CC}$	—	$V_{CC}$	V	
"L" level input voltage	$V_{IL}$	—	—	$V_{SS}$	—	$0.3V_{CC}$	V	
"H" level output voltage	$V_{OH}$	—	—	$V_{CC} - 0.5$	—	—	V	
"L" level output voltage	$V_{OL}$	—	—	—	—	0.4	V	

## 11. Flash Memory Program/Erase Characteristics

Parameter	Condition	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	$T_A = +25 \text{ }^\circ\text{C}$ $V_{CC} = 3.0 \text{ V}$	—	1	15	s	Excludes 00 <sub>H</sub> programming prior to erasure
Chip erase time		—	4	—	s	Excludes 00 <sub>H</sub> programming prior to erasure
Word (16 bit width) programming time		—	16	3,600	$\mu\text{s}$	Except for the over head time of the system
Program/Erase cycle	—	10,000	—	—	cycle	

## EXAMPLE CHARACTERISTICS

- MB90F372

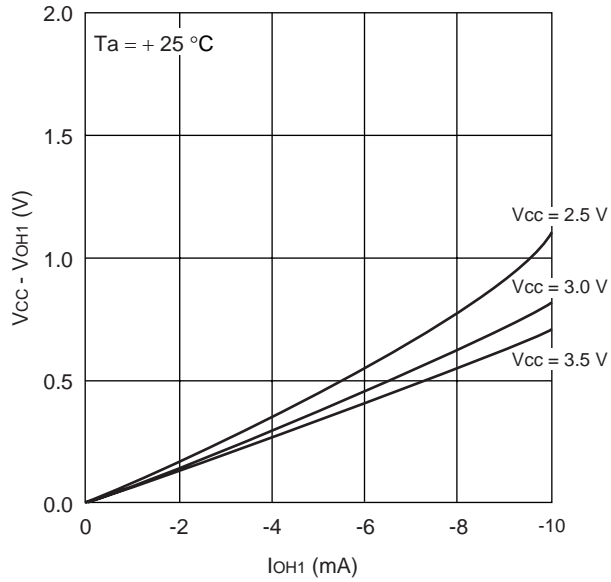


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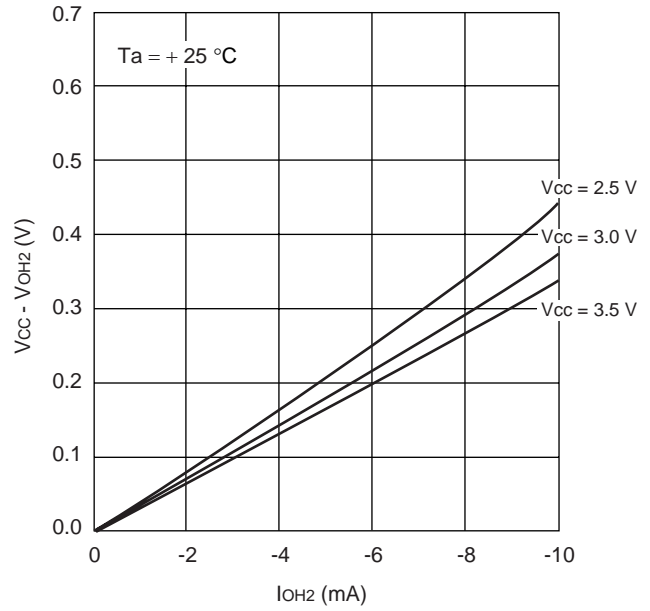
# MB90370 Series

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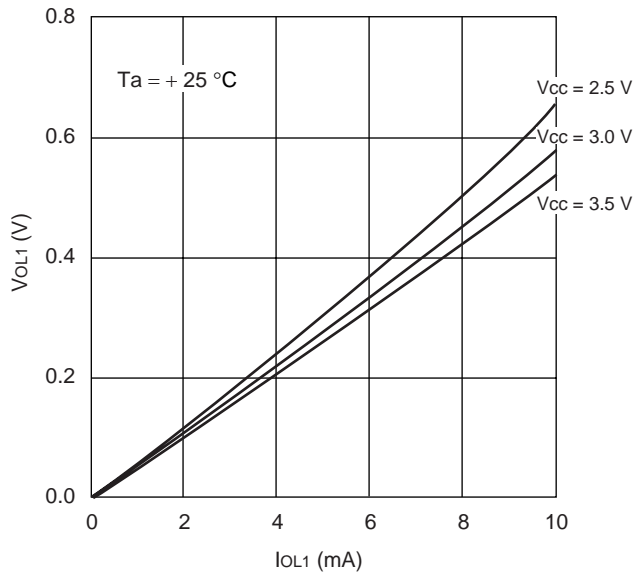
$I_{OH1}$  vs.  $V_{CC} - V_{OH1}$



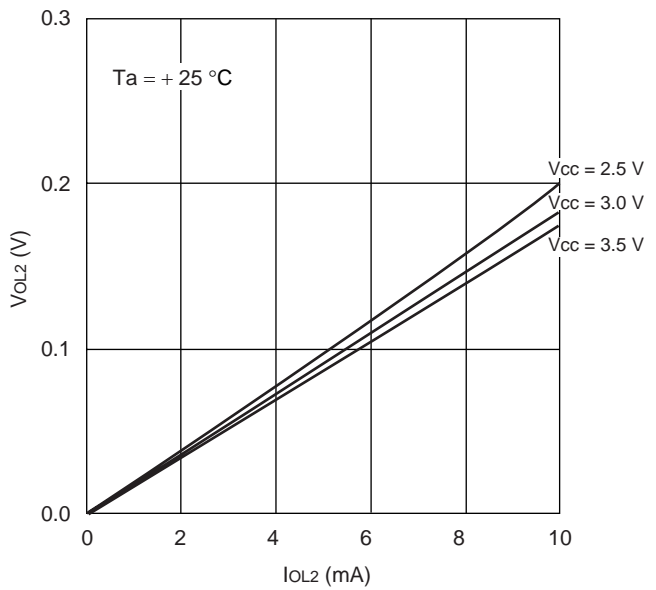
$I_{OH2}$  vs.  $V_{CC} - V_{OH2}$



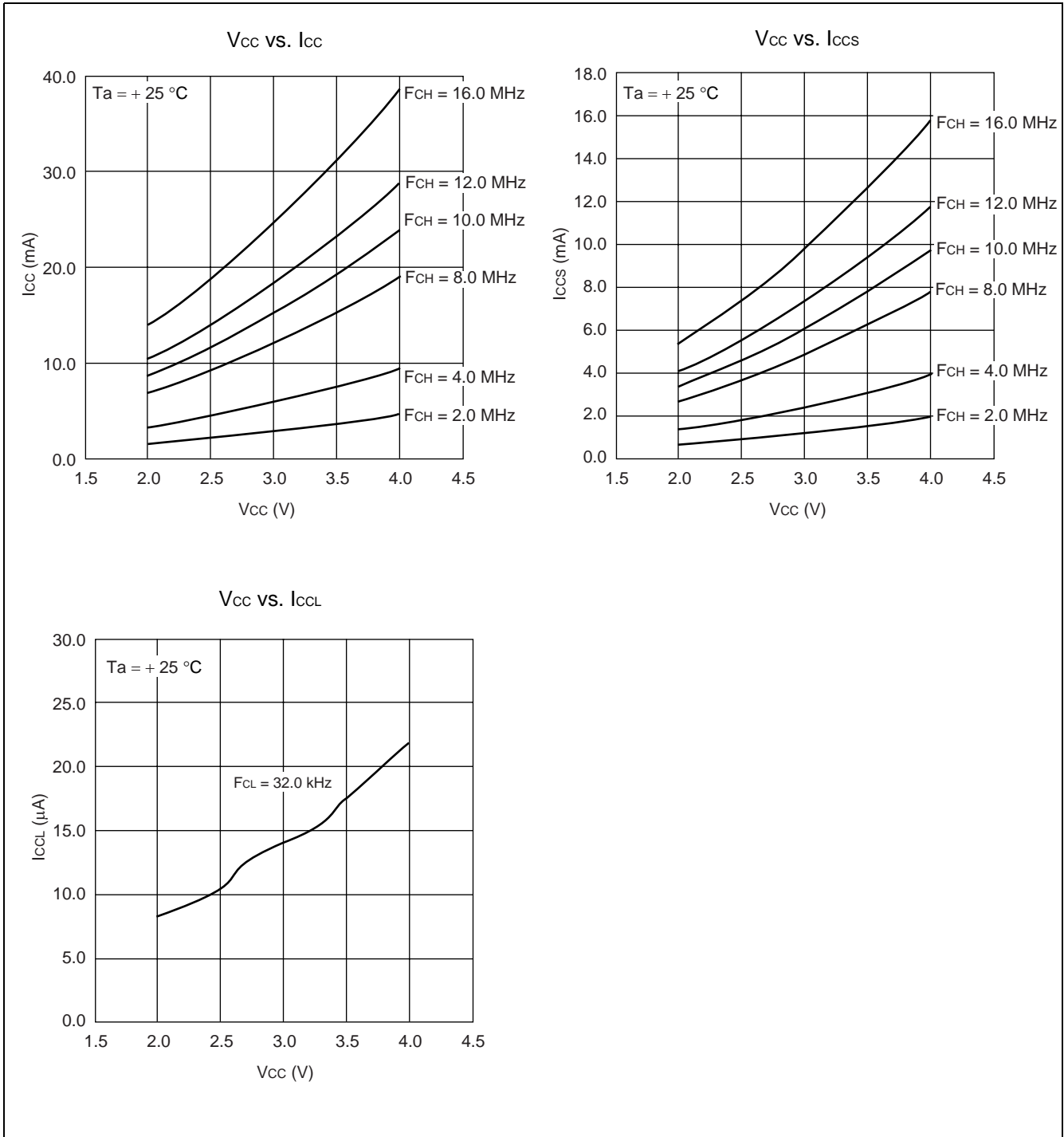
$I_{OL1}$  vs.  $V_{OL1}$



$I_{OL2}$  vs.  $V_{OL2}$



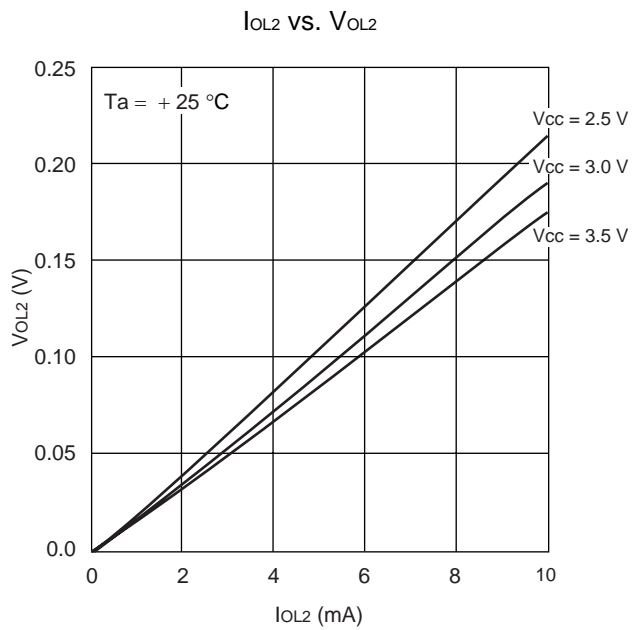
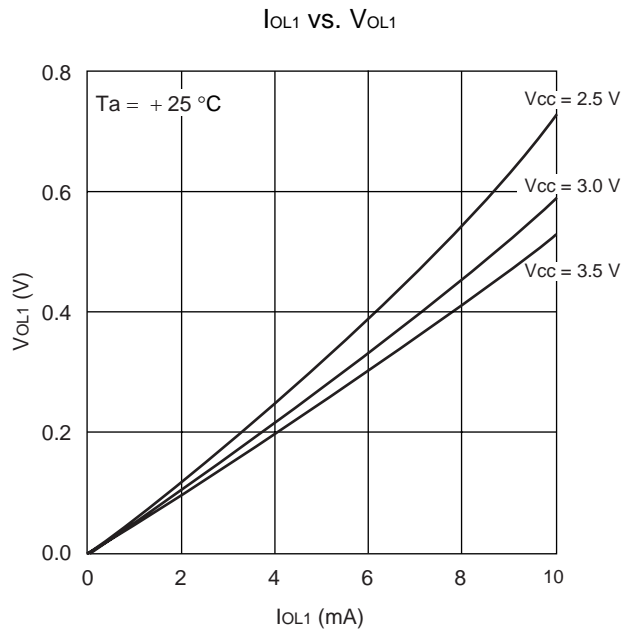
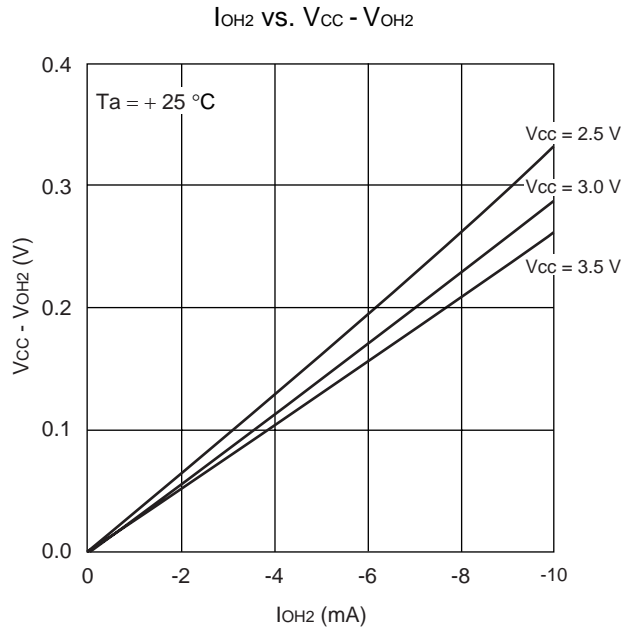
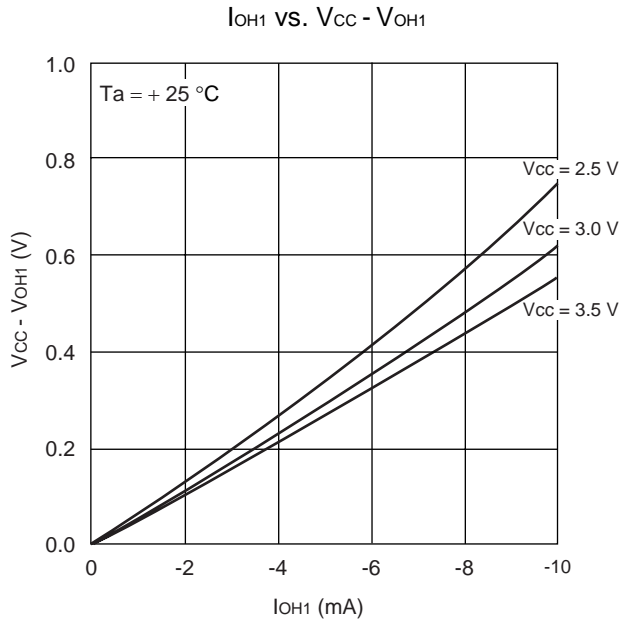
• MB90372



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# MB90370 Series

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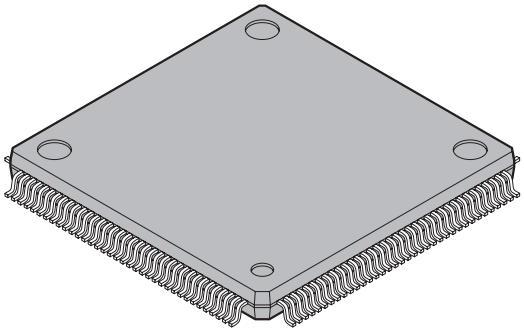


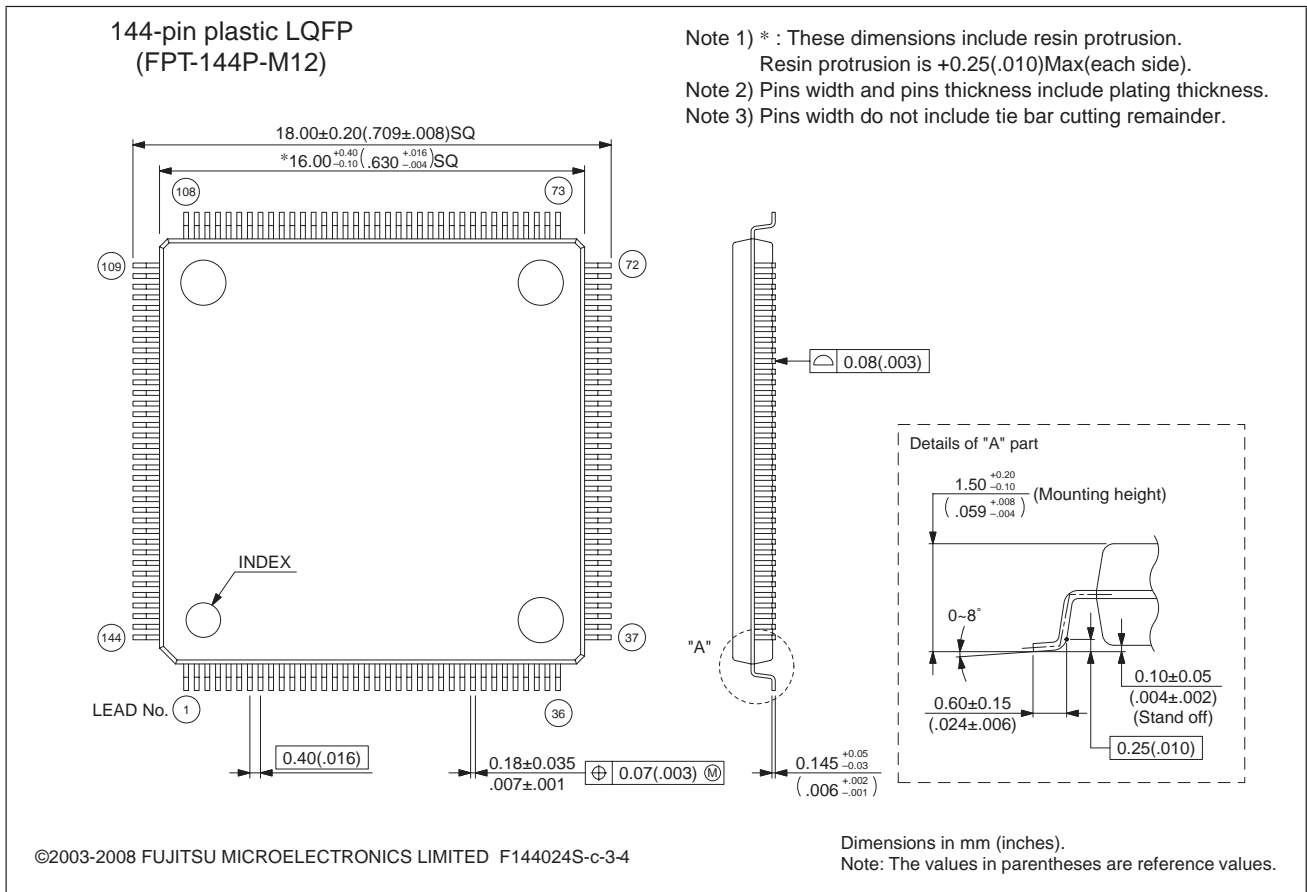
## ■ ORDERING INFORMATION

Part number	Package	Remarks
MB90F372PFF-G MB90372PFF-G-XXX	144-pin Plastic LQFP (FPT-144P-M12)	XXX is the ROM release number.

# MB90370 Series

## PACKAGE DIMENSION

<p>144-pin plastic LQFP</p>  <p>(FPT-144P-M12)</p>	Lead pitch	0.40 mm
	Package width × package length	16.0 × 16.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.88 g
	Code (Reference)	P-LFQFP144-16×16-0.40



Please check the latest package dimensions at the following URL.  
<http://edevice.fujitsu.com/package/en-search/>

## ■ MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
—	—	Changed the series name; (MB90370/365 → MB90370 series)
—	—	Deleted the part numbers; MB90F377
3	■ PRODUCT LINEUP	Changed a name of Low-power consumption (Standby) mode. TBT → Time-base timer
114	■ ELECTRICAL CHARACTERISTICS 4. AC Characteristics (1) Clock Timings	Changed the “Clock frequency”. (maximum value of External clock : 32MHz → 16MHz) (Added the maximum value when PLL is used.)
120	■ ELECTRICAL CHARACTERISTICS 4. AC Characteristics (4) UART1 to UART3	Changed the minimum value of “Serial clock cycle time”. $8t_{CP} \rightarrow 4t_{CP}$
		Changed the minimum value of “Serial clock pulse width”. $4t_{CP} \rightarrow 2t_{CP}$
128	■ ELECTRICAL CHARACTERISTICS 5. A/D Converter Electrical Characteristics	Changed the unit of “Zero transition voltage” and “Full-scale transition voltage”. mV → V

The vertical lines marked in the left side of the page show the changes.

# MB90370 Series

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