FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-13722-11E

16-bit Microcontroller

CMOS

F²MC-16LX MB90480B/485B Series

MB90F481B/F482B/487B/488B/483C
MB90F488B/F489B/V480B/V485B

■ DESCRIPTION

The MB90480B/485B series is a 16-bit general-purpose FUJITSU SEMICONDUCTOR microcontroller designed for process control in consumer devices and other applications requiring high-speed real-time processing.

The F²MC-16LX CPU core instruction set retains the AT architecture of the F²MC*1 family, with additional instructions for high-level languages, expanded addressing mode, enhanced multiply-drive instructions, and complete bit processing. In addition, a 32-bit accumulator is provided to enable long-word processing.

The MB90480B/485B series features embedded peripheral resources including 8/16-bit PPG, expanded I/O serial interface, UART, 10-bit A/D converter, 16-bit I/O timer, 8/16-bit up/down-counter, PWC timer, I²C interface, DTP/external interrupt, chip select, and 16-bit reload timer.

*1 : F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

■ FEATURES

- Clock
  Minimum instruction execution time: 40.0 ns/6.25 MHz base frequency multiplied × 4 (25 MHz internal operating frequency/3.3 V ± 0.3 V)
  62.5 ns/4 MHz base frequency multiplied × 4 (16 MHz internal operating frequency/3.0 V ± 0.3 V) PLL clock multiplier
- Maximum memory space: 16 Mbytes

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The information for microcontroller supports is shown in the following homepage.
Be sure to refer to the "Check Sheet" for the latest cautions on development.

"Check Sheet" is seen at the following support page

"Check Sheet" lists the minimal requirement items to be checked to prevent problems beforehand in system development.

http://edevice.fujitsu.com/micom/en-support/

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- Instruction set optimized for controller applications
  Supported data types (bit, byte, word, or long word)
  Typical addressing modes (23 types)
  32-bit accumulator for enhanced high-precision calculation
  Enhanced signed multiplication/division instruction and RETI instruction functions
- Instruction set designed for high-level programming language (C) and multi-task operations
  System stack pointer adopted
  Instruction set symmetry and barrel shift instructions
- Non-multiplex bus/multiplex bus compatible
- Enhanced execution speed
  4-byte instruction queue
- Enhanced interrupt functions
  8 levels setting with programmable priority, 8 external interrupts
- Data transfer function (μDMAC)
  Up to 16 channels
- Embedded ROM
  Flash versions : 192 Kbytes, 256 Kbytes, 384 Kbytes, MASK versions : 192 Kbytes, 256 Kbytes
- Embedded RAM
  Flash versions : 4 Kbytes, 6 Kbytes, 10 Kbytes, 24 Kbytes, MASK versions : 10 Kbytes, 16 Kbytes
- General purpose ports
  Up to 84 ports
  (Includes 16 ports with input pull-up resistance settings, 16 ports with output open-drain settings)
- A/D converter
  8-channel RC sequential comparison type (10-bit resolution, 3.68 μs conversion time (at 25 MHz))
- I^2C interface (MB90485B series only) : 1channel, P76/P77 N-ch open drain pin (without P-ch)
  Do not apply high voltage in excess of recommended operating ranges to the N-ch open drain pin (with P-ch) in MB90V485B.
- μPG (MB90485B series only) : 1 channel
- UART : 1 channel
- Extended I/O serial interface (SIO) : 2 channels
- 8/16-bit PPG : 3 channels (with 8-bit × 6 channel/16-bit × 3 channel mode switching function)
- 8/16-bit up/down counter/timer: 1 channel (with 8-bit × 2 channels/16-bit × 1-channel mode switching function)
- PWC (MB90485B series only) : 3 channels (Capable of compare the inputs to two of the three)
- 3 V/5 V I/F pin (MB90485B series only)
  P20 to P27, P30 to P37, P40 to P47, P70 to P77
- 16-bit reload timer : 1 channel
- 16-bit I/O timer : 2 channels input capture, 6 channels output compare, 1 channel free-run timer
- On chip dual clock generator system
- Low-power consumption mode
  With stop mode, sleep mode, CPU intermittent operation mode, watch mode, timebase timer mode
- Packages : QFP 100/LQFP 100
- Process : CMOS technology
- Power supply voltage : 3 V, single power supply (some ports can be operated by 5 V power supply at MB90485B series)

■ PRODUCT LINEUP

• MB90480B series

Item \ Part number		MB90F481B	MB90F482B	MB90V480B
Classification		Flash memory product		Evaluation product
ROM size		192 Kbytes	256 Kbytes	—
RAM size		4 Kbytes	6 Kbytes	16 Kbytes
CPU function		Number of instructions : 351 Instruction bit length : 8-bit, 16-bit Instruction length : 1 byte to 7 bytes Data bit length : 1-bit, 8-bit, 16-bit Minimum instruction execution time : 40 ns (25 MHz machine clock)		
Ports		General-purpose I/O ports: up to 84 General-purpose I/O ports (CMOS output) General-purpose I/O ports (with pull-up resistance) General-purpose I/O ports (N-ch open drain output)		
UART		1 channel, start-stop synchronized		
8/16-bit PPG		8-bit × 6 channels/16-bit × 3 channels		
8/16-bit up/down counter/timer		Event input pins : 6, 8-bit up/down counters : 2 8-bit reload/compare registers : 2		
16-bit I/O timers	16-bit free-run timer	Number of channels : 1 Overflow interrupt		
	Output compare (OCU)	Number of channels : 6 Pin input factor : A match signal of compare register		
	Input capture (ICU)	Number of channels : 2 Rewriting a register value upon a pin input (rising, falling, or both edges)		
DTP/external interrupt circuit		Number of external interrupt pin channels : 8 (edge or level detection)		
Extended I/O serial interface		Embedded 2 channels		
Timebase timer		18-bit counter Interrupt cycles: 1.0 ms, 4.1 ms, 16.4 ms, 131.1 ms (at 4 MHz base oscillator)		
A/D converter		Conversion resolution : 8/10-bit, switchable One-shot conversion mode (converts selected channel 1 time only) Scan conversion mode (conversion of multiple consecutive channels, programmable up to 8 channels) Continuous conversion mode (repeated conversion of selected channels) Stop conversion mode (conversion of selected channels with repeated pause)		
Watchdog timer		Reset generation interval : 3.58 ms, 14.33 ms, 57.23 ms, 458.75 ms (minimum value, at 4 MHz base oscillator)		
Low-power consumption (standby) modes		Stop mode, sleep mode, CPU intermittent operation mode, watch mode, timebase timer mode		
Process		CMOS		
Type		Not included security function		User pin*1, 3 V/5 V versions
Emulator power supply*2		—		Included

*1 : User pin : P20 to P27, P30 to P37, P40 to P47, P70 to P77

*2 : It is setting of Jumper switch (TOOL VCC) when emulator (MB2147-01) is used. Please refer to the MB2147-01 or MB2147-20 hardware manual (3.3 Emulator-dedicated Power Supply switching) about details.

Note : Ensure that you must write to Flash at V_{CC} = 3.13 V to 3.60 V (3.3 V + 10%, –5%) .

• **MB90485B series**

Item \ Part number	MB90487B	MB90488B	MB90F488B	MB90V485B	MB90F489B	MB90483C
Classification	MASK ROM product		Flash memory product	Evaluation product	Flash memory product	MASK ROM product
ROM size	192 Kbytes	256 Kbytes	256 Kbytes	—	384 Kbytes	256 Kbytes
RAM size	10 Kbytes	10 Kbytes	10 Kbytes	16 Kbytes	24 Kbytes	16 Kbytes
CPU function	Number of instructions : 351 Instruction bit length : 8-bit, 16-bit Instruction length : 1 byte to 7 bytes Data bit length : 1-bit, 8-bit, 16-bit Minimum instruction execution time : 40 ns (25 MHz machine clock)					
Ports	General-purpose I/O ports : up to 84 General-purpose I/O ports (CMOS output) General-purpose I/O ports (with pull-up resistance) General-purpose I/O ports (N-ch open drain output)					
UART	1 channel, start-stop synchronized					
8/16-bit PPG	8-bit × 6 channels/16-bit × 3 channels					
8/16-bit up/down counter/timer	Event input pins : 6, 8-bit up/down counters : 2 8-bit reload/compare registers : 2					
16-bit I/O timers — 16-bit free-run timer	Number of channels : 1 Overflow interrupt					
16-bit I/O timers — Output compare (OCU)	Number of channels : 6 Pin input factor: A match signal of compare register					
16-bit I/O timers — Input capture (ICU)	Number of channels : 2 Rewriting a register value upon a pin input (rising, falling, or both edges)					
DTP/external interrupt circuit	Number of external interrupt pin channels: 8 (edge or level detection)					
Extended I/O serial interface	Embedded 2 channels					
I^2C interface*2	1 channel					
µPG	1 channel					
PWC	3 channels					
Timebase timer	18-bit counter Interrupt cycles : 1.0 ms, 4.1 ms, 16.4 ms, 131.1 ms (at 4 MHz base oscillator)					
A/D converter	Conversion resolution : 8/10-bit, switchable One-shot conversion mode (converts selected channel 1 time only) Scan conversion mode (conversion of multiple consecutive channels, programmable up to 8 channels) Continuous conversion mode (repeated conversion of selected channels) Stop conversion mode (conversion of selected channels with repeated pause)					

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Item \ Part number	MB90487B	MB90488B	MB90F488B	MB90V485B	MB90F489B	MB90483C
Watchdog timer	Reset generation interval: 3.58 ms, 14.33 ms, 57.23 ms, 458.75 ms (minimum value, at 4 MHz base oscillator)					
Low-power consumption (standby) modes	Stop mode, sleep mode, CPU intermittent operation mode, watch timer mode, timebase timer mode					
Process	CMOS					
Type	3 V/5 V power supply*1	3 V/5 V power supply*1	3 V/5 V power supply*1 Included security function	3 V/5 V power supply*1	3 V/5 V power supply*1 Included security function	3 V/5 V power supply*1
Emulator power supply*3	—	—	—	Included	—	—

*1 : 3 V/5 V I/F pin : All pins should be for 3 V power supply without P20 to P27, P30 to P37, P40 to P47, and P70 to P77.

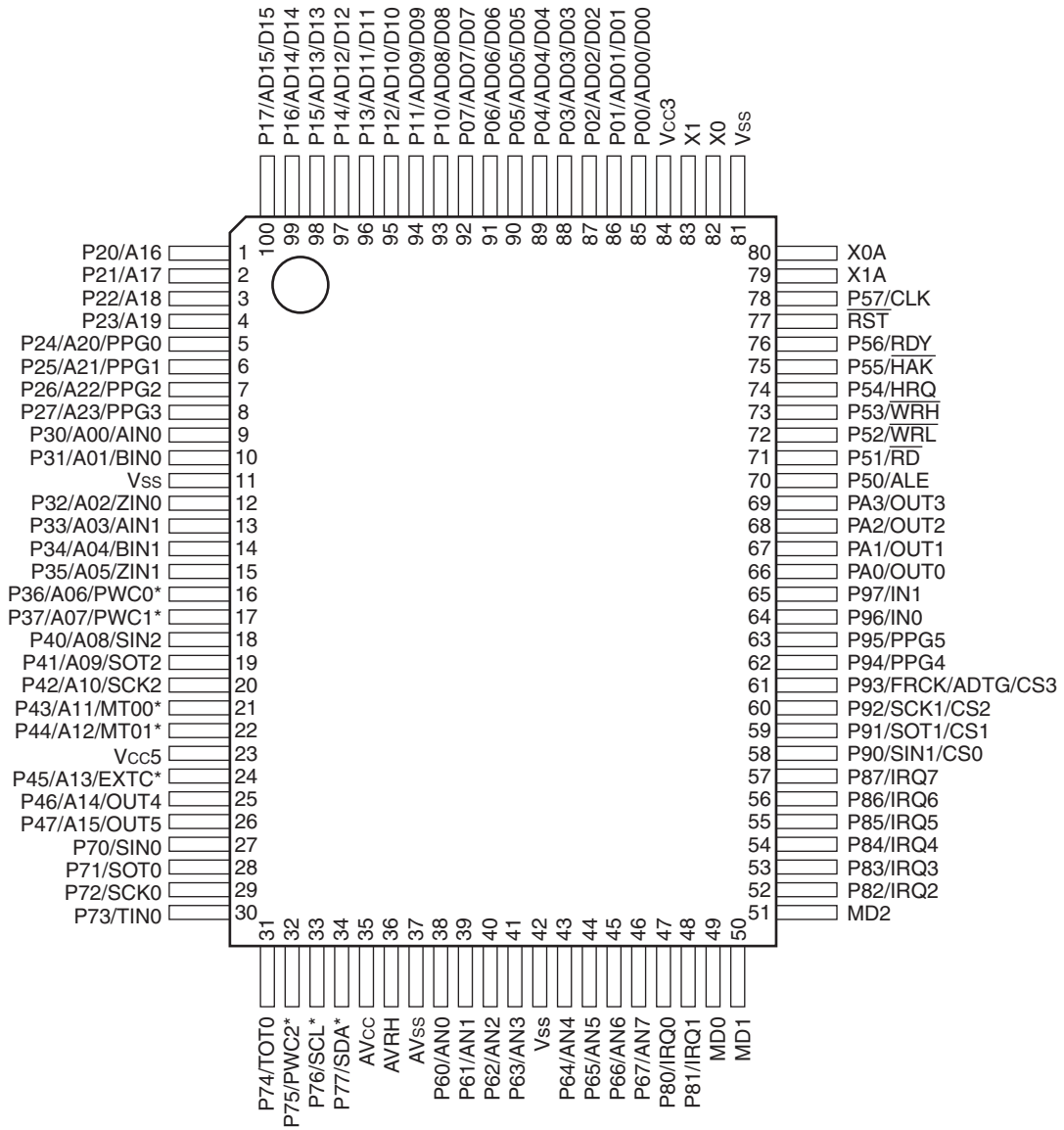
*2 : P76/P77 pins are N-ch open drain pins (without P-ch) at built-in I²C. However, MB90V485B uses the N-ch open drain pin (with P-ch) .

*3 : It is setting of Jumper switch (TOOL VCC) when emulator (MB2147-01) is used.
Please refer to the MB2147-01 or MB2147-20 hardware manual (3.3 Emulator-dedicated Power Supply Switching) about details.

Notes :
- As for MB90V485B, input pins (PWC0, PWC1, PWC2/EXTC/SCL and SDA pins) for PWC/µPG/I²C become CMOS input.
- Ensure that you must write to Flash at V_{CC} = 3.13 V to 3.60 V (3.3 V + 10%, – 5%) .

■ PIN ASSIGNMENT

(TOP VIEW)



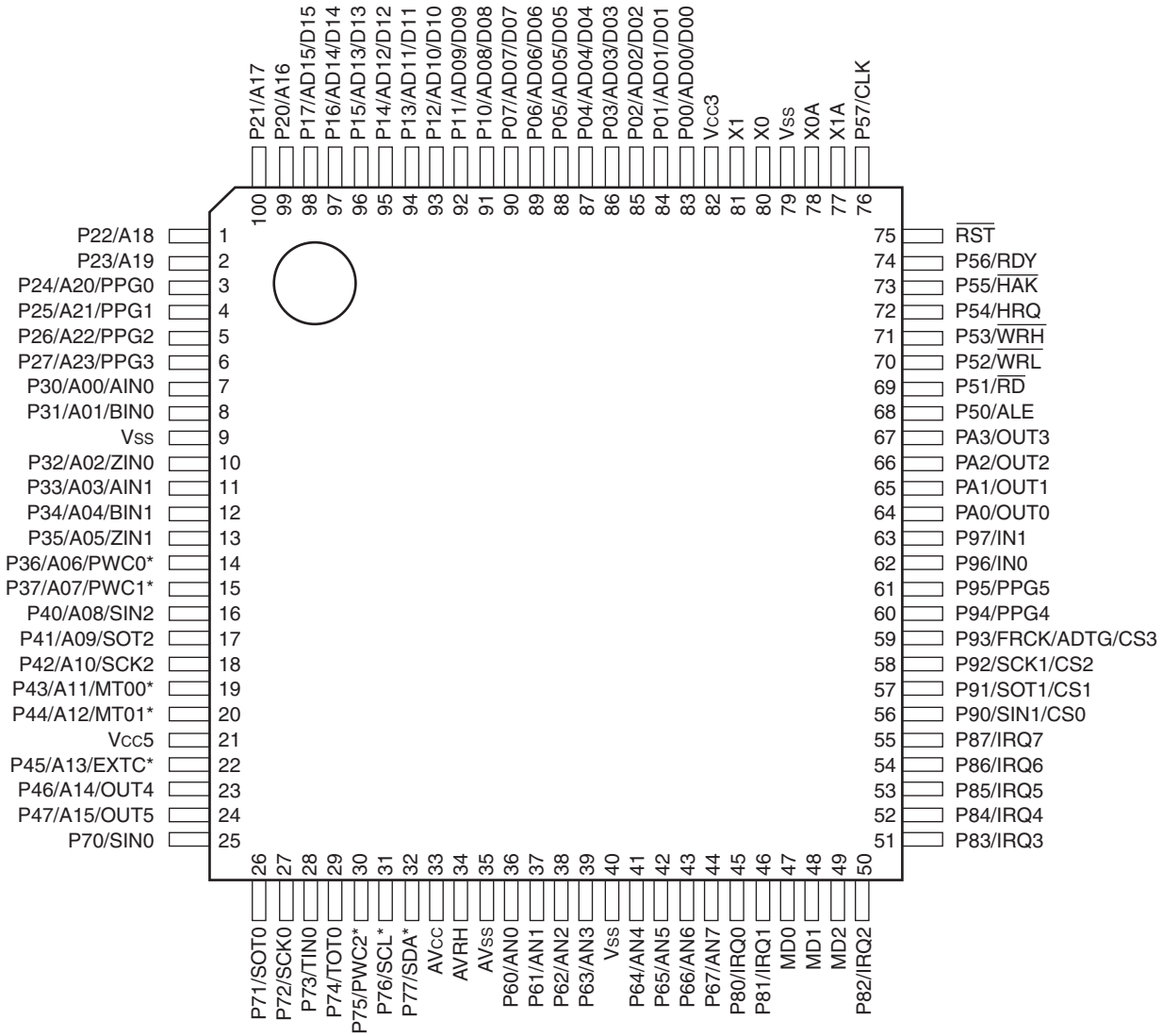
(FPT-100P-M06)

* : These are the pins for MB90485B series. The pins for MB90480B series are P36/A06, P37/A07, P43/A11, P44/A12, P45/A13, P75 to P77.

Note : MB90485B series only

- I²C pin P77 and P76 are N-ch open drain pin (without P-ch) . However, MB90V485B uses the N-ch open drain pin (with P-ch) .
- P20 to P27, P30 to P37, P40 to P47 and P70 to P77 are also used as 3 V/5 V I/F pin.
- As for MB90V485B, input pins (PWC0, PWC1, PWC2/EXTC/SCL and SDA pins) for PWC/μPG/I²C become CMOS input.

(TOP VIEW)



(FPT-100P-M20)

* : These are the pins for MB90485B series. The pins for MB90480B series are P36/A06, P37/A07, P43/A11, P44/A12, P45/A13, P75 to P77.

Note : MB90485B series only

- I²C pin P77 and P76 are N-ch open drain pin (without P-ch) . However, MB90V485B uses the N-ch open drain pin (with P-ch) .
- P20 to P27, P30 to P37, P40 to P47 and P70 to P77 are also used as 3 V/5 V I/F pin.
- As for MB90V485B, input pins (PWC0, PWC1, PWC2/EXTC/SCL and SDA pins) for PWC/µPG/I²C become CMOS input.

■ PIN DESCRIPTIONS

Pin No.		Pin name	I/O circuit type*3	Function
QFP*1	LQFP*2			
82	80	X0	A	Clock (oscillator) input pin
83	81	X1	A	Clock (oscillator) output pin
80	78	X0A	A	Clock (32 kHz oscillator) input pin
79	77	X1A	A	Clock (32 kHz oscillator) output pin
77	75	$\overline{\text{RST}}$	B	Reset input pin
85 to 92	83 to 90	P00 to P07	C (CMOS)	This is a general purpose I/O port. A setting in the port 0 input resistance register (RDR0) can be used to apply pull-up resistance (RD00-RD07 = “1”) . (Disabled when pin is set for output.)
		AD00 to AD07		In multiplex mode, these pins function as the external address/data bus low I/O pins.
		D00 to D07		In non-multiplex mode, these pins function as the external data bus low output pins.
93 to 100	91 to 98	P10 to P17	C (CMOS)	This is a general purpose I/O port. A setting in the port 1 input resistance register (RDR1) can be used to apply pull-up resistance (RD10-RD17 = “1”) . (Disabled when pin is set for output.)
		AD08 to AD15		In multiplex mode, these pins function as the external address/data bus high I/O pins.
		D08 to D15		In non-multiplex mode, these pins function as the external data bus high output pins.
1 to 4	99, 100, 1, 2	P20 to P23	E (CMOS/H)	This is a general purpose I/O port. When the bits of external address output control register (HACR) are set to "1" in external bus mode, these pins function as general purpose I/O ports.
		A16 to A19		When the bits of external address output control register (HACR) are set to "0" in multiplex mode, these pins function as address high output pins (A16 to A19). When the bits of external address output control register (HACR) are set to "0" in non-multiplex mode, these pins function as address high output pins (A16 to A19).
5 to 8	3 to 6	P24 to P27	E (CMOS/H)	This is a general purpose I/O port. When the bits of external address output control register (HACR) are set to "1" in external bus mode, these pins function as general purpose I/O ports.
		A20 to A23		When the bits of external address output control register (HACR) are set to "0" in multiplex mode, these pins function as address high output pins (A20 to A23). When the bits of external address output control register (HACR) are set to "0" in non-multiplex mode, these pins function as address high output pins (A20 to A23).
		PPG0 to PPG3		Output pins for PPG.
9	7	P30	E (CMOS/H)	This is a general purpose I/O port.
		A00		In non-multiplex mode, this pin functions as an external address pin.
		AIN0		8/16-bit up/down timer input pin (ch.0) .

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Pin No.		Pin name	I/O circuit type*3	Function	
QFP*1	LQFP*2				
10	8	P31	E (CMOS/H)	This is a general purpose I/O port.	
		A01		In non-multiplex mode, this pin functions as an external address pin.	
		BIN0		8/16-bit up/down timer input pin (ch.0) .	
12	10	P32	E (CMOS/H)	This is a general purpose I/O port.	
		A02		In non-multiplex mode, this pin functions as an external address pin.	
		ZIN0		8/16-bit up/down timer input pin (ch.0)	
13	11	P33	E (CMOS/H)	This is a general purpose I/O port.	
		A03		In non-multiplex mode, this pin functions as an external address pin.	
		AIN1		8/16-bit up/down timer input pin (ch.1) .	
14	12	P34	E (CMOS/H)	This is a general purpose I/O port.	
		A04		In non-multiplex mode, this pin functions as an external address pin.	
		BIN1		8/16-bit up/down timer input pin (ch.1) .	
15	13	P35	E (CMOS/H)	This is a general purpose I/O port.	
		A05		In non-multiplex mode, this pin functions as an external address pin.	
		ZIN1		8/16-bit up/down timer input pin (ch.1)	
16, 17	14, 15	P36, P37	D (CMOS)	MB90480B series	This is a general purpose I/O port.
		A06, A07			In non-multiplex mode, these pins function as external address pins.
		P36, P37	E (CMOS/H)	MB90485B series	This is a general purpose I/O port.
		A06, A07			In non-multiplex mode, these pins function as external address pins.
		PWC0, PWC1*4			PWC input pins
18	16	P40	G (CMOS/H)	This is a general purpose I/O port.	
		A08		In non-multiplex mode, this pin functions as an external address pin.	
		SIN2		Extended I/O serial interface input pin.	
19	17	P41	F (CMOS)	This is a general purpose I/O port.	
		A09		In non-multiplex mode, this pin functions as an external address pin.	
		SOT2		Extended I/O serial interface output pin.	
20	18	P42	G (CMOS/H)	This is a general purpose I/O port.	
		A10		In non-multiplex mode, this pin functions as an external address pin.	
		SCK2		Extended I/O serial interface clock input/output pin.	

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Pin No.		Pin name	I/O circuit type*3	Function	
QFP*1	LQFP*2				
21, 22	19, 20	P43, P44	F (CMOS)	MB90480B series	This is a general purpose I/O port.
		A11, A12			In non-multiplex mode, these pins function as external address pins.
		P43, P44	F (CMOS)	MB90485B series	This is a general purpose I/O port.
		A11, A12			In non-multiplex mode, these pins function as external address pins.
		MT00, MT01			μPG output pins
24	22	P45	F (CMOS)	MB90480B series	This is a general purpose I/O port.
		A13			In non-multiplex mode, this pin functions as an external address pin.
		P45	G (CMOS/H)	MB90485B series	This is a general purpose I/O port.
		A13			In non-multiplex mode, this pin functions as an external address pin.
		EXTC*4			μPG input pin.
25, 26	23, 24	P46, P47	F (CMOS)	This is a general purpose I/O port.	
		A14, A15		In non-multiplex mode, these pins function as external address pins.	
		OUT4, OUT5		Output compare event output pins.	
70	68	P50	D (CMOS)	This is a general purpose I/O port. In external bus mode, this pin functions as the ALE pin.	
		ALE		In external bus mode, this pin functions as the address load enable (ALE) signal pin.	
71	69	P51	D (CMOS)	This is a general purpose I/O port. In external bus mode, this pin functions as the $\overline{RD}$ pin.	
		$\overline{RD}$		In external bus mode, this pin functions as the read strobe output ($\overline{RD}$) signal pin.	
72	70	P52	D (CMOS)	This is a general purpose I/O port. In external bus mode, when the WRE bit in the EPCR register is set to “1”, this pin functions as the $\overline{WRL}$ pin.	
		$\overline{WRL}$		In external bus mode, this pin functions as the lower data write strobe output ($\overline{WRL}$) pin. When the WRE bit in the EPCR register is set to “0”, this pin functions as a general purpose I/O port.	
73	71	P53	D (CMOS)	This is a general purpose I/O port. In external bus mode with 16-bit bus width, when the WRE bit in the EPCR register is set to “1”, this pin functions as the $\overline{WRH}$ pin.	
		$\overline{WRH}$		In external bus mode with 16-bit bus width, this pin functions as the upper data write strobe output ($\overline{WRH}$) pin. When the WRE bit in the EPCR register is set to “0”, this pin functions as a general purpose I/O port.	

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Pin No.		Pin name	I/O circuit type*3	Function
QFP*1	LQFP*2			
74	72	P54	D (CMOS)	This is a general purpose I/O port. In external bus mode, when the HDE bit in the EPCR register is set to “1”, this pin functions as the HRQ pin.
		HRQ		In external bus mode, this pin functions as the hold request input (HRQ) pin. When the HDE bit in the EPCR register is set to “0”, this pin functions as a general purpose I/O port.
75	73	P55	D (CMOS)	This is a general purpose I/O port. In external bus mode, when the HDE bit in the EPCR register is set to “1”, this pin functions as the $\overline{\text{HAK}}$ pin.
		$\overline{\text{HAK}}$		In external bus mode, this pin functions as the hold acknowledge output ($\overline{\text{HAK}}$) pin. When the HDE bit in the EPCR register is set to “0”, this pin functions as a general purpose I/O port.
76	74	P56	D (CMOS)	This is a general purpose I/O port. In external bus mode, when the RYE bit in the EPCR register is set to “1”, this pin functions as the RDY pin.
		RDY		In external bus mode, this pin functions as the external ready (RDY) input pin. When the RYE bit in the EPCR register is set to “0”, this pin functions as a general purpose I/O port.
78	76	P57	D (CMOS)	This is a general purpose I/O port. In external bus mode, when the CKE bit in the EPCR register is set to “1”, this pin functions as the CLK pin.
		CLK		In external bus mode, this pin functions as the machine cycle clock (CLK) output pin. When the CKE bit in the EPCR register is set to “0”, this pin functions as a general purpose I/O port.
38 to 41	36 to 39	P60 to P63	H (CMOS)	These are general purpose I/O ports.
		AN0 to AN3		These are the analog input pins for A/D converter.
43 to 46	41 to 44	P64 to P67	H (CMOS)	These are general purpose I/O ports.
		AN4 to AN7		These are the analog input pins for A/D converter.
27	25	P70	G (CMOS/H)	This is a general purpose I/O port.
		SIN0		This is the UART serial data input pin.
28	26	P71	F (CMOS)	This is a general purpose I/O port.
		SOT0		This is the UART serial data output pin.
29	27	P72	G (CMOS/H)	This is a general purpose I/O port.
		SCK0		This is the UART serial communication clock I/O pin.
30	28	P73	G (CMOS/H)	This is a general purpose I/O port.
		TIN0		This is the 16-bit reload timer event input pin.
31	29	P74	F (CMOS)	This is a general purpose I/O port.
		TOT0		This is the 16-bit reload timer output pin.

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Pin No.		Pin name	I/O circuit type*3	Function	
QFP*1	LQFP*2				
32	30	P75	F (CMOS)	MB90480B series	This is a general purpose I/O port.
		P75	G (CMOS/H)	MB90485B series	This is a general purpose I/O port.
		PWC2*4			This is a PWC input pin.
33	31	P76	F (CMOS)	MB90480B series	This is a general purpose I/O port.
		P76	I (NMOS/H)	MB90485B series	This is a general purpose I/O port.
		SCL*4			Serves as the I²C interface data I/O pin. During operation of the I²C interface, leave the port output in a high impedance state.
34	32	P77	F (CMOS)	MB90480B series	This is a general purpose I/O port.
		P77	I (NMOS/H)	MB90485B series	This is a general purpose I/O port.
		SDA*4			Serves as the I²C interface data I/O pin. During operation of the I²C interface, leave the port output in a high impedance state.
47, 48	45, 46	P80, P81	E (CMOS/H)	These are general purpose I/O ports.	
		IRQ0, IRQ1		External interrupt input pins.	
52 to 57	50 to 55	P82 to P87	E (CMOS/H)	These are general purpose I/O ports.	
		IRQ2 to IRQ7		External interrupt input pins.	
58	56	P90	E (CMOS/H)	This is a general purpose I/O port.	
		SIN1		Extended I/O serial interface data input pin.	
		CS0		Chip select 0.	
59	57	P91	D (CMOS)	This is a general purpose I/O port.	
		SOT1		Extended I/O serial interface data output pin.	
		CS1		Chip select 1.	
60	58	P92	E (CMOS/H)	This is a general purpose I/O port.	
		SCK1		Extended I/O serial interface clock input/output pin.	
		CS2		Chip select 2.	
61	59	P93	E (CMOS/H)	This is a general purpose I/O port.	
		FRCK		When the free-run timer is in use, this pin functions as the external clock input pin.	
		ADTG		When the A/D converter is in use, this pin functions as the external trigger input pin.	
		CS3		Chip select 3.	
62	60	P94	D (CMOS)	This is a general purpose I/O port.	
		PPG4		PPG timer output pin.	

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Pin No.		Pin name	I/O circuit type*3	Function	
QFP*1	LQFP*2				
63	61	P95	D (CMOS)	This is a general purpose I/O port.	
		PPG5		PPG timer output pin.	
64	62	P96	E (CMOS/H)	This is a general purpose I/O port.	
		IN0		Input capture ch.0 trigger input pin.	
65	63	P97	E (CMOS/H)	This is a general purpose I/O port.	
		IN1		Input capture ch.1 trigger input pin.	
66 to 69	64 to 67	PA0 to PA3	D (CMOS)	These are general purpose I/O ports.	
		OUT0 to OUT3		Output compare event output pins.	
35	33	AV_{CC}	—	A/D converter analog power supply input pin.	
36	34	AVRH	—	A/D converter reference voltage input pin.	
37	35	AV_{SS}	—	A/D converter GND pin.	
49 to 51	47 to 49	MD0 to MD2	J (CMOS/H)	Operating mode selection input pins.	
84	82	$V_{CC}3$	—	3.3 V ± 0.3 V power supply pins ($V_{CC}3$) .	
23	21	$V_{CC}5$	—	MB90480B series	3.3 V ± 0.3 V power supply pin. Usually, use $V_{CC} = V_{CC}3 = V_{CC}5$ as a 3 V power supply.
				MB90485B series	3 V/5 V power supply pin. 5 V power supply pin when P20 to P27, P30 to P37, P40 to P47, P70 to P77 are used as 5 V I/F pins. Usually, use $V_{CC} = V_{CC}3 = V_{CC}5$ as a 3 V power supply (when the 3 V power supply is used alone) .
11, 42, 81	9, 40, 79	V_{SS}	—	GND pins.	

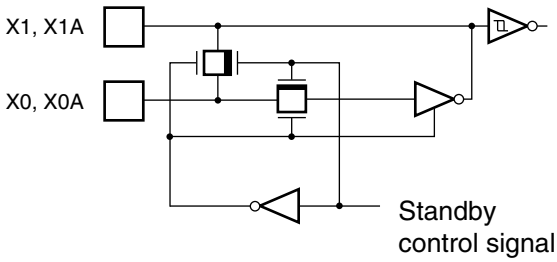
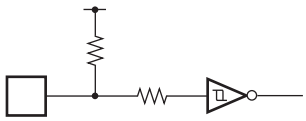
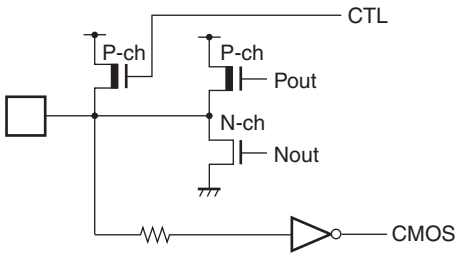
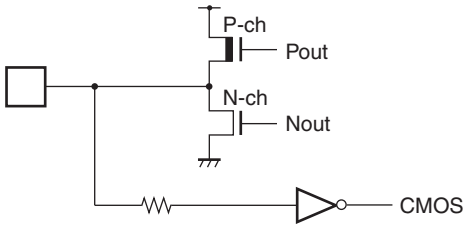
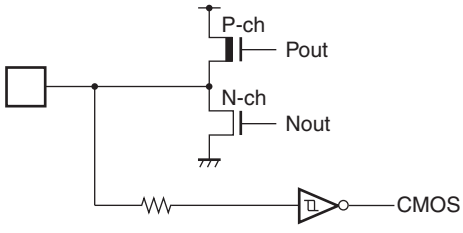
*1 : QFP : FPT-100P-M06

*2 : LQFP : FPT-100P-M20

*3 : For the I/O circuit type, refer to “■ I/O CIRCUIT TYPES”.

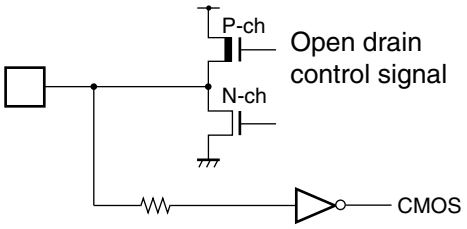
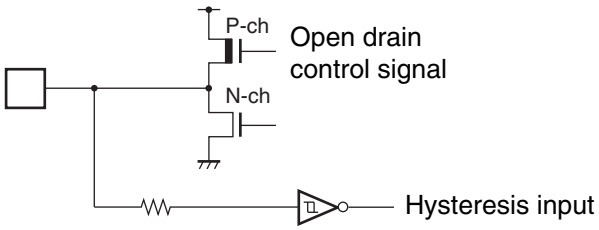
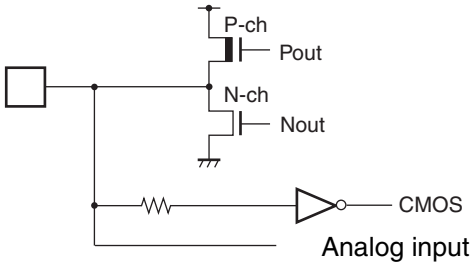
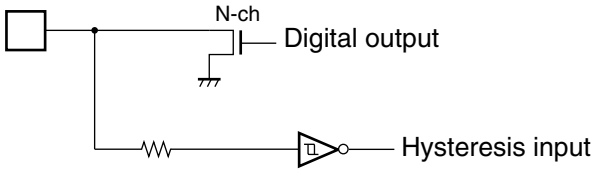
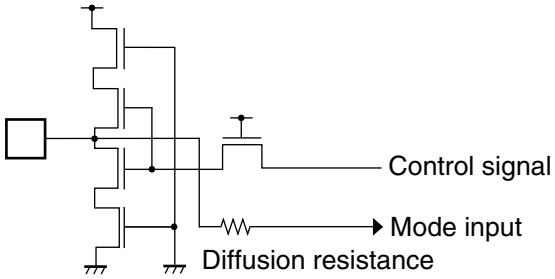
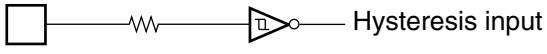
*4 : As for MB90V485B, input pins become CMOS input.

■ I/O CIRCUIT TYPES

Type	Circuit	Remarks
A		• Feedback resistance X1, X0 : approx. 1 MΩ X1A, X0A : approx. 10 MΩ • With standby control
B		Hysteresis input with pull-up resistance
C		• With input pull-up resistance control • CMOS level input/output
D		CMOS level input/output
E		• Hysteresis input • CMOS level output

(Continued)

(Continued)

Type	Circuit	Remarks
F		• CMOS level input/output • With open drain control
G		• CMOS level output • Hysteresis input • With open drain control
H		• CMOS level input/output • Analog input
I		• Hysteresis input • N-ch open drain output
J	(Flash memory product) 	(Flash memory product) • CMOS level input • With high voltage control for flash testing
	(MASK ROM product) 	(MASK ROM product) Hysteresis input

■ HANDLING DEVICES

1. Be careful never to exceed maximum rated voltages (preventing latch-up)

In CMOS IC devices, a condition known as latch-up may occur if voltages higher than V_{CC} or lower than V_{SS} are applied to input or output pins other than medium-or high-voltage pins, or if the voltage applied between V_{CC} and V_{SS} pins exceeds the rated voltage level.
When latch-up occurs, the power supply current increases rapidly causing the possibility of thermal damage to circuit elements. Therefore it is necessary to ensure that maximum ratings are not exceeded in circuit operation.
Similarly, when turning the analog power supply on or off, it is necessary to ensure that the analog power supply voltages (AV_{CC} and AVRH) and analog input voltages do not exceed the digital power supply (V_{CC}) .

2. Treatment of unused pins

Leaving unused input pins unconnected can cause abnormal operation or latch-up, leading to permanent damage. Unused input pins should always be pulled up or down through resistance of at least 2 kΩ. Any unused input/output pins may be set to output mode and left open, or set to input mode and treated the same as unused input pins.

3. Treatment of Power Supply Pins (V_{CC}/V_{SS})

When multiple V_{CC}/V_{SS} pins are present, device design considerations for prevention of latch-up and unwanted electromagnetic interference, abnormal strobe signal operation due to ground level rise, and conformity with total output current ratings require that all power supply pins must be externally connected to power supply or ground.
Consideration should be given to connecting power supply sources to the V_{CC}/V_{SS} pins of this device with as low impedance as possible. It is also recommended that a bypass capacitor of approximately 0.1 μF be placed between the V_{CC} and V_{SS} lines as close to this device as possible.

4. Crystal Oscillator Circuits

Noise around the X0/X1, or X0A/X1A pins may cause this device to operate abnormally. In the interest of stable operation it is strongly recommended that printed circuit board artwork places ground bypass capacitors as close as possible to the X0/X1, X0A/X1A and crystal oscillator (or ceramic oscillator) and that oscillator lines do not cross the lines of other circuits.

5. Precautions when turning the power supply on

In order to prevent abnormal operation in the chip's internal step-down circuits, a voltage rise time during power-on of 50 μs (0.2 V to 2.7 V) or greater should be assured.

6. Supply Voltage Stabilization

Even within the operating range of V_{CC} supply voltage, rapid voltage fluctuations may cause abnormal operation. As a standard for power supply voltage stability, it is recommended that the peak-to-peak V_{CC} ripple voltage at commercial supply frequency (50/60 Hz) be 10 % or less of V_{CC}, and that the transient voltage fluctuation be no more than 0.1 V/ms or less when the power supply is turned on or off.

7. Proper power-on/off sequence

The A/D converter power (AV_{CC}, AVRH) and analog input (AN0 to AN7) must be turned on after the digital power supply (V_{CC}) is turned on. The A/D converter power (AV_{CC}, AVRH) and analog input (AN0 to AN7) must be shut off before the digital power supply (V_{CC}) is shut off. Care should be taken that AVRH does not exceed AV_{CC}. Even when pins used as analog input pins are doubled as input ports, be sure that the input voltage does not exceed AV_{CC}.

8. Treatment of power supply pins on models with A/D converters

Even when the A/D converters are not in use, be sure to make the necessary connections AV_{CC} = AVRH = V_{CC}, and AV_{SS} = V_{SS}.

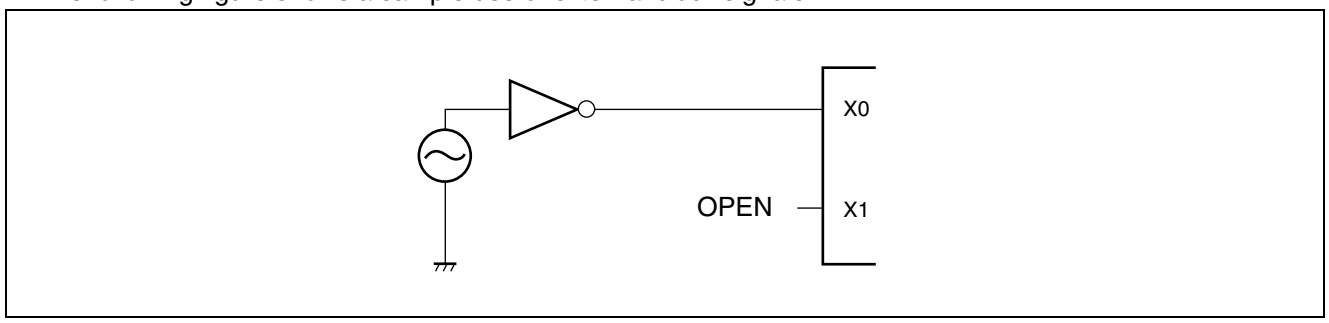
9. Notes on Using Power Supply

Only the MB90485B series usually uses a 3 V power supply. By setting $V_{CC}3$ = 3 V power supply and $V_{CC}5$ = 5 V power supply, P20 to P27, P30 to P37, P40 to P47 and P70 to P77 can be interfaced as 5 V power supplies separately from the main 3 V power supply. Note that the analog power supplies (such as AV_{CC} and AV_{SS}) for the A/D converter can be used only as 3 V power supplies.

10. Notes on Using External Clock

Even when using an external clock signal, an oscillation stabilization delay is applied after a power-on reset or when recovering from sub-clock or stop mode. When using an external clock, 25 MHz should be the upper frequency limit.

The following figure shows a sample use of external clock signals.



11. Treatment of NC pins

NC (internally connected) pins should always be left open.

12. Notes on during operation of PLL clock mode

On this microcontroller, if in case the crystal oscillator breaks off or an external reference clock input stops while the PLL clock mode is selected, a self-oscillator circuit contained in the PLL may continue its operation at its self-running frequency. However, Fujitsu will not guarantee results of operation if such failure occurs.

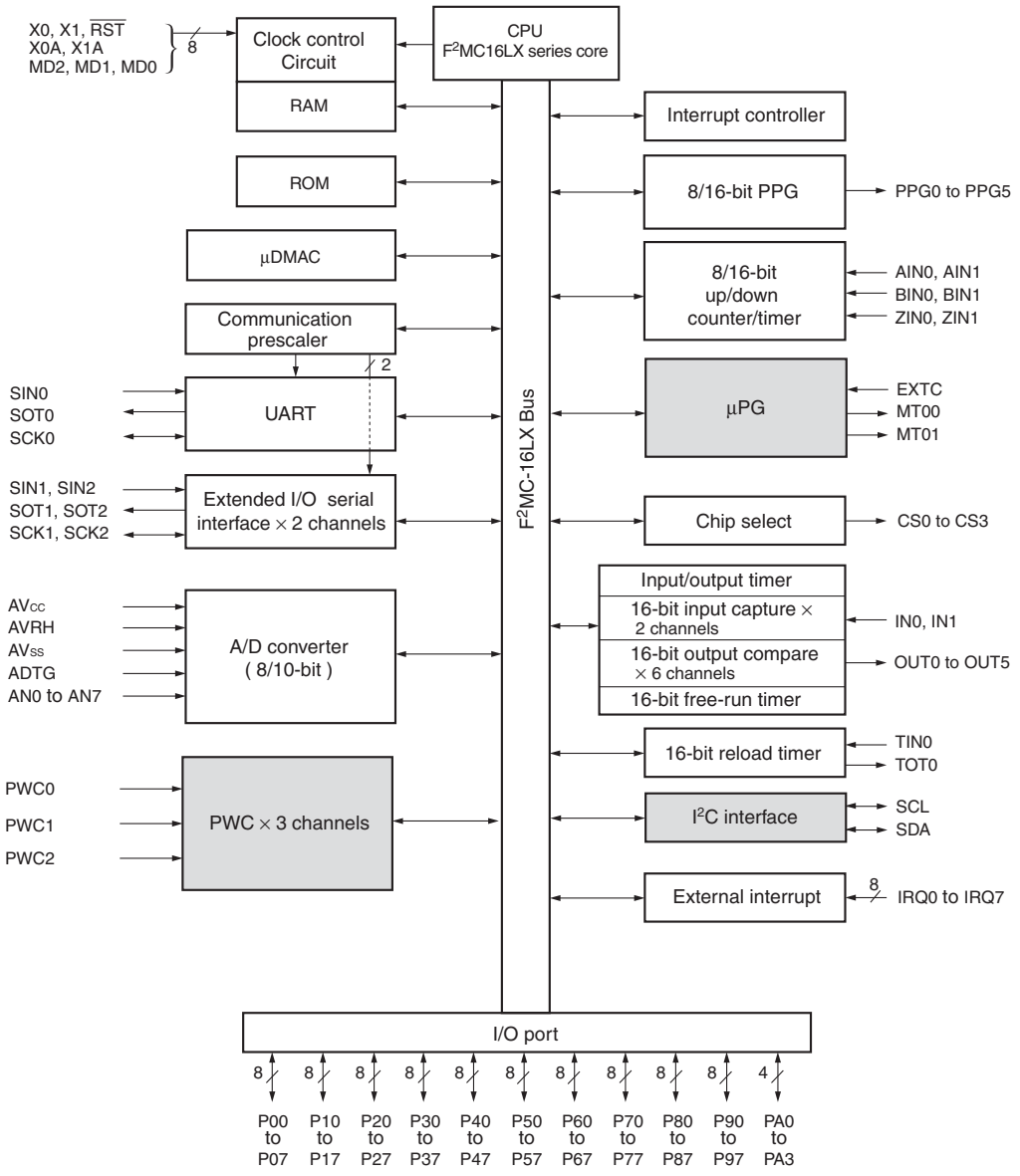
13. When the MB90480B/485B series microcontroller is used as a single system

When the MB90480B/485B series microcontroller is used as a single system, use connections so the X0A = V_{SS}, and X1A = Open.

14. Writing to Flash memory

For writing to Flash memory, always ensure that the operating voltage V_{CC} is between 3.0 V and 3.6 V.

■ BLOCK DIAGRAM



P00 to P07 (8 pins) : with an input pull-up resistance setting register.
P10 to P17 (8 pins) : with an input pull-up resistance setting register.
P40 to P47 (8 pins) : with an open drain setting register.
P70 to P77 (8 pins) : with an open drain setting register.

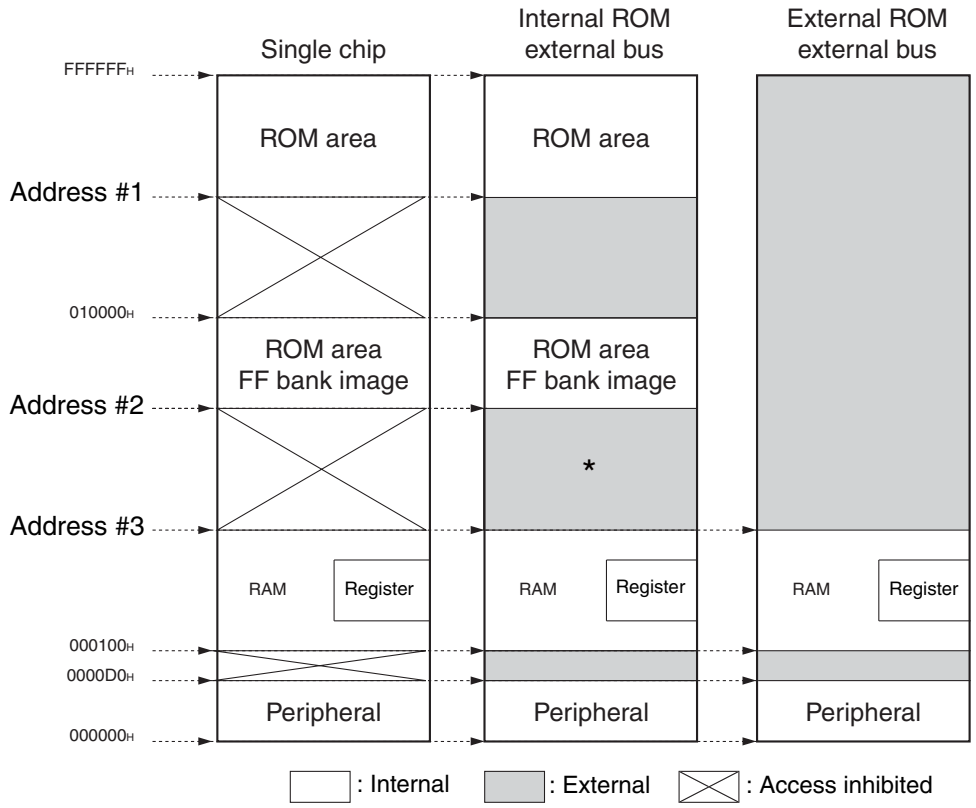
MB90485B series only

- I²C pin P77 and P76 are N-ch open drain pin (without P-ch) . However, MB90V485B uses the N-ch open drain pin (with P-ch) .
- P20 to P27, P30 to P37, P40 to P47 and P70 to P77 are also used as 3 V/5 V I/F pin.
- As for MB90V485B, input pins (PWC0, PWC1, PWC2/EXTC/SCL and SDA pins) for PWC/µPG/I²C become CMOS input.

Note : In the above diagram, I/O ports share internal function blocks and pins. However, when a set of pins is used with an internal module, it cannot also be used as an I/O port.

■ MEMORY MAP

• MB90F481B/F482B/487B/488B/483C/F488B/V480B/V485B/F489B



* : In models where address #3 overlaps with address #2, this external area does not exist.

Model	Address #1	Address #2	Address #3
MB90F481B	FC0000H *1	004000H or 008000H, selected by the MS bit in the ROMM register	001100H
MB90F482B	FC0000H		001900H
MB90487B	FD0000H		002900H
MB90488B	FC0000H		002900H
MB90F488B	FC0000H		002900H
MB90V480B	(FC0000H)		004000H
MB90V485B	(FC0000H)		004000H
MB90483C	FB0000H*4		004000H
MB90F489B	F90000H *2	0080000H fixed	006100H*3

*1 : No memory cells from FC0000H to FC7FFFH and FE0000H to FE7FFFH.
The upper part of the 00 bank is set up to mirror the image of FF bank ROM, to enable efficient use of small model C compilers. Because the lower 16-bit address of the FF bank and the lower 16-bit address of the 00 bank are the same, enabling reference to tables in ROM without using the for specification in the pointer declaration.
For example, in accessing address 00C000H it is actually the contents of ROM at FFC000H that are accessed. If the MS bit in the ROMM register is set to “0”, the ROM area in the FF bank will exceed 48 Kbytes and it is not possible to reflect the entire area in the image in the 00 bank. Therefore the image from FF4000H to FFFFFFH is reflected in the 00 bank and the area from FF0000H to FF3FFFH can be seen in the FF bank only.

(Continued)

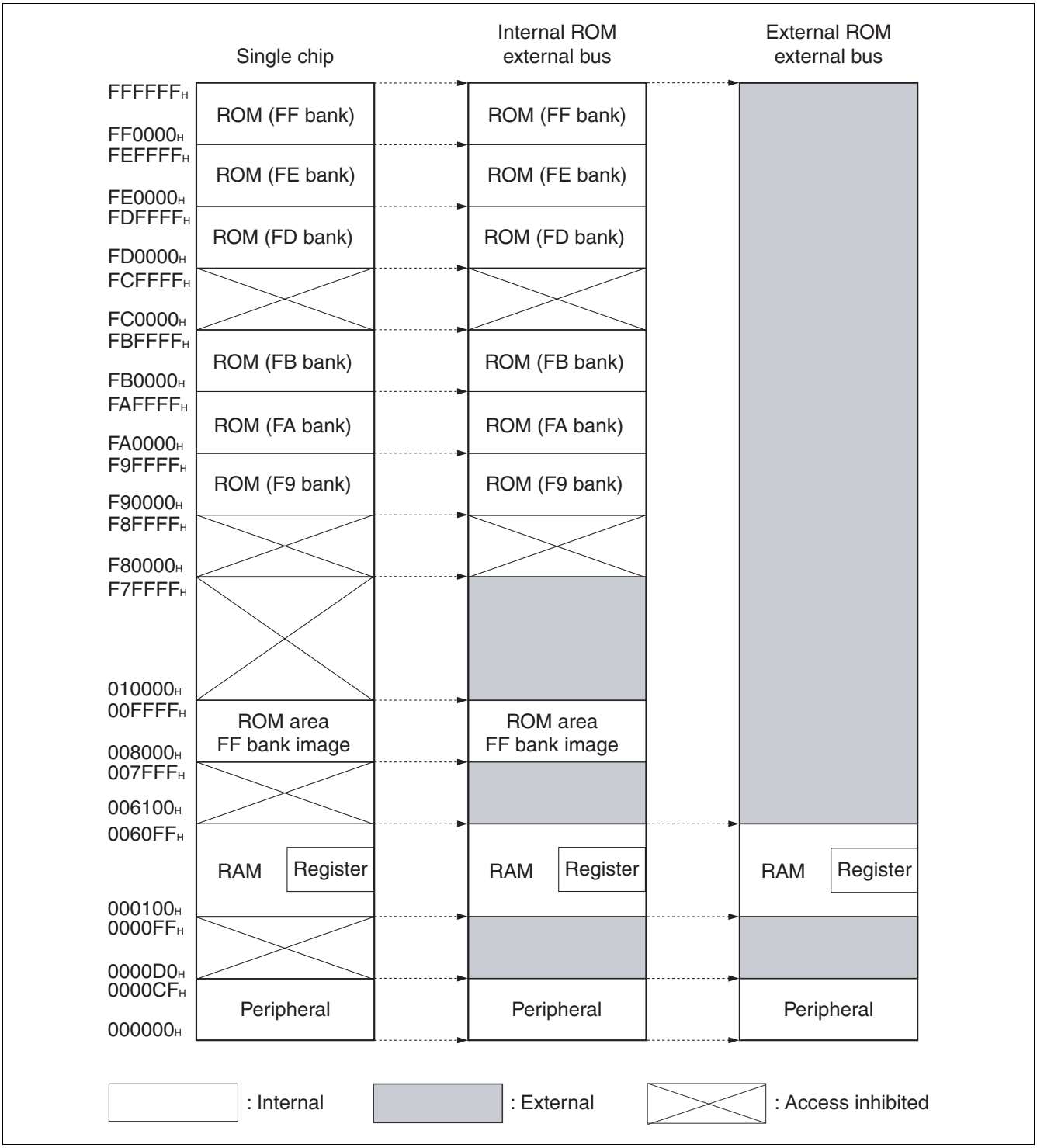
(Continued)

*2 : In MB90F489B, there is no access to F8 bank and FC bank on the single-chip mode or the internal-ROM external-bus mode.

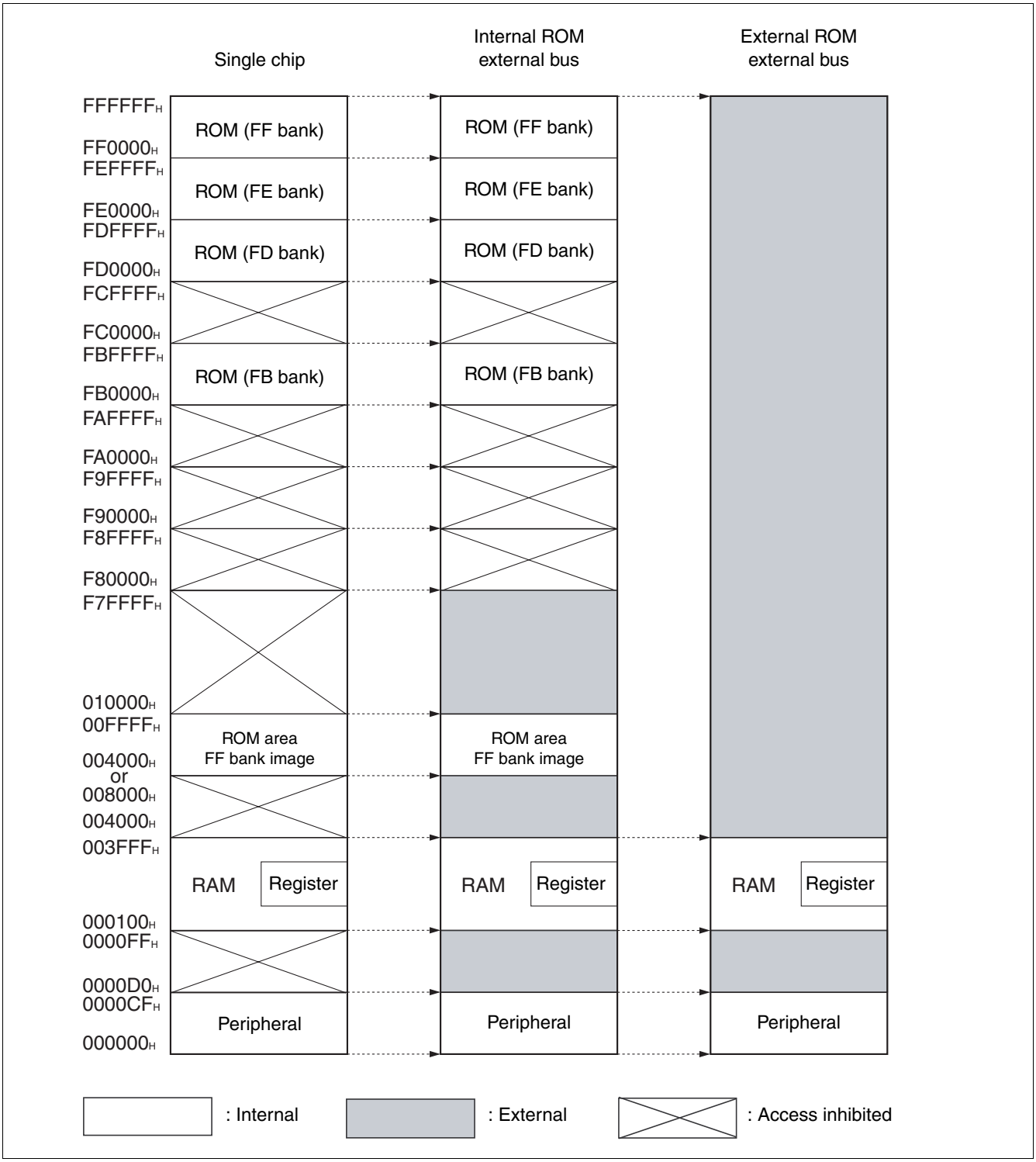
*3 : Because installed-RAM area is larger than MB90V485B, MB90F489B should execute emulation in an area that is larger than 004000_H by the emulation memory area setting on the tool side.

*4 : In MB90483C, there is no access to F8 bank to FA bank and FC bank on the single-chip mode or the internal-ROM external-bus mode.

• MB90F489B

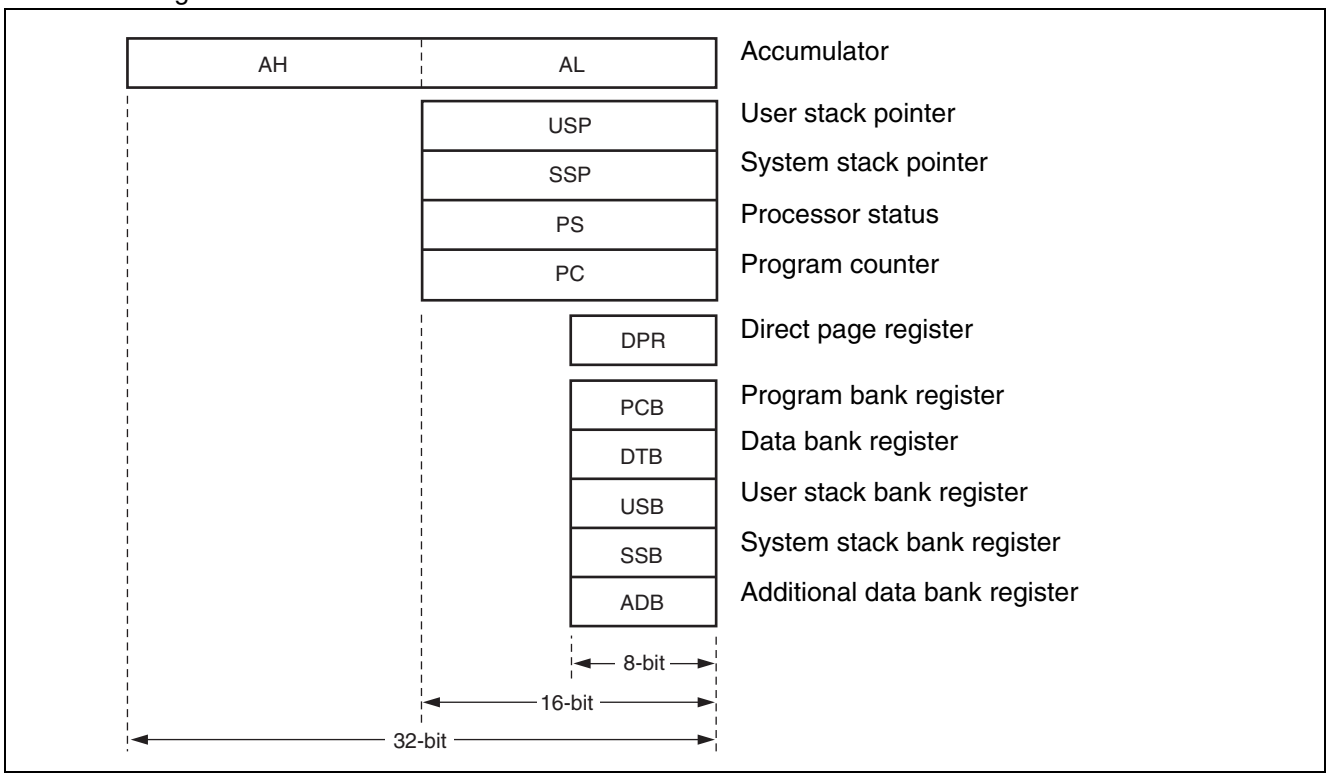

Single chip
Internal ROM external bus
External ROM external bus
FFFFFFH
FF0000H
FEFFFFH
FE0000H
FDFFFFH
FD0000H
FCFFFFH
FC0000H
FBFFFFH
FB0000H
FAFFFFH
FA0000H
F9FFFFH
F90000H
F8FFFFH
F80000H
F7FFFFH
010000H
00FFFFH
008000H
007FFFH
006100H
0060FFH
000100H
0000FFH
0000D0H
0000CFH
000000H
ROM (FF bank)
ROM (FE bank)
ROM (FD bank)
ROM (FB bank)
ROM (FA bank)
ROM (F9 bank)
ROM area FF bank image
RAM
Register
Peripheral
: Internal
: External
: Access inhibited

• MB90483C

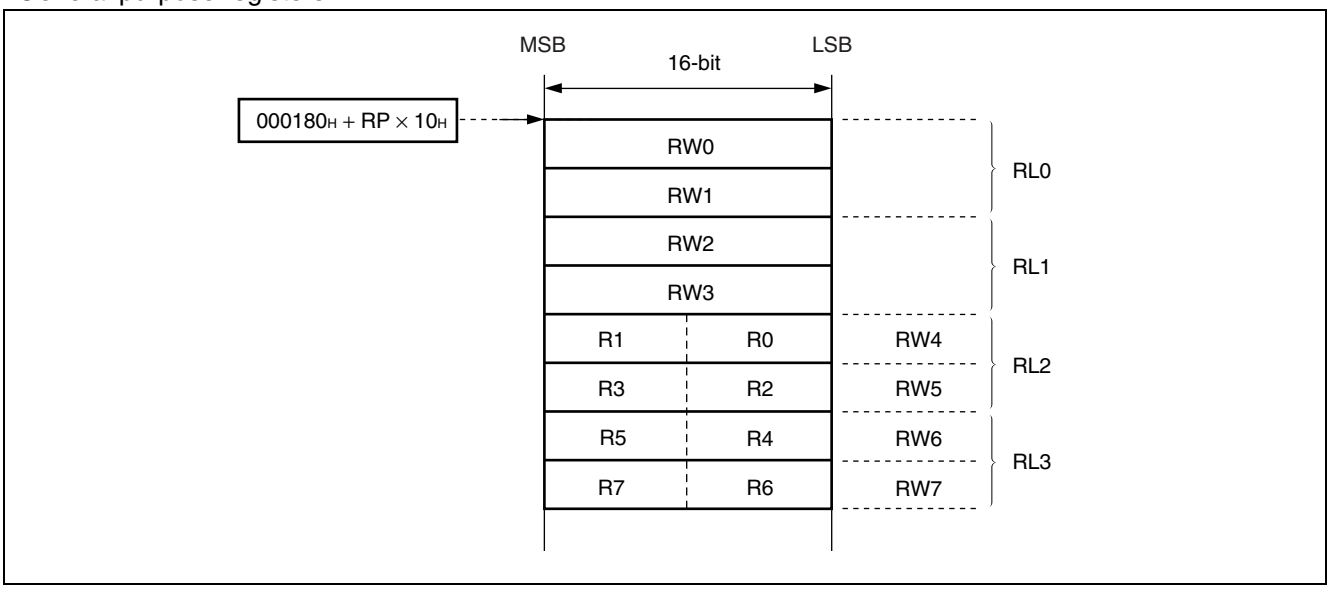

Single chip
Internal ROM external bus
External ROM external bus
FFFFFFH
FF0000H
FEFFFFH
FE0000H
FDFFFFH
FD0000H
FCFFFFH
FC0000H
FBFFFFH
FB0000H
FAFFFFH
FA0000H
F9FFFFH
F90000H
F8FFFFH
F80000H
F7FFFFH
010000H
00FFFFH
004000H
or
008000H
004000H
003FFFH
000100H
0000FFH
0000D0H
0000CFH
000000H
ROM (FF bank)
ROM (FE bank)
ROM (FD bank)
ROM (FB bank)
ROM area
FF bank image
RAM
Register
Peripheral
: Internal
: External
: Access inhibited

■ F²MC-16L CPU PROGRAMMING MODEL

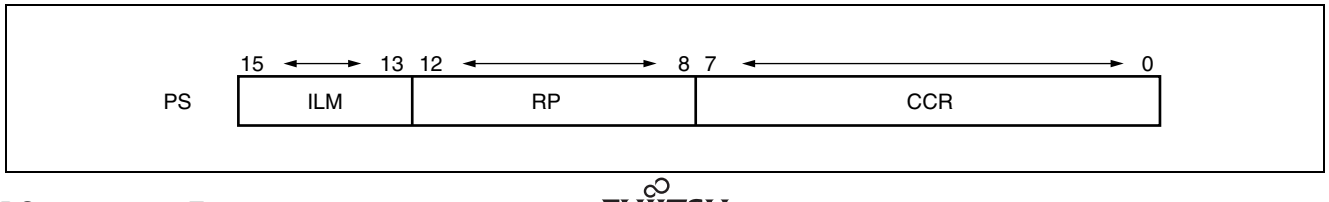
• Dedicated registers



• General purpose registers



• Processor status



■ I/O MAP

Address	Register name	Abbreviated register name	Read/ Write	Resource name	Initial value
00H	Port 0 data register	PDR0	R/W	Port 0	XXXXXXXXB
01H	Port 1 data register	PDR1	R/W	Port 1	XXXXXXXXB
02H	Port 2 data register	PDR2	R/W	Port 2	XXXXXXXXB
03H	Port 3 data register	PDR3	R/W	Port 3	XXXXXXXXB
04H	Port 4 data register	PDR4	R/W	Port 4	XXXXXXXXB
05H	Port 5 data register	PDR5	R/W	Port 5	XXXXXXXXB
06H	Port 6 data register	PDR6	R/W	Port 6	XXXXXXXXB
07H	Port 7 data register	PDR7	R/W	Port 7	XXXXXXXXB (MB90480B series)
					11XXXXXXB (MB90485B series)
08H	Port 8 data register	PDR8	R/W	Port 8	XXXXXXXXB
09H	Port 9 data register	PDR9	R/W	Port 9	XXXXXXXXB
0AH	Port A data register	PDRA	R/W	Port A	----XXXXB
0BH	Up/down timer input enable register	UDRE	R/W	Up/down timer input control	XX000000B
0CH	Interrupt/DTP enable register	ENIR	R/W	DTP/external interrupts	00000000B
0DH	Interrupt/DTP source register	EIRR	R/W		XXXXXXXXB
0EH	Request level setting register	ELVR	R/W		00000000B
0FH	Request level setting register		R/W		00000000B
10H	Port 0 direction register	DDR0	R/W	Port 0	00000000B
11H	Port 1 direction register	DDR1	R/W	Port 1	00000000B
12H	Port 2 direction register	DDR2	R/W	Port 2	00000000B
13H	Port 3 direction register	DDR3	R/W	Port 3	00000000B
14H	Port 4 direction register	DDR4	R/W	Port 4	00000000B
15H	Port 5 direction register	DDR5	R/W	Port 5	00000000B
16H	Port 6 direction register	DDR6	R/W	Port 6	00000000B
17H	Port 7 direction register	DDR7	R/W	Port 7	00000000B (MB90480B series)
					XX000000B (MB90485B series)
18H	Port 8 direction register	DDR8	R/W	Port 8	00000000B
19H	Port 9 direction register	DDR9	R/W	Port 9	00000000B
1AH	Port A direction register	DDRA	R/W	Port A	----0000B
1BH	Port 4 output pin register	ODR4	R/W	Port 4 (Open-drain control)	00000000B
1CH	Port 0 input resistance register	RDR0	R/W	Port 0 (resistance control)	00000000B
1DH	Port 1 input resistance register	RDR1	R/W	Port 1 (resistance control)	00000000B
1EH	Port 7 output pin register	ODR7	R/W	Port 7 (Open-drain control)	00000000B (MB90480B series)
					XX000000B (MB90485B series)
1FH	Analog input enable register	ADER	R/W	Port 6, A/D	11111111B

(Continued)

Address	Register name	Abbreviated register name	Read/ Write	Resource name	Initial value
20H	Serial mode register	SMR	R/W	UART	00000X00B
21H	Serial control register	SCR	W, R/W		00000100B
22H	Serial input/output register	SIDR/SODR	R/W		XXXXXXXXB
23H	Serial status register	SSR	R, R/W		00001000B
24H	(Reserved area)				
25H	Communication prescaler control register	CDCR	R/W	Communication prescaler (UART)	00--0000B
26H	Serial mode control status register 0	SMCS0	R, R/W	SIO1 (ch.0)	----0000B
27H					00000010B
28H	Serial data register 0	SDR0	R/W		XXXXXXXXB
29H	Communication prescaler control register 0	SDCR0	R/W	Communication prescaler SIO1 (ch.0)	0---0000B
2AH	Serial mode control status register 1	SMCS1	R, R/W	SIO2 (ch.1)	----0000B
2BH					00000010B
2CH	Serial data register 1	SDR1	R/W		XXXXXXXXB
2DH	Communication prescaler control register 1	SDCR1	R/W	Communication prescaler SIO2 (ch.1)	0---0000B
2EH	Reload register L (ch.0)	PRLL0	R/W	8/16-bit PPG (ch.0 to ch.5)	XXXXXXXXB
2FH	Reload register H (ch.0)	PRLH0	R/W		XXXXXXXXB
30H	Reload register L (ch.1)	PRLL1	R/W		XXXXXXXXB
31H	Reload resister H (ch.1)	PRLH1	R/W		XXXXXXXXB
32H	Reload register L (ch.2)	PRLL2	R/W		XXXXXXXXB
33H	Reload register H (ch.2)	PRLH2	R/W		XXXXXXXXB
34H	Reload register L (ch.3)	PRLL3	R/W		XXXXXXXXB
35H	Reload register H (ch.3)	PRLH3	R/W		XXXXXXXXB
36H	Reload register L (ch.4)	PRLL4	R/W		XXXXXXXXB
37H	Reload register H (ch.4)	PRLH4	R/W		XXXXXXXXB
38H	Reload register L (ch.5)	PRLL5	R/W		XXXXXXXXB
39H	Reload register H (ch.5)	PRLH5	R/W		XXXXXXXXB
3AH	PPG0 operating mode control register	PPGC0	R/W		0X000XX1B
3BH	PPG1 operating mode control register	PPGC1	R/W		0X000001B
3CH	PPG2 operating mode control register	PPGC2	R/W		0X000XX1B
3DH	PPG3 operating mode control register	PPGC3	R/W		0X000001B
3EH	PPG4 operating mode control register	PPGC4	R/W		0X000XX1B
3FH	PPG5 operating mode control register	PPGC5	R/W		0X000001B
40H	PPG0, PPG1 output control register	PPG01	R/W	8/16-bit PPG	00000000B
41H	(Reserved area)				
42H	PPG2, PPG3 output control register	PPG23	R/W	8/16-bit PPG	00000000B
43H	(Reserved area)				

(Continued)

Address	Register name	Abbreviated register name	Read/ Write	Resource name	Initial value
44H	PPG4, PPG5 output control register	PPG45	R/W	8/16-bit PPG	00000000B
45H	(Reserved area)				
46H	Control status register	ADCS1	R/W	A/D converter	00000000B
47H		ADCS2	W, R/W		00000000B
48H	Data register	ADCR1	R		XXXXXXXXB
49H		ADCR2	W, R		00000XXXB
4AH	Output compare register (ch.0) lower digits	OCCP0	R/W	16-bit input/output timer output compare (ch.0 to ch.5)	00000000B
4BH	Output compare register (ch.0) upper digits				00000000B
4CH	Output compare register (ch.1) lower digits	OCCP1	R/W		00000000B
4DH	Output compare register (ch.1) upper digits				00000000B
4EH	Output compare register (ch.2) lower digits	OCCP2	R/W		00000000B
4FH	Output compare register (ch.2) upper digits				00000000B
50H	Output compare register (ch.3) lower digits	OCCP3	R/W		00000000B
51H	Output compare register (ch.3) upper digits				00000000B
52H	Output compare register (ch.4) lower digits	OCCP4	R/W		00000000B
53H	Output compare register (ch.4) upper digits				00000000B
54H	Output compare register (ch.5) lower digits	OCCP5	R/W		00000000B
55H	Output compare register (ch.5) upper digits				00000000B
56H	Output compare control register (ch.0)	OCS0	R/W		0000--00B
57H	Output compare control register (ch.1)	OCS1	R/W		---00000B
58H	Output compare control register (ch.2)	OCS2	R/W		0000--00B
59H	Output compare control register (ch.3)	OCS3	R/W		---00000B
5AH	Output compare control register (ch.4)	OCS4	R/W		0000--00B
5BH	Output compare control register (ch.5)	OCS5	R/W		---00000B
5CH	Input capture data register (ch.0) lower digits	IPCP0	R	16-bit input/output timer input capture (ch.0, ch.1)	XXXXXXXXB
5DH	Input capture data register (ch.0) upper digits		R		XXXXXXXXB
5EH	Input capture data register (ch.1) lower digits	IPCP1	R		XXXXXXXXB
5FH	Input capture data register (ch.1) upper digits		R		XXXXXXXXB
60H	Input capture control status register	ICS01	R/W		00000000B
61H	(Reserved area)				

(Continued)

Address	Register name	Abbreviated register name	Read/ Write	Resource name	Initial value
62H	Timer counter data register lower digits	TCDT	R/W	16-bit input/output timer free-run timer	00000000B
63H	Timer counter data register upper digits	TCDT	R/W		00000000B
64H	Timer counter control status register	TCCS	R/W		00000000B
65H	Timer counter control status register	TCCS	R/W		0--00000B
66H	Compare clear register lower digits	CPCLR	R/W		XXXXXXXXB
67H	Compare clear register upper digits				XXXXXXXXB
68H	Up/down count register (ch.0)	UDCR0	R	8/16-bit up/down counter/timer	00000000B
69H	Up/down count register (ch.1)	UDCR1	R		00000000B
6AH	Reload/compare register (ch.0)	RCR0	W		00000000B
6BH	Reload/compare register (ch.1)	RCR1	W		00000000B
6CH	Counter control register (ch.0) lower digits	CCRL0	W, R/W		0X00X000B
6DH	Counter control register (ch.0) upper digits	CCRH0	R/W		00000000B
6EH	(Reserved area)				
6FH	ROM mirror function select register	ROMM	R/W	ROM mirroring function	------+1B
70H	Counter control register (ch.1) lower digits	CCRL1	W, R/W	8/16-bit up/down counter/timer	0X00X000B
71H	Counter control register (ch.1) upper digits	CCRH1	R/W		-0000000B
72H	Counter status register (ch.0)	CSR0	R, R/W		00000000B
73H	(Reserved area)				
74H	Counter status register (ch.1)	CSR1	R, R/W	8/16-bit UDC	00000000B
75H	(Reserved area)				
76H*	PWC control/status register	PWCSR0	R, R/W	PWC (ch.0)	00000000B
77H*					0000000XB
78H*	PWC data buffer register	PWCR0	R/W		00000000B
79H*					00000000B
7AH*	PWC control/status register	PWCSR1	R, R/W	PWC (ch.1)	00000000B
7BH*					0000000XB
7CH*	PWC data buffer register	PWCR1	R/W		00000000B
7DH*					00000000B
7EH*	PWC control/status register	PWCSR2	R, R/W	PWC (ch.2)	00000000B
7FH*					0000000XB
80H*	PWC data buffer register	PWCR2	R/W		00000000B
81H*					00000000B
82H*	Dividing ratio control register	DIVR0	R/W	PWC (ch.0)	------00B
83H	(Reserved area)				
84H*	Dividing ratio control register	DIVR1	R/W	PWC (ch.1)	------00B
85H	(Reserved area)				
86H*	Dividing ratio control register	DIVR2	R/W	PWC (ch.2)	------00B
87H	(Reserved area)				

(Continued)

Address	Register name	Abbreviated register name	Read/ Write	Resource name	Initial value
88H*	Bus status register	IBSR	R	I²C	00000000B
89H*	Bus control register	IBCR	R/W		00000000B
8AH*	Clock control register	ICCR	R/W		--0XXXXXB
8BH*	Address register	IADR	R/W		-XXXXXXXB
8CH*	Data register	IDAR	R/W		XXXXXXXXB
8DH	(Reserved area)				
8EH*	µPG control status register	PGCSR	R/W	µPG	00000---B
8FH to 9BH	(Disabled)				
9CH	µDMAC status register lower digits	DSRL	R/W	µDMAC	00000000B
9DH	µDMAC status register upper digits	DSRH	R/W	µDMAC	00000000B
9EH	Program address detection control status resister	PACSR	R/W	Address match detection function	00000000B
9FH	Delayed interrupt source general/ cancel register	DIRR	R/W	Delayed interrupt generator module	-------0B
A0H	Low-power consumption mode control register	LPMCR	W, R/W	Low-power consumption	00011000B
A1H	Clock select register	CKSCR	R, R/W	Low-power consumption	11111100B
A2H, A3H	(Reserved area)				
A4H	µDMAC stop status register	DSSR	R/W	µDMAC	00000000B
A5H	Automatic ready function select register	ARSR	W	External pins	0011 - -00B
A6H	External address output control register	HACR	W	External pins	********B
A7H	Bus control signal select register	EPCR	W	External pins	1000*10 -B
A8H	Watchdog timer control register	WDTC	R, W	Watchdog timer	XXXXX111B
A9H	Timebase timer control register	TBTC	W, R/W	Timebase timer	1XX00100B
AAH	Watch timer control register	WTC	R, R/W	Watch timer	10001000B
ABH	(Reserved area)				
ACH	µDMAC enable register lower digits	DERL	R/W	µDMAC	00000000B
ADH	µDMAC enable register upper digits	DERH	R/W	µDMAC	00000000B
AEH	Flash memory control status register	FMCS	W, R/W	Flash memory interface	000X0000B
AFH	(Disabled)				
B0H	Interrupt control register 00	ICR00	W, R/W	Interrupt controller	XXXX0111B
B1H	Interrupt control register 01	ICR01	W, R/W		XXXX0111B
B2H	Interrupt control register 02	ICR02	W, R/W		XXXX0111B
B3H	Interrupt control register 03	ICR03	W, R/W		XXXX0111B
B4H	Interrupt control register 04	ICR04	W, R/W		XXXX0111B
B5H	Interrupt control register 05	ICR05	W, R/W		XXXX0111B
B6H	Interrupt control register 06	ICR06	W, R/W		XXXX0111B
B7H	Interrupt control register 07	ICR07	W, R/W		XXXX0111B
B8H	Interrupt control register 08	ICR08	W, R/W		XXXX0111B

(Continued)

Address	Register name	Abbreviated register name	Read/ Write	Resource name	Initial value
B9H	Interrupt control register 09	ICR09	W, R/W	Interrupt controller	XXXX0111B
BAH	Interrupt control register 10	ICR10	W, R/W		XXXX0111B
BBH	Interrupt control register 11	ICR11	W, R/W		XXXX0111B
BCH	Interrupt control register 12	ICR12	W, R/W		XXXX0111B
BDH	Interrupt control register 13	ICR13	W, R/W		XXXX0111B
BEH	Interrupt control register 14	ICR14	W, R/W		XXXX0111B
BFH	Interrupt control register 15	ICR15	W, R/W		XXXX0111B
C0H	Chip select area mask register 0	CMR0	R/W	Chip select function	00001111B
C1H	Chip select area register 0	CAR0	R/W		11111111B
C2H	Chip select area mask register 1	CMR1	R/W		00001111B
C3H	Chip select area register 1	CAR1	R/W		11111111B
C4H	Chip select area mask register 2	CMR2	R/W		00001111B
C5H	Chip select area register 2	CAR2	R/W		11111111B
C6H	Chip select area mask register 3	CMR3	R/W		00001111B
C7H	Chip select area register 3	CAR3	R/W		11111111B
C8H	Chip select control register	CSCR	R/W		----000*B
C9H	Chip select active level register	CALR	R/W		----0000B
CAH	Timer control status register	TMCSR	R/W	16-bit reload timer	00000000B
CBH					----0000B
CCH	16-bit timer register/ 16-bit reload register	TMR/TMRLR	R/W		XXXXXXXXB
CDH					
CEH	(Reserved area)				
CFH	PLL output control register	PLLOS	W	Low-power consumption	------X0B
D0H to FFH	(External area)				
100H to #H	(RAM area)				
1FF0H	Program address detection register 0 (Low order address)	PADR0	R/W	Address match detection function	XXXXXXXXB
1FF1H	Program address detection register 0 (Middle order address)				
1FF2H	Program address detection register 0 (High order address)				
1FF3H	Program address detection register 1 (Low order address)	PADR1	R/W	Address match detection function	XXXXXXXXB
1FF4H	Program address detection register 1 (Middle order address)				
1FF5H	Program address detection register 1 (High order address)				

* : These registers are only for MB90485B series.
They are used as the reserved area on MB90480B series.

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Descriptions for read/write

R/W	: Readable and writable
R	: Read only
W	: Write only

Descriptions for initial value

0	: The initial value of this bit is “0”.
1	: The initial value of this bit is “1”.
X	: The initial value of this bit is undefined.
-	: This bit is not used.
*	: The initial value of this bit is “1” or “0”. The value depends on the mode pin (MD2, MD1 and MD0) .
+	: The initial value of this bit is “1” or “0”. The value depends on the RAM area of device.

■ INTERRUPT SOURCES, INTERRUPT VECTORS, AND INTERRUPT CONTROL REGISTERS

Interrupt source	Clear of EI²OS	μDMAC channel number	Interrupt vector		Interrupt control register	
			Number	Address	Number	Address
Reset	×	—	#08	FFFFDC$_H$	—	—
INT9 instruction	×	—	#09	FFFFD8$_H$	—	—
Exception	×	—	#10	FFFFD4$_H$	—	—
INT0 (IRQ0)	○	0	#11	FFFFD0$_H$	ICR00	0000B0$_H$
INT1 (IRQ1)	○	×	#12	FFFFCC$_H$		
INT2 (IRQ2)	○	×	#13	FFFFC8$_H$	ICR01	0000B1$_H$
INT3 (IRQ3)	○	×	#14	FFFFC4$_H$		
INT4 (IRQ4)	○	×	#15	FFFFC0$_H$	ICR02	0000B2$_H$
INT5 (IRQ5)	○	×	#16	FFFFBC$_H$		
INT6 (IRQ6)	○	×	#17	FFFFB8$_H$	ICR03	0000B3$_H$
INT7 (IRQ7)	○	×	#18	FFFFB4$_H$		
PWC1 (MB90485B series only)	○	×	#19	FFFFB0$_H$	ICR04	0000B4$_H$
PWC2 (MB90485B series only)	○	×	#20	FFFFAC$_H$		
PWC0 (MB90485B series only)	○	1	#21	FFFFA8$_H$	ICR05	0000B5$_H$
PPG0/PPG1 counter borrow	×	×	#22	FFFFA4$_H$		
PPG2/PPG3 counter borrow	×	×	#23	FFFFA0$_H$	ICR06	0000B6$_H$
PPG4/PPG5 counter borrow	×	×	#24	FFFF9C$_H$		
8/16-bit up/down counter/ timer (ch.0, ch.1) compare/ underflow/overflow/up/down inversion	○	×	#25	FFFF98$_H$	ICR07	0000B7$_H$
Input capture (ch.0) load	○	5	#26	FFFF94$_H$		
Input capture (ch.1) load	○	6	#27	FFFF90$_H$	ICR08	0000B8$_H$
Output compare (ch.0) match	○	8	#28	FFFF8C$_H$		
Output compare (ch.1) match	○	9	#29	FFFF88$_H$	ICR09	0000B9$_H$
Output compare (ch.2) match	○	10	#30	FFFF84$_H$		
Output compare (ch.3) match	○	×	#31	FFFF80$_H$	ICR10	0000BA$_H$
Output compare (ch.4) match	○	×	#32	FFFF7C$_H$		
Output compare (ch.5) match	○	×	#33	FFFF78$_H$	ICR11	0000BB$_H$
UART sending completed	○	11	#34	FFFF74$_H$		
16-bit free-run timer overflow, 16-bit reload timer underflow*2	○	12	#35	FFFF70$_H$	ICR12	0000BC$_H$
UART receiving completed	◎	7	#36	FFFF6C$_H$		
SIO1 (ch.0)	○	13	#37	FFFF68$_H$	ICR13	0000BD$_H$
SIO2 (ch.1)	○	14	#38	FFFF64$_H$		

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Interrupt source	Clear of EI²OS	μDMAC channel number	Interrupt vector		Interrupt control register	
			Number	Address	Number	Address
I²C interface (MB90485B series only)	×	×	#39	FFFF60H	ICR14	0000BEH
A/D converter	○	15	#40	FFFF5CH		
Flash write/erase, timebase timer, watch timer *1	×	×	#41	FFFF58H	ICR15	0000BFH
Delay interrupt generator module	×	×	#42	FFFF54H		

× : Interrupt request flag is not cleared by the interrupt clear signal.
○ : Interrupt request flag is cleared by the interrupt clear signal.
◎ : Interrupt request flag is cleared by the interrupt clear signal (stop request present) .

*1 : The Flash write/erase, timebase timer, and watch timer cannot be used at the same time.

*2 : When the 16-bit reload timer underflow interrupt is changed from enable (TMCSR : INTE = 1) to disable (TMCSR : INTE = 0) , disable the interrupt in the interrupt control register (ICR12 : IL2 to IL0 =111B) , then set the INTE bit to 0.

Note : If there are two interrupt sources for the same interrupt number, the resource will clear both interrupt request flags at the EI²OS/μDMAC interrupt clear signal. Therefore if either of the two sources uses the EI²OS/μDMAC function, the other interrupt function cannot be used. The interrupt request enable bit for the corresponding resource should be set to “0” and interrupt requests from that resource should be handled by software polling.

■ PERIPHERAL RESOURCES

1. I/O Ports

The I/O ports perform the functions of either sending data from the CPU to the I/O pins, or loading information from the I/O into the CPU, according to the setting of the corresponding port data register (PDR) . The input/output direction of each I/O pin can be set in individual bit units by the port direction register (DDR) for each I/O port. The MB90480B/485B series has 84 input/output pins. The I/O ports are port 0 through port A.

(1) Port Data Registers

	7	6	5	4	3	2	1	0	Initial value	Access
PDR0 Address : 000000H	P07	P06	P05	P04	P03	P02	P01	P00	Undefined	R/W*1
PDR1 Address : 000001H	P17	P16	P15	P14	P13	P12	P11	P10	Undefined	R/W*1
PDR2 Address : 000002H	P27	P26	P25	P24	P23	P22	P21	P20	Undefined	R/W*1
PDR3 Address : 000003H	P37	P36	P35	P34	P33	P32	P31	P30	Undefined	R/W*1
PDR4 Address : 000004H	P47	P46	P45	P44	P43	P42	P41	P40	Undefined	R/W*1
PDR5 Address : 000005H	P57	P56	P55	P54	P53	P52	P51	P50	Undefined	R/W*1
PDR6 Address : 000006H	P67	P66	P65	P64	P63	P62	P61	P60	Undefined	R/W*1
PDR7 Address : 000007H	P77	P76	P75	P74	P73	P72	P71	P70	Undefined*2	R/W*1
PDR8 Address : 000008H	P87	P86	P85	P84	P83	P82	P81	P80	Undefined	R/W*1
PDR9 Address : 000009H	P97	P96	P95	P94	P93	P92	P91	P90	Undefined	R/W*1
PDRA Address : 00000AH	—	—	—	—	PA3	PA2	PA1	PA0	Undefined	R/W*1

*1 : The R/W indication for I/O ports is somewhat different than R/W access to memory, and involves the following operations.

- Input mode
  Read : Reads the corresponding signal pin level.
  Write : Writes to the output latch.
- Output mode
  Read : Reads the value from the data register latch.
  Write : Outputs the value to the corresponding signal pin.

*2 : The initial value of this bit is “11XXXXXXB” on MB90485B series.

(2) Port Direction Registers

	7	6	5	4	3	2	1	0	Initial value	Access
DDR0 Address : 000010H	D07	D06	D05	D04	D03	D02	D01	D00	00000000B	R/W
DDR1 Address : 000011H	D17	D16	D15	D14	D13	D12	D11	D10	00000000B	R/W
DDR2 Address : 000012H	D27	D26	D25	D24	D23	D22	D21	D20	00000000B	R/W
DDR3 Address : 000013H	D37	D36	D35	D34	D33	D32	D31	D30	00000000B	R/W
DDR4 Address : 000014H	D47	D46	D45	D44	D43	D42	D41	D40	00000000B	R/W
DDR5 Address : 000015H	D57	D56	D55	D54	D53	D52	D51	D50	00000000B	R/W
DDR6 Address : 000016H	D67	D66	D65	D64	D63	D62	D61	D60	00000000B	R/W
DDR7 Address : 000017H	D77*1	D76*1	D75	D74	D73	D72	D71	D70	00000000B*2	R/W
DDR8 Address : 000018H	D87	D86	D85	D84	D83	D82	D81	D80	00000000B	R/W
DDR9 Address : 000019H	D97	D96	D95	D94	D93	D92	D91	D90	00000000B	R/W
DDRA Address : 00001AH	—	—	—	—	DA3	DA2	DA1	DA0	----0000B	R/W

*1 : The value is set to "—" on MB90485B series only.

*2 : The initial value of this bit is "XX000000B" on MB90485B series only.

- When a set of pins is functioning as a port, the corresponding signal pins are controlled as follows.
  0 : Input mode.
  1 : Output mode. Reset to "0".

Notes :
- When any of these registers are accessed using a read-modify-write type instruction (such as a bit set instruction) , the bit specified in the instruction will be set to the indicated value. However, the contents of output registers corresponding to any other bits having input settings will be rewritten to the input values of those pins at that time.
  For this reason, when changing any pin that has been used for input to output, first write the desired value to the PDR register before setting the DDR register for output.
- P76, P77 (MB90485B series only)
  This port has no DDR. To use P77 and P76 as I²C pins, set the PDR value to "1" so that port data remains enabled (to use P77 and P76 for general purposes, disable I²C) . The port is an open drain output (with no P-ch) .
  To use it as an input port, therefore, set the PDR to "1" to turn off the output transistor and add a pull-up resistor to the external output.

(3) Port Input Resistance Registers

	7	6	5	4	3	2	1	0	Initial value	Access
RDR0 Address : 00001C$_H$	RD07	RD06	RD05	RD04	RD03	RD02	RD01	RD00	00000000$_B$	R/W
RDR1 Address : 00001D$_H$	RD17	RD16	RD15	RD14	RD13	RD12	RD11	RD10	00000000$_B$	R/W

These registers control the use of pull-up resistance in input mode.
0 : No pull-up resistance in input mode.
1 : With pull-up resistance in input mode.

In output mode, these registers have no function (no pull-up resistance) . Input/output mode settings are controlled by the setting of port direction (DDR) registers.
In case of a stop (SPL = 1) , no pull-up resistance is applied (high impedance) . Using of this function is prohibited when an external bus is used. Do not write to these registers.

(4) Port Output Pin Registers

	7	6	5	4	3	2	1	0	Initial value	Access
ODR7 Address : 00001E$_H$	OD77*1	OD76*1	OD75	OD74	OD73	OD72	OD71	OD70	00000000$_B$*2	R/W
ODR4 Address : 00001B$_H$	OD47	OD46	OD45	OD44	OD43	OD42	OD41	OD40	00000000$_B$	R/W

*1 : The value is set to "—" on MB90485B series only.

*2 : The initial value of this bit is "XX000000$_B$" on MB90485B series only.

These registers control open drain settings in output mode.
0 : Standard output port functions in output mode.
1 : Open drain output port in output mode.

In input mode, these registers have no function (Hi-Z output) . Input/output mode settings are controlled by the setting of port direction (DDR) registers. Using of this function is prohibited when an external bus is used. Do not write to these registers.

(5) Analog Input Enable Register

	7	6	5	4	3	2	1	0	Initial value	Access
ADER Address : 00001F$_H$	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0	11111111$_B$	R/W

This register controls the port 6 pins as follows.
0 : Port input/output mode.
1 : Analog input mode. The default value at reset is all "1".

(6) Up/down Timer Input Enable Register

	7	6	5	4	3	2	1	0	Initial value	Access
UDER Address : 00000B$_H$	—	—	UDE5	UDE4	UDE3	UDE2	UDE1	UDE0	XX000000$_B$	R/W

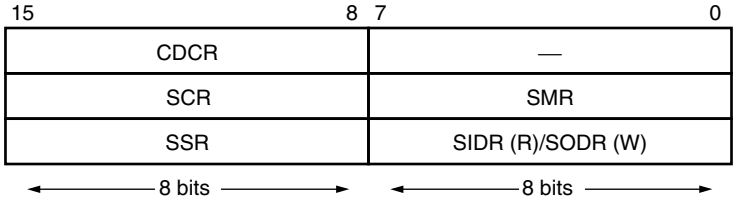
This register controls the port 3 pins as follows.
0 : Port input mode.
1 : Up/down timer input mode.The default value at reset is "0".

2. UART

The UART is a serial I/O port for asynchronous (start-stop synchronized) communication as well as CLK synchronized communication.

- Full duplex double buffer
- Transfer modes : asynchronous (start-stop synchronized) , or CLK synchronized (no start bit or stop bit) .
- Multi-processor mode supported.
- Embedded proprietary baud rate generator
  Asynchronous : 76923/38461/19230/9615/500 k/250 kbps
  CLK synchronized : 16 M/8 M/4 M/2 M/1 M/500 kbps
- External clock setting available, allows use of any desired baud rate.
- Can use internal clock feed from PPG1.
- Data length : 7-bit (asynchronous normal mode only) or 8-bit.
- Master/slave type communication functions (in multi-processor mode) .
- Error detection functions (parity, framing, overrun)
- Transfer signals are NRZ encoded.
- μDMAC supported (for receiving/sending)

(1) Register List



Serial mode register (SMR)

000020H

7	6	5	4	3	2	1	0	
MD1	MD0	CS2	CS1	CS0	Reserved	SCKE	SOE	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	X	0	0	Initial value

Serial control register (SCR)

000021H

15	14	13	12	11	10	9	8	
PEN	P	SBL	CL	A/D	REC	RXE	TXE	
R/W	R/W	R/W	R/W	R/W	W	R/W	R/W	
0	0	0	0	0	1	0	0	Initial value

Serial I/O register (SIDR/SODR)

000022H

7	6	5	4	3	2	1	0	
D7	D6	D5	D4	D3	D2	D1	D0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
X	X	X	X	X	X	X	X	Initial value

Serial status register (SSR)

000023H

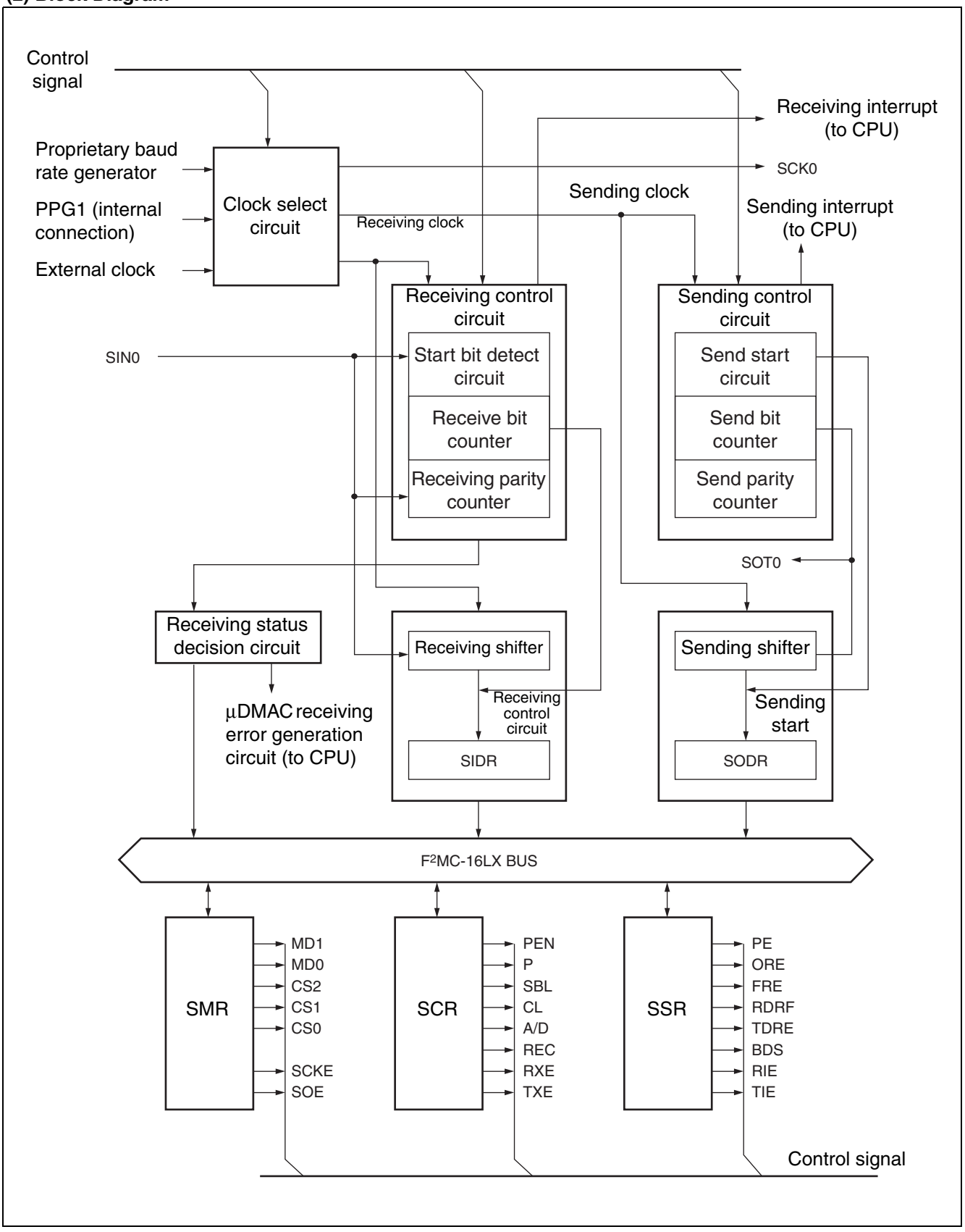
15	14	13	12	11	10	9	8	
PE	ORE	FRE	RDRF	TDRE	BDS	RIE	TIE	
R	R	R	R	R	R/W	R/W	R/W	
0	0	0	0	1	0	0	0	Initial value

Communication prescaler control register (CDCR)

000025H

15	14	13	12	11	10	9	8	
MD	SRST	—	—	DIV3	DIV2	DIV1	DIV0	
R/W	R/W	—	—	R/W	R/W	R/W	R/W	
0	0	—	—	0	0	0	0	Initial value

(2) Block Diagram



3. Expanded I/O Serial Interface

The expanded I/O serial interface is an 8-bit × 1-channel serial I/O interface for clock synchronized data transfer. A selection of LSB-first or MSB-first data transfer is provided.

There are two serial I/O operation modes.

- Internal shift clock mode : Data transfer is synchronized with the internal clock signal.
- External shift clock mode : Data transfer is synchronized with a clock signal input from the external clock signal pin (SCK) . In this mode the general-purpose port that shares the external clock signal pin (SCK) can be used for transfer according to CPU instructions.

(1) Register List

Serial mode control status register 0/1 (SMCS0, SMCS1)

	15	14	13	12	11	10	9	8	Initial value
Address : 000027H 00002BH	SMD2	SMD1	SMD0	SIE	SIR	BUSY	STOP	STRT	00000010B
	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	

	7	6	5	4	3	2	1	0	
Address : 000026H 00002AH	—	—	—	—	MODE	BDS	SOE	SCOE	----0000B
	—	—	—	—	R/W	R/W	R/W	R/W	

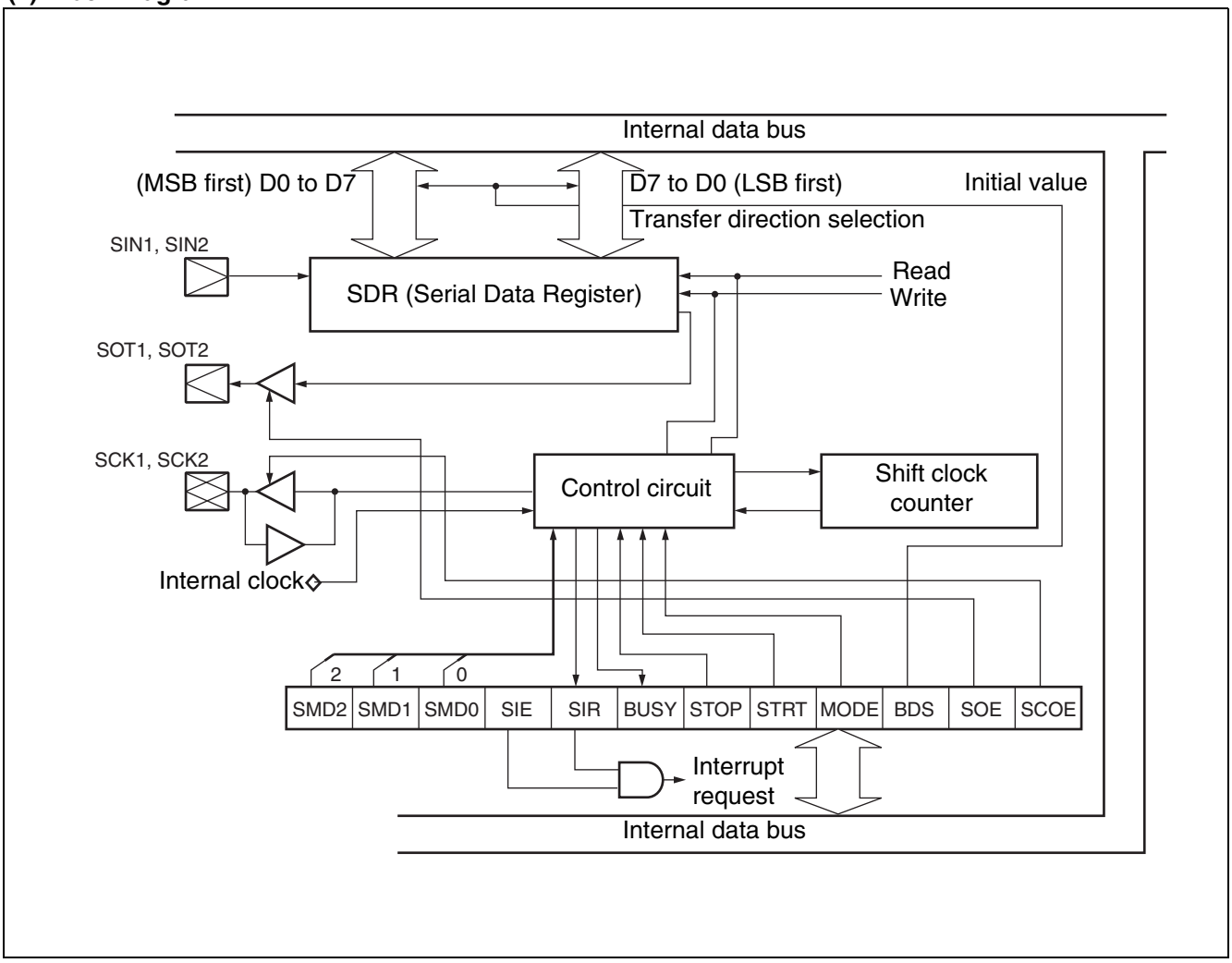
Serial data register 0/1 (SDR0, SDR1)

	7	6	5	4	3	2	1	0	
Address : 000028H 00002CH	D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXXB
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Communication prescaler control register 0/1 (SDCR0, SDCR1)

	15	14	13	12	11	10	9	8	
Address : 000029H 00002DH	MD	—	—	—	DIV3	DIV2	DIV1	DIV0	0---0000B
	R/W	—	—	—	R/W	R/W	R/W	R/W	

(2) Block Diagram



4. 8/10-bit A/D Converter

The A/D converter converts analog input voltage to digital values, and provides the following features.

- Conversion time : minimum 3.68 μs per channel
  (92 machine cycles at 25 MHz machine clock, including sampling time)
- Sampling time : minimum 1.92 μs per channel
  (48 machine cycles at 25 MHz machine clock)
- RC sequential comparison conversion method, with sample & hold circuit.
- 8-bit or 10-bit resolution
- Analog input selection of 8 channels
  Single conversion mode : Conversion from one selected channel.
  Scan conversion mode : Conversion from multiple consecutive channels, programmable selection of up to 8 channels.
  Continuous conversion mode : Repeated conversion of specified channels.
  Stop conversion mode : Conversion from one channel followed by a pause until the next activation allows to synchronize with conversion start.
- At the end of A/D conversion, an A/D conversion completed interrupt request can be generated to the CPU. The interrupt can be used activate the μDMAC in order to transfer the results of A/D conversion to memory for efficient continuous processing.
- The starting factor conversion may be selected from software, external trigger (falling edge) , or timer (rising edge) .

(1) Register List

ADCS2, ADCS1 (Control status register)

ADCS1

Address : 000046H

7	6	5	4	3	2	1	0	
MD1	MD0	ANS2	ANS1	ANS0	ANE2	ANE1	ANE0	
0	0	0	0	0	0	0	0	← Initial value
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	← Bit attributes

ADCS2

Address : 000047H

15	14	13	12	11	10	9	8	
BUSY	INT	INTE	PAUS	STS1	STS0	STRT	Reserved	
0	0	0	0	0	0	0	0	← Initial value
R/W	R/W	R/W	R/W	R/W	R/W	W	R/W	← Bit attributes

ADCR2, ADCR1 (Data register)

ADCR1

Address : 000048H

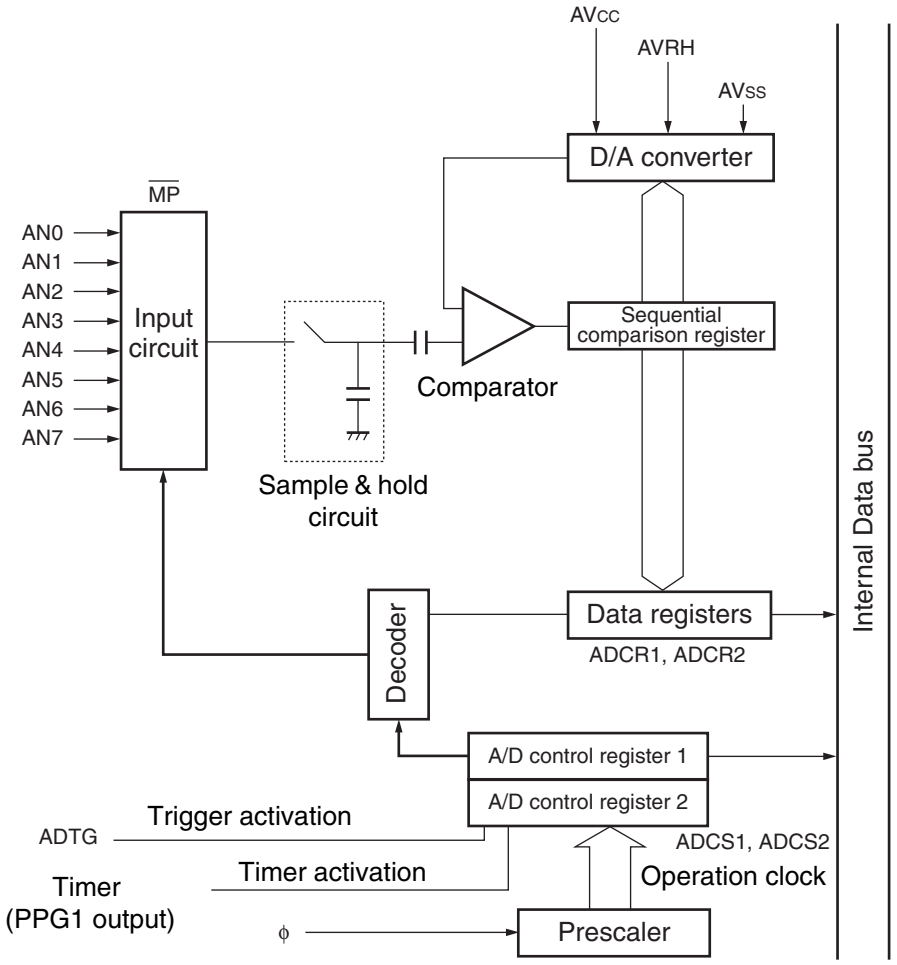
7	6	5	4	3	2	1	0	
D7	D6	D5	D4	D3	D2	D1	D0	
X	X	X	X	X	X	X	X	← Initial value
R	R	R	R	R	R	R	R	← Bit attributes

ADCR2

Address : 000049H

15	14	13	12	11	10	9	8	
S10	ST1	ST0	CT1	CT0	—	D9	D8	
0	0	0	0	0	X	X	X	← Initial value
W	W	W	W	W	R	R	R	← Bit attributes

(2) Block Diagram



5. 8/16-bit PPG

The 8/16-bit PPG is an 8-bit reload timer module that produces a PPG output using a pulse from the timer operation. Hardware resources include 6 × 8-bit down counters, 12 × 8-bit reload timers, 3 × 16-bit control registers, 6 × external pulse output pins, and 6 × interrupt outputs. Note that MB90480B/485B series has six channels for 8-bit PPG use, which can also be combined as PPG0 + PPG1, PPG2 + PPG3, and PPG4 + PPG5 to operate as a three-channel 16-bit PPG. The following is a summary of functions.

- 8-bit PPG output 6-channel independent mode : Provides PPG output operation on six independent channels.
- 16-bit PPG output operation mode : Provides 16-bit PPG output on three channels. The six original channels are used in combination as PPG0 + PPG1, PPG2 + PPG3, and PPG4 + PPG5.
- 8 + 8-bit PPG output operation mode : Output from PPG0 (PPG2/PPG4) is used as clock input to PPG1 (PPG3/PPG5) to provide to 8-bit PPG output at any desired period length.
- PPG output operation : Produces pulse waves at any desired period and duty ratio. The PPG module can also be used with external circuits as a D/A converter.

(1) Register List

PPGC0/PPGC2/PPGC4 (PPG0/PPG2/PPG4 operation mode control register)

	7	6	5	4	3	2	1	0	
00003AH 00003CH 00003EH	PEN0	—	PE00	PIE0	PUF0	—	—	Reserved	
	R/W	—	R/W	R/W	R/W	—	—	—	Read/write
	0	X	0	0	0	X	X	1	Initial value

PPGC1/PPGC3/PPGC5 (PPG1/PPG3/PPG5 operation mode control register)

	15	14	13	12	11	10	9	8	
00003BH 00003DH 00003FH	PEN1	—	PE10	PIE1	PUF1	MD1	MD0	Reserved	
	R/W	—	R/W	R/W	R/W	R/W	R/W	—	Read/write
	0	X	0	0	0	0	0	1	Initial value

PPG01/PPG23/PPG45 (PPG0 to PPG5 output control register)

	7	6	5	4	3	2	1	0	
000040H 000042H 000044H	PCS2	PCS1	PCS0	PCM2	PCM1	PCM0	Reserved	Reserved	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Read/write
	0	0	0	0	0	0	0	0	Initial value

PRLL0 to PRLL5 (Reload register L)

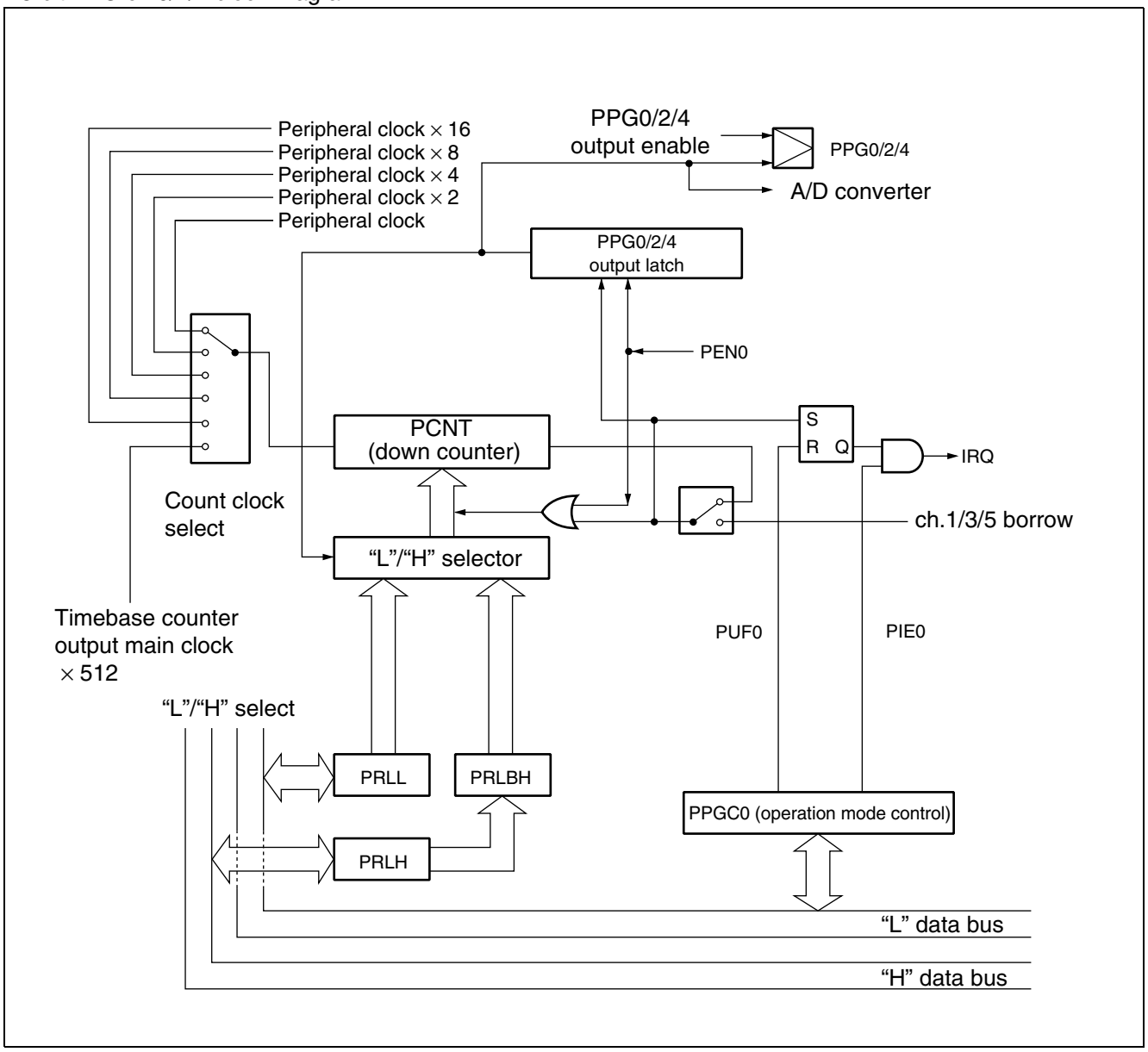
	7	6	5	4	3	2	1	0	
00002EH 000030H 000032H 000034H 000036H 000038H	D07	D06	D05	D04	D03	D02	D01	D00	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Read/write
	X	X	X	X	X	X	X	X	Initial value

PRLH0 to PRLH5 (Reload register H)

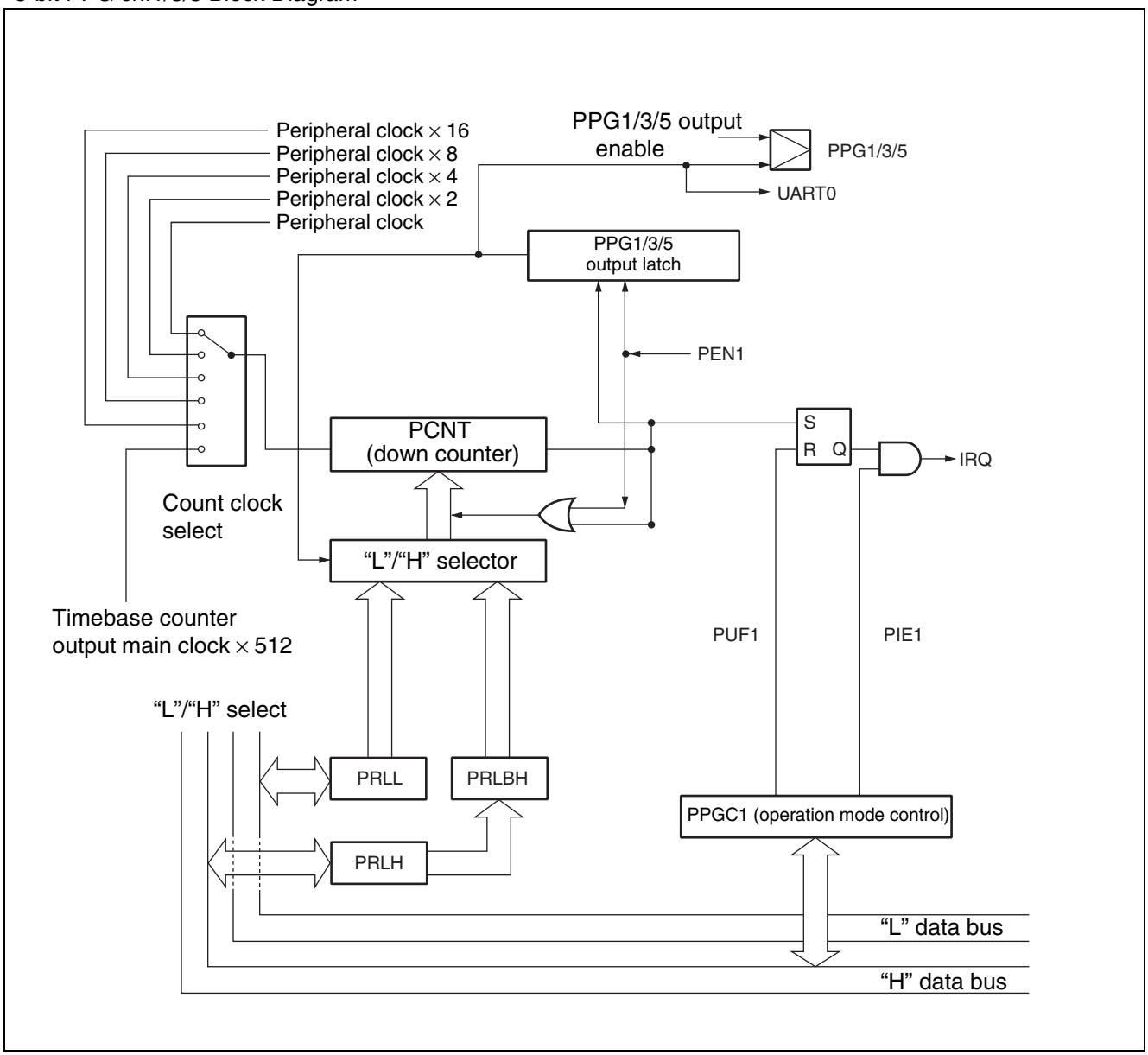
	15	14	13	12	11	10	9	8	
00002FH 000031H 000033H 000035H 000037H 000039H	D15	D14	D13	D12	D11	D10	D09	D08	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Read/write
	X	X	X	X	X	X	X	X	Initial value

(2) Block Diagram

•8-bit PPG ch.0/2/4 block Diagram



• 8-bit PPG ch.1/3/5 Block Diagram



6. 8/16-bit up/down Counter/Timer

8/16-bit up/down counter/timer consists of up/down counter/timer circuits including six event input pins, two 8-bit up/down counters, two 8-bit reload/compare registers, as well as the related control circuits.

(1) Principal Functions

- 8-bit count register enables counting in the range 0 to 256.
  (In 16-bit × 1 mode, counting is enabled in the range 0 to 65535)
- Count clock selection provides four count modes.

Count modes
- Timer mode
- Up/down count mode
- Phase differential down count mode (× 2)
- Phase differential down count mode (× 8)

- In timer mode, there is a choice of two internal count clock signals.

Count clock (at 16 MHz operation)
- 125 ns (8 MHz : × 2)
- 0.5 µs (2 MHz : × 8)

- In up/down count mode, there is a choice of trigger edge detection for the input signal from external pins.

Edge detection
- Falling edge detection
- Rising edge detection
- Both rising/falling edge detection
- Edge detection disabled

- In phase differential count mode, to handle encoder counting for motors, the encoder A-phase, B-phase, and Z-phase are each input, enabling easy and highly accurate counting of angle of rotation, speed of rotation, etc.
- The ZIN pin provides a selection of two functions.

ZIN pin
- Counter clear function
- Gate functions

- A compare function and reload function are provided, each for use separately or in combination. Both functions can be activated together for up/down counting in any desired bandwidth.

Compare/reload function
- Compare function (output interrupt at compare events)
- Compare function (output interrupt and clear counter at compare events)
- Reload function (output interrupt and reload at underflow events)
- Compare/reload function (output interrupt and clear counter at compare events, output interrupt and reload at underflow events)
- Compare/reload disabled

- Individual control over interrupts at compare, reload (underflow) and overflow events.
- Count direction flag enables identification of the last previous count direction.
- Interrupt generated when count direction changes.

(2) Register List

15	8	7	0
UDCR1		UDCR0	
RCR1		RCR0	
Reserved area		CSR0	
CCRH0		CCRL0	
Reserved area		CSR1	
CCRH1		CCRL1	
8-bit		8-bit	

CCRH0 (Counter Control Register High ch.0)

Address : 00006D$_H$

15	14	13	12	11	10	9	8
M16E	CDCF	CFIE	CLKS	CMS1	CMS0	CES1	CES0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value 00000000$_B$

CCRH1 (Counter Control Register High ch.1)

Address : 000071$_H$

15	14	13	12	11	10	9	8
—	CDCF	CFIE	CLKS	CMS1	CMS0	CES1	CES0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value -0000000$_B$

CCRL0/1 (Counter Control Register Low ch.0/ch.1)

Address : 00006C$_H$
Address : 000070$_H$

7	6	5	4	3	2	1	0
UDMS	CTUT	UCRE	RLDE	UDCC	CGSC	CGE1	CGE0
R/W	W	R/W	R/W	W	R/W	R/W	R/W

Initial value 0X00X000$_B$

CSR0/1 (Counter Status Register ch.0/ch.1)

Address : 000072$_H$
Address : 000074$_H$

7	6	5	4	3	2	1	0
CSTR	CITE	UDIE	CMPF	OVFF	UDFF	UDF1	UDF0
R/W	R/W	R/W	R/W	R/W	R/W	R	R

Initial value 00000000$_B$

UDCR0/1 (Up Down Count Register ch.0/ch.1)

Address : 000069$_H$

15	14	13	12	11	10	9	8
D17	D16	D15	D14	D13	D12	D11	D10
R	R	R	R	R	R	R	R

Initial value 00000000$_B$

Address : 000068$_H$

7	6	5	4	3	2	1	0
D07	D06	D05	D04	D03	D02	D01	D00
R	R	R	R	R	R	R	R

Initial value 00000000$_B$

RCR0/1 (Reload/Compare Register ch.0/ch.1)

Address : 00006B$_H$

15	14	13	12	11	10	9	8
D17	D16	D15	D14	D13	D12	D11	D10
W	W	W	W	W	W	W	W

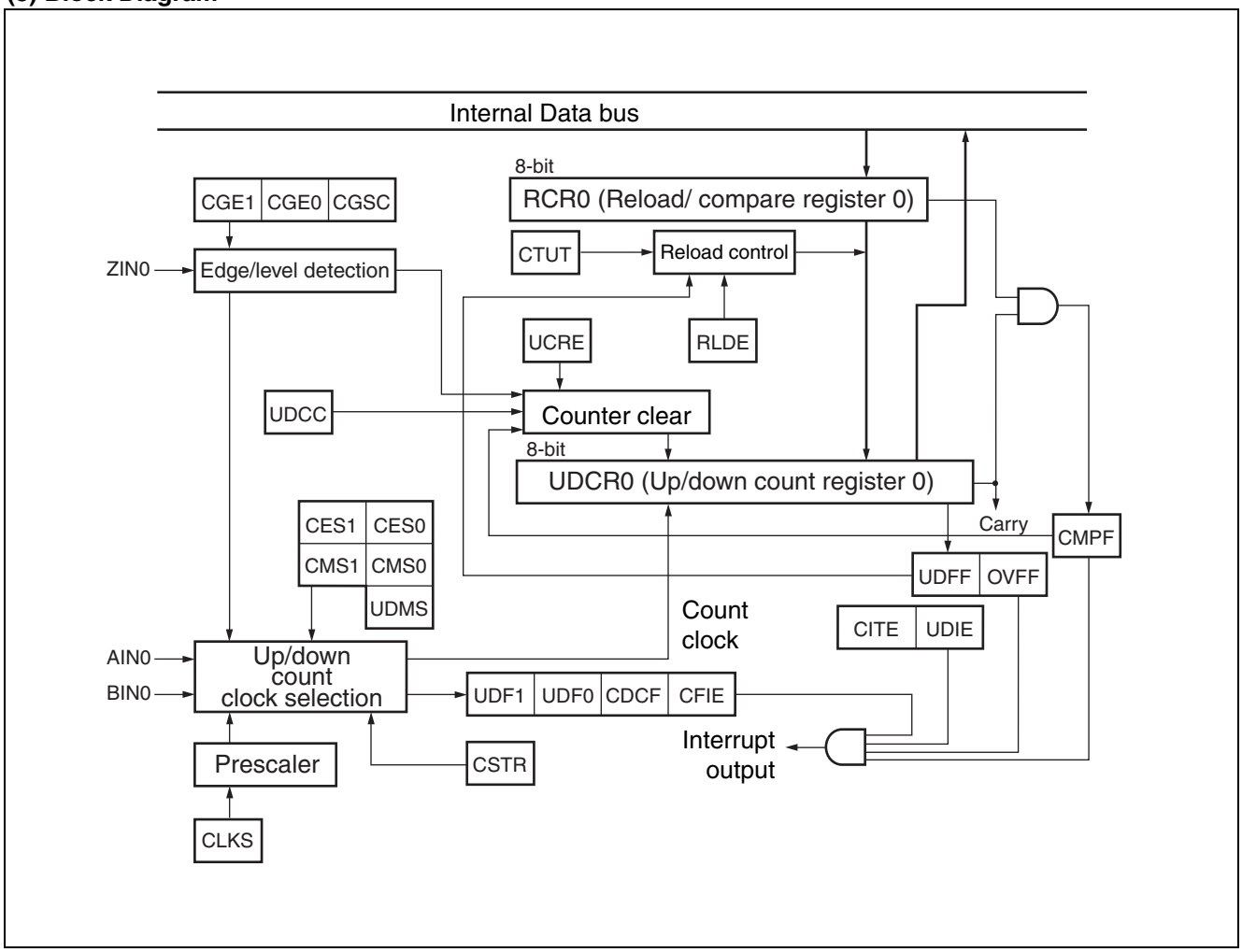
Initial value 00000000$_B$

Address : 00006A$_H$

7	6	5	4	3	2	1	0
D07	D06	D05	D04	D03	D02	D01	D00
W	W	W	W	W	W	W	W

Initial value 00000000$_B$

(3) Block Diagram



7. DTP/External Interrupt

The DTP (Data Transfer Peripheral) is a peripheral block that interfaces external peripherals to the F²MC-16LX CPU. The DTP receives DMA and interrupt processing requests from external peripherals and passes the requests to the F²MC-16LX CPU to activate the extended intelligent μDMAC or interrupt processing.

(1) Detailed Register Descriptions

Interrupt/DTP Enable Register (ENIR : Enable Interrupt Request Register)

ENIR
Address : 00000C$_H$

7	6	5	4	3	2	1	0
EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value
00000000$_B$

Interrupt/DTP Source Register (EIRR : External Interrupt Request Register)

EIRR
Address : 00000D$_H$

15	14	13	12	11	10	9	8
ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value
XXXXXXXX$_B$

Interrupt Level Setting Register (ELVR : External Level Register)

Address : 00000E$_H$

7	6	5	4	3	2	1	0
LB3	LA3	LB2	LA2	LB1	LA1	LB0	LA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

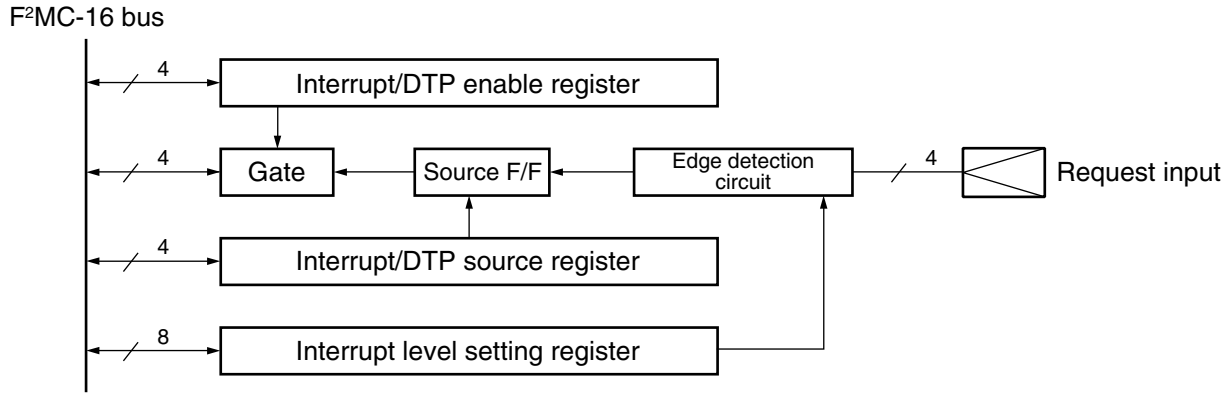
Initial value
00000000$_B$

Address : 00000F$_H$

15	14	13	12	11	10	9	8
LB7	LA7	LB6	LA6	LB5	LA5	LB4	LA4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value
00000000$_B$

(2) Block Diagram

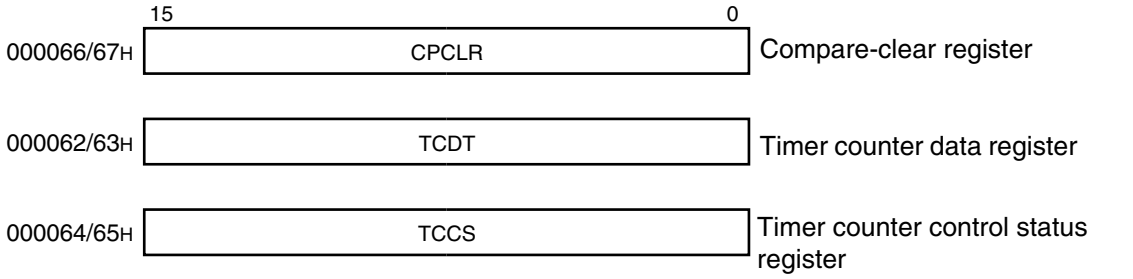


8. 16-bit Input/Output Timer

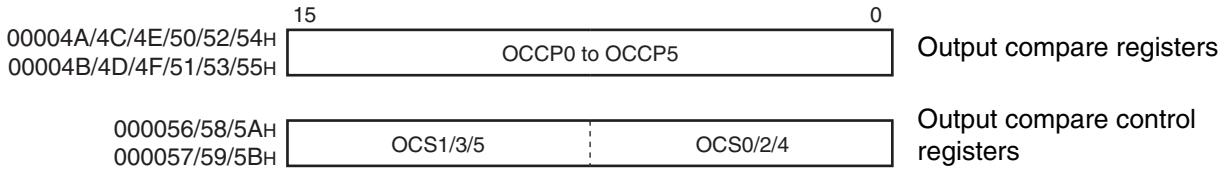
The 16-bit input/output timer module is composed of one 16-bit free-run timer, six output compare and two input capture modules. These functions can be used to output six independent wave form based on the 16-bit free-run timer, enabling input pulse width measurement and external clock frequency measurement.

- Register List

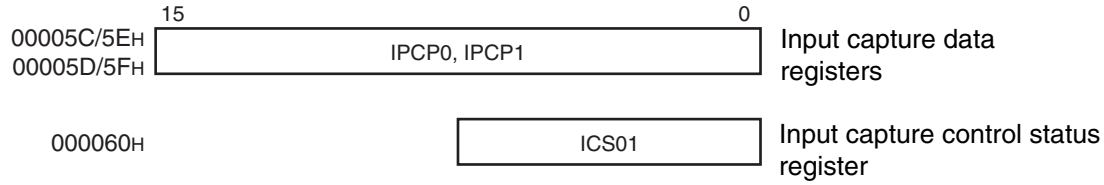
- 16-bit free-run timer



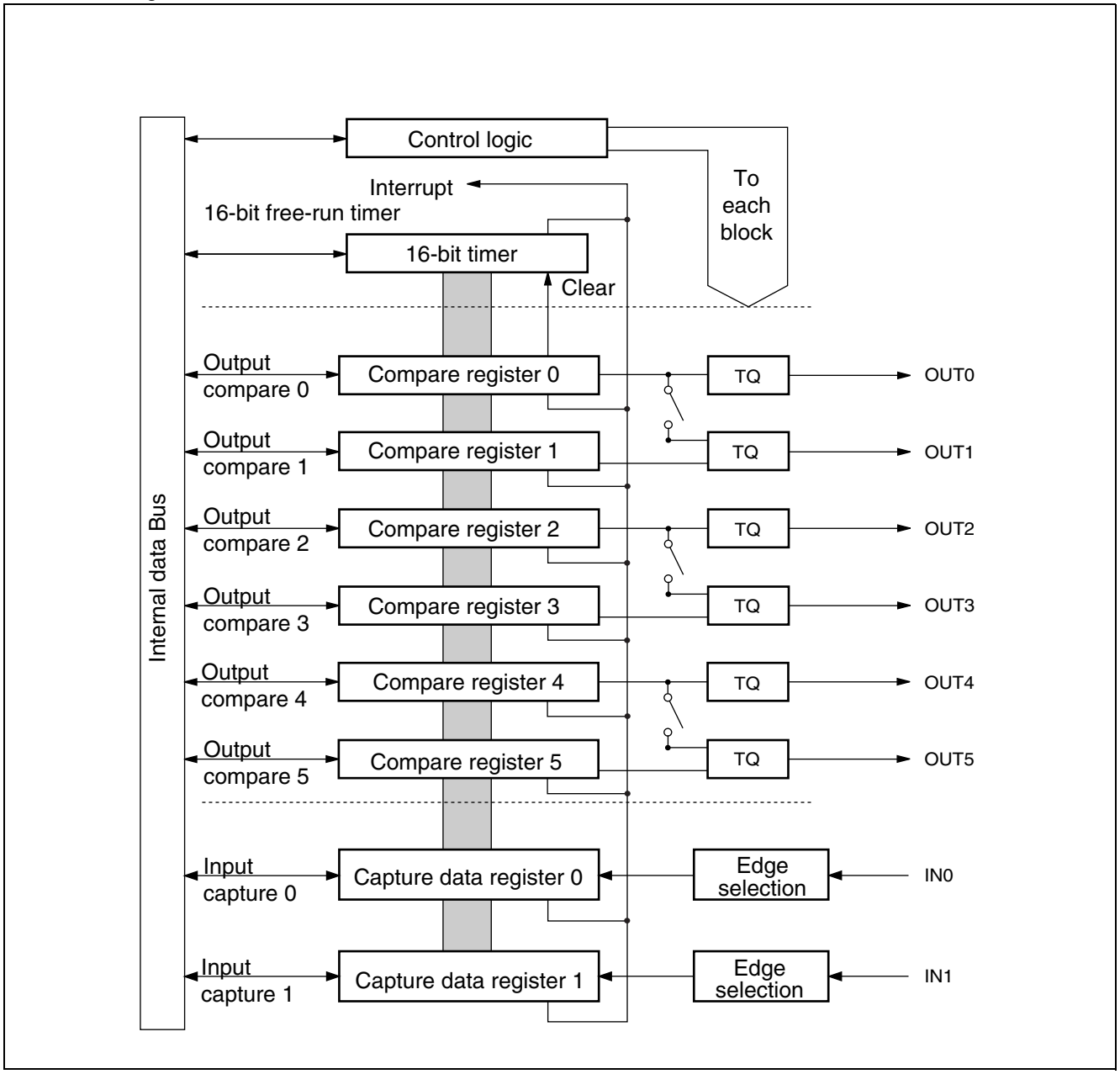
- 16-bit output compare



- 16-bit input capture



• Block Diagram



(1) 16-bit Free Run Timer

The 16-bit free-run timer is composed of a 16-bit up-down counter and control status register.
The counter value of this timer is used as the base timer for the input capture and output compare.

- The counter operation provides a choice of eight clock types.
- A counter overflow interrupt can be produced.
- A mode setting is available to initialize the counter value whenever the output compare value matches the value in the compare clear register.

- Register List

Compare clear register (CPCLR)

	15	14	13	12	11	10	9	8	Initial value
000067H	CL15	CL14	CL13	CL12	CL11	CL10	CL09	CL08	XXXXXXXXB
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

	7	6	5	4	3	2	1	0	Initial value
000066H	CL07	CL06	CL05	CL04	CL03	CL02	CL01	CL00	XXXXXXXXB
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Timer counter data register (TCDT)

	15	14	13	12	11	10	9	8	Initial value
000063H	T15	T14	T13	T12	T11	T10	T09	T08	00000000B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

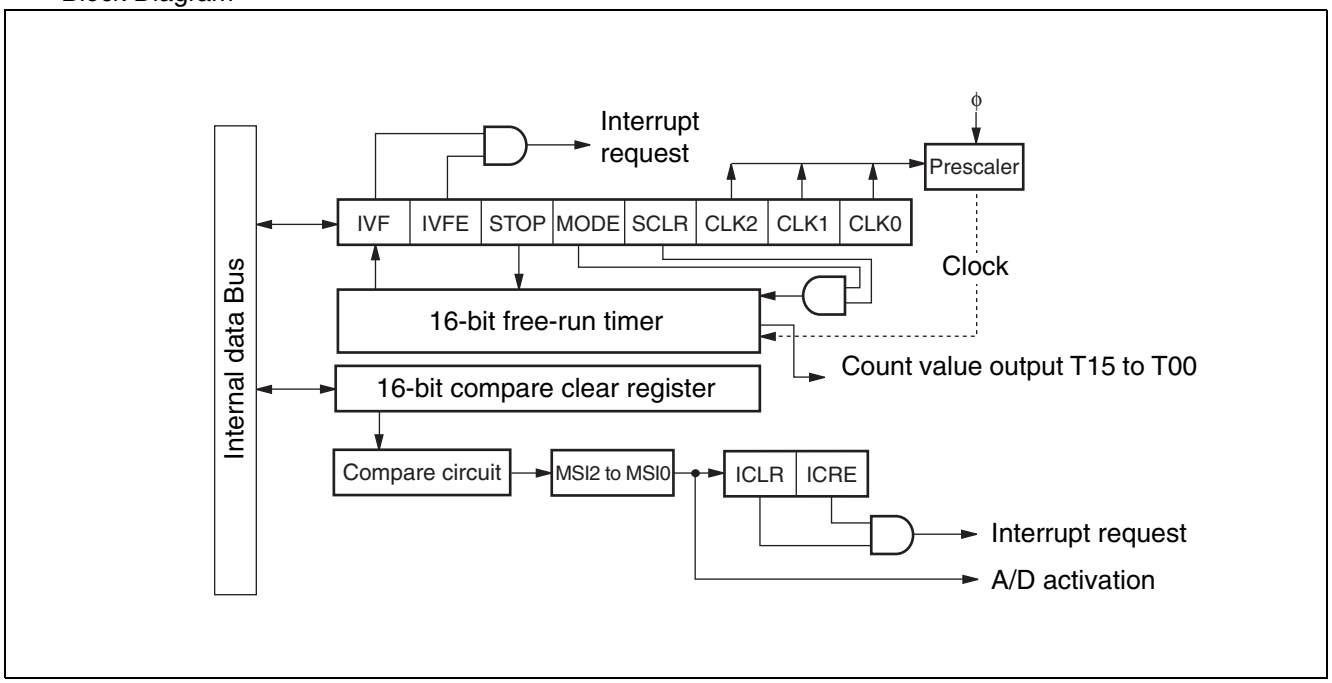
	7	6	5	4	3	2	1	0	Initial value
000062H	T07	T06	T05	T04	T03	T02	T01	T00	00000000B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Timer counter control status register (TCCS)

	15	14	13	12	11	10	9	8	Initial value
000065H	ECKE	—	—	MSI2	MSI1	MSI0	ICLR	ICRE	0--00000B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

	7	6	5	4	3	2	1	0	Initial value
000064H	IVF	IVFE	STOP	MODE	SCLR	CLK2	CLK1	CLK0	00000000B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

• Block Diagram



(2) Output Compare

The output compare module is composed of a 16-bit compare register, compare output pin unit, and control register. When the value in the compare register in this module matches the 16-bit free-run timer, the pin output levels can be inverted and an interrupt generated.

- There are six compare registers in all, each operating independently. A setting is available to allow two compare registers to be used to control output.
- Interrupts can be set in terms of compare match events.

- Register List

Output compare registers (OCCP0 to OCCP5)

	15	14	13	12	11	10	9	8	Initial value
00004BH 00004DH 00004FH 000051H 000053H 000055H	C15	C14	C13	C12	C11	C10	C09	C08	00000000B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

	7	6	5	4	3	2	1	0	Initial value
00004AH 00004CH 00004EH 000050H 000052H 000054H	C07	C06	C05	C04	C03	C02	C01	C00	00000000B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

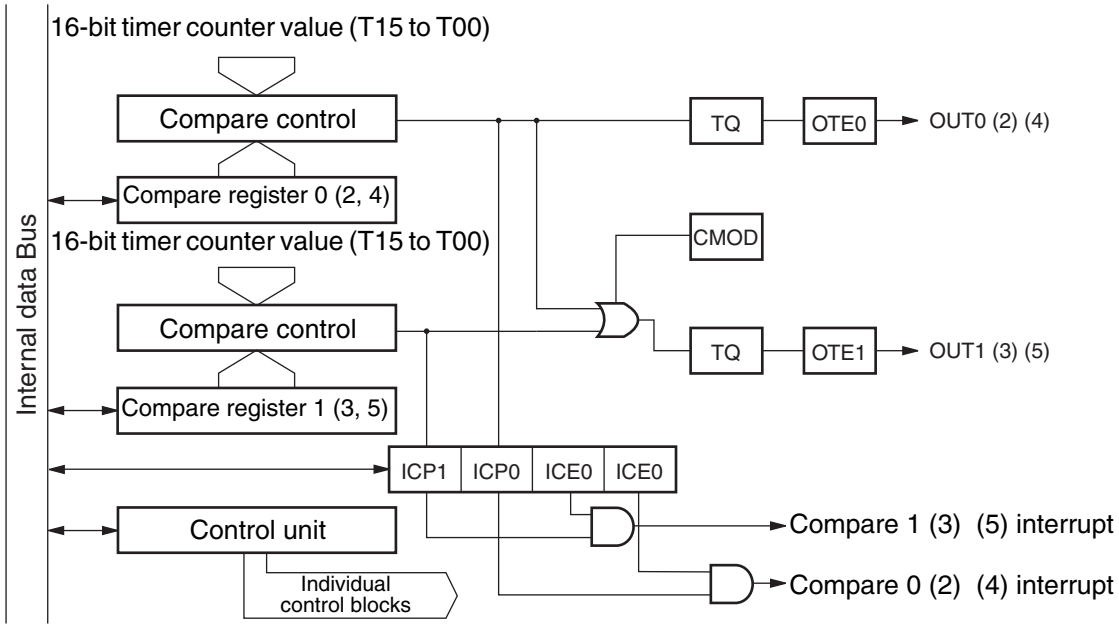
Output compare control registers (OCS1/OCS3/OCS5)

	15	14	13	12	11	10	9	8	Initial value
000057H 000059H 00005BH	—	—	—	CMOD	OTE1	OTE0	OTD1	OTD0	---00000B
	—	—	—	R/W	R/W	R/W	R/W	R/W	

Output compare control registers (OCS0/OCS2/OCS4)

	7	6	5	4	3	2	1	0	Initial values
000056H 000058H 00005AH	ICP1	ICP0	ICE1	ICE0	—	—	CST1	CST0	0000--00B
	R/W	R/W	R/W	R/W	—	—	R/W	R/W	

• Block Diagram



(3) Input Capture

The input capture module performs the functions of detecting the rising edge, falling edge, or both edges of signal input from external circuits, and saving the 16-bit free-run timer value at that moment to a register. An interrupt can also be generated at the instant of edge detection.

The input capture module consists of input capture registers and a control register. Each input capture module has its own external input pin.

- Selection of three types of valid edge for external input signals.
  Rising edge, falling edge, both edges.
- An interrupt can be generated when a valid edge is detected in the external input signal.

- Register List

Input capture data registers (IPCP0, IPCP1)

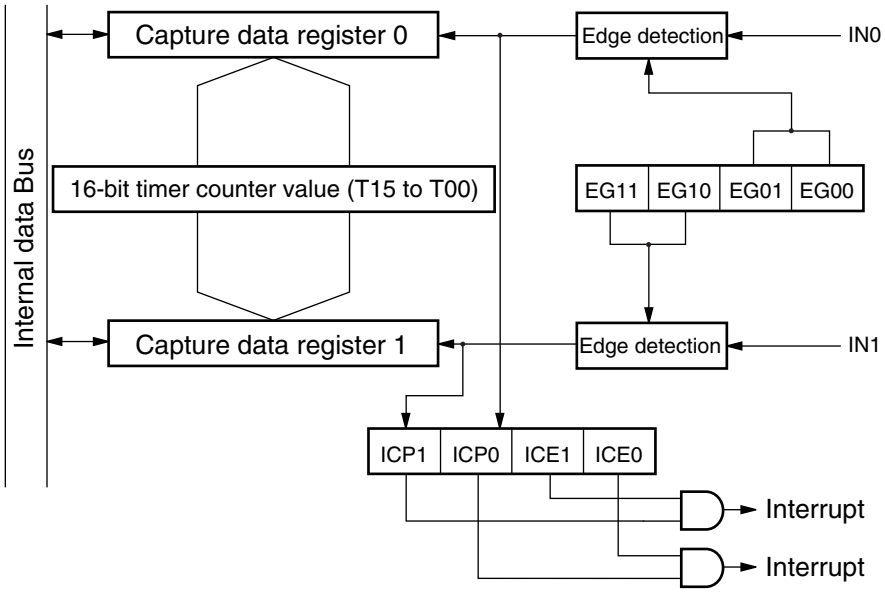
	15	14	13	12	11	10	9	8	Initial value
00005DH 00005FH	CP15	CP14	CP13	CP12	CP11	CP10	CP09	CP08	XXXXXXXXB
	R	R	R	R	R	R	R	R	

	7	6	5	4	3	2	1	0	Initial value
00005CH 00005EH	CP07	CP06	CP05	CP04	CP03	CP02	CP01	CP00	XXXXXXXXB
	R	R	R	R	R	R	R	R	

Input capture control status register (ICS01)

	7	6	5	4	3	2	1	0	Initial value
000060H	ICP1	ICP0	ICE1	ICE0	EG11	EG10	EG01	EG00	00000000B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Block Diagram



9. I²C Interface (MB90485B series only)

The I²C interface is a serial I/O port supporting the Inter IC BUS. Serves as a master/slave device on the I²C bus. The I²C interface has the following functions.

- Master/slave transmit/receive
- Arbitration function
- Clock synchronization
- Slave address/general call address detection function
- Forwarding direction detection function
- Start condition repeated generation and detection
- Bus error detection function

(1) Register List

Bus Status Register (IBSR)

000088H

7	6	5	4	3	2	1	0
BB	RSC	AL	LRB	TRX	AAS	GCA	FBT
R	R	R	R	R	R	R	R

Initial value
00000000B

Bus control register (IBCR)

000089H

15	14	13	12	11	10	9	8
BER	BEIE	SCC	MSS	ACK	GCAA	INTE	INT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value
00000000B

Clock control register (ICCR)

00008AH

7	6	5	4	3	2	1	0
—	—	EN	CS4	CS3	CS2	CS1	CS0
—	—	R/W	R/W	R/W	R/W	R/W	R/W

Initial value
--0XXXXXB

Address register (IADR)

00008BH

15	14	13	12	11	10	9	8
—	A6	A5	A4	A3	A2	A1	A0
—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value
-XXXXXXXB

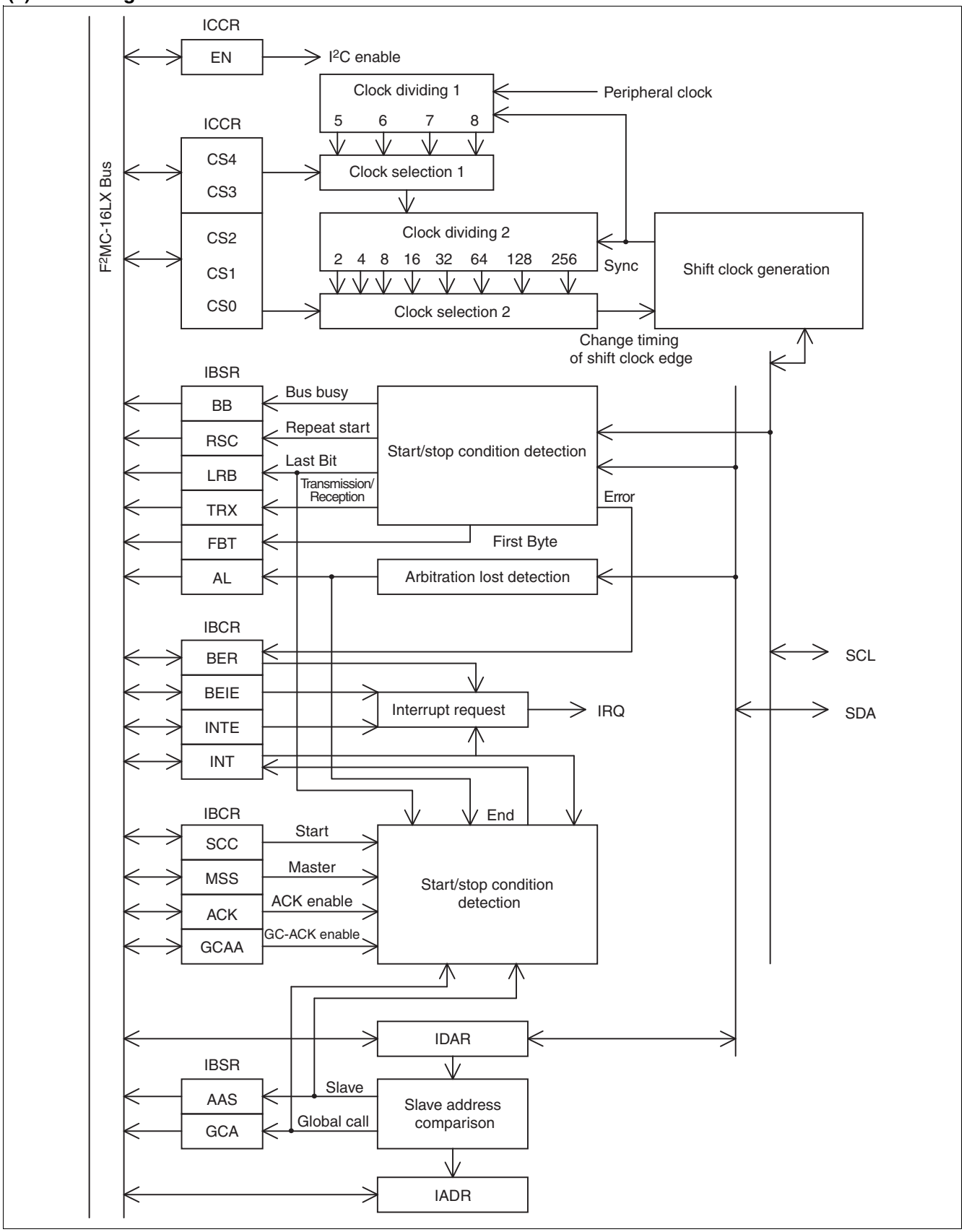
Data register (IDAR)

00008CH

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value
XXXXXXXXB

(2) Block Diagram



10. 16-bit Reload Timer

The 16-bit reload timer provides a choice of functions, including internal clock signals that count down in synchronization with three types of internal clock, as well as an event count mode that counts down at specified edge detection events in pulse signals input from external pins. This timer defines an underflow as a change in count value from 0000_H to $FFFF_H$. Thus an underflow will occur when counting from the value “reload register setting value + 1”. The choice of counting operations includes reload mode, in which the count setting values is reloaded and counting continues following an underflow event, and one-shot mode, in which an underflow event causes counting to stop. An interrupt can be generated at counter underflow, and the timer is DTC compatible.

(1) Register List

- TMCSR (Timer control status register)

Timer control status register (high) (TMCSR)

	15	14	13	12	11	10	9	8	
$0000CB_H$	—	—	—	—	CSL1	CSL0	MOD2	MOD1	
	—	—	—	—	R/W	R/W	R/W	R/W	Read/Write
	—	—	—	—	0	0	0	0	Initial value

Timer control status register (low) (TMCSR)

	7	6	5	4	3	2	1	0	
$0000CA_H$	MOD0	OUTE	OUTL	RELD	INTE	UF	CNTE	TRG	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Read/Write
	0	0	0	0	0	0	0	0	Initial value

- 16-bit timer register/16-bit reload register

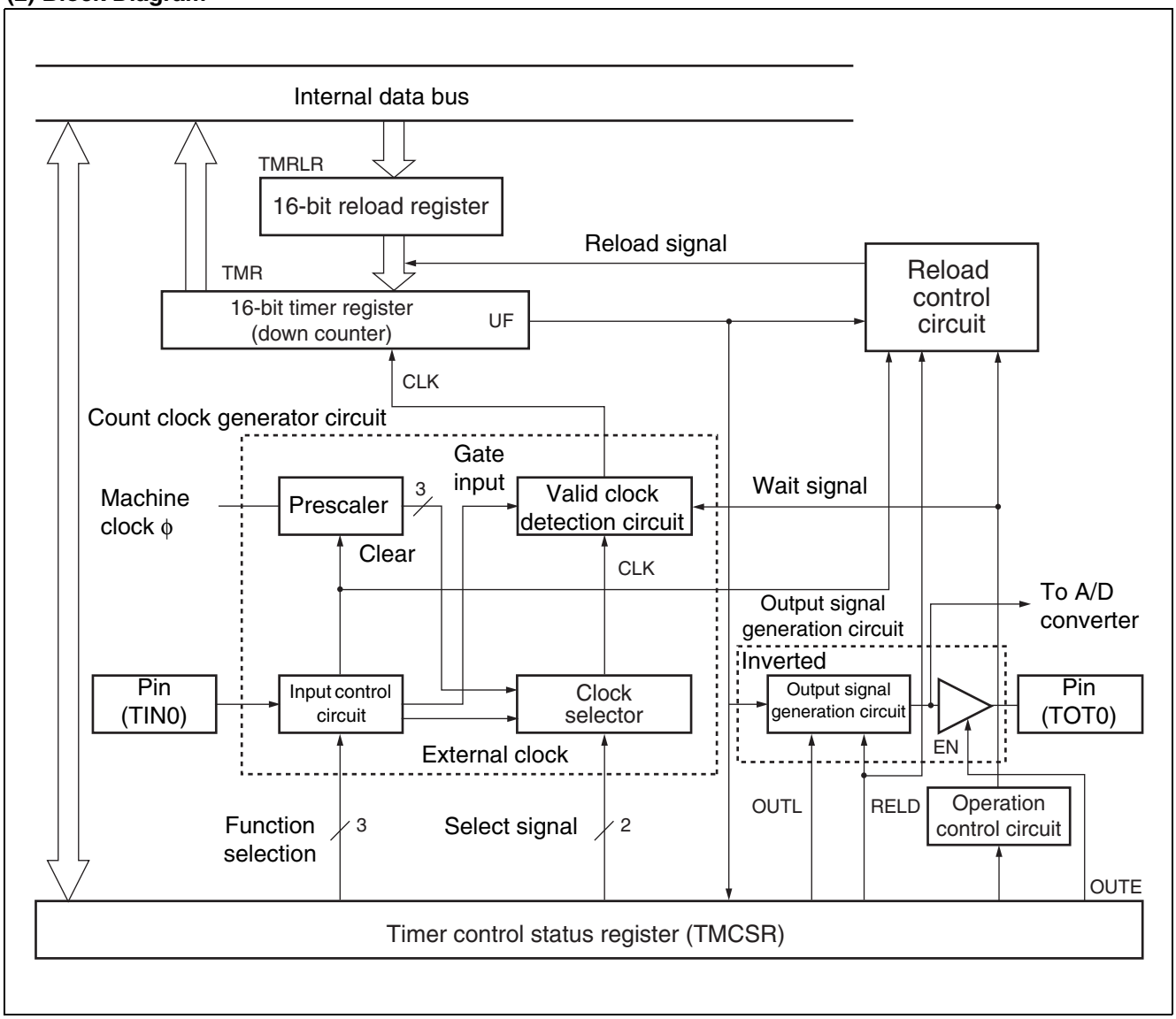
TMR/TMRLR (high)

	15	14	13	12	11	10	9	8	
$0000CD_H$	D15	D14	D13	D12	D11	D10	D09	D08	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Read/Write
	X	X	X	X	X	X	X	X	Initial value

TMR/TMRLR (low)

	7	6	5	4	3	2	1	0	
$0000CC_H$	D07	D06	D05	D04	D03	D02	D01	D00	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Read/Write
	X	X	X	X	X	X	X	X	Initial value

(2) Block Diagram



11. μPG Timer (MB90485B series only)

The μPG timer performs pulse output in response to the external input.

(1) Register List

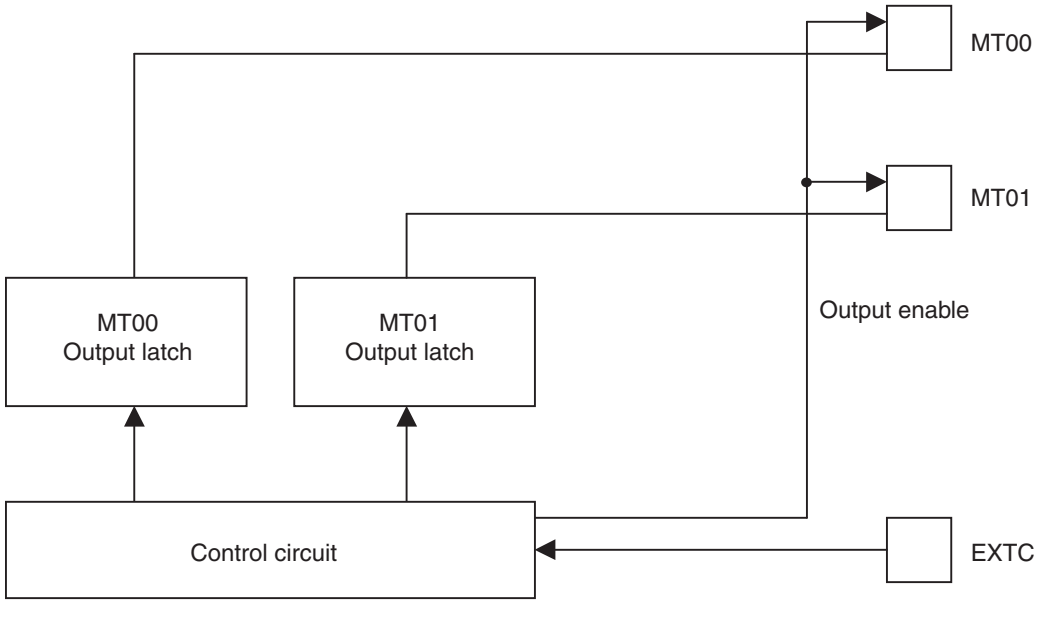
μPG control status register (PGCSR)

Initial value: 00000---B

00008EH

7	6	5	4	3	2	1	0
PEN0	PE1	PE0	PMT1	PMT0	—	—	—
R/W	R/W	R/W	R/W	R/W	—	—	—

(2) Block Diagram



12. PWC Timer (MB90485B series only)

The PWC timer is a 16-bit multifunction up-count timer capable of measuring the pulse width of the input signal. A total of three channels are provided, each consisting of a 16-bit up-count timer, an input pulse divider & divide ratio control register, a measurement input pin, and a 16-bit control register. These components provide the following functions.

Timer function :
- Capable of generating an interrupt request at fixed intervals specified.
- The internal clock used as the reference clock can be selected from among three types.

Pulse width measurement function :
- Measures the time between arbitrary events based on external pulse inputs.
- The internal clock used as the reference clock can be selected from among three types.
- Measurement modes
  - "H" pulse width (↑ to ↓) /"L" pulse width (↑ to ↓)
  - Rising cycle (↑ to ↑) /Falling cycle (↓ to ↓)
  - Measurement between edges (↑ or ↓ to ↓ or ↑)
- The 8-bit input divider can be used for division measurement by dividing the input pulse by 22 × n (n = 1, 2, 3, 4) .
- An interrupt can be generated upon completion of measurement.
- One-time measurement or fast measurement can be selected.

(1) Register list

PWC control/status registers (PWCSR0 to PWCSR2)

Initial value
0000000X$_B$

000077$_H$
00007B$_H$
00007F$_H$

15	14	13	12	11	10	9	8
STRT	STOP	EDIR	EDIE	OVIR	OVIE	ERR	Reserved
R/W	R/W	R	R/W	R/W	R/W	R	—

PWC control/status registers (PWCSR0 to PWCSR2)

Initial value
00000000$_B$

000076$_H$
00007A$_H$
00007E$_H$

7	6	5	4	3	2	1	0
CKS1	CKS0	PIS1	PIS0	S/C	MOD2	MOD1	MOD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PWC data buffer registers (PWCR0 to PWCR2)

Initial value
00000000$_B$

000079$_H$
00007D$_H$
000081$_H$

15	14	13	12	11	10	9	8
D15	D14	D13	D12	D11	D10	D9	D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PWC data buffer registers (PWCR0 to PWCR2)

Initial value
00000000$_B$

000078$_H$
00007C$_H$
000080$_H$

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

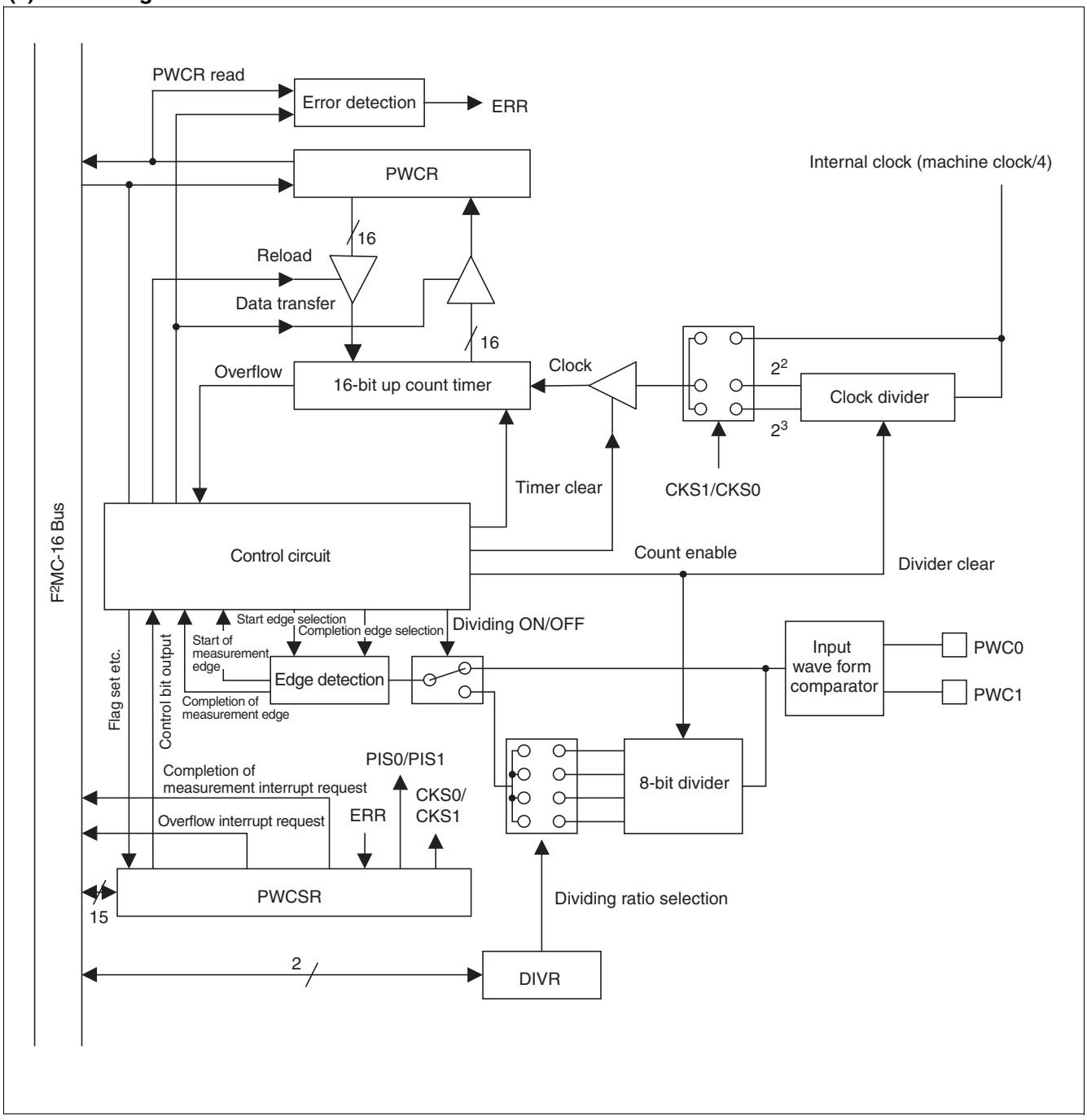
Dividing ratio control registers (DIVR0 to DIVR2)

Initial value
------00$_B$

000082$_H$
000084$_H$
000086$_H$

7	6	5	4	3	2	1	0
–	–	–	–	–	–	DIV1	DIV0
–	–	–	–	–	–	R/W	R/W

(2) Block Diagram



13. Watch Timer

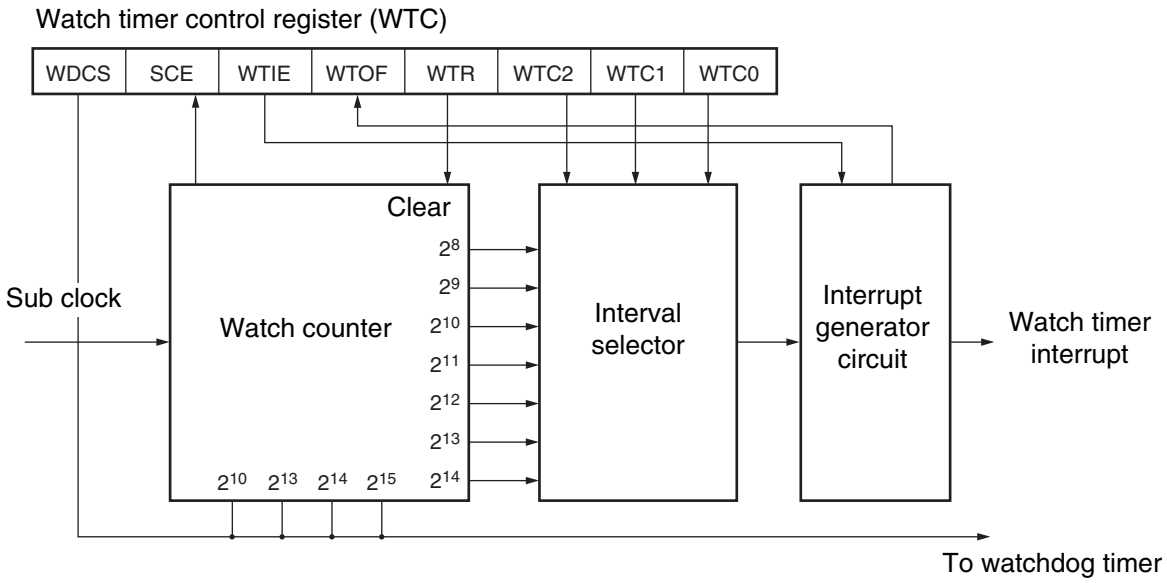
The watch timer is a 15-bit timer using the sub clock. This circuit can generate interrupts at predetermined intervals. Also a setting is available to enable it to be used as the clock source for the watchdog timer.

(1) Register List

Watch timer control register (WTC)

	7	6	5	4	3	2	1	0	
0000AA$_H$	WDCS	SCE	WTIE	WTOF	WTR	WTC2	WTC1	WTC0	
	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	Read/write
	1	0	0	0	1	0	0	0	Initial value

(2) Block Diagram



14. Watchdog timer

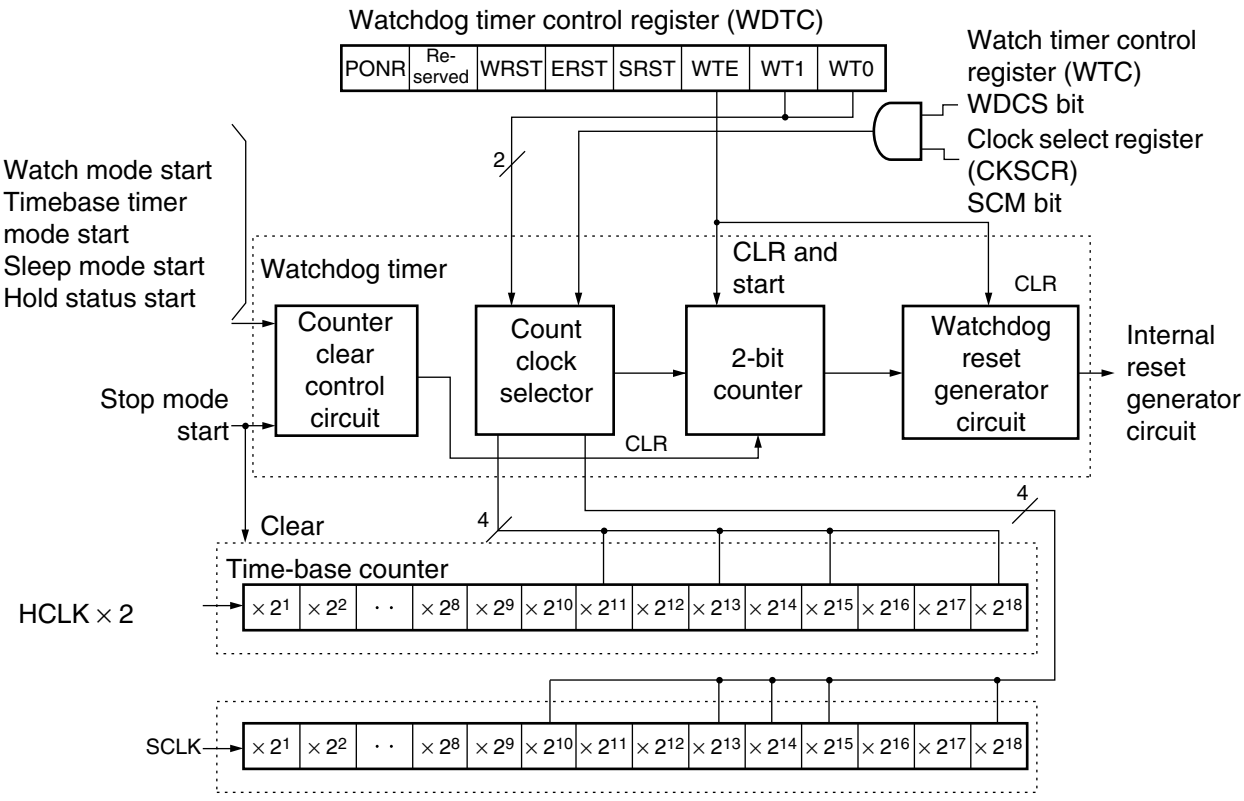
The watchdog timer is a 2-bit counter that uses the output from the timebase timer or watch timer as a count clock signal, and will reset the CPU if not cleared within a predetermined time interval after it is activated.

(1) Register List

Watchdog timer control register (WDTC)

	7	6	5	4	3	2	1	0	
0000A8H	PONR	Reserved	WRST	ERST	SRST	WTE	WT1	WT0	
	R	—	R	R	R	W	W	W	Read/write
	X	X	X	X	X	1	1	1	Initial value

(2) Block Diagram



HCLK : Oscillator clock
SCLK : Sub clock

15. Timebase Timer

The timebase timer is an 18-bit free run counter (timebase counter) that counts up in synchronization with the internal count clock signal (base oscillator × 2) , and functions as an interval timer with a choice of four types of time intervals. Other functions provided by this module include timer output for the oscillator stabilization wait period, and operating clock signal feed for other timer circuits such as the watchdog timer.

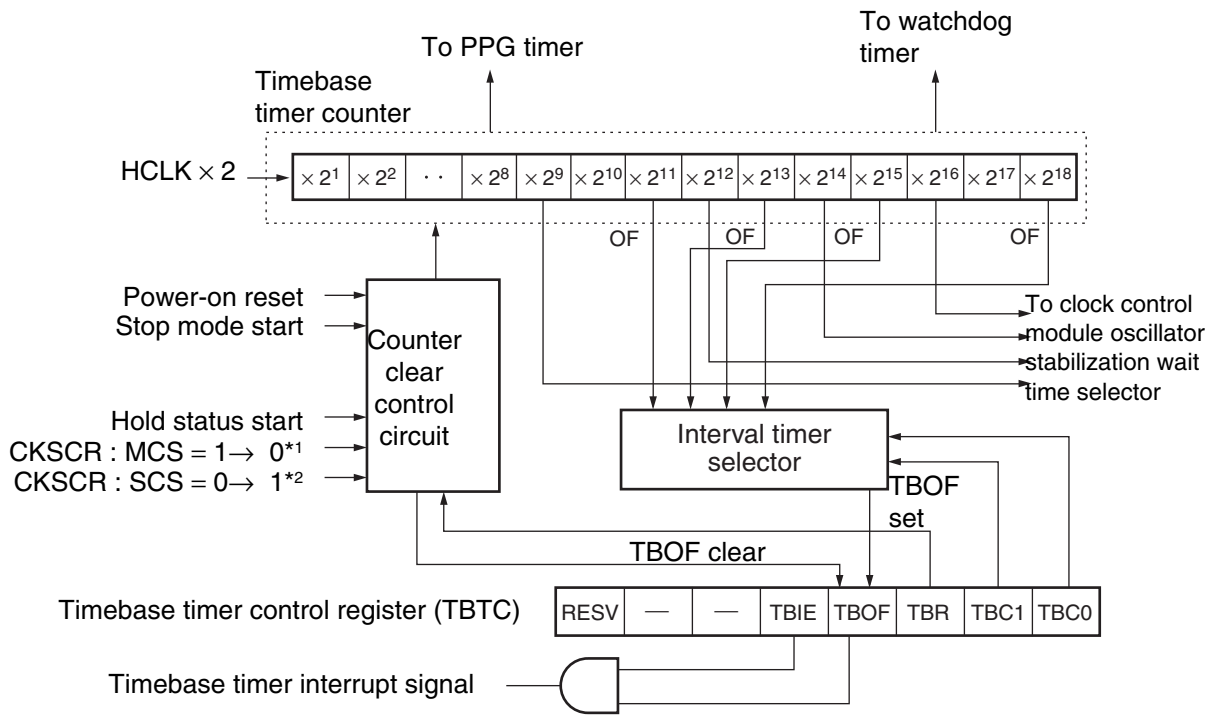
(1) Register List

Timebase timer control register (TBTC)

0000A9H

15	14	13	12	11	10	9	8	
RESV	—	—	TBIE	TBOF	TBR	TBC1	TBC0	
R/W	—	—	R/W	R/W	W	R/W	R/W	Read/write
1	X	X	0	0	1	0	0	Initial value

(2) Block Diagram



OF : Overflow
HCLK : Oscillator clock
*1 : Switch machine clock from main clock or sub clock to PLL clock.
*2 : Switch machine clock from sub clock to main clock.

16. Clock

The clock generator module controls the operation of the internal clock circuits that serve as the operating clock for the CPU and peripheral devices. This internal clock is referred to as the machine clock, and one cycle is referred to as a machine cycle. Also, the clock signals from the base oscillator are called the oscillator clock, and those from the PLL oscillator are called the PLL clock.

(1) Register List

Clock select register (CKSCR)

0000A1H

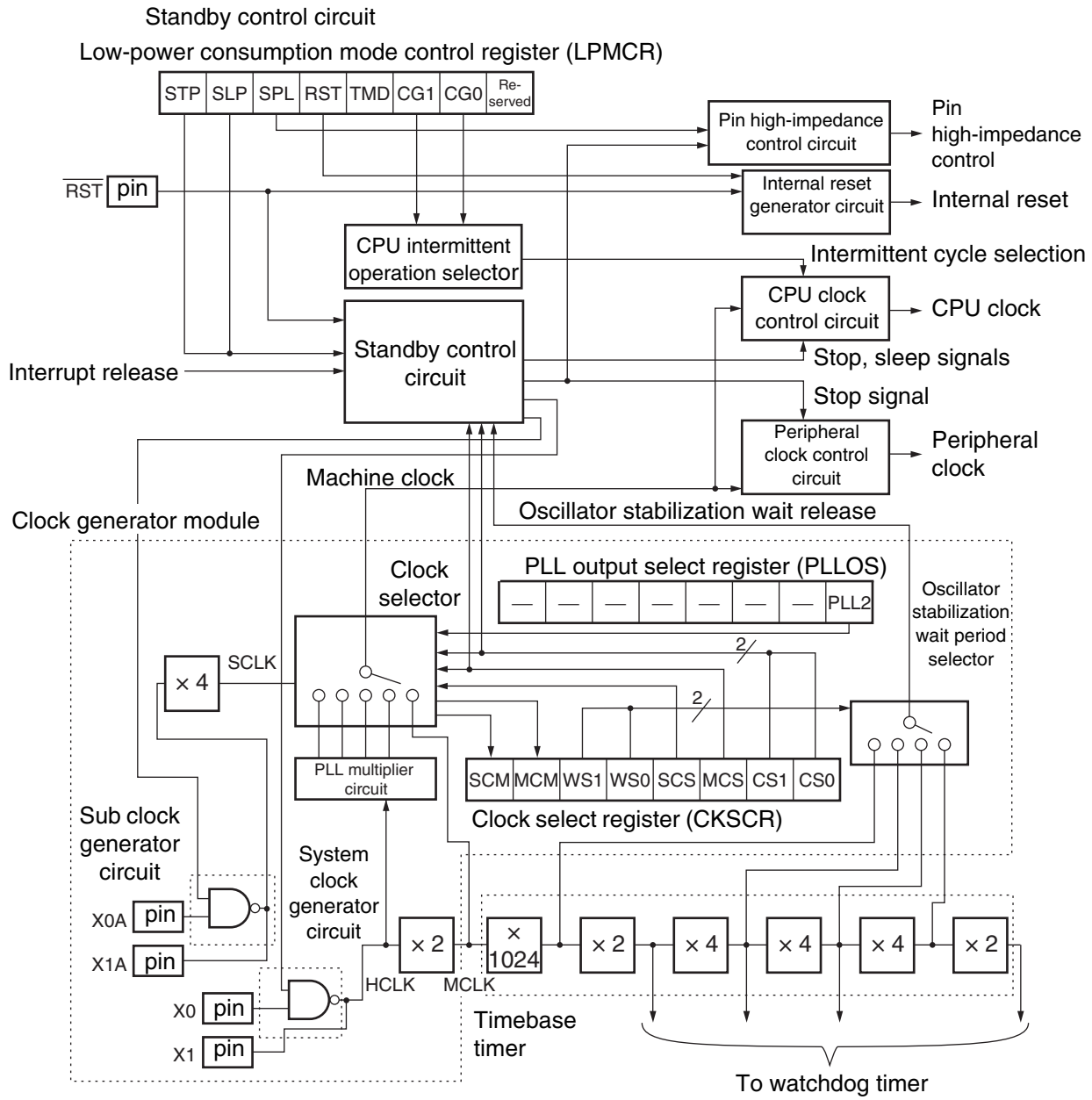
15	14	13	12	11	10	9	8	
SCM	MCM	WS1	WS0	SCS	MCS	CS1	CS0	
R	R	R/W	R/W	R/W	R/W	R/W	R/W	Read/write
1	1	1	1	1	1	0	0	Initial value

PLL output select register (PLLOS)

0000CFH

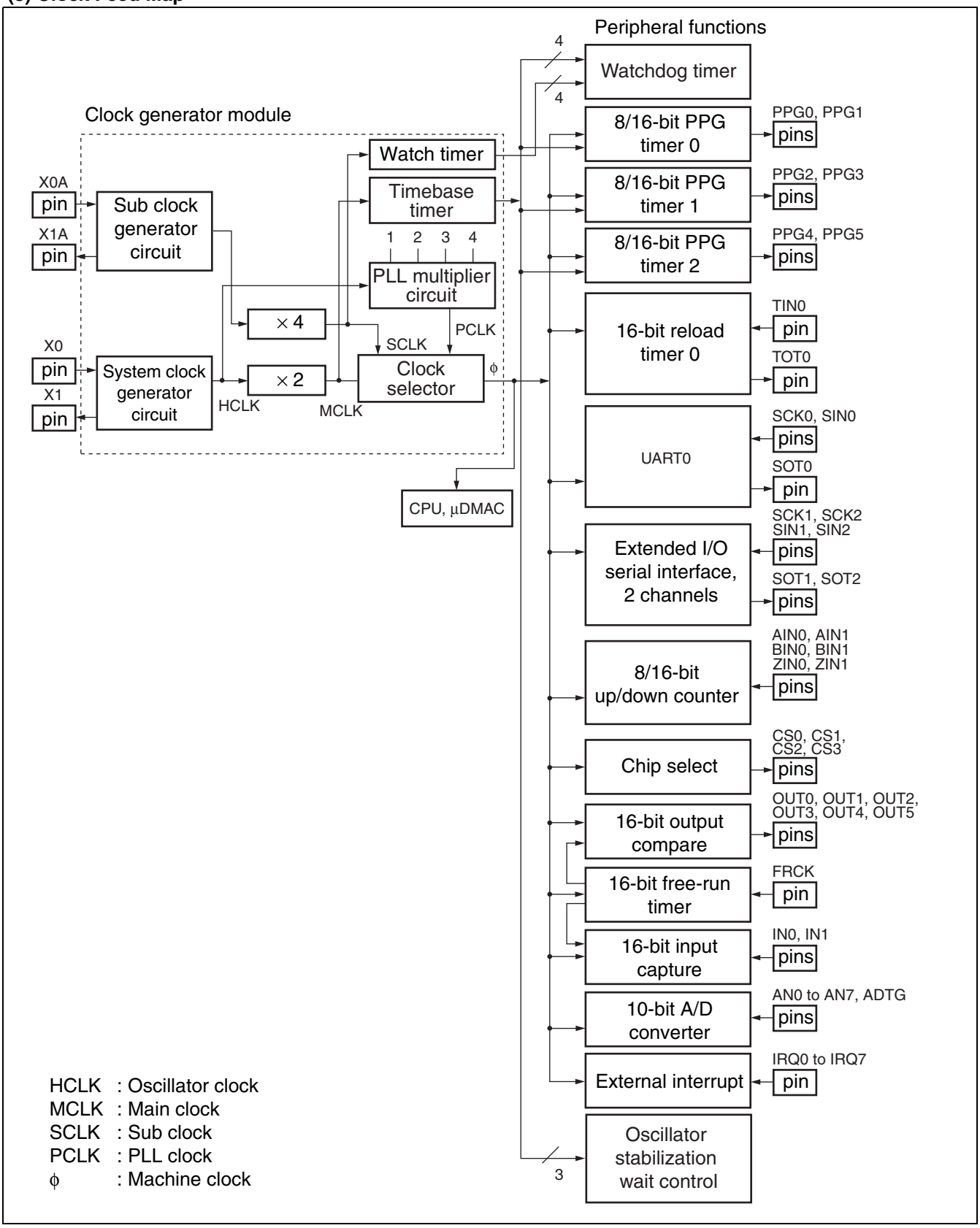
15	14	13	12	11	10	9	8	
—	—	—	—	—	—	—	PLL2	
—	—	—	—	—	—	W	W	Read/write
—	—	—	—	—	—	X	0	Initial value

(2) Block Diagram



HCLK : Oscillator clock
MCLK : Main clock
SCLK : Sub clock

(3) Clock Feed Map



17. Low-power Consumption Mode

The MB90480B/485B series uses operating clock selection and clock operation controls to provide the following CPU operating modes :

- Clock modes
  (PLL clock mode, main clock mode, sub clock mode)
- CPU intermittent operating modes
  (PLL clock intermittent mode, main clock intermittent mode, sub clock intermittent mode)
- Standby modes
  (Sleep mode, timebase timer mode, stop mode, watch mode)

(1) Register List

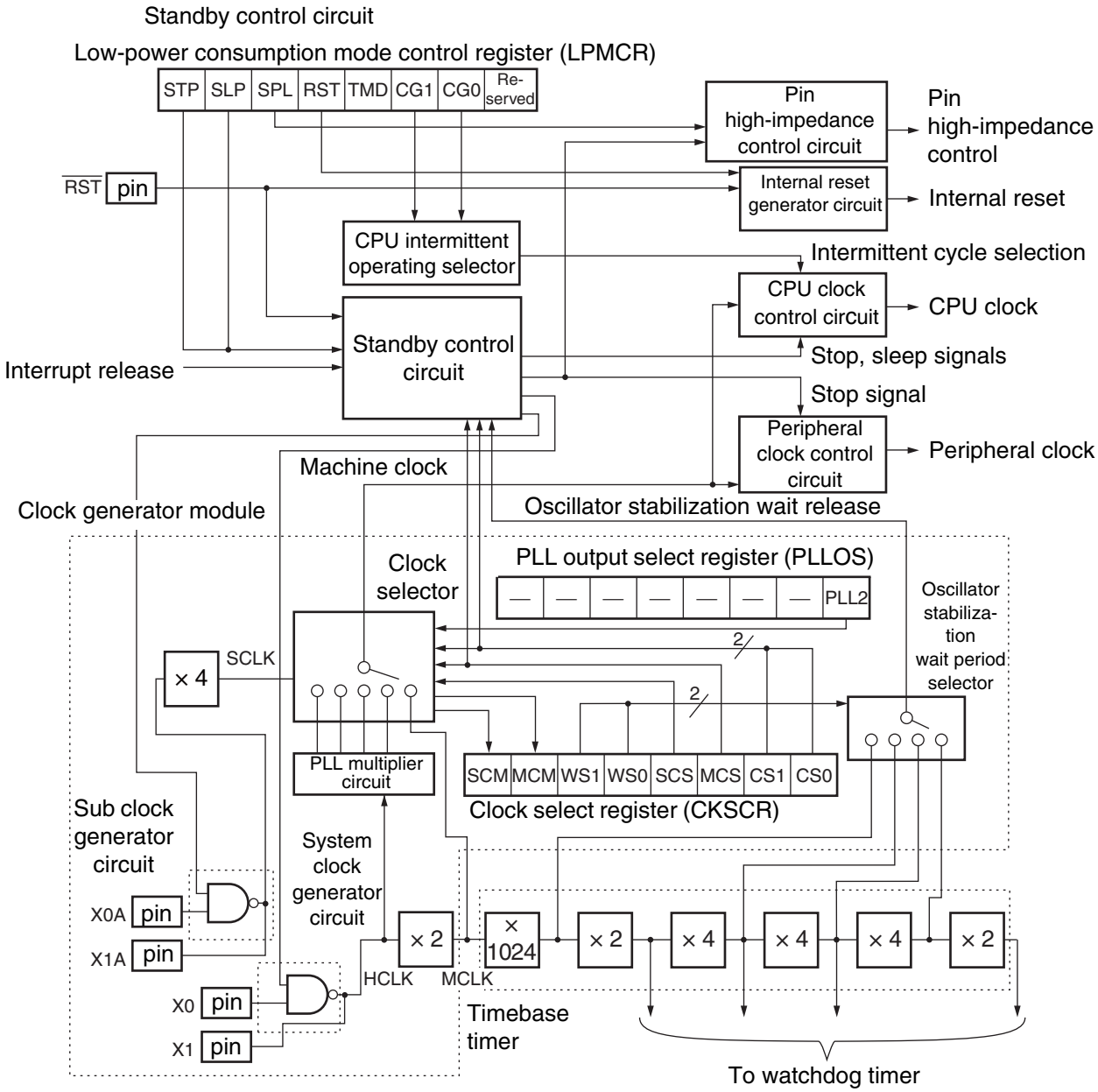
Low-power consumption mode control register (LPMCR)

0000A0H

7	6	5	4	3	2	1	0
STP	SLP	SPL	RST	TMD	CG1	CG0	Reserved
W	W	R/W	W	R/W	R/W	R/W	R/W
0	0	0	1	1	0	0	0

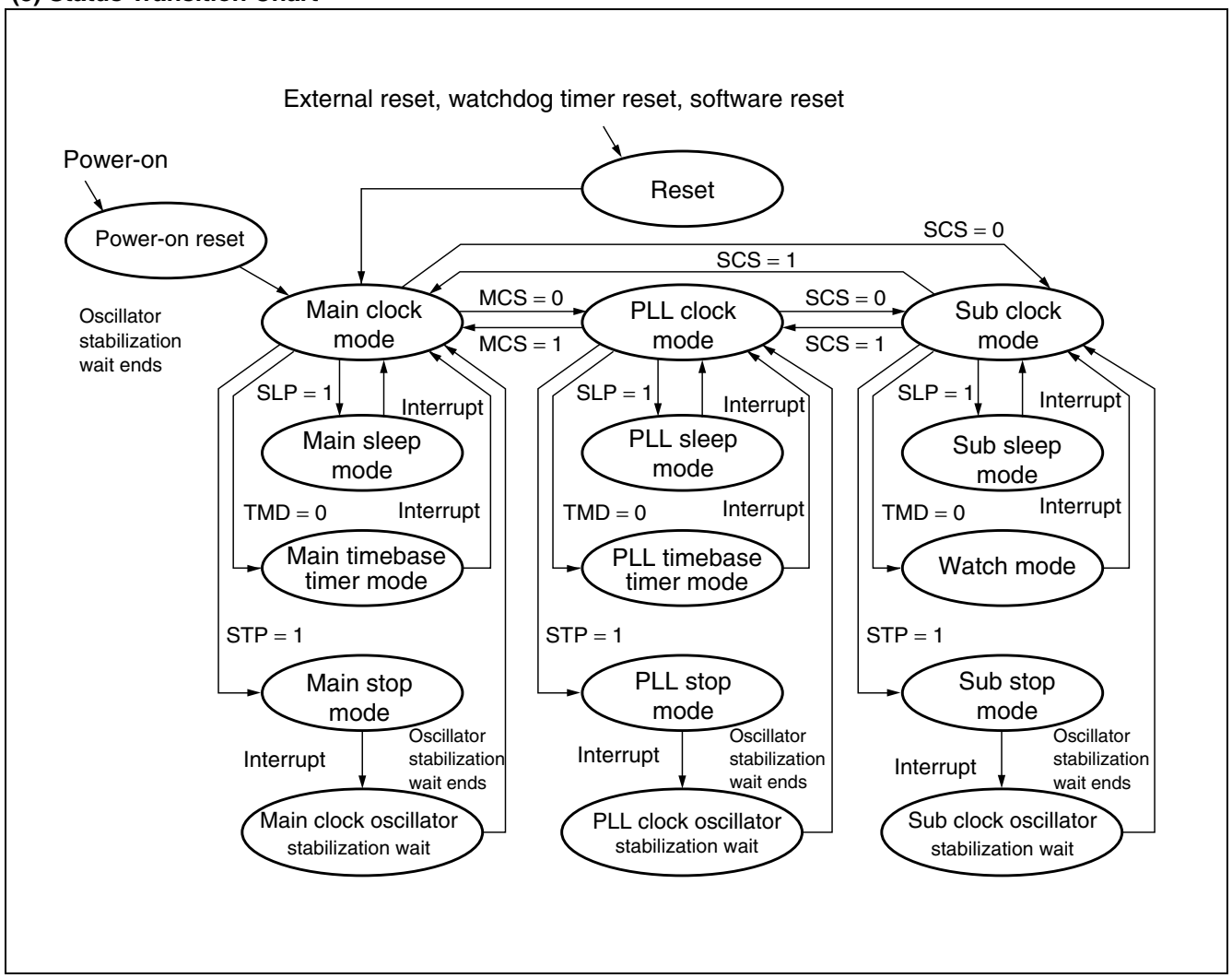
Read/write
Initial value

(2) Block Diagram



HCLK : Oscillator clock
MCLK : Main clock
SCLK : Sub clock

(3) Status Transition Chart



18. External Bus Pin Control Circuit

The external bus pin control circuit controls the external bus pins used to expand the CPU address/data bus connections to external circuits.

(1) Register List

- Auto ready function select register (ARSR)

Address : 0000A5H

15	14	13	12	11	10	9	8
IOR1	IOR0	HMR1	HMR0	—	—	LMR1	LMR0
W	W	W	W	—	—	W	W

Initial value 0011--00B

- External address output control register (HACR)

Address : 0000A6H

7	6	5	4	3	2	1	0
E23	E22	E21	E20	E19	E18	E17	E16
W	W	W	W	W	W	W	W

Initial value ********B

- Bus control signal select register (EPCR)

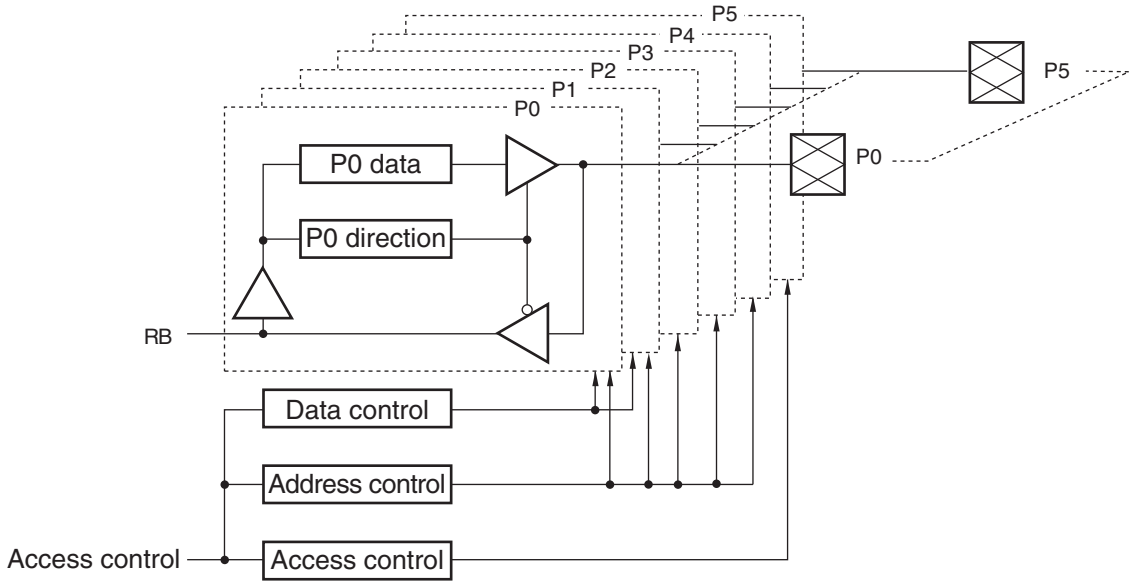
Address : 0000A7H

15	14	13	12	11	10	9	8
CKE	RYE	HDE	IOBS	HMBS	WRE	LMBS	—
W	W	W	W	W	W	W	—

Initial value 1000*10-B

W : Write only
– : Not used
* : May be either “1” or “0”

(2) Block Diagram



19. Chip Select Function Description

The chip select module generates a chip select signals, which are used to facilitate connections to external memory devices. The MB90480B/485B series has four chip select output pins, each having a chip select area register setting that specifies the corresponding hardware area and select signal that is output when access to the corresponding external address is detected.

- Chip select function features

The chip select function uses two 8-bit registers for each output pin. One of these registers (CARx) is able to detect memory areas in 64 Kbytes units by specifying the upper 8-bit of the address for match detection. The other register (CMRx) can be used to expand the detection area beyond 64 Kbytes by masking bits for match detection.
Note that during external bus holds, the CS output is set to high impedance.

(1) Register List

15 8	7 0	
CAR0	CMR0	R/W
CAR1	CMR1	R/W
CAR2	CMR2	R/W
CAR3	CMR3	R/W
CALR	CSCR	R/W

Chip select area mask registers (CMRx)

	7	6	5	4	3	2	1	0	
0000C0H 0000C2H 0000C4H 0000C6H	M7	M6	M5	M4	M3	M2	M1	M0	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Read/write
	0	0	0	0	1	1	1	1	Initial value

Chip select area registers (CARx)

	15	14	13	12	11	10	9	8	
0000C1H 0000C3H 0000C5H 0000C7H	A7	A6	A5	A4	A3	A2	A1	A0	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Read/write
	1	1	1	1	1	1	1	1	Initial value

Chip select control register (CSCR)

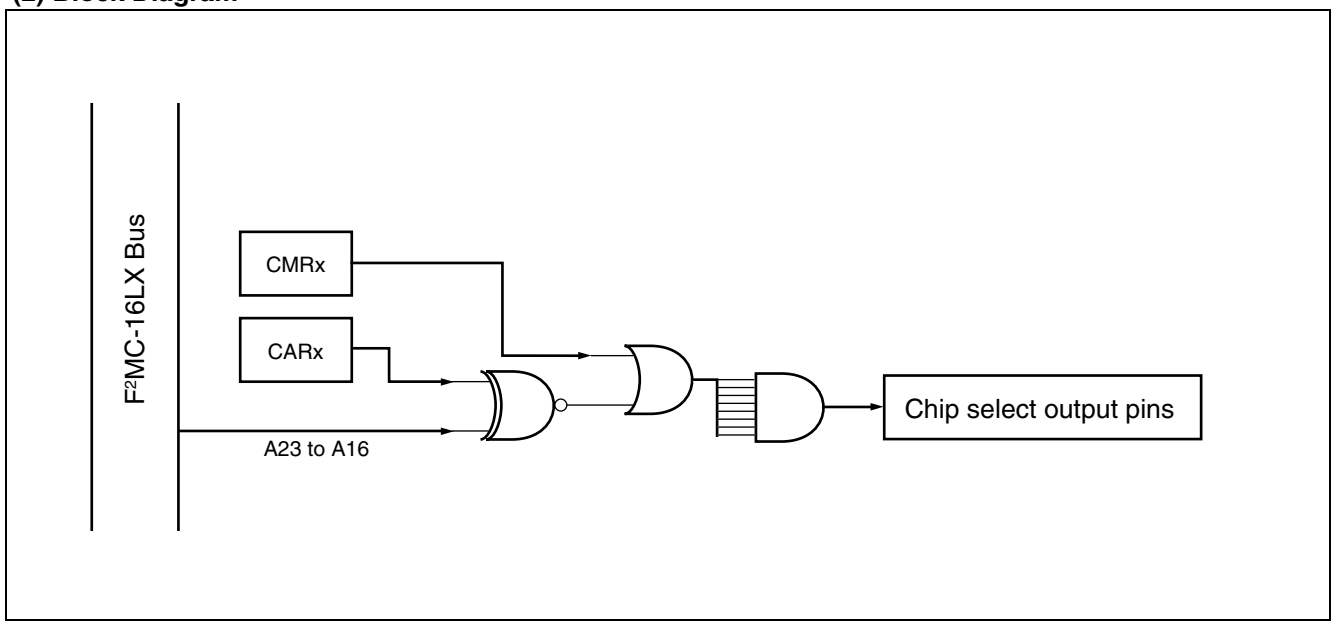
	7	6	5	4	3	2	1	0	
0000C8H	—	—	—	—	OPL3	OPL2	OPL1	OPL0	
	—	—	—	—	R/W	R/W	R/W	R/W	Read/write
	—	—	—	—	0	0	0	*	Initial value

Chip select active level register (CALR)

	15	14	13	12	11	10	9	8	
0000C9H	—	—	—	—	ACTL3	ACTL2	ACTL1	ACTL0	
	—	—	—	—	R/W	R/W	R/W	R/W	Read/write
	—	—	—	—	0	0	0	0	Initial value

* : The initial value of this bit is “1” or “0”.
The value depends on the mode pin (MD2, MD1 and MD0) .

(2) Block Diagram



20. ROM Mirror Function Select Module

The ROM mirror function selection module sets the data in ROM assigned to FF bank so that the data is read by access to 00 bank.

(1) Register List

• ROM mirror function select register (ROMM)

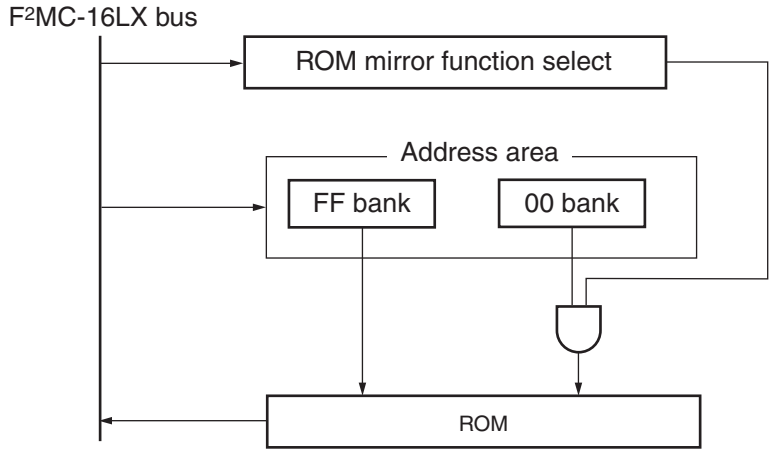
Address : 00006F$_H$

15	14	13	12	11	10	9	8
—	—	—	—	—	—	MS	MI
						R/W (+)	R/W

Initial value
------+1$_B$
(+) : MB90F489B : Read only, fixed at “1”
Other : Selectable, Initial value 0

- : Not used

(2) Block Diagram



Note : Do not access ROM mirror function selection register (ROMM) on using the area of address 004000$_H$ to 00FFFF$_H$ (008000$_H$ to 00FFFF$_H$) .

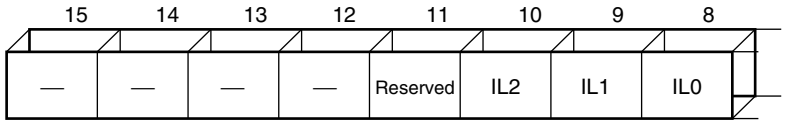
21. Interrupt Controller

The interrupt control register is built in interrupt controller, and is supported for all I/O of interrupt function. This register sets corresponding peripheral interrupt level.

(1) Register List

Interrupt control registers

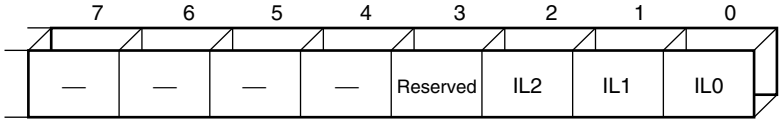
Address : ICR01 0000B1H
ICR03 0000B3H
ICR05 0000B5H
ICR07 0000B7H
ICR09 0000B9H
ICR11 0000BBH
ICR13 0000BDH
ICR15 0000BFH



	15	14	13	12	11	10	9	8
Read/write→	W	W	W	W	R/W	R/W	R/W	R/W
Initial value→	X	X	X	X	0	1	1	1

Interrupt control registers

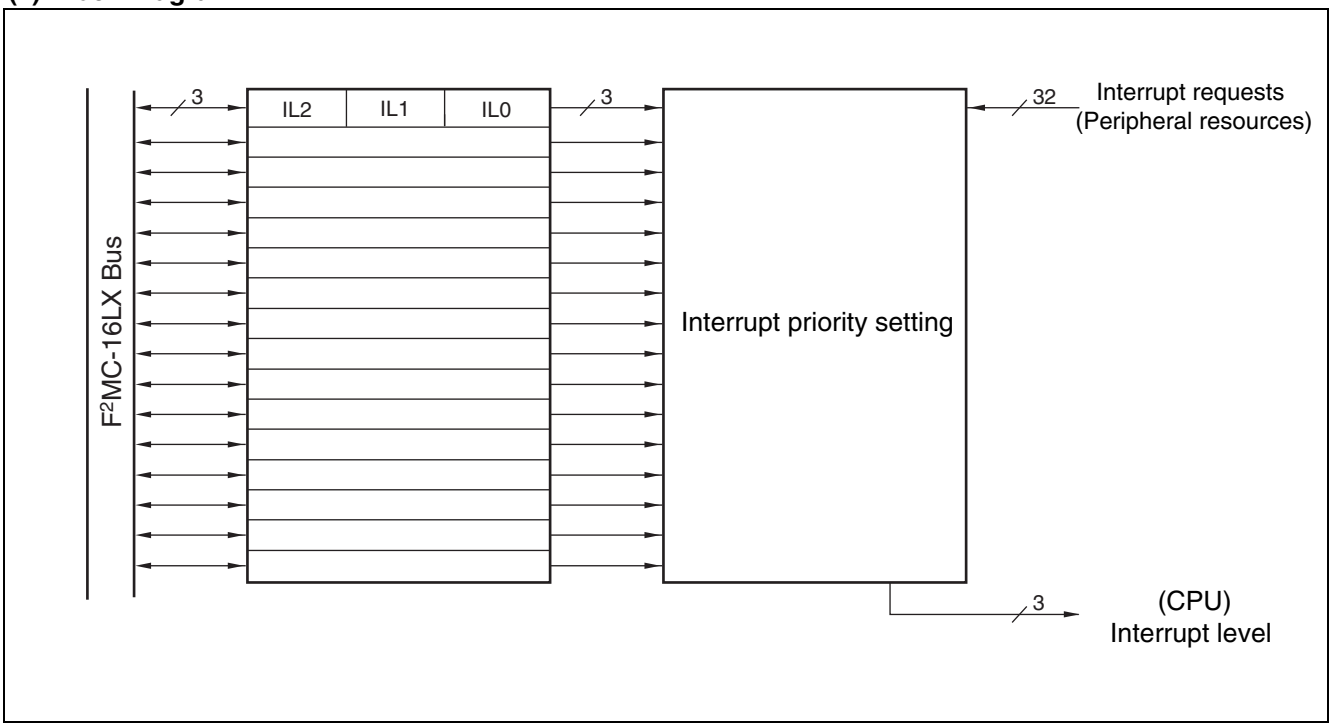
Address : ICR00 0000B0H
ICR02 0000B2H
ICR04 0000B4H
ICR06 0000B6H
ICR08 0000B8H
ICR10 0000BAH
ICR12 0000BCH
ICR14 0000BEH



	7	6	5	4	3	2	1	0
Read/write→	W	W	W	W	R/W	R/W	R/W	R/W
Initial value→	X	X	X	X	0	1	1	1

Note : The use of access involving read-modify-write instructions may lead to abnormal operation, and should be avoided.

(2) Block Diagram



22. µDMAC

The µDMAC is a simplified DMA module with functions equivalent to EI²OS. The µDMAC has 16 DMA data transfer channels, and provides the following functions.

- Automatic data transfer between peripheral resources (I/O) and memory.
- CPU program execution stops during DMA operation.
- Incremental addressing for transfer source and destination can be turned on/off.
- DMA transfer control from the µDMAC enable register, µDMAC stop status register, µDMAC status register, and descriptor.
- Stop requests from resources can stop DMA transfer.
- When DMA transfer is completed, the µDMAC status register sets a flag in the bit for the corresponding channel on which transfer was completed, and outputs a completion interrupt to the interrupt controller.

(1) Register List

µDMAC enable register

DERH : 0000AD$_H$

15	14	13	12	11	10	9	8
EN15	EN14	EN13	EN12	EN11	EN10	EN9	EN8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value 00000000$_B$

µDMAC enable register

DERL : 0000AC$_H$

7	6	5	4	3	2	1	0
EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value 00000000$_B$

µDMAC stop status register

DSSR : 0000A4$_H$

7	6	5	4	3	2	1	0
STP7	STP6	STP5	STP4	STP3	STP2	STP1	STP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value 00000000$_B$

µDMAC status register

DSRH : 00009D$_H$

15	14	13	12	11	10	9	8
DE15	DE14	DE13	DE12	DE11	DE10	DE9	DE8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value 00000000$_B$

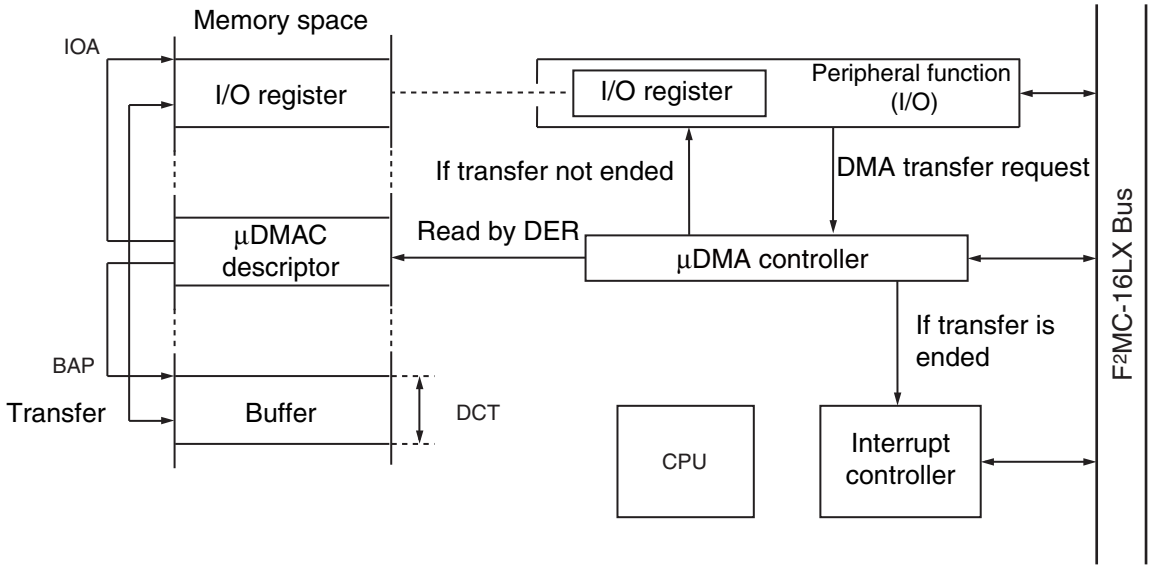
µDMAC status register

DSRL : 00009C$_H$

7	6	5	4	3	2	1	0
DE7	DE6	DE5	DE4	DE3	DE2	DE1	DE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value 00000000$_B$

(2) Block Diagram



IOA : I/O address pointer
BAP : Buffer address pointer
DER : μDMAC enable register (ENx selection)
DCT : Data counter

23. Address Match Detection Function

When the address is equal to a value set in the address detection register, the instruction code loaded into the CPU is replaced forcibly with the INT9 instruction code (01H). As a result, when the CPU executes a set instruction, the INT9 instruction is executed. Processing by the INT#9 interrupt routine allows the program patching function to be implemented.

Two address detection registers are supported. An interrupt enable bit is prepared for each register. If the value set in the address detection register matches an address and if the interrupt enable bit is set at "1", the instruction code loaded into the CPU is replaced forcibly with the INT9 instruction code.

(1) Register List

- Program address detection register 0 (PADR0)

Address	7	6	5	4	3	2	1	0	Initial value
PADR0 (Low order address) : 001FF0H									XXXXXXXXB
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Address	7	6	5	4	3	2	1	0	Initial value
PADR0 (Middle order address) : 001FF1H									XXXXXXXXB
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Address	7	6	5	4	3	2	1	0	Initial value
PADR0 (High order address) : 001FF2H									XXXXXXXXB
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Program address detection register 1 (PADR1)

Address	7	6	5	4	3	2	1	0	Initial value
PADR1 (Low order address) : 001FF3H									XXXXXXXXB
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Address	7	6	5	4	3	2	1	0	Initial value
PADR1 (Middle order address) : 001FF4H									XXXXXXXXB
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

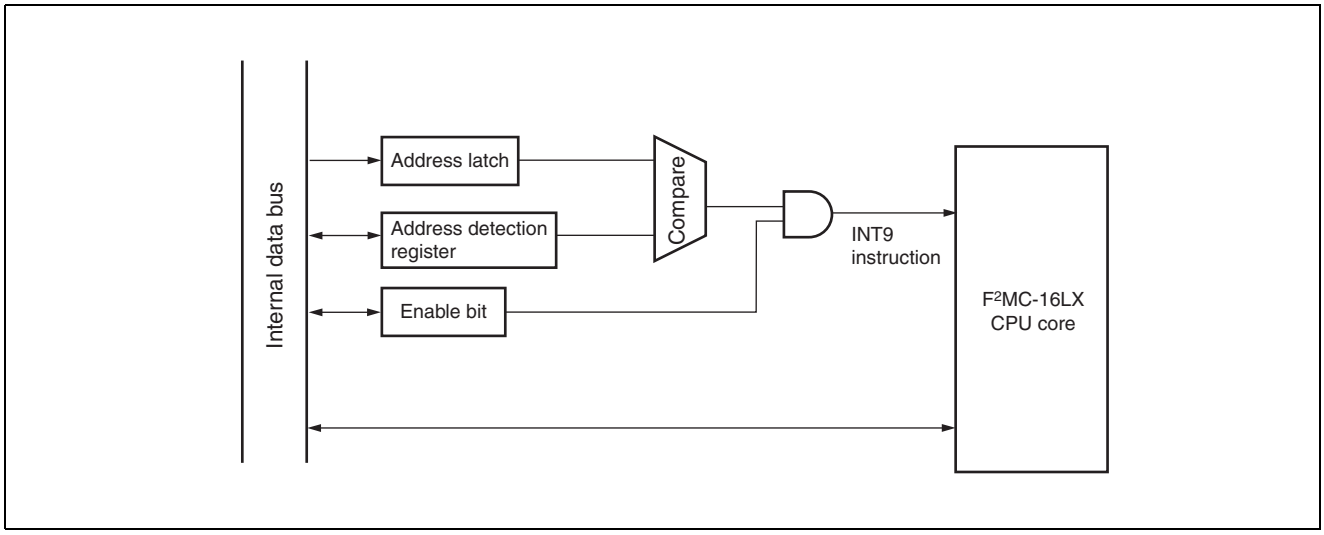
Address	7	6	5	4	3	2	1	0	Initial value
PADR1 (High order address) : 001FF5H									XXXXXXXXB
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Program address detection control status register (PACSR)

Address	7	6	5	4	3	2	1	0	Initial value
00009EH	RESV	RESV	RESV	RESV	AD1E	RESV	AD0E	RESV	00000000B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

R/W : Readable and writable
X : Undefined
RESV : Reserved bit

(2) Block Diagram



■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	$V_{CC}3$	V_{SS} – 0.3	V_{SS} + 4.0	V	
	$V_{CC}5$	V_{SS} – 0.3	V_{SS} + 7.0	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 4.0	V	*2
	AVRH	V_{SS} – 0.3	V_{SS} + 4.0	V	*2
Input voltage*1	V_I	V_{SS} – 0.3	V_{SS} + 4.0	V	*3
		V_{SS} – 0.3	V_{SS} + 7.0	V	*3, *8, *9
Output voltage*1	V_O	V_{SS} – 0.3	V_{SS} + 4.0	V	*3
		V_{SS} – 0.3	V_{SS} + 7.0	V	*3, *8, *9
Maximum clamp current	I_{CLAMP}	– 2.0	+ 2.0	mA	*7
Total maximum clamp current	$\Sigma \lvert I_{CLAMP} \rvert$	—	20	mA	*7
“L” level maximum output current	I_{OL}	—	10	mA	*4
“L” level average output current	I_{OLAV}	—	3	mA	*5
“L” level maximum total output current	ΣI_{OL}	—	60	mA	
“L” level total average output current	ΣI_{OLAV}	—	30	mA	*6
“H” level maximum output current	I_{OH}	—	–10	mA	*4
“H” level average output current	I_{OHAV}	—	–3	mA	*5
“H” level maximum total output current	ΣI_{OH}	—	–60	mA	
“H” level total average output current	ΣI_{OHAV}	—	–30	mA	*6
Power consumption	P_D	—	320	mW	
Operating temperature	T_A	– 40	+ 85	°C	
Storage temperature	Tstg	– 55	+ 150	°C	

*1 : This parameter is based on $V_{SS} = AV_{SS} = 0.0$ V.

*2 : AV_{CC} and AVRH must not exceed V_{CC}. Also, AVRH must not exceed AV_{CC}.

*3 : V_I and V_0 must not exceed V_{CC} + 0.3 V. However, if the maximum current to/from and input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

*4 : Maximum output current is defined as the peak value for one of the corresponding pins.

*5 : Average output current is defined as the average current flow in a 100 ms interval at one of the corresponding pins.

*6 : Average total output current is defined as the average current flow in a 100 ms interval at all corresponding pins.

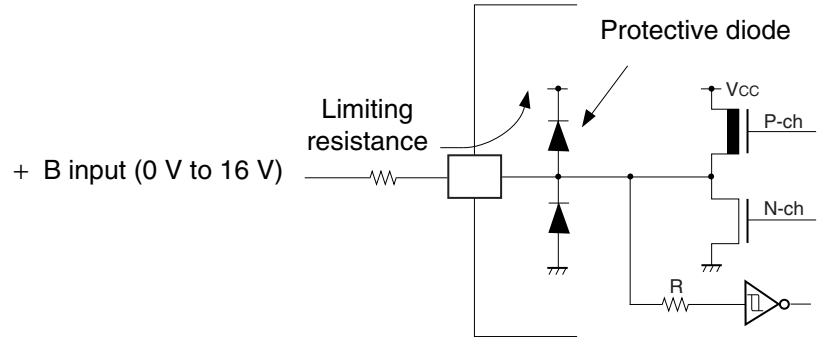
*7 : • Applicable to pins : P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0 to PA3
• Use within recommended operating conditions.
• Use at DC voltage (current) .
• The + B signal should always be applied with a limiting resistance placed between the + B signal and the microcontroller.
• The value of the limiting resistance should be set so that when the + B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.

(Continued)

(Continued)

- Note that when the microcontroller drive current is low, such as in the power saving modes, the + B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a + B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the + B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the + B input pin open.
- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept + B signal input.
- Sample recommended circuits:

• Input/Output Equivalent circuits



*8 : MB90485B series only
P20 to P27, P30 to P37, P40 to P47, P70 to P77 pins can be used as 5 V I/F pin on applied 5 V to $V_{CC}5$ pin.
P76 and P77 is N-ch open drain pin.

*9 : As for P76 and P77 (N-ch open drain pin) , even if using at 3 V simplicity ($V_{CC}3 = V_{CC}5$) , the ratings are applied.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	$V_{CC}3$	2.7	3.6	V	During normal operation
		1.8	3.6	V	To maintain RAM state in stop mode
	$V_{CC}5$	2.7	5.5	V	During normal operation*
		1.8	5.5	V	To maintain RAM state in stop mode*
"H" level input voltage	V_{IH}	0.7 V_{CC}	V_{CC} + 0.3	V	All pins other than V_{IH2}, V_{IHS}, V_{IHM} and V_{IHX}
	V_{IH2}	0.7 V_{CC}	V_{SS} + 5.8	V	MB90485B series only P76, P77 pins (N-ch open drain pins)
	V_{IHS}	0.8 V_{CC}	V_{CC} + 0.3	V	Hysteresis input pins
	V_{IHM}	V_{CC} – 0.3	V_{CC} + 0.3	V	MD pin input
	V_{IHX}	0.8 V_{CC}	V_{CC} + 0.3	V	X0A pin, X1A pin
"L" level input voltage	V_{IL}	V_{SS} – 0.3	0.3 V_{CC}	V	All pins other than V_{ILS}, V_{ILM} and V_{ILX}
	V_{ILS}	V_{SS} – 0.3	0.2 V_{CC}	V	Hysteresis input pins
	V_{ILM}	V_{SS} – 0.3	V_{SS} + 0.3	V	MD pin input
	V_{ILX}	V_{SS} – 0.3	0.1	V	X0A pin, X1A pin
Operating temperature	T_A	0	+ 70	°C	At external bus operation

* : MB90485B series only
P20 to P27, P30 to P37, P40 to P47, P70 to P77 pins can be used as 5 V I/F pin on applied 5 V to $V_{CC}5$ pin.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

3. DC Characteristics

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	V_{OH}	All output pins	V_{CC} = 2.7 V, I_{OH} = − 1.6 mA	$V_{CC}3$ – 0.3	—	—	V	
			V_{CC} = 4.5 V, I_{OH} = − 4.0 mA	$V_{CC}5$ – 0.5	—	—	V	At using 5 V power supply
"L" level output voltage	V_{OL}	All output pins	V_{CC} = 2.7 V, I_{OL} = 2.0 mA	—	—	0.4	V	
			V_{CC} = 4.5 V, I_{OH} = 4.0 mA	—	—	0.4	V	At using 5 V power supply
Input leakage current	I_{IL}	All input pins	V_{CC} = 3.3 V, $V_{SS} < V_I < V_{CC}$	−10	—	+10	µA	
Pull-up resistance	R_{PULL}	—	V_{CC} = 3.0 V, at T_A = + 25 °C	20	53	200	kΩ	
Open drain output current	I_{leak}	P40 to P47, P70 to P77	—	—	0.1	10	µA	
Power supply current	I_{CC}	—	At V_{CC} = 3.3 V, internal 25 MHz operation, normal operation	—	45	60	mA	
			At V_{CC} = 3.3 V, internal 25 MHz operation, Flash programming	—	55	70	mA	
	I_{CCS}	—	At V_{CC} = 3.3 V, internal 25 MHz operation, sleep mode	—	17	35	mA	
	I_{CCL}	—	At V_{CC} = 3.3 V, external 32 kHz, internal 8 kHz operation, sub clock operation (T_A = + 25 °C)	—	15	140	µA	
	I_{CCT}	—	At V_{CC} = 3.3 V, external 32 kHz, internal 8 kHz operation, watch mode (T_A = + 25 °C)	—	1.8	40	µA	
	I_{CCH}	—	T_A = + 25 °C, stop mode, At V_{CC} = 3.3 V	—	0.8	40	µA	
Input capacitance	C_{IN}	Other than AV_{CC}, AV_{SS}, V_{CC}, V_{SS}	—	—	5	15	pF	

Notes : • MB90485B series only

- P40 to P47 and P70 to P77 are N-ch open drain pins with control, which are usually used as CMOS.
- P76 and P77 are open drain pins without P-ch.
- For use as a single 3 V power supply products, set $V_{CC} = V_{CC}3 = V_{CC}5$.
- When the device is used with dual power supplies, P20 to P27, P30 to P37, P40 to P47 and P70 to P77 serve as 5 V pins while the other pins serve as 3 V I/O pins.

4. AC Characteristics

(1) Clock Timing

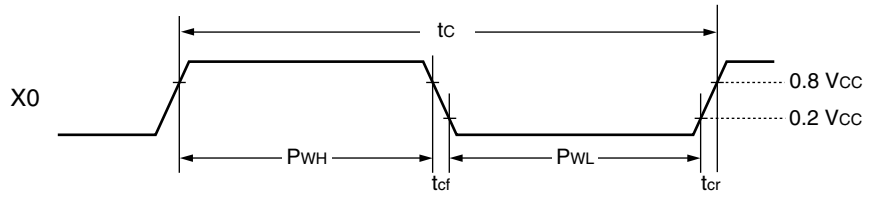
(V_{SS} = 0.0 V, T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_{CH}	X0, X1	—	3	—	25	MHz	External crystal oscillator
			—	3	—	50		External clock input
			—	4	—	25		1 multiplied PLL
			—	3	—	12.5		2 multiplied PLL
			—	3	—	6.66		3 multiplied PLL
			—	3	—	6.25		4 multiplied PLL
			—	3	—	4.16		6 multiplied PLL
			—	3	—	3.12		8 multiplied PLL
	F_{CL}	X0A, X1A	—	—	32.768	—	kHz	
Clock cycle time	t_C	X0, X1	—	20	—	333	ns	*1
	t_{CL}	X0A, X1A	—	—	30.5	—	µs	
Input clock pulse width	P_{WH} P_{WL}	X0	—	5	—	—	ns	
	P_{WLH} P_{WLL}	X0A	—	—	15.2	—	µs	*2
Input clock rise, fall time	t_{cr} t_{cf}	X0	—	—	—	5	ns	With external clock
Internal operating clock frequency	f_{CP}	—	—	1.5	—	25	MHz	*1
	f_{CPL}	—	—	—	8.192	—	kHz	
Internal operating clock cycle time	t_{CP}	—	—	40.0	—	666	ns	*1
	t_{CPL}	—	—	—	122.1	—	µs	

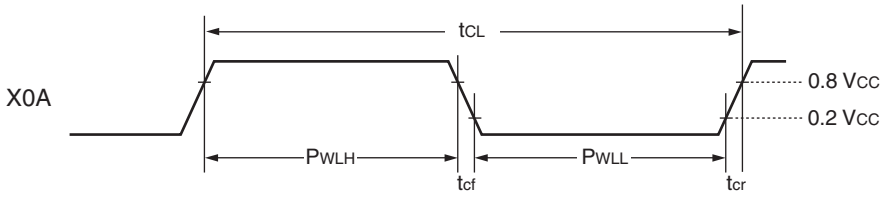
*1 : Be careful of the operating voltage.

*2 : Duty ratio should be 50 % ± 3 %.

- X0, X1 clock timing

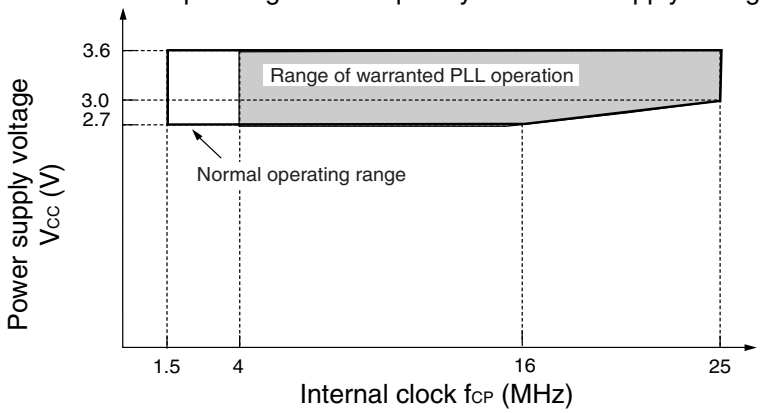


- X0A, X1A clock timing



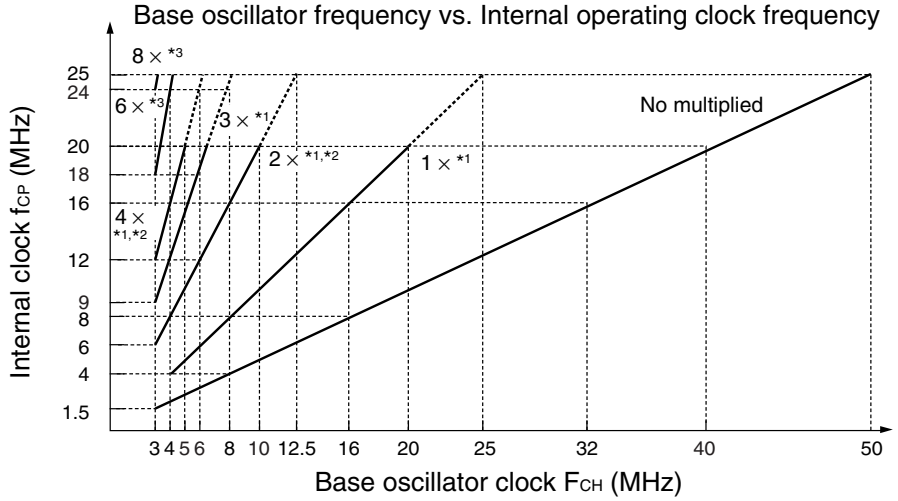
• Range of warranted PLL operation

Internal operating clock frequency vs. Power supply voltage



Notes: • For A/D operating frequency, refer to “5. A/D Converter Electrical Characteristics”
• Only at 1 multiplied PLL, use with more than f_{CP} = 4 MHz.

Base oscillator frequency vs. Internal operating clock frequency



*1 : In setting as 1, 2, 3 and 4 multiplied PLL, when the internal clock is used at 20 MHz < f_{CP} ≤ 25 MHz, set the PLLOS register to “DIV2 bit = 1” and “PLL2 bit = 1”.
[Example] When using the base oscillator frequency of 24 MHz at 1 multiplied PLL :
CKSCR register : CS1 bit = “0”, CS0 bit = “0” PLLOS register : PLL2 bit = “1”
[Example] When using the base oscillator frequency of 6 MHz at 3 multiplied PLL :
CKSCR register : CS1 bit = “1”, CS0 bit = “0” PLLOS register : PLL2 bit = “1”

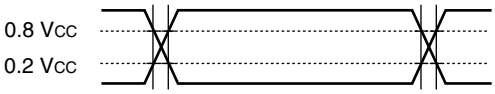
*2 : In setting as 2 and 4 multiplied PLL, when the internal clock is used at 20 MHz < f_{CP} ≤ 25 MHz, the following setting is also enabled.
2 multiplied PLL : CKSCR register : CS1 bit = “0”, CS0 bit = “0”
PLLOS register : PLL2 bit = “1”
4 multiplied PLL : CKSCR register : CS1 bit = “0”, CS0 bit = “1”
PLLOS register : PLL2 bit = “1”

*3 : When using in setting as 6 and 8 multiplied PLL, set the PLLOS register to “DIV2 bit = 0” and “PLL2 bit = 1”.
[Example] When using the base oscillator frequency of 4 MHz at 6 multiplied PLL :
CKSCR register : CS1 bit = “1”, CS0 bit = “0” PLLOS register : PLL2 bit = “1”
[Example] When using the base oscillator frequency of 3 MHz at 8 multiplied PLL :
CKSCR register : CS1 bit = “1”, CS0 bit = “1” PLLOS register : PLL2 bit = “1”

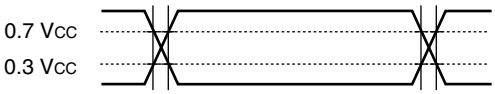
AC standards are set at the following measurement voltage values.

- Input signal wave form

Hysteresis input pins

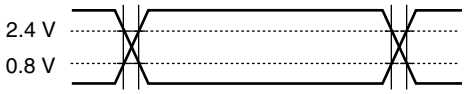


- Pins other than hysteresis input/MD input



- Output signal wave form

Output pins

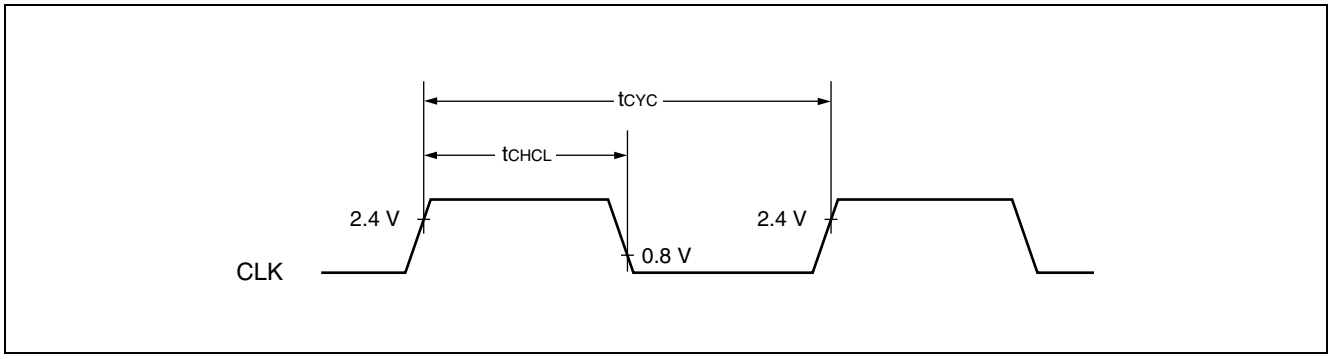


(2) Clock Output Timing

(V_{SS} = 0.0 V, T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	CLK	—	t_{CP}*	—	ns	
CLK↑→ CLK↓	t_{CHCL}	CLK	V_{CC} = 3.0 V to 3.6 V	t_{CP}* / 2 – 15	t_{CP}* / 2 + 15	ns	at f_{CP} = 25 MHz
			V_{CC} = 2.7 V to 3.3 V	t_{CP}* / 2 – 20	t_{CP}* / 2 + 20	ns	at f_{CP} = 16 MHz
			V_{CC} = 2.7 V to 3.3 V	t_{CP}* / 2 – 64	t_{CP}* / 2 + 64	ns	at f_{CP} = 5 MHz

* : t_{CP} is internal operating clock cycle time. Refer to “ (1) Clock Timing”.



(3) Reset Input Standards

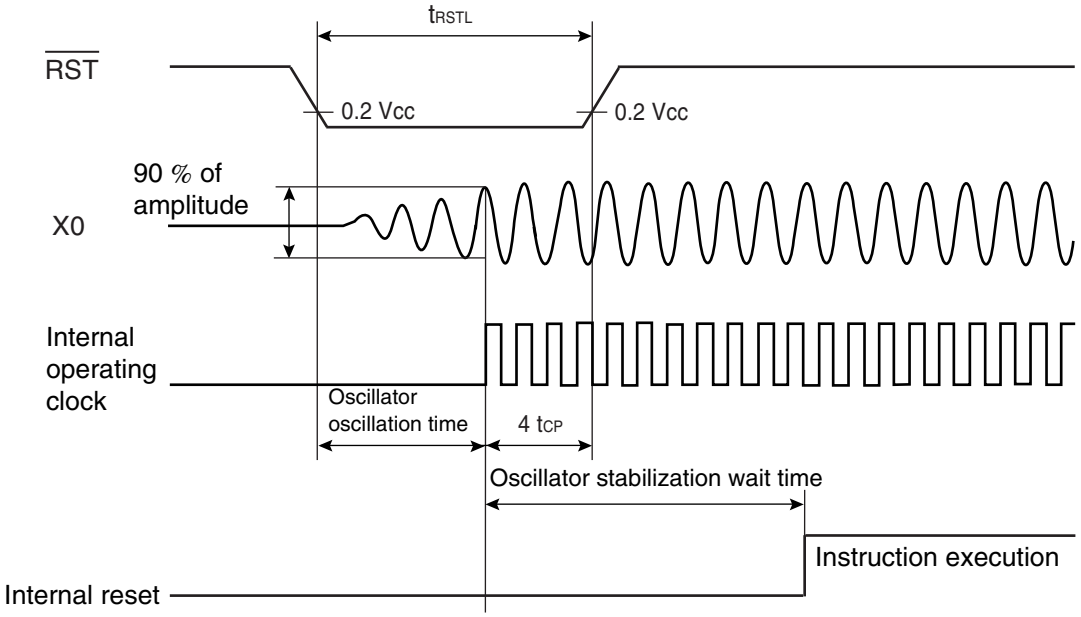
(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condi-tions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	—	16 t_{CP}*1	—	ns	Normal operation
				Oscillator oscillation time*2 + 4 t_{CP}*1	—	ms	Stop mode

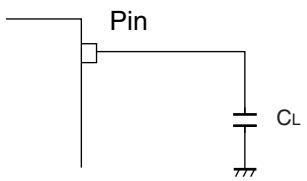
*1 : t_{CP} is internal operating clock cycle time. Refer to " (1) Clock Timing".

*2 : Oscillator oscillation time is the time to 90 % of amplitude. For a crystal oscillator this is on the order of several milliseconds to tens of milliseconds. For a ceramic oscillator, this is several hundred microseconds to several milliseconds. For an external clock signal the value is 0 ms.

• In stop mode



• Condition for measurement of AC standards



C_L : Load capacitance applied to pins during testing
CLK, ALE : C_L = 30 pF
AD15 to AD00 (address data bus) , $\overline{RD}$, $\overline{WR}$,
A23 to A00/D15 to D00 : C_L = 30 pF

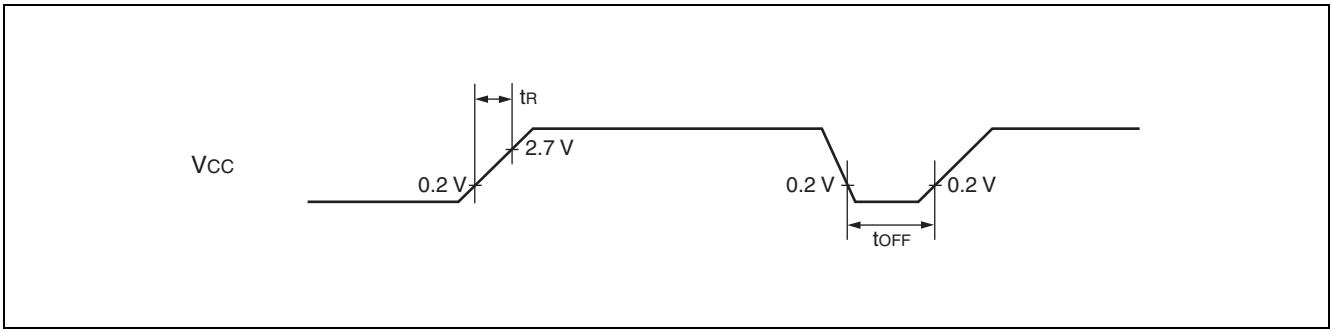
(4) Power-on Reset Standards

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = – 40 °C to + 85 °C)

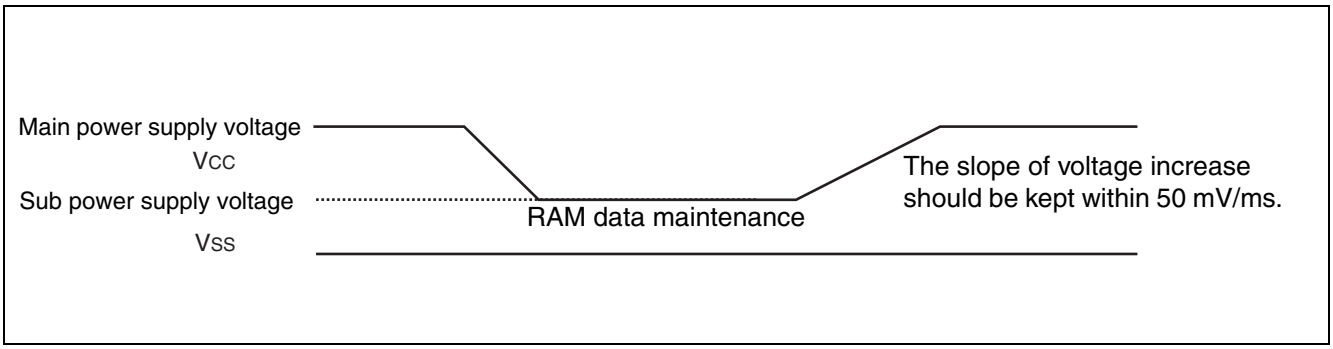
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Power rise time	t_R	V_{CC}	—	0.05	30	ms	*
Power down time	t_{OFF}	V_{CC}		1	—	ms	In repeated operation

* : Power rise time requires V_{CC} < 0.2 V.

Notes: • The above standards are for the application of a power-on reset.
• Within the device, the power-on reset should be applied by switching the power supply off and on again.



Note : Rapid fluctuations in power supply voltage may trigger a power-on reset in some cases. As shown below, when changing supply voltage during operation, it is recommended that voltage changes be suppressed and a smooth restart be applied.

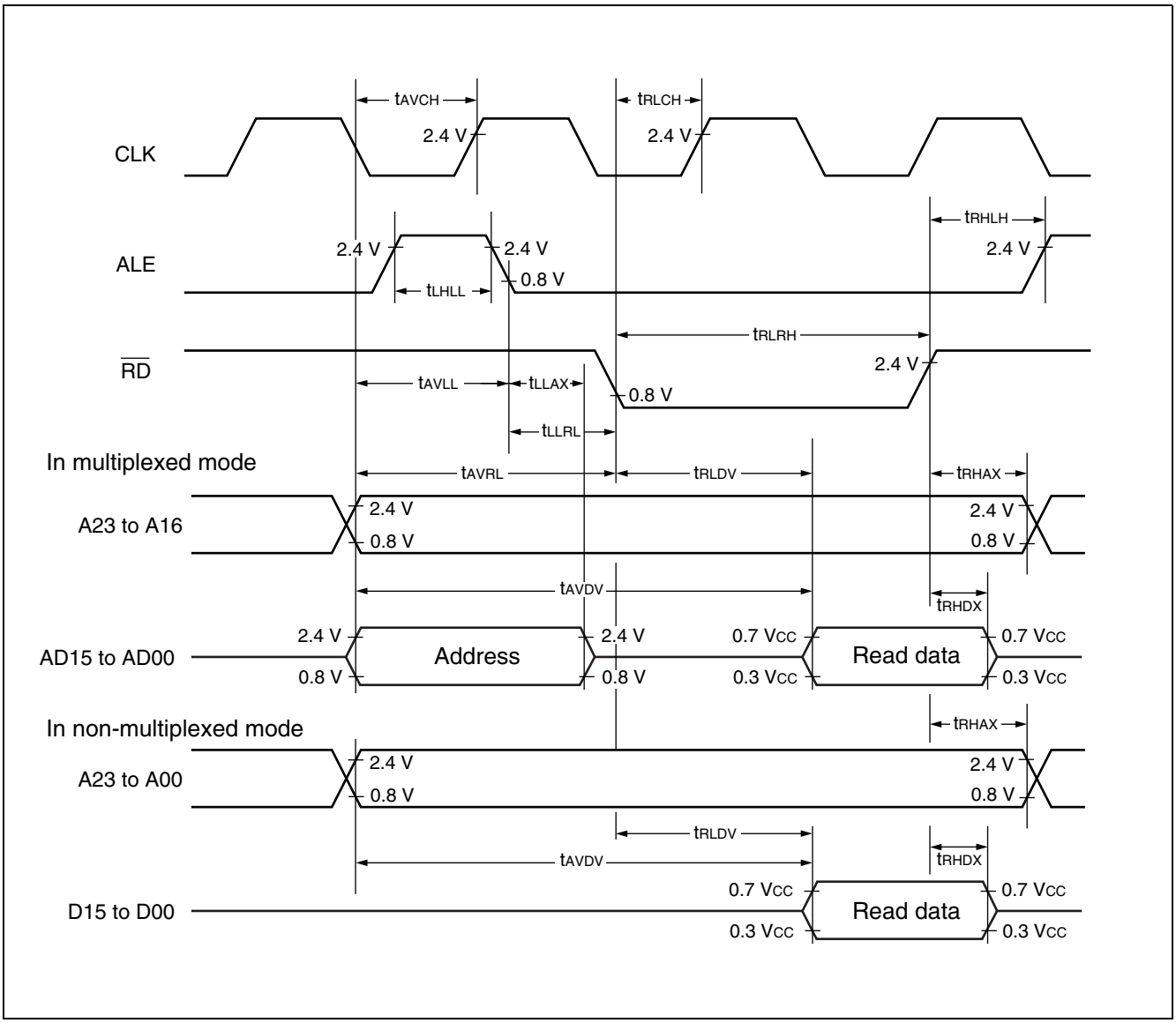


(5) Bus Read Timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = 0 °C to +70 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
ALE pulse width	t_{LHLL}	ALE	—	t_{CP}* / 2 – 15	—	ns	16 MHz < f_{CP} ≤ 25 MHz
				t_{CP}* / 2 – 20	—	ns	8 MHz < f_{CP} ≤ 16 MHz
				t_{CP}* / 2 – 35	—	ns	f_{CP} ≤ 8 MHz
Valid address→ ALE↓ time	t_{AVLL}	Address, ALE	—	t_{CP}* / 2 – 17	—	ns	
				t_{CP}* / 2 – 40	—	ns	f_{CP} ≤ 8 MHz
ALE↓ → address valid time	t_{LLAX}	ALE, Address	—	t_{CP}* / 2 – 15	—	ns	
Valid address → $\overline{RD}$↓ time	t_{AVRL}	$\overline{RD}$, Address	—	t_{CP}* – 25	—	ns	
Valid address → valid data input	t_{AVDV}	Address, Data	—	—	5 t_{CP}* / 2 – 55	ns	
				—	5 t_{CP}* / 2 – 80	ns	f_{CP} ≤ 8 MHz
$\overline{RD}$ pulse width	t_{RLRH}	$\overline{RD}$	—	3 t_{CP}* / 2 – 25	—	ns	16 MHz < f_{CP} ≤ 25 MHz
				3 t_{CP}* / 2 – 20	—	ns	8 MHz < f_{CP} ≤ 16 MHz
$\overline{RD}$↓ → valid data input	t_{RLDV}	$\overline{RD}$, Data	—	—	3 t_{CP}* / 2 – 55	ns	
				—	3 t_{CP}* / 2 – 80	ns	f_{CP} ≤ 8 MHz
$\overline{RD}$↑ → data hold time	t_{RHDX}	$\overline{RD}$, Data	—	0	—	ns	
$\overline{RD}$↑ → ALE↑time	t_{RHLH}	$\overline{RD}$, ALE	—	t_{CP}* / 2 – 15	—	ns	
$\overline{RD}$↑ → address valid time	t_{RHAX}	Address, $\overline{RD}$	—	t_{CP}* / 2 – 10	—	ns	
Valid address → CLK↑ time	t_{AVCH}	Address, CLK	—	t_{CP}* / 2 – 17	—	ns	
$\overline{RD}$↓ → CLK↑time	t_{RLCH}	$\overline{RD}$, CLK	—	t_{CP}* / 2 – 17	—	ns	
ALE↓ → $\overline{RD}$↓ time	t_{LLRL}	$\overline{RD}$, ALE	—	t_{CP}* / 2 – 15	—	ns	

* : t_{CP} is internal operating clock cycle time. Refer to " (1) Clock Timing".

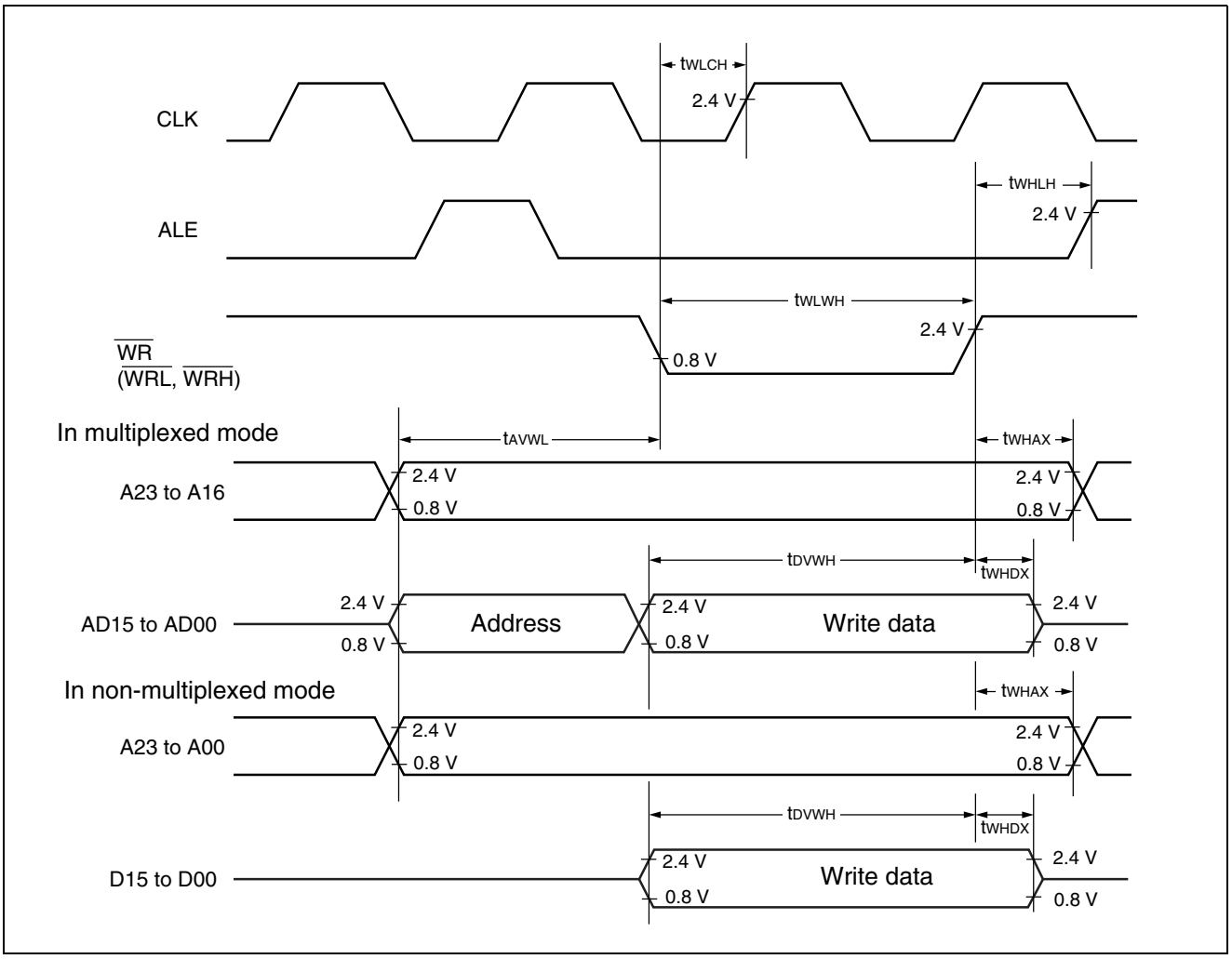

CLK
ALE
RD
In multiplexed mode
A23 to A16
AD15 to AD00
In non-multiplexed mode
A23 to A00
D15 to D00
tAVCH
tRLCH
tRHLH
tLHLL
tRLRH
tAVLL
tLLAX
tLLRL
tAVRL
tRLDV
tRHAX
tAVDV
tRHDX
2.4 V
0.8 V
0.7 VCC
0.3 VCC
Address
Read data

(6) Bus Write Timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = 0 °C to +70 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Valid address → $\overline{WR}\downarrow$ time	t_{AVWL}	Address, $\overline{WR}$	—	t_{CP}* – 15	—	ns	
$\overline{WR}$ pulse width	t_{WLWH}	$\overline{WRL}$, $\overline{WRH}$	—	3 t_{CP}* / 2 – 25	—	ns	16 MHz < f_{CP} ≤ 25 MHz
			—	3 t_{CP}* / 2 – 20	—	ns	8 MHz < f_{CP} ≤ 16 MHz
Valid data output → $\overline{WR}\uparrow$ time	t_{DVWH}	Data, $\overline{WR}$	—	3 t_{CP}* / 2 – 15	—	ns	
$\overline{WR}\uparrow$ → data hold time	t_{WHDX}	$\overline{WR}$, Data	—	10	—	ns	16 MHz < f_{CP} ≤ 25 MHz
			—	20	—	ns	8 MHz < f_{CP} ≤ 16 MHz
			—	30	—	ns	f_{CP} ≤ 8 MHz
$\overline{WR}\uparrow$ → address valid time	t_{WHAX}	$\overline{WR}$, Address	—	t_{CP}* / 2 – 10	—	ns	
$\overline{WR}\uparrow$ → ALE↑ time	t_{WHLH}	$\overline{WR}$, ALE	—	t_{CP}* / 2 – 15	—	ns	
$\overline{WR}\downarrow$ → CLK↑ time	t_{WLCH}	$\overline{WR}$, CLK	—	t_{CP}* / 2 – 17	—	ns	

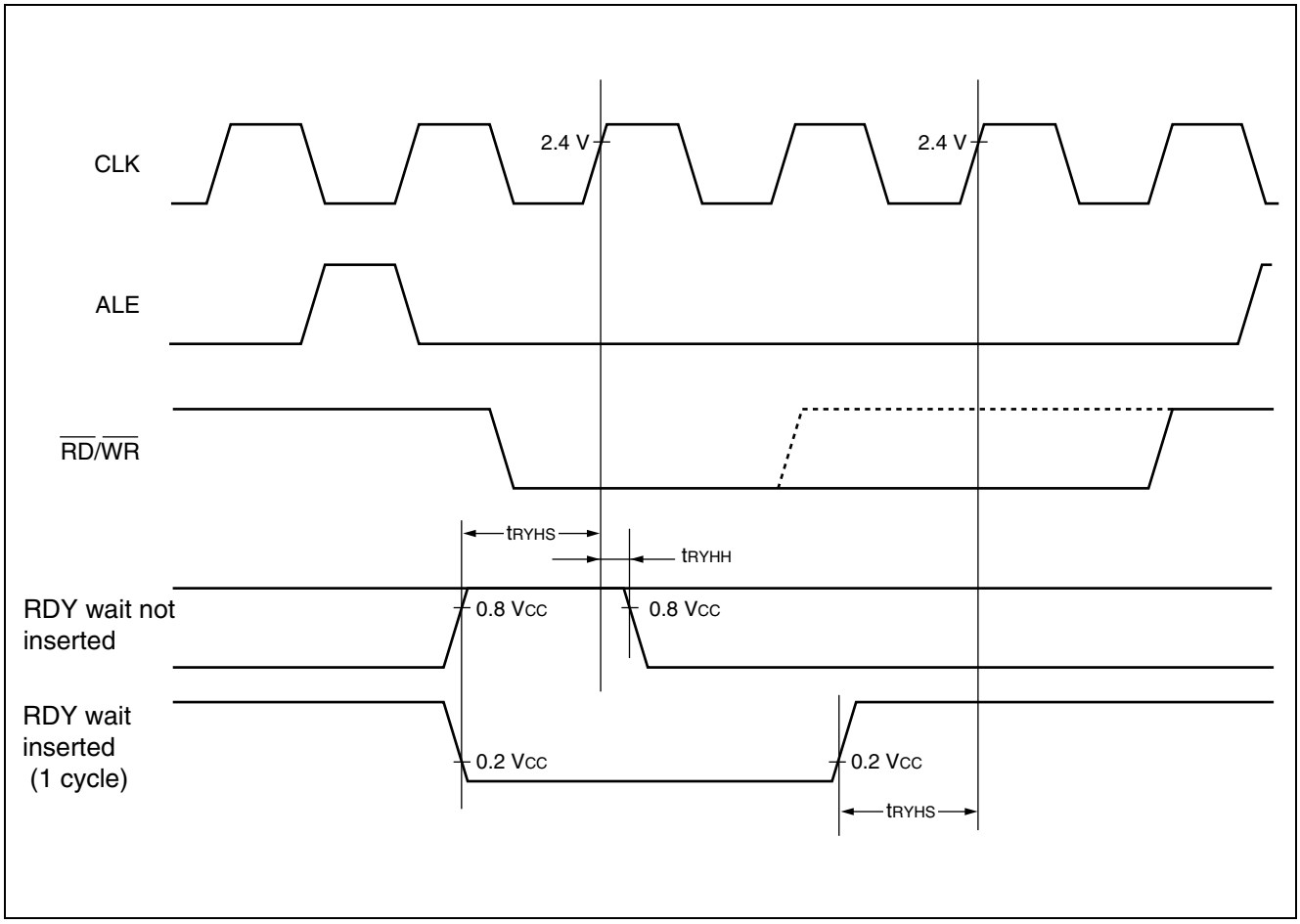
* : t_{CP} is internal operating clock cycle time. Refer to " (1) Clock Timing".


tWLCH
2.4 V
CLK
tWHLH
2.4 V
ALE
tWLWH
2.4 V
WR
(WRL, WRH)
0.8 V
In multiplexed mode
tAVWL
tWHAX
A23 to A16
2.4 V
0.8 V
2.4 V
0.8 V
tDVWH
tWHDX
AD15 to AD00
2.4 V
0.8 V
Address
2.4 V
0.8 V
Write data
2.4 V
0.8 V
In non-multiplexed mode
tWHAX
A23 to A00
2.4 V
0.8 V
2.4 V
0.8 V
tDVWH
tWHDX
D15 to D00
2.4 V
0.8 V
Write data
2.4 V
0.8 V

(7) Ready Input Timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = 0 °C to +70 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY	—	35	—	ns	
			—	70	—	ns	at f_{CP} = 8 MHz
RDY hold time	t_{RYHH}		—	0	—	ns	



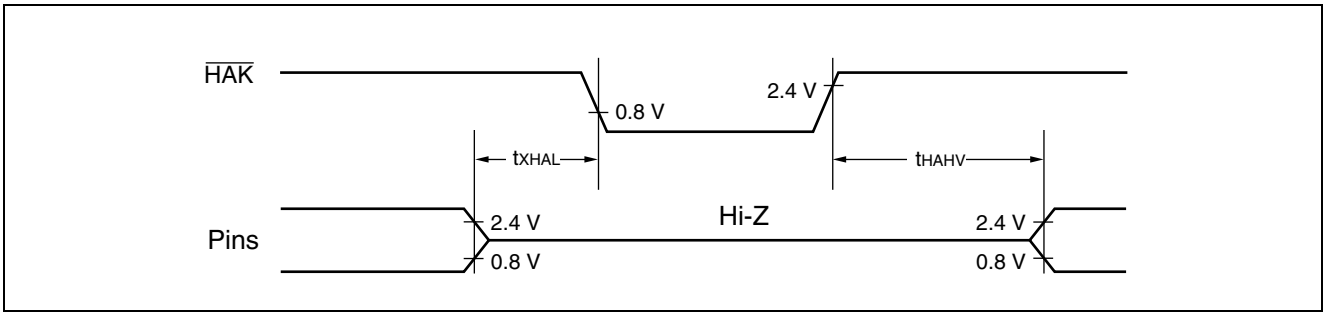
(8) Hold Timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Pin floating→ $\overline{HAK}$ ↓ time	t_{XHAL}	$\overline{HAK}$	—	30	t_{CP}*	ns
$\overline{HAK}$↓ → pin valid time	t_{HAHV}	$\overline{HAK}$		t_{CP}*	2 t_{CP}*	ns

* : t_{CP} is internal operating clock cycle time. Refer to " (1) Clock Timing".

Note : One or more cycles are required from the time the HRQ pin is read until the $\overline{HAK}$ signal changes.



(9) UART Timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = − 40 °C to + 85 °C)

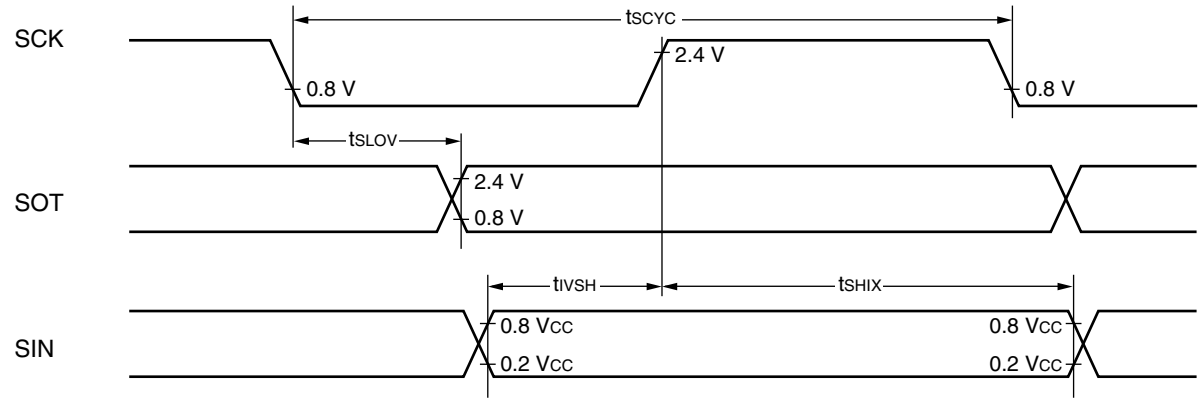
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	—	Internal shift clock mode output pins : C_L*1 = 80 pF + 1 TTL	8 t_{CP}*2	—	ns	
SCK↓ → SOT delay time	t_{SLOV}	—		− 80	+ 80	ns	
				− 120	+ 120	ns	f_{CP} = 8 MHz
Valid SIN→ SCK↑	t_{IVSH}	—		100	—	ns	
				200	—	ns	f_{CP} = 8 MHz
SCK↑ → valid SIN hold time	t_{SHIX}	—		t_{CP}*2	—	ns	
Serial clock "H" pulse width	t_{SHSL}	—	External shift clock mode output pins : C_L*1 = 80 pF + 1 TTL	4 t_{CP}*2	—	ns	
Serial clock "L" pulse width	t_{SLSH}	—		4 t_{CP}*2	—	ns	
SCK↓ → SOT delay time	t_{SLOV}	—		—	150	ns	
				—	200	ns	f_{CP} = 8 MHz
Valid SIN → SCK↑	t_{IVSH}	—		60	—	ns	
				120	—	ns	f_{CP} = 8 MHz
SCK↑ → valid SIN hold time	t_{SHIX}	—		60	—	ns	
				120	—	ns	f_{CP} = 8 MHz

*1 : C_L is the load capacitance applied to pins for testing.

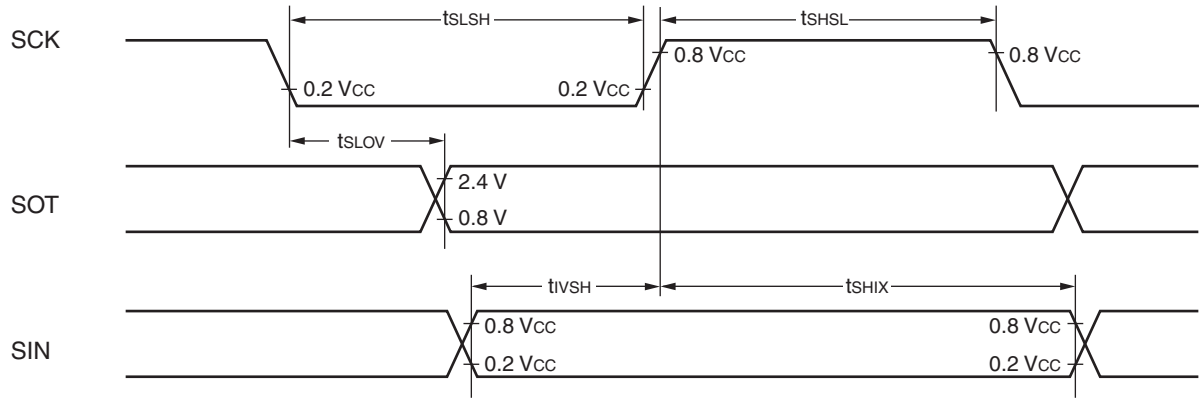
*2 : t_{CP} is internal operating clock cycle time. Refer to " (1) Clock Timing".

Note : The above rating is in CLK synchronous mode.

• Internal shift clock mode



• External shift clock mode



(10) Extended I/O Serial Interface Timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = – 40 °C to + 85 °C)

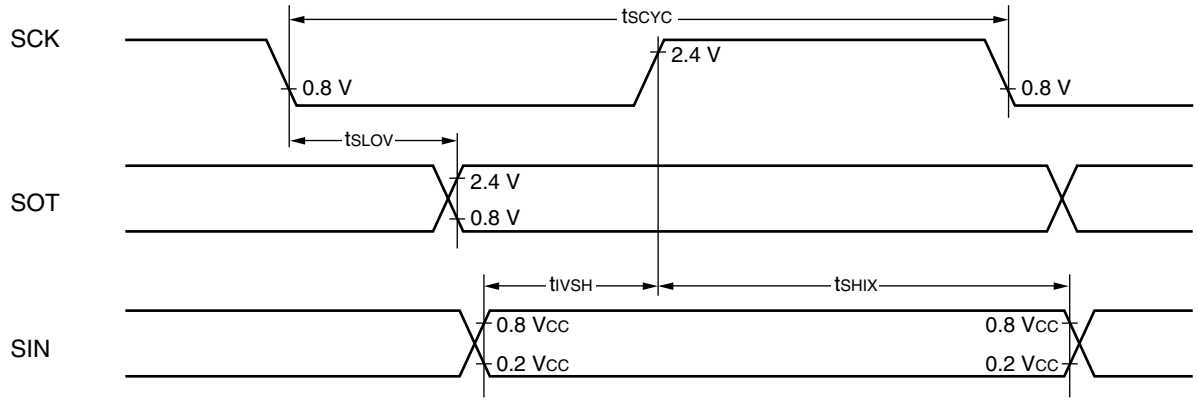
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	—	Internal shift clock mode output pins : C_L*1 = 80 pF + 1 TTL	8 t_{CP}*2	—	ns	
SCK↓ → SOT delay time	t_{SLOV}	—		–80	+ 80	ns	
				–120	+ 120	ns	f_{CP} = 8 MHz
Valid SIN → SCK↑	t_{IVSH}	—		100	—	ns	
				200	—	ns	f_{CP} = 8 MHz
SCK↑ → valid SIN hold time	t_{SHIX}	—		t_{CP}*2	—	ns	
Serial clock “H” pulse width	t_{SHSL}	—	External shift clock mode output pins : C_L*1 = 80 pF + 1 TTL	4 t_{CP}*2	—	ns	
Serial clock “L” pulse width	t_{SLSH}	—		4 t_{CP}*2	—	ns	
SCK↓ → SOT delay time	t_{SLOV}	—		—	150	ns	
				—	200	ns	f_{CP} = 8 MHz
Valid SIN → SCK↑	t_{IVSH}	—		60	—	ns	
				120	—	ns	f_{CP} = 8 MHz
SCK↑ → valid SIN hold time	t_{SHIX}	—		60	—	ns	
				120	—	ns	f_{CP} = 8 MHz

*1 : C_L is the load capacitance applied to pins for testing.

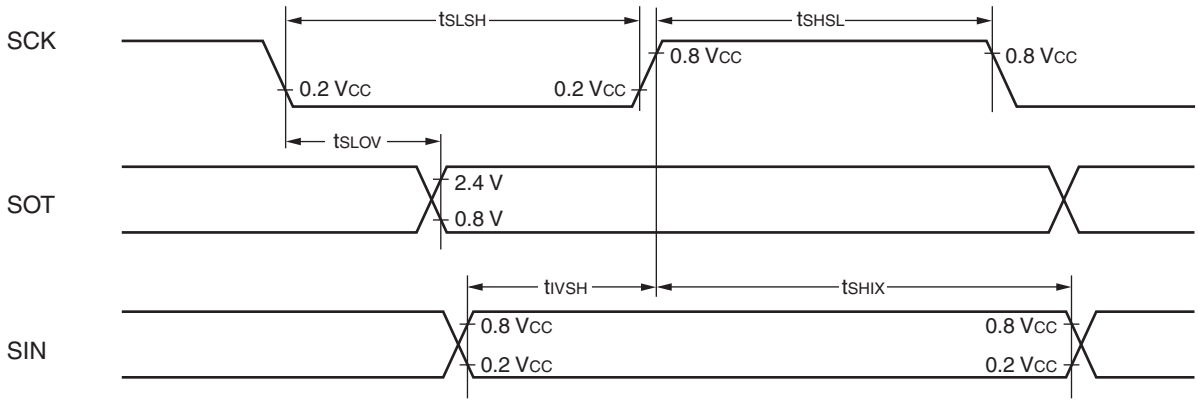
*2 : t_{CP} is internal operating clock cycle time. Refer to “ (1) Clock Timing”.

Notes : • The above rating is in CLK synchronous mode.
• Values on this table are target values.

• Internal shift clock mode



• External shift clock mode

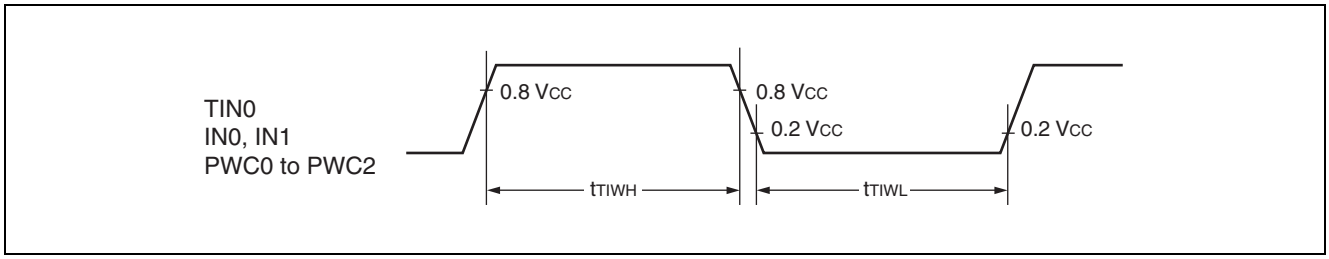


(11) Timer Input Timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	TIN0, IN0, IN1, PWC0 to PWC2	—	4 t_{CP}*	—	ns

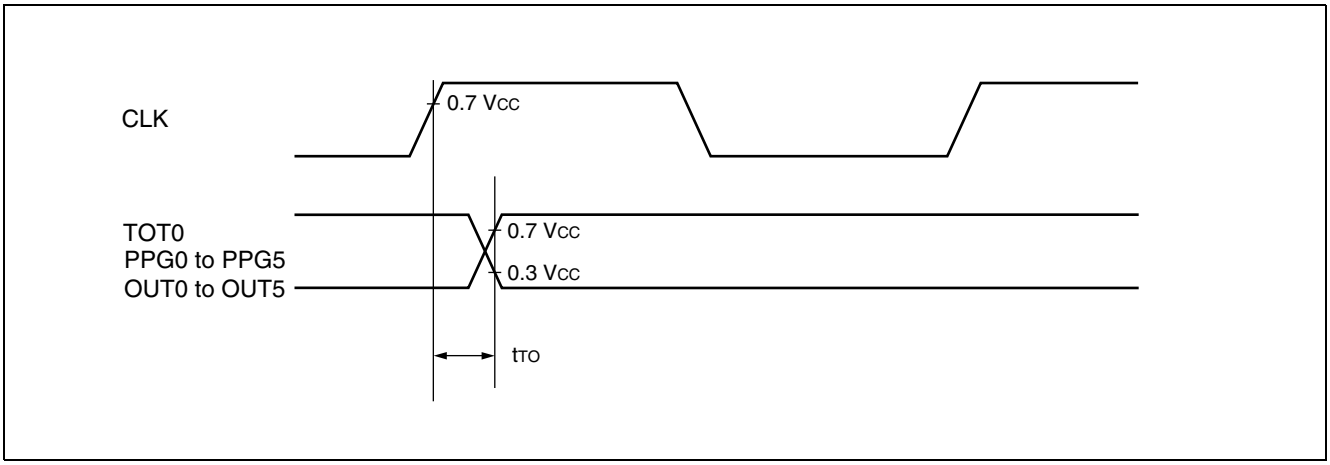
* : t_{CP} is internal operating clock cycle time. Refer to " (1) Clock Timing".



(12) Timer Output Timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
CLK↑ → T_{OUT} change time PPG0 to PPG5 change time OUT0 to OUT5 change time	t_{TO}	TOT0, PPG0 to PPG5, OUT0 to OUT5	Load conditions 80 pF	30	—	ns



(13) I²C Timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Condition	Standard-mode		Unit
			Min	Max	
SCL clock frequency	f_{SCL}	When power supply voltage of external pull-up resistance is 5.5 V R = 1.3 kΩ, C = 50 pF*2 When power supply voltage of external pull-up resistance is 3.6 V R = 1.6 kΩ, C = 50 pF*2	0	100	kHz
Hold time (repeated) START condition SDA↓ → SCL↓	t_{HDSTA}		4.0	—	µs
"L" width of the SCL clock	t_{LOW}		4.7	—	µs
"H" width of the SCL clock	t_{HIGH}		4.0	—	µs
Set-up time (repeated) START condition SCL↑ → SDA↓	t_{SUSTA}		4.7	—	µs
Data hold time SCL↓ → SDA↓↑	t_{HDDAT}		0	3.45*3	µs
Data set-up time SDA↓↑ → SCL↑	t_{SUDAT}	When power supply voltage of external pull-up resistance is 5.5 V f_{CP}*1 ≤ 20 MHz, R = 1.3 kΩ, C = 50 pF*2 When power supply voltage of external pull-up resistance is 3.6 V f_{CP}*1 ≤ 20 MHz, R = 1.6 kΩ, C = 50 pF*2	250*4	—	ns
		When power supply voltage of external pull-up resistance is 5.5 V f_{CP}*1 > 20 MHz, R = 1.3 kΩ, C = 50 pF*2 When power supply voltage of external pull-up resistance is 3.6 V f_{CP}*1 > 20 MHz, R = 1.6 kΩ, C = 50 pF*2	200*4	—	ns
Set-up time for STOP condition SCL↑ → SDA↑	t_{SUSTO}	When power supply voltage of external pull-up resistance is 5.5 V R = 1.3 kΩ, C = 50 pF*2 When power supply voltage of external pull-up resistance is 3.6 V R = 1.6 kΩ, C = 50 pF*2	4.0	—	µs
Bus free time between a STOP and START condition	t_{BUS}		4.7	—	µs

*1 : f_{CP} is internal operation clock frequency. Refer to " (1) Clock Timing".

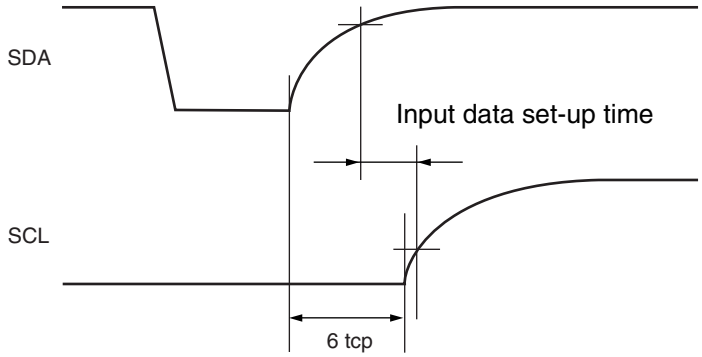
*2 : R,C : Pull-up resistor and load capacitor of the SCL and SDA lines.

*3 : The maximum t_{HDDAT} only has to be met if the device does not stretch the "L" width (t_{LOW}) of the SCL signal.

*4 : Refer to "• Note of SDA and SCL set-up time".

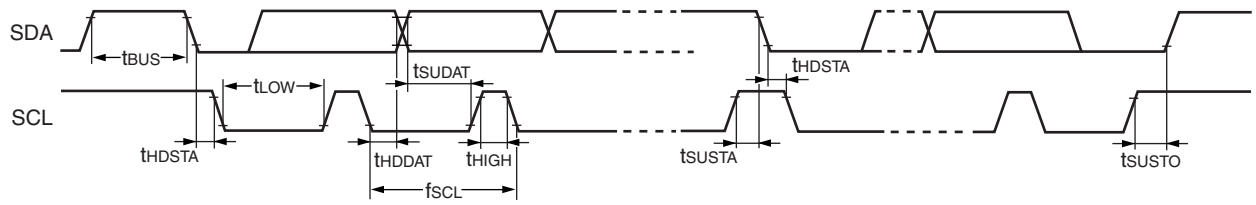
Note : V_{CC} = $V_{CC}3$ = $V_{CC}5$

• Note of SDA and SCL set-up time



Note : The rating of the input data set-up time in the device connected to the bus cannot be satisfied depending on the load capacitance or pull-up resistor.
Be sure to adjust the pull-up resistor of SDA and SCL if the rating of the input data set-up time cannot be satisfied.

• Timing definition

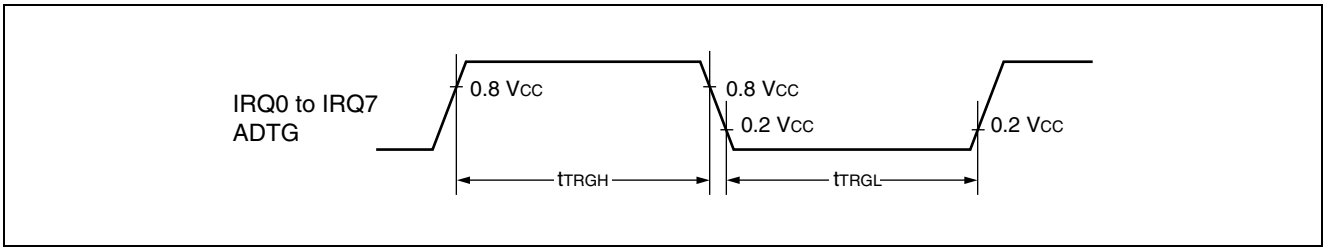


(14) Trigger Input Timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH} t_{TRGL}	ADTG, IRQ0 to IRQ7	—	5 t_{CP}*	—	ns	Normal operation
				1	—	µs	Stop mode

* : t_{CP} is internal operating clock cycle time. Refer to “ (1) Clock Timing”.

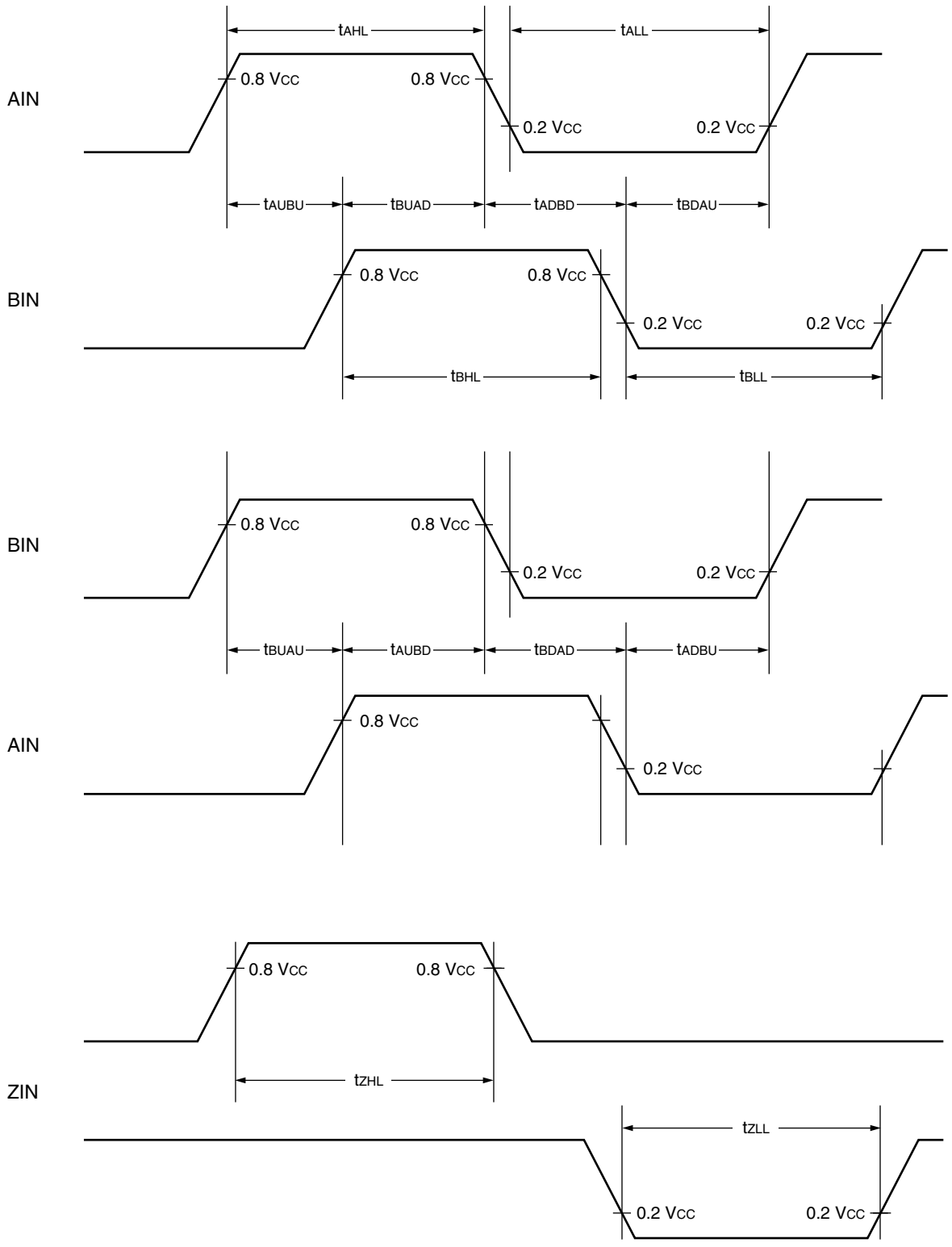


(15) Up-down Counter Timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
AIN input “H” pulse width	t_{AHL}	AIN0, AIN1, BIN0, BIN1	Load conditions 80 pF	8 t_{CP}*	—	ns
AIN input “L” pulse width	t_{ALL}			8 t_{CP}*	—	ns
BIN input “H” pulse width	t_{BHL}			8 t_{CP}*	—	ns
BIN input “L” pulse width	t_{BLL}			8 t_{CP}*	—	ns
AIN↑→ BIN↑ time	t_{AUBU}			4 t_{CP}*	—	ns
BIN↑→ AIN↓ time	t_{BUAD}			4 t_{CP}*	—	ns
AIN↓→ BIN↑ time	t_{ADBD}			4 t_{CP}*	—	ns
BIN↓→ AIN↑ time	t_{BDAU}			4 t_{CP}*	—	ns
BIN↑→ AIN↑ time	t_{BUAU}			4 t_{CP}*	—	ns
AIN↑→ BIN↓ time	t_{AUBD}			4 t_{CP}*	—	ns
BIN↓→ AIN↑ time	t_{BDAD}			4 t_{CP}*	—	ns
AIN↓→ BIN↑ time	t_{ADBU}			4 t_{CP}*	—	ns
ZIN input “H” pulse width	t_{ZHL}	ZIN0, ZIN1		4 t_{CP}*	—	ns
ZIN input “L” pulse width	t_{ZLL}			4 t_{CP}*	—	ns

* : t_{CP} is internal operating clock cycle time. Refer to “ (1) Clock Timing”.

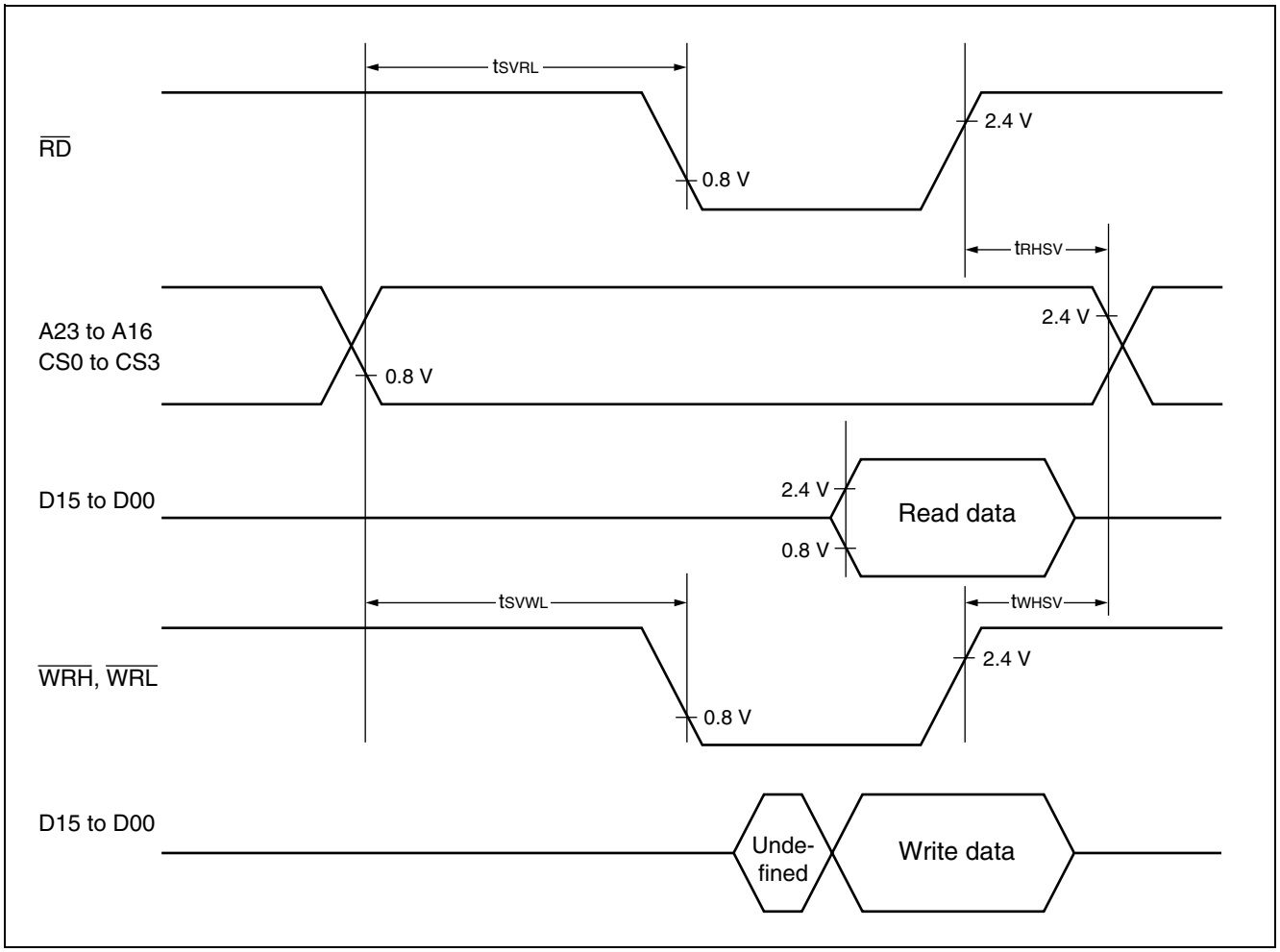

AIN
tAHL
tALL
0.8 VCC
0.8 VCC
0.2 VCC
0.2 VCC
tAUBU
tBUAD
tADBD
tBDAU
BIN
0.8 VCC
0.8 VCC
0.2 VCC
0.2 VCC
tBHL
tBLL
BIN
0.8 VCC
0.8 VCC
0.2 VCC
0.2 VCC
tBUAU
tAUBD
tBDAD
tADBU
AIN
0.8 VCC
0.2 VCC
ZIN
0.8 VCC
0.8 VCC
tZHL
tZLL
0.2 VCC
0.2 VCC

(16) Chip Select Output Timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Chip select output valid time → $\overline{RD}$↓	t_{SVRL}	CS0 to CS3, $\overline{RD}$	—	t_{CP}* / 2 – 7	—	ns
Chip select output valid time→ $\overline{WR}$↓	t_{SVWL}	CS0 to CS3, $\overline{WRH}$, $\overline{WRL}$	—	t_{CP}* / 2 – 7	—	ns
$\overline{RD}$↑→ chip select output valid time	t_{RHSV}	$\overline{RD}$, CS0 to CS3	—	t_{CP}* / 2 – 17	—	ns
$\overline{WR}$↑→ chip select output valid time	t_{WHSV}	$\overline{WRH}$, $\overline{WRL}$, CS0 to CS3	—	t_{CP}* / 2 – 17	—	ns

* : t_{CP} is internal operating clock cycle time. Refer to “ (1) Clock Timing”.



Note : Due to the configuration of the internal bus, the chip select output signals are changed simultaneously and therefore may cause the bus conflict conditions. AC cannot be warranted between the ALE output signal and the chip select output signal.

5. A/D Converter Electrical Characteristics

(V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, 2.7 V ≤ AVRH, T_A = –40 °C to +85 °C)

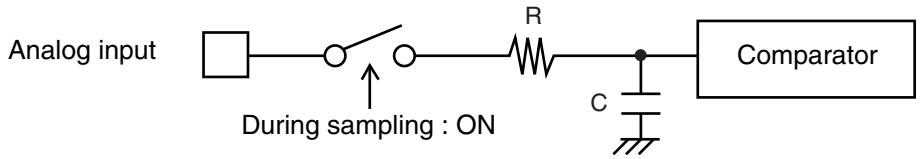
Parameter	Symbol	Pin name	Value			Unit
			Min	Typ	Max	
Resolution	—	—	—	—	10	bit
Total error	—	—	—	—	± 3.0	LSB
Linear error	—	—	—	—	± 2.5	LSB
Differential linearity error	—	—	—	—	± 1.9	LSB
Zero transition voltage	V_{OT}	AN0 to AN7	AV_{SS} – 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	V
Full scale transition voltage	V_{FST}	AN0 to AN7	AVRH – 3.5 LSB	AVRH – 1.5 LSB	AVRH + 0.5 LSB	V
Conversion time	—	—	3.68 *1	—	—	µs
Analog port input current	I_{AIN}	AN0 to AN7	—	0.1	10	µA
Analog input voltage	V_{AIN}	AN0 to AN7	AV_{SS}	—	AVRH	V
Reference voltage	—	AVRH	AV_{SS} + 2.2	—	AV_{CC}	V
Power supply current	I_A	AV_{CC}	—	1.4	3.5	mA
	I_{AH}	AV_{CC}	—	—	5 *2	µA
Reference voltage supply current	I_R	AVRH	—	94	150	µA
	I_{RH}	AVRH	—	—	5 *2	µA
Offset between channels	—	AN0 to AN7	—	—	4	LSB

*1 : At machine clock frequency of 25 MHz.

*2 : CPU stop mode current when A/D converter is not operating (at V_{CC} = AV_{CC} = AVRH = 3.0 V) .

- **About the external impedance of the analog input and its sampling time**
  - A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision.

- Analog input equivalent circuit



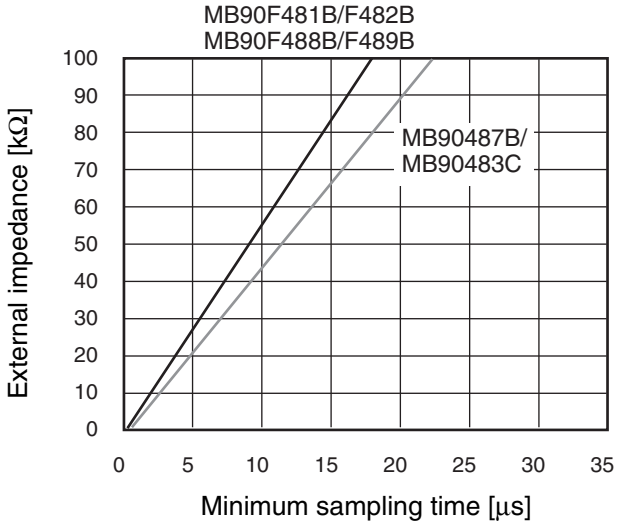
	R	C
MB90487B	2.5 kΩ (Max)	31.0 pF (Max)
MB90F481B/F482B	1.9 kΩ (Max)	25.0 pF (Max)
MB90F488B/F489B	1.9 kΩ (Max)	25.0 pF (Max)

Note: The values are reference values.

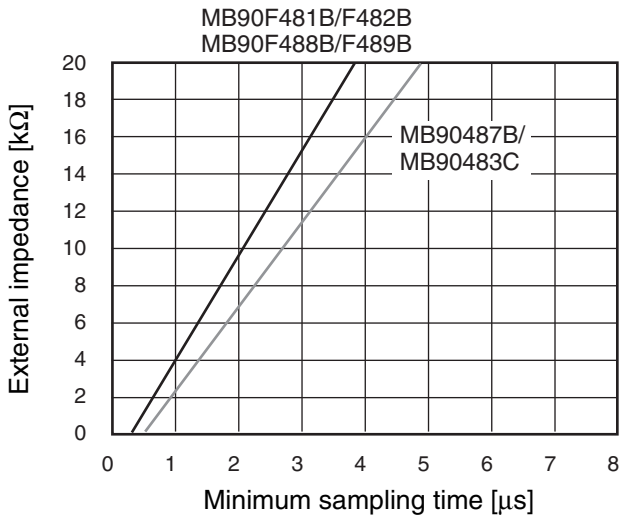
  - To satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value.

- The relationship between external impedance and minimum sampling time

(External impedance = 0 kΩ to 100 kΩ)



(External impedance = 0 kΩ to 20 kΩ)



  - If the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin.

- **About errors**

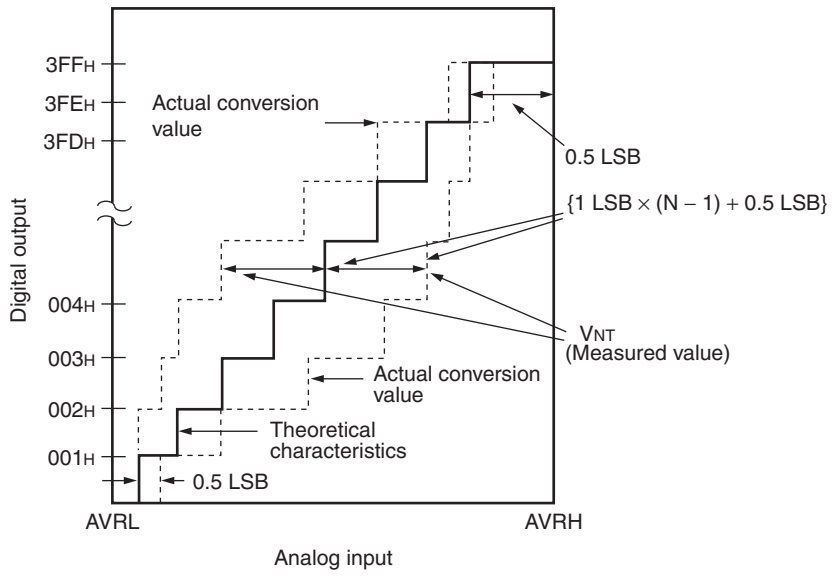
As |AVRH – AVSS| becomes smaller, values of relative errors grow larger.

Note : Concerning sampling time, and compare time when 3.6 V ≥ AVCC ≥ 2.7 V, then
Sampling time : 1.92 µs, compare time : 1.1 µs
Settings should ensure that actual values do not go below these values due to operating frequency changes.

• A/D Converter Glossary

Resolution :	Analog changes that are identifiable with the A/D converter.
Linearity error :	The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1110” ↔ “11 1111 1111”) from actual conversion characteristics.
Differential linearity error :	The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value.
Total error :	The total error is defined as a difference between the actual value and the theoretical value, which includes zero-transition error/full-scale transition error and linearity error.

Total error



$$\text{Total error for digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\ \text{LSB (Theoretical value)} = \frac{AVR - AVss}{1024}\ [V]$$

N : A/D converter digital output value

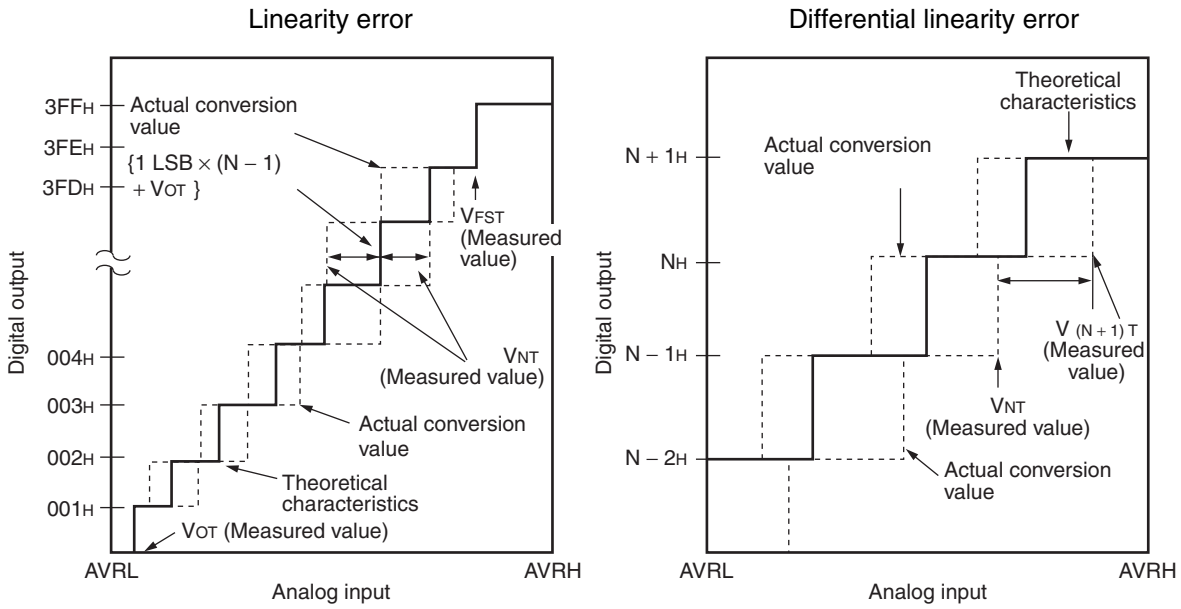
V_{OT} (Theoretical value) = AVss + 0.5 LSB [V]

V_{FST} (Theoretical value) = AVR – 1.5 LSB [V]

V_{NT} : Voltage at a transition of digital output from (N-1) H, N_H

(Continued)

(Continued)



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

N : A/D converter digital output value
V_{OT} : Voltage at transition of digital output from “000H” to “001H”
V_{FST} : Voltage at transition of digital output from “3FEH” to “3FFH”

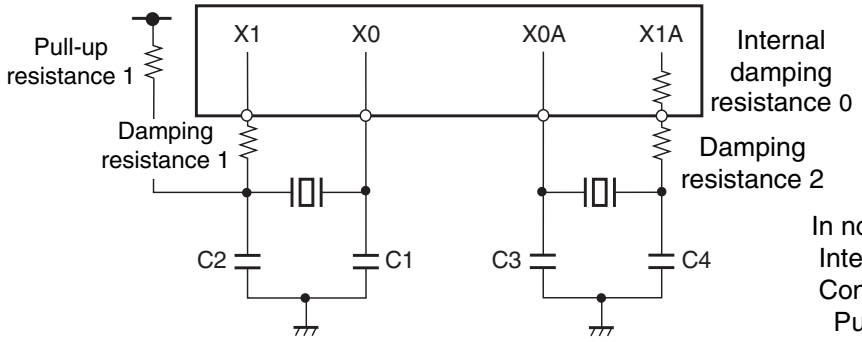
•Flash Memory Program/Erase Characteristics

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	T_A = + 25 °C, V_{CC} = 3.0 V	—	1	15	s	Excludes 00_H programming prior erasure
Chip erase time		—	7	—	s	Excludes 00_H programming prior erasure
Word (16-bit) programming time		—	16	3600	µs	Excludes system-level overhead
Program/Erase cycle	—	10000	—	—	cycle	
Flash Memory Data hold time	Average T_A = + 85 °C	10	—	—	year	*

* : The value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85 °C) .

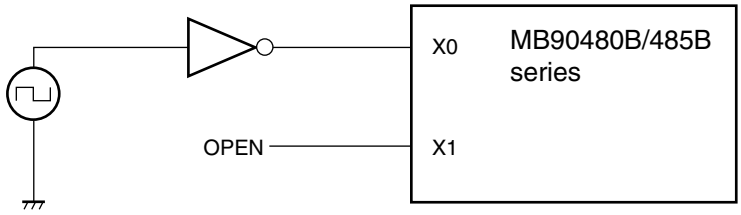
• Use of the X0/X1, X0A/X1A pins

When used with a crystal oscillator



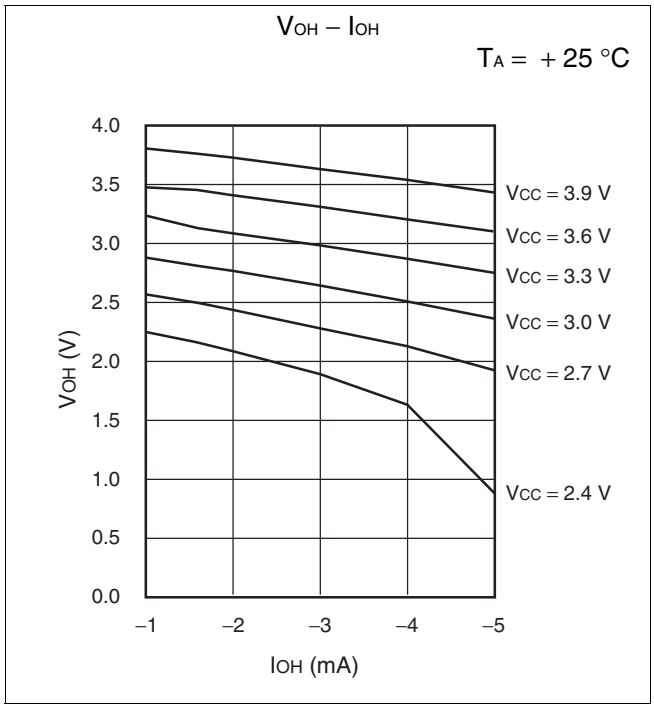
In normal use :
Internal damping resistance 0 : Typ 600 Ω
Consult with the oscillator manufacturer.
Pull-up resistance 1,
Damping resistance 1, 2,
C1 to C4

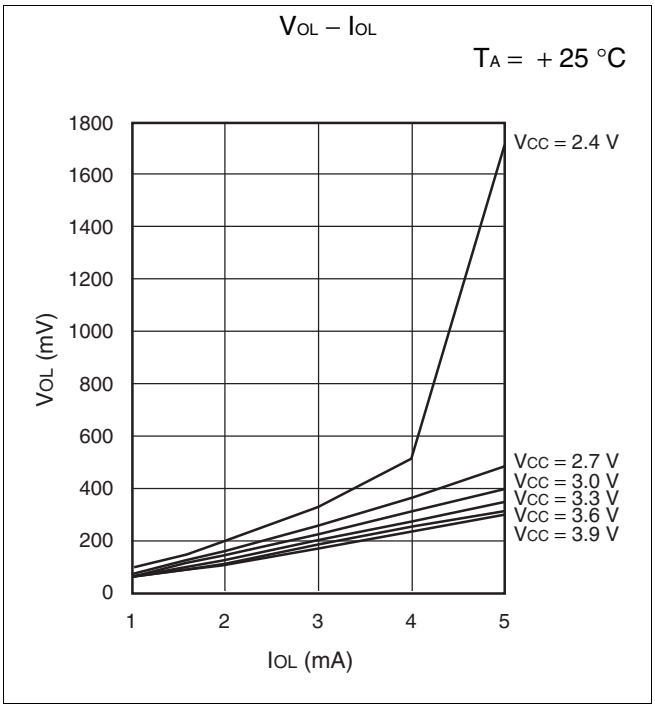
•Sample use with external clock input

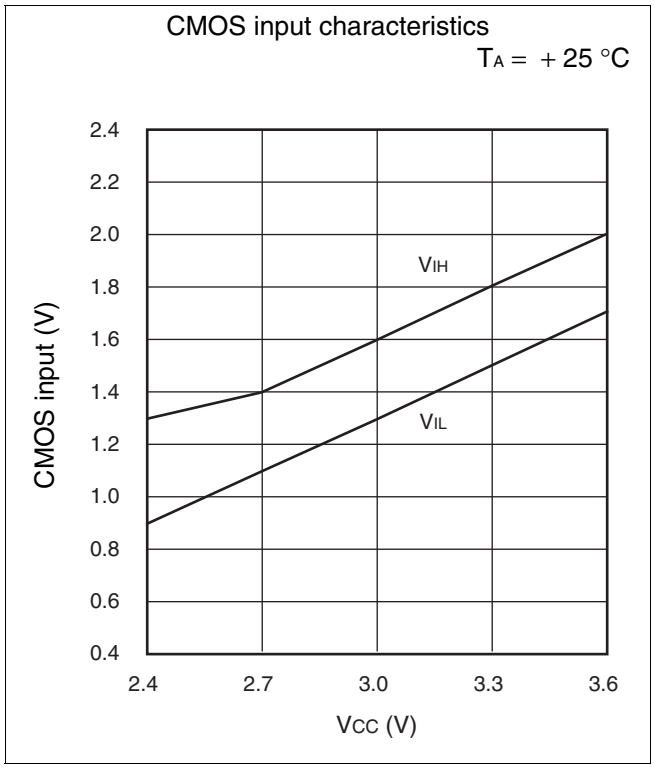


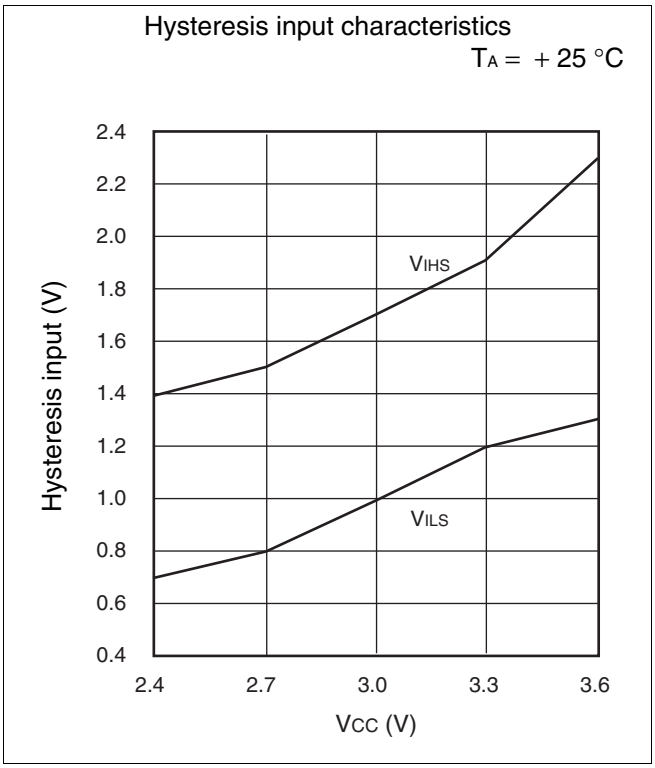
■ EXAMPLE CHARACTERISTICS

• MB90F482B

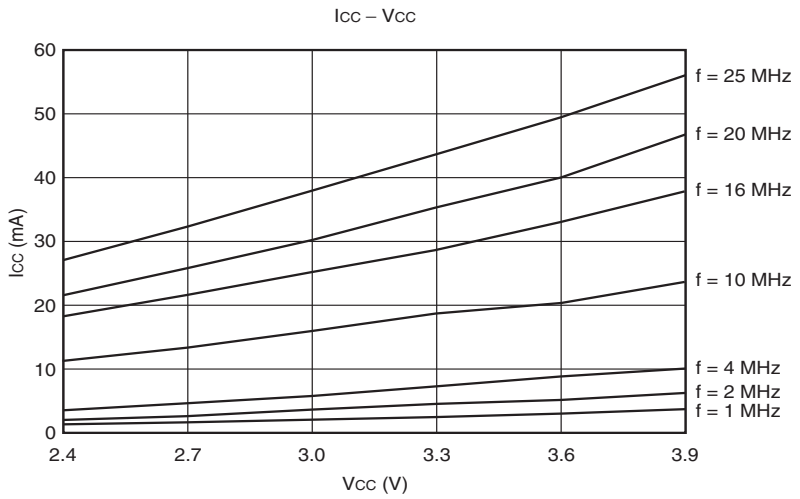


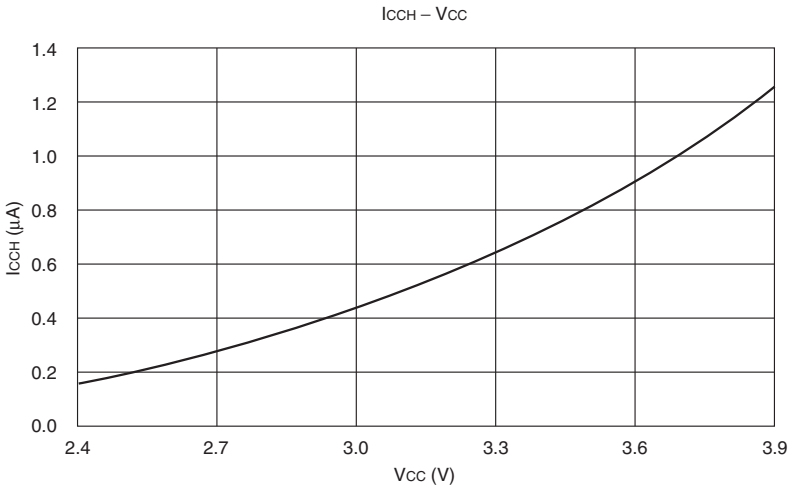


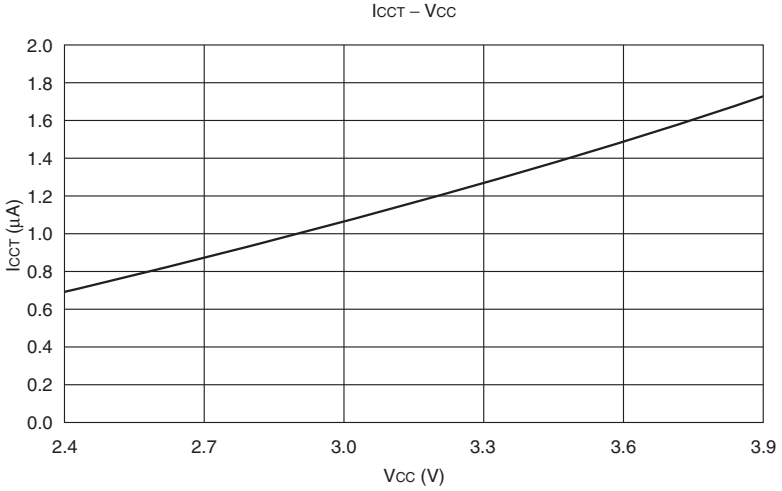




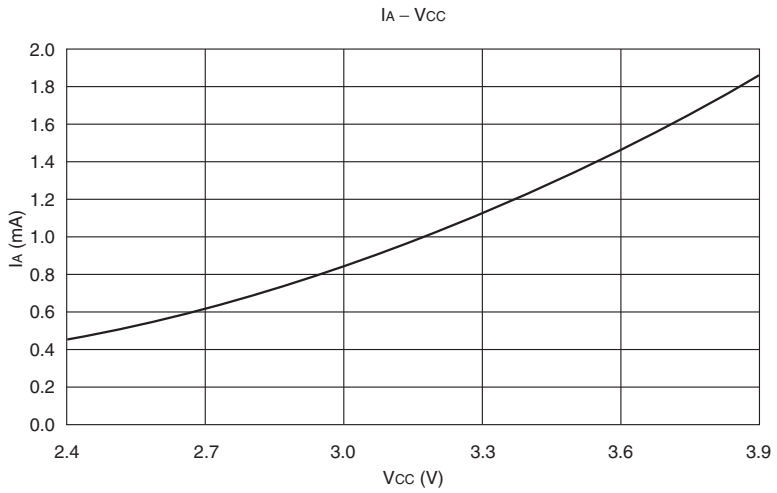
(Continued)

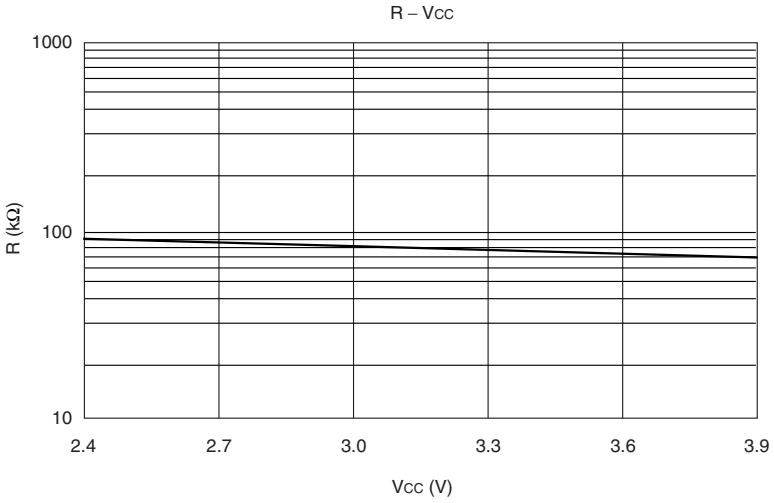

ICC – VCC
60
50
40
30
20
10
0
ICC (mA)
2.4
2.7
3.0
3.3
3.6
3.9
VCC (V)
f = 25 MHz
f = 20 MHz
f = 16 MHz
f = 10 MHz
f = 4 MHz
f = 2 MHz
f = 1 MHz


ICCH – VCC
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0.0
ICCH (µA)
2.4
2.7
3.0
3.3
3.6
3.9
VCC (V)


ICCT – VCC
2.0
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0.0
ICCT (µA)
2.4
2.7
3.0
3.3
3.6
3.9
VCC (V)

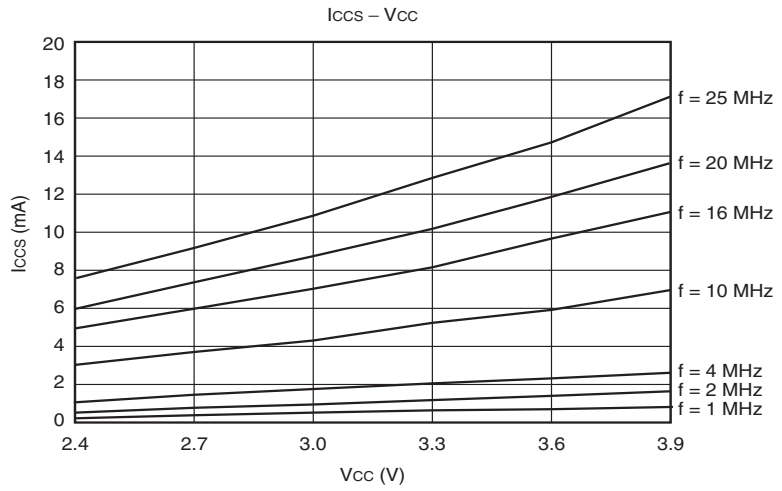
(Continued)

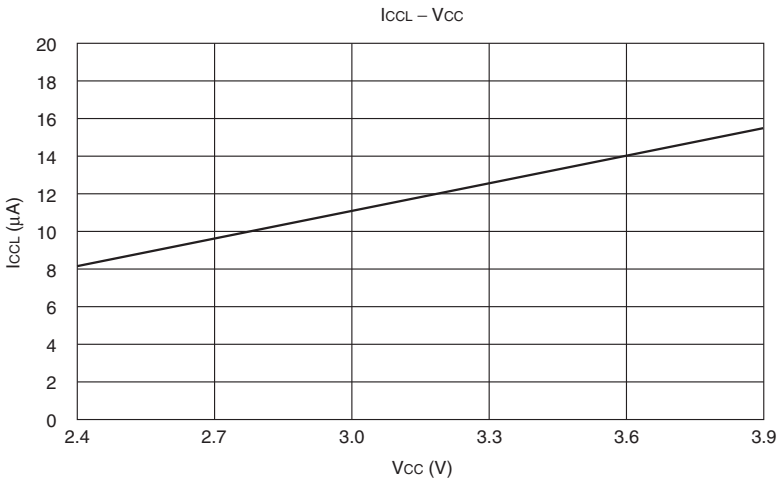

IA – VCC
2.0
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0.0
IA (mA)
2.4
2.7
3.0
3.3
3.6
3.9
VCC (V)

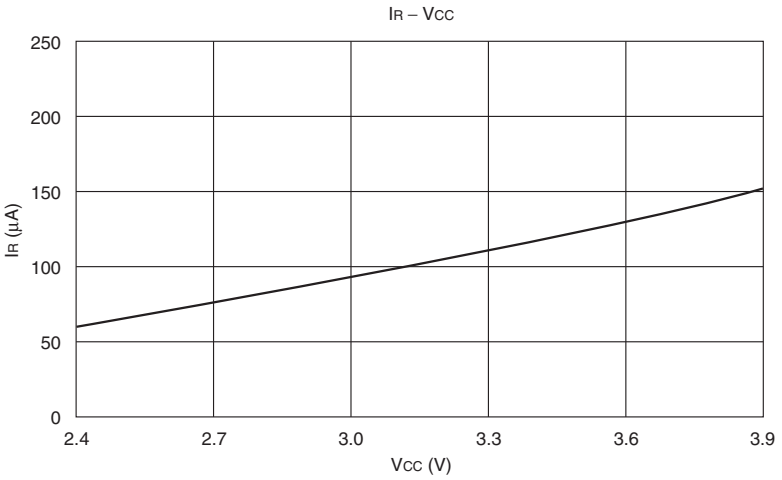

R – VCC
1000
100
10
R (kΩ)
2.4
2.7
3.0
3.3
3.6
3.9
VCC (V)

(Continued)

(Continued)


ICCS – VCC
ICCS (mA)
VCC (V)
f = 25 MHz
f = 20 MHz
f = 16 MHz
f = 10 MHz
f = 4 MHz
f = 2 MHz
f = 1 MHz
0
2
4
6
8
10
12
14
16
18
20
2.4
2.7
3.0
3.3
3.6
3.9

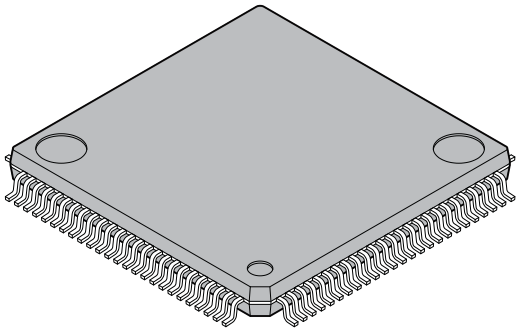

ICCL – VCC
ICCL (µA)
VCC (V)
0
2
4
6
8
10
12
14
16
18
20
2.4
2.7
3.0
3.3
3.6
3.9

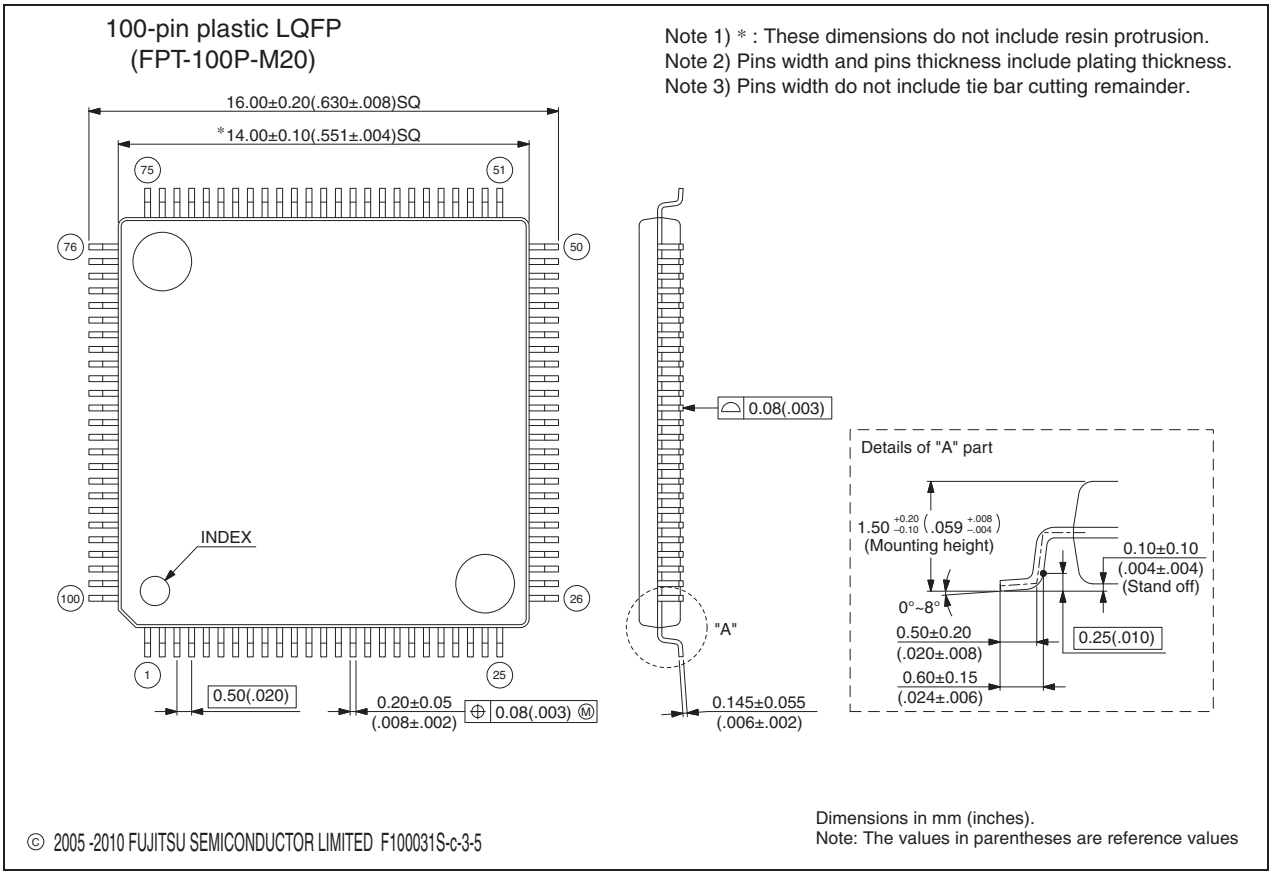

IR – VCC
IR (µA)
VCC (V)
0
50
100
150
200
250
2.4
2.7
3.0
3.3
3.6
3.9

■ ORDERING INFORMATION

Part number	Package
MB90F481BPF MB90F482BPF MB90487BPF MB90488BPF MB90F488BPF MB90483CPF MB90F489BPF	100-pin plastic QFP (FPT-100P-M06)
MB90483CPMC MB90487BPMC MB90488BPMC MB90F481BPMC MB90F482BPMC MB90F488BPMC MB90F489BPMC	100-pin plastic LQFP (FPT-100P-M20)

■ PACKAGE DIMENSIONS

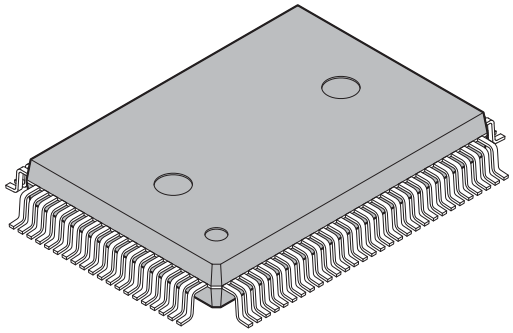
100-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	14.0 mm × 14.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm Max
	Weight	0.65 g
(FPT-100P-M20)	Code (Reference)	P-LFQFP100-14×14-0.50



Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

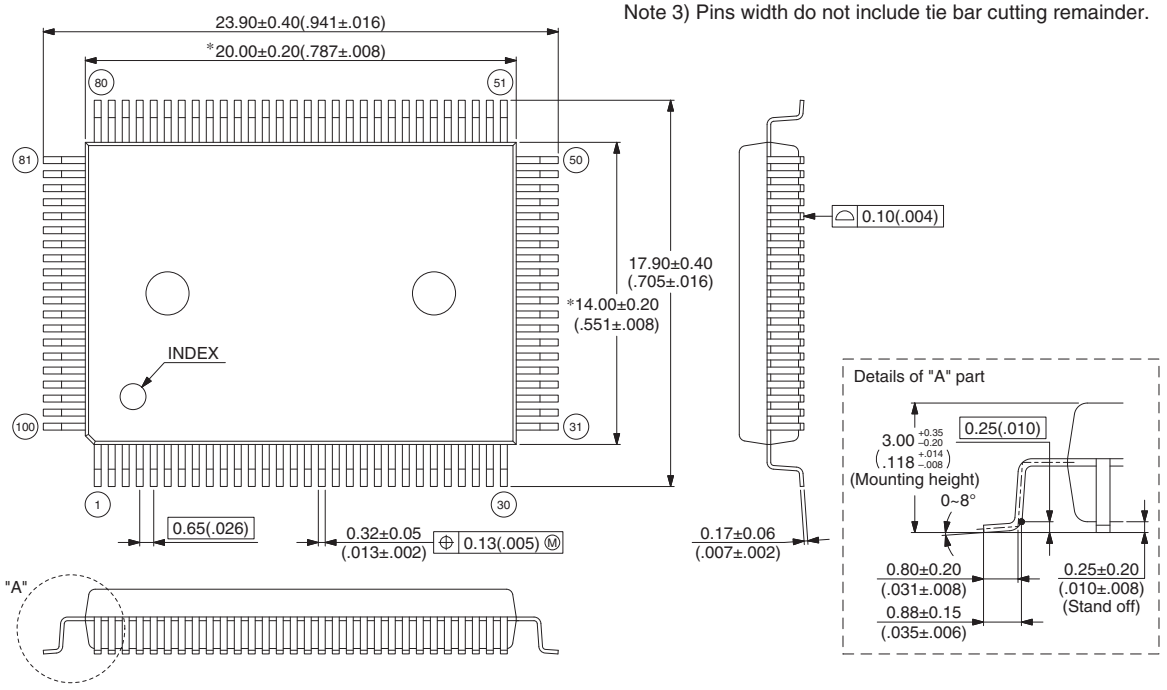
(Continued)

(Continued)

100-pin plastic QFP		
	Lead pitch	0.65 mm
	Package width package length	14.00 20.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	3.35 mm MAX
	Code (Reference)	P-QFP100-14 20-0.65
(FPT-100P-M06)		

100-pin plastic QFP
(FPT-100P-M06)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

■ MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
86	■ ELECTRICAL CHARACTERISTICS 2. Recommended Operating Conditions	Corrected the “Operating temperature” as follows. Added “At external bus operation” to remarks. Corrected the value; Min: $-40 \rightarrow 0$ / Max: $+85 \rightarrow +70$

The vertical lines marked in the left side of the page show the changes.

MEMO

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