

8-bit Microcontroller

CMOS

F²MC-8FX MB95150M Series

MB95156M/F156M/F156N/F156J/FV100D-103

■ DESCRIPTION

The MB95150M series is general-purpose, single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers contain a variety of peripheral functions.

Note : F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

■ FEATURE

- F²MC-8FX CPU core
 - Instruction set optimized for controllers
 - Multiplication and division instructions
 - 16-bit arithmetic operations
 - Bit test branch instruction
 - Bit manipulation instructions etc.
- Clock
 - Main clock
 - Main PLL clock
 - Sub clock
 - Sub PLL clock

(Continued)

For the information for microcontroller supports, see the following web site.

This web site includes the "**Customer Design Review Supplement**" which provides the latest cautions on system development and the minimal requirements to be checked to prevent problems before the system development.

<http://edevic.fujitsu.com/micom/en-support/>

MB95150M Series

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- Timer
 - 8/16-bit compound timer × 2 channels
 - Can be used to interval timer, PWC timer, PWM timer and input capture.
 - 8/16-bit PPG × 2 channels
 - 16-bit PPG × 1 channel
 - Time-base timer × 1 channel
 - Watch prescaler × 1 channel
- LIN-UART × 1 channel
 - LIN function, clock asynchronous (UART) or clock synchronous (SIO) serial data transfer capable
 - Full duplex double buffer
- UART/SIO × 1 channel
 - Clock asynchronous (UART) or clock synchronous (SIO) serial data transfer capable
 - Full duplex double buffer
- External interrupt × 8 channels
 - Interrupt by edge detection (rising, falling, or both edges can be selected)
 - Can be used to recover from low-power consumption (standby) modes.
- 8/10-bit A/D converter × 8 channels
 - 8-bit or 10-bit resolution can be selected.
- LCD controller (LCDC)
 - 16 SEG × 4 COM (Max 64 pixels)
 - With blinking function
- Low-power consumption (standby) mode
 - Stop mode
 - Sleep mode
 - Watch mode
 - Time-base timer mode
- I/O port: Max 39
 - General-purpose I/O ports (CMOS) : 39 ports
- Programmable input voltage levels of port
 - Automotive input level / CMOS input level / hysteresis input level
- Flash memory security function
 - Protects the content of Flash memory (Flash memory device only)

MB95150M Series

■ PRODUCT LINEUP

Part number		MB95156M	MB95F156M	MB95F156N	MB95F156J
Parameter					
Type		MASK ROM product	Flash memory product		
ROM capacity		32 Kbytes			
RAM capacity		1 Kbyte			
Reset output		Yes/No	Yes		No
Option*	Clock system	Dual clock			
	Low voltage detection reset	Yes/No	No	Yes	
	Clock supervisor	Yes/No	No		Yes
CPU functions		Number of basic instructions : 136 Instruction bit length : 8 bits Instruction length : 1 to 3 bytes Data bit length : 1, 8, and 16 bits Minimum instruction execution time : 61.5 ns (at machine clock frequency 16.25 MHz) Interrupt processing time : 0.6 μs (at machine clock frequency 16.25 MHz)			
Peripheral functions	Ports (Max 39 ports)	General-purpose I/O port (CMOS) : 39 ports Programmable input voltage levels of port : Automotive input level / CMOS input level / hysteresis input level			
	Time-base timer (1 channel)	Interrupt cycle : 0.5 ms, 2.1 ms, 8.2 ms, 32.8 ms (at main oscillation clock 4 MHz)			
	Watchdog timer	Reset generated cycle At main oscillation clock 10 MHz : Min 105 ms At sub oscillation clock 32.768 kHz : Min 250 ms			
	Wild register	Capable of replacing 3 bytes of ROM data			
	UART/SIO (1 channel)	Data transfer capable in UART/SIO Full duplex double buffer, variable data length (5/6/7/8-bit), built-in baud rate generator NRZ type transfer format, error detected function LSB-first or MSB-first can be selected. Clock asynchronous (UART) or clock synchronous (SIO) serial data transfer capable			
	LIN-UART (1 channel)	Dedicated reload timer allowing a wide range of communication speeds to be set. Full duplex double buffer Clock asynchronous (UART) or clock synchronous (SIO) serial data transfer capable LIN functions available as the LIN master or LIN slave.			
	8/10-bit A/D converter (8 channels)	8-bit or 10-bit resolution can be selected.			
	LCD controller (LCDC)	COM output : 4 (Max) SEG output : 16 (Max) LCD drive power supply (bias) pin : 4 16 SEG × 4 COM : 64 pixels can be displayed. Duty LCD mode Operable in LCD standby mode With blinking function Built-in division resistance for LCD drive			

(Continued)

MB95150M Series

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Part number		MB95156M	MB95F156M	MB95F156N	MB95F156J
Parameter					
Peripheral functions	8/16-bit compound timer (2 channels)	Each channel of the timer can be used as “8-bit timer × 2 channels” or “16-bit timer × 1 channel”. Built-in timer function, PWC function, PWM function, capture function, and square waveform output Count clock : 7 internal clocks and external clock can be selected.			
	16-bit PPG (1 channel)	PWM mode or one-shot mode can be selected. Counter operating clock : Eight selectable clock sources Support for external trigger start			
	8/16-bit PPG (2 channels)	Each channel of the PPG can be used as “8-bit PPG × 2 channels” or “16-bit PPG × 1 channel”. Counter operating clock : Eight selectable clock sources			
	Watch counter	Count clock : Four selectable clock sources (125 ms, 250 ms, 500 ms, or 1 s) Counter value can be set from 0 to 63. (Capable of counting for 1 minute when selecting clock source 1 second and setting counter value to 60)			
	Watch prescaler (1 channel)	4 selectable interval times (125 ms, 250 ms, 500 ms, or 1 s)			
	External interrupt (8 channels)	Interrupt by edge detection (rising, falling, or both edges can be selected.) Can be used to recover from standby modes.			
Flash memory		Supports automatic programming, Embedded Algorithm Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Number of write/erase cycles (Minimum) : 10000 times Data retention time : 20 years Boot block configuration Erase can be performed on each block Block protection with external programming voltage Flash Security Feature for protecting the content of the Flash			
Standby mode		Sleep, stop, watch, and time-base timer			

* : For details of option, refer to “■ MASK OPTION”.

Note : Part number of evaluation products in MB95150M series is MB95FV100D-103. When using it, the MCU board (MB2146-303A-E) is required.

■ OSCILLATION STABILIZATION WAIT TIME

The initial value of the main clock oscillation stabilization wait time is fixed to the maximum value. The maximum value is shown as follows.

Oscillation stabilization wait time	Remarks
$(2^{14}-2) / F_{CH}$	Approx. 4.10 ms (at main oscillation clock 4 MHz)

■ PACKAGES AND CORRESPONDING PRODUCTS

Package \ Part number	MB95156M	MB95F156M/F156N/F156J	MB95FV100D-103
FPT-48P-M26	○	○	×
FPT-52P-M01	○	○	×
BGA-224P-M08	×	×	○

- : Available
 × : Unavailable

■ DIFFERENCES AMONG PRODUCTS AND NOTES ON SELECTING PRODUCTS

• Notes on Using Evaluation Products

The Evaluation product has not only the functions of the MB95150M series but also those of other products to support software development for multiple series and models of the F²MC-8FX family. The I/O addresses for peripheral resources not used by the MB95150M series are therefore access-barred. Read/write access to these access-barred addresses may cause peripheral resources supposed to be unused to operate, resulting in unexpected malfunctions of hardware or software.

Particularly, do not use word access to odd numbered byte address in the prohibited areas (If these access are used, the address may be read or written unexpectedly).

Also, as the read values of prohibited addresses on the evaluation product are different to the values on the Flash memory and MASK ROM products, do not use these values in the program.

The functions corresponding to certain bits in single-byte registers may not be supported on some mask ROM and Flash memory products. However, reading or writing to these bits will not cause malfunction of the hardware. Also, as the evaluation, Flash memory, and mask ROM products are designed to have identical software operation, no particular precautions are required.

• Difference of Memory Spaces

If the amount of memory on the Evaluation product is different from that of the Flash memory product or MASK ROM product, carefully check the difference in the amount of memory from the model to be actually used when developing software.

For details of memory space, refer to “■ CPU CORE”.

• Current Consumption

- The current consumption of Flash memory product is typically greater than for MASK ROM product.
- For details of current consumption, refer to “■ ELECTRICAL CHARACTERISTICS”.

• Package

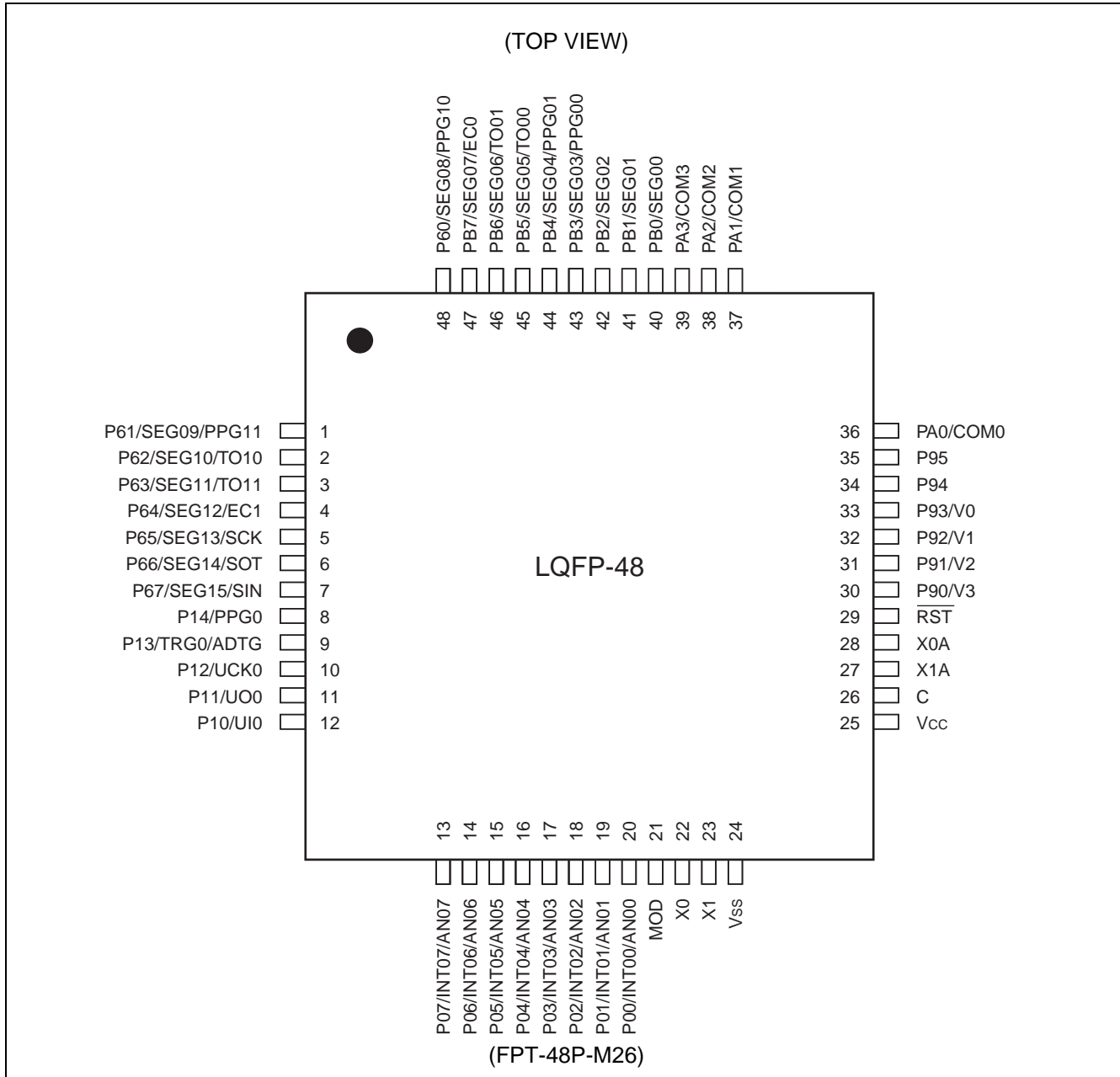
For details of information on each package, refer to “■ PACKAGES AND CORRESPONDING PRODUCTS” and “■ PACKAGE DIMENSIONS”.

• Operating voltage

The operating voltage are different between the Evaluation, Flash memory products, and MASK ROM product.

For details of operating voltage, refer to “■ ELECTRICAL CHARACTERISTICS”.

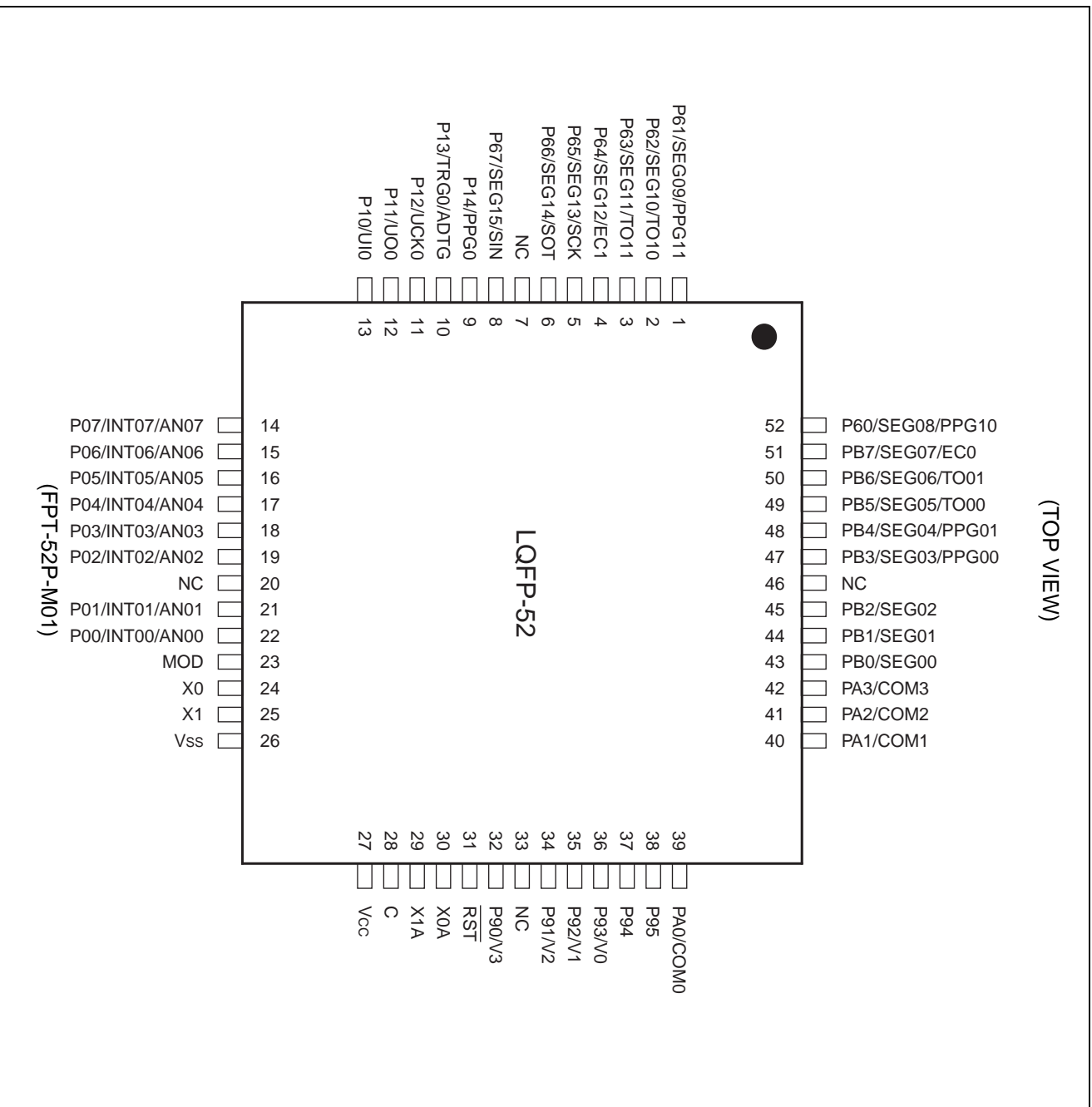
■ PIN ASSIGNMENT



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MB95150M Series

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■ PIN DESCRIPTION

Pin no.		Pin name	I/O circuit type*3	Function
LQFP*1	LQFP*2			
1	1	P61/SEG09/PPG11	M	General-purpose I/O port. The pin is shared with LCDDC SEG output (SEG09) and 8/16-bit PPG ch.1 output (PPG11).
2	2	P62/SEG10/TO10		General-purpose I/O port. The pins are shared with LCDDC SEG output (SEG10, SEG11) and 8/16-bit compound timer ch.1 output (TO10, TO11) .
3	3	P63/SEG11/TO11		General-purpose I/O port. The pin is shared with LCDDC SEG output (SEG12) and 8/16-bit compound timer ch.1 clock input (EC1).
4	4	P64/SEG12/EC1		General-purpose I/O port. The pin is shared with LCDDC SEG output (SEG13) and LIN-UART clock I/O (SCK) .
5	5	P65/SEG13/SCK		General-purpose I/O port. The pin is shared with LCDDC SEG output (SEG14) and LIN-UART data output (SOT) .
6	6	P66/SEG14/SOT		N
7	8	P67/SEG15/SIN	H	
8	9	P14/PPG0		General-purpose I/O port. The pin is shared with 16-bit PPG ch.0 trigger input (TRG0) and A/D converter trigger input (ADTG) .
9	10	P13/TRG0/ADTG		General-purpose I/O port. The pin is shared with UART/SIO ch.0 clock I/O (UCK0) .
10	11	P12/UCK0		General-purpose I/O port. The pin is shared with UART/SIO ch.0 data output (UO0) .
11	12	P11/UO0	G	General-purpose I/O port. The pin is shared with UART/SIO ch.0 data input (UI0) .
12	13	P10/UI0		D
13	14	P07/INT07/AN07		
14	15	P06/INT06/AN06		
15	16	P05/INT05/AN05		
16	17	P04/INT04/AN04		
17	18	P03/INT03/AN03		
18	19	P02/INT02/AN02		
19	21	P01/INT01/AN01		
20	22	P00/INT00/AN00	B	The operating mode designation pin
21	23	MOD		

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MB95150M Series

(Continued)

Pin no.		Pin name	I/O circuit type*3	Function
LQFP*1	LQFP*2			
22	24	X0	A	Main clock oscillation pins
23	25	X1		
24	26	V _{ss}	—	Power supply pin (GND)
25	27	V _{cc}	—	Power supply pin
26	28	C	—	Capacitor connection pin
27	29	X1A	A	Sub clock oscillation pins (32 kHz)
28	30	X0A		
29	31	\overline{RST}	B'	Reset pin
30	32	P90/V3	R	General-purpose I/O port. The pins are shared with power supply pin for LCDC drive (V0 to V3) .
31	34	P91/V2		
32	35	P92/V1		
33	36	P93/V0		
34	37	P94	S	General-purpose I/O port
35	38	P95		
36	39	PA0/COM0	M	General-purpose I/O port. The pins are shared with LCDC COM output (COM0 to COM3) .
37	40	PA1/COM1		
38	41	PA2/COM2		
39	42	PA3/COM3		
40	43	PB0/SEG00	M	General-purpose I/O port. The pins are shared with LCDC SEG output (SEG00 to SEG02) .
41	44	PB1/SEG01		
42	45	PB2/SEG02		
43	47	PB3/SEG03/ PPG00		General-purpose I/O port. The pins are shared with LCDC SEG output (SEG03, SEG04) and 8/16-bit PPG ch.0 output (PPG00, PPG01).
44	48	PB4/SEG04/ PPG01		
45	49	PB5/SEG05/TO00		General-purpose I/O port. The pins are shared with LCDC SEG output (SEG05, SEG06) and 8/16-bit compound timer ch.0 output (TO00, TO01).
46	50	PB6/SEG06/TO01		
47	51	PB7/SEG07/EC0	General-purpose I/O port. The pin is shared with LCDC SEG output (SEG07) and 8/16-bit compound timer ch.0 clock input (EC0).	
48	52	P60/SEG08/ PPG10	M	General-purpose I/O port. The pin is shared with LCDC SEG output (SEG08) and 8/16-bit PPG ch.1 output (PPG10) .
—	7, 20, 33, 46	NC	—	Internal connect pins. Be sure this pin is left open.

*1 : FPT-48P-M26

*2 : FPT-52P-M01

*3 : For the I/O circuit type, refer to “■ I/O CIRCUIT TYPE”.

I/O CIRCUIT TYPE

Type	Circuit	Remarks
A	<p>Standby control</p>	<ul style="list-style-type: none"> • Oscillation circuit • High-speed side Feedback resistance : approx. 1 MΩ • Low-speed side Feedback resistance : approx. 10 MΩ
B	<p>Mode input</p>	<ul style="list-style-type: none"> • Only for input • Hysteresis input
B'	<p>Reset input Reset output</p>	<ul style="list-style-type: none"> • Hysteresis input • Reset output
D	<p>Pull-up control Digital output Digital output Analog input Automotive input Hysteresis input A/D control Standby control External interrupt control</p>	<ul style="list-style-type: none"> • CMOS output • Hysteresis input • Analog input • With pull-up control • Automotive input
G	<p>Pull-up control Digital output Digital output CMOS input Hysteresis input Automotive input Standby control</p>	<ul style="list-style-type: none"> • CMOS output • CMOS input • Hysteresis input • With pull-up control • Automotive input
H	<p>Pull-up control Digital output Digital output Hysteresis input Automotive input Standby control</p>	<ul style="list-style-type: none"> • CMOS output • Hysteresis input • With pull-up control • Automotive input

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MB95150M Series

(Continued)

Type	Circuit	Remarks
M		<ul style="list-style-type: none"> • CMOS output • LCD output • Hysteresis input • Automotive input
N		<ul style="list-style-type: none"> • CMOS output • LCD output • CMOS input • Hysteresis input • Automotive input
R		<ul style="list-style-type: none"> • CMOS output • LCD power supply • Hysteresis input • Automotive input
S		<ul style="list-style-type: none"> • CMOS output • Hysteresis input • Automotive input

■ HANDLING DEVICES

- Preventing Latch-up

Care must be taken to ensure that maximum voltage ratings are not exceeded when they are used.

Latch-up may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- and high-withstand voltage pins or if higher than the rating voltage is applied between V_{CC} pin and V_{SS} pin.

When latch-up occurs, power supply current increases rapidly and might thermally damage elements.

- Stable Supply Voltage

Supply voltage should be stabilized.

A sudden change in power-supply voltage may cause a malfunction even within the guaranteed operating range of the V_{CC} power-supply voltage.

For stabilization, in principle, keep the variation in V_{CC} ripple (p-p value) in a commercial frequency range (50/60 Hz) not to exceed 10% of the standard V_{CC} value and suppress the voltage variation so that the transient variation rate does not exceed 0.1 V/ms during a momentary change such as when the power supply is switched.

- Precautions for Use of External Clock

Even when an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from sub clock mode or stop mode.

- Serial communication

There is a possibility to receive wrong data due to noise or other causes on the serial communication.

Therefore, design a printed circuit board so as to avoid noise.

Consider receiving of wrong data when designing the system. For example apply a checksum and retransmit the data if an error occurs.

■ PIN CONNECTION

- Treatment of Unused Pin

Leaving unused input pins unconnected can cause abnormal operation or latch-up, leaving to permanent damage. Unused input pins should always be pulled up or down through resistance of at least 2 k Ω . Any unused input/output pins may be set to output mode and left open, or set to input mode and treated the same as unused input pins. If there is unused output pin, make it to open.

- Power Supply Pins

In products with multiple V_{CC} or V_{SS} pins, the pins of the same potential are internally connected in the device to avoid abnormal operations including latch-up. However, you must connect the pins to external power supply and a ground line to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with the V_{CC} and V_{SS} pins of this device at the low impedance.

It is also advisable to connect a ceramic bypass capacitor of approximately 0.1 μ F between V_{CC} and V_{SS} pins near this device.

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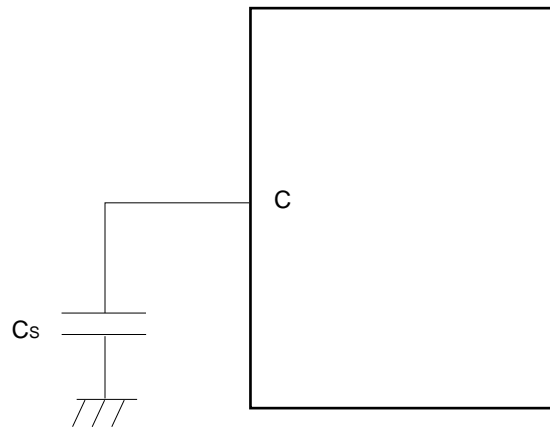
- Mode Pin (MOD)

Connect the MOD pin directly to V_{CC} or V_{SS} .

To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the MOD pin to V_{CC} or V_{SS} pins and to provide a low-impedance connection.

Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. A bypass capacitor of V_{CC} pin must have a capacitance value higher than C_s . For connection of smoothing capacitor C_s , refer to the diagram below.

- C pin connection diagram



- NC Pins

Any pins marked "NC" (not connected) must be left open.

■ PROGRAMMING FLASH MEMORY MICROCONTROLLERS USING PARALLEL PROGRAMMER

• Supported Parallel Programmers and Adapters

The following table lists supported parallel programmers and adapters.

Package	Applicable adapter model	Parallel programmers
FPT-48P-M26	TEF110-95F156HPFV	AF9708 (Ver 02.35G or more) AF9709/B (Ver 02.35G or more) AF9723+AF9834 (Ver 02.08E or more)
FPT-52P-M01	TEF110-95F156HPMC	

Note : For information on applicable adapter models and parallel programmers, contact the following:
Flash Support Group, Inc. TEL: +81-53-428-8380

• Sector Configuration

The individual sectors of Flash memory correspond to addresses used for CPU access and programming by the parallel programmer as follows:

• MB95F156M/F156N/F156J

Flash memory	CPU address	Programmer address*
32 Kbytes	8000 _H	18000 _H
	FFFF _H	1FFFF _H

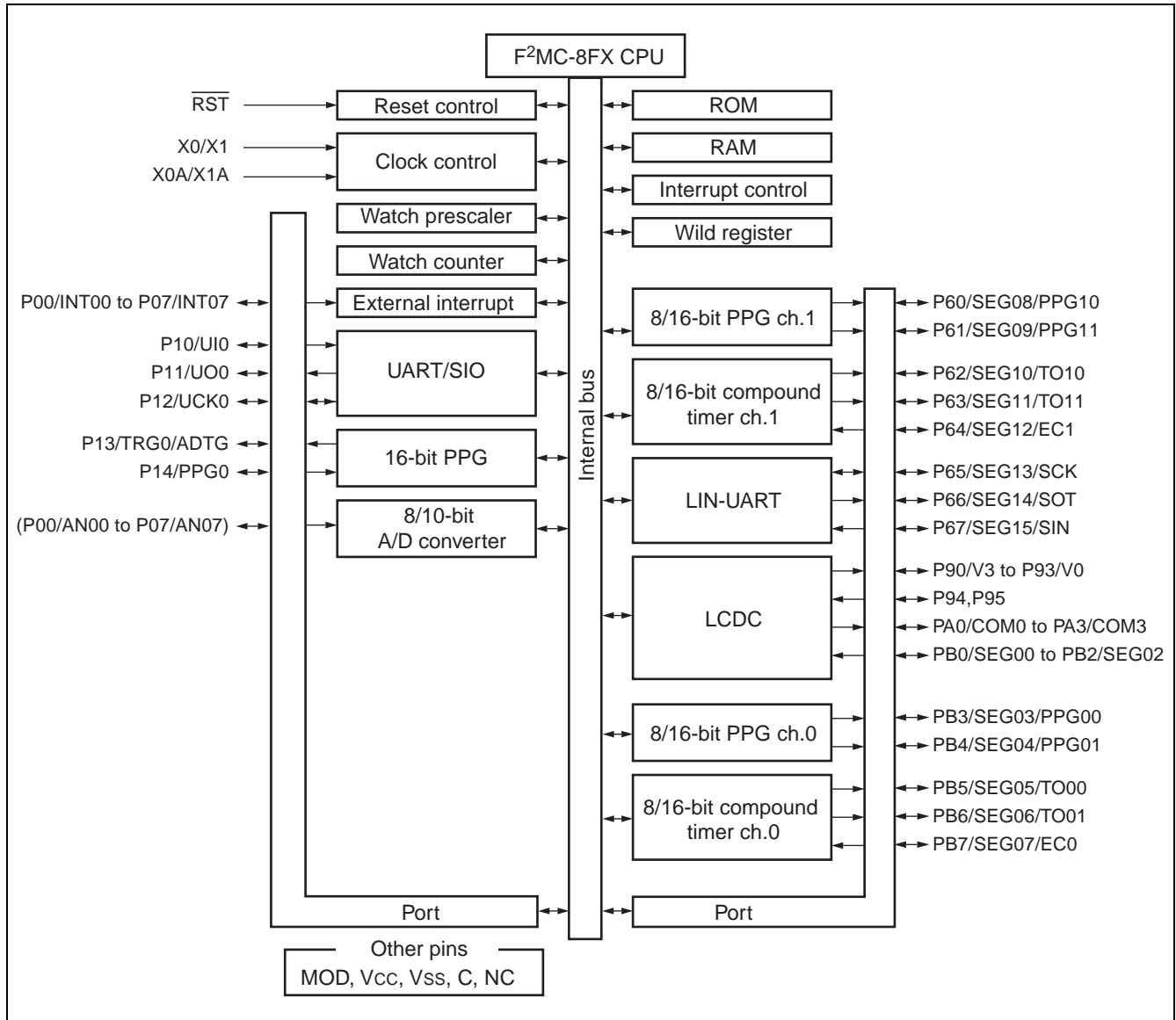
*: Programmer addresses are corresponding to CPU addresses, used when the parallel programmer programs data into Flash memory.
These programmer addresses are used for the parallel programmer to program or erase data in Flash memory.

• Programming Method

- 1) Set the type code of the parallel programmer to 17222.
- 2) Load program data to programmer addresses 18000_H to 1FFFF_H.
- 3) Programmed by parallel programmer.

MB95150M Series

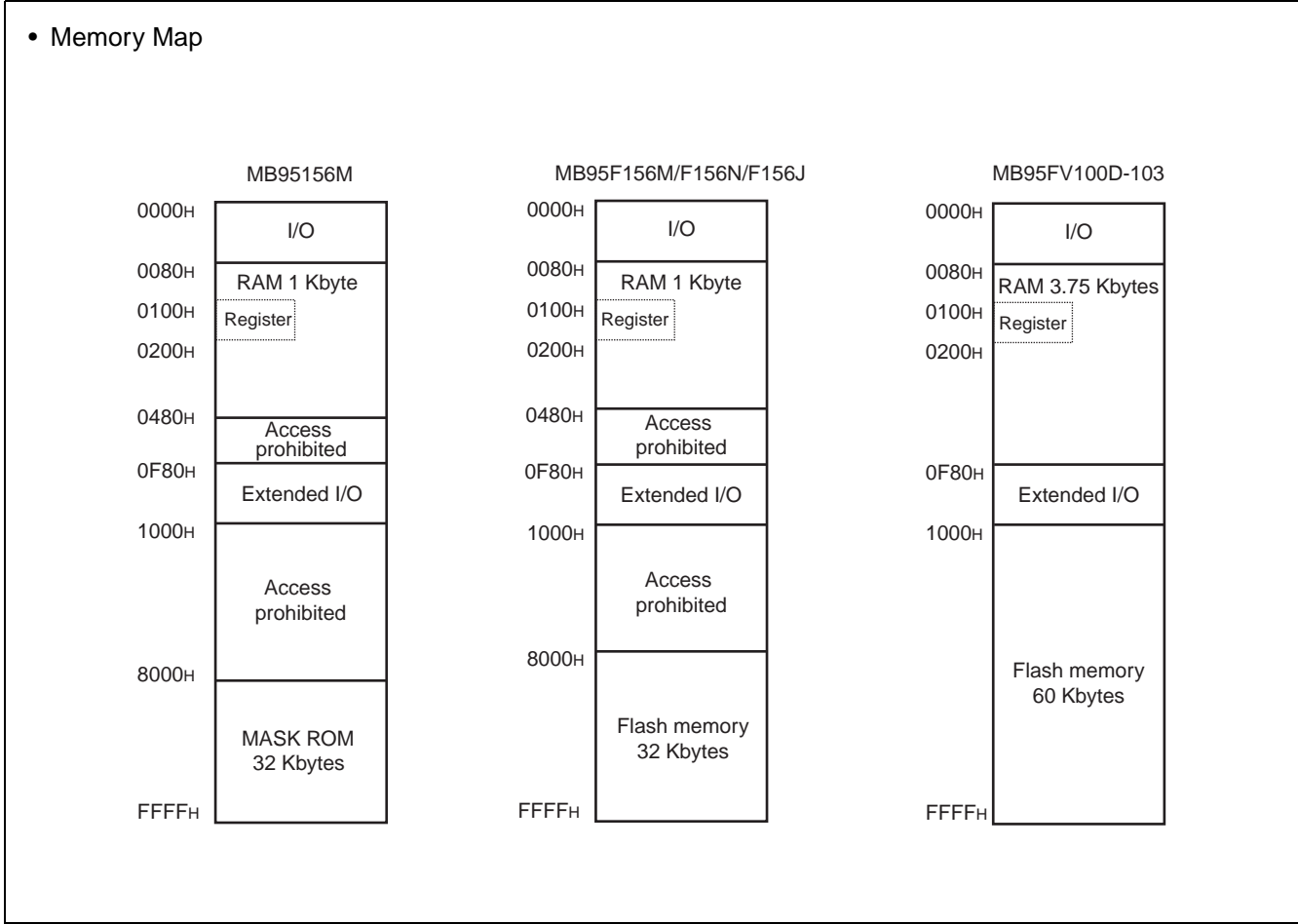
■ BLOCK DIAGRAM



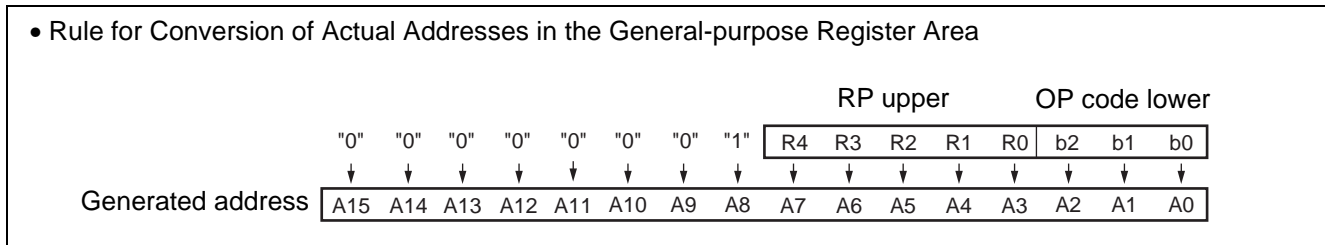
■ CPU CORE

1. Memory space

Memory space of the MB95150M series is 64 Kbytes and consists of I/O area, data area, and program area. The memory space includes special-purpose areas such as the general-purpose registers and vector table. Memory map of the MB95150M series is shown below.



The RP indicates the address of the register bank currently being used. The relationship between the content of RP and the real address conforms to the conversion rule illustrated below:



The DP specifies the area for mapping instructions (16 different instructions such as MOV A, dir) using direct addresses to 0080H to 00FFH.

Direct bank pointer (DP2 to DP0)	Specified address area	Mapping area
XXX _B (no effect to mapping)	0000 _H to 007F _H	0000 _H to 007F _H (without mapping)
000 _B (initial value)	0080 _H to 00FF _H	0080 _H to 00FF _H (without mapping)
001 _B		0100 _H to 017F _H
010 _B		0180 _H to 01FF _H
011 _B		0200 _H to 027F _H
100 _B		0280 _H to 02FF _H
101 _B		0300 _H to 037F _H
110 _B		0380 _H to 03FF _H
111 _B		0400 _H to 047F _H

The CCR consists of the bits indicating arithmetic operation results or transfer data contents and the bits that control CPU operations at interrupt.

- H flag : Set to "1" when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared to "0" otherwise. This flag is for decimal adjustment instructions.
- I flag : Interrupt is enabled when this flag is set to "1". Interrupt is disabled when this flag is set to "0". The flag is set to "0" when reset.
- IL1, IL0 : Indicates the level of the interrupt currently enabled. Processes an interrupt only if its request level is higher than the value indicated by these bits.

IL1	IL0	Interrupt level	Priority
0	0	0	High ↑ ↓ Low (no interruption)
0	1	1	
1	0	2	
1	1	3	

- N flag : Set to "1" if the MSB is set to "1" as the result of an arithmetic operation. Cleared to "0" when the bit is set to "0".
- Z flag : Set to "1" when an arithmetic operation results in "0". Cleared to "0" otherwise.
- V flag : Set to "1" if the complement on 2 overflows as a result of an arithmetic operation. Cleared to "0" otherwise.
- C flag : Set to "1" when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared to "0" otherwise. Set to the shift-out value in the case of a shift instruction.

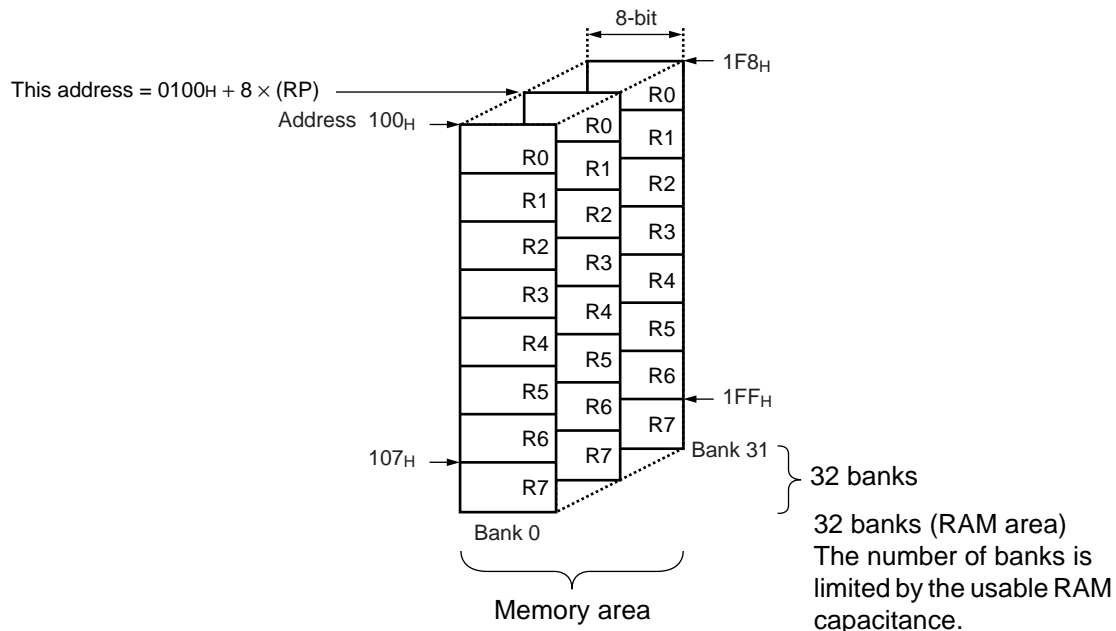
MB95150M Series

The following general-purpose registers are provided:

General-purpose registers: 8-bit data storage registers

The general-purpose registers are 8 bits and located in the register banks on the memory. 1-bank contains 8-register. Up to a total of 32 banks can be used on the MB95150M series. The bank currently in use is specified by the register bank pointer (RP), and the lower 3 bits of OP code indicates the general-purpose register 0 (R0) to general-purpose register 7 (R7).

• Register Bank Configuration



■ I/O MAP

Address	Register abbreviation	Register name	R/W	Initial value
0000 _H	PDR0	Port 0 data register	R/W	00000000 _B
0001 _H	DDR0	Port 0 direction register	R/W	00000000 _B
0002 _H	PDR1	Port 1 data register	R/W	00000000 _B
0003 _H	DDR1	Port 1 direction register	R/W	00000000 _B
0004 _H	—	(Disabled)	—	—
0005 _H	WATR	Oscillation stabilization wait time setting register	R/W	11111111 _B
0006 _H	PLLC	PLL control register	R/W	00000000 _B
0007 _H	SYCC	System clock control register	R/W	1010X011 _B
0008 _H	STBC	Standby control register	R/W	00000000 _B
0009 _H	RSRR	Reset source register	R/W	XXXXXXXX _B
000A _H	TBTC	Time-base timer control register	R/W	00000000 _B
000B _H	WPCR	Watch prescaler control register	R/W	00000000 _B
000C _H	WDTC	Watchdog timer control register	R/W	00000000 _B
000D _H to 0015 _H	—	(Disabled)	—	—
0016 _H	PDR6	Port 6 data register	R/W	00000000 _B
0017 _H	DDR6	Port 6 direction register	R/W	00000000 _B
0018 _H to 001B _H	—	(Disabled)	—	—
001C _H	PDR9	Port 9 data register	R/W	00000000 _B
001D _H	DDR9	Port 9 direction register	R/W	00000000 _B
001E _H	PDRA	Port A data register	R/W	00000000 _B
001F _H	DDRA	Port A direction register	R/W	00000000 _B
0020 _H	PDRB	Port B data register	R/W	00000000 _B
0021 _H	DDRB	Port B direction register	R/W	00000000 _B
0022 _H to 002B _H	—	(Disabled)	—	—
002C _H	PUL0	Port 0 pull-up register	R/W	00000000 _B
002D _H	PUL1	Port 1 pull-up register	R/W	00000000 _B
002E _H to 0035 _H	—	(Disabled)	—	—

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MB95150M Series

Address	Register abbreviation	Register name	R/W	Initial value
0036 _H	T01CR1	8/16-bit compound timer 01 control status register 1 ch.0	R/W	00000000 _B
0037 _H	T00CR1	8/16-bit compound timer 00 control status register 1 ch.0	R/W	00000000 _B
0038 _H	T11CR1	8/16-bit compound timer 11 control status register 1 ch.1	R/W	00000000 _B
0039 _H	T10CR1	8/16-bit compound timer 10 control status register 1 ch.1	R/W	00000000 _B
003A _H	PC01	8/16-bit PPG1 control register ch.0	R/W	00000000 _B
003B _H	PC00	8/16-bit PPG0 control register ch.0	R/W	00000000 _B
003C _H	PC11	8/16-bit PPG1 control register ch.1	R/W	00000000 _B
003D _H	PC10	8/16-bit PPG0 control register ch.1	R/W	00000000 _B
003E _H to 0041 _H	—	(Disabled)	—	—
0042 _H	PCNTH0	16-bit PPG status control register (upper byte) ch.0	R/W	00000000 _B
0043 _H	PCNTL0	16-bit PPG status control register (lower byte) ch.0	R/W	00000000 _B
0044 _H to 0047 _H	—	(Disabled)	—	—
0048 _H	EIC00	External interrupt circuit control register ch.0/ch.1	R/W	00000000 _B
0049 _H	EIC10	External interrupt circuit control register ch.2/ch.3	R/W	00000000 _B
004A _H	EIC20	External interrupt circuit control register ch.4/ch.5	R/W	00000000 _B
004B _H	EIC30	External interrupt circuit control register ch.6/ch.7	R/W	00000000 _B
004C _H to 004F _H	—	(Disabled)	—	—
0050 _H	SCR	LIN-UART serial control register	R/W	00000000 _B
0051 _H	SMR	LIN-UART serial mode register	R/W	00000000 _B
0052 _H	SSR	LIN-UART serial status register	R/W	00001000 _B
0053 _H	RDR/TDR	LIN-UART reception/transmission data register	R/W	00000000 _B
0054 _H	ESCR	LIN-UART extended status control register	R/W	00000100 _B
0055 _H	ECCR	LIN-UART extended communication control register	R/W	000000XX _B
0056 _H	SMC10	UART/SIO serial mode control register 1 ch.0	R/W	00000000 _B
0057 _H	SMC20	UART/SIO serial mode control register 2 ch.0	R/W	00100000 _B
0058 _H	SSR0	UART/SIO serial status register ch.0	R/W	00000001 _B
0059 _H	TDR0	UART/SIO serial output data register ch.0	R/W	00000000 _B
005A _H	RDR0	UART/SIO serial input data register ch.0	R	00000000 _B
005B _H to 006B _H	—	(Disabled)	—	—

(Continued)

MB95150M Series

Address	Register abbreviation	Register name	R/W	Initial value
006C _H	ADC1	8/10-bit A/D converter control register 1	R/W	00000000 _B
006D _H	ADC2	8/10-bit A/D converter control register 2	R/W	00000000 _B
006E _H	ADDH	8/10-bit A/D converter data register (Upper byte)	R/W	00000000 _B
006F _H	ADDL	8/10-bit A/D converter data register (Lower byte)	R/W	00000000 _B
0070 _H	WCSR	Watch counter status register	R/W	00000000 _B
0071 _H	—	(Disabled)	—	—
0072 _H	FSR	Flash memory status register	R/W	000X0000 _B
0073 _H	SWRE0	Flash memory sector writing control register 0	R/W	00000000 _B
0074 _H	SWRE1	Flash memory sector writing control register 1	R/W	00000000 _B
0075 _H	—	(Disabled)	—	—
0076 _H	WREN	Wild register address compare enable register	R/W	00000000 _B
0077 _H	WROR	Wild register data test setting register	R/W	00000000 _B
0078 _H	—	Register bank pointer (RP) , Mirror of direct bank pointer (P)	—	—
0079 _H	ILR0	Interrupt level setting register 0	R/W	11111111 _B
007A _H	ILR1	Interrupt level setting register 1	R/W	11111111 _B
007B _H	ILR2	Interrupt level setting register 2	R/W	11111111 _B
007C _H	ILR3	Interrupt level setting register 3	R/W	11111111 _B
007D _H	ILR4	Interrupt level setting register 4	R/W	11111111 _B
007E _H	ILR5	Interrupt level setting register 5	R/W	11111111 _B
007F _H	—	(Disabled)	—	—
0F80 _H	WRARH0	Wild register address setting register (upper byte) ch.0	R/W	00000000 _B
0F81 _H	WRARL0	Wild register address setting register (lower byte) ch.0	R/W	00000000 _B
0F82 _H	WRDR0	Wild register data setting register ch.0	R/W	00000000 _B
0F83 _H	WRARH1	Wild register address setting register (upper byte) ch.1	R/W	00000000 _B
0F84 _H	WRARL1	Wild register address setting register (lower byte) ch.1	R/W	00000000 _B
0F85 _H	WRDR1	Wild register data setting register ch.1	R/W	00000000 _B
0F86 _H	WRARH2	Wild register address setting register (upper byte) ch.2	R/W	00000000 _B
0F87 _H	WRARL2	Wild register address setting register (lower byte) ch.2	R/W	00000000 _B
0F88 _H	WRDR2	Wild register data setting register ch.2	R/W	00000000 _B
0F89 _H to 0F91 _H	—	(Disabled)	—	—
0F92 _H	T01CR0	8/16-bit compound timer 01 control status register 0 ch.0	R/W	00000000 _B
0F93 _H	T00CR0	8/16-bit compound timer 00 control status register 0 ch.0	R/W	00000000 _B
0F94 _H	T01DR	8/16-bit compound timer 01 data register ch.0	R/W	00000000 _B

(Continued)

MB95150M Series

Address	Register abbreviation	Register name	R/W	Initial value
0F95 _H	T00DR	8/16-bit compound timer 00 data register ch.0	R/W	0000000 _B
0F96 _H	TMCR0	8/16-bit compound timer 00/01 timer mode control register ch.0	R/W	0000000 _B
0F97 _H	T11CR0	8/16-bit compound timer 11 control status register 0 ch.1	R/W	0000000 _B
0F98 _H	T10CR0	8/16-bit compound timer 10 control status register 0 ch.1	R/W	0000000 _B
0F99 _H	T11DR	8/16-bit compound timer 11 data register ch.1	R/W	0000000 _B
0F9A _H	T10DR	8/16-bit compound timer 10 data register ch.1	R/W	0000000 _B
0F9B _H	TMCR1	8/16-bit compound timer 10/11 timer mode control register ch.1	R/W	0000000 _B
0F9C _H	PPS01	8/16-bit PPG1 cycle setting buffer register ch.0	R/W	1111111 _B
0F9D _H	PPS00	8/16-bit PPG0 cycle setting buffer register ch.0	R/W	1111111 _B
0F9E _H	PDS01	8/16-bit PPG1 duty setting buffer register ch.0	R/W	1111111 _B
0F9F _H	PDS00	8/16-bit PPG0 duty setting buffer register ch.0	R/W	1111111 _B
0FA0 _H	PPS11	8/16-bit PPG1 cycle setting buffer register ch.1	R/W	1111111 _B
0FA1 _H	PPS10	8/16-bit PPG0 cycle setting buffer register ch.1	R/W	1111111 _B
0FA2 _H	PDS11	8/16-bit PPG1 duty setting buffer register ch.1	R/W	1111111 _B
0FA3 _H	PDS10	8/16-bit PPG0 duty setting buffer register ch.1	R/W	1111111 _B
0FA4 _H	PPGS	8/16-bit PPG start register	R/W	0000000 _B
0FA5 _H	REVC	8/16-bit PPG output inversion register	R/W	0000000 _B
0FA6 _H to 0FA9 _H	—	(Disabled)	—	—
0FAA _H	PDCRH0	16-bit PPG down counter register (upper byte) ch.0	R	0000000 _B
0FAB _H	PDCRL0	16-bit PPG down counter register (lower byte) ch.0	R	0000000 _B
0FAC _H	PCSRH0	16-bit PPG cycle setting buffer register (upper byte) ch.0	R/W	1111111 _B
0FAD _H	PCSRL0	16-bit PPG cycle setting buffer register (lower byte) ch.0	R/W	1111111 _B
0FAE _H	PDUTH0	16-bit PPG duty setting buffer register (upper byte) ch.0	R/W	1111111 _B
0FAF _H	PDUTL0	16-bit PPG duty setting buffer register (lower byte) ch.0	R/W	1111111 _B
0FB0 _H to 0FBB _H	—	(Disabled)	—	—
0FBC _H	BGR1	LIN-UART baud rate generator register 1	R/W	0000000 _B
0FBD _H	BGR0	LIN-UART baud rate generator register 0	R/W	0000000 _B
0FBE _H	PSSR0	UART/SIO dedicated baud rate generator prescaler selection register ch.0	R/W	0000000 _B
0FBF _H	BRSR0	UART/SIO dedicated baud rate generator baud rate setting register ch.0	R/W	0000000 _B
0FC0 _H to 0FC2 _H	—	(Disabled)	—	—

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Address	Register abbreviation	Register name	R/W	Initial value
0FC3 _H	AIDRL	A/D input disable register (lower byte)	R/W	00000000 _B
0FC4 _H	LCDCC	LCDC control register	R/W	00010000 _B
0FC5 _H	LCDCE1	LCDC enable register 1	R/W	00110000 _B
0FC6 _H	LCDCE2	LCDC enable register 2	R/W	00000000 _B
0FC7 _H	LCDCE3	LCDC enable register 3	R/W	00000000 _B
0FC8 _H to 0FCA _H	—	(Disabled)	—	—
0FCB _H	LCDCB1	LCDC blinking setting register 1	R/W	00000000 _B
0FCC _H	LCDCB2	LCDC blinking setting register 2	R/W	00000000 _B
0FCD _H to 0FD4 _H	LCDRAM	LCDC display RAM	R/W	00000000 _B
0FD5 _H to 0FE2 _H	—	(Disabled)	—	—
0FE3 _H	WCDR	Watch counter data register	R/W	00111111 _B
0FE4 _H to 0FE6 _H	—	(Disabled)	—	—
0FE7 _H	ILSR2	Input level select register 2	R/W	00000000 _B
0FE8 _H , 0FE9 _H	—	(Disabled)	—	—
0FEA _H	CSVCR	Clock supervisor control register	R/W	00011100 _B
0FEB _H to 0FED _H	—	(Disabled)	—	—
0FEE _H	ILSR	Input level select register	R/W	00000000 _B
0FEF _H	WICR	Interrupt pin control register	R/W	01000000 _B
0FF0 _H to 0FFF _H	—	(Disabled)	—	—

- R/W access symbols

R/W : Readable/Writable

R : Read only

W : Write only

- Initial value symbols

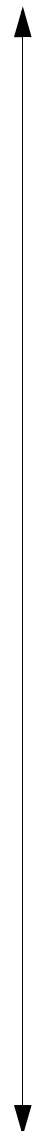
0 : The initial value of this bit is "0".

1 : The initial value of this bit is "1".

X : The initial value of this bit is undefined.

MB95150M Series

■ INTERRUPT SOURCE TABLE

Interrupt source	Interrupt request number	Vector table address		Bit name of interrupt level setting register	Same level priority order (at simultaneous occurrence)
		Upper	Lower		
External interrupt ch.0	IRQ0	FFFA _H	FFFB _H	L00 [1 : 0]	High  Low
External interrupt ch.4					
External interrupt ch.1	IRQ1	FFF8 _H	FFF9 _H	L01 [1 : 0]	
External interrupt ch.5					
External interrupt ch.2	IRQ2	FFF6 _H	FFF7 _H	L02 [1 : 0]	
External interrupt ch.6					
External interrupt ch.3	IRQ3	FFF4 _H	FFF5 _H	L03 [1 : 0]	
External interrupt ch.7					
UART/SIO ch.0	IRQ4	FFF2 _H	FFF3 _H	L04 [1 : 0]	
8/16-bit compound timer ch.0 (Lower)	IRQ5	FFF0 _H	FFF1 _H	L05 [1 : 0]	
8/16-bit compound timer ch.0 (Upper)	IRQ6	FFEE _H	FFEF _H	L06 [1 : 0]	
LIN-UART (reception)	IRQ7	FFEC _H	FFED _H	L07 [1 : 0]	
LIN-UART (transmission)	IRQ8	FFEA _H	FFEB _H	L08 [1 : 0]	
8/16-bit PPG ch.1 (Lower)	IRQ9	FFE8 _H	FFE9 _H	L09 [1 : 0]	
8/16-bit PPG ch.1 (Upper)	IRQ10	FFE6 _H	FFE7 _H	L10 [1 : 0]	
(Unused)	IRQ11	FFE4 _H	FFE5 _H	L11 [1 : 0]	
8/16-bit PPG ch.0 (Upper)	IRQ12	FFE2 _H	FFE3 _H	L12 [1 : 0]	
8/16-bit PPG ch.0 (Lower)	IRQ13	FFE0 _H	FFE1 _H	L13 [1 : 0]	
8/16-bit compound timer ch.1 (Upper)	IRQ14	FFDE _H	FFDF _H	L14 [1 : 0]	
16-bit PPG ch.0	IRQ15	FFDC _H	FFDD _H	L15 [1 : 0]	
(Unused)	IRQ16	FFDA _H	FFDB _H	L16 [1 : 0]	
(Unused)	IRQ17	FFD8 _H	FFD9 _H	L17 [1 : 0]	
8/10-bit A/D converter	IRQ18	FFD6 _H	FFD7 _H	L18 [1 : 0]	
Time-base timer	IRQ19	FFD4 _H	FFD5 _H	L19 [1 : 0]	
Watch prescaler/Watch counter	IRQ20	FFD2 _H	FFD3 _H	L20 [1 : 0]	
(Unused)	IRQ21	FFD0 _H	FFD1 _H	L21 [1 : 0]	
8/16-bit compound timer ch.1 (Lower)	IRQ22	FFCE _H	FFCF _H	L22 [1 : 0]	
Flash memory	IRQ23	FFCC _H	FFCD _H	L23 [1 : 0]	

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V _{CC}	V _{SS} – 0.3	V _{SS} + 6.0	V	
Power supply voltage for LCD	V ₀ to V ₃	V _{SS} – 0.3	V _{SS} + 6.0	V	*2
Input voltage*1	V _I	V _{SS} – 0.3	V _{SS} + 6.0	V	*3
Output voltage*1	V _O	V _{SS} – 0.3	V _{SS} + 6.0	V	*3
Maximum clamp current	I _{CLAMP}	– 2.0	+ 2.0	mA	Applicable to pins*4
Total maximum clamp current	Σ I _{CLAMP}	—	20	mA	Applicable to pins*4
“L” level maximum output current	I _{OL}	—	15	mA	Applicable to pins*4
“L” level average current	I _{OLAV}	—	4	mA	Applicable to pins*4 Average output current = operating current × operating ratio (1 pin)
“L” level total maximum output current	ΣI _{OL}	—	100	mA	
“L” level total average output current	ΣI _{OLAV}	—	50	mA	Total average output current = operating current × operating ratio (Total of pins)
“H” level maximum output current	I _{OH}	—	– 15	mA	Applicable to pins*4
“H” level average current	I _{OHAV}	—	– 4	mA	Applicable to pins*4 Average output current = operating current × operating ratio (1 pin)
“H” level total maximum output current	ΣI _{OH}	—	– 100	mA	
“H” level total average output current	ΣI _{OHAV}	—	– 50	mA	Total average output current = operating current × operating ratio (Total of pins)
Power consumption	P _d	—	320	mW	
Operating temperature	T _A	– 40	+ 85	°C	
Storage temperature	T _{stg}	– 55	+ 150	°C	

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MB95150M Series

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*1 : The parameter is based on $V_{SS} = 0.0 \text{ V}$.

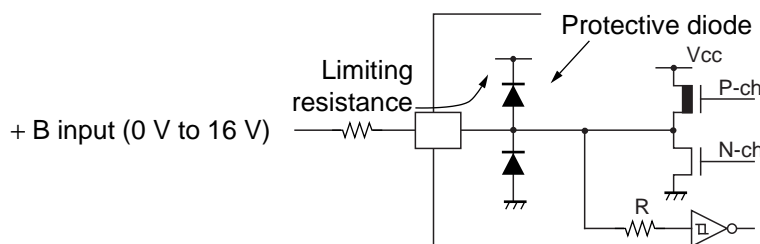
*2 : V_0 to V_3 should not exceed $V_{CC} + 0.3 \text{ V}$.

*3 : V_I and V_O should not exceed $V_{CC} + 0.3 \text{ V}$. V_I must not exceed the rating voltage. However, if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

*4 : Applicable to pins : P00 to P07, P10 to P14, P60 to P67, P90 to P95, PA0 to PA3, PB0 to PB7

- Use within recommended operating conditions.
- Use at DC voltage (current).
- +B signal is an input signal that exceeds V_{CC} voltage. The + B signal should always be applied a limiting resistance placed between the + B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the + B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this affects other devices.
- Note that if the + B signal is inputted when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the + B input is applied during power-on, the power supply is provided from the pins and the resulting power supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the + B input pin open.
- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, etc.) cannot accept + B signal input.
- Sample recommended circuits :

- Input/Output Equivalent circuits



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(V_{SS} = 0.0 V)

Parameter	Symbol	Conditions	Value		Unit	Remarks	
			Min	Max			
Power supply voltage	V _{CC}	—	2.4*1,*2	5.5*1	V	In normal operating	Other than MB95FV100D-103
			2.3	5.5		Hold condition in STOP mode	
			2.7	5.5		In normal operating	MB95FV100D-103
			2.3	5.5		Hold condition in STOP mode	
Power supply voltage for LCD	V ₀ to V ₃	—	V _{SS}	V _{CC}	V	The range of liquid crystal power supply (The optimal value depends on liquid crystal display elements used.)	
Smoothing capacitor	C _s	—	0.1	1.0	μF	*3	
Operating temperature	T _A	—	-40	+85	°C	Other than MB95FV100D-103	
			+5	+35	°C	MB95FV100D-103	

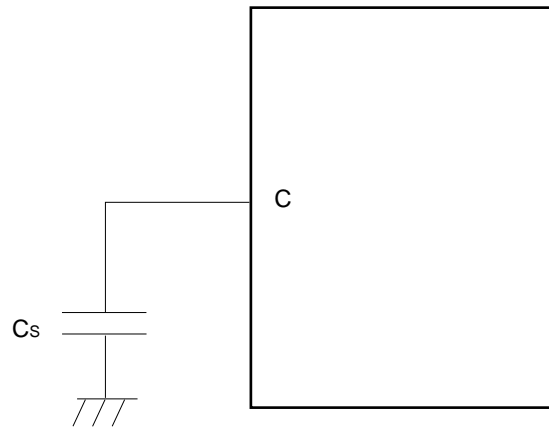
*1 : The values vary with the operating frequency, machine clock or analog guarantee range.

*2 : When the low voltage detection reset is used, reset occurs while the low voltage is detected. For details on Low voltage detection, see "(8) Low Voltage Detection" in "4. AC Characteristics".

*3 : Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. A bypass capacitor of V_{CC} pin must have a capacitance value higher than C_s. For connection of smoothing capacitor C_s, refer to the diagram below.

MB95150M Series

- C pin connection diagram



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

MB95150M Series

3. DC Characteristics

($V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH1}	P10, P67	*1	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	When selecting CMOS input level
	V_{IHA}	P00 to P07, P10 to P14, P60 to P67, P90 to P95, PA0 to PA3, PB0 to PB7	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	Pin input at selecting of automotive input level
	V_{IHS1}	PA0 to PA3, PB0 to PB7	*1	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	Hysteresis input
	V_{IHM}	\overline{RST} , MOD	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	Hysteresis input
"L" level input voltage	V_{IL}	P10, P67	*1	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	When selecting CMOS input level (Hysteresis input)
	V_{ILA}	P00 to P07, P10 to P14, P60 to P67, P90 to P95, PA0 to PA3, PB0 to PB7	—	$V_{SS} - 0.3$	—	$0.5 V_{CC}$	V	Pin input at selecting of automotive input level
	V_{ILS}	PA0 to PA3, PB0 to PB7	*1	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	Hysteresis input
	V_{ILM}	\overline{RST} , MOD	—	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	Hysteresis input
"H" level output voltage	V_{OH}	All output pins	$I_{OH} = -4.0\text{ mA}$	$V_{CC} - 0.5$	—	—	V	
"L" level output voltage	V_{OL}	All output pins, \overline{RST}^{*2}	$I_{OL} = 4.0\text{ mA}$	—	—	0.4	V	
Input leak current (Hi-Z output leak current)	I_{LI}	Port other than P00 to P07, P10 to P14	$0.0\text{ V} < V_i < V_{CC}$	-5	—	+5	μA	When specifying without pull-up resistance
Pull-up resistance	R_{PULL}	P00 to P07, P10 to P14	$V_i = 0.0\text{ V}$	25	50	100	k Ω	When specifying with pull-up resistance
Pull-down resistance	R_{MOD}	MOD	$V_i = V_{CC}$	50	100	200	k Ω	MASK ROM product only

(Continued)

MB95150M Series

(V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, T_A = - 40 °C to + 85 °C)

Parameter	Sym- bol	Pin name	Conditions	Value			Unit	Remarks		
				Min	Typ	Max				
Power supply current*3	I _{CC}	V _{CC} (External clock operation)	V _{CC} = 5.5 V, F _{CH} = 20 MHz, F _{MP} = 10 MHz Main clock mode (divided by 2)	—	9.5	12.5	mA	Flash memory product (at other than Flash memory writing and erasing)		
				—	30	35	mA	Flash memory product (at Flash memory writing and erasing)		
				—	11.9	17.2	mA	Flash memory product (When A/D conversion)		
				—	7.2	9.5	mA	MASK ROM product		
				—	9.6	14.2	mA	MASK ROM product (When A/D conversion)		
			V _{CC} (External clock operation)	Main clock mode (divided by 2)	—	15.2	20.0	mA	Flash memory product (at other than Flash memory writing and erasing)	
					—	35.7	42.5	mA	Flash memory product (at Flash memory writing and erasing)	
					—	19.0	27.5	mA	Flash memory product (When A/D conversion)	
			I _{CCS}	V _{CC} (External clock operation)	Main sleep mode (divided by 2)	—	11.6	15.2	mA	MASK ROM product
						—	15.4	22.7	mA	MASK ROM product (When A/D conversion)
	I _{CCS}	V _{CC} (External clock operation)	Main sleep mode (divided by 2)	V _{CC} = 5.5 V, F _{CH} = 20 MHz, F _{MP} = 10 MHz	—	4.5	7.5	mA		
				V _{CC} = 5.5 V, F _{CH} = 32 MHz, F _{MP} = 16 MHz	—	7.2	12.0	mA		
I _{CCL}	V _{CC} (External clock operation)	Sub clock mode (divided by 2), T _A = + 25 °C	—	45	100	μA				

(Continued)

MB95150M Series

($V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*3	I _{CCLS}	V _{CC} (External clock operation)	V _{CC} = 5.5 V, F _{CL} = 32 kHz, F _{MPL} = 16 kHz Sub sleep mode (divided by 2), T _A = +25 °C	—	10	81	μA	
	I _{CCCT}		V _{CC} = 5.5 V, F _{CL} = 32 kHz Watch mode, Main stop mode T _A = +25 °C	—	4.6	27.0	μA	
	I _{CCMPLL}		V _{CC} = 5.5 V, F _{CH} = 4 MHz, F _{MP} = 10 MHz Main PLL mode (multiplied by 2.5)	—	9.3	12.5	mA	Flash memory product
				—	7.0	9.5	mA	MASK ROM product
			V _{CC} = 5.5 V, F _{CH} = 6.4 MHz, F _{MP} = 16 MHz Main PLL mode (multiplied by 2.5)	—	14.9	20.0	mA	Flash memory product
				—	11.2	15.2	mA	MASK ROM product
	I _{CCSPLL}		V _{CC} = 5.5 V, F _{CL} = 32 kHz, F _{MPL} = 128 kHz Sub PLL mode (multiplied by 4) T _A = +25 °C	—	160	400	μA	
	I _{CTS}		V _{CC} = 5.5 V, F _{CH} = 10 MHz Time-base timer mode T _A = +25 °C	—	0.40	1.10	mA	
I _{CCH}	V _{CC} = 5.5 V, Sub stop mode T _A = +25 °C	—	3.5	20	μA			
LCD division resistance	R _{LCD}	—	Between V ₃ and V _{SS}	—	300	—	kΩ	
COM0 to COM3 output impedance	R _{VCOM}	COM0 to COM3	V ₁ to V ₃ = 5.0V	—	—	5	kΩ	
SEG00 to SEG15 output impedance	R _{VSEG}	SEG00 to SEG15		—	—	7	kΩ	

(Continued)

MB95150M Series

(Continued)

(V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, T_A = -40 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
LCD leak current	I _{LCDL}	V0 to V3 COM0 to COM3 SEG00 to SEG15	—	-1	—	+1	μA	
Input capacitance	C _{IN}	Other than V _{CC} , V _{SS}	f = 1 MHz	—	5	15	pF	

*1 : P10 and P67 can switch the input level to either the “CMOS input level” or “hysteresis input level”.
The switching of the input level can be set by the input level selection register (ILSR) .

*2 : Product without clock supervisor only

*3 : • The power-supply current is determined by the external clock. When both low voltage detection option and clock supervisor are selected, the power-supply current will be a value of adding current consumption of the low voltage detection circuit (I_{LVD}) and current consumption of built-in CR oscillator (I_{CSV}) to the specified value.

- Refer to “4. AC Characteristics (1) Clock Timing” for F_{CH} and F_{CL}.
- Refer to “4. AC Characteristics (2) Source Clock/Machine Clock” for F_{MPL} and F_{MPL}.

4. AC Characteristics

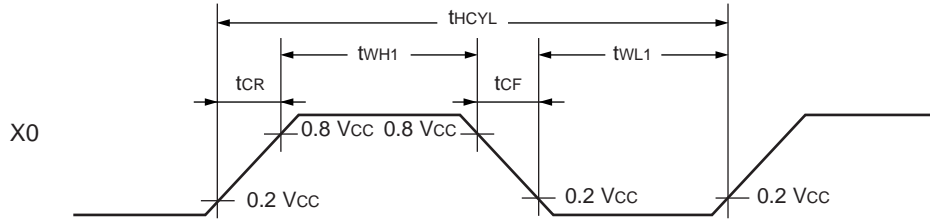
(1) Clock Timing

(V_{CC} = 2.4 V to 5.5 V, V_{SS} = 0.0 V, T_A = -40 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F _{CH}	X0, X1	—	1.00	—	16.25	MHz	When using main oscillation circuit
				1.00	—	32.50	MHz	When using external clock
				3.00	—	10.00	MHz	Main PLL multiplied by 1
				3.00	—	8.13	MHz	Main PLL multiplied by 2
				3.00	—	6.50	MHz	Main PLL multiplied by 2.5
				3.00	—	4.06	MHz	Main PLL multiplied by 4
	F _{CL}	X0A, X1A		—	32.768	—	kHz	When using sub oscillation circuit
	—	—		—	32.768	—	kHz	When using sub PLL
Clock cycle time	t _{H CYL}	X0, X1	61.5	—	1000	ns	When using oscillation circuit	
	t _{L CYL}	X0A, X1A	30.8	—	1000	ns	When using external clock	
			—	30.5	—	μs	When using sub clock	
Input clock pulse width	t _{WH1} t _{WL1}	X0	61.5	—	—	ns	When using external clock Duty ratio is about 30% to 70%.	
	t _{WH2} t _{WL2}	X0A	—	15.2	—	μs		
Input clock rise time and fall time	t _{CR} t _{CF}	X0, X0A	—	—	5	ns	When using external clock	

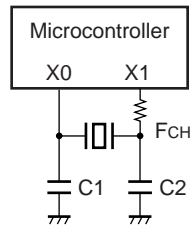
MB95150M Series

- Input wave form for using external clock (main clock)

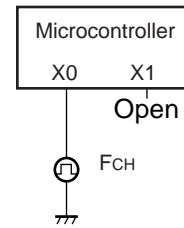


- Figure of main clock input port external connection

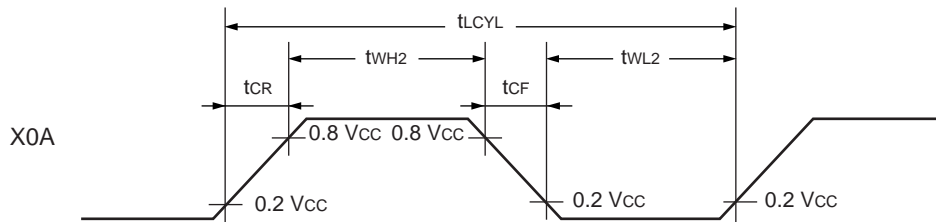
When using a crystal or ceramic oscillator



When using external clock

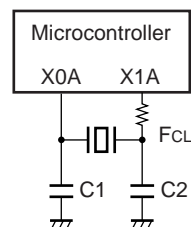


- Input wave form for using external clock (sub clock)

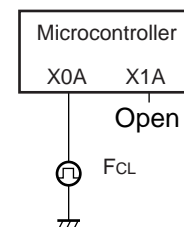


- Figure of sub clock input port external connection

When using a crystal or ceramic oscillator



When using external clock



(2) Source Clock/Machine Clock

($V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$)

Parameter	Sym- bol	Pin name	Condi- tions	Value			Unit	Remarks
				Min	Typ	Max		
Source clock cycle time* ¹ (Clock before setting division)	t _{SCLK}	—	—	61.5	—	2000	ns	When using main clock Min : F _{CH} = 8.125 MHz, PLL multiplied by 2 Max : F _{CH} = 1 MHz, divided by 2
				7.6	—	61.0	μs	When using sub clock Min : F _{CL} = 32 kHz, PLL multiplied by 4 Max : F _{CL} = 32 kHz, divided by 2
Source clock frequency	F _{SP}	—	—	0.50	—	16.25	MHz	When using main clock
	F _{SPL}	—		16.384	—	131.072	kHz	When using sub clock
Machine clock cycle time* ² (Minimum instruction execution time)	t _{MCLK}	—	—	61.5	—	32000	ns	When using main clock Min : F _{SP} = 16.25 MHz, no division Max : F _{SP} = 0.5 MHz, divided by 16
				7.6	—	976.5	μs	When using sub clock Min : F _{SPL} = 131 kHz, no division Max : F _{SPL} = 16 kHz, divided by 16
Machine clock frequency	F _{MP}	—	—	0.031	—	16.250	MHz	When using main clock
	F _{MPL}	—		1.024	—	131.072	kHz	When using sub clock

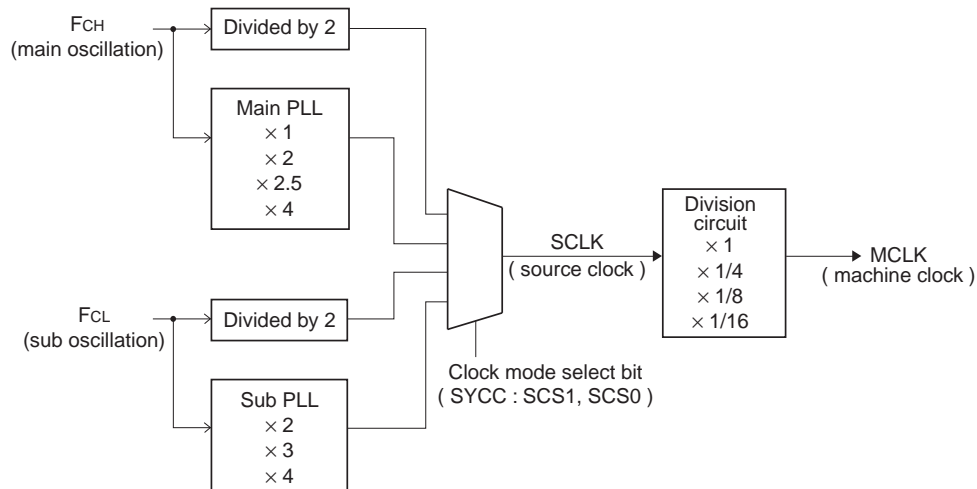
*1 : Clock before setting division due to machine clock division ratio selection bit (SYCC : DIV1 and DIV0) . This source clock is divided by the machine clock division ratio selection bit (SYCC : DIV1 and DIV0) , and it becomes the machine clock. Further, the source clock can be selected as follows.

- Main clock divided by 2
- PLL multiplication of main clock (select from 1, 2, 2.5, 4 multiplication)
- Sub clock divided by 2
- PLL multiplication of sub clock (select from 2, 3, 4 multiplication)

*2 : Operation clock of the microcontroller. Machine clock can be selected as follows.

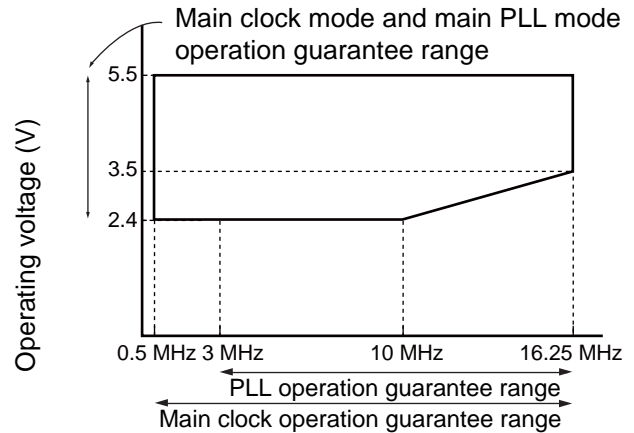
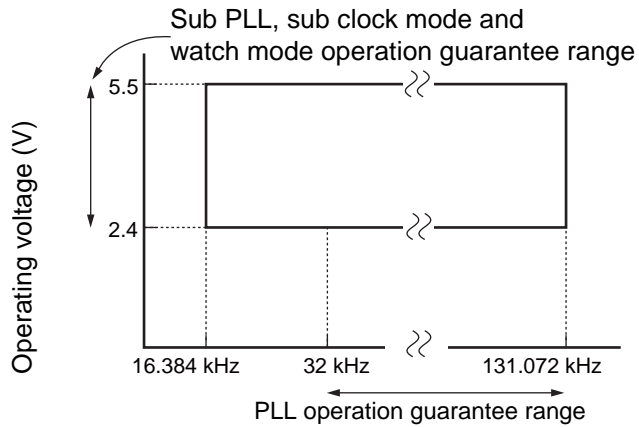
- Source clock (no division)
- Source clock divided by 4
- Source clock divided by 8
- Source clock divided by 16

• Outline of clock generation block

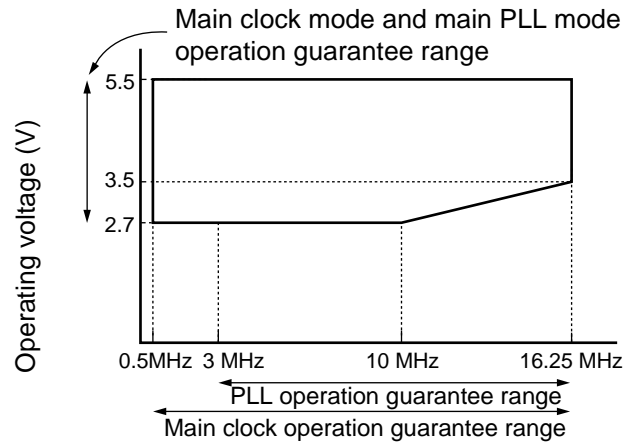
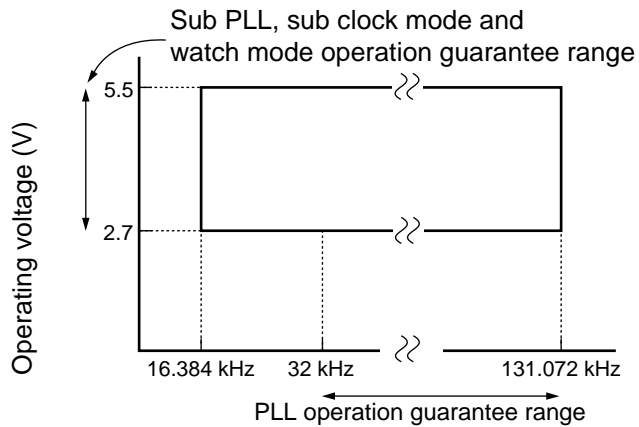


MB95150M Series

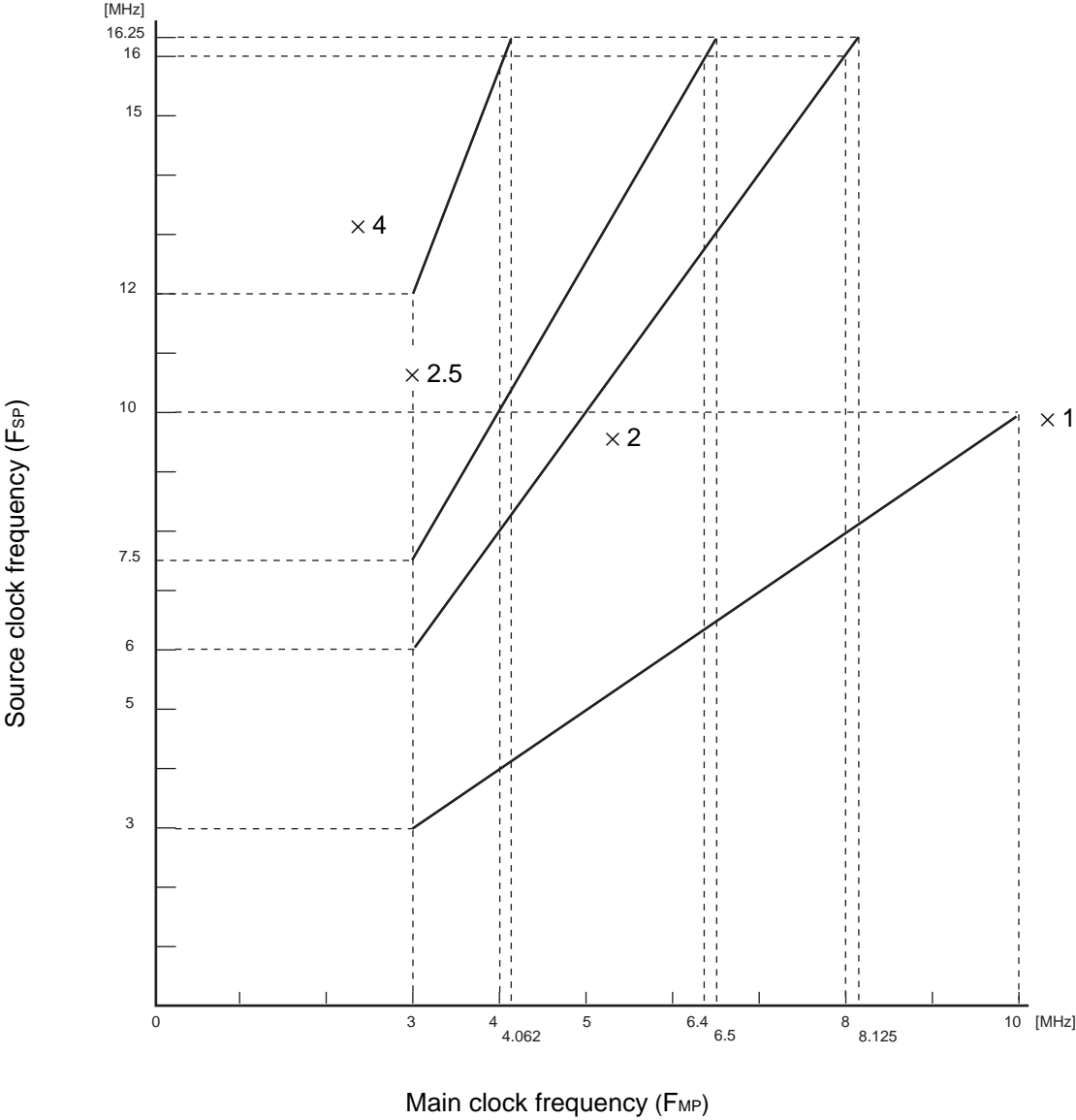
- Operating voltage - Operating frequency (When $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$)
 - MB95156M/F156M/F156N/F156J



- Operating voltage - Operating frequency (When $T_A = +5\text{ }^\circ\text{C}$ to $+35\text{ }^\circ\text{C}$)
 - MB95FV100D-103



• Main PLL operation frequency



MB95150M Series

(3) External Reset

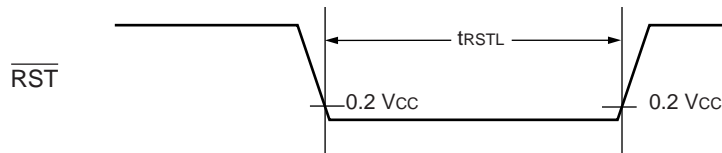
($V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
$\overline{\text{RST}}$ "L" level pulse width	t_{RSTL}	$\overline{\text{RST}}$	—	$2 t_{\text{MCLK}}^{*1}$	—	ns	At normal operating
				Oscillation time of oscillator ^{*2} + 100	—	μs	At stop mode, sub clock mode, sub sleep mode, and watch mode
				100	—	μs	At time-base timer mode

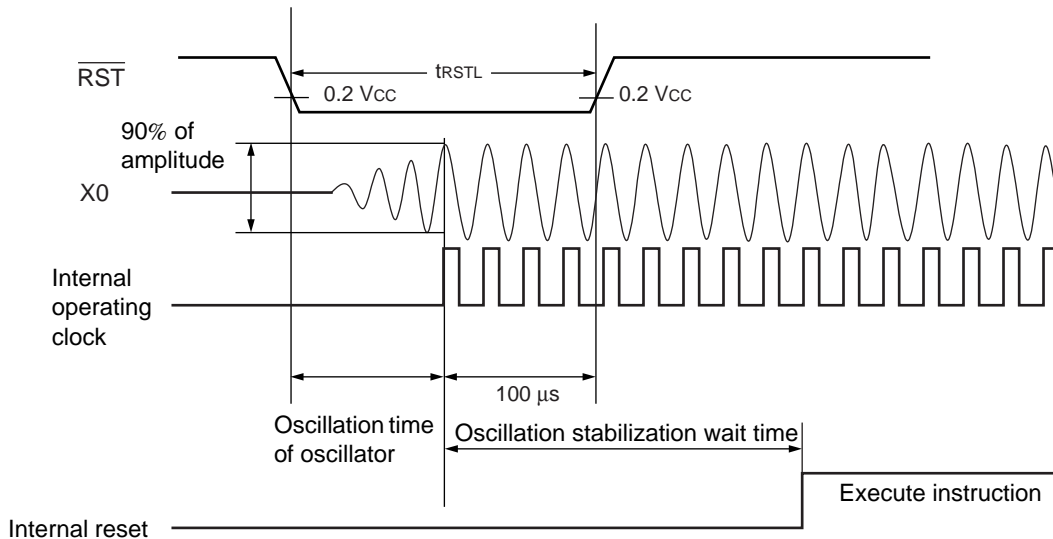
*1 : Refer to "(2) Source Clock/Machine Clock" for t_{MCLK} .

*2 : Oscillation time of oscillator is the time that the amplitude reaches 90 %. In the crystal oscillator, the oscillation time is between several ms and tens of ms. In ceramic oscillators, the oscillation time is between hundreds of μs and several ms. In the external clock, the oscillation time is 0 ms.

- At normal operating



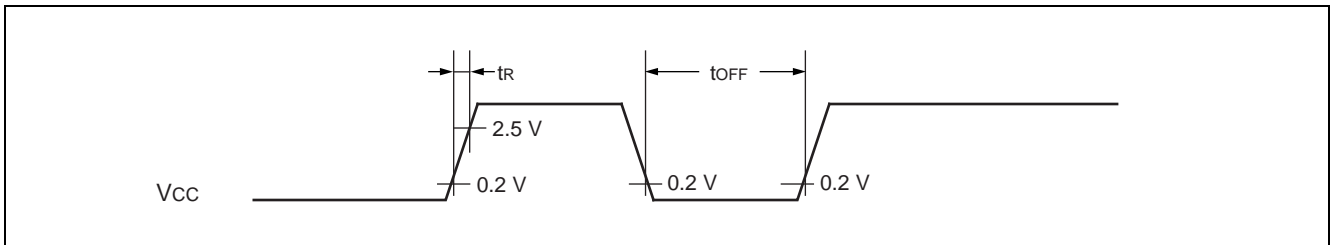
- At stop mode, sub clock mode, sub sleep mode, watch mode, and power-on



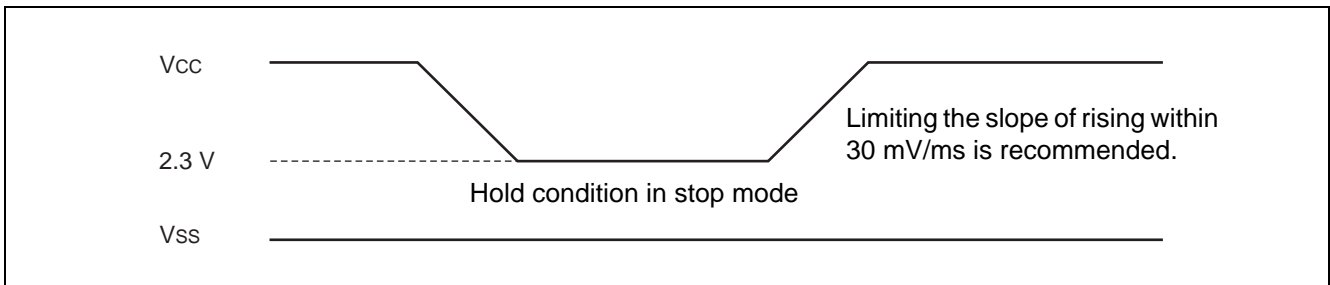
(4) Power-on Reset

(V_{SS} = 0.0 V, T_A = -40 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Power supply rising time	t _R	V _{CC}	—	—	50	ms	
Power supply cutoff time	t _{OFF}			1	—	ms	Waiting time until power-on



Note : Sudden change of power supply voltage may activate the power-on reset function. When changing power supply voltages during operation, set the slope of rising within 30 mV/ms as shown below.



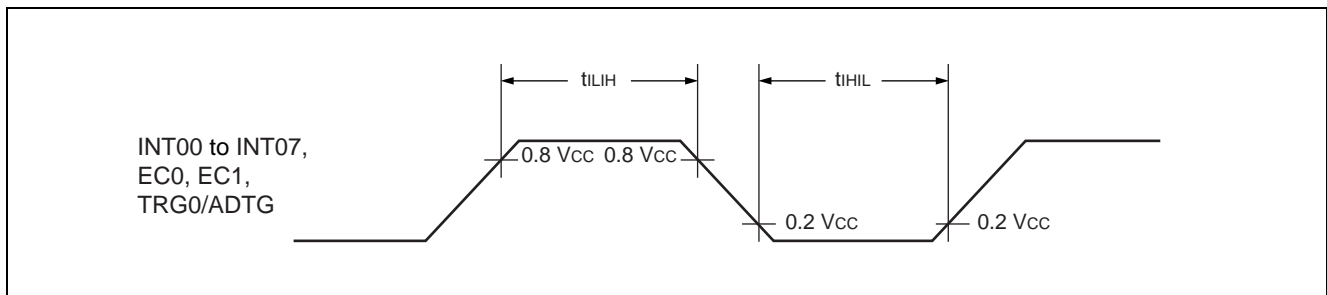
MB95150M Series

(5) Peripheral Input Timing

($V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Peripheral input "H" pulse width	t_{LIH}	INT00 to INT07, EC0, EC1, TRG0/ADTG	—	$2 t_{MCLK}^*$	—	ns
Peripheral input "L" pulse width	t_{LIL}			$2 t_{MCLK}^*$	—	ns

* : Refer to "(2) Source Clock/Machine Clock" for t_{MCLK} .



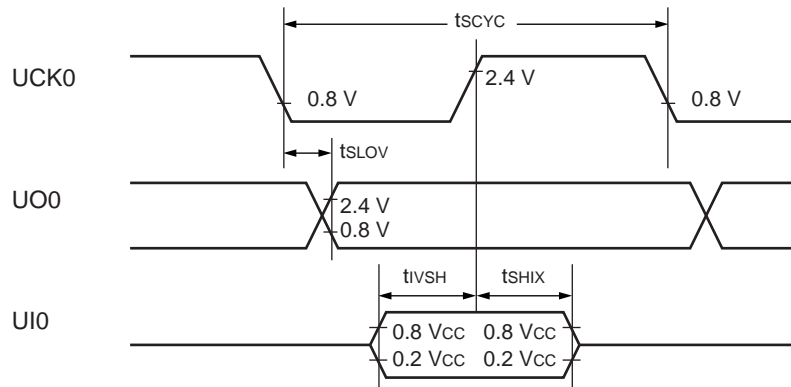
(6) UART/SIO, Serial I/O Timing

($V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$)

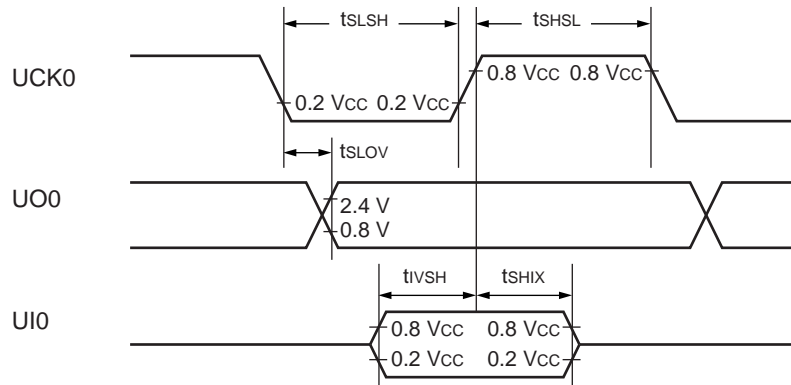
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	UCK0	Internal clock operation Output pin : $C_L = 80\text{ pF}$ $+ 1\text{ TTL}$.	$4 t_{MCLK}^*$	—	ns
UCK ↓ → UO time	t_{SLOV}	UCK0, UO0		- 190	+ 190	ns
Valid UI → UCK ↑	t_{IVSH}	UCK0, UI0		$2 t_{MCLK}^*$	—	ns
UCK ↑ → valid UI hold time	t_{SHIX}	UCK0, UI0		$2 t_{MCLK}^*$	—	ns
Serial clock "H" pulse width	t_{SHSL}	UCK0	External clock operation Output pin : $C_L = 80\text{ pF}$ $+ 1\text{ TTL}$.	$4 t_{MCLK}^*$	—	ns
Serial clock "L" pulse width	t_{SLSH}	UCK0		$4 t_{MCLK}^*$	—	ns
UCK ↓ → UO time	t_{SLOV}	UCK0, UO0		—	190	ns
Valid UI → UCK ↑	t_{IVSH}	UCK0, UI0		$2 t_{MCLK}^*$	—	ns
UCK ↑ → valid UI hold time	t_{SHIX}	UCK0, UI0	$2 t_{MCLK}^*$	—	ns	

* : Refer to "(2) Source Clock/Machine Clock" for t_{MCLK} .

• Internal shift clock mode



• External shift clock mode



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(7) LIN-UART Timing

Sampling at the rising edge of sampling clock*1 and prohibited serial clock delay*2
(ESCR register : SCES bit = 0, ECCR register : SCDE bit = 0)

(V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, T_A = -40 °C to + 85 °C)

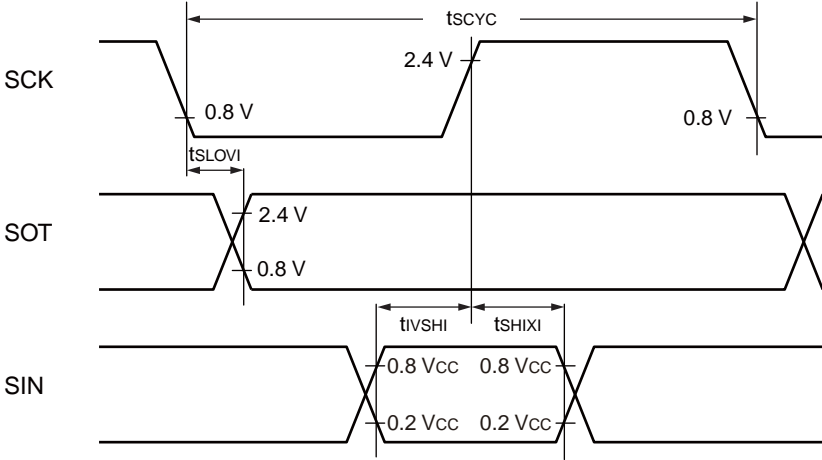
Parameter	Sym- bol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t _{SCYC}	SCK	Internal clock operation output pin : C _L = 80 pF + 1 TTL.	5 t _{MCLK} *3	—	ns
SCK ↓ → SOT delay time	t _{SLOVI}	SCK, SOT		-95	+ 95	ns
Valid SIN → SCK ↑	t _{IVSHI}	SCK, SIN		t _{MCLK} *3 + 190	—	ns
SCK ↑ → valid SIN hold time	t _{SHIXI}	SCK, SIN		0	—	ns
Serial clock "L" pulse width	t _{SLSH}	SCK	External clock operation output pin : C _L = 80 pF + 1 TTL.	3 t _{MCLK} *3 - t _R	—	ns
Serial clock "H" pulse width	t _{SHSL}	SCK		t _{MCLK} *3 + 95	—	ns
SCK ↓ → SOT delay time	t _{SLOVE}	SCK, SOT		—	2 t _{MCLK} *3 + 95	ns
Valid SIN → SCK ↑	t _{IVSHE}	SCK, SIN		190	—	ns
SCK ↑ → valid SIN hold time	t _{SHIXE}	SCK, SIN		t _{MCLK} *3 + 95	—	ns
SCK fall time	t _F	SCK		—	10	ns
SCK rise time	t _R	SCK		—	10	ns

*1 : Provide switch function whether sampling of reception data is performed at rising edge or falling edge of the serial clock.

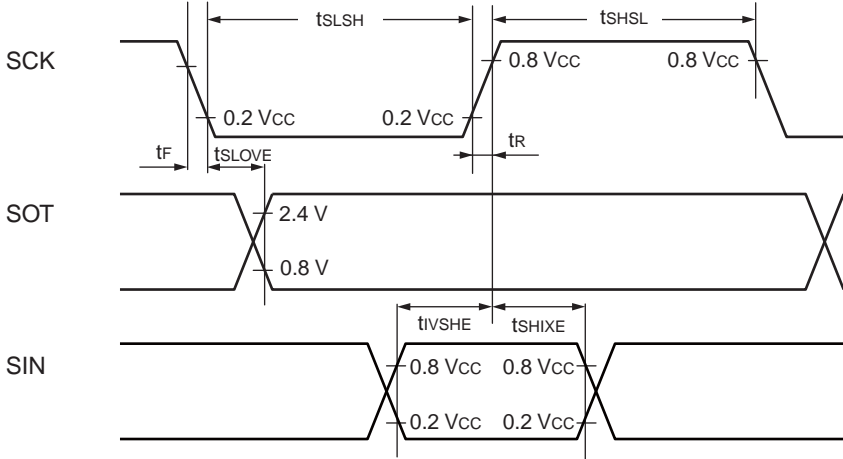
*2 : Serial clock delay function is used to delay half clock for the output signal of serial clock.

*3 : Refer to " (2) Source Clock/Machine Clock" for t_{MCLK}.

- Internal shift clock mode



- External shift clock mode



MB95150M Series

Sampling at the falling edge of sampling clock*1 and prohibited serial clock delay*2
(ESCR register : SCES bit = 1, ECCR register : SCDE bit = 0)

(V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, T_A = -40 °C to +85 °C)

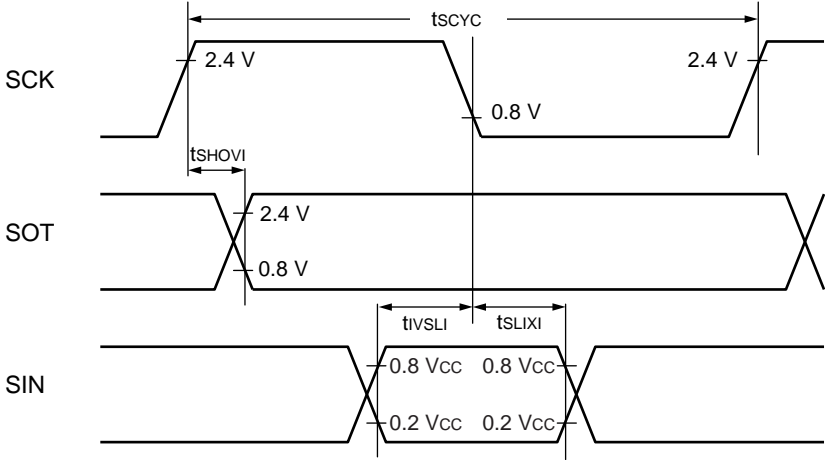
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t _{SCYC}	SCK	Internal clock operation output pin : C _L = 80 pF + 1 TTL.	5 t _{MCLK} *3	—	ns
SCK↑→SOT delay time	t _{SHOVI}	SCK, SOT		-95	+95	ns
Valid SIN→SCK↓	t _{IVSLI}	SCK, SIN		t _{MCLK} *3 + 190	—	ns
SCK↓→valid SIN hold time	t _{SLIXI}	SCK, SIN		0	—	ns
Serial clock "H" pulse width	t _{SHSL}	SCK	External clock operation output pin : C _L = 80 pF + 1 TTL.	3 t _{MCLK} *3 - t _R	—	ns
Serial clock "L" pulse width	t _{SLSH}	SCK		t _{MCLK} *3 + 95	—	ns
SCK↑→SOT delay time	t _{SHOVE}	SCK, SOT		—	2 t _{MCLK} *3 + 95	ns
Valid SIN→SCK↓	t _{IVSLE}	SCK, SIN		190	—	ns
SCK↓→valid SIN hold time	t _{SLIXE}	SCK, SIN		t _{MCLK} *3 + 95	—	ns
SCK fall time	t _F	SCK		—	10	ns
SCK rise time	t _R	SCK		—	10	ns

*1 : Provide switch function whether sampling of reception data is performed at rising edge or falling edge of the serial clock.

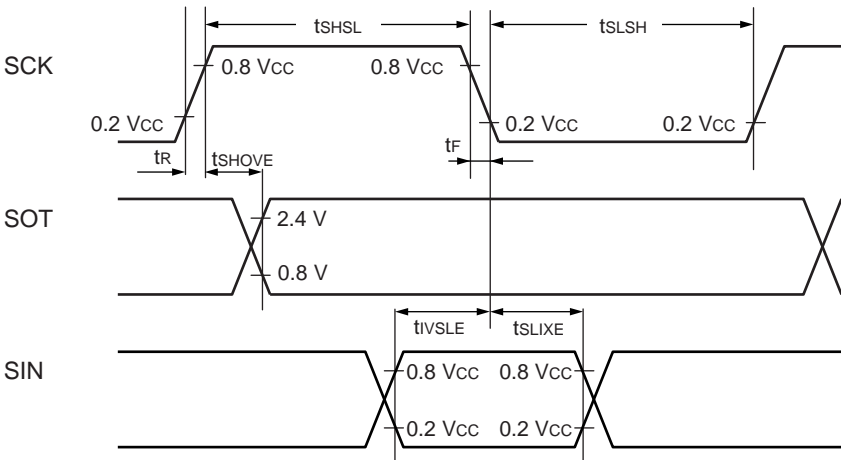
*2 : Serial clock delay function is used to delay half clock for the output signal of serial clock.

*3 : Refer to “ (2) Source Clock/Machine Clock” for t_{MCLK}.

- Internal shift clock mode



- External shift clock mode



MB95150M Series

Sampling at the rising edge of sampling clock*¹ and enabled serial clock delay*²
 (ESCR register : SCES bit = 0, ECCR register : SCDE bit = 1)

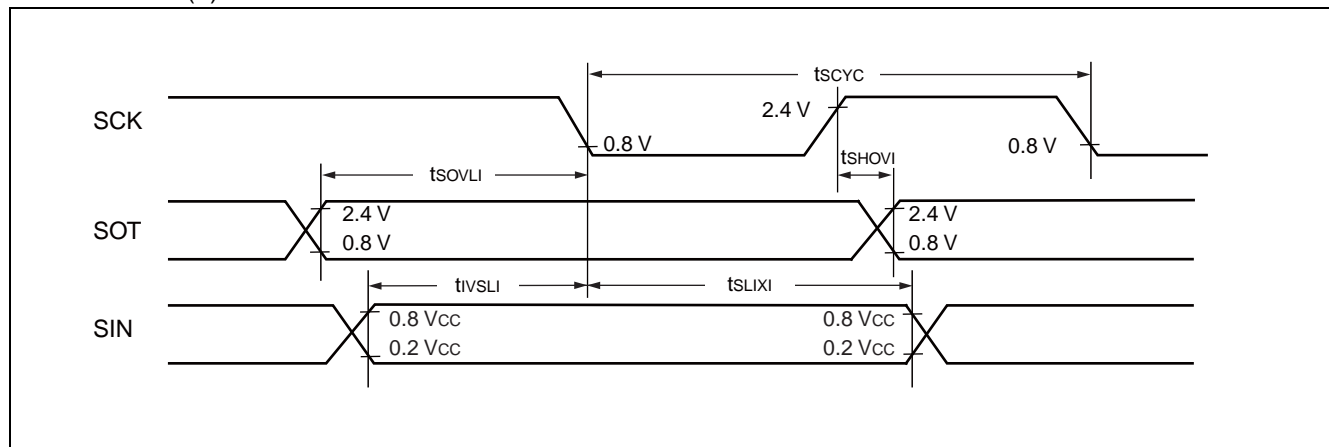
($V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin : $C_L = 80\text{ pF} + 1\text{ TTL}$.	$5 t_{MCLK}^{*3}$	—	ns
SCK \uparrow → SOT delay time	t_{SHOVI}	SCK, SOT		-95	+95	ns
Valid SIN→SCK \downarrow	t_{IVSLI}	SCK, SIN		$t_{MCLK}^{*3} + 190$	—	ns
SCK \downarrow → valid SIN hold time	t_{SLIXI}	SCK, SIN		0	—	ns
SOT→SCK \downarrow delay time	t_{SOVLI}	SCK, SOT		—	$4 t_{MCLK}^{*3}$	ns

*1 : Provide switch function whether sampling of reception data is performed at rising edge or falling edge of the serial clock.

*2 : Serial clock delay function is used to delay half clock for the output signal of serial clock.

*3 : Refer to “ (2) Source Clock/Machine Clock” for t_{MCLK} .



**Sampling at the falling edge of sampling clock*1 and enabled serial clock delay*2
(ESCR register : SCES bit = 1, ECCR register : SCDE bit = 1)**

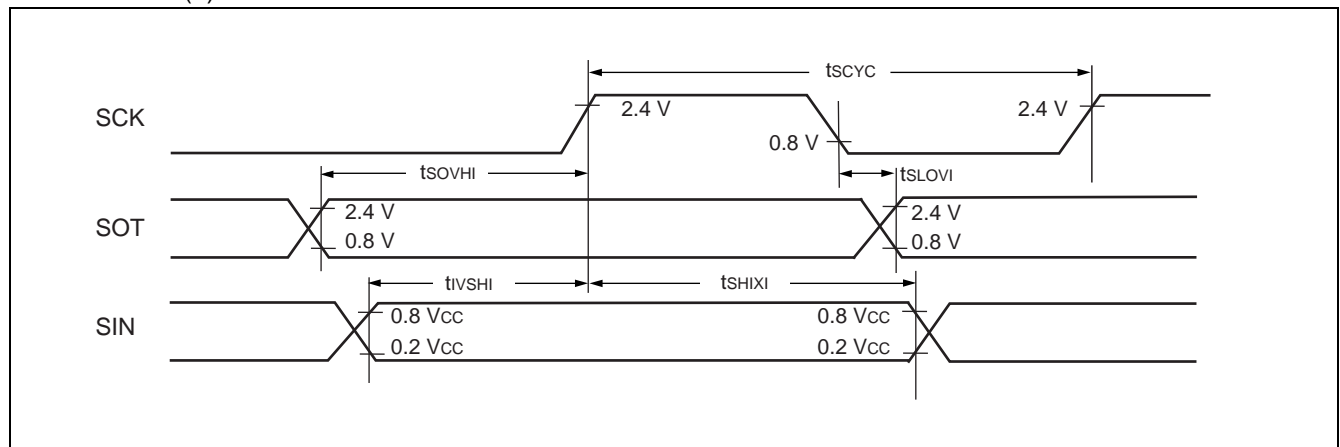
($V_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^\circ\text{C}$ to $+85 \text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin : $C_L = 80 \text{ pF} + 1 \text{ TTL.}$	$5 t_{MCLK}^{*3}$	—	ns
SCK↓→SOT delay time	t_{SLOVI}	SCK, SOT		-95	+95	ns
Valid SIN→SCK↑	t_{VSHI}	SCK, SIN		$t_{MCLK}^{*3} + 190$	—	ns
SCK↑ → valid SIN hold time	t_{SHIXI}	SCK, SIN		0	—	ns
SOT→SCK↑ delay time	t_{SOVHI}	SCK, SOT		—	$4 t_{MCLK}^{*3}$	ns

*1 : Provide switch function whether sampling of reception data is performed at rising edge or falling edge of the serial clock.

*2 : Serial clock delay function is used to delay half clock for the output signal of serial clock.

*3 : Refer to “ (2) Source Clock/Machine Clock” for t_{MCLK} .

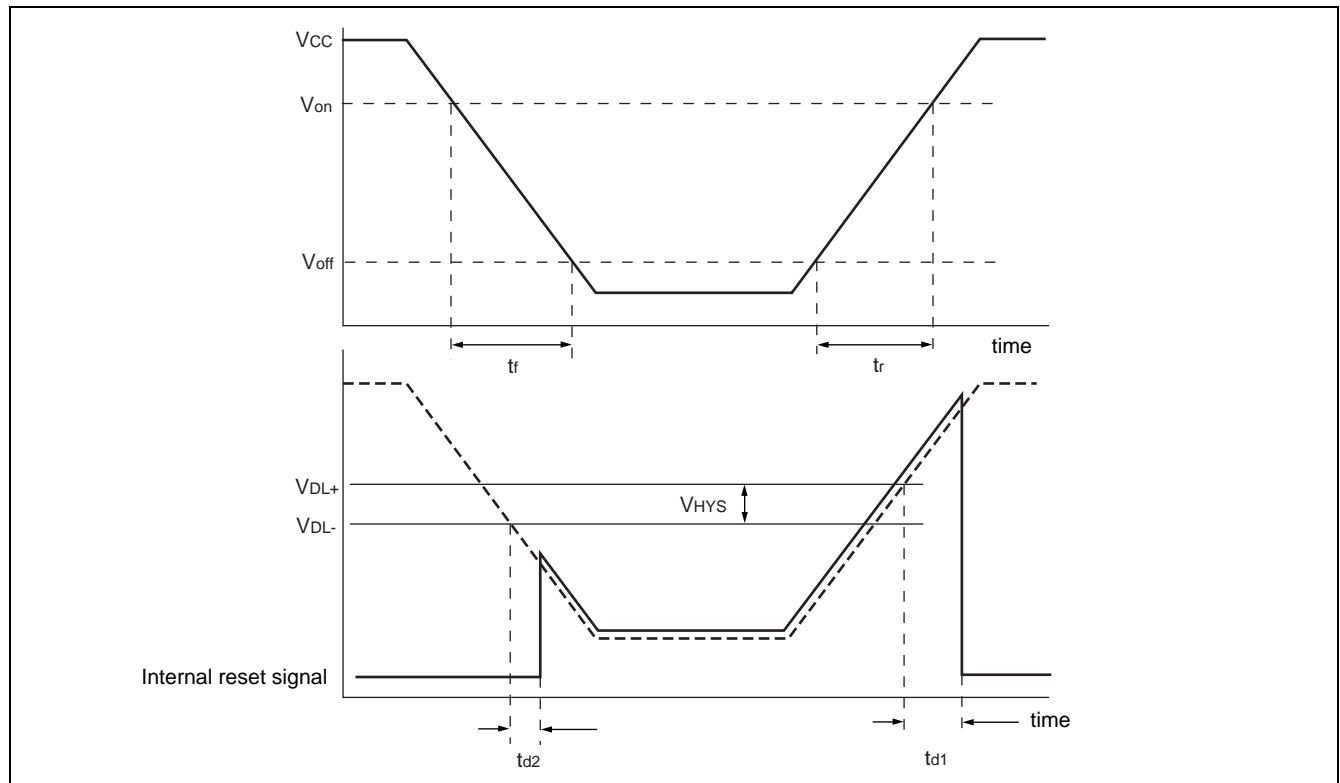


MB95150M Series

(8) Low Voltage Detection

(V_{SS} = 0.0 V, T_A = -40 °C to +85 °C)

Parameter	Symbol	Condi- tions	Value			Unit	Remarks
			Min	Typ	Max		
Release voltage	V _{DL+}	—	2.52	2.70	2.88	V	At power-supply rise
Detection voltage	V _{DL-}		2.42	2.60	2.78	V	At power-supply fall
Hysteresis width	V _{HYS}		70	100	—	mV	
Power-supply start voltage	V _{off}		—	—	2.3	V	
Power-supply end voltage	V _{on}		4.9	—	—	V	
Power-supply voltage change time (at power supply rise)	t _r		0.3	—	—	μs	Slope of power supply that reset release signal generates
			—	3000	—	μs	Slope of power supply that reset release signal generates within rating (V _{DL+})
Power-supply voltage change time (at power supply fall)	t _r		300	—	—	μs	Slope of power supply that reset detection signal generates
			—	300	—	μs	Slope of power supply that reset detection signal generates within rating (V _{DL-})
Reset release delay time	t _{d1}		—	—	400	μs	
Reset detection delay time	t _{d2}		—	—	30	μs	
Current consumption	I _{LVD}		—	38	50	μA	Current consumption of low voltage detection circuit only



(9) Clock Supervisor Clock

($V_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^\circ\text{C}$ to $+85 \text{ }^\circ\text{C}$)

Parameter	Symbol	Condi- tions	Value			Unit	Remarks
			Min	Typ	Max		
Oscillation frequency	f_{OUT}	—	50	100	200	kHz	
Oscillation start time	t_{wk}		—	—	10	μs	
Current consumption	I_{CSV}		—	20	36	μA	Current consumption of built-in CR oscillator, at 100 kHz oscillation

MB95150M Series

5. A/D Converter

(1) A/D Converter Electrical Characteristics

($V_{CC} = 4.0\text{ V to }5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$)

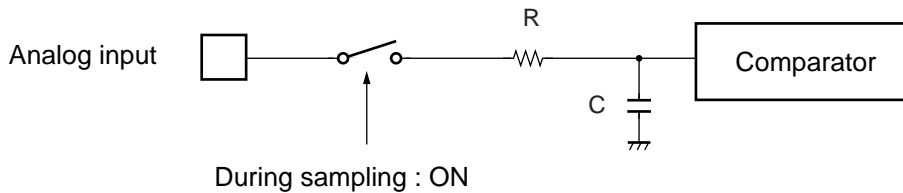
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	10	bit	
Total error		-3.0	—	+3.0	LSB	
Linearity error		-2.5	—	+2.5	LSB	
Differential linear error		-1.9	—	+1.9	LSB	
Zero transition voltage	V_{OT}	$V_{SS} - 1.5\text{ LSB}$	$V_{SS} + 0.5\text{ LSB}$	$V_{SS} + 2.5\text{ LSB}$	V	
Full-scale transition voltage	V_{FST}	$V_{CC} - 3.5\text{ LSB}$	$V_{CC} - 1.5\text{ LSB}$	$V_{CC} + 0.5\text{ LSB}$	V	
Compare time	—	0.9	—	16500	μs	$4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$
		1.8	—	16500	μs	$4.0\text{ V} \leq V_{CC} < 4.5\text{ V}$
Sampling time	—	0.6	—	∞	μs	$4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$, At external impedance < 5.4 k Ω
		1.2	—	∞	μs	$4.0\text{ V} \leq V_{CC} < 4.5\text{ V}$, At external impedance < 2.4 k Ω
Analog input current	I_{AIN}	-0.3	—	+0.3	μA	
Analog input voltage	V_{AIN}	V_{SS}	—	V_{CC}	V	

(2) Notes on Using A/D Converter

• About the external impedance of analog input and its sampling time

A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. Also, if the sampling time cannot be sufficient, connect a capacitor of about 0.1 μF to the analog input pin.

• Analog input equivalent circuit

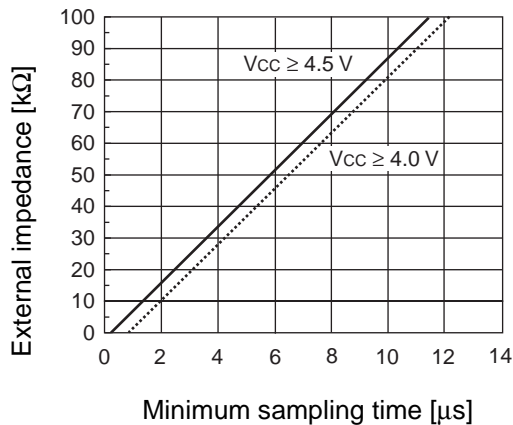


	R	C
$4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$	2.0 k Ω (Max)	16 pF (Max)
$4.0\text{ V} \leq V_{CC} < 4.5\text{ V}$	8.2 k Ω (Max)	16 pF (Max)

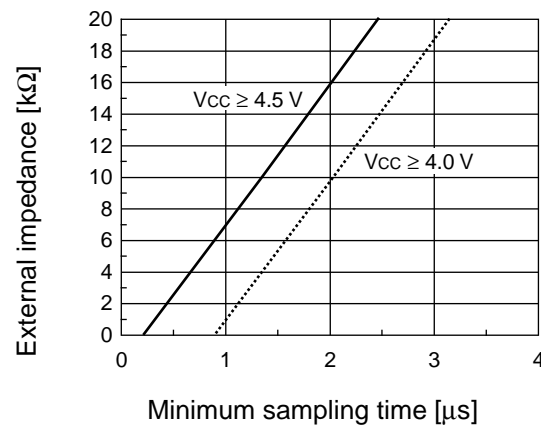
Note : The values are reference values.

• The relationship between external impedance and minimum sampling time

(External impedance = 0 k Ω to 100 k Ω)



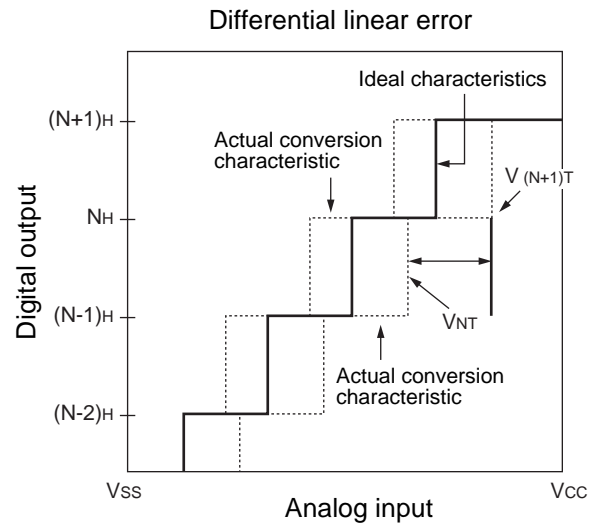
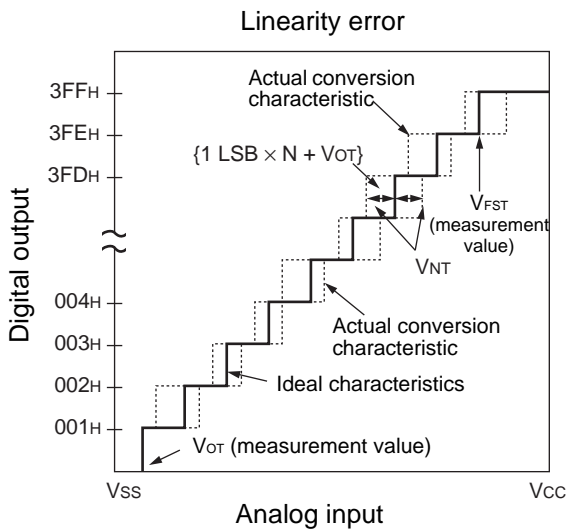
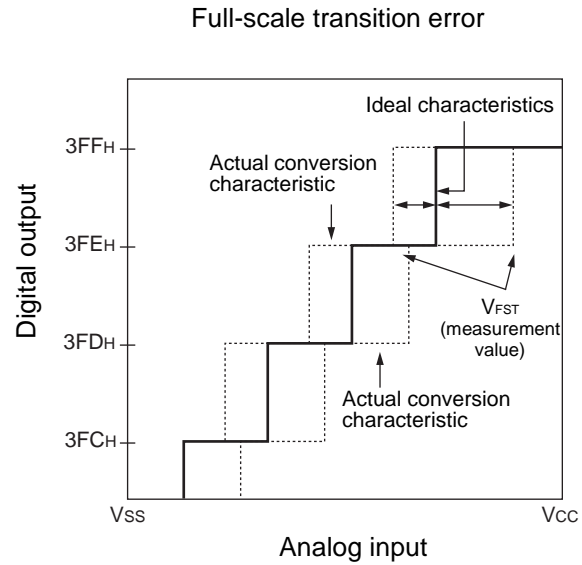
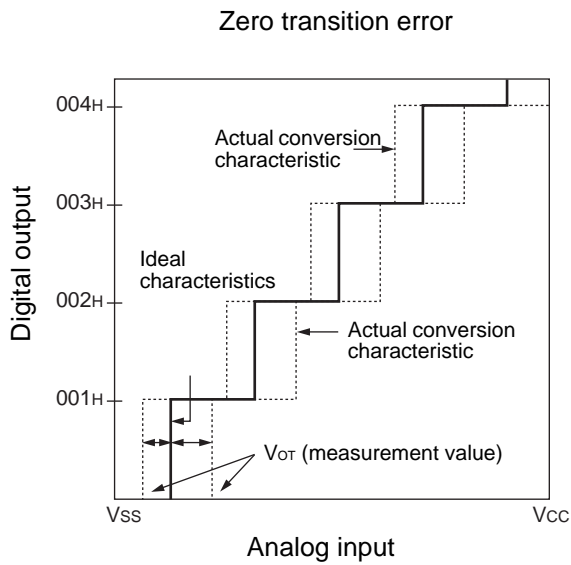
(External impedance = 0 k Ω to 20 k Ω)



• About errors

As $|V_{CC} - V_{SS}|$ becomes smaller, values of relative errors grow larger.

(Continued)



$$\text{Linearity error in digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times N + V_{OT}\}}{1 \text{ LSB}}$$

$$\text{Differential linear error in digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}} - 1$$

N : A/D converter digital output value

V_{NT} : A voltage at which digital output transits from (N - 1)_H to N_H

V_{OT} (Ideal value) = $V_{SS} + 0.5 \text{ LSB [V]}$

V_{FST} (Ideal value) = $V_{CC} - 1.5 \text{ LSB [V]}$

MB95150M Series

6. Flash Memory Program/Erase Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Chip erase time	—	1.0* ¹	15.0* ²	s	Excludes 00 _H programming prior erasure.
Byte programming time	—	32	3600	μs	Excludes system-level overhead.
Erase/program cycle	10000	—	—	cycle	
Power supply voltage at erase/program	4.5	—	5.5	V	
Flash memory data retention time	20* ³	—	—	year	Average T _A = +85 °C

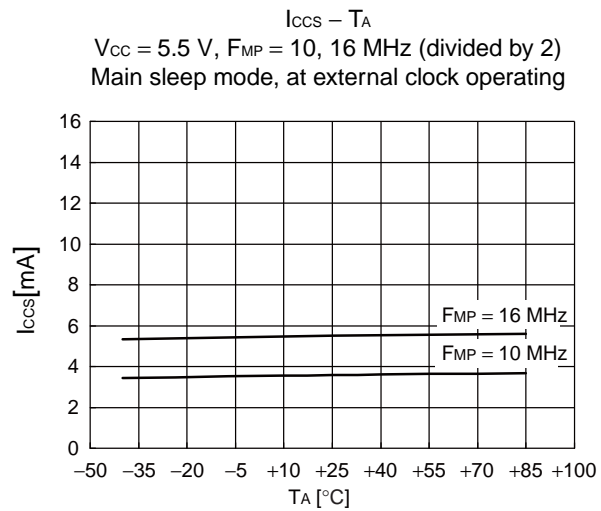
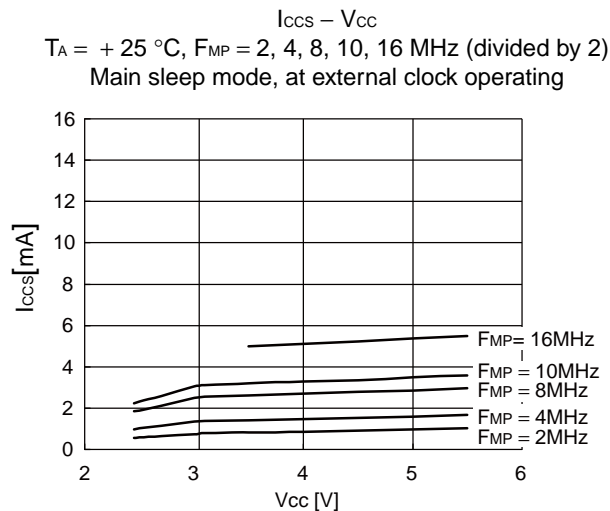
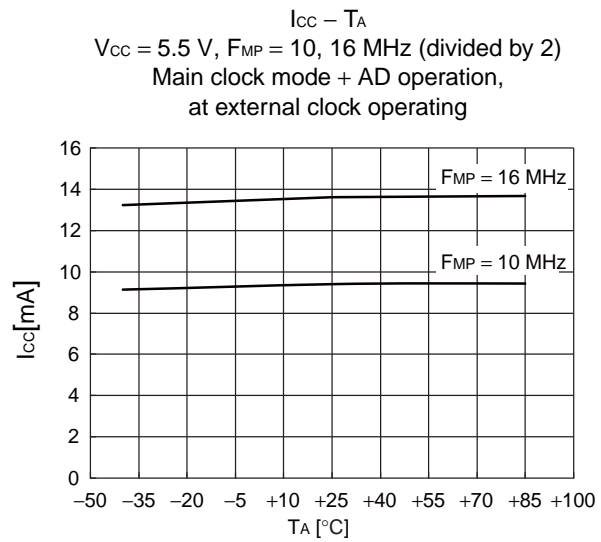
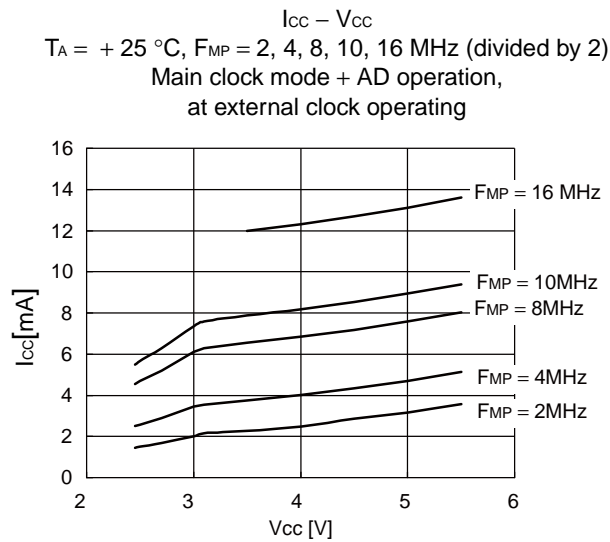
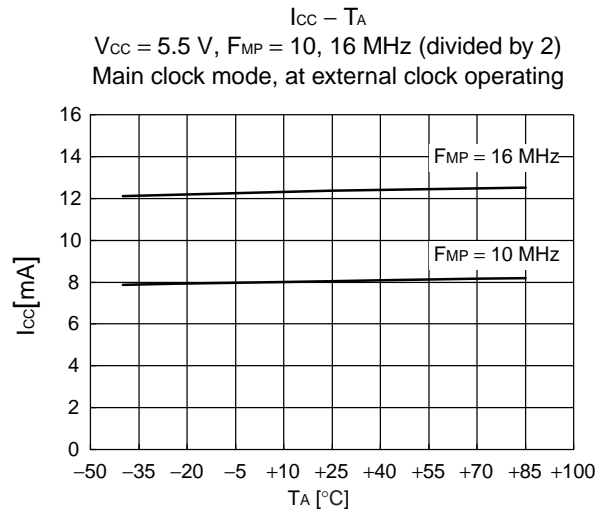
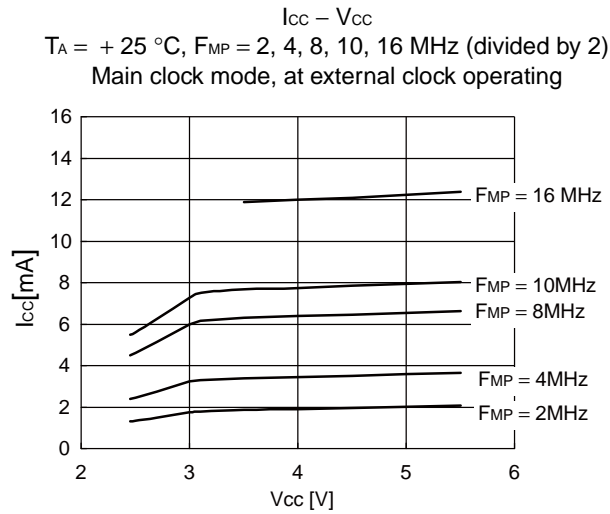
*1 : T_A = + 25 °C, V_{CC} = 5.0 V, 10000 cycles

*2 : T_A = + 85 °C, V_{CC} = 4.5 V, 10000 cycles

*3 : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at +85 °C) .

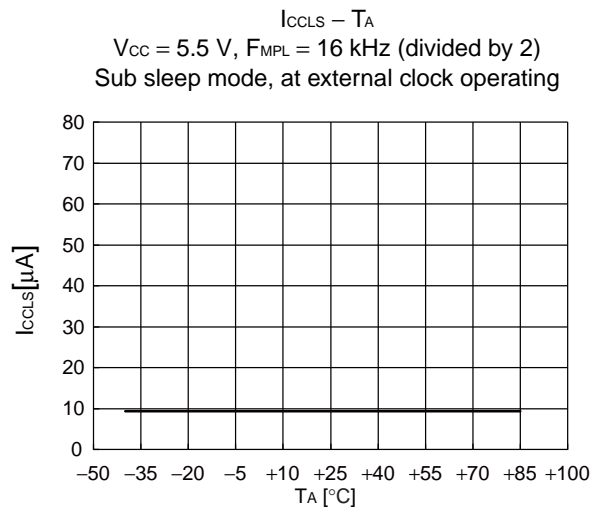
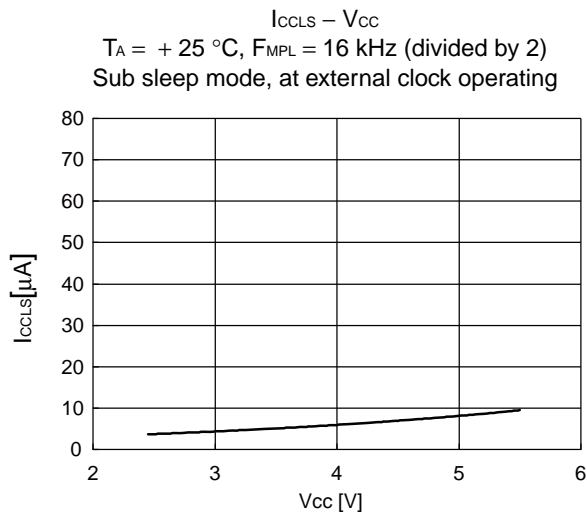
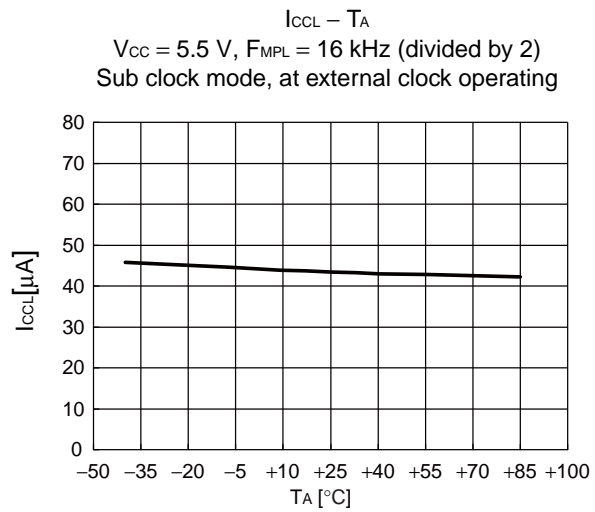
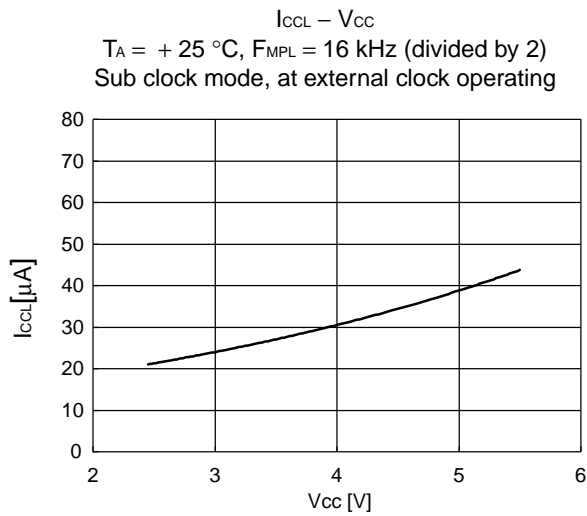
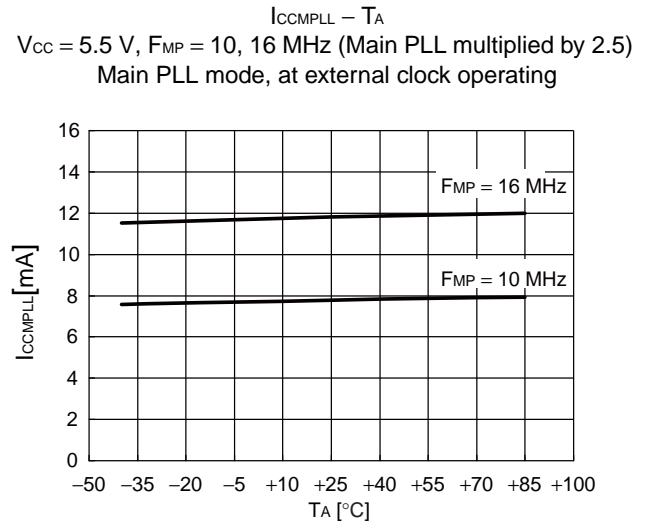
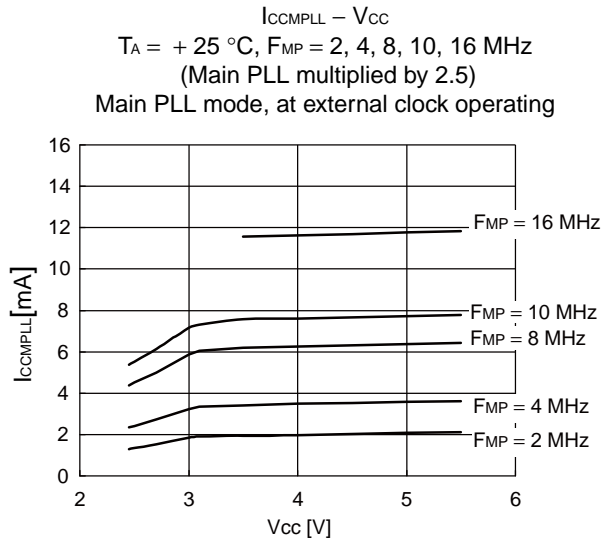
EXAMPLE CHARACTERISTICS

- Power supply current temperature (Flash memory product)

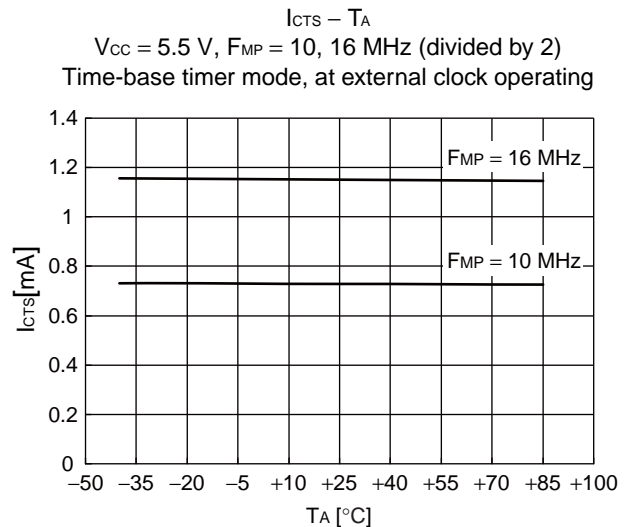
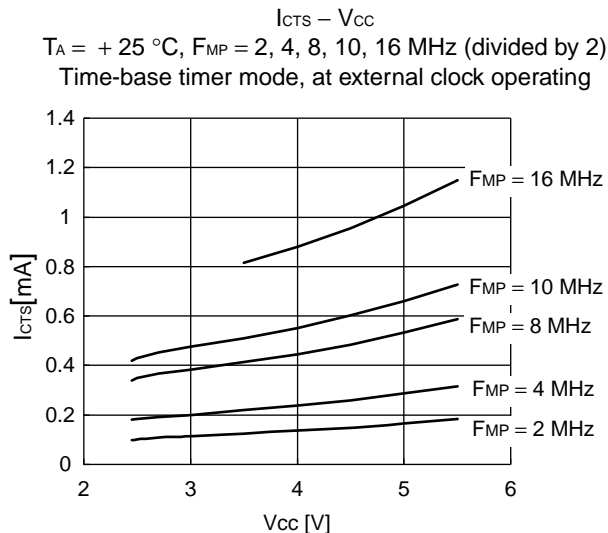
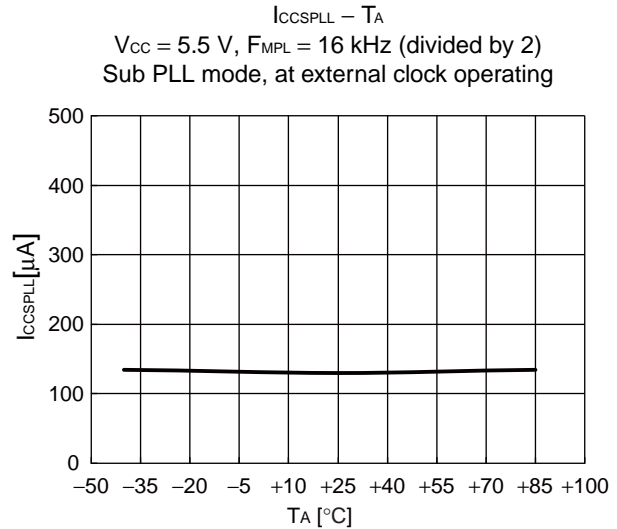
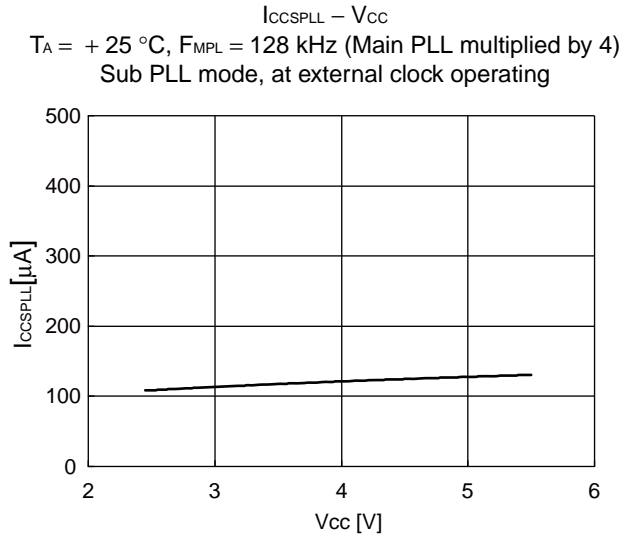
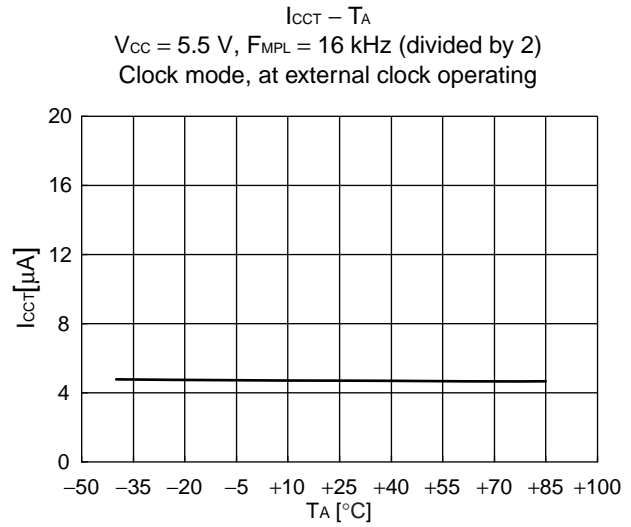
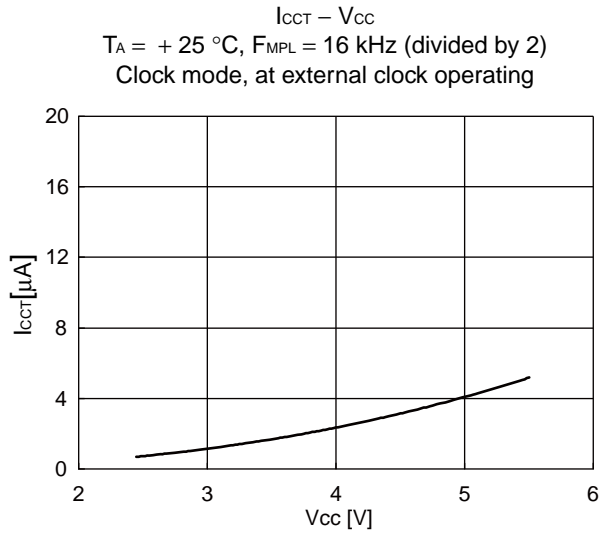


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MB95150M Series



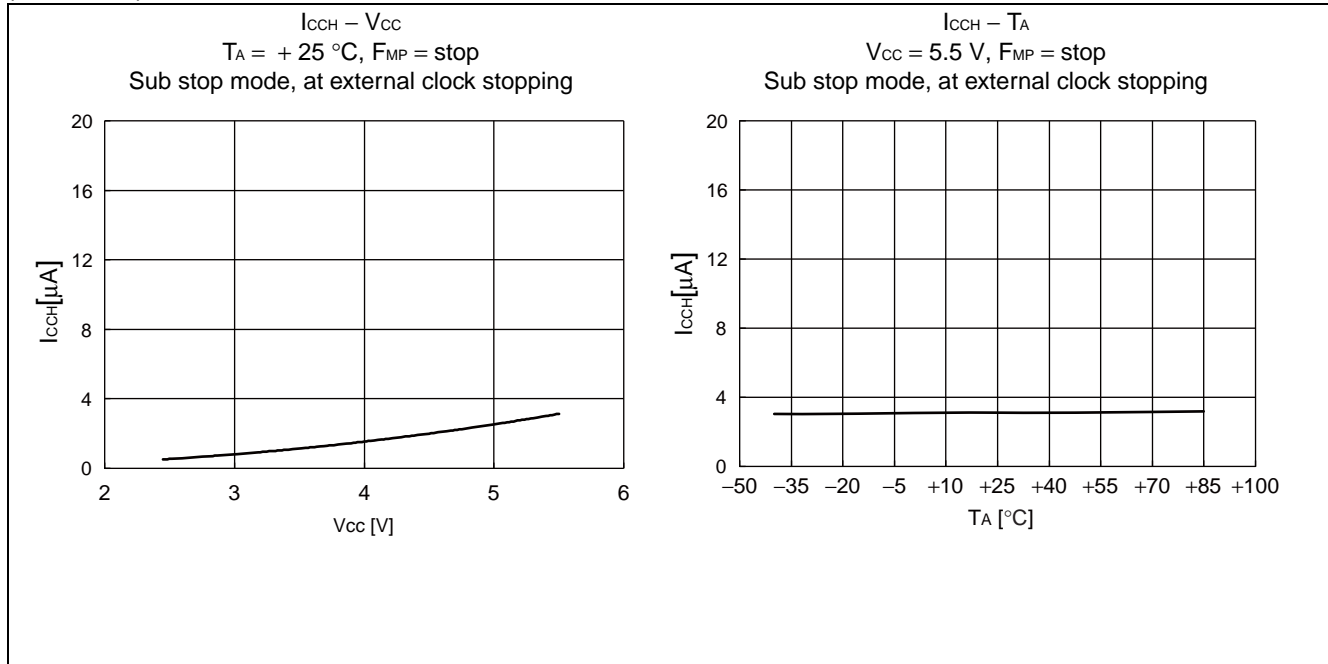
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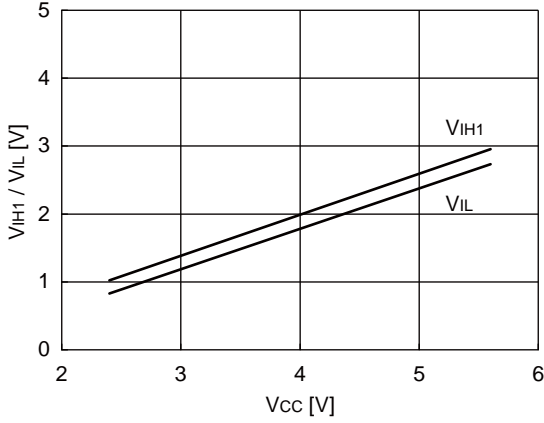
MB95150M Series

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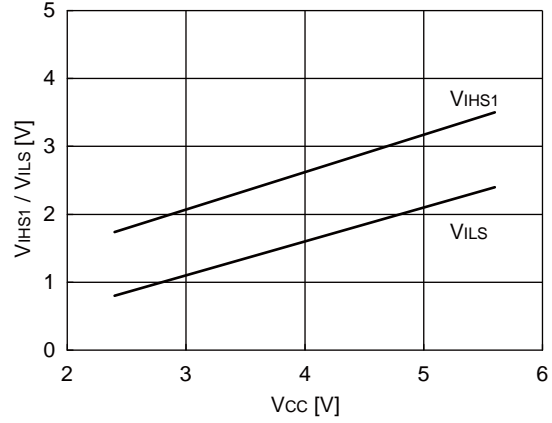


• Input voltage (Flash memory product)

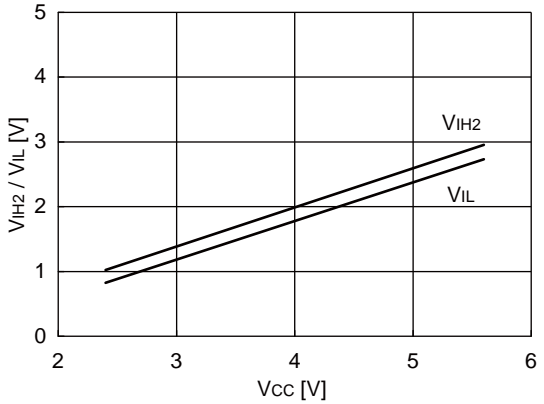
$V_{IH1} - V_{CC}$ and $V_{IL} - V_{CC}$
 $T_A = +25\text{ }^\circ\text{C}$



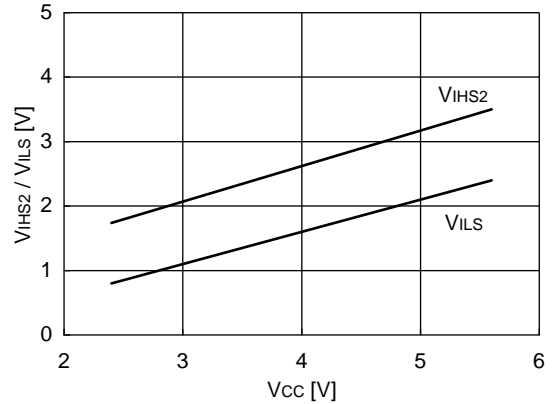
$V_{IHS1} - V_{CC}$ and $V_{ILS} - V_{CC}$
 $T_A = +25\text{ }^\circ\text{C}$



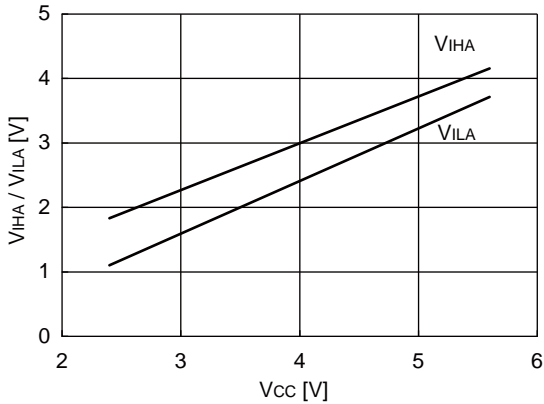
$V_{IH2} - V_{CC}$ and $V_{IL} - V_{CC}$
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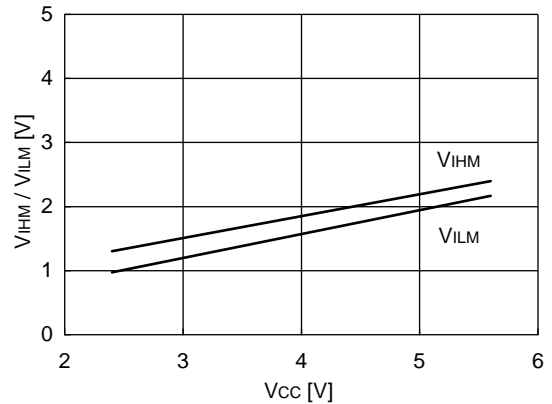
$V_{IHS2} - V_{CC}$ and $V_{ILS} - V_{CC}$
 $T_A = +25\text{ }^\circ\text{C}$



$V_{IHA} - V_{CC}$ and $V_{ILA} - V_{CC}$
 $T_A = +25\text{ }^\circ\text{C}$

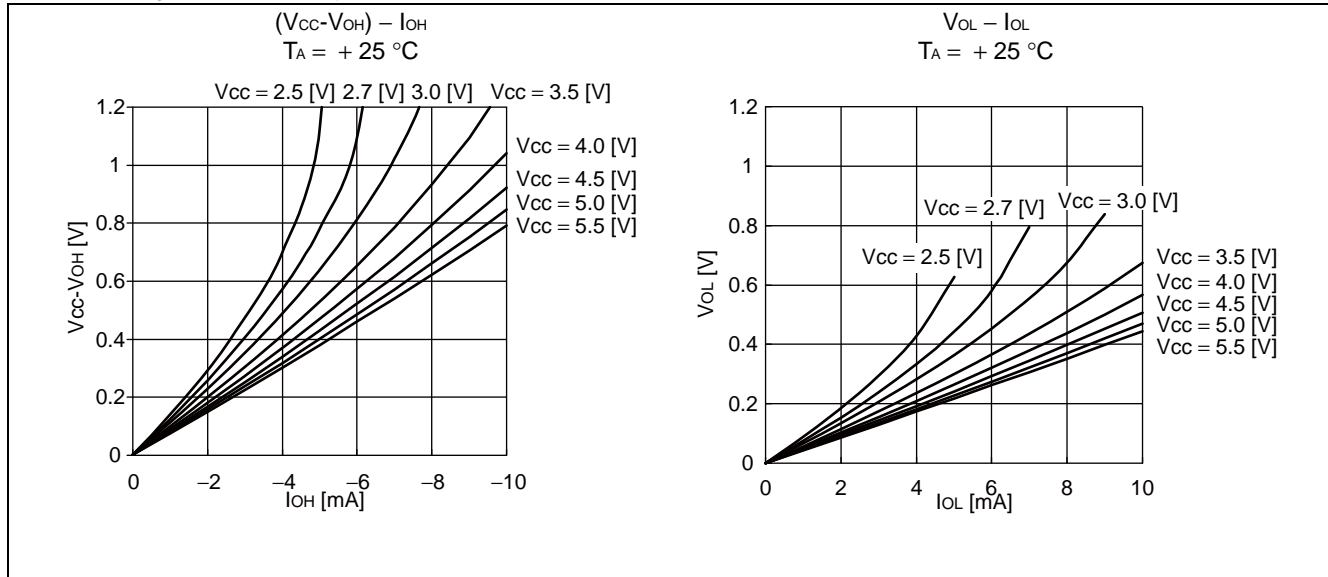


$V_{IHM} - V_{CC}$ and $V_{ILM} - V_{CC}$
 $T_A = +25\text{ }^\circ\text{C}$

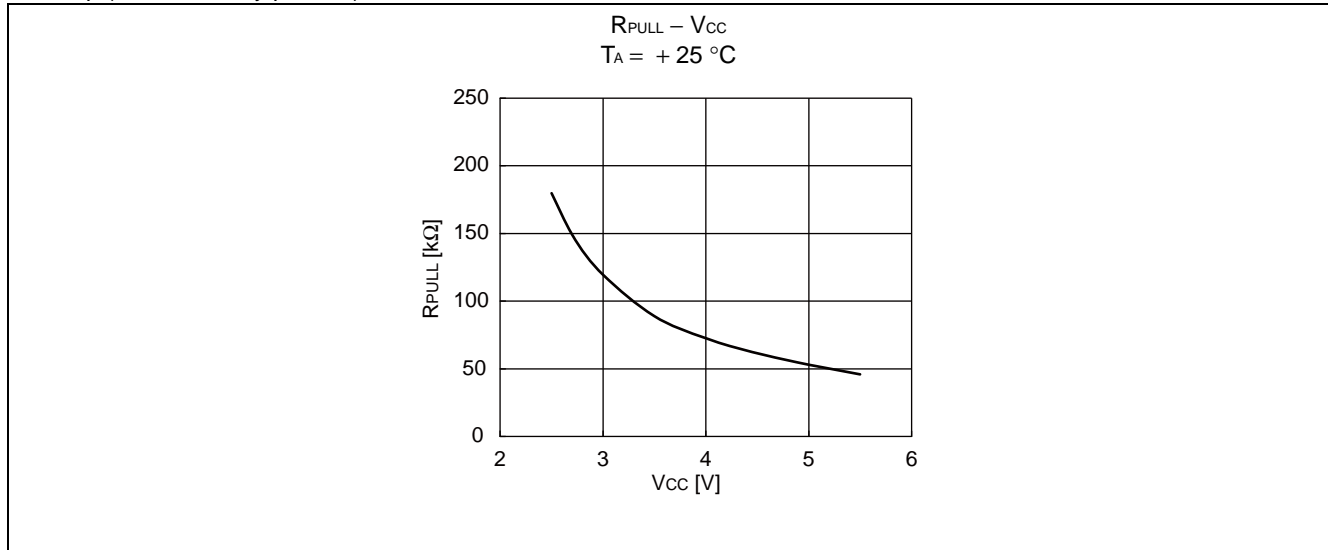


MB95150M Series

- Output voltage (Flash memory product)



- Pull-up (Flash memory product)



■ MASK OPTION

No.	Part number	MB95156M	MB95F156M MB95F156N MB95F156J	MB95FV100D-103
	Specifying procedure	Specify when ordering MASK	Setting disabled	Setting disabled
1	Clock mode select • Single-system clock mode • Dual-system clock mode	Dual-system clock mode	Dual-system clock mode	Changing by the switch on MCU board
2	Low voltage detection reset* • With low voltage detection reset • Without low voltage detection reset	Specify when ordering MASK	Specified by part number	Changing by the switch on MCU board
3	Clock supervisor* • With clock supervisor • Without clock supervisor	Specify when ordering MASK	Specified by part number	Changing by the switch on MCU board
4	Reset output* • With reset output • Without reset output	Specify when ordering MASK	Specified by part number	MCU board switch sets as follows ; • With clock supervisor : Without reset output • Without clock supervisor : With reset output
5	Oscillation stabilization wait time	Fixed to oscillation stabilization wait time of $(2^{14} - 2) / F_{CH}$	Fixed to oscillation stabilization wait time of $(2^{14} - 2) / F_{CH}$	Fixed to oscillation stabilization wait time of $(2^{14} - 2) / F_{CH}$

* : Refer to table below about clock mode select, low voltage detection reset, clock supervisor select and reset output.

Part number	Clock mode select	Low voltage detection reset	Clock supervisor	Reset output
MB95156M	Dual-system	No	No	Yes
		Yes	No	Yes
		Yes	Yes	No
MB95F156M	Dual-system	No	No	Yes
MB95F156N		Yes	No	Yes
MB95F156J		Yes	Yes	No
MB95FV100D-103	Single-system	No	No	Yes
		Yes	No	Yes
		Yes	Yes	No
	Dual-system	No	No	Yes
		Yes	No	Yes
		Yes	Yes	No

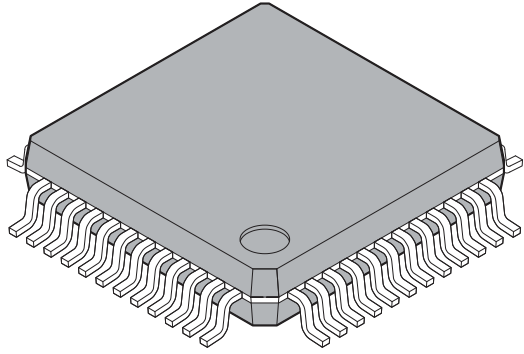
MB95150M Series

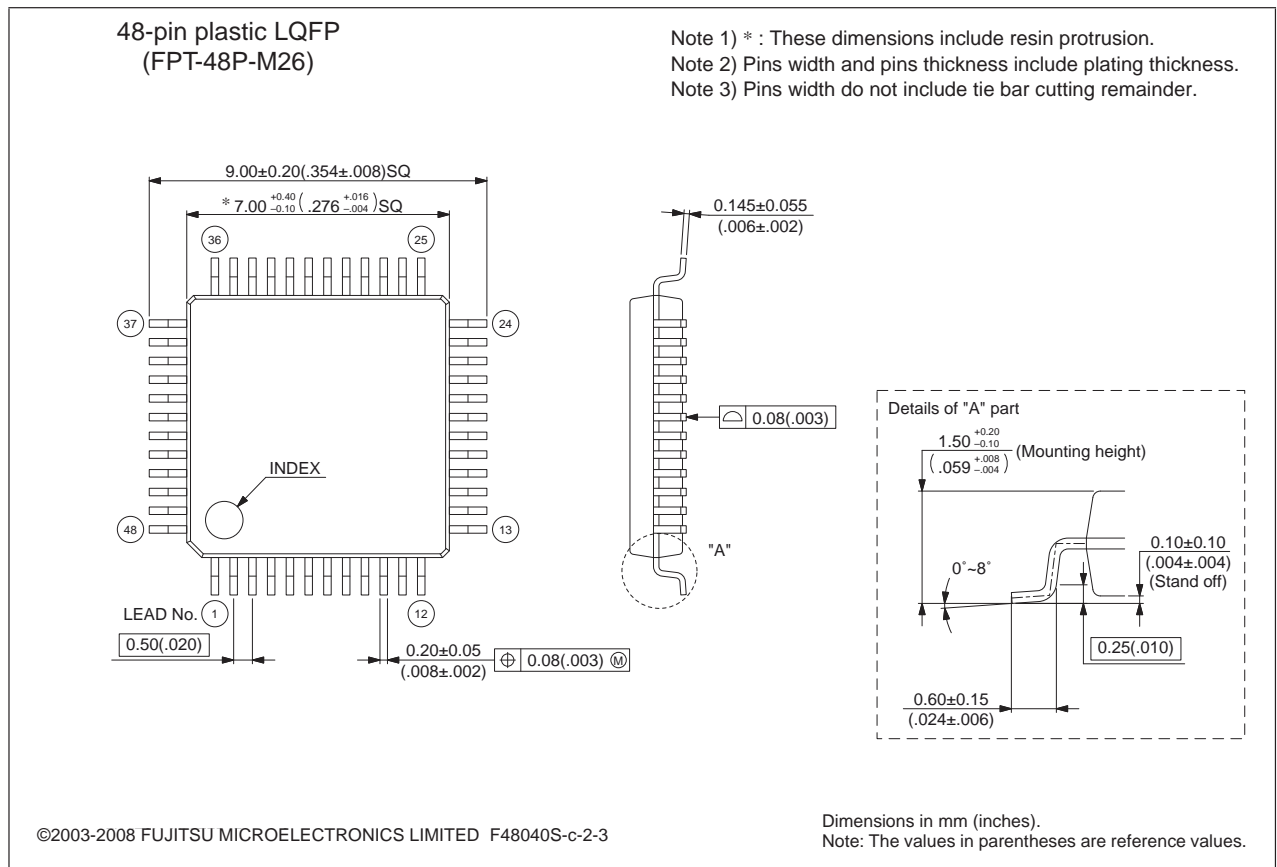
■ ORDERING INFORMATION

Part number	Package
MB95156MPMT MB95F156MPMT MB95F156NPMT MB95F156JPMT	48-pin plastic LQFP (FPT-48P-M26)
MB95156MPMC MB95F156MPMC MB95F156NPMC MB95F156JPMC	52-pin plastic LQFP (FPT-52P-M01)
MB2146-303A-E (MB95FV100D-103PBT)	MCU board (224-pin plastic PFBGA) (BGA-224P-M08)

MB95150M Series

PACKAGE DIMENSIONS

<p>48-pin plastic LQFP</p>  <p>(FPT-48P-M26)</p>	Lead pitch	0.50 mm
	Package width × package length	7 × 7 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.17 g
	Code (Reference)	P-LFQFP48-7×7-0.50

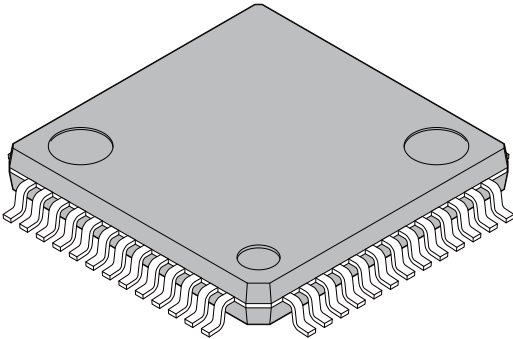


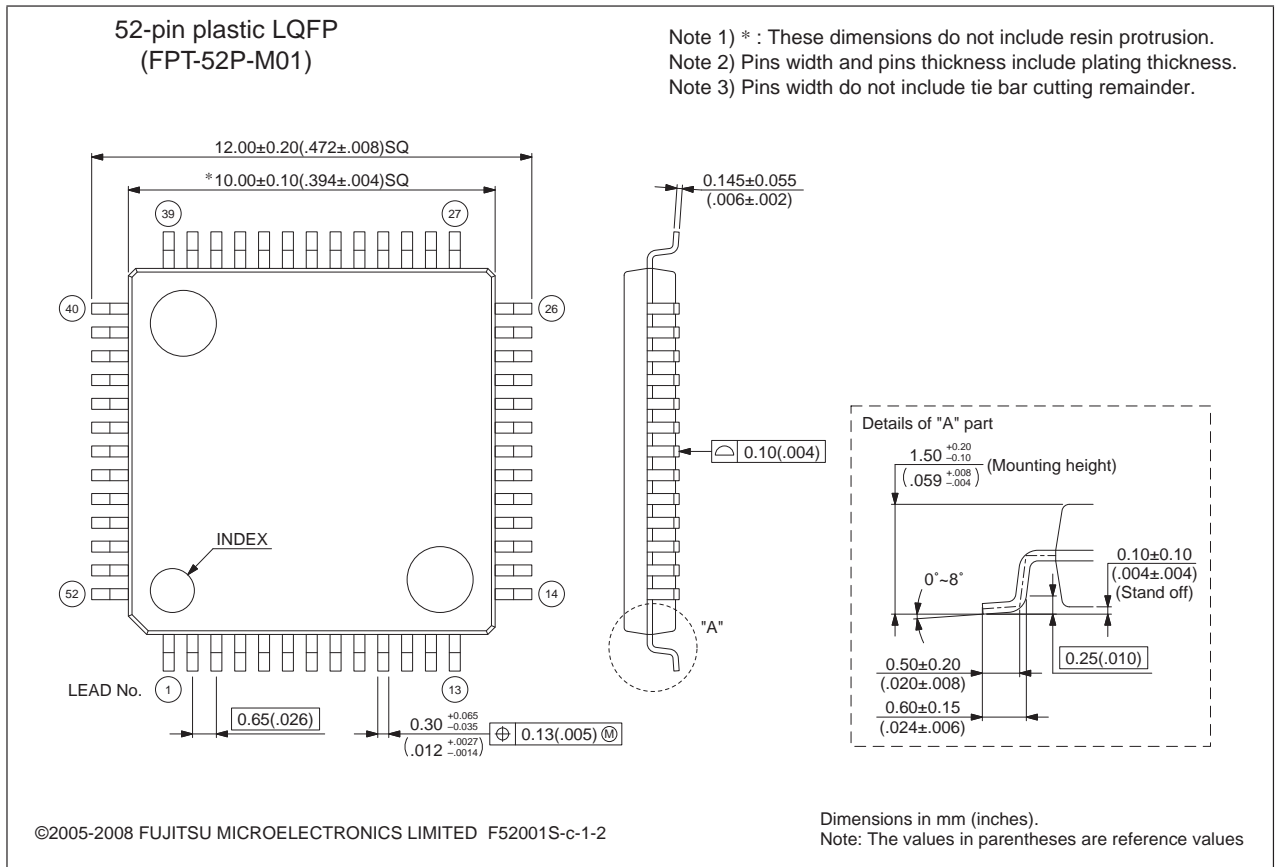
Please confirm the latest Package dimension by following URL.
<http://edevic.fujitsu.com/package/en-search/>

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MB95150M Series

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 <p>52-pin plastic LQFP</p> <p>(FPT-52P-M01)</p>	Lead pitch	0.65 mm
	Package width × package length	10.0 × 10.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm Max
	Code (Reference)	P-LQFP52-10×10-0.65



Please confirm the latest Package dimension by following URL.
<http://edevic.fujitsu.com/package/en-search/>

■ MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
4	■ PRODUCT LINEUP	Changed the Note. (MB2146-303A → MB2146-303A-E)
13	■ HANDLING DEVICES	Added the item of “• Serial communication”.
29	■ ELECTRICAL CHARACTERISTICS 2. Recommended Operating Conditions	Changed *2 its table footnote.
64	■ ORDERING INFORMATION	Changed the part number. (MB2146-303A → MB2146-303A-E)

The vertical lines marked in the left side of the page show the changes.

MB95150M Series

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