FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-12621-3E

8-bit Microcontrollers

CMOS

F^2MC-8FX MB95130MB Series

MB95136MB/F133MBS/F133NBS/F133JBS/F134MBS/F134NBS/F134JBS/ MB95F136MBS/F136NBS/F136JBS/F133MBW/F133NBW/F133JBW/F134MBW/ MB95F134NBW/F134JBW/F136MBW/F136NBW/F136JBW/FV100D-103

■ DESCRIPTION

The MB95130MB series is general-purpose, single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers contain a variety of peripheral functions.

Note: F^2MC is the abbreviation of FUJITSU Flexible Microcontroller.

■ FEATURES

- F^2MC-8FX CPU core
  Instruction set optimized for controllers
  - Multiplication and division instructions
  - 16-bit arithmetic operations
  - Bit test branch instruction
  - Bit manipulation instructions etc.
- Clock
  - Main clock
  - Main PLL clock
  - Sub clock (for dual clock product)
  - Sub PLL clock (for dual clock product)

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For the information for microcontroller supports, see the following web site.

http://edevice.fujitsu.com/micom/en-support/

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- Timer
    - 8/16-bit compound timer × 1 channel
    - 8/16-bit PPG × 1 channel
    - 16-bit PPG × 1 channel
    - Time-base timer × 1 channel
    - Watch prescaler (for dual clock product) × 1 channel
- LIN-UART × 1 channel
    - LIN function, Clock asynchronous (UART) or clock synchronous (SIO) serial data transfer capable
    - Full duplex double buffer
- UART/SIO × 1 channel
    - Clock asynchronous (UART) or clock synchronous (SIO) serial data transfer capable
    - Full duplex double buffer
- External interrupt × 8 channels
    - Interrupt by edge detection (rising, falling, or both edges can be selected)
    - Can be used to recover from low-power consumption (standby) modes.
- 8/10-bit A/D converter × 8 channels
    - 8-bit or 10-bit resolution can be selected.
- Low-power consumption (standby) mode
    - Stop mode
    - Sleep mode
    - Watch mode (for dual clock product)
    - Time-base timer mode
- I/O port
    - The number of maximum ports
        - Single clock product : 19 ports
        - Dual clock product : 17 ports
    - Configuration

      General-purpose I/O ports (COMS) : Single clock product : 19 ports
      Dual clock product : 17 ports
- Power-on reset

  A power-on reset is generated when the power is switched on.
- Programmable input voltage levels of port

  Automotive input level / CMOS input level / hysteresis input level
- Flash memory security function

  Protects the content of Flash memory (Flash memory device only)

■ MEMORY LINEUP

	Flash memory	RAM
MB95F133MBS/F133NBS/F133JBS	8 Kbytes	256 bytes
MB95F133MBW/F133NBW/F133JBW		
MB95F134MBS/F134NBS/F134JBS	16 Kbytes	512 bytes
MB95F134MBW/F134NBW/F134JBW		
MB95F136MBS/F136NBS/F136JBS	32 Kbytes	1 Kbyte
MB95F136MBW/F136NBW/F136JBW		

■ PRODUCT LINEUP

Part number / Parameter		MB95136MB	MB95 F133MBS/ F134MBS/ F136MBS	MB95 F133NBS/ F134NBS/ F136NBS	MB95 F133MBW/ F134MBW/ F136MBW	MB95 F133NBW/ F134NBW/ F136NBW	MB95 F133JBS/ F134JBS/ F136JBS	MB95 F133JBW/ F134JBW/ F136JBW
Type		MASK ROM product	Flash memory product					
ROM capacity*1		32 Kbytes (Max)						
RAM capacity*1		1 Kbyte (Max)						
Power-on reset		Yes						
Reset output		Not selectable*2	Yes				No	
Option*2	Clock system	Selectable single/dual clock*3	Single clock		Dual clock		Single clock	Dual clock
	Low voltage detection reset	Yes/No	No	Yes	No	Yes		
	Clock supervisor	Yes/No	No				Yes	
CPU functions		Number of basic instructions : 136 Instruction bit length : 8 bits Instruction length : 1 to 3 bytes Data bit length : 1, 8, and 16 bits Minimum instruction execution time : 61.5 ns (at machine clock frequency 16.25 MHz) Interrupt processing time : 0.6 µs (at machine clock frequency 16.25 MHz)						
Peripheral functions	General-purpose I/O port	• Single clock product : 19 ports • Dual clock product : 17 ports Programmable input voltage levels of port : Automotive input level / CMOS input level / hysteresis input level						
	Time-base timer (1 channel)	Interval time : 0.5 ms, 2.1 ms, 8.2 ms, 32.8 ms (at main oscillation clock 4 MHz)						
	Watchdog timer	Reset generated cycle At main oscillation clock 10 MHz : Min 105 ms At sub oscillation clock 32.768 kHz (for dual clock product) : Min 250 ms						
	Wild register	Capable of replacing 3 bytes of ROM data						
	UART/SIO (1 channel)	Data transfer capable in UART/SIO Full duplex double buffer, variable data length (5/6/7/8-bit), built-in baud rate generator NRZ type transfer format, error detected function LSB-first or MSB-first can be selected. Clock asynchronous (UART) or clock synchronous (SIO) serial data transfer capable						
	LIN-UART (1 channel)	Dedicated reload timer allowing a wide range of communication speeds to be set. Full duplex double buffer. Clock asynchronous (UART) or clock synchronous (SIO) serial data transfer capable LIN functions available as the LIN master or LIN slave.						

(Continued)

Part number Parameter		MB95136MB	MB95 F133MBS/ F134MBS/ F136MBS	MB95 F133NBS/ F134NBS/ F136NBS	MB95 F133MBW/ F134MBW/ F136MBW	MB95 F133NBW/ F134NBW/ F136NBW	MB95 F133JBS/ F134JBS/ F136JBS	MB95 F133JBW/ F134JBW/ F136JBW
Peripheral functions	8/10-bit A/D converter (8 channels)	8-bit or 10-bit resolution can be selected.						
	8/16-bit compound timer (1 channel)	Each channel of the timer can be used as “8-bit timer x 2 channels” or “16-bit timer x 1 channel”. Built-in timer function, PWC function, PWM function, capture function and square wave-form output Count clock: 7 internal clocks and external clock can be selected.						
	16-bit PPG (1 channel)	PWM mode or one-shot mode can be selected. Counter operating clock: Eight selectable clock sources Support for external trigger start						
	8/16-bit PPG (1 channel)	Each channel of the PPG can be used as “8-bit PPG x 2 channels” or “16-bit PPG x 1 channel”. Counter operating clock: Eight selectable clock sources						
	Watch counter (for dual clock product) (1 channel)	Count clock : Four selectable clock sources (125 ms, 250 ms, 500 ms, or 1 s) Counter value can be set from 0 to 63. (Capable of counting for 1 minute when selecting clock source 1 second and setting counter value to 60)						
	Watch prescaler (for dual clock product) (1 channel)	Four selectable interval times (125 ms, 250 ms, 500 ms, or 1 s)						
	External interrupt (8 channels)	Interrupt by edge detection (rising, falling, or both edges can be selected.) Can be used to recover from standby modes.						
Flash memory		Supports automatic programming, Embedded Algorithm Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Number of write/erase cycles (Minimum) : 10000 times Data retention time : 20 years Erase can be performed on each block Block protection with external programming voltage Flash Security Feature for protecting the content of the Flash (MB95F136MBS/F136NBS/F136JBS/F136MBW/F136NBW/F136JBW)						
Standby mode		Sleep, stop, watch (for dual clock product), and time-base timer						

*1 : For ROM capacity and RAM capacity, refer to “■ MEMORY LINEUP”.

*2 : For details of option, refer to “■ MASK OPTION”.

*3 : Specify clock mode when ordering MASK ROM.

Note: Part number of evaluation product in MB95130MB series is MB95FV100D-103.
When using it, the MCU board (MB2146-303A-E) is required.

■ OSCILLATION STABILIZATION WAIT TIME

The initial value of the main clock oscillation stabilization wait time is fixed to the maximum value. The maximum value is shown below.

Oscillation stabilization wait time	Remarks
$(2^{14}-2)/F_{CH}$	Approx. 4.10 ms (at main oscillation clock 4 MHz)

■ PACKAGES AND CORRESPONDING PRODUCTS

Part number / Package	MB95136MB	MB95F133MBS MB95F133NBS MB95F134MBS MB95F134NBS MB95F136MBS MB95F136NBS MB95F133JBS MB95F134JBS MB95F136JBS	MB95F133MBW MB95F133NBW MB95F134MBW MB95F134NBW MB95F136MBW MB95F136NBW MB95F133JBW MB95F134JBW MB95F136JBW	MB95FV100D-103
FPT-28P-M17	○	○	○	×
FPT-30P-M02	○	○	○	×
BGA-224P-M08	×	×	×	○

○ : Available
× : Unavailable

■ DIFFERENCES AMONG PRODUCTS AND NOTES ON SELECTING PRODUCTS

- Notes on using evaluation products

  The Evaluation product has not only the functions of the MB95130MB series but also those of other products to support software development for multiple series and models of the F^2MC-8FX. The I/O addresses for peripheral resources not used by the MB95130MB series are therefore access-barred. Read/write access to those access-barred addresses may cause peripheral resources supposed to be unused to operate, resulting in unexpected malfunctions of hardware or software.

  Particularly, do not use word access to an odd-numbered-byte address in the prohibited areas (If such access is used, the address may be read or written unexpectedly) .

  Also, as the read values of prohibited addresses on the evaluation product are different to the values on the flash memory and mask ROM products, do not use these values in the software processing.

  The Evaluation product does not support the functions of some bits in single-byte registers. Read/write access to these bits does not cause hardware malfunctions. No particular precautions are required to the flash memory and mask ROM products, as they have the identical read/write operation to the evaluation products.

- Difference of memory spaces

  If the amount of memory on the Evaluation product is different from that of the Flash memory or MASK ROM product, carefully check the difference in the amount of memory from the model to be actually used when developing software.

  For details of memory space, refer to “■ CPU CORE”.

- Current consumption
  - The current consumption of Flash memory product is greater than for MASK ROM product.
  - For details of current consumption, refer to “■ ELECTRICAL CHARACTERISTICS”.

- Package

  For details of information on each package, refer to “■ PACKAGES AND CORRESPONDING PRODUCTS” and “■ PACKAGE DIMENSION”.

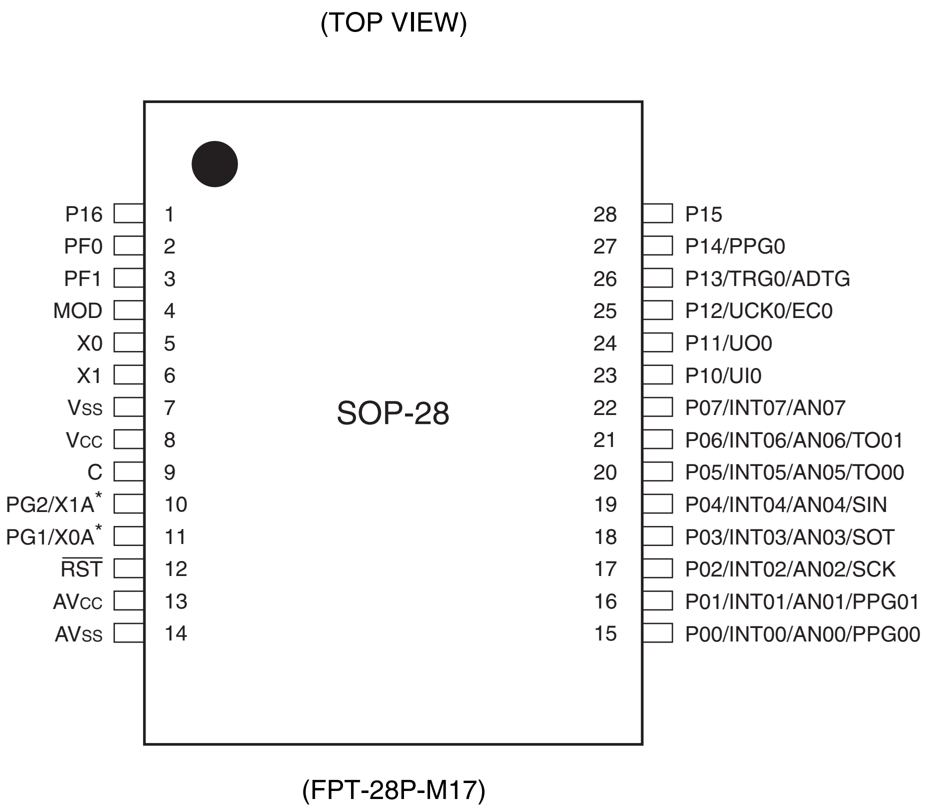
- Operating voltage

  The operating voltage is different among the Evaluation, Flash memory, and MASK ROM products.
  For details of the operating voltage, refer to “■ ELECTRICAL CHARACTERISTICS”.

- Difference MOD Pins

  A pull-down resistor is provided for the MOD pin of the MASK ROM product.

■ PIN ASSIGNMENT


(TOP VIEW)
SOP-28
P16 1
PF0 2
PF1 3
MOD 4
X0 5
X1 6
Vss 7
Vcc 8
C 9
PG2/X1A* 10
PG1/X0A* 11
$\overline{\text{RST}}$ 12
AVcc 13
AVss 14
15 P00/INT00/AN00/PPG00
16 P01/INT01/AN01/PPG01
17 P02/INT02/AN02/SCK
18 P03/INT03/AN03/SOT
19 P04/INT04/AN04/SIN
20 P05/INT05/AN05/TO00
21 P06/INT06/AN06/TO01
22 P07/INT07/AN07
23 P10/UI0
24 P11/UO0
25 P12/UCK0/EC0
26 P13/TRG0/ADTG
27 P14/PPG0
28 P15
(FPT-28P-M17)

* : Single clock product is general-purpose port, and dual clock product is sub clock oscillation pin.

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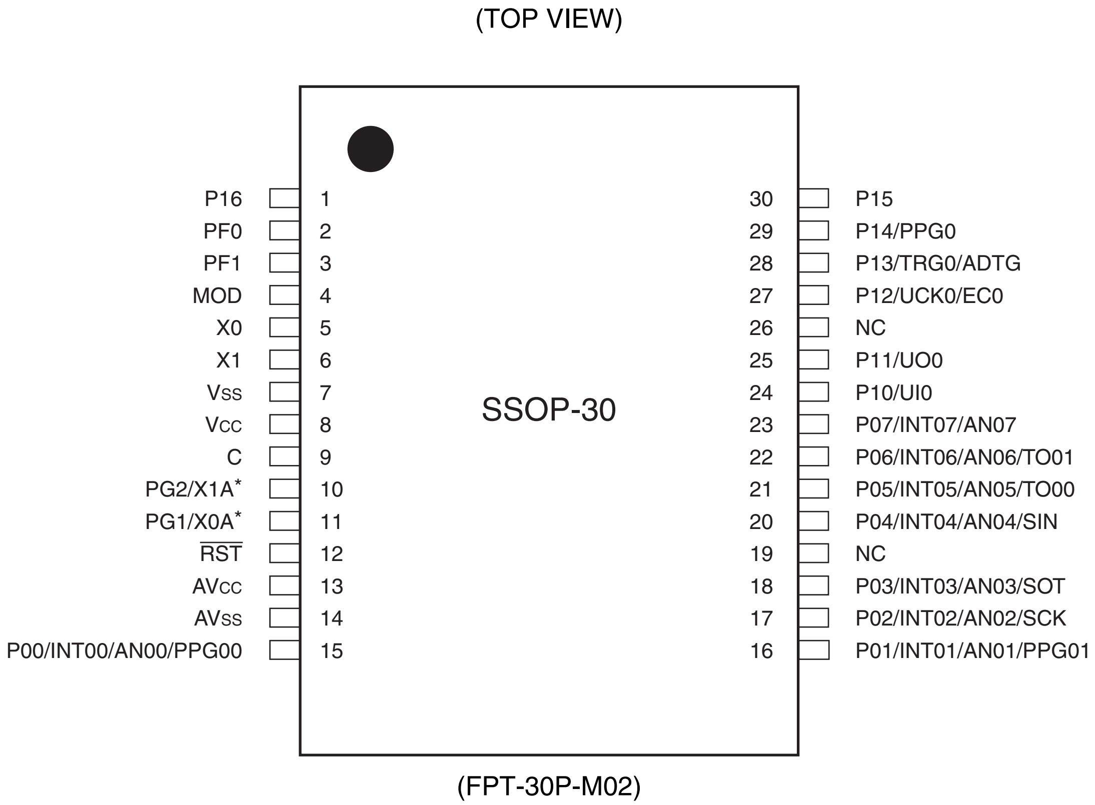

(TOP VIEW)
SSOP-30
(FPT-30P-M02)
P16 1
PF0 2
PF1 3
MOD 4
X0 5
X1 6
Vss 7
Vcc 8
C 9
PG2/X1A* 10
PG1/X0A* 11
$\overline{\text{RST}}$ 12
AVcc 13
AVss 14
P00/INT00/AN00/PPG00 15
30 P15
29 P14/PPG0
28 P13/TRG0/ADTG
27 P12/UCK0/EC0
26 NC
25 P11/UO0
24 P10/UI0
23 P07/INT07/AN07
22 P06/INT06/AN06/TO01
21 P05/INT05/AN05/TO00
20 P04/INT04/AN04/SIN
19 NC
18 P03/INT03/AN03/SOT
17 P02/INT02/AN02/SCK
16 P01/INT01/AN01/PPG01

* : Single clock product is general-purpose port, and dual clock product is sub clock oscillation pin.

■ PIN DESCRIPTION

Pin no.		Pin name	I/O circuit type*3	Function
SSOP*1	SOP*2			
1	1	P16	H	General-purpose I/O port
2	2	PF0	K	General-purpose I/O port for large current
3	3	PF1		
4	4	MOD	B	Operating mode designation pin
5	5	X0	A	Main clock oscillation input pin
6	6	X1		Main clock oscillation input/output pin
7	7	V_{SS}	—	Power supply pin (GND)
8	8	V_{CC}	—	Power supply pin
9	9	C	—	Capacity connection pin
10	10	PG2/X1A	H/A	Single clock product is general-purpose port (PG2) . Dual clock product is sub clock input/output oscillation pin (32 kHz) .
11	11	PG1/X0A		Single clock product is general-purpose port (PG1) . Dual clock product is sub clock input oscillation pin (32 kHz) .
12	12	$\overline{\text{RST}}$	B’	Reset pin
13	13	AV_{CC}	—	A/D converter power supply pin
14	14	AV_{SS}	—	A/D converter power supply pin (GND)
15	15	P00/INT00/AN00/PPG00	D	General-purpose I/O port Shared with external interrupt input (INT00), A/D converter analog input (AN00) and 8/16-bit PPG ch.0 output (PPG00).
16	16	P01/INT01/AN01/PPG01		General-purpose I/O port Shared with external interrupt input (INT01), A/D converter analog input (AN01) and 8/16-bit PPG ch.0 output (PPG01).
17	17	P02/INT02/AN02/SCK		General-purpose I/O port Shared with external interrupt input (INT02), A/D converter analog input (AN02) and LIN-UART clock I/O (SCK).
18	18	P03/INT03/AN03/SOT		General-purpose I/O port Shared with external interrupt input (INT03), A/D converter analog input (AN03) and LIN-UART data output (SOT).
20	19	P04/INT04/AN04/SIN	E	General-purpose I/O port Shared with external interrupt input (INT04), A/D converter analog input (AN04) and LIN-UART data input (SIN).
21	20	P05/INT05/AN05/TO00	D	General-purpose I/O port Shared with external interrupt input (INT05 & INT06), A/D converter analog input (AN05 & AN06) and 8/16-bit compound timer ch.0 output (TO00 & TO01).
22	21	P06/INT06/AN06/TO01		
23	22	P07/INT07/AN07		General-purpose I/O port Shared with external interrupt input (INT07) and A/D converter analog input (AN07).

(Continued)

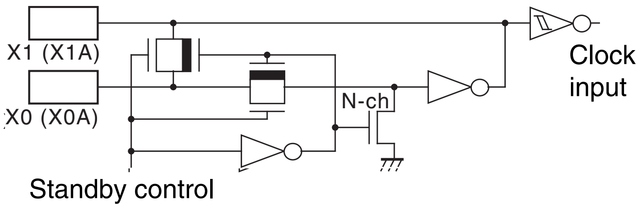
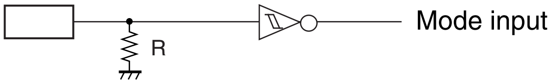
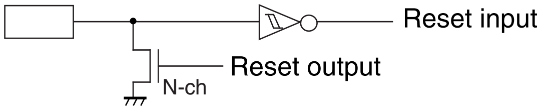
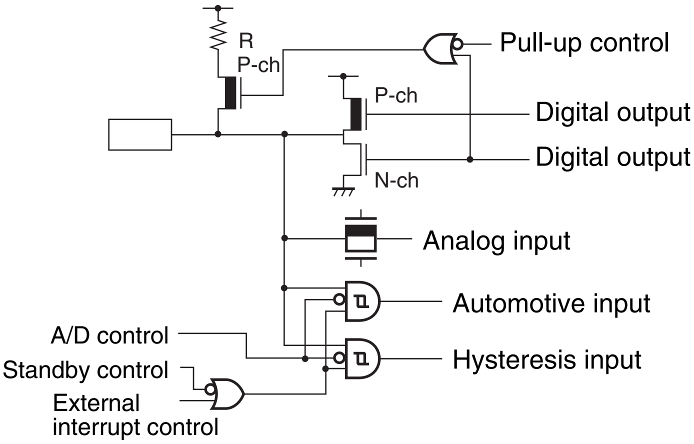
Pin no.		Pin name	I/O circuit type*3	Function
SSOP*1	SOP*2			
24	23	P10/UIO	G	General-purpose I/O port Shared with UART/SIO ch.0 data input (UI0)
25	24	P11/UO0	H	General-purpose I/O port Shared with UART/SIO ch.0 data output (UO0)
27	25	P12/UCK0/ EC0		General-purpose I/O port Shared with UART/SIO ch.0 clock I/O (UCK0) and 8/16-bit compound timer ch.0 clock input (EC0)
28	26	P13/TRG0/ ADTG		General-purpose I/O port Shared with 16-bit PPG ch.0 trigger input (TRG0) and A/D converter trigger input (ADTG)
29	27	P14/PPG0		General-purpose I/O port Shared with 16-bit PPG ch.0 output (PPG0)
30	28	P15		General-purpose I/O port
19,26	—	NC	—	Internally connected pins. Be sure to leave it open.

*1 : FPT-30P-M02

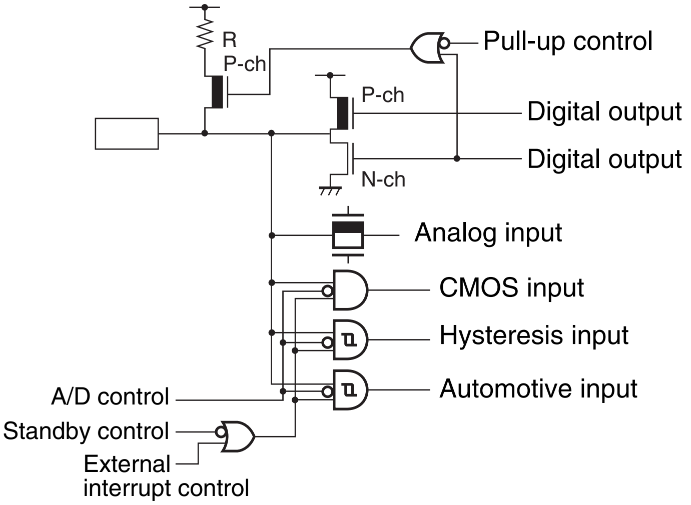
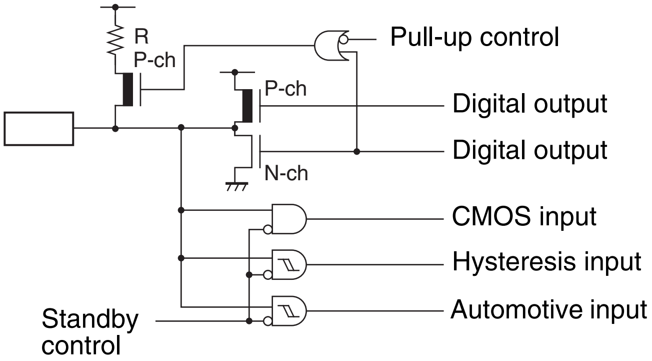
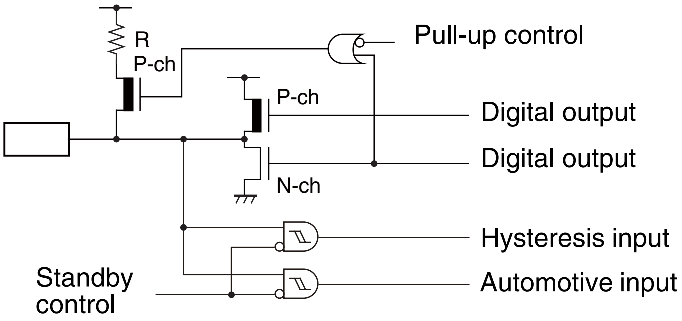
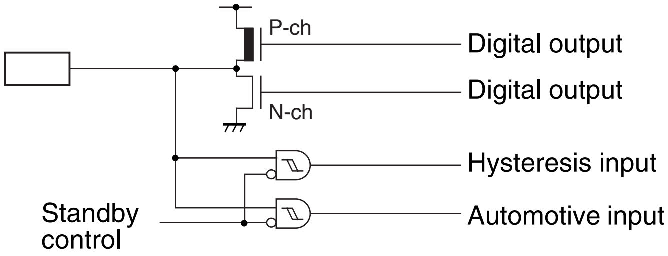
*2 : FPT-28P-M17

*3 : For the I/O circuit type, refer to "■ I/O CIRCUIT TYPE".

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A	 X1 (X1A) X0 (X0A) N-ch Clock input Standby control	• Oscillation circuit • High-speed side Feedback resistance: approx. 1 MΩ • Low-speed side Feedback resistance: approx. 10 MΩ
B	 R Mode input	Only for input • Hysteresis input • Pull-down resistor available only to MASK ROM product
B’	 Reset input Reset output N-ch	• Hysteresis input only for MASK ROM product • Reset output
D	 R P-ch Pull-up control P-ch Digital output Digital output N-ch Analog input Automotive input A/D control Hysteresis input Standby control External interrupt control	• CMOS output • Hysteresis input • Analog input • Pull-up control available • Automotive input

(Continued)

Type	Circuit	Remarks
E	 R P-ch Pull-up control P-ch Digital output Digital output N-ch Analog input CMOS input Hysteresis input Automotive input A/D control Standby control External interrupt control	• CMOS output • CMOS input • Hysteresis input • Analog input • Pull-up control available • Automotive input
G	 R P-ch Pull-up control P-ch Digital output Digital output N-ch CMOS input Hysteresis input Automotive input Standby control	• CMOS output • CMOS input • Hysteresis input • Pull-up control available • Automotive input
H	 R P-ch Pull-up control P-ch Digital output Digital output N-ch Hysteresis input Automotive input Standby control	• CMOS output • Hysteresis input • Pull-up control available • Automotive input
K	 P-ch Digital output Digital output N-ch Hysteresis input Automotive input Standby control	• CMOS output • Hysteresis input • Automotive input

■ HANDLING DEVICES

- Preventing latch-up

  Care must be taken to ensure that maximum voltage ratings are not exceeded when the devices are used. Latch-up may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- and high-withstand voltage pins or if voltage higher than the rating voltage is applied between V_{CC} pin and V_{SS} pin.
  When latch-up occurs, power supply current increases rapidly and might thermally damage elements.
  Also, take care to prevent the analog power supply voltage (AV_{CC}) and analog input voltage from exceeding the digital power supply voltage (V_{CC}) when the analog system power supply is turned on or off.

- Stable supply voltage

  Supply voltage should be stabilized.
  A sudden change in power supply voltage may cause a malfunction even within the guaranteed operating range of the V_{CC} power supply voltage.
  For stabilization, in principle, keep the variation in V_{CC} ripple (p-p value) in a commercial frequency range (50 / 60 Hz) not to exceed 10% of the standard V_{CC} value and suppress the voltage variation so that the transient variation rate does not exceed 0.1 V/ms during a momentary change such as when the power supply is switched.

- Precautions for use of external clock

  Even when an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from the sub clock mode or stop mode.

PIN CONNECTION

- Treatment of unused pins

  Leaving unused input pins unconnected can cause abnormal operation or latch-up, leading to permanent damage. Unused input pins should always be pulled up or down through resistance of at least 2 kΩ.
  Any unused input/output pins may be set to the output mode and left open, or set to the input mode and treated the same as unused input pins. If there is any unused output pin, make it open.

- Treatment of power supply pins on A/D converter

  Connect to be $AV_{CC} = V_{CC}$ and $AV_{SS} = V_{SS}$ even if the A/D converter is not in use.
  Noise riding on the AV_{CC} pin may cause accuracy degradation. So, connect approx. 0.1 µF ceramic capacitor as a bypass capacitor between AV_{CC} and AV_{SS} pins in the vicinity of this device.

- Power Supply Pins

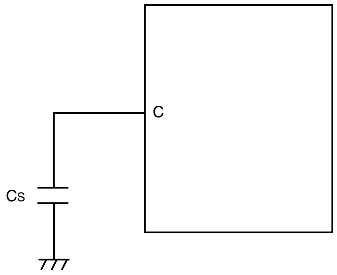
  In products with multiple V_{CC} or V_{SS} pins, the pins of the same potential are internally connected in the device to avoid abnormal operations including latch-up. However, all the pins must be connected to external power supply and a ground line to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating. Moreover, connect the current supply source with the V_{CC} and V_{SS} pins of this device at the low impedance.
  It is also advisable to connect a ceramic bypass capacitor of approximately 0.1 µF between V_{CC} and V_{SS} pins near this device.

- Mode pin (MOD)

  Connect the mode pin directly to V_{CC} or V_{SS} pins.
  To prevent the device unintentionally entering the test mode due to noise, lay out the printed circuit board so as to minimize the distance from the mode pins to V_{CC} or V_{SS} pins and to provide a low-impedance connection.

Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. A bypass capacitor of V_{CC} pin must have a capacitance value higher than C_S. For connection of smoothing capacitor C_S, refer to the diagram below.

- C Pin Connection Diagram



- Analog power supply

  Always set the same potential to AV_{CC} pin and V_{CC} pin. When $V_{CC} > AV_{CC}$, the current may flow through the AN00 to AN07 pins.

- NC pins

  Any pins marked "NC"(not connected) must be left open.

■ PROGRAMMING FLASH MEMORY MICROCONTROLLERS USING PARALLEL PROGRAMMER

• Supported parallel programmers and adapters

The following table lists supported parallel programmers and adapters.

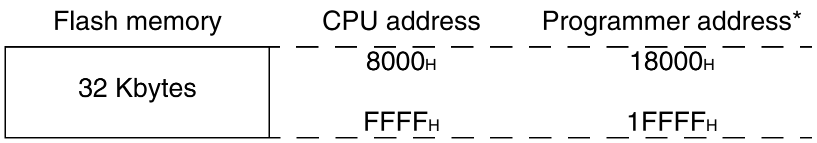
Package	Applicable adapter model	Parallel programmers
FPT-28P-M17	TEF110-95F136HSPF	AF9708 (Since Rev 02.43E) AF9709/B (Since Rev 02.43E)
FPT-30P-M02	TEF110-95F136MB	

Note: : For information about applicable adapter models and parallel programmers, contact the following:
Flash Support Group, Inc. TEL: +81-53-428-8380

• Sector configuration

The following table shows sector-specific addresses for data access by CPU and by the parallel programmer.

• MB95F136MBS/F136NBS/F136MBW/F136NBW/F136JBS/F136JBW (32 Kbytes)



*: Programmer addresses are corresponding to CPU addresses, used when the parallel programmer programs data into Flash memory.
These programmer addresses are used for the parallel programmer to program or erase data in Flash memory.

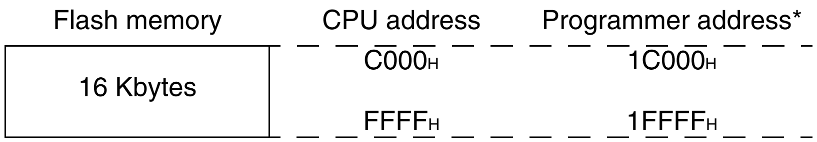
• Programming method

1) Set the type code of the parallel programmer to “17237”.

2) Load program data to programmer addresses 18000_H to $1FFFF_H$.

3) Write data with the parallel programmer.

• MB95F134MBS/F134NBS/F134JBS/F134MBW/F134NBW/F134JBW (16 Kbytes)



*: Programmer addresses are corresponding to CPU addresses, used when the parallel programmer programs data into Flash memory.
These programmer addresses are used for the parallel programmer to program or erase data in Flash memory.

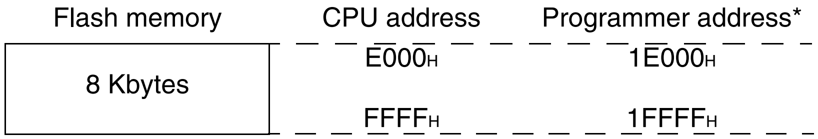
• Programming method

1) Set the type code of the parallel programmer to “17237”.

2) Load program data to programmer addresses $1C000_H$ to $1FFFF_H$.

3) Write data with the parallel programmer.

- MB95F133MBS/F133NBS/F133JBS/F133MBW/F133NBW/F133JBW (8 Kbytes)

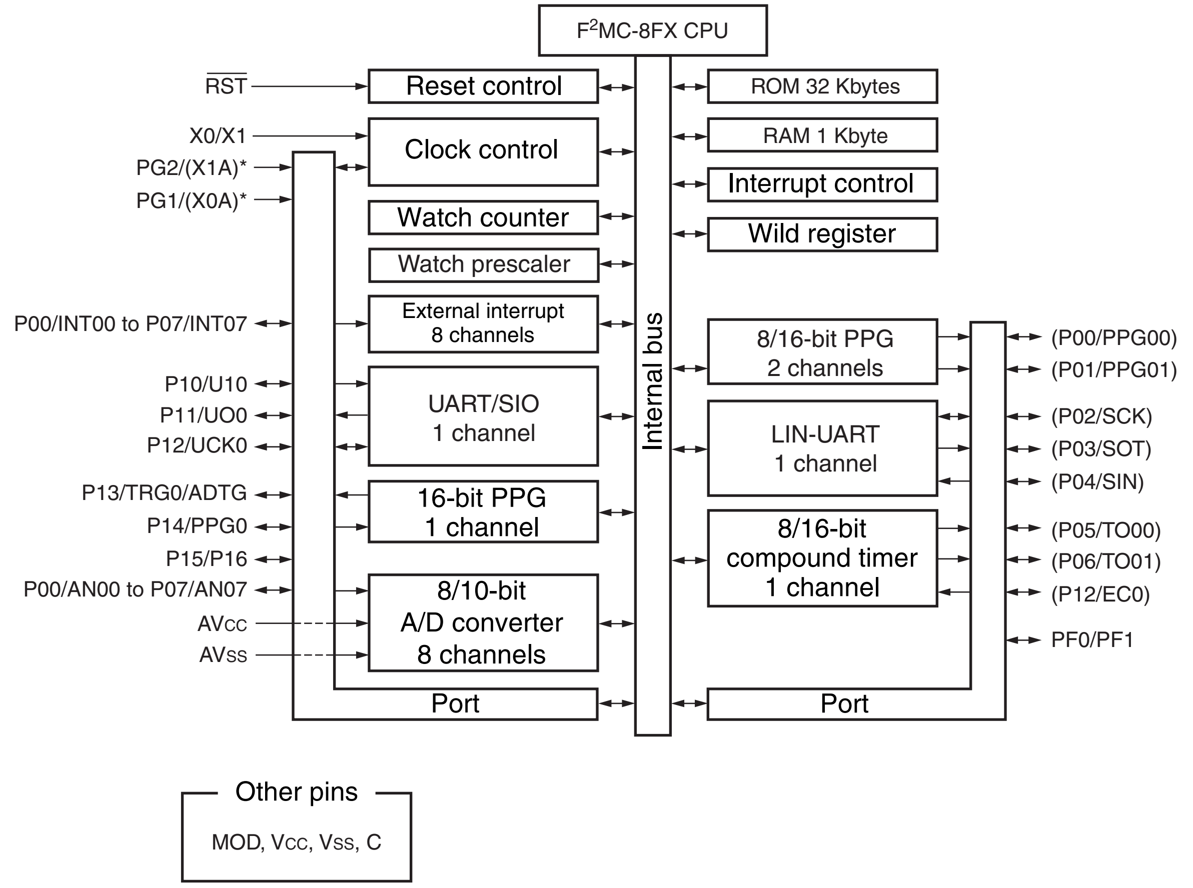

Flash memory
CPU address
Programmer address*
8 Kbytes
$E000_H$
$1E000_H$
$FFFF_H$
$1FFFF_H$

*: Programmer addresses are corresponding to CPU addresses, used when the parallel programmer programs data into Flash memory.
These programmer addresses are used for the parallel programmer to program or erase data in Flash memory.

- **Programming method**

1) Set the type code of the parallel programmer to “17237”.
2) Load program data to programmer addresses $1E000_H$ to $1FFFF_H$.
3) Write data with the parallel programmer.

■ BLOCK DIAGRAM


F²MC-8FX CPU
RST
Reset control
ROM 32 Kbytes
X0/X1
Clock control
RAM 1 Kbyte
PG2/(X1A)*
PG1/(X0A)*
Interrupt control
Watch counter
Wild register
Watch prescaler
P00/INT00 to P07/INT07
External interrupt
8 channels
Internal bus
8/16-bit PPG
2 channels
(P00/PPG00)
(P01/PPG01)
P10/U10
P11/UO0
P12/UCK0
UART/SIO
1 channel
LIN-UART
1 channel
(P02/SCK)
(P03/SOT)
(P04/SIN)
P13/TRG0/ADTG
P14/PPG0
P15/P16
16-bit PPG
1 channel
8/16-bit
compound timer
1 channel
(P05/TO00)
(P06/TO01)
(P12/EC0)
P00/AN00 to P07/AN07
AVcc
AVss
8/10-bit
A/D converter
8 channels
PF0/PF1
Port
Port
Other pins
MOD, Vcc, Vss, C

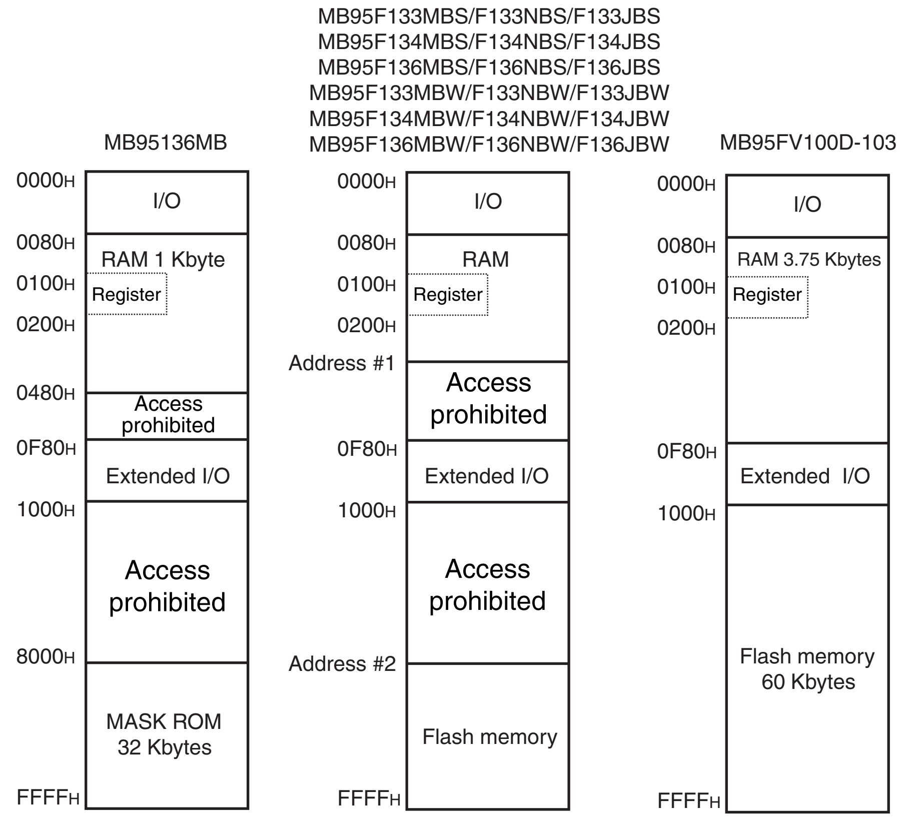
*: Single clock product is a general-purpose port, and dual clock product is a sub clock oscillation pin.

■ CPU CORE

1. Memory Space

Memory space of the MB95130MB series is 64 Kbytes and consists of I/O area, data area, and program area. The memory space includes special-purpose areas such as the general-purpose registers and vector table. Memory map of the MB95130MB series is shown below.

- Memory Map

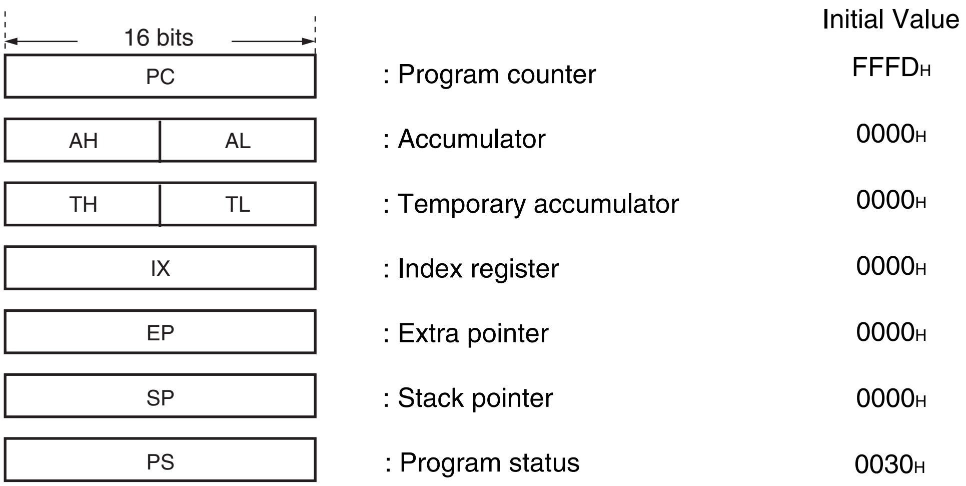

MB95136MB
0000H
I/O
0080H
RAM 1 Kbyte
0100H
Register
0200H
0480H
Access prohibited
0F80H
Extended I/O
1000H
Access prohibited
8000H
MASK ROM 32 Kbytes
FFFFH
MB95F133MBS/F133NBS/F133JBS
MB95F134MBS/F134NBS/F134JBS
MB95F136MBS/F136NBS/F136JBS
MB95F133MBW/F133NBW/F133JBW
MB95F134MBW/F134NBW/F134JBW
MB95F136MBW/F136NBW/F136JBW
0000H
I/O
0080H
RAM
0100H
Register
0200H
Address #1
Access prohibited
0F80H
Extended I/O
1000H
Access prohibited
Address #2
Flash memory
FFFFH
MB95FV100D-103
0000H
I/O
0080H
RAM 3.75 Kbytes
0100H
Register
0200H
0F80H
Extended I/O
1000H
Flash memory 60 Kbytes
FFFFH

	Flash memory	RAM	Address #1	Address #2
MB95F133MBS/F133NBS/F133JBS MB95F133MBW/F133NBW/F133JBW	8 Kbytes	256 bytes	0180H	E000H
MB95F134MBS/F134NBS/F134JBS MB95F134MBW/F134NBW/F134JBW	16 Kbytes	512 bytes	0280H	C000H
MB95F136MBS/F136NBS/F136JBS MB95F136MBW/F136NBW/F136JBW	32 Kbytes	1 Kbyte	0480H	8000H

2. Register

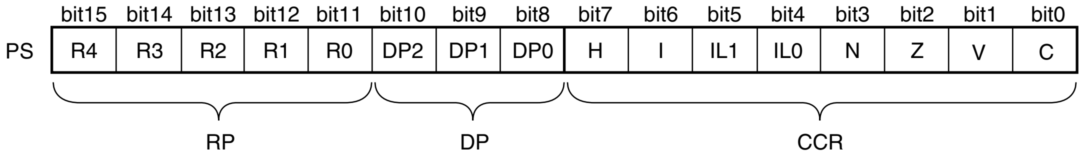
The MB95130MB series has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The dedicated registers are as include:

Program counter (PC)	: A 16-bit register to indicate locations where instructions are stored.
Accumulator (A)	: A 16-bit register for temporary storage of arithmetic operations. In the case of an 8-bit data processing instruction, the lower 1-byte is used.
Temporary accumulator (T)	: A 16-bit register which performs arithmetic operations with the accumulator. In the case of an 8-bit data processing instruction, the lower 1-byte is used.
Index register (IX)	: A 16-bit register for index modification
Extra pointer (EP)	: A 16-bit pointer to point to a memory address.
Stack pointer (SP)	: A 16-bit register to indicate a stack area.
Program status (PS)	: A 16-bit register for storing a register bank pointer, a direct bank pointer, and a condition code register


16 bits
Initial Value
PC
: Program counter
FFFDH
AH
AL
: Accumulator
0000H
TH
TL
: Temporary accumulator
0000H
IX
: Index register
0000H
EP
: Extra pointer
0000H
SP
: Stack pointer
0000H
PS
: Program status
0030H

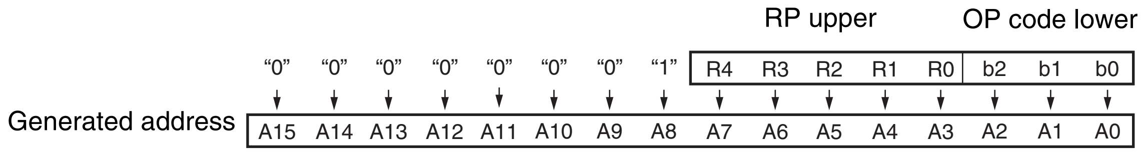
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and a direct bank pointer (DP) and the lower 8 bits for use as a condition code register (CCR). (Refer to the diagram below.)

- Structure of the program status


bit15
bit14
bit13
bit12
bit11
bit10
bit9
bit8
bit7
bit6
bit5
bit4
bit3
bit2
bit1
bit0
PS
R4
R3
R2
R1
R0
DP2
DP1
DP0
H
I
IL1
IL0
N
Z
V
C
RP
DP
CCR

The RP indicates the address of the register bank currently being used. The relationship between the content of RP and the real address conforms to the conversion rule illustrated below:

- Rule for Conversion of Actual Addresses in the General-purpose Register Area



The DP specifies the area for mapping instructions (16 different types of instructions such as MOV A and dir) using direct addresses to 0080$_H$ to 00FF$_H$.

Direct bank pointer (DP2 to DP0)	Specified address area	Mapping area
XXX$_B$ (no effect to mapping)	0000$_H$ to 007F$_H$	0000$_H$ to 007F$_H$ (without mapping)
000$_B$ (initial value)	0080$_H$ to 00FF$_H$	0080$_H$ to 00FF$_H$ (without mapping)
001$_B$		0100$_H$ to 017F$_H$
010$_B$		0180$_H$ to 01FF$_H$
011$_B$		0200$_H$ to 027F$_H$
100$_B$		0280$_H$ to 02FF$_H$
101$_B$		0300$_H$ to 037F$_H$
110$_B$		0380$_H$ to 03FF$_H$
111$_B$		0400$_H$ to 047F$_H$

The CCR consists of the bits indicating arithmetic operation results or transfer data content and the bits that control CPU operations at interrupt.

H flag : Set to "1" when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared to "0" otherwise. This flag is for decimal adjustment instructions.

I flag : Interrupt is enabled when this flag is set to "1". Interrupt is disabled when this flag is set to "0". The flag is cleared to "0" when reset.

IL1, IL0 : Indicates the level of the interrupt currently enabled. Processes an interrupt only if its request level is higher than the value indicated by these bits.

IL1	IL0	Interrupt level	Priority
0	0	0	High ↕ Low (no interruption)
0	1	1	
1	0	2	
1	1	3	

N flag : Set to "1" if the MSB is set to "1" as the result of an arithmetic operation. Cleared to "0" when the bit is set to "0".

Z flag : Set to "1" when an arithmetic operation results in "0". Cleared to "0" otherwise.

V flag : Set to "1" if the complement on 2 overflows as a result of an arithmetic operation. Cleared to "0" otherwise.

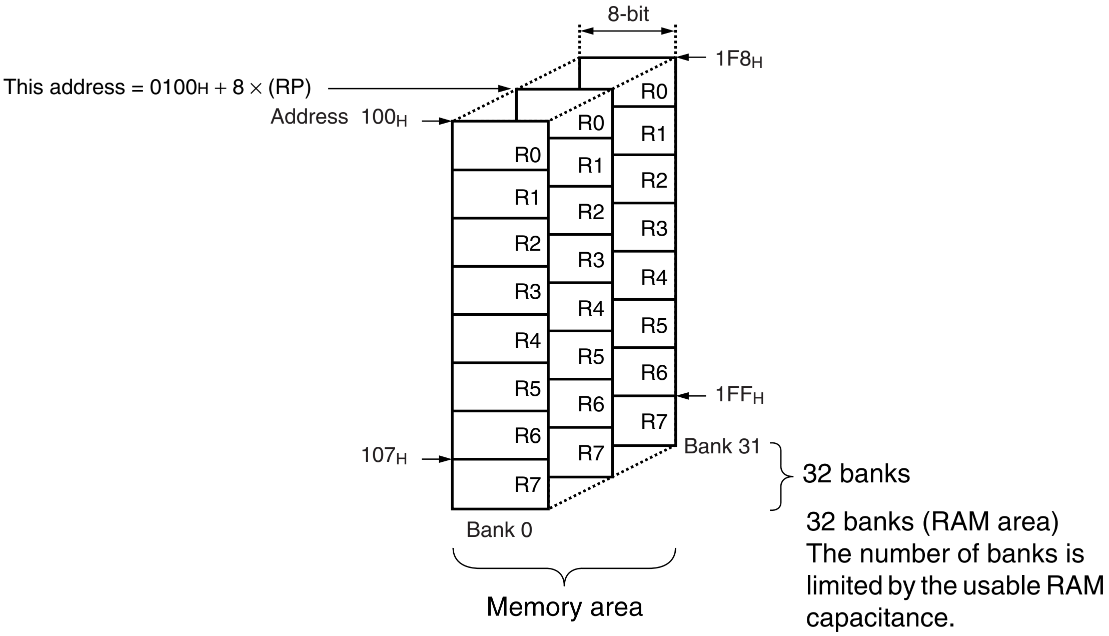
C flag : Set to "1" when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared to "0" otherwise. Set to the shift-out value in the case of a shift instruction.

The following general-purpose registers are provided:

General-purpose registers: 8-bit data storage registers

The general-purpose registers are 8 bits and located in the register banks on the memory. 1-bank contains 8 registers. Up to a total of 32 banks can be used on the MB95130MB series. The bank currently in use is specified by the register bank pointer (RP), and the lower 3 bits of OP code indicates the general-purpose register 0 (R0) to general-purpose register 7 (R7).

- Register Bank Configuration


8-bit
1F8H
This address = 0100H + 8 × (RP)
Address 100H
R0
R1
R2
R3
R4
R5
R6
R7
1FFH
107H
Bank 31
Bank 0
32 banks
Memory area

32 banks (RAM area)
The number of banks is limited by the usable RAM capacitance.

■ I/O MAP

Address	Register abbreviation	Register name	R/W	Initial value
0000H	PDR0	Port 0 data register	R/W	00000000B
0001H	DDR0	Port 0 direction register	R/W	00000000B
0002H	PDR1	Port 1 data register	R/W	00000000B
0003H	DDR1	Port 1 direction register	R/W	00000000B
0004H	—	(Disabled)	—	—
0005H	WATR	Oscillation stabilization wait time setting register	R/W	11111111B
0006H	PLLC	PLL control register	R/W	00000000B
0007H	SYCC	System clock control register	R/W	1010X011B
0008H	STBC	Standby control register	R/W	00000000B
0009H	RSRR	Reset source register	R/W	XXXXXXXXB
000AH	TBTC	Timebase timer control register	R/W	00000000B
000BH	WPCR	Watch prescaler control register	R/W	00000000B
000CH	WDTC	Watchdog timer control register	R/W	00000000B
000DH to 0027H	—	(Disabled)	—	—
0028H	PDRF	Port F data register	R/W	00000000B
0029H	DDRF	Port F direction register	R/W	00000000B
002AH	PDRG	Port G data register	R/W	00000000B
002BH	DDRG	Port G direction register	R/W	00000000B
002CH	PUL0	Port 0 pull-up register	R/W	00000000B
002DH	PUL1	Port 1 pull-up register	R/W	00000000B
002EH to 0034H	—	(Disabled)	—	—
0035H	PULG	Port G pull-up register	R/W	00000000B
0036H	T01CR1	8/16-bit compound timer 01 control status register 1 ch.0	R/W	00000000B
0037H	T00CR1	8/16-bit compound timer 00 control status register 1 ch.0	R/W	00000000B
0038H, 0039H	—	(Disabled)	—	—
003AH	PC01	8/16-bit PPG1 control register ch.0	R/W	00000000B
003BH	PC00	8/16-bit PPG0 control register ch.0	R/W	00000000B
003CH to 0041H	—	(Disabled)	—	—
0042H	PCNTH0	16-bit PPG control status register (Upper byte) ch.0	R/W	00000000B
0043H	PCNTL0	16-bit PPG control status register (Lower byte) ch.0	R/W	00000000B

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0044H to 0047H	—	(Disabled)	—	—
0048H	EIC00	External interrupt circuit control register ch.0,ch.1	R/W	00000000B
0049H	EIC10	External interrupt circuit control register ch.2,ch.3	R/W	00000000B
004AH	EIC20	External interrupt circuit control register ch.4,ch.5	R/W	00000000B
004BH	EIC30	External interrupt circuit control register ch.6,ch.7	R/W	00000000B
004CH to 004FH	—	(Disabled)	—	—
0050H	SCR	LIN-UART serial control register	R/W	00000000B
0051H	SMR	LIN-UART serial mode register	R/W	00000000B
0052H	SSR	LIN-UART serial status register	R/W	00001000B
0053H	RDR/TDR	LIN-UART reception/transmission data register	R/W	00000000B
0054H	ESCR	LIN-UART extended status control register	R/W	00000100B
0055H	ECCR	LIN-UART extended communication control register	R/W	000000XXB
0056H	SMC10	UART/SIO serial mode control register 1 ch.0	R/W	00000000B
0057H	SMC20	UART/SIO serial mode control register 2 ch.0	R/W	00100000B
0058H	SSR0	UART/SIO serial status register ch.0	R/W	00000001B
0059H	TDR0	UART/SIO serial output data register ch.0	R/W	00000000B
005AH	RDR0	UART/SIO serial input data register ch.0	R	00000000B
005BH to 006BH	—	(Disabled)	—	—
006CH	ADC1	8/10-bit A/D converter control register 1	R/W	00000000B
006DH	ADC2	8/10-bit A/D converter control register 2	R/W	00000000B
006EH	ADDH	8/10-bit A/D converter data register (Upper byte)	R/W	00000000B
006FH	ADDL	8/10-bit A/D converter data register (Lower byte)	R/W	00000000B
0070H	WCSR	Watch counter status register	R/W	00000000B
0071H	—	(Disabled)	—	—
0072H	FSR	Flash memory status register	R/W	000X0000B
0073H	—	(Disabled)	—	—
0074H	—	(Disabled)	—	—
0075H	—	(Disabled)	—	—
0076H	WREN	Wild register address compare enable register	R/W	00000000B
0077H	WROR	Wild register data test setting register	R/W	00000000B

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0078$_H$	—	(Register bank pointer (RP) Mirror of direct bank pointer (DP)	—	—
0079$_H$	ILR0	Interrupt level setting register 0	R/W	11111111$_B$
007A$_H$	ILR1	Interrupt level setting register 1	R/W	11111111$_B$
007B$_H$	ILR2	Interrupt level setting register 2	R/W	11111111$_B$
007C$_H$	ILR3	Interrupt level setting register 3	R/W	11111111$_B$
007D$_H$	ILR4	Interrupt level setting register 4	R/W	11111111$_B$
007E$_H$	ILR5	Interrupt level setting register 5	R/W	11111111$_B$
007F$_H$	—	(Disabled)	—	—
0F80$_H$	WRARH0	Wild register address setting register (Upper byte) ch.0	R/W	00000000$_B$
0F81$_H$	WRARL0	Wild register address setting register (Lower byte) ch.0	R/W	00000000$_B$
0F82$_H$	WRDR0	Wild register data setting register ch.0	R/W	00000000$_B$
0F83$_H$	WRARH1	Wild register address setting register (Upper byte) ch.1	R/W	00000000$_B$
0F84$_H$	WRARL1	Wild register address setting register (Lower byte) ch.1	R/W	00000000$_B$
0F85$_H$	WRDR1	Wild register data setting register ch.1	R/W	00000000$_B$
0F86$_H$	WRARH2	Wild register address setting register (Upper byte) ch.2	R/W	00000000$_B$
0F87$_H$	WRARL2	Wild register address setting register (Lower byte) ch.2	R/W	00000000$_B$
0F88$_H$	WRDR2	Wild register data setting register ch.2	R/W	00000000$_B$
0F89$_H$ to 0F91$_H$	—	(Disabled)	—	—
0F92$_H$	T01CR0	8/16-bit compound timer 01 control status register 0 ch.0	R/W	00000000$_B$
0F93$_H$	T00CR0	8/16-bit compound timer 00 control status register 0 ch.0	R/W	00000000$_B$
0F94$_H$	T01DR	8/16-bit compound timer 01 data register ch.0	R/W	00000000$_B$
0F95$_H$	T00DR	8/16-bit compound timer 00 data register ch.0	R/W	00000000$_B$
0F96$_H$	TMCR0	8/16-bit compound timer 00/01 timer mode control register ch.0	R/W	00000000$_B$
0F97$_H$ to 0F9B$_H$	—	(Disabled)	—	—
0F9C$_H$	PPS01	8/16-bit PPG1 cycle setting buffer register ch.0	R/W	11111111$_B$
0F9D$_H$	PPS00	8/16-bit PPG0 cycle setting buffer register ch.0	R/W	11111111$_B$
0F9E$_H$	PDS01	8/16-bit PPG1 duty setting buffer register ch.0	R/W	11111111$_B$
0F9F$_H$	PDS00	8/16-bit PPG0 duty setting buffer register ch.0	R/W	11111111$_B$
0FA0$_H$ to 0FA3$_H$	—	(Disabled)	—	—

(Continued)

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0FA4$_H$	PPGS	8/16-bit PPG start register	R/W	00000000$_B$
0FA5$_H$	REVC	8/16-bit PPG output inversion register	R/W	00000000$_B$
0FA6$_H$ to 0FA9$_H$	—	(Disabled)	—	—
0FAA$_H$	PDCRH0	16-bit PPG down counter register (Upper byte) ch.0	R	00000000$_B$
0FAB$_H$	PDCRL0	16-bit PPG down counter register (Lower byte) ch.0	R	00000000$_B$
0FAC$_H$	PCSRH0	16-bit PPG cycle setting buffer register (Upper byte) ch.0	R/W	11111111$_B$
0FAD$_H$	PCSRL0	16-bit PPG cycle setting buffer register (Lower byte) ch.0	R/W	11111111$_B$
0FAE$_H$	PDUTH0	16-bit PPG duty setting buffer register (Upper byte) ch.0	R/W	11111111$_B$
0FAF$_H$	PDUTL0	16-bit PPG duty setting buffer register (Lower byte) ch.0	R/W	11111111$_B$
0FB0$_H$ to 0FBB$_H$	—	(Disabled)	—	—
0FBC$_H$	BGR1	LIN-UART baud rate generator register 1	R/W	00000000$_B$
0FBD$_H$	BGR0	LIN-UART baud rate generator register 0	R/W	00000000$_B$
0FBE$_H$	PSSR0	UART/SIO dedicated baud rate generator prescaler selection register ch.0	R/W	00000000$_B$
0FBF$_H$	BRSR0	UART/SIO dedicated baud rate generator baud rate setting register ch.0	R/W	00000000$_B$
0FC0$_H$ to 0FC2$_H$	—	(Disabled)	—	—
0FC3$_H$	AIDRL	A/D input disable register (Lower byte)	R/W	00000000$_B$
0FC4$_H$ to 0FE2$_H$	—	(Disabled)	—	—
0FE3$_H$	WCDR	Watch counter data register	R/W	00111111$_B$
0FE4$_H$ to 0FE6$_H$	—	(Disabled)	—	—
0FE7$_H$	ILSR2	Input level select register 2 (option)	R/W	00000000$_B$
0FE8$_H$, 0FE9$_H$	—	(Disabled)	—	—
0FEA$_H$	CSVCR	Clock supervisor control register	R/W	00011100$_B$
0FEB$_H$ to 0FED$_H$	—	(Disabled)	—	—
0FEE$_H$	ILSR	Input level select register	R/W	00000000$_B$
0FEF$_H$	WICR	Interrupt pin control register	R/W	01000000$_B$
0FF0$_H$ to 0FFF$_H$	—	(Disabled)	—	—

- R/W access symbols

  R/W : Readable / Writable
  R : Read only
  W : Write only

- Initial value symbols

  0 : The initial value of this bit is “0”.
  1 : The initial value of this bit is “1”.
  X : The initial value of this bit is undefined.

Note: : Do not write to the “ (Disabled) ”. Reading the “ (Disabled) ” returns an undefined value.

■ INTERRUPT SOURCE TABLE

Interrupt source	Interrupt request number	Vector table address		Bit name of interrupt level setting register	Same level priority order (at simultaneous occurrence)
		Upper	Lower		
External interrupt ch.0	IRQ0	FFFA$_{H}$	FFFB$_{H}$	L00 [1 : 0]	High
External interrupt ch.4					
External interrupt ch.1	IRQ1	FFF8$_{H}$	FFF9$_{H}$	L01 [1 : 0]	
External interrupt ch.5					
External interrupt ch.2	IRQ2	FFF6$_{H}$	FFF7$_{H}$	L02 [1 : 0]	
External interrupt ch.6					
External interrupt ch.3	IRQ3	FFF4$_{H}$	FFF5$_{H}$	L03 [1 : 0]	
External interrupt ch.7					
UART/SIO ch.0	IRQ4	FFF2$_{H}$	FFF3$_{H}$	L04 [1 : 0]	
8/16-bit compound timer ch.0 (Lower)	IRQ5	FFF0$_{H}$	FFF1$_{H}$	L05 [1 : 0]	
8/16-bit compound timer ch.0 (Higher)	IRQ6	FFEE$_{H}$	FFEF$_{H}$	L06 [1 : 0]	
LIN-UART (reception)	IRQ7	FFEC$_{H}$	FFED$_{H}$	L07 [1 : 0]	
LIN-UART (transmission)	IRQ8	FFEA$_{H}$	FFEB$_{H}$	L08 [1 : 0]	
(Unused)	IRQ9	FFE8$_{H}$	FFE9$_{H}$	L09 [1 : 0]	
(Unused)	IRQ10	FFE6$_{H}$	FFE7$_{H}$	L10 [1 : 0]	
(Unused)	IRQ11	FFE4$_{H}$	FFE5$_{H}$	L11 [1 : 0]	
8/16-bit PPG ch.0 (Upper)	IRQ12	FFE2$_{H}$	FFE3$_{H}$	L12 [1 : 0]	
8/16-bit PPG ch.0 (Lower)	IRQ13	FFE0$_{H}$	FFE1$_{H}$	L13 [1 : 0]	
(Unused)	IRQ14	FFDE$_{H}$	FFDF$_{H}$	L14 [1 : 0]	
16-bit PPG ch.0	IRQ15	FFDC$_{H}$	FFDD$_{H}$	L15 [1 : 0]	
(Unused)	IRQ16	FFDA$_{H}$	FFDB$_{H}$	L16 [1 : 0]	
(Unused)	IRQ17	FFD8$_{H}$	FFD9$_{H}$	L17 [1 : 0]	
8/10-bit A/D converter	IRQ18	FFD6$_{H}$	FFD7$_{H}$	L18 [1 : 0]	
Timebase timer	IRQ19	FFD4$_{H}$	FFD5$_{H}$	L19 [1 : 0]	
Watch prescaler/Watch counter	IRQ20	FFD2$_{H}$	FFD3$_{H}$	L20 [1 : 0]	
(Unused)	IRQ21	FFD0$_{H}$	FFD1$_{H}$	L21 [1 : 0]	
(Unused)	IRQ22	FFCE$_{H}$	FFCF$_{H}$	L22 [1 : 0]	
Flash memory	IRQ23	FFCC$_{H}$	FFCD$_{H}$	L23 [1 : 0]	Low

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC} AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*2
Input voltage*1	V_{I}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*3
Output voltage*1	V_{O}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*3
Maximum clamp current	I_{CLAMP}	– 2.0	+ 2.0	mA	Applicable to pins*4
Total maximum clamp current	$\Sigma\lvert I_{CLAMP}\rvert$	—	20	mA	Applicable to pins*4
"L" level maximum output current	I_{OL1}	—	15	mA	Other than PF0, PF1
	I_{OL2}		15		PF0, PF1
"L" level average current	I_{OLAV1}	—	4	mA	Other than PF0, PF1 Average output current = operating current × operating ratio (1 pin)
	I_{OLAV2}		12		PF0, PF1 Average output current = operating current × operating ratio (1 pin)
"L" level total maximum output current	ΣI_{OL}	—	100	mA	
"L" level total average output current	ΣI_{OLAV}	—	50	mA	Total average output current = operating current × operating ratio (Total of pins)
"H" level maximum output current	I_{OH1}	—	– 15	mA	Other than PF0, PF1
	I_{OH2}		– 15		PF0, PF1
"H" level average current	I_{OHAV1}	—	– 4	mA	Other than PF0, PF1 Average output current = operating current × operating ratio (1 pin)
	I_{OHAV2}		– 8		PF0, PF1 Average output current = operating current × operating ratio (1 pin)
"H" level total maximum output current	ΣI_{OH}	—	– 100	mA	
"H" level total average output current	ΣI_{OHAV}	—	– 50	mA	Total average output current = operating current × operating ratio (Total number of pins)
Power consumption	Pd	—	320	mW	
Operating temperature	T_{A}	– 40	+ 105	°C	
Storage temperature	Tstg	– 55	+ 150	°C	

(Continued)

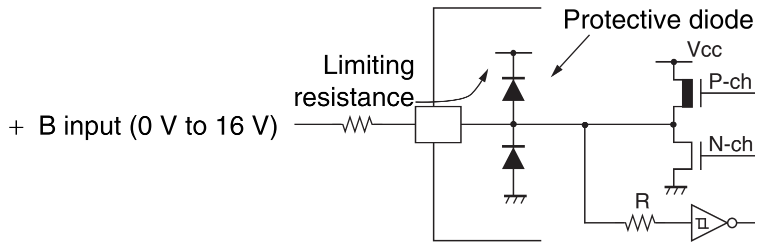
*1: These parameters are based on the condition that both AV_{SS} and V_{SS} are 0.0 V.

*2: Apply equal potential to AV_{CC} and V_{CC}.

*3: V_I and V_O should not exceed Vcc + 0.3 V. V_I must not exceed the rating voltage. However, if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

*4: Applicable pins: P10 to P15, PF0, PF1 (Inapplicable pins: PG1, PG2)
- Use within recommended operating conditions.
- Use at DC voltage (current).
- +B signal is an input signal that exceeds V_{CC} voltage. The + B signal should always be applied a limiting resistance placed between the + B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the + B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this affects other devices.
- Note that if the + B signal is inputted when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the + B input is applied during power-on, the power supply is provided from the pins and the resulting power supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the + B input pin open.
- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, etc.) cannot accept +B signal input.
- Sample recommended circuits :

- Input/Output Equivalent circuits



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

($AV_{SS} = V_{SS} = 0.0$ V)

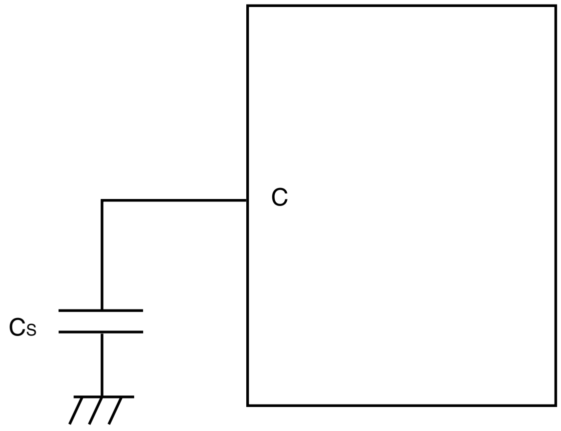
Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}, AV_{CC}	2.42*2	5.5*1	V	At normal operation
		2.3	5.5		Holds condition in stop mode
Smoothing capacitor	C_S	0.1	1.0	μF	*3
Operating temperature	T_A	− 40	+ 105	°C	

*1: The value varies depending on the operating frequency.

*2: The value is 2.88 V when the low-voltage detection reset is used.

*3: Use ceramic capacitor or a capacitor with equivalent frequency characteristics. A bypass capacitor of V_{CC} pin must have a capacitance value higher than C_S. For connection of smoothing capacitor C_S, refer to the diagram below.

- C pin connection diagram



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

3. DC Characteristics

(V_{CC} = = AV_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = – 40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IHI}	P04 (selectable in SIN), P10 (selectable in UI0)	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
	V_{IHSI}	P00 to P07, P10 to P16, PF0, PF1, PG1, PG2	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
	V_{IHA}	P00 to P07, P10 to P16, PF0, PF1, PG1, PG2	—	0.8 Vcc	—	V_{CC} + 0.3	V	Pin input at selecting of Automotive input level
	V_{IHM}	$\overline{RST}$, MOD	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	CMOS input (Flash memory product)
			—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input (MASK ROM product)
"L" level input voltage	V_{IL}	P04 (selectable in SIN), P10 (selectable in UI0)	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	Hysteresis input
	V_{ILS}	P00 to P07, P10 to P16, PF0, PF1, PG1, PG2	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	Hysteresis input
	V_{ILA}	P00 to P07, P10 to P16, PF0, PF1, PG1, PG2	—	V_{SS} – 0.3	—	0.5 V_{CC}	V	Pin input at selecting of Automotive input level
	V_{ILM}	$\overline{RST}$, MOD	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	CMOS input (Flash memory product)
			—	V_{SS} – 0.3	—	0.2 V_{CC}	V	Hysteresis input (MASK ROM product)
"H" level output voltage	V_{OH1}	Output pins other than PF0, PF1	I_{OH} = – 4.0 mA	V_{CC} – 0.5	—	—	V	
	V_{OH2}	PF0, PF1	I_{OH} = – 8.0 mA	V_{CC} – 0.5	—	—	V	
"L" level output voltage	V_{OL1}	Output pins other than PF0 to PF7, $\overline{RST}$[*1]	I_{OL} = 4.0 mA	—	—	0.4	V	
	V_{OL2}	PF0, PF1	I_{OL} = 12 mA	—	—	0.4	V	

(Continued)

($V_{CC} = AV_{CC} = 5.0$ V ± 10%, $AV_{SS} = V_{SS} = 0.0$ V, $T_A = -40$ °C to $+105$ °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input leakage current (Hi-Z output leakage current)	I_{LI}	P00 to P07, P10 to P16, PF0, PF1, PG1, PG2	$0.0\ \text{V} < V_I < V_{CC}$	− 5	—	+ 5	µA	When the pull-up prohibition setting
Pull-up resistor	R_{PULL}	P00 to P07, P10 to P16, PG1, PG2	$V_I = 0.0$ V	25	50	100	kΩ	When the pull-up permission setting
Pull-down resistor	R_{MOD}	MOD	$V_I = V_{CC}$	50	100	200	kΩ	MASK ROM product only
Input capacity	C_{IN}	Other than AV_{CC}, AV_{ss}, C, V_{cc} and V_{ss}	f = 1 MHz	—	5	15	pF	
Power supply current*2	I_{CC}	V_{CC} (External clock operation)	$V_{CC} = 5.5$ V $F_{CH} = 20$ MHz $F_{MP} = 10$ MHz Main clock mode (divided by 2)	—	9.5	12.5	mA	Flash memory product (at other than Flash memory writing and erasing)
				—	30	35	mA	Flash memory product (at Flash memory writing and erasing)
				—	7.2	9.5	mA	MASK ROM product
			$F_{CH} = 32$ MHz $F_{MP} = 16$ MHz Main clock mode (divided by 2)	—	15.2	20.0	mA	Flash memory product (at other than Flash memory writing and erasing)
				—	35.7	42.5	mA	Flash memory product (at Flash memory writing and erasing)
				—	11.6	15.2	mA	MASK ROM product

(Continued)

(V_{CC} = AV_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*2	I_{CCS}	V_{CC} (External clock operation)	V_{CC} = 5.5 V F_{CH} = 20 MHz F_{MP} = 10 MHz Main Sleep mode (divided by 2)	—	4.5	7.5	mA	
			F_{CH} = 32 MHz F_{MP} = 16 MHz Main Sleep mode (divided by 2)	—	7.2	12.0	mA	
	I_{CCL}		V_{CC} = 5.5 V F_{CL} = 32 kHz F_{MPL} = 16 kHz Sub clock mode (divided by 2) , T_A = + 25 °C	—	45	100	µA	Dual clock product only
	I_{CCLS}		V_{CC} = 5.5 V F_{CL} = 32 kHz F_{MPL} = 16 kHz Sub sleep mode (divided by 2) , T_A = + 25 °C	—	10	81	µA	Dual clock product only
	I_{CCT}		V_{CC} = 5.5 V F_{CL} = 32 kHz Watch mode Main stop mode T_A = + 25 °C	—	4.6	27	µA	Dual clock product only
	I_{CCMPLL}		V_{CC} = 5.5 V F_{CH} = 4 MHz F_{MP} = 10 MHz Main PLL mode (multiplied by 2.5)	—	9.3	12.5	mA	Flash memory product
				—	7	9.5	mA	MASK ROM product
			F_{CH} = 6.4 MHz F_{MP} = 16 MHz Main PLL mode (multiplied by 2.5)	—	14.9	20.0	mA	Flash memory product
				—	11.2	15.2	mA	MASK ROM product
	I_{CCSPLL}		V_{CC} = 5.5 V F_{CL} = 32 kHz F_{MPL} = 128 kHz Sub PLL mode (multiplied by 4) , T_A = + 25 °C	—	160	400	µA	Dual clock product only

(Continued)

(V_{CC} = AV_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*2	I_{CTS}	V_{CC} (External clock operation)	V_{CC} = 5.5 V F_{CH} = 10 MHz Timebase timer mode T_A = + 25 °C	—	0.15	1.1	mA	
	I_{CCH}		V_{CC} = 5.5 V Sub stop mode T_A = + 25 °C	—	3.5	20.0	µA	Main stop mode for single clock product
	I_A	AV_{cc}	V_{CC} = 5.5 V F_{CH} = 16 MHz When A/D conversion is in operation	—	2.4	4.7	mA	
	I_{AH}		V_{CC} = 5.5 V F_{CH} = 16 MHz When A/D conversion is stopped T_A = + 25 °C	—	1	5	µA	

*1: Product without clock supervisor only

*2:
- The power supply current is specified by the external clock. When the low-voltage detection and clock supervisor options are selected, the consumption current values of both the low-voltage detection circuit (I_{LVD}) and the built-in CR oscillator (I_{CSV}) must also be added to the power supply current value.
- Refer to “4. AC Characteristics: (1) Clock Timing” for F_{CH} and F_{CL}.
- Refer to “4. AC Characteristics: (2) Source Clock / Machine Clock” for F_{MP} and F_{MPL}.

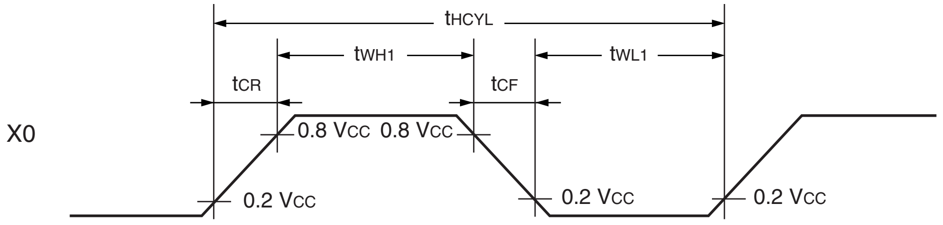
4. AC Characteristics

(1) Clock Timing

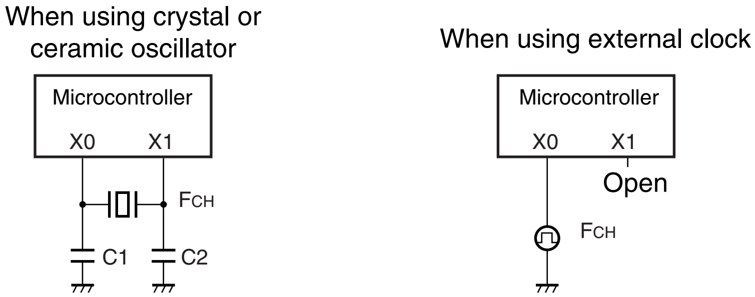
(V_{CC} = 2.42 V to 5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_{CH}	X0, X1	—	1.00	—	16.25	MHz	When using main oscillation circuit
				1.00	—	32.50	MHz	When using external clock
				3.00	—	10.00	MHz	Main PLL multiplied by 1
				3.00	—	8.13	MHz	Main PLL multiplied by 2
				3.00	—	6.50	MHz	Main PLL multiplied by 2.5
				3.00	—	4.06	MHz	Main PLL multiplied by 4
	F_{CL}	X0A, X1A		—	32.768	—	kHz	When using sub oscillation circuit
				—	32.768	—	kHz	When using sub PLL V_{CC} = 2.3 V to 3.6 V
Clock cycle time	t_{HCYL}	X0, X1		61.5	—	1000	ns	When using main oscillation circuit
				30.8	—	1000	ns	When using external clock
	t_{LCYL}	X0A, X1A		—	30.5	—	µs	When using sub oscillation circuit
Input clock pulse width	t_{WH1} t_{WL1}	X0		61.5	—	—	ns	When using external clock duty ratio is about 30% to 70%.
	t_{WH2} t_{WL2}	X0A		—	15.2	—	µs	
Input clock rise/fall time	t_{CR} t_{CF}	X0, X0A		—	—	5	ns	When using external clock

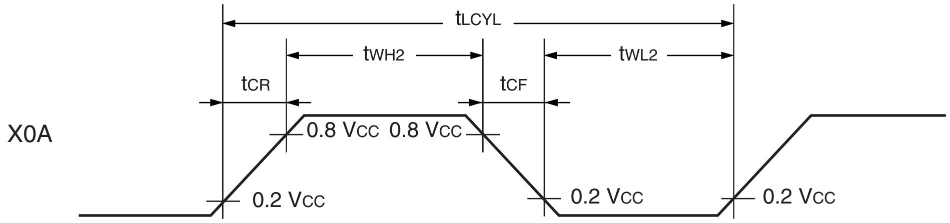
- Input wave form for using external clock (main clock)


tHCYL
tWH1
tWL1
tCR
tCF
X0
0.8 VCC
0.8 VCC
0.2 VCC
0.2 VCC
0.2 VCC

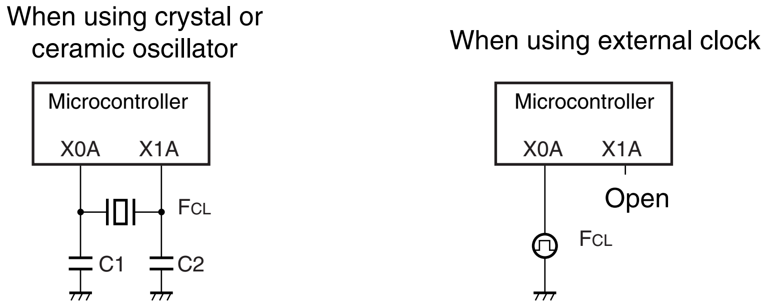
- Figure of Main Clock Input Port External Connection


When using crystal or ceramic oscillator
Microcontroller
X0
X1
FCH
C1
C2
When using external clock
Microcontroller
X0
X1
Open
FCH

- Input wave form for using external clock (sub clock)


tLCYL
tWH2
tWL2
tCR
tCF
X0A
0.8 VCC
0.8 VCC
0.2 VCC
0.2 VCC
0.2 VCC

- Figure of Sub clock Input Port External Connection


When using crystal or ceramic oscillator
Microcontroller
X0A
X1A
FCL
C1
C2
When using external clock
Microcontroller
X0A
X1A
Open
FCL

(2) Source Clock / Machine Clock

(V_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Source clock cycle time*1 (Clock before setting division)	t_{SCLK}	—	61.5	—	2000	ns	When using main clock Min : F_{CH} = 8.125 MHz, PLL multiplied by 2 Max : F_{CH} = 1 MHz, divided by 2
			7.6	—	61.0	µs	When using sub clock Min : F_{CL} = 32 kHz, PLL multiplied by 4 Max : F_{CL} = 32 kHz, divided by 2
Source clock frequency	F_{SP}	—	0.50	—	16.25	MHz	When using main clock
	F_{SPL}	—	16.384	—	131.072	kHz	When using sub clock
Machine clock cycle time*2 (Minimum instruction execution time)	t_{MCLK}	—	61.5	—	32000	ns	When using main clock Min : F_{SP} = 16.25 MHz, no division Max : F_{SP} = 0.5 MHz, divided by 16
			7.6	—	976.5	µs	When using sub clock Min : F_{SPL} = 131 kHz, no division Max : F_{SPL} = 16 kHz, divided by 16
Machine clock frequency	F_{MP}	—	0.031	—	16.250	MHz	When using main clock
	F_{MPL}		1.024	—	131.072	kHz	When using sub clock

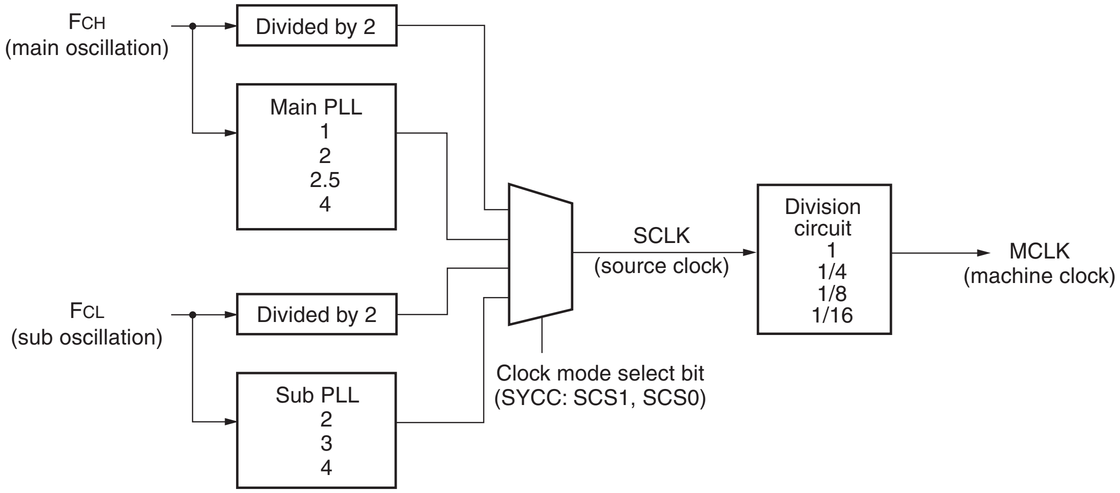
*1 : Clock before setting division due to machine clock division ratio selection bit (SYCC : DIV1 and DIV0) . This source clock is divided by the machine clock division ratio selection bit (SYCC : DIV1 and DIV0) , and it becomes the machine clock. Further, the source clock can be selected as follows.

- Main clock divided by 2
- PLL multiplication of main clock (select from 1, 2, 2.5, 4 multiplication)
- Sub clock divided by 2
- PLL multiplication of sub clock (select from 2, 3, 4 multiplication)

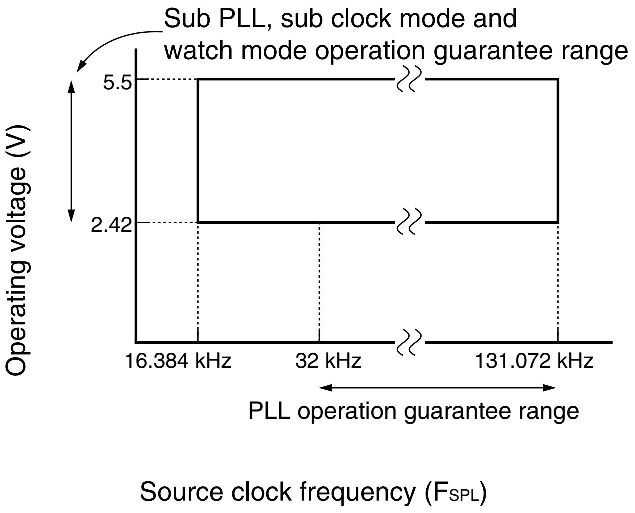
*2 : Operation clock of the microcontroller. Machine clock can be selected as follows.

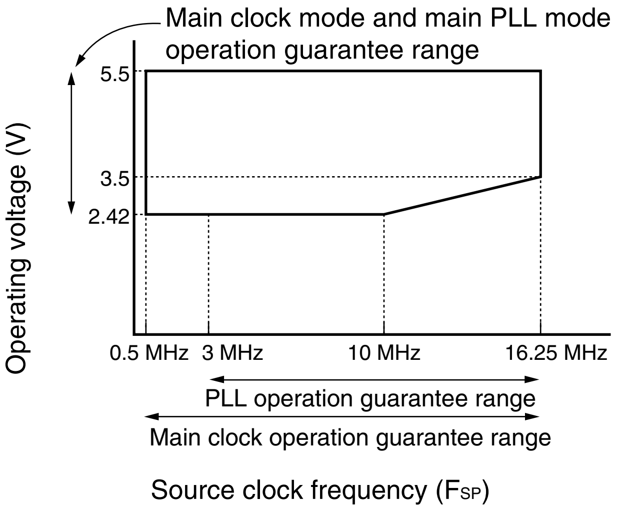
- Source clock (no division)
- Source clock divided by 4
- Source clock divided by 8
- Source clock divided by 16

- Outline of clock generation block

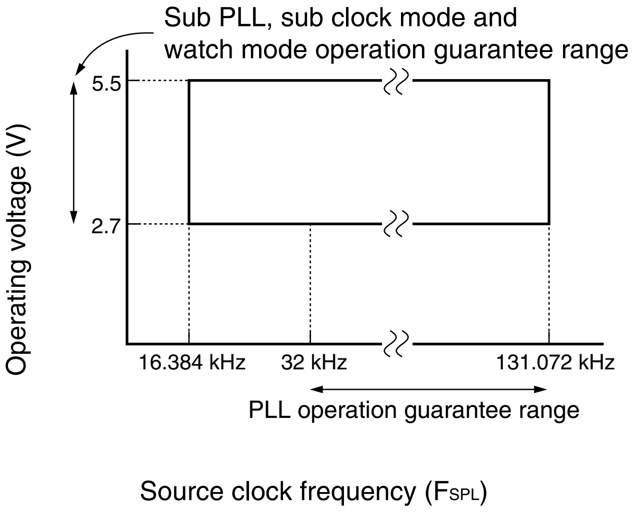

FCH
(main oscillation)
Divided by 2
Main PLL
1
2
2.5
4
FCL
(sub oscillation)
Divided by 2
Sub PLL
2
3
4
SCLK
(source clock)
Clock mode select bit
(SYCC: SCS1, SCS0)
Division
circuit
1
1/4
1/8
1/16
MCLK
(machine clock)

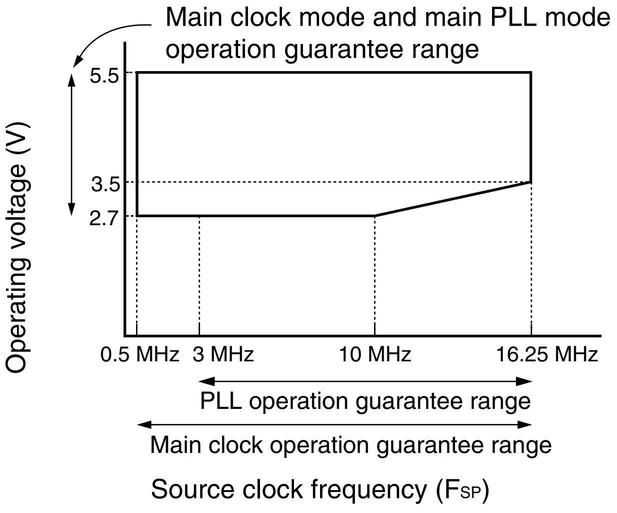
- Operating voltage - Operating frequency (When $T_A = -40$ °C to $+105$ °C)
  - MB95136MB/F133MBS/F133NBS/F133JBS/F134MBS/F134NBS/F134JBS/F136MBS/F136NBS/F136JBS/ MB95F133MBW/F133NBW/F133JBW/F134MBW/F134NBW/F134JBW/F136MBW/F136NBW/ MB95F136JBW



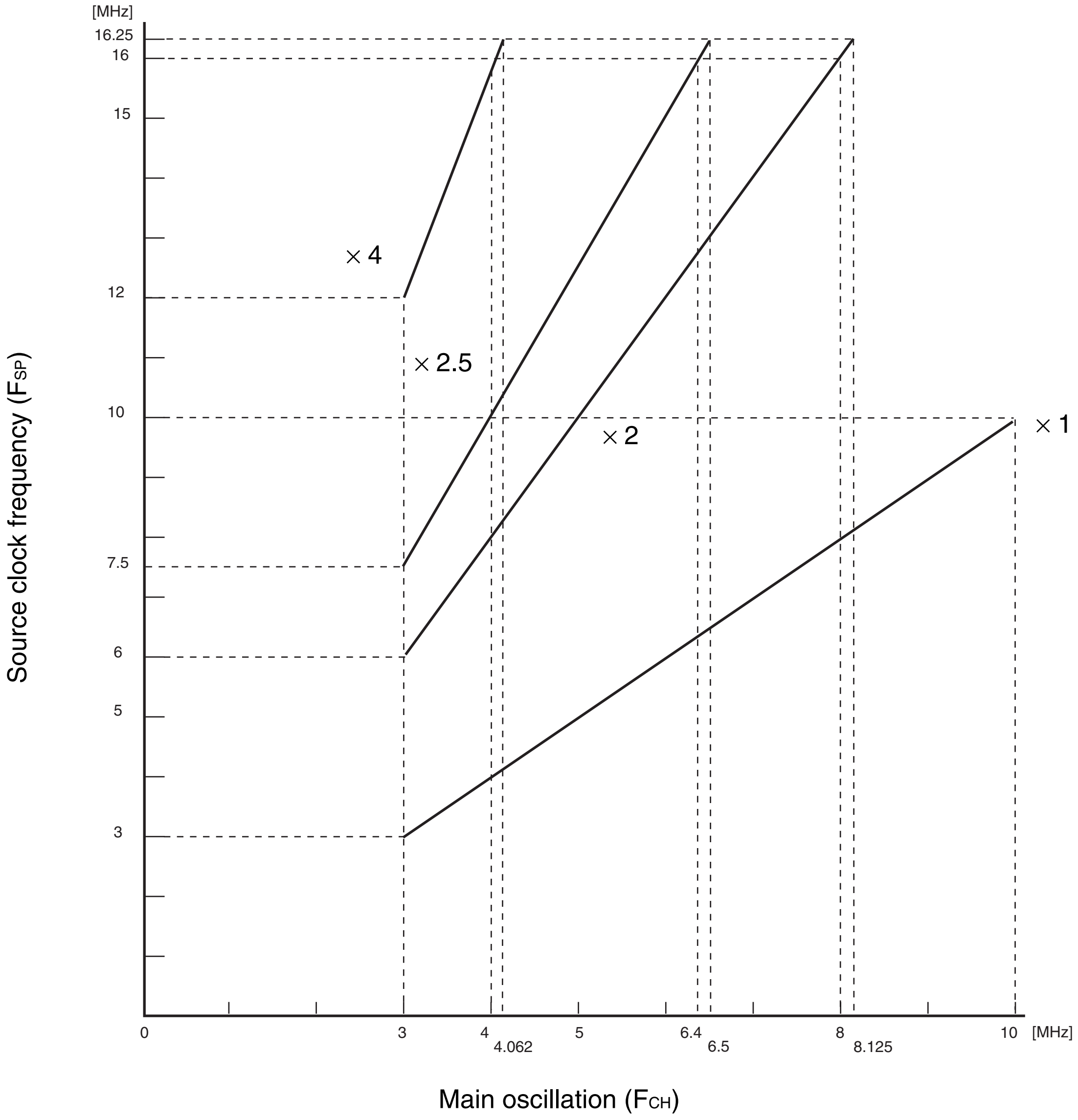


- Operating voltage - Operating frequency (When $T_A = +5$ °C to $+35$ °C)
  - MB95FV100D-103





- Main PLL operation frequency



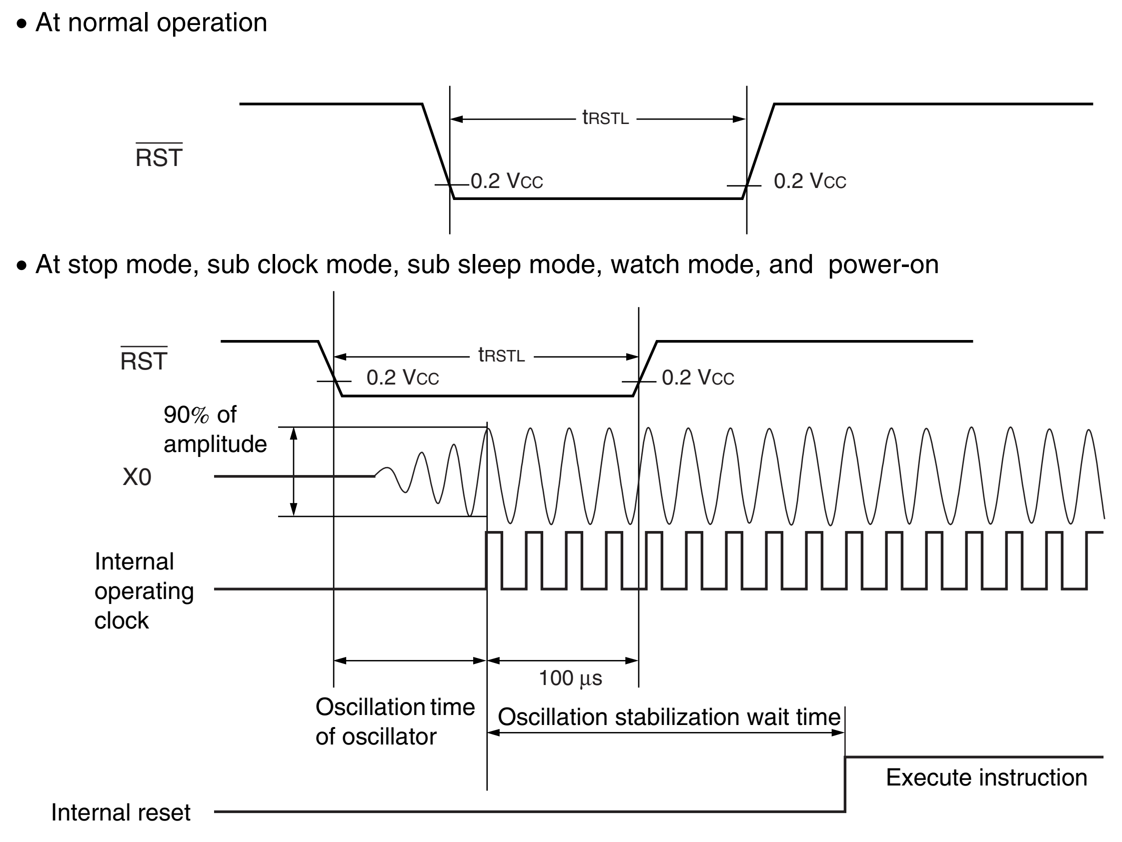
(3) External Reset

(V_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
$\overline{RST}$ "L" level pulse width	t_{RSTL}	$\overline{RST}$	2 t_{MCLK}*1	—	ns	At normal operation
			Oscillation time of oscillator*2 + 100	—	µs	At stop mode, sub clock mode, sub sleep mode & watch mode
			100	—	µs	At timebase timer mode

*1 : Refer to " (2) Source Clock / Machine Clock" for t_{MCLK}.

*2 : Oscillation start time of oscillator is the time that the amplitude reaches 90 %. In the crystal oscillator, the oscillation time is between several ms and tens of ms. In ceramic oscillators, the oscillation time is between hundreds of µs and several ms. In the external clock, the oscillation time is 0 ms.

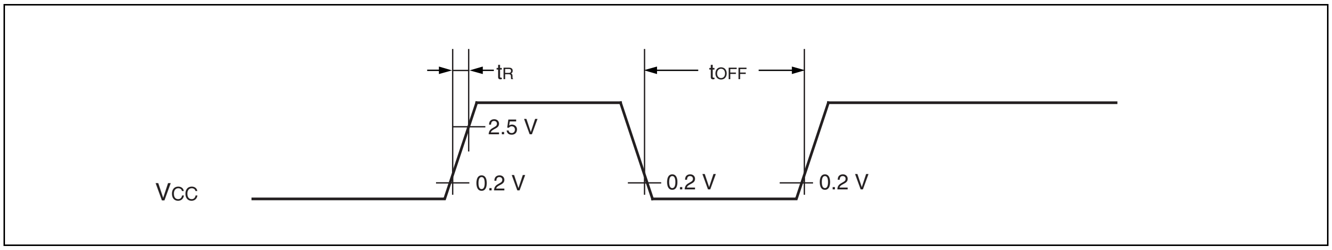

• At normal operation
$\overline{RST}$
t_{RSTL}
0.2 V_{CC}
0.2 V_{CC}
• At stop mode, sub clock mode, sub sleep mode, watch mode, and power-on
$\overline{RST}$
t_{RSTL}
0.2 V_{CC}
0.2 V_{CC}
90% of amplitude
X0
Internal operating clock
100 µs
Oscillation time of oscillator
Oscillation stabilization wait time
Execute instruction
Internal reset

(4) Power-on Reset

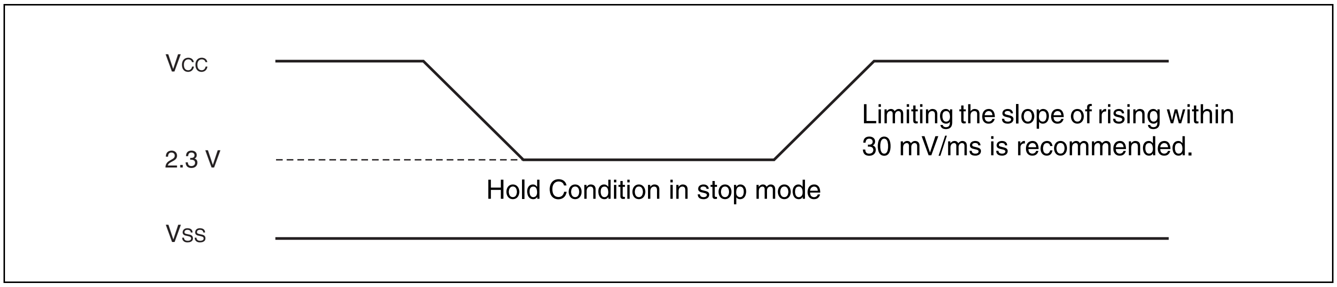
($AV_{SS} = V_{SS} = 0.0$ V, $T_A = -40$ °C to +105 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Power supply rising time	t_R	V_{CC}	—	—	50	ms	
Power supply cutoff time	t_{OFF}		—	1	—	ms	Waiting time until power-on

Note: Complete the power-on process within the selected oscillation stabilization wait time.


tR
tOFF
2.5 V
0.2 V
0.2 V
0.2 V
VCC

Note: Sudden change of power supply voltage may activate the power-on reset function. When changing power supply voltages during operation, set the slope of rising within 30 mV/ms as shown below.

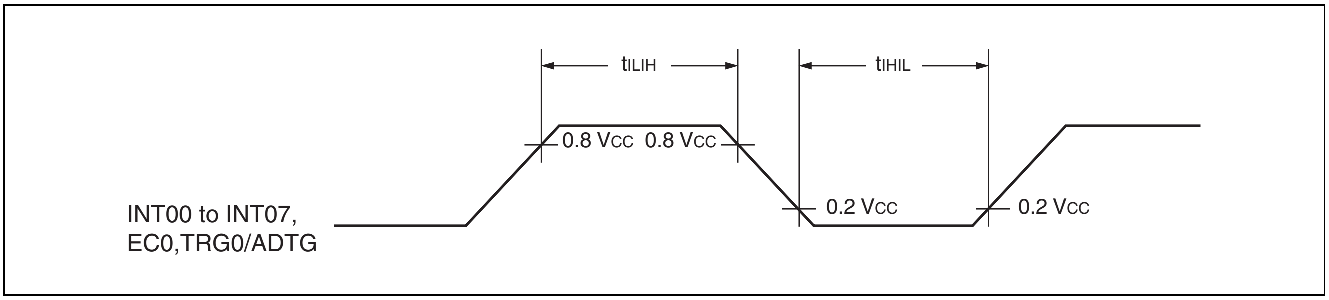

VCC
2.3 V
VSS
Hold Condition in stop mode
Limiting the slope of rising within 30 mV/ms is recommended.

(5) Peripheral Input Timing

(V_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
Peripheral input “H” pulse	t_{ILIH}	INT00 to INT07, EC0, TRG0/ADTG	2 t_{MCLK}*	—	ns
Peripheral input “L” pulse	t_{IHIL}		2 t_{MCLK}*	—	ns

* : Refer to “ (2) Source Clock / Machine Clock” for t_{MCLK}.

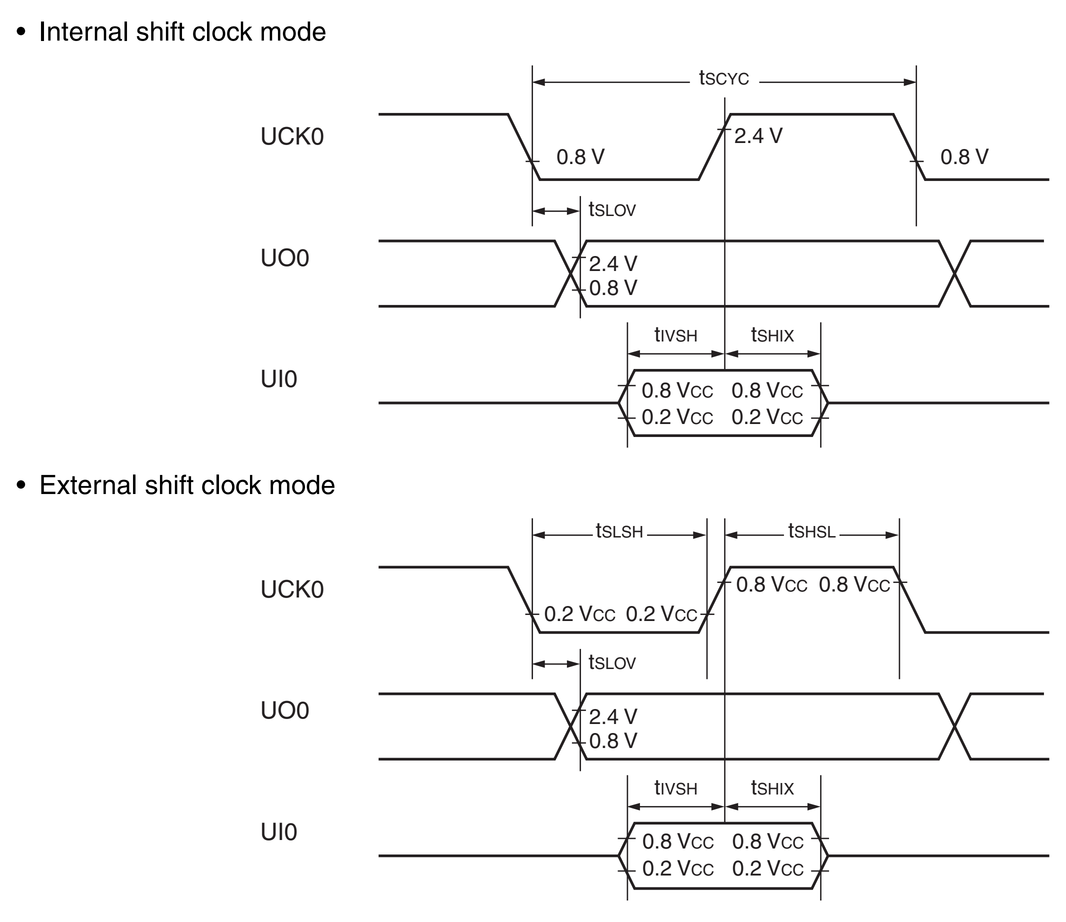

tILIH
tIHIL
0.8 VCC
0.8 VCC
0.2 VCC
0.2 VCC
INT00 to INT07,
EC0,TRG0/ADTG

(6) UART/SIO Serial I/O Timing

(V_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	UCK0	Internal clock operation output pin : C_L = 80 pF + 1 TTL.	4 t_{MCLK}*	—	ns
UCK ↓ → UO time	t_{SLOV}	UCK0, UO0		− 190	+190	ns
Valid UI → UCK ↑	t_{IVSH}	UCK0, UI0		2 t_{MCLK}*	—	ns
UCK ↑→ valid UI hold time	t_{SHIX}	UCK0, UI0		2 t_{MCLK}*	—	ns
Serial clock “H” pulse width	t_{SHSL}	UCK0	External clock operation output pin : C_L = 80 pF + 1 TTL.	4 t_{MCLK}*	—	ns
Serial clock “L” pulse width	t_{SLSH}	UCK0		4 t_{MCLK}*	—	ns
UCK ↓ → UO time	t_{SLOV}	UCK0, UO0		—	190	ns
Valid UI → UCK ↑	t_{IVSH}	UCK0, UI0		2 t_{MCLK}*	—	ns
UCK ↑→ valid UI hold time	t_{SHIX}	UCK0, UI0		2 t_{MCLK}*	—	ns

* : Refer to “ (2) Source Clock / Machine Clock” for t_{MCLK}.


• Internal shift clock mode
tSCYC
UCK0
0.8 V
2.4 V
0.8 V
tSLOV
UO0
2.4 V
0.8 V
tIVSH
tSHIX
UI0
0.8 VCC 0.8 VCC
0.2 VCC 0.2 VCC
• External shift clock mode
tSLSH
tSHSL
UCK0
0.2 VCC 0.2 VCC
0.8 VCC 0.8 VCC
tSLOV
UO0
2.4 V
0.8 V
tIVSH
tSHIX
UI0
0.8 VCC 0.8 VCC
0.2 VCC 0.2 VCC

(7) LIN-UART Timing

Sampling at the rising edge of sampling clock*¹ and prohibited serial clock delay*²
(ESCR register : SCES bit = 0, ECCR register : SCDE bit = 0)

(V_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

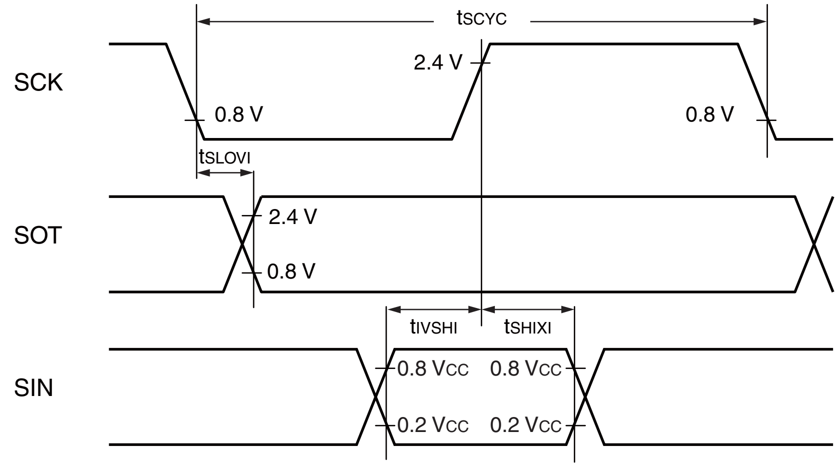
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin : C_L = 80 pF + 1 TTL.	5 t_{MCLK}*3	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK, SOT		− 95	+95	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK, SIN		t_{MCLK}*3 + 190	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXI}	SCK, SIN		0	—	ns
Serial clock "L" pulse width	t_{SLSH}	SCK	External clock operation output pin : C_L = 80 pF + 1 TTL.	3 t_{MCLK}*3 − t_R	—	ns
Serial clock "H" pulse width	t_{SHSL}	SCK		t_{MCLK}*3 + 95	—	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCK, SOT		—	2 t_{MCLK}*3 + 95	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCK, SIN		190	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXE}	SCK, SIN		t_{MCLK}*3 + 95	—	ns
SCK fall time	t_F	SCK		—	10	ns
SCK rise time	t_R	SCK		—	10	ns

*1 : Provide switch function whether sampling of reception data is performed at rising edge or falling edge of the serial clock.

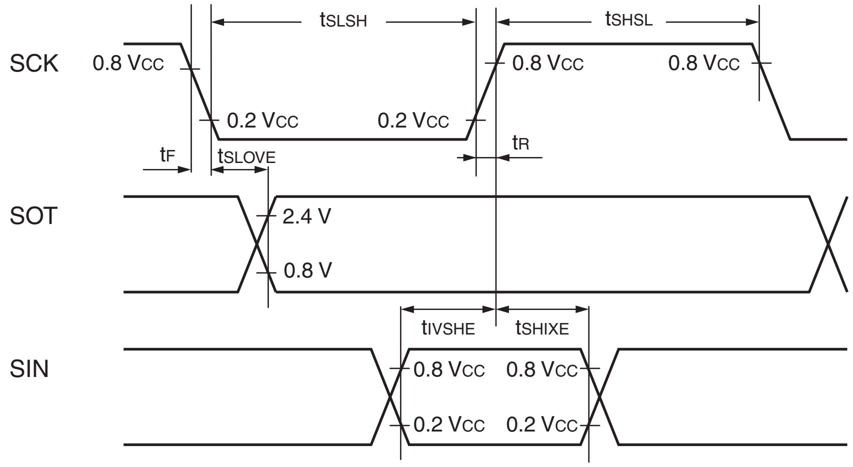
*2 : Serial clock delay function is used to delay half clock for the output signal of serial clock.

*3 : Refer to " (2) Source Clock / Machine Clock" for t_{MCLK}.

- Internal shift clock mode


t_{SCYC}
SCK
2.4 V
0.8 V
0.8 V
t_{SLOVI}
SOT
2.4 V
0.8 V
t_{IVSHI}
t_{SHIXI}
SIN
0.8 V_{CC}
0.8 V_{CC}
0.2 V_{CC}
0.2 V_{CC}

- External shift clock mode


t_{SLSH}
t_{SHSL}
SCK
0.8 V_{CC}
0.8 V_{CC}
0.8 V_{CC}
0.2 V_{CC}
0.2 V_{CC}
t_F
t_{SLOVE}
t_R
SOT
2.4 V
0.8 V
t_{IVSHE}
t_{SHIXE}
SIN
0.8 V_{CC}
0.8 V_{CC}
0.2 V_{CC}
0.2 V_{CC}

Sampling at the falling edge of sampling clock*1 and prohibited serial clock delay*2
(ESCR register : SCES bit = 1, ECCR register : SCDE bit = 0)

(V_{CC} = 5.0 V± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

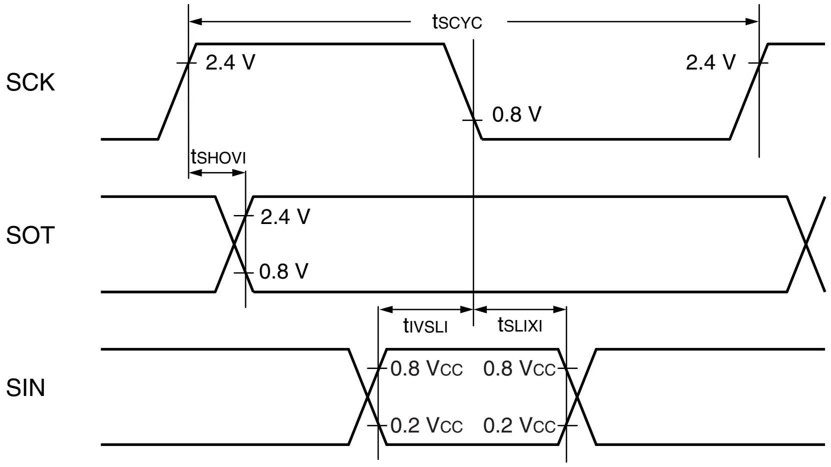
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin : C_L = 80 pF + 1 TTL.	5 t_{MCLK}*3	—	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCK, SOT		− 95	+95	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK, SIN		t_{MCLK}*3 + 190	—	ns
SCK ↓ → valid SIN hold time	t_{SLIXI}	SCK, SIN		0	—	ns
Serial clock "H" pulse width	t_{SHSL}	SCK	External clock operation output pin : C_L = 80 pF + 1 TTL.	3 t_{MCLK}*3 − t_R	—	ns
Serial clock "L" pulse width	t_{SLSH}	SCK		t_{MCLK}*3 + 95	—	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCK, SOT		—	2 t_{MCLK}*3 + 95	ns
Valid SIN → SCK ↓	t_{IVSLE}	SCK, SIN		190	—	ns
SCK ↓ → valid SIN hold time	t_{SLIXE}	SCK, SIN		t_{MCLK}*3 + 95	—	ns
SCK fall time	t_F	SCK		—	10	ns
SCK rise time	t_R	SCK		—	10	ns

*1 : Provide switch function whether sampling of reception data is performed at rising edge or falling edge of the serial clock.

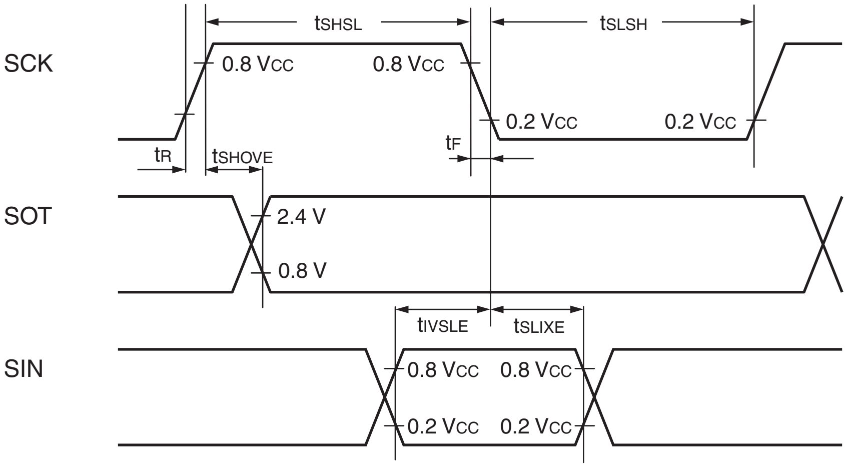
*2 : Serial clock delay function is used to delay half clock for the output signal of serial clock.

*3 : Refer to "(2) Source Clock / Machine Clock" for t_{MCLK}.

- Internal shift clock mode


tSCYC
SCK
2.4 V
0.8 V
2.4 V
tSHOVI
SOT
2.4 V
0.8 V
tIVSLI
tSLIXI
SIN
0.8 VCC
0.8 VCC
0.2 VCC
0.2 VCC

- External shift clock mode


tSHSL
tSLSH
SCK
0.8 VCC
0.8 VCC
0.2 VCC
0.2 VCC
tR
tSHOVE
tF
SOT
2.4 V
0.8 V
tIVSLE
tSLIXE
SIN
0.8 VCC
0.8 VCC
0.2 VCC
0.2 VCC

Sampling at the rising edge of sampling clock*1 and enabled serial clock delay*2
(ESCR register : SCES bit = 0, ECCR register : SCDE bit = 1)

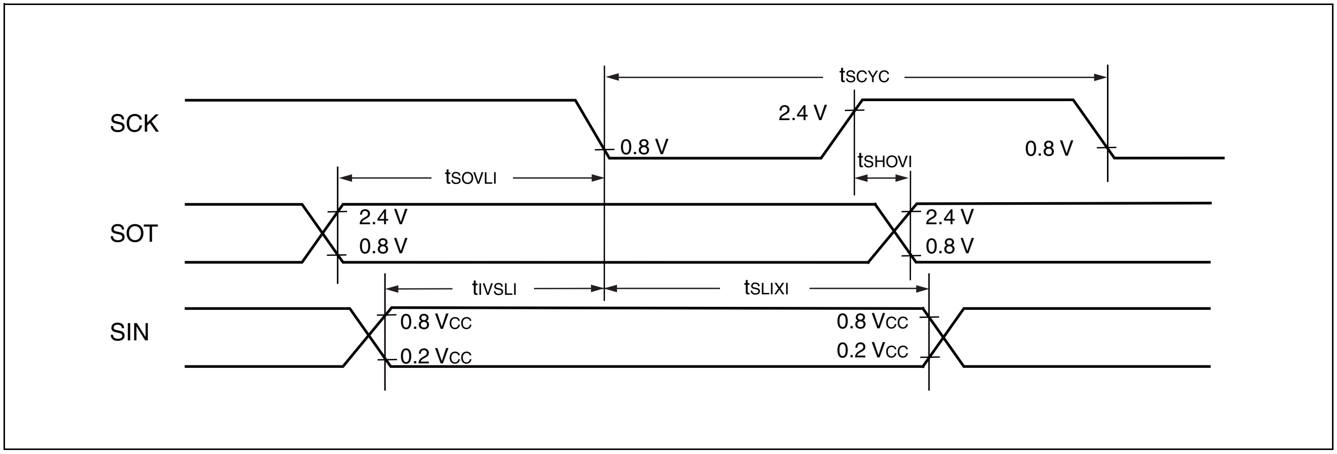
(V_{CC} = 5.0 V± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Sym-bol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin : C_L = 80 pF + 1 TTL.	5 t_{MCLK}*3	—	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCK, SOT		− 95	+95	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK, SIN		t_{MCLK}*3 + 190	—	ns
SCK ↓ → valid SIN hold time	t_{SLIXI}	SCK, SIN		0	—	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCK, SOT		—	4 t_{MCLK}*3	ns

*1 : Provide switch function whether sampling of reception data is performed at rising edge or falling edge of the serial clock.

*2 : Serial clock delay function is used to delay half clock for the output signal of serial clock.

*3 : Refer to “ (2) Source Clock / Machine Clock” for t_{MCLK}.



SCK
SOT
SIN
tSCYC
2.4 V
0.8 V
tSHOVI
0.8 V
tSOVLI
2.4 V
0.8 V
2.4 V
0.8 V
tIVSLI
tSLIXI
0.8 VCC
0.2 VCC
0.8 VCC
0.2 VCC

Sampling at the falling edge of sampling clock*1 and enabled serial clock delay*2
(ESCR register : SCES bit = 1, ECCR register : SCDE bit = 1)

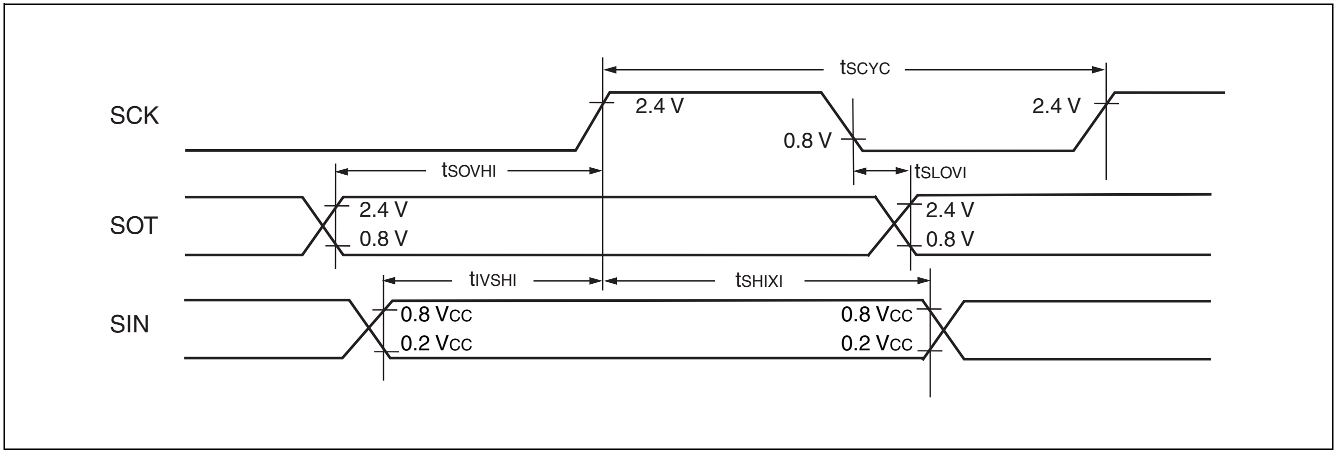
(V_{CC} = 5.0 V± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Sym-bol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operating output pin : C_L = 80 pF + 1 TTL.	5 t_{MCLK}*3	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK, SOT		− 95	+95	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK, SIN		t_{MCLK}*3 + 190	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXI}	SCK, SIN		0	—	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCK, SOT		—	4 t_{MCLK}*3	ns

*1 : Provide switch function whether sampling of reception data is performed at rising edge or falling edge of the serial clock.

*2 : Serial clock delay function is used to delay half clock for the output signal of serial clock.

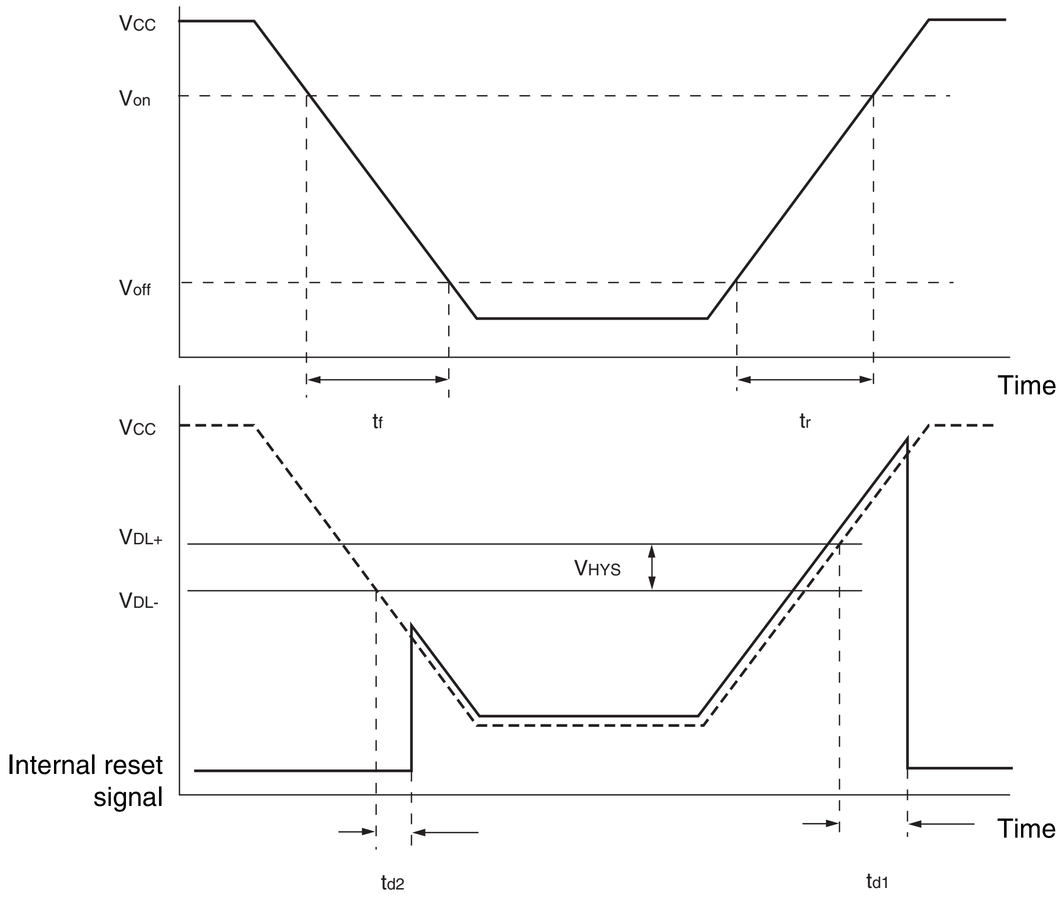
*3 : Refer to " (2) Source Clock / Machine Clock" for t_{MCLK}.


SCK
SOT
SIN
tSCYC
2.4 V
0.8 V
2.4 V
tSOVHI
tSLOVI
2.4 V
0.8 V
2.4 V
0.8 V
tIVSHI
tSHIXI
0.8 VCC
0.2 VCC
0.8 VCC
0.2 VCC

(8) Low voltage Detection

($AV_{SS} = V_{SS} = 0.0$ V, $T_A =$ – 40 °C to + 105 °C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Release voltage	V_{DL+}	2.52	2.70	2.88	V	At power-supply rise
Detection voltage	V_{DL-}	2.42	2.60	2.78	V	At power-supply fall
Hysteresis width	V_{HYS}	70	100	—	mV	
Power-supply start voltage	V_{off}	—	—	2.3	V	
Power-supply end voltage	V_{on}	4.9	—	—	V	
Power-supply voltage change time (at power supply rise)	t_r	0.3	—	—	µs	Slope of power supply that reset release signal generates
		—	3000	—	µs	Slope of power supply that reset release signal generates within rating (V_{DL+})
Power-supply voltage change time (at power supply fall)	t_f	300	—	—	µs	Slope of power supply that reset detection signal generates
		—	300	—	µs	Slope of power supply that reset detection signal generates within rating (V_{DL-})
Reset release delay time	t_{d1}	—	—	400	µs	
Reset detection delay time	t_{d2}	—	—	30	µs	
Consumption current	I_{LVD}	—	38	50	µA	Consumption current of low voltage detection circuit only


VCC
Von
Voff
Time
tf
tr
VCC
VDL+
VHYS
VDL-
Internal reset signal
Time
td2
td1

(9) Clock Supervisor Clock

($V_{CC} = AV_{CC} = 5$ V ± 10%, $AV_{SS} = V_{SS} = 0.0$ V, $T_A = -40$ °C to $+105$ °C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Oscillation frequency	f_{OUT}	50	100	200	kHz	
Oscillation start time	t_{wk}	—	—	10	µs	
Current consumption	I_{CSV}	—	20	36	µA	Current consumption of built-in CR oscillator at 100 kHz oscillation

5. A/D Converter

(1) A/D Converter Electrical Characteristics

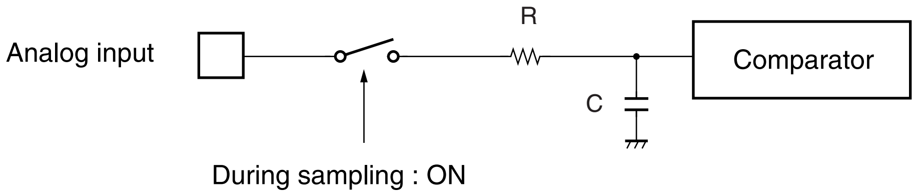
($AV_{CC} = V_{CC} = 4.0$ V to 5.5 V, $AV_{SS} = V_{SS} = 0.0$ V, $T_A =$ – 40 °C to + 105 °C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	10	bit	
Total error		– 3.0	—	+ 3.0	LSB	
Linearity error		– 2.5	—	+ 2.5	LSB	
Differential linear error		– 1.9	—	+ 1.9	LSB	
Zero transition voltage	V_{OT}	AV_{SS} – 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	V	
Full-scale transition voltage	V_{FST}	AV_{CC} – 4.5 LSB	AV_{CC} – 1.5 LSB	AV_{CC} + 0.5 LSB	V	
Compare time	—	0.9	—	16500	µs	4.5 V ≤ AV_{CC} ≤ 5.5 V
		1.8	—	16500	µs	4.0 V ≤ AV_{CC} < 4.5 V
Sampling time	—	0.6	—	∞	µs	4.5 V ≤ AVcc ≤ 5.5 V, At external impedance < at 5.4 kΩ
		1.2	—	∞	µs	4.0 V ≤ AVcc ≤ 4.5 V, At external impedance < at 2.4 kΩ
Analog input current	I_{AIN}	– 0.3	—	+ 0.3	µA	
Analog input voltage	V_{AIN}	AV_{SS}	—	AV_{CC}	V	

(2) Notes on Using A/D Converter

- **External impedance of analog input and its sampling time**
  - A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision. Therefore to satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. Also, if the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin.

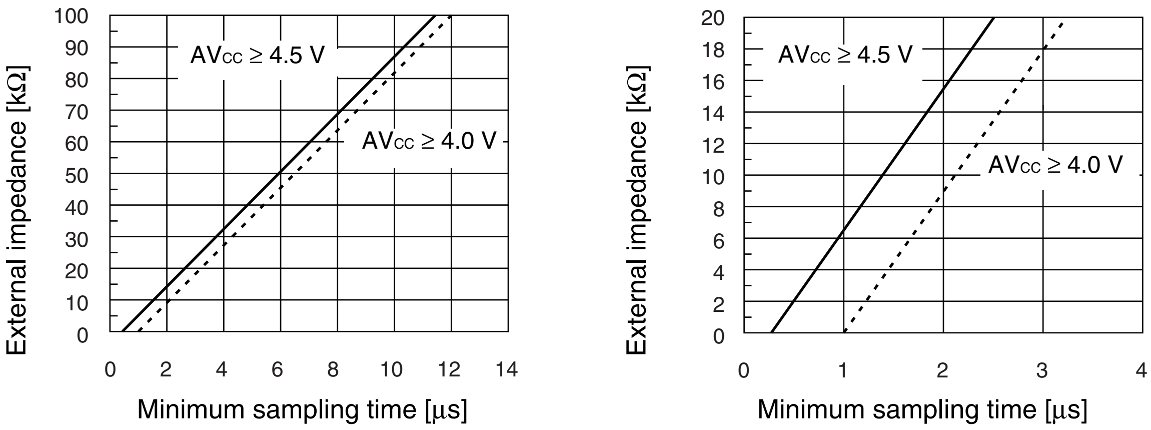
- Analog input equivalent circuit



	R	**C**
4.5 V ≤ AV_{CC} ≤ 5.5 V	2.0 kΩ (Max)	16 pF (Max)
4.0 V ≤ AV_{CC} < 4.5 V	8.2 kΩ (Max)	16 pF (Max)

Note : The values are reference values.

- The relationship between external impedance and minimum sampling time



(External impedance = at 0 kΩ to 100 kΩ)

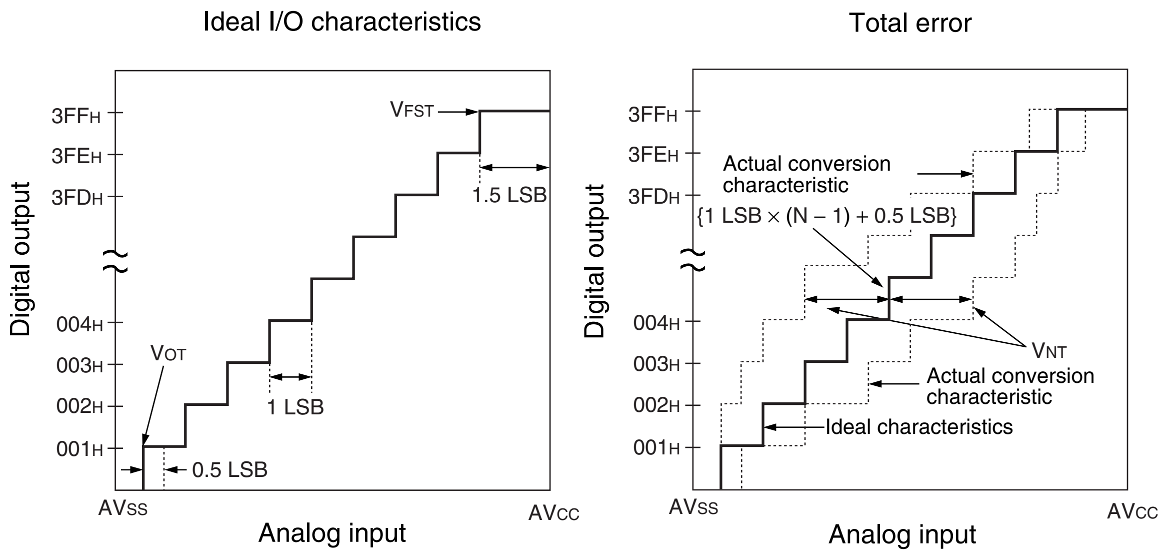
(External impedance = at 0 kΩ to 20 kΩ)

- **Errors**

  As $|AV_{CC} - AV_{SS}|$ becomes smaller, values of relative errors grow larger.

(3) Definition of A/D Converter Terms

- Resolution
  The level of analog variation that can be distinguished by the A/D converter.
  When the number of bits is 10, analog voltage can be divided into $2^{10} = 1024$.
- Linearity error (unit : LSB)
  The deviation between the value along a straight line connecting the zero transition point (“00 0000 0000” ← → “00 0000 0001”) of a device and the full-scale transition point (“11 1111 1111” ← → “11 1111 1110”) compared with the actual conversion values obtained.
- Differential linear error (Unit : LSB)
  Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.
- Total error (unit: LSB)
  Difference between actual and theoretical values, caused by a zero transition error, full-scale transition error, linearity error, quantum error, and noise.


Ideal I/O characteristics
Digital output
3FFH
3FEH
3FDH
004H
003H
002H
001H
VFST
1.5 LSB
VOT
1 LSB
0.5 LSB
AVSS
AVCC
Analog input
Total error
Digital output
3FFH
3FEH
3FDH
004H
003H
002H
001H
Actual conversion characteristic
{1 LSB × (N − 1) + 0.5 LSB}
VNT
Actual conversion characteristic
Ideal characteristics
AVSS
AVCC
Analog input

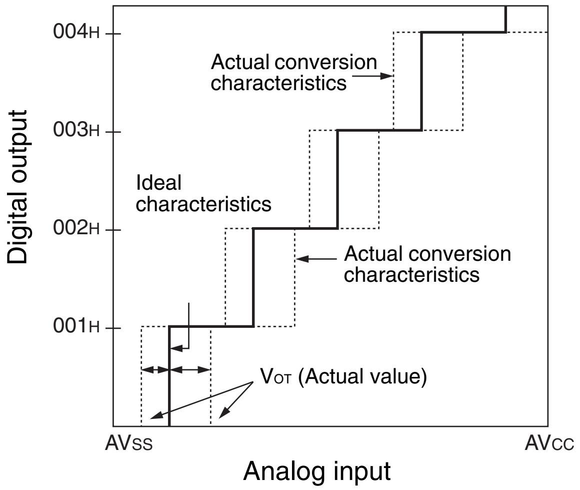
$$1\ \text{LSB} = \frac{AV_{CC} - AV_{SS}}{1024} \quad (\text{V})$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}} \ [\text{LSB}]$$

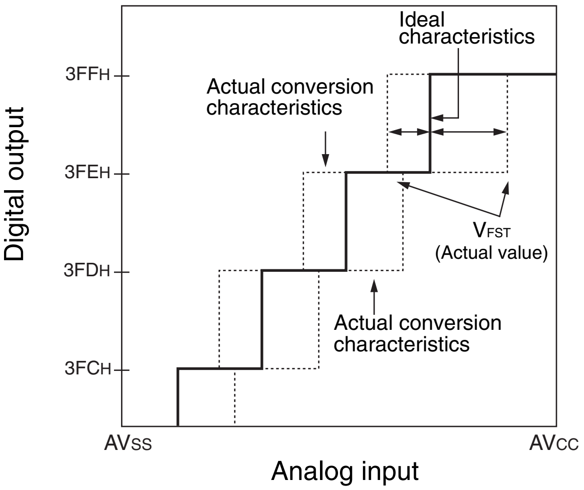
N : A/D converter digital output value
V_{NT} : Voltage at which digital output transits from $(N\text{-}1)_H$ to N_H.

(Continued)

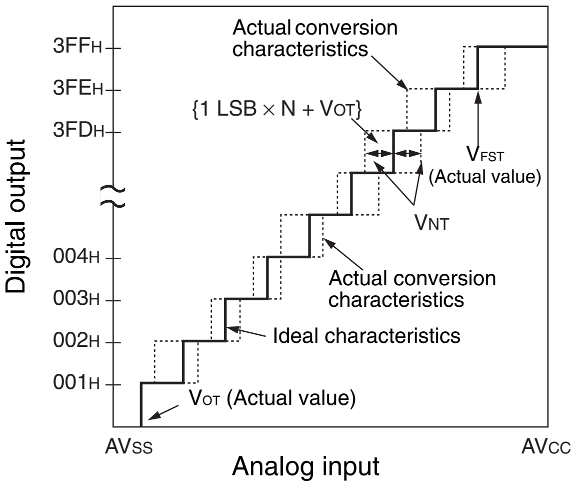
Zero transition error


004H
003H
002H
001H
Digital output
Actual conversion characteristics
Ideal characteristics
Actual conversion characteristics
VOT (Actual value)
AVSS
AVCC
Analog input

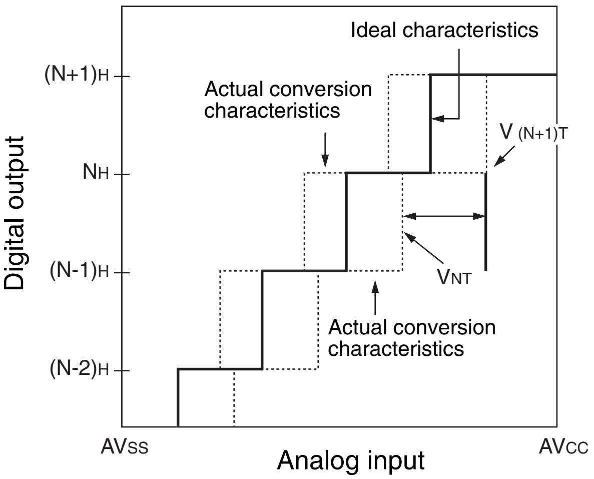
Full-scale transition error


3FFH
3FEH
3FDH
3FCH
Digital output
Ideal characteristics
Actual conversion characteristics
VFST (Actual value)
Actual conversion characteristics
AVSS
AVCC
Analog input

Linearity error


3FFH
3FEH
3FDH
004H
003H
002H
001H
Digital output
Actual conversion characteristics
{1 LSB × N + VOT}
VFST (Actual value)
VNT
Actual conversion characteristics
Ideal characteristics
VOT (Actual value)
AVSS
AVCC
Analog input

Differential linear error


(N+1)H
NH
(N-1)H
(N-2)H
Digital output
Ideal characteristics
Actual conversion characteristics
V (N+1)T
VNT
Actual conversion characteristics
AVSS
AVCC
Analog input

$$\text{Linear error of digital output N} = \frac{V_{NT} - \{1\text{ LSB} \times N + V_{OT}\}}{1\text{ LSB}}$$

$$\text{Differential linear error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\text{ LSB}} - 1$$

N : A/D converter digital output value
V_{NT} : Voltage at which digital output transits from (N - 1)$_H$ to N$_H$.
V_{OT} (Ideal value) = AV_{SS} + 0.5 LSB [V]
V_{FST} (Ideal value) = AV_{CC} – 1.5 LSB [V]

6. Flash Memory Program/Erase Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Chip erase time	—	1.0*1	15.0*2	s	Excludes 00_H programming prior erasure.
Byte programming time	—	32	3600	µs	Excludes system-level overhead.
Erase/program cycle	10000	—	—	cycle	
Power supply voltage at erase/ program	4.5	—	5.5	V	
Flash memory data retention time	20*3	—	—	year	Average $T_A = +85$ °C

*1 : $T_A = +25$ °C, $V_{CC} = 5.0$ V, 10000 cycles

*2 : $T_A = +85$ °C, $V_{CC} = 4.5$ V, 10000 cycles

*3 : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at +85 °C) .

■ MASK OPTION

No.	Part number	MB95136MB	MB95F133MBS MB95F133NBS MB95F133JBS MB95F134MBS MB95F134NBS MB95F134JBS MB95F136MBS MB95F136NBS MB95F136JBS	MB95F133MBW MB95F133NBW MB95F133JBW MB95F134MBW MB95F134NBW MB95F134JBW MB95F136MBW MB95F136NBW MB95F136JBW	MB95FV100D-103
	Specifying procedure	**Specify when ordering MASK**	**Setting disabled**	**Setting disabled**	**Setting disabled**
1	Clock mode select • Single-system clock mode • Dual-system clock mode	selectable	Single-system clock mode	Dual-system clock mode	Changing by the switch on MCU board
2	Low voltage detection reset* • With low voltage detection reset • Without low voltage detection reset	Specify when ordering MASK	Specified by part number	Specified by part number	Change by the switch on MCU board
3	Clock supervisor* • With clock supervisor • Without clock supervisor	Specify when ordering MASK	Specified by part number	Specified by part number	Change by the switch on MCU board
4	Reset output* • With reset output • Without reset output	Not selectable	Not selectable	Not selectable	MCU board switch set as following ; • With supervisor : Without reset output • Without supervisor : With reset output
5	Oscillation stabilization wait time	Fixed to oscillation stabilization wait time of $(2^{14} - 2) / F_{CH}$	Fixed to oscillation stabilization wait time of $(2^{14} - 2) / F_{CH}$	Fixed to oscillation stabilization wait time of $(2^{14} - 2) / F_{CH}$	Fixed to oscillation stabilization wait time of $(2^{14} - 2) / F_{CH}$

*: Refer to table below about clock mode select, low voltage detection reset, clock supervisor select and reset output.

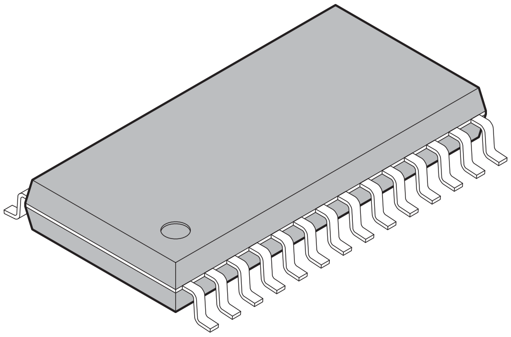
Part number	Clock mode select	Low-voltage detection reset	Clock supervisor	Reset output*
MB95136MB	Single - system	No	No	Yes
		Yes	No	Yes
		Yes	Yes	No
	Dual - system	No	No	Yes
		Yes	No	Yes
		Yes	Yes	No
MB95F133MBS	Single - system	No	No	Yes
MB95F133NBS		Yes	No	Yes
MB95F133JBS		Yes	Yes	No
MB95F134MBS		No	No	Yes
MB95F134NBS		Yes	No	Yes
MB95F134JBS		Yes	Yes	No
MB95F136MBS		No	No	Yes
MB95F136NBS		Yes	No	Yes
MB95F136JBS		Yes	Yes	No
MB95F133MBW	Dual - system	No	No	Yes
MB95F133NBW		Yes	No	Yes
MB95F133JBW		Yes	Yes	No
MB95F134MBW		No	No	Yes
MB95F134NBW		Yes	No	Yes
MB95F134JBW		Yes	Yes	No
MB95F136MBW		No	No	Yes
MB95F136NBW		Yes	No	Yes
MB95F136JBW		Yes	Yes	No
MB95FV100D-103	Single - system	No	No	Yes
		Yes	No	Yes
		Yes	Yes	No
	Dual - system	No	No	Yes
		Yes	No	Yes
		Yes	Yes	No

*: If the clock supervisor is selected, reset output is always disabled.

■ ORDERING INFORMATION

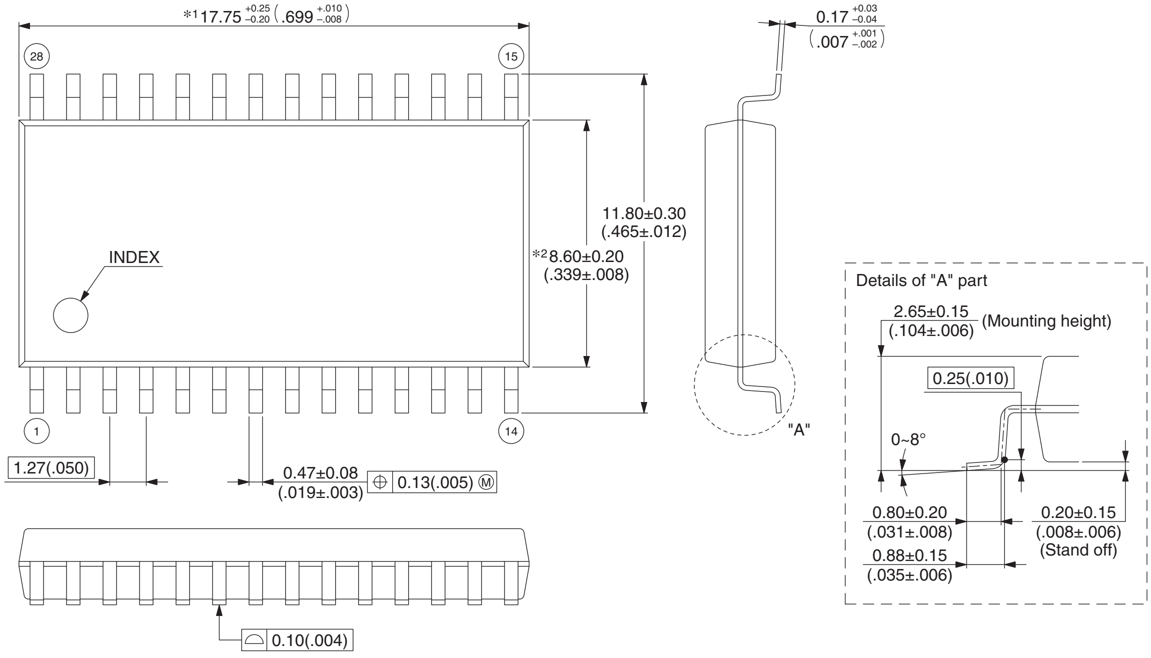
Part number	Package
MB95136MBPF MB95F133MBSPF MB95F133NBSPF MB95F133JBSPF MB95F134MBSPF MB95F134NBSPF MB95F134JBSPF MB95F136MBSPF MB95F136NBSPF MB95F136JBSPF MB95F133MBWPF MB95F133NBWPF MB95F133JBWPF MB95F134MBWPF MB95F134NBWPF MB95F134JBWPF MB95F136MBWPF MB95F136NBWPF MB95F136JBWPF	28-pin plastic SOP (FPT-28P-M17)
MB95136MBPFV MB95F133MBSPFV MB95F133NBSPFV MB95F133JBSPFV MB95F134MBSPFV MB95F134NBSPFV MB95F134JBSPFV MB95F136MBSPFV MB95F136NBSPFV MB95F136JBSPFV MB95F133MBWPFV MB95F133NBWPFV MB95F133JBWPFV MB95F134MBWPFV MB95F134NBWPFV MB95F134JBWPFV MB95F136MBWPFV MB95F136NBWPFV MB95F136JBWPFV	30-pin plastic SSOP (FPT-30P-M02)
MB2146-303A-E (MB95FV100D-103PBT)	MCU board (224-pin plastic PFBGA (BGA-224P-M08))

■ PACKAGE DIMENSION

28-pin plastic SOP  (FPT-28P-M17)	Lead pitch	1.27 mm
	Package width × package length	8.6 × 17.75 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	2.80 mm MAX
	Weight	0.82 g
	Code (Reference)	P-SOP28-8.6×17.75-1.27

28-pin plastic SOP
(FPT-28P-M17)

Note 1) *1 : These dimensions include resin protrusion.
Note 2) *2 : These dimensions do not include resin protrusion.
Note 3) Pins width and pins thickness include plating thickness.
Note 4) Pins width do not include tie bar cutting remainder.


*1 17.75 +0.25 −0.20 (.699 +.010 −.008)
28
15
1
14
INDEX
11.80±0.30 (.465±.012)
*2 8.60±0.20 (.339±.008)
1.27(.050)
0.47±0.08 (.019±.003)
0.13(.005) M
0.10(.004)
0.17 +0.03 −0.04 (.007 +.001 −.002)
"A"
Details of "A" part
2.65±0.15 (.104±.006) (Mounting height)
0.25(.010)
0~8°
0.80±0.20 (.031±.008)
0.88±0.15 (.035±.006)
0.20±0.15 (.008±.006) (Stand off)

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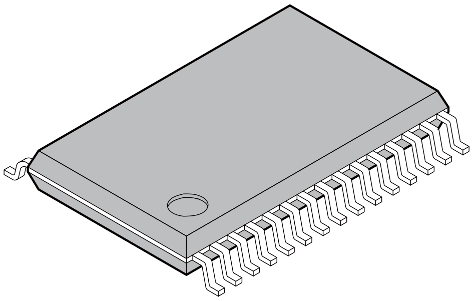
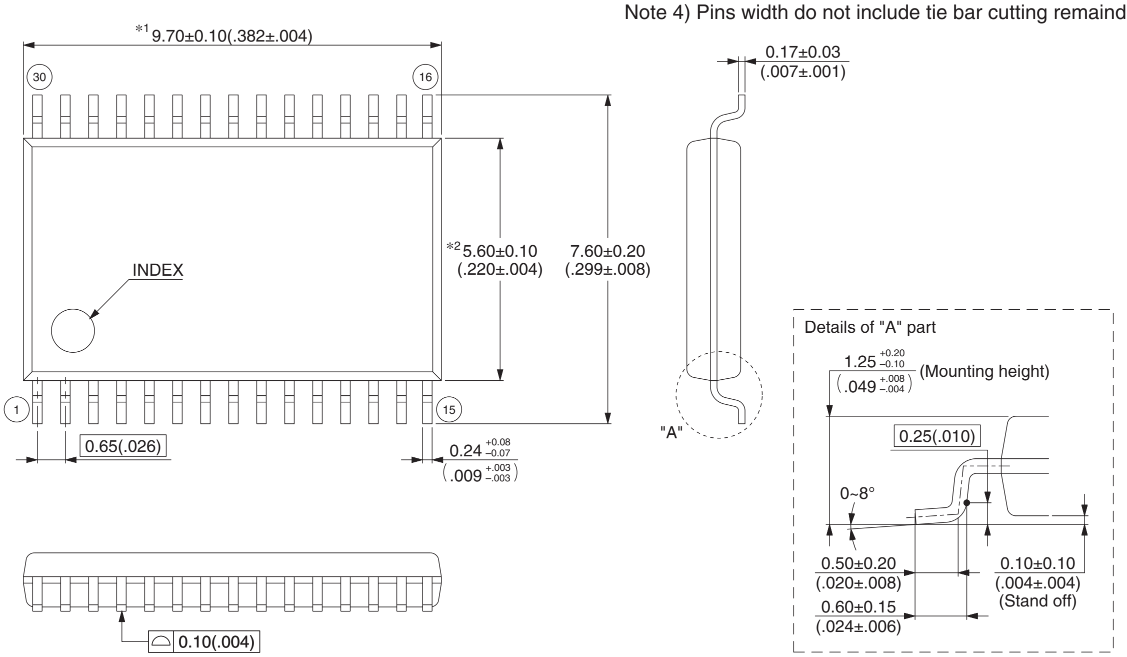
Dimensions in mm (inches).
Note: The values in parentheses are reference values.

(Continued)

30-pin plastic SSOP  (FPT-30P-M02)	Lead pitch	0.65 mm
	Package width × package length	5.60 × 9.70 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.45 mm MAX
	Code (Reference)	P-SSOP30-5.6×9.7-0.65

30-pin plastic SSOP
(FPT-30P-M02)

Note 1) *1 : Resin protrusion. (Each side : +0.15 (.006) Max).
Note 2) *2 : These dimensions do not include resin protrusion.
Note 3) Pins width and pins thickness include plating thickness.
Note 4) Pins width do not include tie bar cutting remainder.


*1 9.70±0.10(.382±.004)
30
16
1
15
INDEX
*2 5.60±0.10 (.220±.004)
7.60±0.20 (.299±.008)
0.65(.026)
0.24 +0.08 −0.07 (.009 +.003 −.003)
0.10(.004)
0.17±0.03 (.007±.001)
"A"
Details of "A" part
1.25 +0.20 −0.10 (.049 +.008 −.004) (Mounting height)
0.25(.010)
0~8°
0.50±0.20 (.020±.008)
0.60±0.15 (.024±.006)
0.10±0.10 (.004±.004) (Stand off)

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Dimensions in mm (inches).
Note: The values in parentheses are reference values

■ MAJOR CHANGES IN THIS EDITION

A change on a page is indicated by a vertical line drawn on the left side of that page.

Page	Section	Change Results
2	■ FEATURES	Added "• Power-on reset".
4	■ PRODUCT LINEUP	Added the parameter "Power-on reset". Changed the reset output of MB95136MB. Yes → Not selectable
29	■ ELECTRICAL CHARACTERISTICS 1. Absolute Maximum Ratings	Changed the maximum rating of the operating temperature. 85 → 105
40	■ ELECTRICAL CHARACTERISTICS 4. AC Characteristics (2) Source Clock / Machine Clock	Added MB95136MB to the part numbers in "• Operating voltage - Operating frequency".
41		Changed the x-axis of the graph in " • Main PLL operation frequency". Machine clock frequency (F_{MP}) → Main oscillation (F_{CH})
60	■ MASK OPTION	Changed the "Reset output" of the products listed below to "Not selectable". MB95136MB MB95F133MBS MB95F133NBS MB95F133JBS MB95F134MBS MB95F134NBS MB95F134JBS MB95F136MBS MB95F136NBS MB95F136JBS MB95F133MBW MB95F133NBW MB95F133JBW MB95F134MBW MB95F134NBW MB95F134JBW MB95F136MBW MB95F136NBW MB95F136JBW
61		Added the following note. If the clock supervisor is selected, reset output is always disabled.

MEMO

MEMO

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