# 8-bit Proprietary Microcontroller

**CMOS**

# F²MC-8L MB89630R Series

# MB89635R/636R/637R/P637/PV630

## ■ OUTLINE

The MB89630R series has been developed as a general-purpose version of the F²MC*-8L family consisting of proprietary 8-bit, single-chip microcontrollers.

In addition to a compact instruction set, the microcontrollers contain a variety of peripheral functions such as dual-clock control system, five operating speed control stages, a UART, timers, a PWM timer, a serial interface, an A/D converter, an external interrupt, and a watch prescaler.

* : F²MC is the abbreviation for Fujitsu Flexible Microcontroller.

## ■ FEATURES

- High-speed operating capability at low voltage
- Minimum execution time: 0.4 µs@3.5 V, 0.8 µs@2.7 V
- F²MC-8L family CPU core

Instruction set optimized for controllers
- Multiplication and division instructions
- 16-bit arithmetic operations
- Test and branch instructions
- Bit manipulation instructions, etc.

- Five types of timers
  - 8-bit PWM timer: 2 channels (Also usable as a reload timer)
  - 8-bit pulse-width count timer (Continuous measurement capable, applicable to remote control, etc.)
  - 16-bit timer/counter
  - 21-bit timebase timer

*(Continued)*

For the information for microcontroller supports, see the following web site.

http://edevice.fujitsu.com/micom/en-support/

**FUJITSU**

*(Continued)*
- UART
  CLK-synchronous/CLK-asynchronous data transfer capable (6, 7, and 8 bits)
- Serial interface
  Switchable transfer direction to allows communication with various equipment.
- 10-bit A/D converter
  Start by an external input capable
- External interrupt: 4 channels
  Four channels are independent and capable of wake-up from low-power consumption modes (with an edge detection function).
- Low-power consumption modes
  Stop mode (Oscillation stops to minimize the current consumption.)
  Sleep mode (The CPU stops to reduce the current consumption to approx. 1/3 of normal.)
  Subclock mode
  Watch mode
- Bus interface function
  With hold and ready function

FUJITSU

## ■ PRODUCT LINEUP

| Part number / Item | MB89635R | MB89636R | MB89637R | MB89P637 | MB89PV630 |
|---|---|---|---|---|---|
| Classification | Mass-produced products (mask ROM products) | | | One-time PROM product | Piggyback/ evaluation product (for evaluation and development) |
| ROM size | 16 K × 8 bits (internal mask ROM) | 24 K × 8 bits (internal mask ROM) | 32 K × 8 bits (internal mask ROM) | 32 K × 8 bits (Internal PROM, to be programmed with general-purpose EPROM programmer) | 32 K × 8 bits (external ROM) |
| RAM size | 512 × 8 bits | 768 × 8 bits | 1024 × 8 bits | 1024 × 8 bits | 1024 × 8 bits |
| CPU functions | The number of instructionns:     136<br>Instruction bit length:     8 bits<br>Instruction length:     1 to 3 bytes<br>Data bit length:     1, 8, 16 bits<br>Minimum execution time:     0.4 μs/10 MHz, 61 μs@32.768 kHz<br>Interrupt processing time:     3.6 to 57.6 μs/10 MHz, 562.5 μs@32.768 kHz | | | | |
| Ports | Input ports:     5 (All also serve as peripherals.)<br>Output ports (N-ch open-drain):     8 (All also serve as peripherals.)<br>I/O ports (N-ch open-drain):     4 (All also serve as peripherals.)<br>Output ports (CMOS):     8 (All also serve as bus control.)<br>I/O ports (CMOS):     28 (27 ports also serve as bus pins and peripherals.)<br>Total:     53 | | | | |
| Watch timer | 21 bits × 1 (in main clock)/15 bits × 1 (at 32.768 kHz) | | | | |
| 8-bit PWM timer | 8-bit reload timer operation (toggled output capable, operating clock cycle: 0.4 μs to 3.3 ms) × 2 channels<br>7/8-bit resolution PWM operation (conversion cycle: 51.2 μs to 839 ms) × 2 channels | | | | |
| 8-bit pulse width count timer | 8-bit timer operation (overflow output capable, operating clock cycle: 0.4 to 12.8 μs)<br>8-bit reload timer operation (toggled output capable, operating clock cycle: 0.4 to 12.8 μs)<br>8-bit pulse width measurement operation (capable of continuous measurement, and measurement of "H" pulse width/ "L" pulse width/ from ↑ to ↑/from ↓ to ↓) | | | | |
| 16-bit timer/ counter | 16-bit timer operation (operating clock cycle: 0.4 μs)<br>16-bit event counter operation (rising edge/falling edge/both edge selectable) | | | | |
| 8-bit serial I/O | 8 bits<br>LSB first/MSB first selectable<br>One clock selectable from four transfer clocks<br>(one external shift clock, three internal shift clocks: 0.8 μs, 3.2 μs, 12.8 μs) | | | | |
| UART | Capable of switching two I/O systems by software<br>Transfer data length (6, 7, and 8 bits)<br>Transfer rate (300 to 62500 bps. at 10 MHz oscillation) | | | | |
| 10-bit A/D converter | 10-bit resolution × 8 channels<br>A/D conversion mode (conversion time: 13.2 μs)<br>Sense mode (conversion time: 7.2 μs)<br>Capable of continuous activation by an external activation or an internal timer | | | | |

*(Continued)*

# MB89630R Series

*(Continued)*

| Part number / Item | MB89635R | MB89636R | MB89637R | MB89P637 | MB89PV630 |
|---|---|---|---|---|---|
| External interrupt input | 4 independent channels (edge selection, interrupt vector, source flag). Rising edge/falling edge selectable Used also for wake-up from stop/sleep mode. (Edge detection is also permitted in stop mode.) | | | | |
| Standby mode | Sleep mode, stop mode, watch mode, and subclock mode | | | | |
| Process | CMOS | | | | |
| Operating voltage* | 2.2 V to 6.0 V | | | 2.7 V to 6.0 V | |
| EPROM for use | | | | | MBM27C256A-20CZ MBM27C256A-20TV |

\* : Varies with conditions such as the operating frequency. (See section "■ Electrical Characteristics.")
In the case of the MB89PV630, the voltage varies with the restrictions of the EPROM for use.

## ■ PACKAGE AND CORRESPONDING PRODUCTS

| Package | MB89635R | MB89636R MB89637R | MB89P637 | MB89PV630 |
|---|---|---|---|---|
| DIP-64P-M01 | ○ | ○ | ○ | × |
| FPT-64P-M06 | ○ | ○ | ○ | × |
| FPT-64P-M23 | ○ | ○ | × | × |
| MQP-64C-P01 | × | × | × | ○ |
| MDP-64C-P02 | × | × | × | ○ |

○ : Available     ×: Not available

Note: For more information about each package, see section "■ Package Dimensions."

FUJITSU

## ■ DIFFERENCES AMONG PRODUCTS

### 1. Memory Size

Before evaluating using the piggyback product, verify its differences from the product that will actually be used. Take particular care on the following points:

- On the MB89P637, the program area starts from address 8007$_H$ but on the MB89PV630 and MB89637R starts from 8000$_H$.

  (On the MB89P637, addresses 8000$_H$ to 8006$_H$ comprise the option setting area, option settings can be read by reading these addresses. On the MB89PV630/MB89637R, addresses 8000$_H$ to 8006$_H$ could also be used as a program ROM. However, do not use these addresses in order to maintain compatibility of the MB89P637.)

- The stack area, etc., is set at the upper limit of the RAM.

- The external area is used.

### 2. Current Consumption

- In the case of the MB89PV630, add the current consumed by the EPROM which connected to the top socket.

- When operated at low speed, the product with an OTPROM (one-time PROM) or an EPROM will consume more current than the product with a mask ROM. However, the current consumption in sleep/stop modes is the same. (For more information, see sections "■ Electrical Characteristics" and "■ Example Characteristics".)

### 3. Mask Options

Functions that can be selected as options and how to designate these options vary by the product.

Before using options check section "■ Mask Options".

Take particular care on the following points:

- A pull-up resistor cannot be set for P50 to P53 on the MB89P637.

- Options are fixed on the MB89PV630.

### 4. Differences between the MB89630 and MB89630R Series

- Memory access area
  There are no difference between the access area of MB89635/MB89635R, and that of MB89637/MB89637R. The access area of MB89636 is different from that of the MB89636R when using in external bus mode.

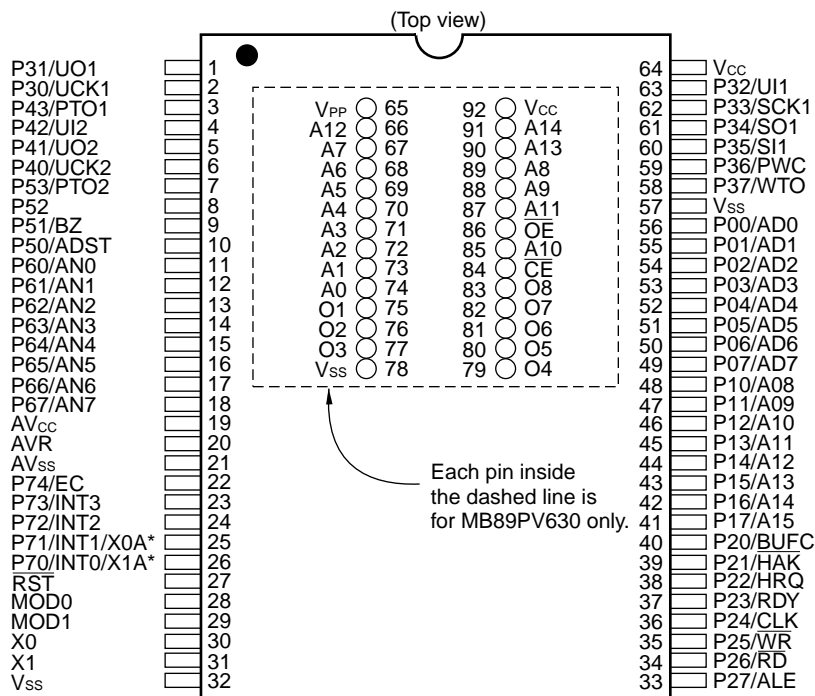| Address | Memory area | |
|---|---|---|
| | MB89636 | MB89636R |
| 0000$_H$ to 007F$_H$ | I/O area | I/O area |
| 0080$_H$ to 037F$_H$ | RAM area | RAM area |
| 0380$_H$ to 047F$_H$ | External area | Access prohibited |
| 0480$_H$ to 7FFF$_H$ | | External area |
| 8000$_H$ to 9FFF$_H$ | | Access prohibited |
| A000$_H$ to FFFF$_H$ | ROM area | ROM area |

- Other specifications

  Both MB89630 series and MB89635R/636R/637R is the same.

- Electrical specifications/electrical characteristics

  Electrical specifications of the MB89635R/636R/637R series are the same as that of the MB89630 series.

  Electrical characteristics of both the series are much the same.

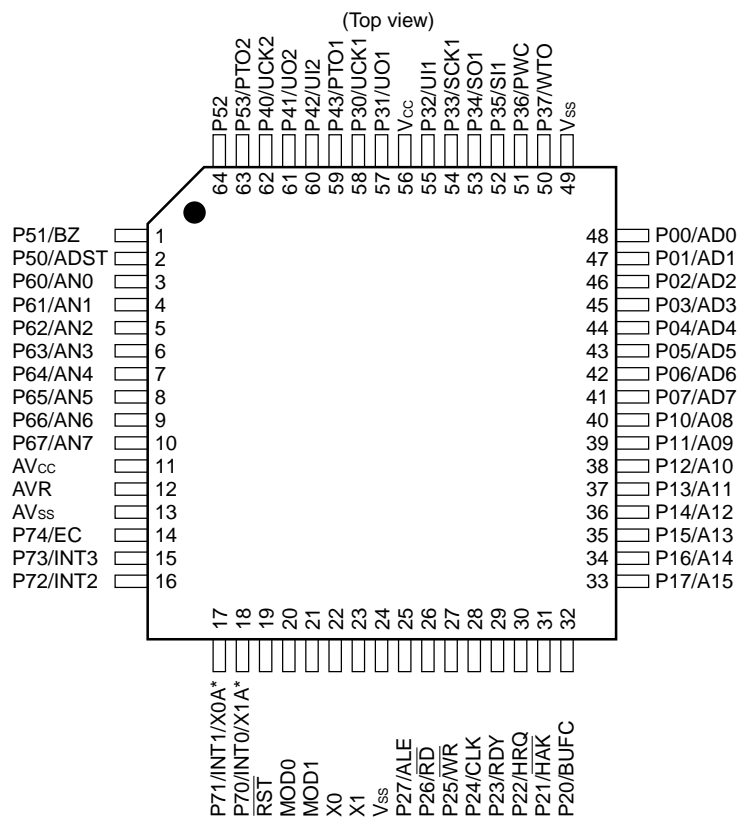## ■ CORRESPONDENCE BETWEEN THE MB89630 AND MB89630R SERIES

- The MB89630R series is the reduction version of the MB89630 series.

- The the MB89630 and MB89630R series consist of the following products:

| MB89630 series | MB89635 | MB89636 | MB89637 | MB89P637 | MB89PV630 |
|---|---|---|---|---|---|
| MB89630R series | MB89635R | MB89636R | MB89637R | | |

# ■ PIN ASSIGNMENT

(Top view)

P31/UO1 — 1
P30/UCK1 — 2
P43/PTO1 — 3
P42/UI2 — 4
P41/UO2 — 5
P40/UCK2 — 6
P53/PTO2 — 7
P52 — 8
P51/BZ — 9
P50/ADST — 10
P60/AN0 — 11
P61/AN1 — 12
P62/AN2 — 13
P63/AN3 — 14
P64/AN4 — 15
P65/AN5 — 16
P66/AN6 — 17
P67/AN7 — 18
AVcc — 19
AVR — 20
AVss — 21
P74/EC — 22
P73/INT3 — 23
P72/INT2 — 24
P71/INT1/X0A* — 25
P70/INT0/X1A* — 26
RST — 27
MOD0 — 28
MOD1 — 29
X0 — 30
X1 — 31
Vss — 32

Vpp 65     92 Vcc
A12 66     91 A14
A7 67      90 A13
A6 68      89 A8
A5 69      88 A9
A4 70      87 A11
A3 71      86 OE
A2 72      85 A10
A1 73      84 CE
A0 74      83 O8
O1 75      82 O7
O2 76      81 O6
O3 77      80 O5
Vss 78     79 O4

Each pin inside the dashed line is for MB89PV630 only.

64 — Vcc
63 — P32/UI1
62 — P33/SCK1
61 — P34/SO1
60 — P35/SI1
59 — P36/PWC
58 — P37/WTO
57 — Vss
56 — P00/AD0
55 — P01/AD1
54 — P02/AD2
53 — P03/AD3
52 — P04/AD4
51 — P05/AD5
50 — P06/AD6
49 — P07/AD7
48 — P10/A08
47 — P11/A09
46 — P12/A10
45 — P13/A11
44 — P14/A12
43 — P15/A13
42 — P16/A14
41 — P17/A15
40 — P20/BUFC
39 — P21/HAK
38 — P22/HRQ
37 — P23/RDY
36 — P24/CLK
35 — P25/WR
34 — P26/RD
33 — P27/ALE

(DIP-64P-M01)
(MDP-64C-P02)

*: When the dual-clock system is selected.

(Top view)

P52 64
P53/PTO2 63
P40/UCK2 62
P41/UO2 61
P42/UI2 60
P43/PTO1 59
P30/UCK1 58
P31/UO1 57
Vcc 56
P32/UI1 55
P33/SCK1 54
P34/SO1 53
P35/SI1 52
P36/PWC 51
P37/WTO 50
Vss 49

P51/BZ — 1
P50/ADST — 2
P60/AN0 — 3
P61/AN1 — 4
P62/AN2 — 5
P63/AN3 — 6
P64/AN4 — 7
P65/AN5 — 8
P66/AN6 — 9
P67/AN7 — 10
AVcc — 11
AVR — 12
AVss — 13
P74/EC — 14
P73/INT3 — 15
P72/INT2 — 16

48 — P00/AD0
47 — P01/AD1
46 — P02/AD2
45 — P03/AD3
44 — P04/AD4
43 — P05/AD5
42 — P06/AD6
41 — P07/AD7
40 — P10/A08
39 — P11/A09
38 — P12/A10
37 — P13/A11
36 — P14/A12
35 — P15/A13
34 — P16/A14
33 — P17/A15

17 P71/INT1/X0A*
18 P70/INT0/X1A*
19 RST
20 MOD0
21 MOD1
22 X0
23 X1
24 Vss
25 P27/ALE
26 P26/RD
27 P25/WR
28 P24/CLK
29 P23/RDY
30 P22/HRQ
31 P21/HAK
32 P20/BUFC

(FPT-64P-M23)     *: When the dual-clock system is selected.

(Top view)



P52 — 1
P51/BZ — 2
P50/ADST — 3
P60/AN0 — 4
P61/AN1 — 5
P62/AN2 — 6
P63/AN3 — 7
P64/AN4 — 8
P65/AN5 — 9
P66/AN6 — 10
P67/AN7 — 11
AVcc — 12
AVR — 13
AVss — 14
P74/EC — 15
P73/INT3 — 16
P72/INT2 — 17
P71/INT1/X0A* — 18
P70/INT0/X1A* — 19

51 — P37/WTO
50 — Vss
49 — P00/AD0
48 — P01/AD1
47 — P02/AD2
46 — P03/AD3
45 — P04/AD4
44 — P05/AD5
43 — P06/AD6
42 — P07/AD7
41 — P10/A08
40 — P11/A09
39 — P12/A10
38 — P13/A11
37 — P14/A12
36 — P15/A13
35 — P16/A14
34 — P17/A15
33 — P20/BUFC

Top pins (64–52): P53/PTO2, P40/UCK2, P41/UO2, P42/UI2, P43/PTO1, P30/UCK1, P31/UO1, Vcc, P32/UI1, P33/SCK1, P34/SO1, P35/SI1, P36/PWC

Bottom pins (20–32): RST, MOD0, MOD1, X0, X1, Vss, P27/ALE, P26/RD, P25/WR, P24/CLK, P23/RDY, P22/HRQ, P21/HAK

Each pin inside the dashed line is for MB89PV630 only.

(FPT-64P-M06)
(MQP-64C-P01)

*: When the dual-clock system is selected.

• **Pin assignment on package top (MB89PV630 only)**

| Pin no. | Pin name | Pin no. | Pin name | Pin no. | Pin name | Pin no. | Pin name |
|---|---|---|---|---|---|---|---|
| 65 | N.C. | 73 | A2 | 81 | N.C. | 89 | $\overline{OE}$ |
| 66 | Vpp | 74 | A1 | 82 | O4 | 90 | N.C. |
| 67 | A12 | 75 | A0 | 83 | O5 | 91 | A11 |
| 68 | A7 | 76 | N.C. | 84 | O6 | 92 | A9 |
| 69 | A6 | 77 | O1 | 85 | O7 | 93 | A8 |
| 70 | A5 | 78 | O2 | 86 | O8 | 94 | A13 |
| 71 | A4 | 79 | O3 | 87 | $\overline{CE}$ | 95 | A14 |
| 72 | A3 | 80 | Vss | 88 | A10 | 96 | Vcc |

N.C.: Internally connected. Do not use.

## ■ PIN DESCRIPTION

| Pin no. | | | Pin name | Circuit type | Function |
|---|---|---|---|---|---|
| SH-DIP[*1] MDIP[*2] | QFP2[*3] | QFP1[*4] MQFP[*5] | | | |
| 30 | 22 | 23 | X0 | A | Main clock crystal oscillator pins |
| 31 | 23 | 24 | X1 | | |
| 28 | 20 | 21 | MOD0 | D | Operating mode selection pins Connect directly to $V_{CC}$ or $V_{SS}$. |
| 29 | 21 | 22 | MOD1 | | |
| 27 | 19 | 20 | $\overline{RST}$ | C | Reset I/O pin This pin is an N-ch open-drain output type with a pull-up resistor, and a hysteresis input type. "L" is output from this pin by an internal reset source. The internal circuit is initialized by the input of "L". |
| 56 to 49 | 48 to 41 | 49 to 42 | P00/AD0 to P07/AD7 | F | General-purpose I/O ports When an external bus is used, these ports function as the multiplex pins of the lower address output and the data I/O. |
| 48 to 41 | 40 to 33 | 41 to 34 | P10/A08 to P17/A157 | F | General-purpose I/O ports When an external bus is used, these ports function as an upper address output. |
| 40 | 32 | 33 | P20/BUFC | H | General-purpose output port When an external bus is used, this port can also be used as a buffer control output by setting the BCTR. |
| 39 | 31 | 32 | P21/$\overline{HAK}$ | H | General-purpose output port When an external bus is used, this port can also be used as a hold acknowledge by setting the BCTR. |
| 38 | 30 | 31 | P22/HRQ | F | General-purpose output port When an external bus is used, this port can also be used as a hold request input by setting the BCTR. |
| 37 | 29 | 30 | P23/RDY | F | General-purpose output port When an external bus is used, this port functions as a ready input. |
| 36 | 28 | 29 | P24/CLK | H | General-purpose output port When an external bus is used, this port functions as a clock output. |
| 35 | 27 | 28 | P25/$\overline{WR}$ | H | General-purpose output port When an external bus is used, this port functions as a write signal output. |
| 34 | 26 | 27 | P26/$\overline{RD}$ | H | General-purpose output port When an external bus is used, this port functions as a read signal output. |

*1: DIP-64P-M01
*2: MDP-64C-P02
*3: FPT-64P-M23
*4: FPT-64P-M06
*5: MQP-M64C-P01

*(Continued)*

FUJITSU

| Pin no. | | | Pin name | Circuit type | Function |
|---|---|---|---|---|---|
| SH-DIP*1 MDIP*2 | QFP2*3 | QFP1*4 MQFP*5 | | | |
| 33 | 25 | 26 | P27/ALE | H | General-purpose output port When an external bus is used, this port functions as an address latch signal output. |
| 2 | 58 | 59 | P30/UCK1 | G | General-purpose I/O port Also serves as the clock I/O 1 for the UART. This port is a hysteresis input type. |
| 1 | 57 | 58 | P31/UO1 | F | General-purpose I/O port Also serves as the data output 1 for the UART. |
| 63 | 55 | 56 | P32/UI1 | G | General-purpose I/O port Also serves as the data input 1 for the UART. This port is a hysteresis input type. |
| 62 | 54 | 55 | P33/SCK1 | G | General-purpose I/O port Also serves as the data input for the 8-bit serial I/O. This port is a hysteresis input type. |
| 61 | 53 | 54 | P34/SO1 | F | General-purpose I/O port Also serves as the data output for the 8-bit serial I/O. |
| 60 | 52 | 53 | P35/SI1 | G | General-purpose I/O port Also serves as the data input for the 8-bit serial I/O. This port is a hysteresis input type. |
| 59 | 51 | 52 | P36/PWC | G | General-purpose I/O port Also serves as the measured pulse input for the 8-bit pulse width counter. This port is a hysteresis input type. |
| 58 | 50 | 51 | P37/WTO | F | General-purpose I/O port Also serves as the toggle output for the 8-bit pulse width counter. |
| 6 | 62 | 63 | P40/UCK2 | G | General-purpose I/O port Also serves as the clock I/O 2 for the UART. This port is a hysteresis input type. |
| 5 | 61 | 62 | P41/UO2 | F | General-purpose I/O port Also serves as the data output 2 for the UART. |
| 4 | 60 | 61 | P42/UI2 | G | General-purpose I/O port Also serves as the data input 2 for the UART. This port is a hysteresis input type. |
| 3 | 59 | 60 | P43/PTO1 | F | General-purpose I/O port Also serves as the toggle output for the 8-bit PWM timer. |
| 10 | 2 | 3 | P50/ADST | K | General-purpose I/O port Also serves as an A/D converter external activation. This port is a hysteresis input type. |

*1: DIP-64P-M01
*2: MDP-64C-P02
*3: FPT-64P-M23

*4: FPT-64P-M06
*5: MQP-M64C-P01

*(Continued)*

*(Continued)*

| Pin no. | | | Pin name | Circuit type | Function |
|---|---|---|---|---|---|
| SH-DIP[*1] MDIP[*2] | QFP2[*3] | QFP1[*4] MQFP[*5] | | | |
| 9 | 1 | 2 | P51/BZ | J | General-purpose I/O port<br>Also serves as a buzzer output. |
| 8 | 64 | 1 | P52 | J | General-purpose I/O port |
| 7 | 63 | 64 | P53/PTO2 | J | General-purpose I/O port<br>Also serves as the toggle output for the 8-bit PWM timer. |
| 11 to 18 | 3 to 10 | 4 to 11 | P60/AN0 to P67/AN7 | I | N-ch open-drain output ports<br>Also serve as an A/D converter analog input. |
| 26, 25 | 18, 17 | 19, 18 | P70/INT0/X1A, P71/INT1/X0A | B/E | Input-only ports<br>These ports are a hysteresis input type.<br>Also serve as an external interrupt input (at single-clock operation).<br>Subclock crystal oscillator pins (at dual-clock operation) |
| 24, 23 | 16, 15 | 17, 16 | P72/INT2, P73/INT3 | E | Input-only ports<br>Also serve as an external interrupt input.<br>These ports are a hysteresis input type. |
| 22 | 14 | 15 | P74/EC | E | General-purpose input port<br>Also serves as the external clock input for the 16-bit timer/counter.<br>This port is a hysteresis input type. |
| 64 | 56 | 57 | $V_{CC}$ | — | Power supply pin |
| 32, 57 | 24,49 | 25, 50 | $V_{SS}$ | — | Power supply (GND) pin |
| 19 | 11 | 12 | $AV_{CC}$ | — | A/D converter power supply pin |
| 20 | 12 | 13 | AVR | — | A/D converter reference voltage input pin |
| 21 | 13 | 14 | $AV_{SS}$ | — | A/D converter power supply pin<br>Use this pin at the same voltage as $V_{SS}$. |

*1: DIP-64P-M01  
*2: MDP-64C-P02  
*3: FPT-64P-M23  
*4: FPT-64P-M06  
*5: MQP-M64C-P01
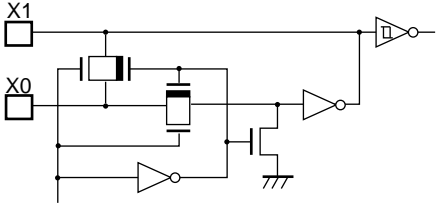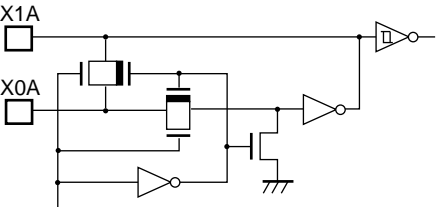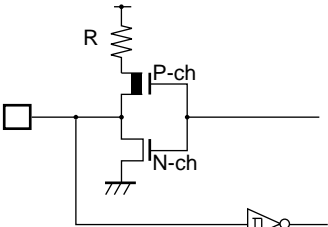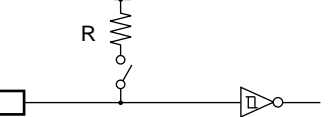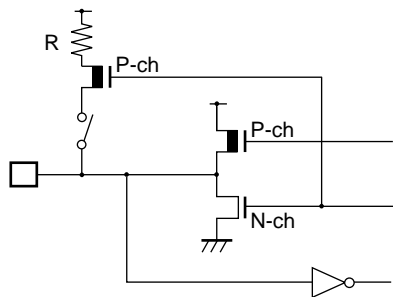
• **External EPROM pins (MB89PV630 only)**

| Pin no. | | Pin name | I/O | Function |
|---|---|---|---|---|
| MDIP | MQFP | | | |
| 65 | 66 | V$_{PP}$ | O | "H" level output pin |
| 66<br>67<br>68<br>69<br>70<br>71<br>72<br>73<br>74 | 67<br>68<br>69<br>70<br>71<br>72<br>73<br>74<br>75 | A12<br>A7<br>A6<br>A5<br>A4<br>A3<br>A2<br>A1<br>A0 | O | Address output pins |
| 75<br>76<br>77 | 77<br>78<br>79 | O1<br>O2<br>O3 | I | Data input pins |
| 78 | 80 | V$_{SS}$ | O | Power supply (GND) pin |
| 79<br>80<br>81<br>82<br>83 | 82<br>83<br>84<br>85<br>86 | O4<br>O5<br>O6<br>O7<br>O8 | I | Data input pins |
| 84 | 87 | $\overline{CE}$ | O | ROM chip enable pin<br>Outputs "H" during standby. |
| 85 | 88 | A10 | O | Address output pin |
| 86 | 89 | $\overline{OE}$ | O | ROM output enable pin<br>Outputs "L" at all times. |
| 87<br>88<br>89 | 91<br>92<br>93 | A11<br>A9<br>A8 | O | Address output pins |
| 90 | 94 | A13 | O | |
| 91 | 95 | A14 | O | |
| 92 | 96 | V$_{CC}$ | O | EPROM power supply pin |
| — | 65<br>76<br>81<br>90 | N.C. | — | Internally connected pins<br>Be sure to leave them open. |

## ■ I/O CIRCUIT TYPE

| Type | Circuit | Remarks |
|------|---------|---------|
| A | X1<br>X0<br>Standby control signal | • Crystal or ceramic oscillation type (main clock)<br>  External clock input selection versions of MB89PV630,<br>  MB89P637, MB89635R, MB89636R, and MB89637R<br>  At an oscillation feedback resistor of approximately<br>  1 M$\Omega$@5.0 V |
| B | X1A<br>X0A<br>Standby control signal | • Crystal or ceramic oscillation type (subclock)<br>  MB89PV630, MB89P637, MB89635R, MB89636R, and<br>  MB89637R with dual-clock system<br>  At an oscillation feedback resistor of approximately<br>  4.5 M$\Omega$@5.0 V |
| C | R  P-ch  N-ch | • At an output pull-up resistor (P-ch) of approximately<br>  50 k$\Omega$@5.0 V<br>• Hysteresis input |
| D | | |
| E | R | • Hysteresis input<br>• Pull-up resistor optional (except P70 and P71) |
| F | R  P-ch  P-ch  N-ch | • CMOS output<br>• CMOS input<br>• Pull-up resistor optional (except P22 and P23) |

*(Continued)*

# MB89630R Series

*(Continued)*

| Type | Circuit | Remarks |
|------|---------|---------|
| G | | • CMOS output<br>• Hysteresis input<br>• Pull-up resistor optional |
| H | | CMOS output |
| I | | Analog input |
| J | | • CMOS input<br>• Pull-up resistor optional |
| K | | • Hysteresis input<br>• Pull-up resistor optional |

FUJITSU

## ■ HANDLING DEVICES

### 1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than $V_{CC}$ or lower than $V_{SS}$ is applied to input and output pins other than medium- and high-voltage pins or if higher than the voltage which shows on "1. Absolute Maximum Ratings" in section "■ Electrical Characteristics" is applied between $V_{CC}$ and $V_{SS}$.

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog power supply (AV$_{CC}$ and AVR) and analog input from exceeding the digital power supply ($V_{CC}$) when the analog system power supply is turned on and off.

### 2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

### 3. Treatment of Power Supply Pins on Microcontrollers with A/D and D/A Converters

Connect to be AV$_{CC}$ = DAVC = $V_{CC}$ and AV$_{SS}$ = AVR = $V_{SS}$ even if the A/D and D/A converters are not in use.

### 4. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

### 5. Power Supply Voltage Fluctuations

Although $V_{CC}$ power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that $V_{CC}$ ripple fluctuations (P-P value) will be less than 10% of the standard $V_{CC}$ value at the commercial frequency (50 Hz to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

### 6. Precautions when Using an External Clock

When an external clock is used, oscillation stabilization time is required even for power-on reset (option selection) and wake-up from stop mode.
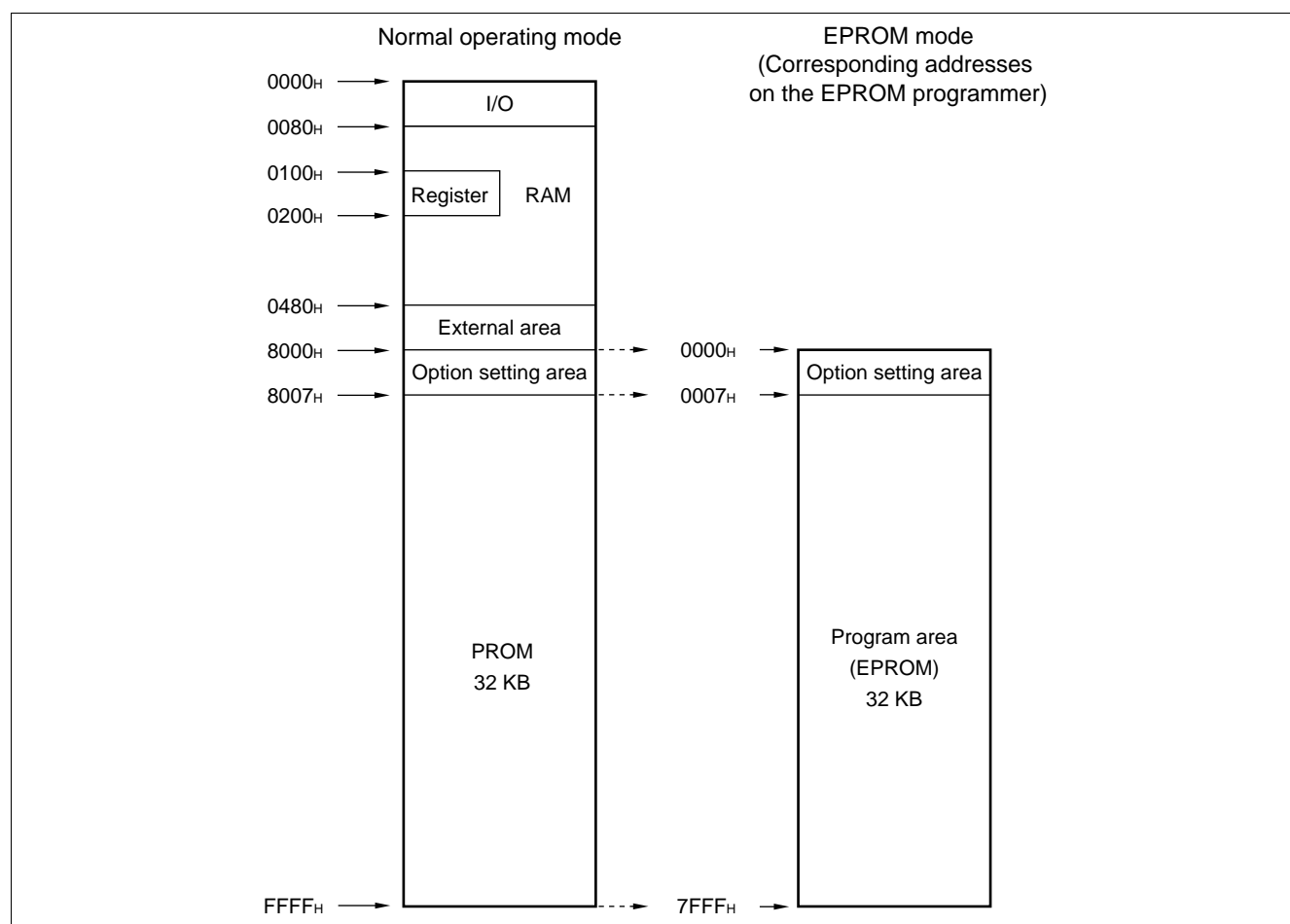
## ■ PROGRAMMING TO THE EPROM ON THE MB89P637

The MB89P637 is an OTPROM version of the MB89630 series.

### 1. Features

- 32-Kbytes PROM on chip
- Options can be set using the EPROM programmer.
- Equivalency to the MBM27C256A in EPROM mode (when programmed with the EPROM programmer)

### 2. Memory Space

Memory space in each mode is illustrated below.



### 3. Programming to the EPPROM

In EPROM mode, the MB89P637 functions equivalent to the MBM27C256A. This allows the PROM to be programmed with a general-purpose EPROM programmer by using the dedicated socket adapter.

However, the electronic signature mode cannot be used.

When the operating ROM area for a single chip is 32 Kbytes ($8007_H$ to $FFFF_H$) the EPROM can be programmed as follows:

- **Programming procedure**

(1) Set the EPROM programmer to the MBM27C256A.

(2) Load program data into the EPROM programmer at 0007$_H$ to 7FFF$_H$. (Note that addresses 8000$_H$ to FFFF$_H$ in the operating mode assign to 0000$_H$ to 7FFF$_H$ in EPROM mode).

(3) Load option data into addresses 0000$_H$ to 0006$_H$ of the EPROM programmer.
(For information about each corresponding option, see "8. OTPROM Option Bit Map".)

(4) Program with the EPROM programmer.

## 4. Recommended Screening Conditions

High-temperature aging is recommended as the pre-assembly screening procedure for a product with a blanked OTPROM microcomputer program.

```
┌─────────────────────────┐
│     Program, verify     │
└─────────────────────────┘
             │
             ▼
┌─────────────────────────┐
│          Aging          │
│     +150°C, 48 Hrs.     │
└─────────────────────────┘
             │
             ▼
┌─────────────────────────┐
│    Data verification    │
└─────────────────────────┘
             │
             ▼
    (      Assembly      )
```
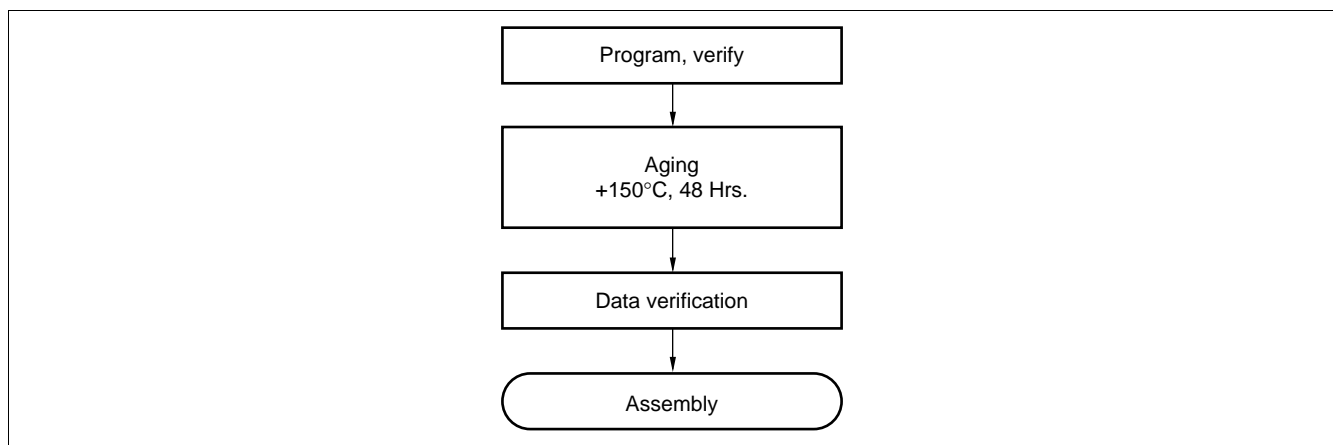
## 5. Programming Yield

All bits cannot be programmed at Fujitsu shipping test to a blanked OTPROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

## 6. OTPROM Option Bit Map

| Address | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| 0000$_H$ | Vacancy<br><br>Readable and writable | Vacancy<br><br>Readable and writable | Vacancy<br><br>Readable and writable | Single/dual-clock system<br>1: Dual clock<br>0: Single clock | Reset pin output<br>1: Yes<br>0: No | Power-on reset<br>1: Yes<br>0: No | Oscillation stabilization (/$F_{CH}$)<br>11:$2^{18}$/$F_{CH}$  01:$2^{17}$/$F_{CH}$<br>10:$2^{14}$/$F_{CH}$  00:$2^4$/$F_{CH}$ | |
| 0001$_H$ | P07<br>Pull-up<br>1: No<br>0: Yes | P06<br>Pull-up<br>1: No<br>0: Yes | P05<br>Pull-up<br>1: No<br>0: Yes | P04<br>Pull-up<br>1: No<br>0: Yes | P03<br>Pull-up<br>1: No<br>0: Yes | P02<br>Pull-up<br>1: No<br>0: Yes | P01<br>Pull-up<br>1: No<br>0: Yes | P00<br>Pull-up<br>1: No<br>0: Yes |
| 0002$_H$ | P17<br>Pull-up<br>1: No<br>0: Yes | P16<br>Pull-up<br>1: No<br>0: Yes | P15<br>Pull-up<br>1: No<br>0: Yes | P14<br>Pull-up<br>1: No<br>0: Yes | P13<br>Pull-up<br>1: No<br>0: Yes | P12<br>Pull-up<br>1: No<br>0: Yes | P11<br>Pull-up<br>1: No<br>0: Yes | P10<br>Pull-up<br>1: No<br>0: Yes |
| 0003$_H$ | P37<br>Pull-up<br>1: No<br>0: Yes | P36<br>Pull-up<br>1: No<br>0: Yes | P35<br>Pull-up<br>1: No<br>0: Yes | P34<br>Pull-up<br>1: No<br>0: Yes | P33<br>Pull-up<br>1: No<br>0: Yes | P32<br>Pull-up<br>1: No<br>0: Yes | P31<br>Pull-up<br>1: No<br>0: Yes | P30<br>Pull-up<br>1: No<br>0: Yes |
| 0004$_H$ | Vacancy<br><br>Readable and writable | Vacancy<br><br>Readable and writable | Vacancy<br><br>Readable and writable | Vacancy<br><br>Readable and writable | P43<br>Pull-up<br>1: No<br>0: Yes | P42<br>Pull-up<br>1: No<br>0: Yes | P41<br>Pull-up<br>1: No<br>0: Yes | P40<br>Pull-up<br>1: No<br>0: Yes |
| 0005$_H$ | Vacancy<br><br>Readable and writable | Vacancy<br><br>Readable and writable | Vacancy<br><br>Readable and writable | P74<br>Pull-up<br>1: No<br>0: Yes | P73<br>Pull-up<br>1: No<br>0: Yes | P72<br>Pull-up<br>1: No<br>0: Yes | Vacancy<br><br>Readable and writable | Vacancy<br><br>Readable and writable |
| 0006$_H$ | Vacancy<br><br>Readable and writable | Vacancy<br><br>Readable and writable | Vacancy<br><br>Readable and writable | Vacancy<br><br>Readable and writable | Vacancy<br><br>Readable and writable | Vacancy<br><br>Readable and writable | Vacancy<br><br>Readable and writable | Reserved bit<br><br>Readable and writable |

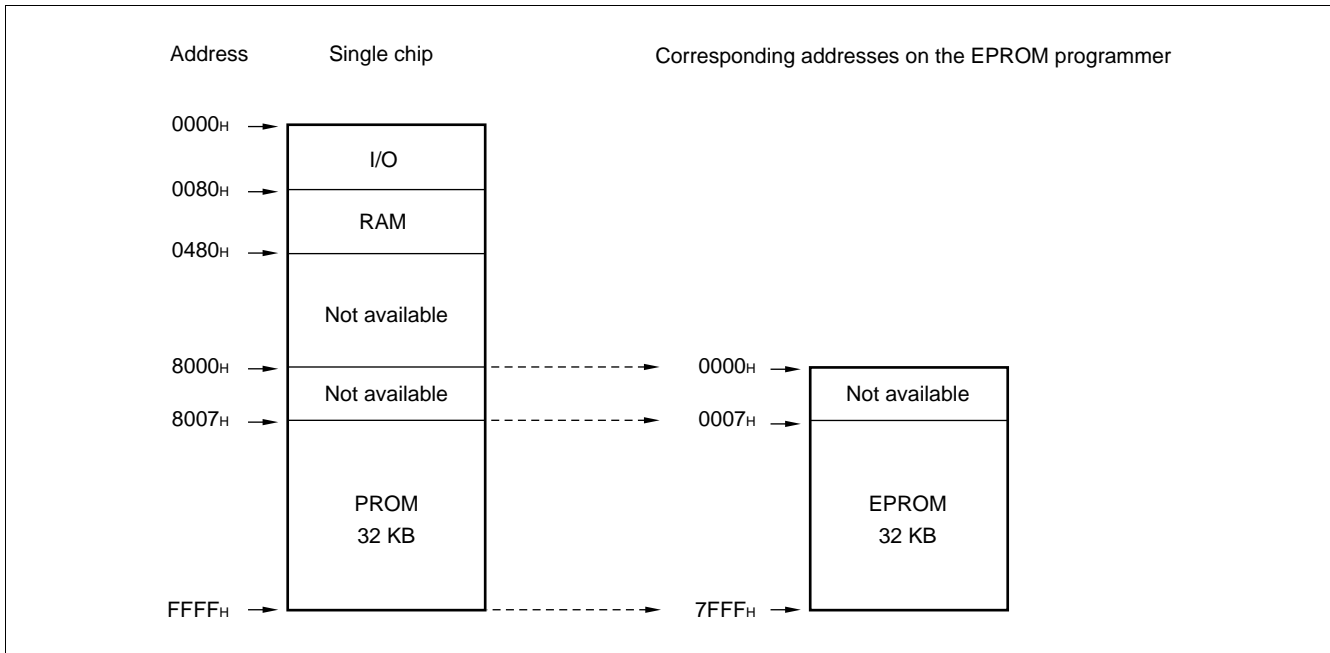Note: Each bit is set to '1' as the initialized value.

■ **PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE**

**1. EPROM for Use**

MBM27C256A-20CZ, MBM27C256A-20TV

**2. Memory Space**

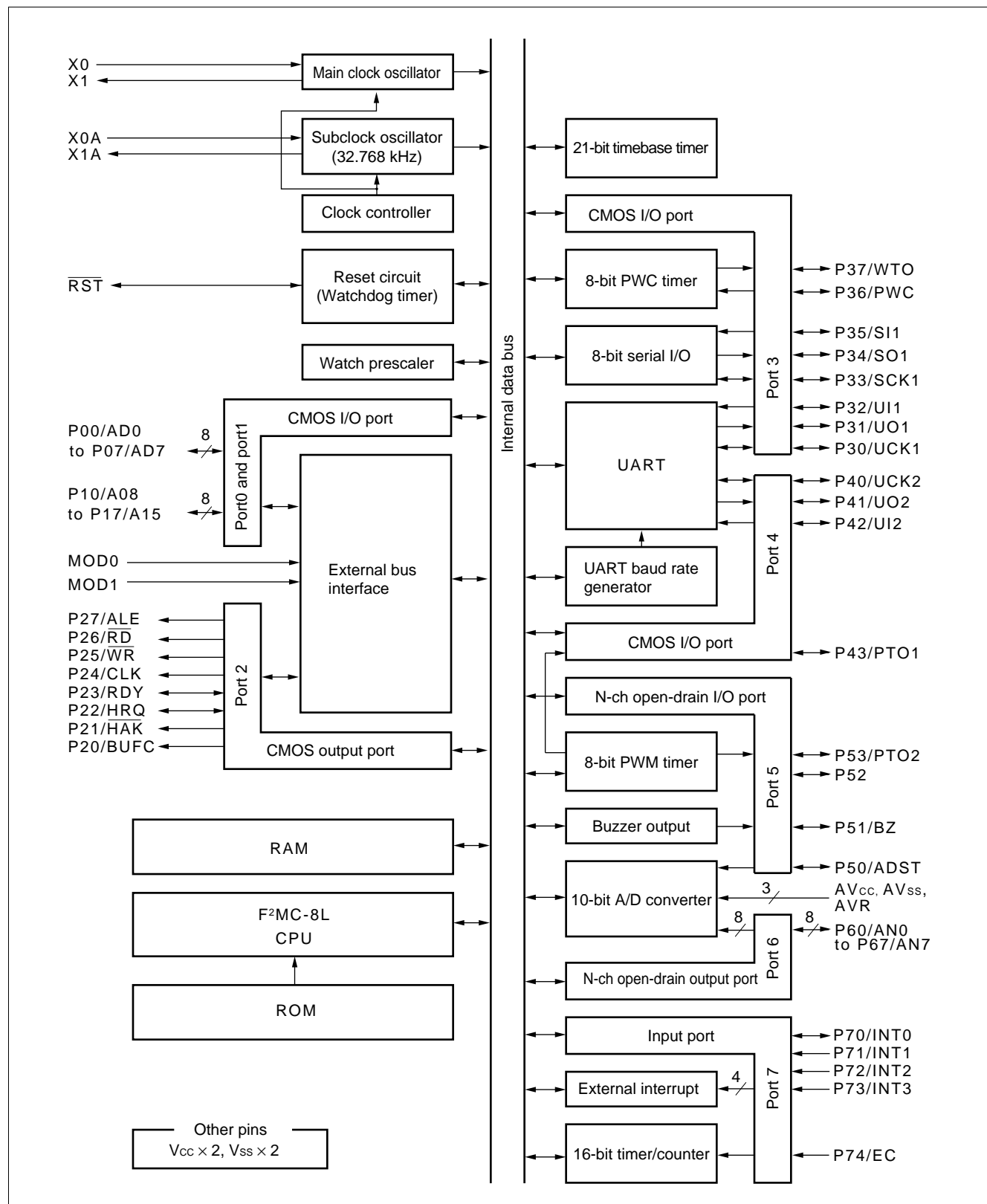Memory space in each mode, such as 32-Kbyte PROM, option area is diagrammed below.



**3. Programming to the EPROM**

(1) Set the EPROM programmer to the MBM27C256A.

(2) Load program data into the EPROM programmer at $0007_H$ to $7FFF_H$.

(3) Program to $0000_H$ to $7FFF_H$ with the EPROM programmer.

## ■ BLOCK DIAGRAM

## ■ CPU CORE

### 1. Memory Space

The microcontrollers of the MB89630R series offer 64 Kbytes of memory for storing all of I/O, data, and program areas. The I/O area is located at the lowest address. The data area is provided immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is located at exactly the opposite end of I/O area, that is, near the highest address. Provide the tables of interrupt reset vectors and vector call instructions toward the highest address within the program area. The memory space of the MB89630R series is structured as illustrated below.

• Memory space
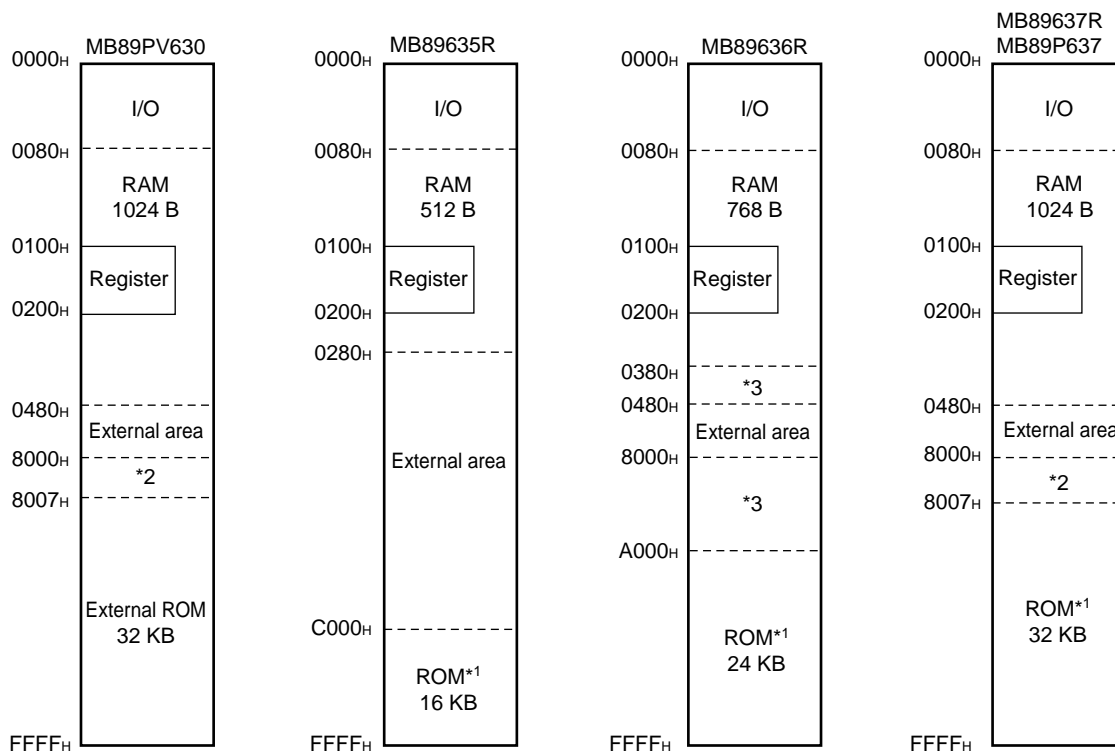


*1: The ROM area is an external area depending on the mode.

*2: Addresses 8000$_H$ to 8006$_H$ for the MB89P637 comprise an option area, do not use this area for the MB89PV630 and MB89637R.

*3: The access is forbidden in the external bus mode.

## 2. Registers

The F$^2$MC-8L family has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following dedicated registers are provided:

Program counter (PC): A 16-bit register for indicating the instruction storage positions

Accumulator (A): A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.

Temporary accumulator (T): A16-bit register which performs arithmetic operations with the accumulator When the instruction is an 8-bit data processing instruction, the lower byte is used.

Index register (IX): A16-bit register for index modification

Extra pointer (EP): A16-bit pointer for indicating a memory address

Stack pointer (SP): A16-bit register for indicating a stack area

Program status (PS): A16-bit register for storing a register pointer, a condition code

```
        ◄──── 16 bits ────►              Initial value

        ┌─────────────────┐
        │       PC        │   : Program counter          FFFD_H
        └─────────────────┘
        ┌─────────────────┐
        │        A        │   : Accumulator              Indeterminate
        └─────────────────┘
        ┌─────────────────┐
        │        T        │   : Temporary accumulator    Indeterminate
        └─────────────────┘
        ┌─────────────────┐
        │       IX        │   : Index register           Indeterminate
        └─────────────────┘
        ┌─────────────────┐
        │       EP        │   : Extra pointer            Indeterminate
        └─────────────────┘
        ┌─────────────────┐
        │       SP        │   : Stack pointer            Indeterminate
        └─────────────────┘
        ┌─────────────────┐
        │       PS        │   : Program status     I-flag = 0, IL1, IL0 = 11
        └─────────────────┘                         The other bit values are indeterminate.
```

The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)

**• Structure of the program status register**

```
        15    14    13    12    11   10    9     8    7    6    5     4    3    2    1    0
      ┌─────────────────────────────┬──────┬──────┬──────┬────┬────┬────────┬────┬────┬────┬────┐
  PS  │             RP              │Vacancy│Vacancy│Vacancy│ H  │ I  │IL1,IL0 │ N  │ Z  │ V  │ C  │
      └─────────────────────────────┴──────┴──────┴──────┴────┴────┴────────┴────┴────┴────┴────┘
      └───────────────────────────────────────────┘       └──────────────────────────────────┘
                          RP                                               CCR
```
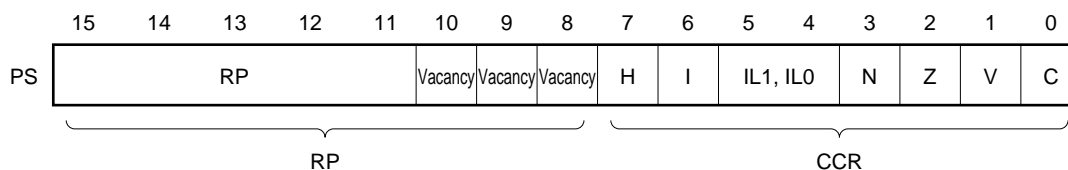
The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

**• Rule for conversion of actual addresses of the general-purpose register area**

RP          Lower OP codes

"0"  "0"  "0"  "0"  "0"  "0"  "0"  "1"  | R4  R3  R2  R1  R0 | b2  b1  b0 |

↓    ↓    ↓    ↓    ↓    ↓    ↓    ↓    ↓    ↓    ↓    ↓    ↓    ↓    ↓    ↓

Generated addresses  | A15 A14 A13 A12 A11 A10  A9   A8   A7   A6   A5   A4   A3   A2   A1   A0 |

The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

H-flag: Set to '1' when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared to '0' otherwise. This flag is for decimal adjustment instructions.

I-flag: Interrupt is enabled when this flag is set to '1'. Interrupt is disabled when the flag is cleared to '0'. Cleared to '0' at the reset.

IL1, IL0: Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

| IL1 | IL0 | Interrupt level | High-low |
|-----|-----|-----------------|----------|
| 0 | 0 | 1 | High |
| 0 | 1 | 1 | |
| 1 | 0 | 2 | |
| 1 | 1 | 3 | Low |

N-flag: Set to '1' if the MSB becomes to '1' as the result of an arithmetic operation. Cleared to '0' when the bit is cleared to '0'.

Z-flag: Set to '1' when an arithmetic operation results in 0. Cleared to '0' otherwise.

V-flag: Set to '1' if the complement on 2 overflows as a result of an arithmetic operation. Cleared to '0' if the overflow does not occur.

C-flag: Set to '1' when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared to '0' otherwise.
Set to the shift-out value in the case of a shift instruction.

The following general-purpose registers are provided:

General-purpose registers: An 8-bit register for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers and up to a total of 32 banks can be used on the MB89630R series. The bank currently in use is indicated by the register bank pointer (RP).

**• Register bank configuration**

This address = $0100_H + 8 \times (RP)$

| R 0 |
| R 1 |
| R 2 |
| R 3 |
| R 4 |
| R 5 |
| R 6 |
| R 7 |

} 32 banks

Memory area
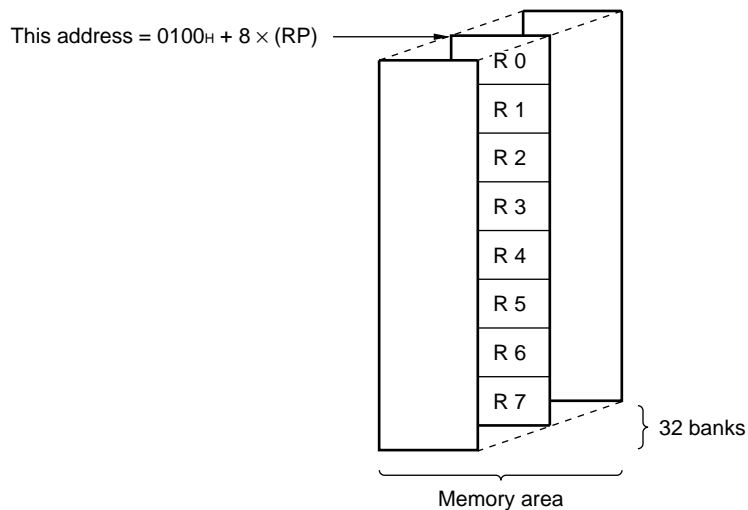
## ■ I/O MAP

| Address | Read/write | Register name | Register description |
|---------|-----------|---------------|---------------------|
| 00$_H$ | (R/W) | PDR0 | Port 0 data register |
| 01$_H$ | (W) | DDR0 | Port 0 data direction register |
| 02$_H$ | (R/W) | PDR1 | Port 1 data register |
| 03$_H$ | (W) | DDR1 | Port 1 data direction register |
| 04$_H$ | (R/W) | PDR2 | Port 2 data register |
| 05$_H$ | (W) | BCTR | External bus pin control register |
| 06$_H$ | | Vacancy | |
| 07$_H$ | (R/W) | SYCC | System clock control register |
| 08$_H$ | (R/W) | STBC | System clock control register |
| 09$_H$ | (R/W) | WDTE | Watchdog timer control register |
| 0A$_H$ | (R/W) | TBCR | Timebase timer control register |
| 0B$_H$ | (R/W) | WPCR | Watch prescaler control register |
| 0C$_H$ | (R/W) | CHG3 | Port 3 switching register |
| 0D$_H$ | (R/W) | PDR3 | Port 3 data register |
| 0E$_H$ | (W) | DDR3 | Port 3 data direction register |
| 0F$_H$ | (R/W) | PDR4 | Port 4 data register |
| 10$_H$ | (W) | DDR4 | Port 4 data direction register |
| 11$_H$ | (R/W) | BUZR | Buzzer register |
| 12$_H$ | (R/W) | PDR5 | Port 5 data register |
| 13$_H$ | (R/W) | PDR6 | Port 6 data register |
| 14$_H$ | (R) | PDR7 | Port 7 data register |
| 15$_H$ | (R/W) | PCR1 | PWC pulse width control register 1 |
| 16$_H$ | (R/W) | PCR2 | PWC pulse width control register 2 |
| 17$_H$ | (R/W) | RLBR | PWC reload buffer register |
| 18$_H$ | (R/W) | TMCR | 16-bit timer control register |
| 19$_H$ | (R/W) | TCHR | 16-bit timer count register (H) |
| 1A$_H$ | (R/W) | TCLR | 16-bit timer count register (L) |
| 1B$_H$ | | Vacancy | |
| 1C$_H$ | (R/W) | SMR1 | Serial mode register |
| 1D$_H$ | (R/W) | SDR1 | Serial data register |
| 1E$_H$ | | Vacancy | |
| 1F$_H$ | | Vacancy | |

*(Continued)*

*(Continued)*

| Address | Read/write | Register name | Register description |
|---|---|---|---|
| 20$_H$ | (R/W) | ADC1 | A/D converter control register 1 |
| 21$_H$ | (R/W) | ADC2 | A/D converter control register 2 |
| 22$_H$ | (R/W) | ADDH | A/D converter data register (H) |
| 23$_H$ | (R/W) | ADDL | A/D converter data register (L) |
| 24$_H$ | (R/W) | EIC1 | External interrupt control register 1 |
| 25$_H$ | (R/W) | EIC2 | External interrupt control register 2 |
| 26$_H$ | Vacancy | | |
| 27$_H$ | Vacancy | | |
| 28$_H$ | (R/W) | CNTR1 | PWM timer control register 1 |
| 29$_H$ | (R/W) | CNTR2 | PWM timer control register 2 |
| 2A$_H$ | (R/W) | CNTR3 | PWM timer control register 3 |
| 2B$_H$ | (W) | COMR1 | PWM timer compare register 1 |
| 2C$_H$ | (W) | COMR2 | PWM timer compare register 2 |
| 2D$_H$ | (R/W) | SMC | UART serial mode control register |
| 2E$_H$ | (R/W) | SRC | UART serial rate control register |
| 2F$_H$ | (R/W) | SSD | UART serial status/data register |
| 30$_H$ | (R)<br>(W) | SIDR<br>SODR | UART serial input data control register<br>UART serial output data control register |
| 31$_H$ to 7B$_H$ | Vacancy | | |
| 7C$_H$ | (W) | ILR1 | Interrupt level setting register 1 |
| 7D$_H$ | (W) | ILR2 | Interrupt level setting register 2 |
| 7E$_H$ | (W) | ILR3 | Interrupt level setting register 3 |
| 7F$_H$ | Vacancy | | |

Note:   Do not use vacancies.

## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Ratings

$(AV_{SS} = V_{SS} = 0.0 \text{ V})$

| Parameter | Symbol | Value Min. | Value Max. | Unit | Remarks |
|---|---|---|---|---|---|
| Power supply voltage | $V_{CC}$ | $V_{SS} - 0.3$ | $V_{SS} + 7.0$ | V | * |
| | $AV_{CC}$ | $V_{SS} - 0.3$ | $V_{SS} + 7.0$ | V | * |
| A/D converter reference input voltage | AVR | $V_{SS} - 0.3$ | $V_{SS} + 7.0$ | V | AVR must not exceed "$AV_{CC} + 0.3$ V". |
| Input voltage | $V_I$ | $V_{SS} - 0.3$ | $V_{CC} + 0.3$ | V | Except P50 to P53 |
| | $V_{I2}$ | $V_{SS} - 0.3$ | $V_{SS} + 7.0$ | V | P50 to P53 |
| Output voltage | $V_O$ | $V_{SS} - 0.3$ | $V_{CC} + 0.3$ | V | Except P50 to P53 |
| | $V_{O2}$ | $V_{SS} - 0.3$ | $V_{SS} + 7.0$ | V | P50 to P53 |
| "L" level maximum output current | $I_{OL}$ | — | 20 | mA | |
| "L" level average output current | $I_{OLAV}$ | — | 4 | mA | Average value (operating current × operating rate) |
| "L" level total maximum output current | $\Sigma I_{OL}$ | — | 100 | mA | |
| "L" level total average output current | $\Sigma I_{OLAV}$ | — | 40 | mA | Average value (operating current × operating rate) |
| "H" level maximum output current | $I_{OH}$ | — | −20 | mA | |
| "H" level average output current | $I_{OHAV}$ | — | −4 | mA | Average value (operating current × operating rate) |
| "H" level total maximum output current | $\Sigma I_{OH}$ | — | −50 | mA | |
| "H" level total average output current | $\Sigma I_{OHAV}$ | — | −20 | mA | Average value (operating current × operating rate) |
| Power consumption | $P_D$ | — | 500 | mW | |
| Operating temperature | $T_A$ | −40 | +85 | °C | |
| Storage temperature | Tstg | −55 | +150 | °C | |

\* : Use $AV_{CC}$ and $V_{CC}$ set at the same voltage.
   Take care so that $AV_{CC}$ does not exceed $V_{CC}$, such as when power is turned on.

WARNING:   Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## 2. Recommended Operating Conditions

$(AV_{SS} = V_{SS} = 0.0\ V)$

| Parameter | Symbol | Value | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min. | Max | | |
| Power supply voltage | $V_{CC}$ | 2.2* | 6.0* | V | Normal operation assurance range* MB89635R/636R/637R |
| | | 2.7* | 6.0* | V | Normal operation assurance range* MB89PV630/P637 |
| | $AV_{CC}$ | 1.5 | 6.0 | V | Retains the RAM state in stop mode |
| A/D converter reference input voltage | AVR | 3.0 | $AV_{CC}$ | V | |
| Operating temperature | $T_A$ | –40 | +85 | °C | |

* : These values vary with the operating frequency, instruction cycle, and analog assurance range. See Figure 1 and "5. A/D Converter Electrical Characteristics".

**Figure 1  Operating Voltage vs. Main Clock Operating Frequency**
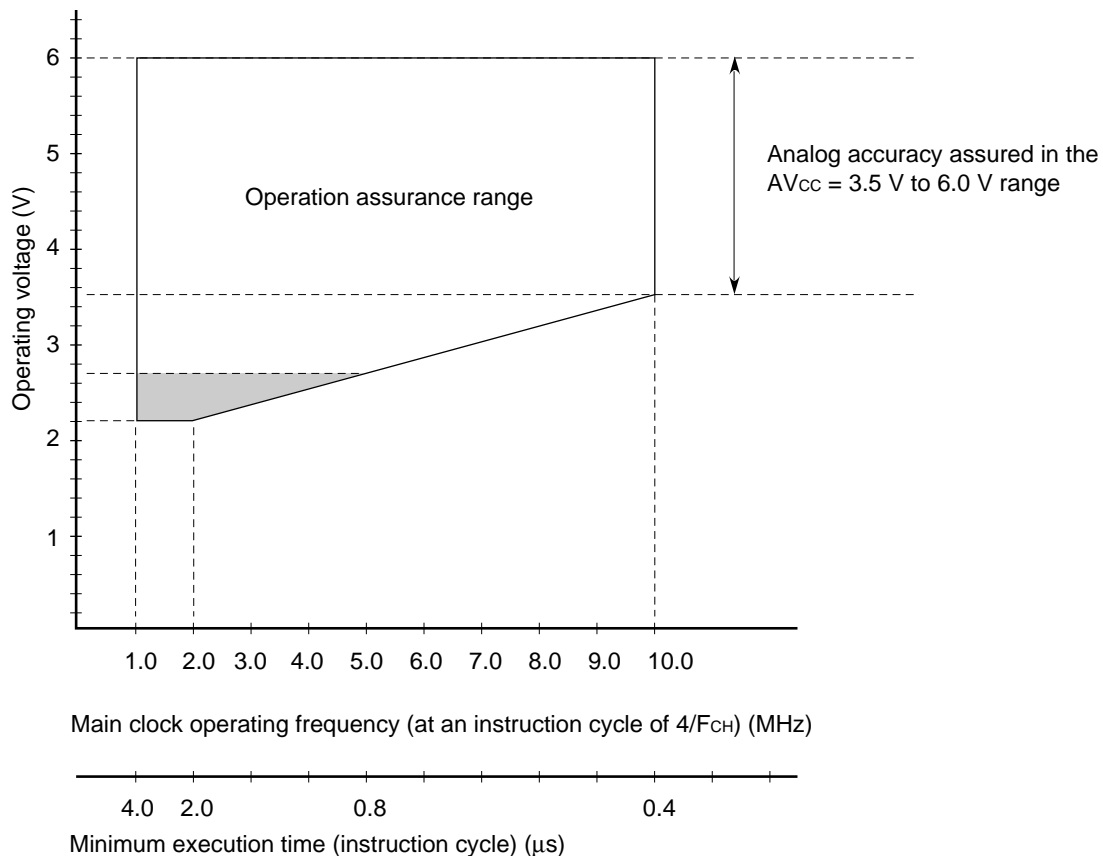


Note: The shaded area is assured only for the MB89635R/636R/637R.

Figure 1 indicates the operating frequency of the external oscillator at an instruction cycle of 4/$F_{CH}$.
Since the operating voltage range is dependent on the instruction cycle, see minimum execution time if the operating speed is switched using a gear.

FUJITSU

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

## 3. DC Characteristics

$(AV_{CC} = V_{CC} = 5.0 \text{ V}, AV_{SS} = V_{SS} = 0.0 \text{ V}, T_A = -40°C \text{ to } +85°C)$

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | | |
| "H" level input voltage | $V_{IH1}$ | P00 to P07, P10 to P17, P22, P23, P31, P34, P37, P41, P43, P51 to P53 | — | $0.7\ V_{CC}$ | — | $V_{CC} + 0.3$ | V | P51 to P53 with pull-up resistor |
| | $V_{IH2}$ | P51 to P53 | | $0.7\ V_{CC}$ | — | $V_{SS} + 6.0$ | V | Without pull-up resistor |
| | $V_{IHS}$ | $\overline{RST}$, MOD0, MOD1, P30, P32, P33, P35, P36, P40, P42,P50, P72 to P74 | | $0.8\ V_{CC}$ | — | $V_{CC} + 0.3$ | V | P50 with pull-up resistor |
| | $V_{IHS2}$ | P50, P70, P71 | | $0.8\ V_{CC}$ | — | $V_{SS} + 6.0$ | V | Without pull-up resistor |
| "L" level input voltage | $V_{IL}$ | P00 to P07, P10 to P17, P22, P23, P31, P34, P37, P41, P43 | | $V_{SS} - 0.3$ | — | $0.3\ V_{CC}$ | V | |
| | $V_{ILS}$ | P30, P32, P33, P35, P36, P40, P42, P50 to P53, P70 to P74, $\overline{RST}$, MOD0, MOD1 | | $V_{SS} - 0.3$ | — | $0.2\ V_{CC}$ | V | |
| Open-drain output pin application voltage | $V_D$ | P50 to P53 | | $V_{SS} - 0.3$ | — | $V_{SS} + 6.0$ | V | |
| "H" level output voltage | $V_{OH}$ | P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P43 | $I_{OH} = -2.0 \text{ mA}$ | 4.0 | — | — | V | |
| "L" level output voltage | $V_{OL}$ | P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P43, P50 to P53, P60 to P67, $\overline{RST}$ | $I_{OL} = 4.0 \text{ mA}$ | — | — | 0.4 | V | |
| Input leakage current (Hi-z output leakage current) | $I_{LI}$ | P00 to P07, P10 to P17, P20 to P23, P30 to P37, P40 to P43, P50 to P53, P70 to P74, MOD0, MOD1 | $0.0 \text{ V} < V_I < V_{CC}$ | — | — | $\pm 5$ | µA | Without pull-up resistor |

*(Continued)*

$(AV_{CC} = V_{CC} = 5.0 \text{ V}, AV_{SS} = V_{SS} = 0.0 \text{ V}, T_A = -40°C \text{ to } +85°C)$

| Parameter | Symbol | Pin name | Condition | Value Min. | Value Typ. | Value Max. | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| Pull-up resistance | $R_{PULL}$ | P00 to P07, P10 to P17, P30 to P37, P40 to P43, P50 to P53, P72 to P74 | $V_I = 0.0 \text{ V}$ | 25 | 50 | 100 | $k\Omega$ | With pull-up resistor |
| Power supply current[1] | $I_{CC1}$ | $V_{CC}$ | $F_{CH} = 10 \text{ MHz}$ $V_{CC} = 5.0 \text{ V}$ $t_{inst}{}^{*2} = 0.4 \text{ μs}$ | — | 12 | 20 | mA | |
| | $I_{CC2}$ | | $F_{CH} = 10 \text{ MHz}$ $V_{CC} = 3.0 \text{ V}$ $t_{inst}{}^{*2} = 6.4 \text{ μs}$ | — | 1.0 | 2 | mA | MB89635R/ 636R/637R/ PV630 |
| | | | | — | 1.5 | 2.5 | mA | MB89P637 |
| | $I_{CCS1}$ | | Sleep mode $F_{CH} = 10 \text{ MHz}$ $V_{CC} = 5.0 \text{ V}$ $t_{inst}{}^{*2} = 0.4 \text{ μs}$ | — | 3 | 7 | mA | |
| | $I_{CCS2}$ | | Sleep mode $F_{CH} = 10 \text{ MHz}$ $V_{CC} = 3.0 \text{ V}$ $t_{inst}{}^{*2} = 6.4 \text{ μs}$ | — | 0.5 | 1.5 | mA | |
| | $I_{CCL}$ | | $F_{CL} = 32.768 \text{ kHz}$, $V_{CC} = 3.0 \text{ V}$ Subclock mode | — | 50 | 100 | μA | MB89635R/ 636R/637R/ PV630 |
| | | | | — | 500 | 700 | μA | MB89P637 |
| | $I_{CCLS}$ | | $F_{CL} = 32.768 \text{ kHz}$, $V_{CC} = 3.0 \text{ V}$ Subclock sleep mode | — | 25 | 50 | μA | |
| | $I_{CCT}$ | | $F_{CL} = 32.768 \text{ kHz}$, $V_{CC} = 3.0 \text{ V}$ • Watch mode • Main clock stop mode at dual-clock system | — | 3 | 15 | μA | |
| | $I_{CCH}$ | | $T_A = +25°C$ • Subclock stop mode • Main clock stop mode at single-clock system | — | — | 1 | μA | |

*(Continued)*

*(Continued)*

$(AV_{CC} = V_{CC} = 5.0 \text{ V}, AV_{SS} = V_{SS} = 0.0 \text{ V}, T_A = -40°C \text{ to } +85°C)$

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|-----------|--------|----------|-----------|-------|-----|------|------|---------|
| | | | | Min. | Typ. | Max. | | |
| Power supply current[*1] | I_A | AV_CC | $F_{CH} = 10$ MHz, when A/D conversion operates. | — | 6 | — | mA | |
| | I_AH | | $F_{CH} = 10$ MHz, $T_A = +25°C$, when A/D conversion in a stop. | — | — | 1 | μA | |
| Input capacitance | C_IN | Other than AV_CC, AV_SS, V_CC, and V_SS | f = 1 MHz | — | 10 | — | pF | |

*1: The power supply current is measured at the external clock.

In the case of the MB89PV630, the current consumed by the connected EPROM and ICE is not counted.

*2: For information on $t_{inst}$, see "(4) Instruction Cycle" in "4. AC Characteristics".

## 4. AC Characteristics

### (1) Reset Timing

$(V_{CC} = 5.0 \text{ V} \pm 10\%, AV_{SS} = V_{SS} = 0.0 \text{ V}, T_A = -40°C \text{ to } +85°C)$

| Parameter | Symbol | Condition | Value | | Unit | Remarks |
|-----------|--------|-----------|-------|------|------|---------|
| | | | Min. | Max. | | |
| $\overline{RST}$ "L" pulse width | t_ZLZH | — | 48 t_HCYL | — | ns | |

DS07-12531-4E
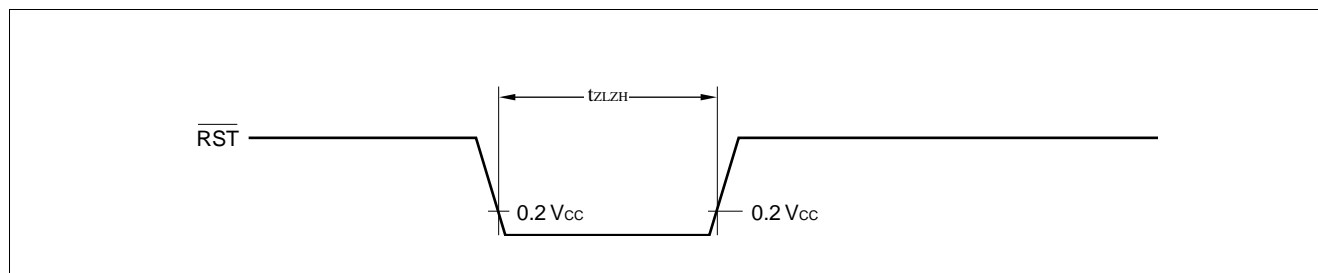
### (2) Specification for Power-on Reset

$(AV_{SS} = V_{SS} = 0.0 \text{ V}, T_A = -40°\text{C to } +85°\text{C})$

| Parameter | Symbol | Condition | Value Min. | Value Max. | Unit | Remarks |
|---|---|---|---|---|---|---|
| Power supply rising time | $t_R$ | — | — | 50 | ms | Power-on reset function only |
| Power supply cut-off time | $t_{OFF}$ | | 1 | — | ms | Min. interval time for the next power-on reset |

Note: Make sure that power supply rises within the selected oscillation stabilization time.
If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.
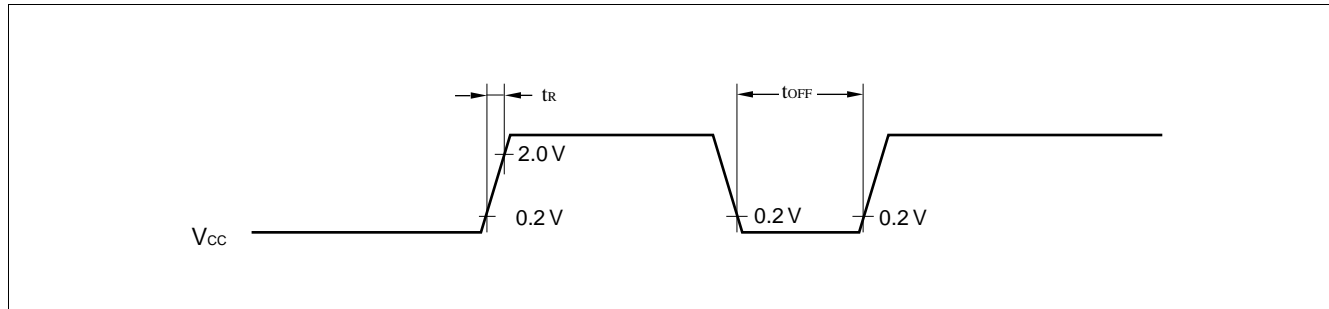


### (3) Clock Timing

$(AV_{SS} = V_{SS} = 0.0 \text{ V}, T_A = -40°\text{C to } +85°\text{C})$

| Parameter | Symbol | Pin name | Condition | Value Min. | Value Typ. | Value Max. | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| Clock frequency | $F_{CH}$ | X0, X1 | — | 1 | — | 10 | MHz | |
| | $F_{CL}$ | X0A, X1A | | — | 32.768 | — | kHz | |
| Clock cycle time | $t_{HCYL}$ | X0, X1 | | 100 | — | 1000 | ns | |
| | $t_{LCYL}$ | X0A, X1A | | — | 30.5 | — | µs | |
| Input clock pulse width | $P_{WH}$ $P_{WL}$ | X0 | | 20 | — | — | ns | External clock |
| | $P_{WLH}$ $P_{WLL}$ | X0A | | — | 15.2 | — | µs | External clock |
| Input clock rising/ falling time | $t_{CR}$ $t_{CF}$ | X0 | | — | — | 10 | ns | External clock |

FUJITSU

• **Main clock timing condition**
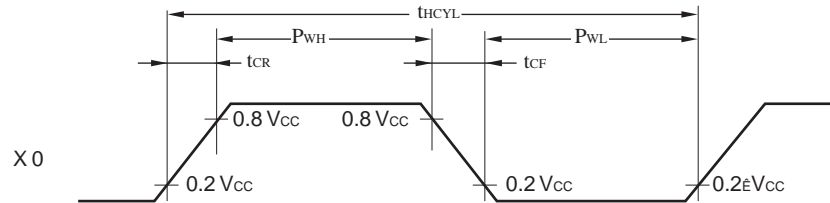
X 0

$t_{HCYL}$ $P_{WH}$ $P_{WL}$ $t_{CR}$ $t_{CF}$
0.8 $V_{CC}$  0.8 $V_{CC}$
0.2 $V_{CC}$  0.2 $V_{CC}$  0.2 $V_{CC}$

• **Main clock configurations**

When a crystal
or
ceramic reasonator is used

X0    X1

$F_{CH}$

When an external clock is used

X0    X1

Open

• **Subclock timing condition**

X0A

$t_{LCYL}$ $P_{WLH}$ $P_{WLL}$ $t_{CR}$ $t_{CF}$
0.8 $V_{CC}$  0.8 $V_{CC}$
0.2 $V_{CC}$  0.2 $V_{CC}$  0.2 $V_{CC}$

• **Subclock configurations**

When a crystal
or
ceramic reasonator is used

X0A    X1A

$F_{CL}$

When an external clock is used

X0A    X1A

Open

FUJITSU
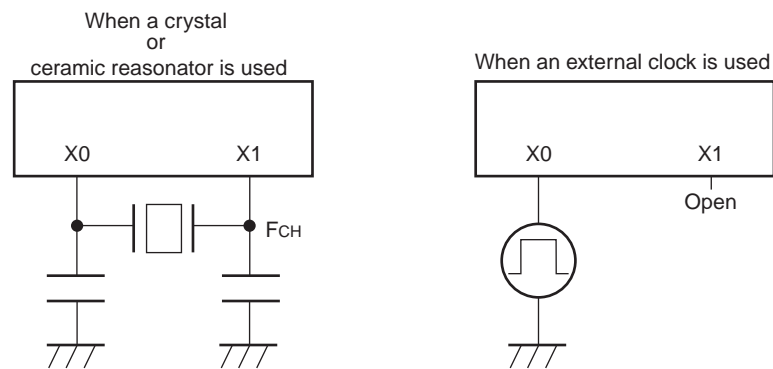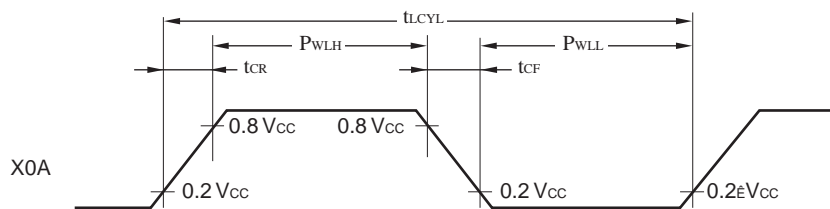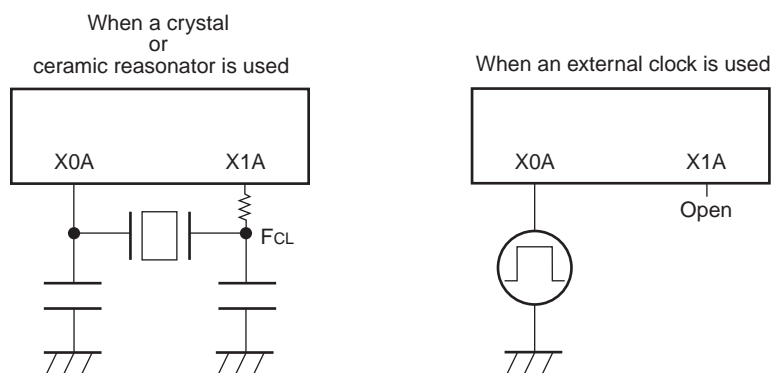
### (4)  Instruction Cycle

| Parameter | Symbol | Value (typical) | Unit | Remarks |
|---|---|---|---|---|
| Instruction cycle (minimum execution time) | $t_{inst}$ | $4/F_{CH}$, $8/F_{CH}$, $16/F_{CH}$, $64/F_{CH}$ | µs | $(4/F_{CH})$ $t_{inst}$ = 0.4 µs, operating at $F_{CH}$ = 10 MHz |
| | | $2/F_{CL}$ | µs | $t_{inst}$ = 61.036 µs, operating at $F_{CL}$ = 32.768 kHz |

Note:  Operating at 10 MHz, the cycle varies with the set execution time.

### (5)  Clock Output Timing

$(V_{CC} = 5.0$ V$\pm10\%$, AV$_{SS} = V_{SS} = 0.0$ V, $T_A = -40°C$ to $+85°C)$

| Parameter | Symbol | Pin name | Condition | Value Min. | Value Max. | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| Cycle time | $t_{CYC}$ | CLK | — | 1/2 $t_{inst}$* | — | µs | |
| CLK $\uparrow \rightarrow$ CLK $\downarrow$ | $t_{CHCL}$ | CLK | | 1/4 $t_{inst}$* − 70 ns | 1/4 $t_{inst}$* | µs | |

* : For information on $t_{inst}$, see "(4) Instruction Cycle".
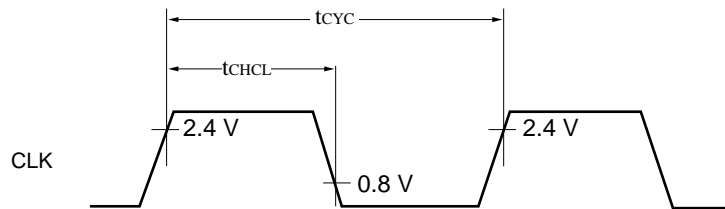
### (6) Bus Read Timing

$(V_{CC} = 5.0\ V\pm10\%, 10\ MHz, AV_{SS} = V_{SS} = 0.0\ V, T_A = -40°C\ to\ +85°C)$

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | | |
| Valid address $\to$ $\overline{RD}$ $\downarrow$ time | $t_{AVRL}$ | $\overline{RD}$, A15 to A08, AD7 to AD0 | | $1/4\ t_{inst}* - 64\ ns$ | — | $\mu s$ | |
| $\overline{RD}$ pulse width | $t_{RLRH}$ | $\overline{RD}$ | | $1/2\ t_{inst}* - 20\ ns$ | — | $\mu s$ | |
| Valid address $\to$ data read time | $t_{AVDV}$ | AD7 to AD0, A15 to A08 | | $1/2\ t_{inst}*$ | 200 | $\mu s$ | No wait |
| $\overline{RD}$ $\downarrow$ $\to$ data read time | $t_{RLDV}$ | $\overline{RD}$, AD7 to AD0 | | $1/2\ t_{inst}* - 80\ ns$ | 120 | $\mu s$ | No wait |
| $\overline{RD}$ $\uparrow$ $\to$ data hold time | $t_{RHDX}$ | AD7 to AD0, $\overline{RD}$ | | 0 | — | $\mu s$ | |
| $\overline{RD}$ $\uparrow$ $\to$ ALE $\uparrow$ time | $t_{RHLH}$ | $\overline{RD}$, ALE | — | $1/4\ t_{inst}* - 40\ ns$ | — | $\mu s$ | |
| $\overline{RD}$ $\uparrow$ $\to$ address loss time | $t_{RHAX}$ | $\overline{RD}$, A15 to A08 | | $1/4\ t_{inst}* - 40\ ns$ | — | $\mu s$ | |
| $\overline{RD}$ $\downarrow$ $\to$ CLK $\uparrow$ time | $t_{RLCH}$ | $\overline{RD}$, CLK | | $1/4\ t_{inst}* - 40\ ns$ | — | $\mu s$ | |
| CLK $\downarrow$ $\to$ $\overline{RD}$ $\uparrow$ time | $t_{CLRH}$ | | | 0 | — | ns | |
| $\overline{RD}$ $\downarrow$ $\to$ BUFC $\downarrow$ time | $t_{RLBL}$ | $\overline{RD}$, BUFC | | –5 | — | $\mu s$ | |
| BUFC $\uparrow$ $\to$ valid address time | $t_{BHAV}$ | A15 to A08, AD7 to AD0, BUFC | | 5 | — | $\mu s$ | |

* : For information on $t_{inst}$, see "(4) Instruction Cycle".

FUJITSU
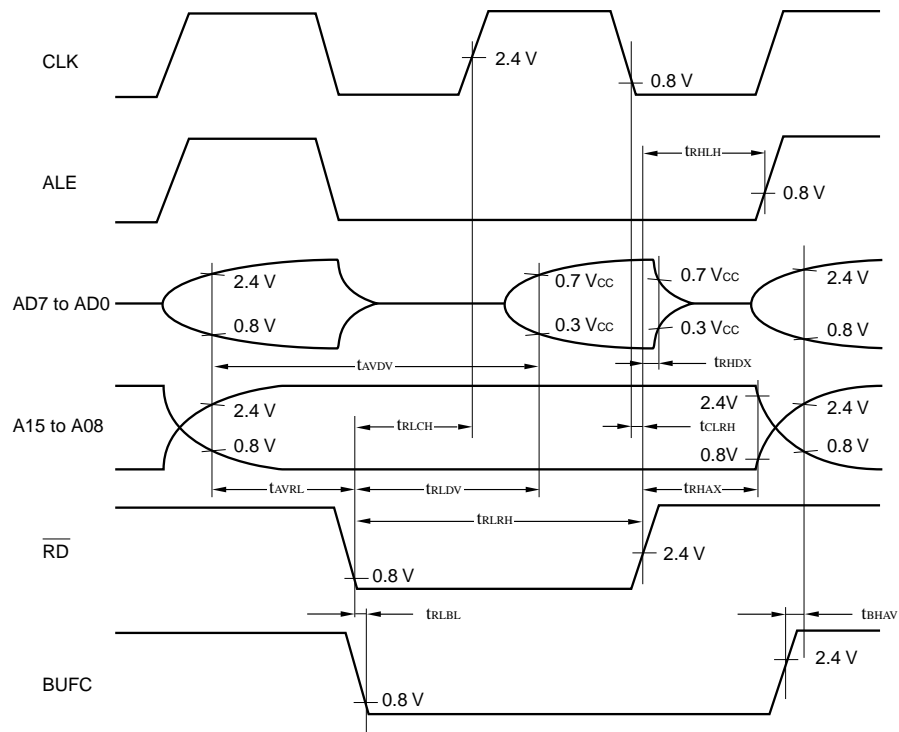
### (7) Bus Write Timing

(V<sub>CC</sub> = 5.0 V±10%, F<sub>CH</sub> = 10 MHz, AV<sub>SS</sub> = V<sub>SS</sub>= 0.0 V, T<sub>A</sub> = –40°C to +85°C)

 $(V_{CC} = 5.0\ V\pm10\%, F_{CH} = 10\ MHz, AV_{SS} = V_{SS} = 0.0\ V, T_A = -40°C\ to\ +85°C)$

| Parameter | Symbol | Pin name | Condition | Value Min. | Value Max. | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| Valid address → ALE ↓ time | $t_{AVLL}$ | AD7 to AD0, ALE A15 to A08 | | 1/4 $t_{inst}$*1 – 64 ns*2 | — | μs | |
| ALE ↓ time → address loss time | $t_{LLAX}$ | | | 5 | — | ns | |
| Valid address → $\overline{WR}$ ↓ time | $t_{AVWL}$ | $\overline{WR}$, ALE | | 1/4 $t_{inst}$*1 – 60 ns*2 | — | μs | |
| $\overline{WR}$ pulse width | $t_{WLWH}$ | $\overline{WR}$ | | 1/2 $t_{inst}$*1 – 20 ns*2 | — | μs | |
| Write data → $\overline{WR}$ ↑ time | $t_{DVWH}$ | AD7 to AD0, $\overline{WR}$ | | 1/2 $t_{inst}$*1 – 60 ns*2 | — | μs | |
| $\overline{WR}$ ↑ → address loss time | $t_{WHAX}$ | $\overline{WR}$, A15 to A08 | — | 1/4 $t_{inst}$*1 – 40 ns*2 | — | μs | |
| $\overline{WR}$ ↑ → data hold time | $t_{WHDX}$ | AD7 to AD0, $\overline{WR}$ | | 1/4 $t_{inst}$*1 – 40 ns*2 | — | μs | |
| $\overline{WR}$ ↑ → ALE ↑ time | $t_{WHLH}$ | $\overline{WR}$, ALE | | 1/4 $t_{inst}$*1 – 40 ns*2 | — | μs | |
| $\overline{WR}$ ↓ → CLK ↑ time | $t_{WLCH}$ | $\overline{WR}$, CLK | | 1/4 $t_{inst}$*1 – 40 ns*2 | — | μs | |
| CLK ↓ → $\overline{WR}$ ↑ time | $t_{CLWH}$ | | | 0 | — | ns | |
| ALE pulse width | $t_{LHLL}$ | ALE | | 1/4 $t_{inst}$*1 – 35 ns*2 | — | μs | |
| ALE ↓ → CLK ↑ time | $t_{LLCH}$ | ALE,CLK | | 1/4 $t_{inst}$*1 – 30 ns*2 | — | μs | |

*1: For information on $t_{inst}$, see "(4) Instruction Cycle".

*2: This characteristics are also applicable to the bus read timing.
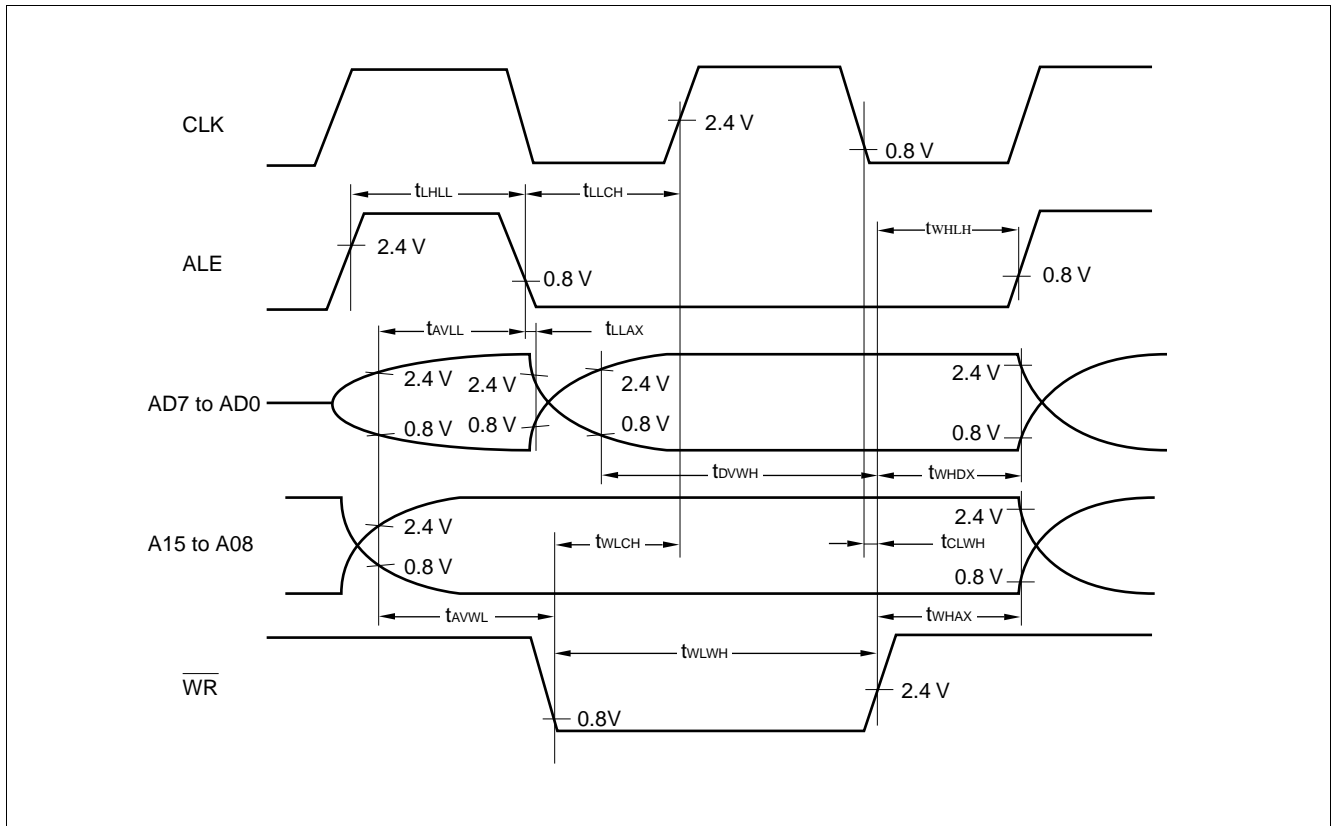
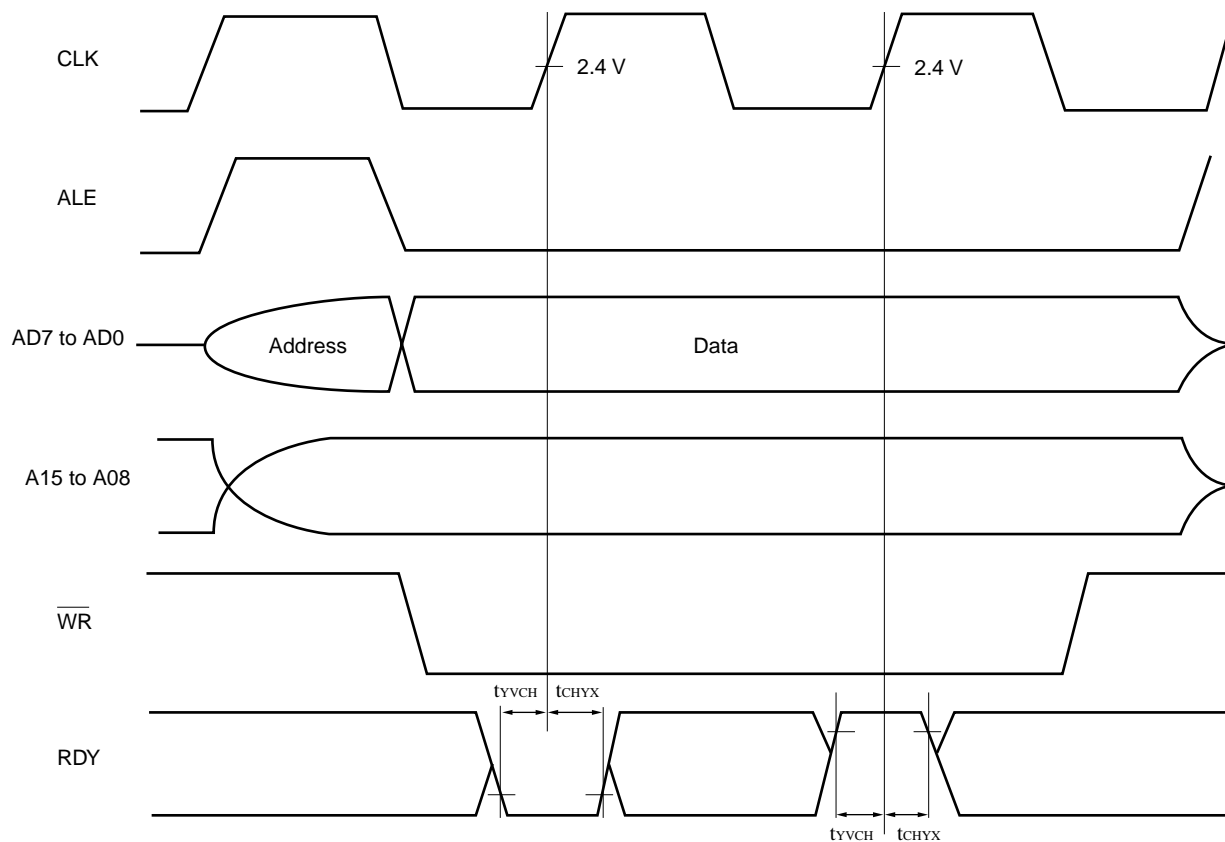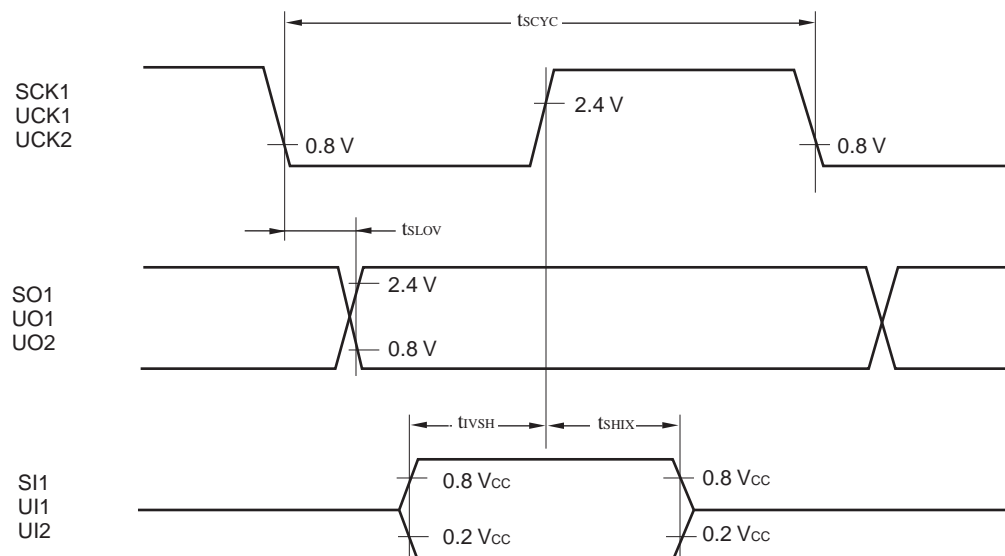### (8)   Ready Input Timing

$(V_{CC} = 5.0 \text{ V} \pm 10\%, F_{CH} = 10 \text{ MHz}, AV_{SS} = V_{SS} = 0.0 \text{ V}, T_A = -40°C \text{ to } +85°C)$

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | | |
| RDY valid $\rightarrow$ CLK $\uparrow$ time | $t_{YVCH}$ | RDY, CLK | — | 60 | — | ns | * |
| CLK $\uparrow$ $\rightarrow$ RDY loss time | $t_{CHYX}$ | | | 0 | — | ns | * |

* : This characteristics are also applicable to the read cycle.



Note: The bus cycle is also extended in the read cycle in the same manner.

### (9) Serial I/O Timing

$(V_{CC} = 5.0 \ V \pm 10\%, \ F_{CH} = 10 \ MHz, \ AV_{SS} = V_{SS} = 0.0 \ V, \ T_A = -40°C \ to \ +85°C)$

| Parameter | Symbol | Pin name | Condition | Value Min. | Value Max. | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| Serial clock cycle time | $t_{SCYC}$ | SCK1, UCK1, UCK2 | Internal shift clock mode | 2 $t_{inst}$* | — | μs | |
| SCK1 $\downarrow \rightarrow$ SO1 time<br>UCK1 $\downarrow \rightarrow$ UO1 time<br>UCK2 $\downarrow \rightarrow$ UO2 time | $t_{SLOV}$ | SCK1, SO1<br>UCK1, UO1<br>UCK2, UO2 | | –200 | 200 | ns | |
| Valid SI1 $\rightarrow$ SCK1 $\uparrow$<br>Valid UI1 $\rightarrow$ UCK1 $\uparrow$<br>Valid UI2 $\rightarrow$ UCK2 $\uparrow$ | $t_{IVSH}$ | SI1, SCK1<br>UI1, UCK1<br>UI2, UCK2 | | 1/2 $t_{inst}$* | — | μs | |
| SCK1 $\uparrow \rightarrow$ valid SI1 hold time<br>UCK1 $\uparrow \rightarrow$ valid UI1 hold time<br>UCK2 $\uparrow \rightarrow$ valid UI2 hold time | $t_{SHIX}$ | SCK1, SI1<br>UCK1, UI1<br>UCK2, UI2 | | 1/2 $t_{inst}$* | — | μs | |
| Serial clock "H" pulse width | $t_{SHSL}$ | SCK1, UCK1, UCK2 | External shift clock mode | 1 $t_{inst}$* | — | μs | |
| Serial clock "L" pulse width | $t_{SLSH}$ | SCK1, UCK1, UCK2 | | 1 $t_{inst}$* | — | μs | |
| SCK1 $\downarrow \rightarrow$ SO1 time<br>UCK1 $\downarrow \rightarrow$ UO1 time<br>UCK2 $\downarrow \rightarrow$ UO2 time | $t_{SLOV}$ | SCK1, SO1<br>UCK1, UO1<br>UCK2, UO2 | | 0 | 200 | ns | |
| Valid SI1 $\rightarrow$ SCK1 $\uparrow$<br>Valid UI1 $\rightarrow$ UCK1 $\uparrow$<br>Valid UI2 $\rightarrow$ UCK2 $\uparrow$ | $t_{IVSH}$ | SI1, SCK1<br>UI1, UCK1<br>UI2, UCK2 | | 1/2 $t_{inst}$* | — | μs | |
| SCK1 $\downarrow \rightarrow$ valid SI1 hold time<br>UCK1 $\downarrow \rightarrow$ valid UI1 hold time<br>UCK2 $\downarrow \rightarrow$ valid UI2 hold time | $t_{SHIX}$ | SCK1, SI1<br>UCK1, UI1<br>UCK2, UI2 | | 1/2 $t_{inst}$* | — | μs | |

* : For information on $t_{inst}$, see "(4) Instruction Cycle".

• **Internal shift clock mode**



• **External shift clock mode**
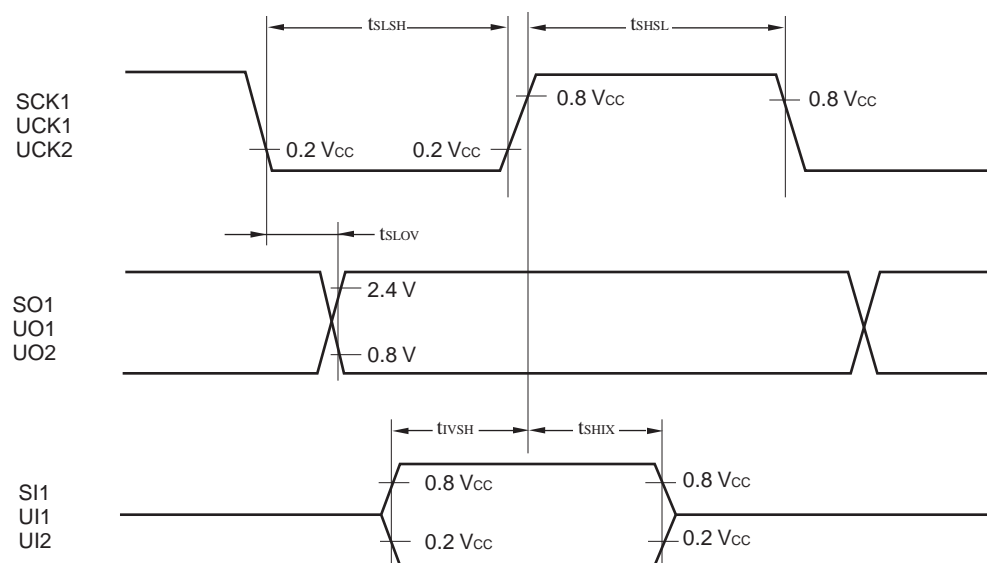
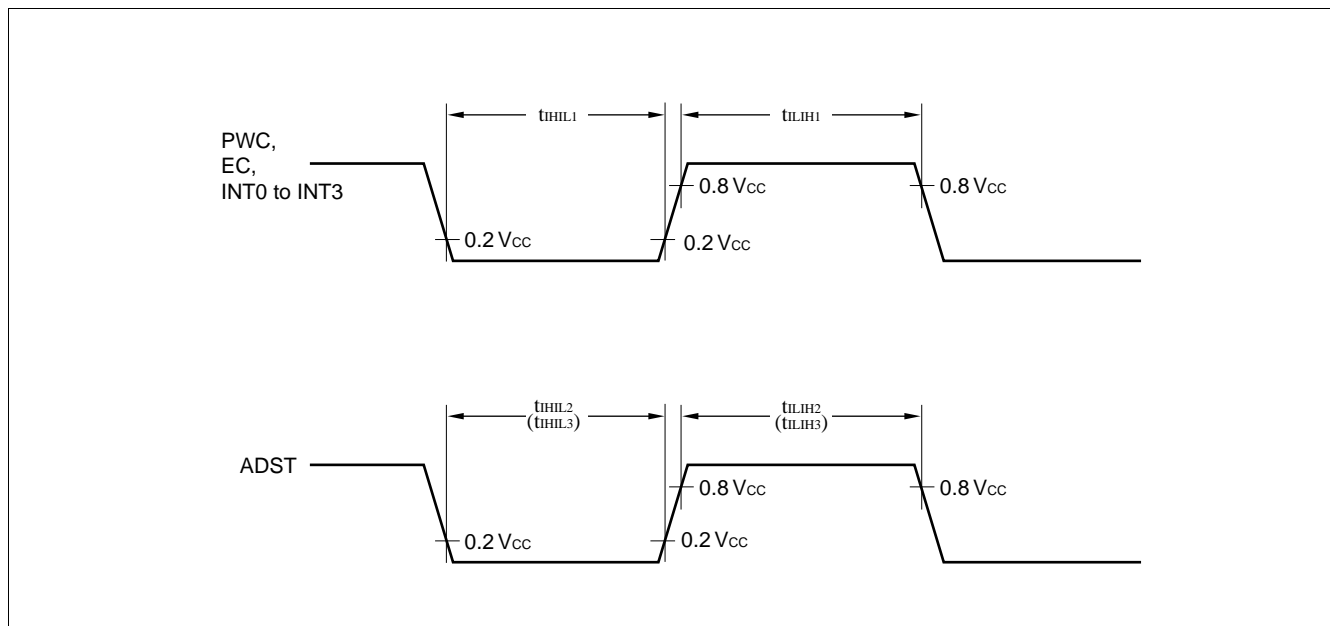### (10) Peripheral Input Timing

$(V_{CC} = 5.0 \text{ V} \pm 10\%, AV_{SS} = V_{SS} = 0.0 \text{ V}, T_A = -40°C \text{ to } +85°C)$

| Parameter | Symbol | Pin name | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | | Min. | Max. | | |
| Peripheral input "H" pulse width 1 | $t_{ILIH1}$ | PWC, INT0 to INT3,EC | $2\ t_{inst}$* | — | μs | |
| Peripheral input "L" pulse width 1 | $t_{IHIL1}$ | | $2\ t_{inst}$* | — | μs | |
| Peripheral input "H" pulse width 2 | $t_{ILIH2}$ | ADST | $2^8\ t_{inst}$* | — | μs | A/D mode |
| Peripheral input "L" pulse width 2 | $t_{IHIL2}$ | | $2^8\ t_{inst}$* | — | μs | A/D mode |
| Peripheral input "H" pulse width 3 | $t_{ILIH3}$ | ADST | $2^8\ t_{inst}$* | — | μs | Sense mode |
| Peripheral input "L" pulse width 3 | $t_{IHIL3}$ | | $2^8\ t_{inst}$* | — | μs | Sense mode |

* : For information on $t_{inst,}$ see "(4) Instruction Cycle".

## 5. A/D Converter Electrical Characteristics

(AV$_{CC}$ = V$_{CC}$ = 3.5 V to 6.0 V, F$_{CH}$ = 10 MHz, AV$_{SS}$ = V$_{SS}$ = 0.0 V, T$_A$ = –40°C to +85°C)

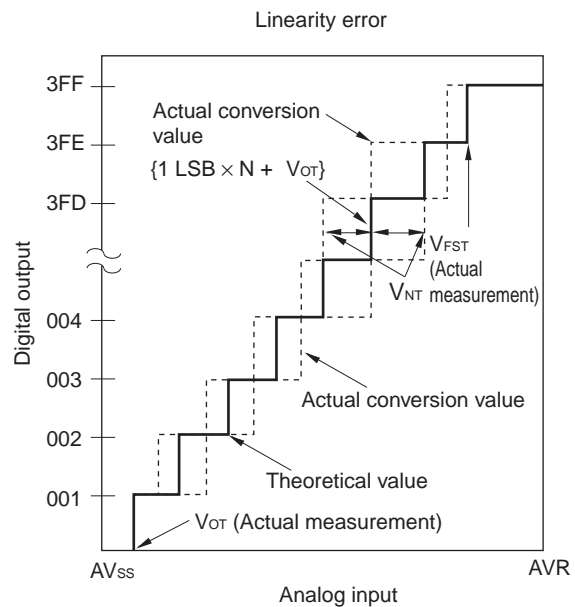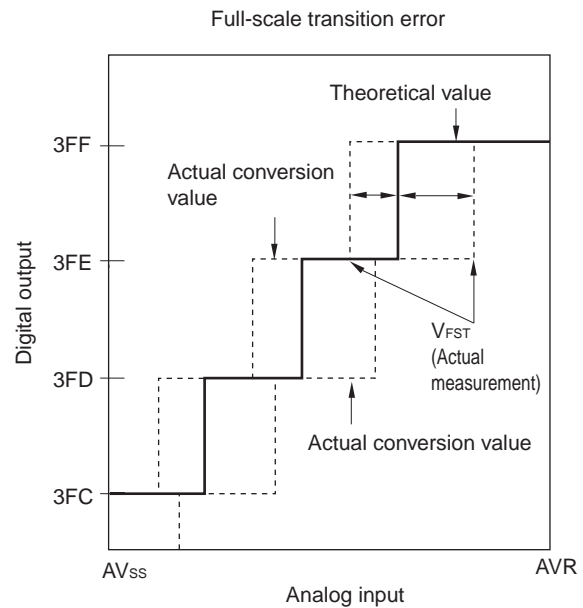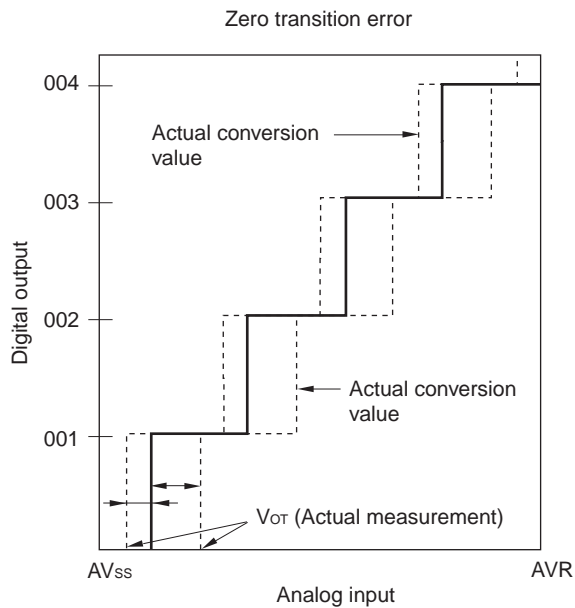| Parameter | Symbol | Pin name | Value | | | Unit | Remarks |
| --- | --- | --- | --- | --- | --- | --- | --- |
| | | | Min. | Typ. | Max. | | |
| Resolution | — | — | — | — | 10 | bit | At AV$_{CC}$ = V$_{CC}$ |
| Linearity error | | | — | — | ±2.0 | LSB | |
| Differential linearity error | | | — | — | ±1.5 | LSB | |
| Total error | | | — | — | ±3.0 | LSB | |
| Zero transition voltage | V$_{OT}$ | AN0 to AN7 | AV$_{SS}$ – 1.5 LSB | AV$_{SS}$ + 0.5 LSB | AV$_{SS}$ + 2.5 LSB | V | |
| Full-scale transition voltage | V$_{FST}$ | | AVR – 3.5 LSB | AVR – 1.5 LSB | AVR + 0.5 LSB | V | |
| Interchannel disparity | — | — | — | — | 4 | LSB | |
| A/D mode conversion time | | | — | 13.2 | — | µs | At 10 MHz oscillation |
| Analog port input current | I$_{AIN}$ | AN0 to AN7 | — | — | 10 | µA | |
| Analog input voltage | — | | 0.0 | — | AVR | V | |
| Reference voltage | | — | 0.0 | — | AV$_{CC}$ | V | |
| Reference voltage supply current | I$_R$ | | — | 200 | — | µA | AVR = 5.0 V |

FUJITSU

## 6. A/D Converter Glossary

- Resolution
  Analog changes that are identifiable with the A/D converter
- Linearity error
  The deviation of the straight line connecting the zero transition point ("00 0000 0000" ↔ "00 0000 0001") with the full-scale transition point ("11 1111 1110" ↔ "11 1111 1111") from actual conversion characteristics
- Differential linearity error
  The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value
- Total error (unit: LSB)
  The difference between theoretical and actual conversion values caused by the zero transition error, full-scale transition error, linearity error, quantization error, and noise



Theoretical I/O characteristics

Total error

$$1 \text{ LSB} = \frac{V_{FST} - V_{OT}}{1022} \text{ (V)}$$

$$\text{Digital output N total error} = \frac{V_{NT} - \{1 \text{ LSB} \times N + 0.5 \text{ LSB}\}}{1 \text{ LSB}}$$

*(Continued)*

(Continued)

### Zero transition error

Digital output

004
003
002
001

Actual conversion value

Actual conversion value

$V_{OT}$ (Actual measurement)

$AV_{SS}$

AVR

Analog input

### Full-scale transition error

Digital output

3FF
3FE
3FD
3FC

Theoretical value

Actual conversion value

$V_{FST}$ (Actual measurement)

Actual conversion value

$AV_{SS}$

AVR

Analog input

### Linearity error

Digital output

3FF
3FE
3FD

004
003
002
001

Actual conversion value {1 LSB × N + $V_{OT}$}

$V_{FST}$ (Actual $V_{NT}$ measurement)

Actual conversion value

Theoretical value

$V_{OT}$ (Actual measurement)

$AV_{SS}$

AVR

Analog input

### Differential linearity error

Digital output

N + 1
N
N - 1
N - 2

Theoretical value

Actual conversion value

$V_{(N+1)T}$

$V_{NT}$

Actual conversion value

$AV_{SS}$

AVR

Analog input

Digital output N linearity error = $\dfrac{V_{NT} - \{1\ LSB \times N + V_{OT}\}}{1\ LSB}$

Digital output N differential linearity error = $\dfrac{V_{(N+1)T} - V_{NT}}{1\ LSB} - 1$

FUJITSU

## 7. Notes on Using A/D Converter

• **Input impedance of the analog input pins**
The output impedance of the external circuit for the analog input must satisfy the following conditions.
If the output impedance of the external circuit is too high, an analog voltage sampling time might be insufficient (sampling time = 6 $\mu$s at 10 MHz oscillation.) Therefore, it is recommended to keep the output impedance of the external circuit below 10 k$\Omega$.

• **Analog input circuit model**

Analog input

$R_{ON1}$    $R_{ON2}$    $C_0$    Converter    $C_1$

$R_{ON1}$:  Approx. 1.5 k$\Omega$
$R_{ON2}$:  Approx. 1.5 k$\Omega$
$C_0$:    Approx. 60 pF
$C_1$:    Approx. 4 pF
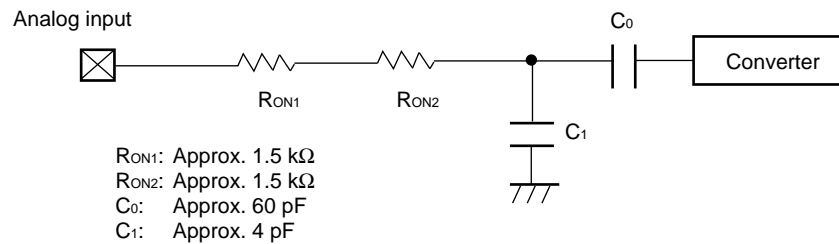
Note: The values mentioned here should be used as a guideline.

• **Error**
The smaller the | AVR–AVss |, the greater the error would become relatively.

## ■ CHARACTERISTICS EXAMPLE

**(1) "L" Level Output Voltage**

VOL vs. IOL

$V_{OL}$ (V)

$V_{CC} = 3.0$ V
$V_{CC} = 4.0$ V
$T_A = +25°C$
$V_{CC} = 5.0$ V
$V_{CC} = 6.0$ V

0.5
0.4
0.3
0.2
0.1

0  1  2  3  4  5  6  7  8  9  10

$I_{OL}$ (mA)

**(2) "H" Level Output Voltage**

VCC - VOH vs. IOH

$V_{CC} - V_{OH}$ (V)

1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0

$T_A = +25°C$
$V_{CC} = 2.5$ V
$V_{CC} = 3.0$ V
$V_{CC} = 4.0$ V
$V_{CC} = 5.0$ V
$V_{CC} = 6.0$ V

0.0  −0.5  −1.0  −1.5  −2.0  −2.5  −3.0

$I_{OH}$ (mA)
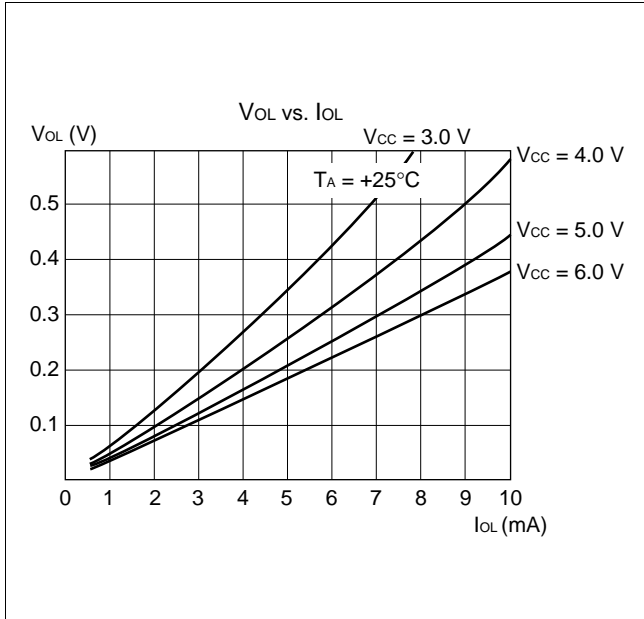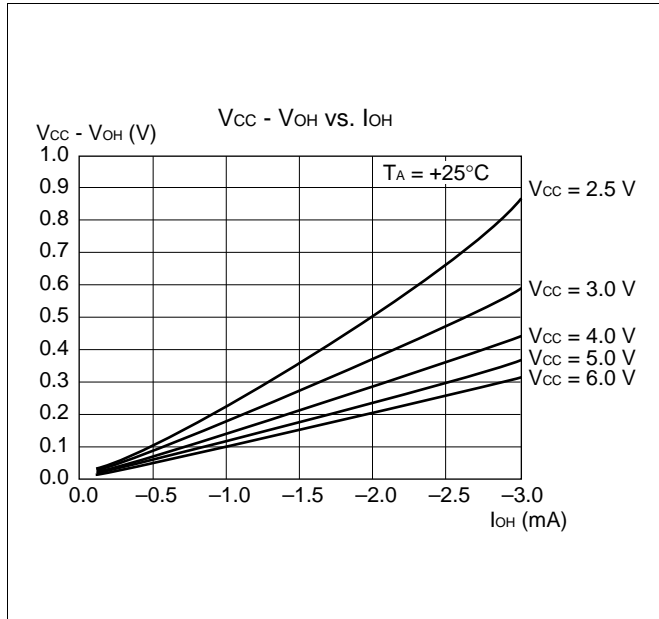
**(3) "H" Level Input Voltage/"L" Level Input Voltage (CMOS Input)**

VIN vs. VCC

$V_{IN}$ (V)

5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0

$T_A = +25°C$

0  1  2  3  4  5  6  7

$V_{CC}$ (V)
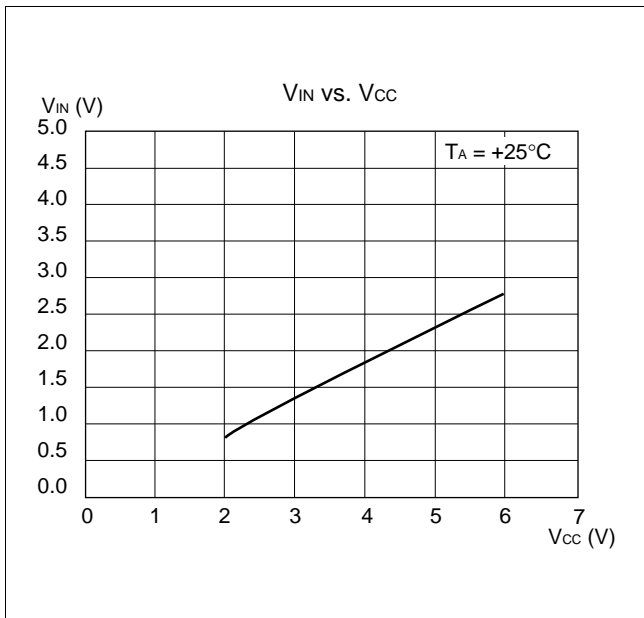
**(4) "H" Level Input Voltage/"L" Level Input Voltage (Hysteresis Input)**

VIN vs. VCC

$V_{IN}$ (V)

5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0

$T_A = +25°C$
$V_{IHS}$
$V_{ILS}$

0  1  2  3  4  5  6  7

$V_{CC}$ (V)

$V_{IHS}$: Threshold as the input voltage in hysteresis characteristics is set to "H" level

$V_{ILS}$: Threshold as the input voltage in hysteresis characteristics is set to "L" level
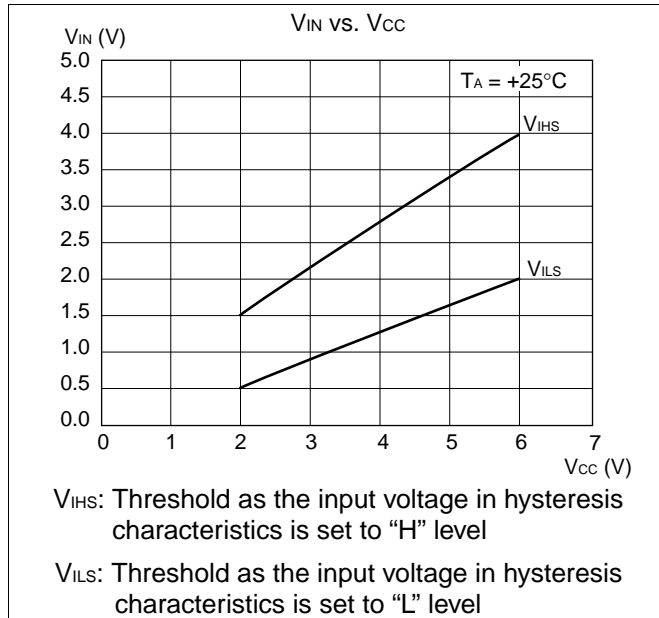
## (5) Power Supply Current (External Clock)

### $I_{CC1}$ vs. $V_{CC}$, $I_{CC2}$ vs. $V_{CC}$

$I_{CC}$ (mA)

$F_{CH} = 10MHz$
$T_A = +25°C$

Divide by 4 ($I_{CC1}$)

Divide by 8

Divide by 16

Divide by 64 ($I_{CC2}$)

$V_{CC}$ (V)
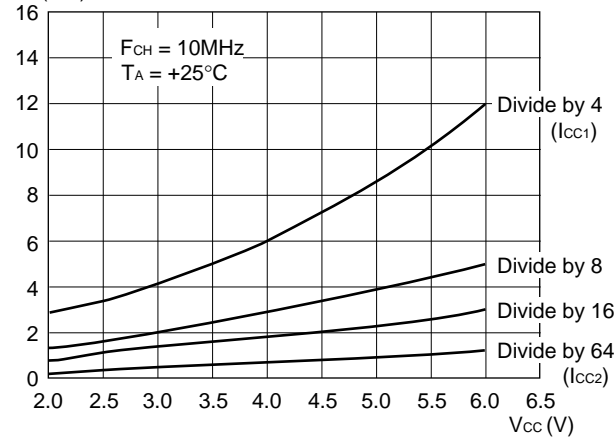
### $I_{CCS1}$ vs. $V_{CC}$, $I_{CCS2}$ vs. $V_{CC}$

$I_{CCS}$ (mA)

$F_{CH} = 10MHz$
$T_A = +25°C$

Divide by 4 ($I_{CCS1}$)

Divide by 8

Divide by 16

Divide by 64 ($I_{CCS2}$)

$V_{CC}$ (V)

### $I_{CCL}$ vs. $V_{CC}$

$I_{CCL}$ (µA)

$T_A = +25°C$

$V_{CC}$ (V)

### $I_{CCLS}$ vs. $V_{CC}$

$I_{CCLS}$ (µA)

$T_A = +25°C$

$V_{CC}$ (V)

*(Continued)*

*(Continued)*



I CCT vs. V CC

I CCH vs. V CC
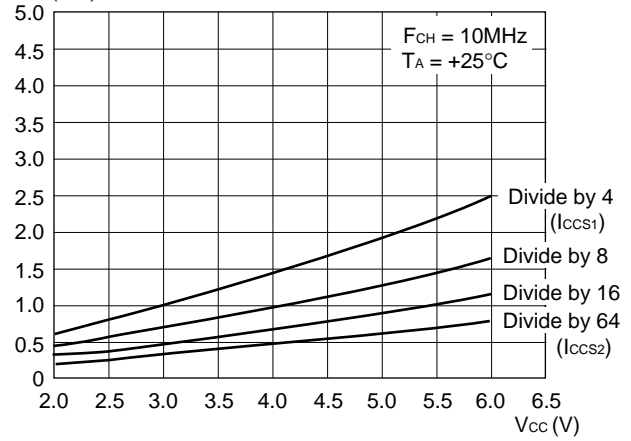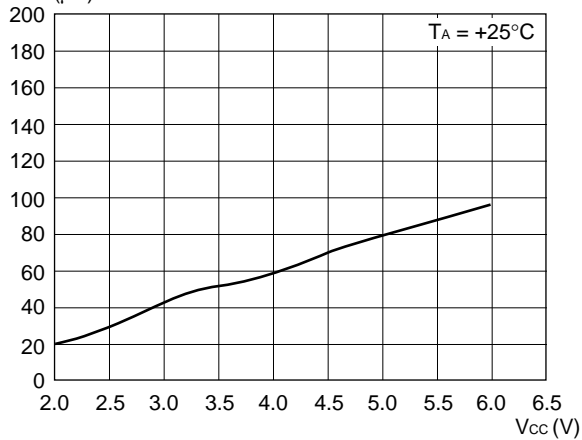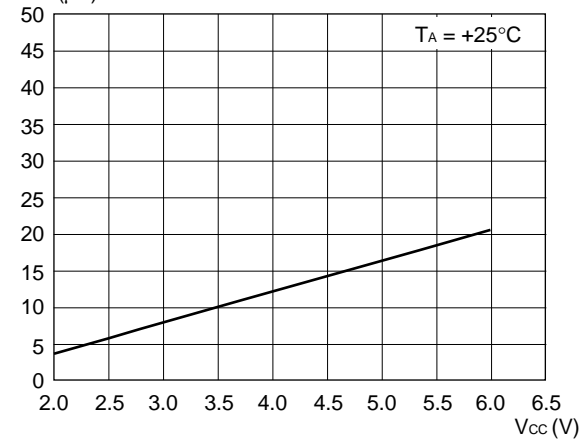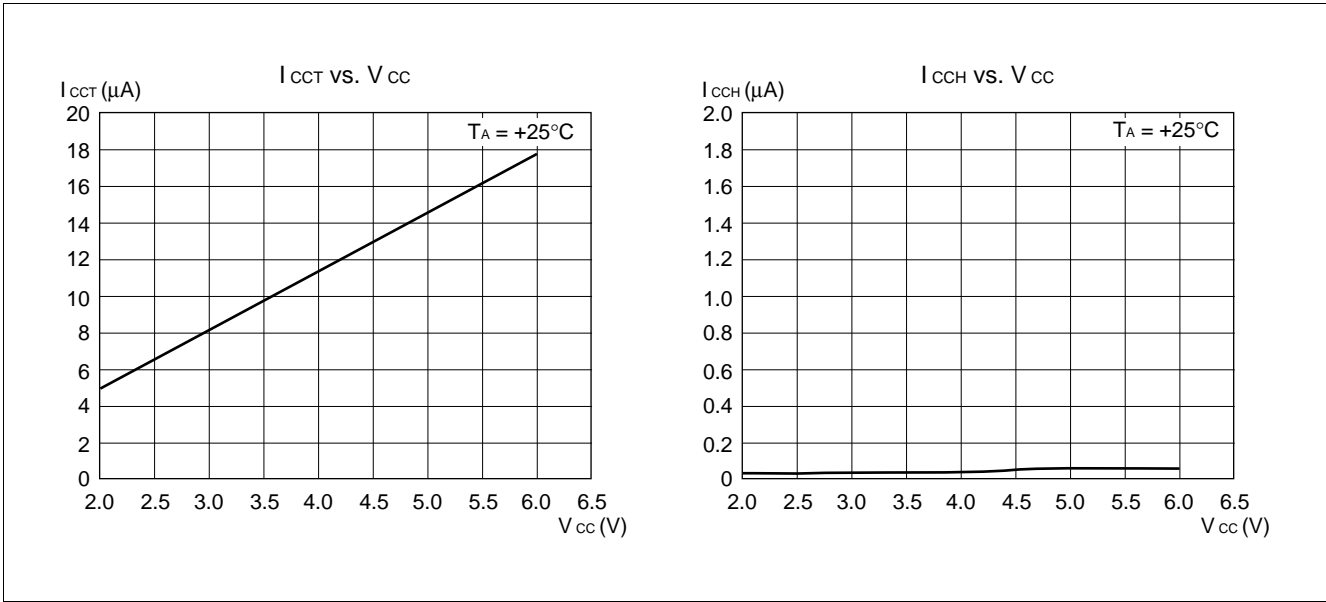
**(6) Pull-up Resistance**



R PULL vs. V CC
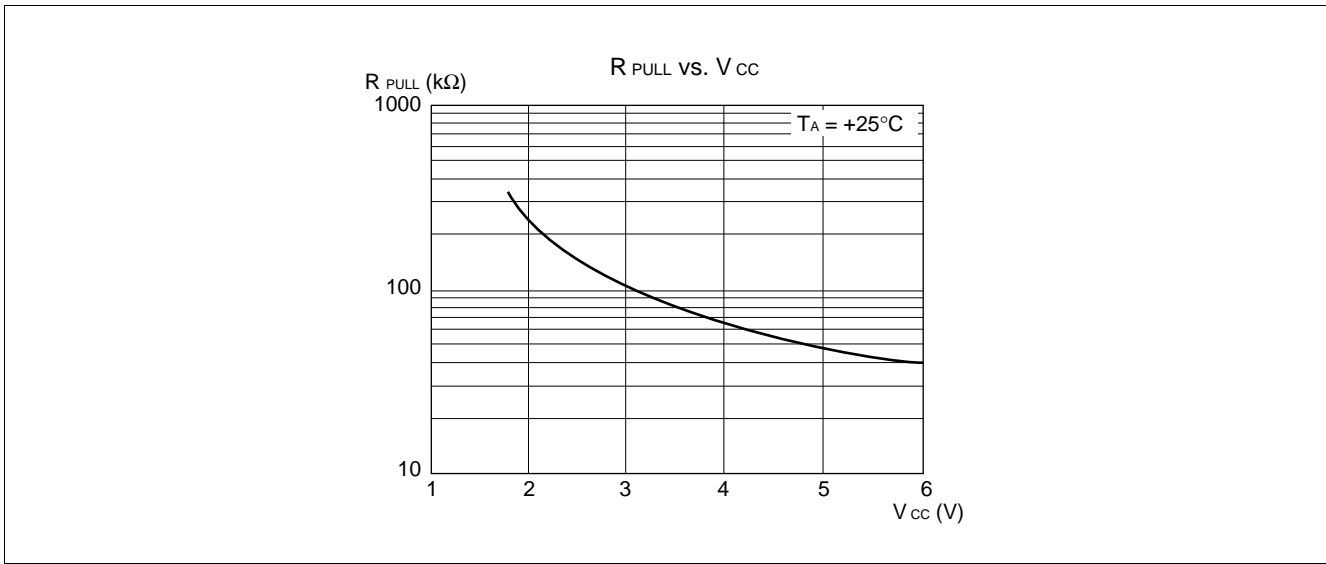
■ MASK OPTIONS

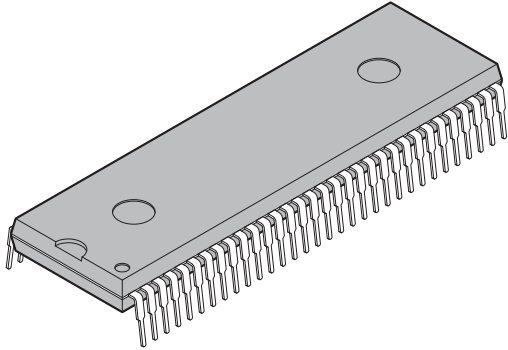| No. | Part number | MB89635R MB89636R MB89637R | MB89P637 | MB89PV630 |
|---|---|---|---|---|
| | Specifying procedure | Specify when ordering masking | Set with EPROM programmer | Setting not possible |
| 1 | Pull-up resistors<br> P00 to P07, P10 to P17,<br> P30 to P37, P40 to P43,<br> P50 to P53, P72 to P74 | Selectable by pin | Can be set per pin* | Fixed to "without pull-up resistor" |
| 2 | Power-on reset selection<br> With power-on reset<br> Without power-on reset | Selectable | Setting possible | Fixed to "with power-on reset" |
| 3 | Selection of the main clock oscillation stabilization time (at 10 MHz)<br> $2^{18}/F_{CH}$ (Approx. 26.2 ms)<br> $2^{17}/F_{CH}$ (Approx. 13.1 ms)<br> $2^{14}/F_{CH}$ (Approx. 1.6 ms)<br> $2^{4}/F_{CH}$ (Approx. 1.6 μs)<br>$F_{CH}$ : Main clock frequency | Selectable | Setting possible | Fixed to $2^{18}/F_{CH}$ (Approx. 26.2 ms) |
| 4 | Reset pin output<br> Reset output provided<br> No reset output | Selectable | Setting possible | Fixed to "with reset output" |
| 5 | Single/dual-clock system option<br> Single clock<br> Dual clock | Selectable | Setting possible | MB89PV630-101  Single-clock system<br>MB89PV630-102  Dual-clock systems |

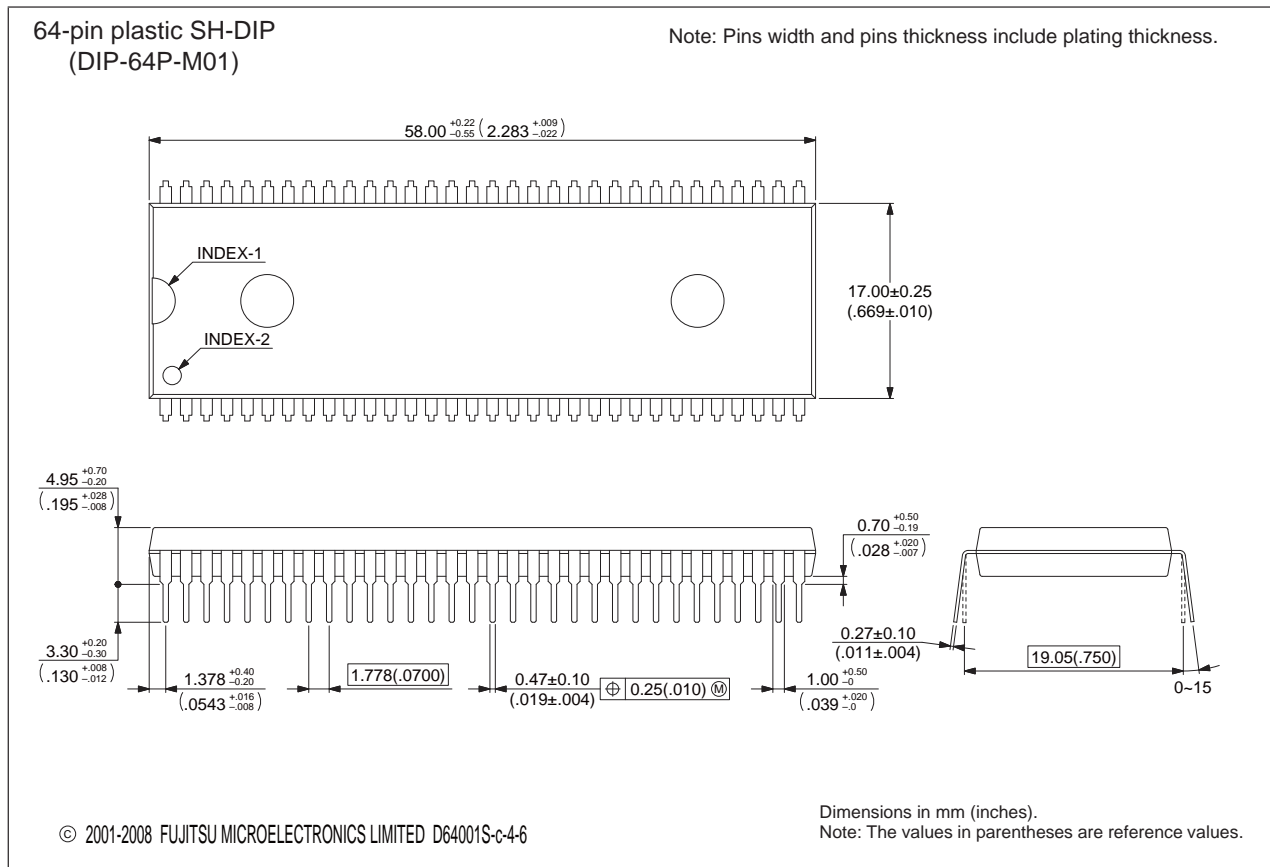\* : For P50 to P53, fixed to "Without pull-up resistor."

## ■ ORDERING INFORMATION

| Part number | Package | Remarks |
|---|---|---|
| MB89635RP-SH<br>MB89636RP-SH<br>MB89637RP-SH<br>MB89P637P-SH | 64-pin Plastic SH-DIP<br>(DIP-64P-M01) | |
| MB89635RPF<br>MB89636RPF<br>MB89637RPF<br>MB89P637PF | 64-pin Plastic QFP<br>(FPT-64P-M06) | |
| MB89635RPMC<br>MB89636RPMC<br>MB89637RPMC | 64-pin Plastic QFP<br>(FPT-64P-M23) | |
| MB89PV630-101CF<br>MB89PV630-102CF | 64-pin Ceramic MQFP<br>(MQP-64C-P01) | |
| MB89PV630-101C<br>MB89PV630-102C | 64-pin Ceramic MDIP<br>(MDP-64C-P02) | |

FUJITSU

## ■ PACKAGE DIMENSIONS
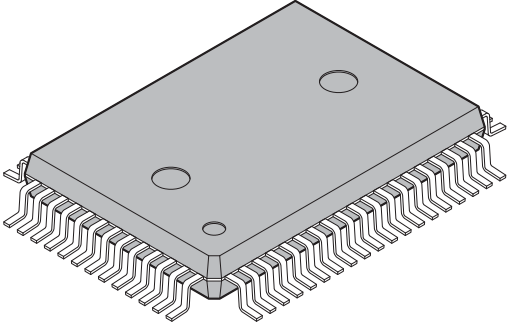
| | |
|---|---|
| 64-pin plastic SH-DIP | Lead pitch |
| | Package width × package length |
| | Sealing method |
| | Mounting height |
| (DIP-64P-M01) | |

| | |
|---|---|
| Lead pitch | 1.778mm(70mil) |
| Package width × package length | 17 × 58 mm |
| Sealing method | Plastic mold |
| Mounting height | 5.65 mm MAX |
| | |
| | |
| | |

64-pin plastic SH-DIP
(DIP-64P-M01)

Note: Pins width and pins thickness include plating thickness.

$58.00 \, ^{+0.22}_{-0.55} \left( 2.283 \, ^{+.009}_{-.022} \right)$

INDEX-1

INDEX-2

$17.00 \pm 0.25$
$(.669 \pm .010)$

$4.95 \, ^{+0.70}_{-0.20}$
$\left( .195 \, ^{+.028}_{-.008} \right)$

$0.70 \, ^{+0.50}_{-0.19}$
$\left( .028 \, ^{+.020}_{-.007} \right)$

$3.30 \, ^{+0.20}_{-0.30}$
$\left( .130 \, ^{+.008}_{-.012} \right)$

$1.378 \, ^{+0.40}_{-0.20}$
$\left( .0543 \, ^{+.016}_{-.008} \right)$

1.778(.0700)

$0.47 \pm 0.10$
$(.019 \pm .004)$

$\oplus$ 0.25(.010) Ⓜ

$1.00 \, ^{+0.50}_{-0}$
$\left( .039 \, ^{+.020}_{-.0} \right)$

$0.27 \pm 0.10$
$(.011 \pm .004)$

19.05(.750)

0~15

© 2001-2008 FUJITSU MICROELECTRONICS LIMITED D64001S-c-4-6

Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

*(Continued)*
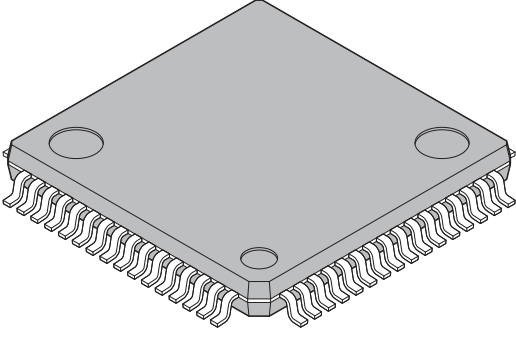
| | |
|---|---|
| Lead pitch | 1.00 mm |
| Package width × package length | 14 × 20 mm |
| Lead shape | Gullwing |
| Sealing method | Plastic mold |
| Mounting height | 3.35 mm MAX |
| Code (Reference) | P-QFP64-14×20-1.00 |

64-pin plastic QFP

(FPT-64P-M06)

64-pin plastic QFP
(FPT-64P-M06)

Note 1) ＊ : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.

24.70±0.40(.972±.016)

＊20.00±0.20(.787±.008)

0.17±0.06
(.007±.002)

18.70±0.40
(.736±.016)

＊14.00±0.20
(.551±.008)

INDEX

1.00(.039)

0.42±0.08
(.017±.003)

0.20(.008) Ⓜ

Details of "A" part

$3.00 ^{+0.35}_{-0.20}$ (Mounting height)
$(.118 ^{+.014}_{-.008})$

0~8°

$0.25 ^{+0.15}_{-0.20}$
$(.010 ^{+.006}_{-.008})$
(Stand off)

1.20±0.20
(.047±.008)

"A"

0.10(.004)

© 2003-2008 FUJITSU MICROELECTRONICS LIMITED F64013S-c-5-6

Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

*(Continued)*

DS07-12531-4E

| 64-pin plastic LQFP | Lead pitch | 0.65 mm |
|---|---|---|
| | Package width × package length | 12.0 × 12.0 mm |
| | Lead shape | Gullwing |
| | Sealing method | Plastic mold |
| | Mounting height | 1.70 mm MAX |
| | Code (Reference) | P-LFQFP64-12×12-0.65 |
| (FPT-64P-M23) | | |

64-pin plastic LQFP
(FPT-64P-M23)

Note 1) ∗ : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.

14.00±0.20(.551±.008)SQ

∗12.00±0.10(.472±.004)SQ

48    33

49    32

INDEX

64    17

1    16

0.65(.026)

0.32±0.05
(.013±.002)

⊕ 0.13(.005) Ⓜ

0.145±0.055
(.0057±.0022)

△ 0.10(.004)

"A"

Details of "A" part

1.50 $^{+0.20}_{-0.10}$ (Mounting height)
(.059 $^{+.008}_{-.004}$ )

0.25(.010)

0~8°

0.50±0.20
(.020±.008)

0.60±0.15
(.024±.006)

0.10±0.10
(.004±.004)
(Stand off)

©2003-2008 FUJITSU MICROELECTRONICS LIMITED  F64034S-c-1-2

Dimensions in mm (inches).
Note: The values in parentheses are reference values

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

*(Continued)*

| 64-pin ceramic MQFP | Lead pitch | 1.00 mm |
|---|---|---|
| | Lead shape | Straight |
| | Motherboard material | Ceramic |
| | Mounted package material | Plastic |
| | | |
| | | |
| (MQP-64C-P01) | | |

64-pin ceramic MQFP
(MQP-64C-P01)



INDEX AREA

18.70(.736)TYP
16.30±0.33 (.642±.013)
15.58±0.20 (.613±.008)
1.27±0.13 (.050±.005)
22.30±0.33 (.878±.013)
24.70(.972) TYP
0.30(.012) TYP
12.02(.473) TYP
10.16(.400) TYP
18.12±0.20 (.713±.008)
14.22(.560) TYP
1.27±0.13 (.050±.005)
0.30(.012)TYP
7.62(.300)TYP
9.48(.373)TYP
11.68(.460)TYP

12.00(.472)TYP
1.00±0.25 (.039±.010)
$1.20 ^{+0.40}_{-0.20}$ $\left(.047 ^{+.016}_{-.008}\right)$
1.00±0.25 (.039±.010)
18.00(.709) TYP
0.40±0.10 (.016±.004)
0.40±0.10 (.016±.004)
$1.20 ^{+0.40}_{-0.20}$ $\left(.047 ^{+.016}_{-.008}\right)$

10.82(.426) MAX
0.15±0.05 (.006±.002)
0.50(.020)TYP

© 1994-2008 FUJITSU MICROELECTRONICS LIMITED M64004SC-1-4

Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

*(Continued)*

*(Continued)*

| 64-pin ceramic MDIP | Lead pitch | 1.778mm (70mil) |
|---|---|---|
|  | Row spacing | 19.05mm (750mil) |
|  | Motherboard material | Ceramic |
|  | Mounted packing material | Plastic |
|  |  |  |
|  |  |  |
| (MDP-64C-P02) |  |  |
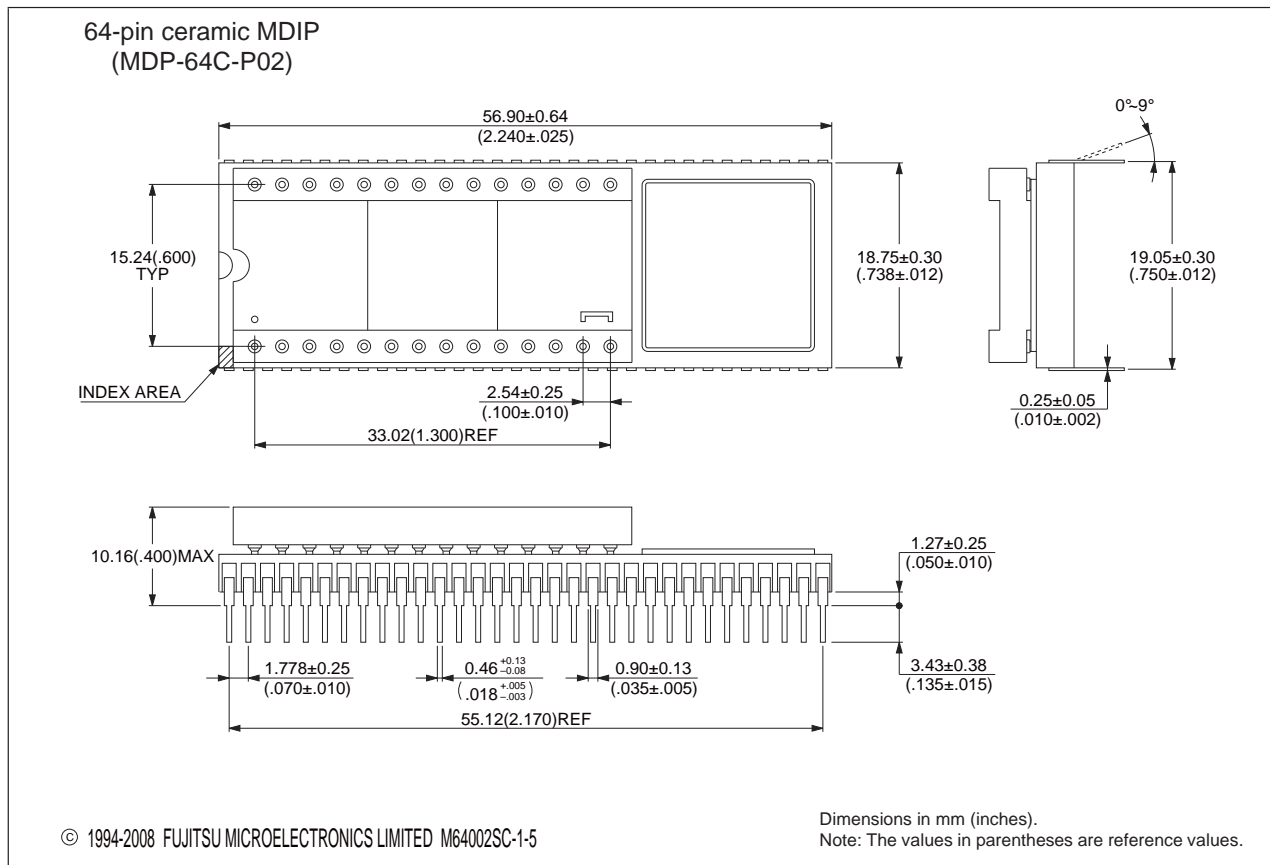
64-pin ceramic MDIP
(MDP-64C-P02)

56.90±0.64
(2.240±.025)

0°~9°

15.24(.600)
TYP

18.75±0.30
(.738±.012)

19.05±0.30
(.750±.012)

INDEX AREA

2.54±0.25
(.100±.010)

33.02(1.300)REF

0.25±0.05
(.010±.002)

10.16(.400)MAX

1.27±0.25
(.050±.010)

1.778±0.25
(.070±.010)

$0.46^{+0.13}_{-0.08}$
$(.018^{+.005}_{-.003})$

0.90±0.13
(.035±.005)

3.43±0.38
(.135±.015)

55.12(2.170)REF

© 1994-2008 FUJITSU MICROELECTRONICS LIMITED M64002SC-1-5

Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

## ■ MAIN CHANGES IN THIS EDITION

| Page | Section | Change Results |
|------|---------|----------------|
| 49 | ■ MASK OPTIONS | Changed the explanation for "*" in "■ MASK OPTIONS". |

The vertical lines marked in the left side of the page show the changes.

**MEMO**

**MEMO**

**MEMO**

# FUJITSU MICROELECTRONICS LIMITED

Shinjuku Dai-Ichi Seimei Bldg., 7-1, Nishishinjuku 2-chome,
Shinjuku-ku, Tokyo 163-0722, Japan
Tel: +81-3-5322-3329
*http://jp.fujitsu.com/fml/en/*

*For further information please contact:*

**North and South America**
FUJITSU MICROELECTRONICS AMERICA, INC.
1250 E. Arques Avenue, M/S 333
Sunnyvale, CA 94085-5401, U.S.A.
Tel: +1-408-737-5600   Fax: +1-408-737-5999
*http://www.fma.fujitsu.com/*

**Europe**
FUJITSU MICROELECTRONICS EUROPE GmbH
Pittlerstrasse 47, 63225 Langen, Germany
Tel: +49-6103-690-0 Fax: +49-6103-690-122
*http://emea.fujitsu.com/microelectronics/*

**Korea**
FUJITSU MICROELECTRONICS KOREA LTD.
206 Kosmo Tower Building, 1002 Daechi-Dong,
Gangnam-Gu, Seoul 135-280, Republic of Korea
Tel: +82-2-3484-7100 Fax: +82-2-3484-7111
*http://kr.fujitsu.com/fmk/*

**Asia Pacific**
FUJITSU MICROELECTRONICS ASIA PTE. LTD.
151 Lorong Chuan,
#05-08 New Tech Park 556741 Singapore
Tel : +65-6281-0770 Fax : +65-6281-0220
*http://www.fmal.fujitsu.com/*

FUJITSU MICROELECTRONICS SHANGHAI CO., LTD.
Rm. 3102, Bund Center, No.222 Yan An Road (E),
Shanghai 200002, China
Tel : +86-21-6146-3688 Fax : +86-21-6335-1605
*http://cn.fujitsu.com/fmc/*

FUJITSU MICROELECTRONICS PACIFIC ASIA LTD.
10/F., World Commerce Centre, 11 Canton Road,
Tsimshatsui, Kowloon, Hong Kong
Tel : +852-2377-0226 Fax : +852-2376-3269
*http://cn.fujitsu.com/fmc/en/*

Edited: Sales Promotion Department