

8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89920 Series

MB89923/925/P928/PV920

■ DESCRIPTION

The MB89920 series is a line of single-chip microcontrollers using the F²MC*-8L CPU core which can operate at low voltage but at high speed.

The microcontrollers in this series contain peripheral functions such as a PWM timer, an input capture/output compare control counter, an LCD controller/driver, an A/D converter, and a UART.

The MB89920 series can suit a wide range of applications such as analog input conversion, pulse input measurement/pulse output control, serial communications control, and display control.

*: F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

■ FEATURES

- High speed processing at low voltage
Minimum execution time: 0.5 μ s/8.0 MHz
- F²MC-8L family CPU core

Instruction set optimized for controllers { Multiplication and division instructions
16-bit arithmetic operations
Test and branch instructions
Bit manipulation instructions, etc.

- 8-bit PWM timer: 2 channels (also usable as a reload timer)
- 16-bit input capture: 2 channels / 16-bit output compare: 2 channels

(Continued)

For the information for microcontroller supports, see the following web site.

<http://edevic.fujitsu.com/micom/en-support/>

MB89920 Series

(Continued)

- 20-bit time-base counter
- UART: 1 channel (with asynchronous transfer mode and 8-bit synchronous serial mode)
- 8-bit serial interface: 1 channel (LSB first/MSB first selectability)
- 10-bit A/D converter: 8 channels
- LCD controller/driver: 28 segments × 4 commons (max. 112 pixels)
- Low-voltage detection reset
- Watchdog timer reset
- External interrupt: 4 channels
Four channels are independent and capable of wake-up from the low-power consumption mode (with edge detection function)
- Buzzer output/clock output
- Low-power consumption modes:
Stop mode (The software stops oscillation to minimize the current consumption.)
Sleep mode (The CPU stops to reduce current consumption to approx. 1/3 of normal.)
Hardware standby mode (The pin input stops oscillation.)

MB89920 Series

■ PRODUCT LINEUP

| Part number Parameter | MB89923 | MB89925 | MB89P928 | MB89PV920 |
|--------------------------------|---|--------------------------------------|---|---|
| Classification | Mass production products (mask ROM products) | | One-time PROM product (for development) | Piggyback/evaluation product (for development) |
| ROM size | 8 K × 8 bits (internal mask ROM) | 16 K × 8 bits (internal mask ROM) | 48 K × 8 bits (internal PROM) | 48 K × 8 bits (external ROM) |
| RAM size | 256 × 8 bits | 512 × 8 bits | 1024 × 8 bits | |
| CPU functions | Number of instructions: Instruction bit length: Instruction length: Data bit length: Minimum execution time: Interrupt processing time: | | 136 8 bits 1 to 3 bytes 1, 8, 16 bits 0.5 μs/8 MHz 4.5 μs/8 MHz | |
| Ports | I/O ports (CMOS): I/O ports (N-ch open-drain): Total: | | 35 (25 ports also serve as peripherals.) 34 (All also serve as peripherals.) 69 | |
| Options | Specify with mask options | | Set with EPROM programmer | None |
| 20-bit time-base timer | 20 bits (interval time selection: 4.10 ms, 16.38 ms, 65.54 ms, 262 ms/8 MHz) | | | |
| Real-time I/O | 16-bit timer: operating clock cycle (0.5 μs, 1.0 μs, 2.0 μs, 4.0 μs), overflow interrupt Input capture: 16 bits × 2 channels, external trigger edge selectability Output compare: 16 bits × 2 channels | | | |
| LCD controller/ driver | Common output: 4 (selectable from 2 to 4 by software) Segment output: 28 (can be switched to ports in 4-pin unit by software) Bias power supply pins: 3 LCD display RAM size: 14 × 8 bits Dividing resistor for LCD driving: built-in (external resistor selectability) | | | |
| 8-bit PWM timer | 8 bits × 2-channel reload timer operation 8 bits × 2-channel PWM operation (4 cycles selectable) 8 bits × 1-channel PPG operation (4 oscillation clocks selectable) | | | |
| UART | Variable data length (7 or 8 bits), internal baud rate generator, error detection function, full-duplex with internal double buffer, NRZ transmission formation, Clock synchronous/asynchronous transfer capable | | | |
| 8-bit serial I/O | 8 bits, LSB first/MSB first selectability, One clock selectable from four transfer clocks (one external shift clock, three internal shift clocks: 1.0 μs, 4.0 μs, 16.0 μs) | | | |
| 10-bit A/D converter | 10-bit resolution × 8 channels A/D conversion mode (conversion time: 16.5 μs (33 instruction cycles)) Sense mode (conversion time: 9.0 μs (18 instruction cycles)) Continuous activation by an internal clock capable | | | |
| Watchdog timer | Interval time: approx. 130 to 260 ms | | | |
| Low-voltage detection reset | Reset activation voltage: 3.0 to 4.3 V Reset release voltage: 3.1 to 4.5 V | | | |
| Hardware standby | Stop the clock oscillation by pin input | | | |
| Buzzer/clock output | 1 channel (output a frequency from 1 KHz, 2 KHz, 4 KHz, and divided clock frequency) | | | |
| External interrupt | 4 channels (rising edge/falling edge selectability) | | | |
| Package | QFP-80 | | | MQFP-80 |
| Operating voltage | 2.2 to 6.0 V* | | 2.7 to 6.0 V* | |
| EPROM for use | — | | | MBM27C512-20TV (LCC package) |

* : The minimum operating voltage varies with conditions such as the operating frequencies, functions, and development tool.

MB89920 Series

■ PACKAGE AND CORRESPONDING PRODUCTS

| Package | MB89923 MB89925 MB89P928 | MB89PV920 |
|-------------|--------------------------------|-----------|
| FPT-80P-M06 | ○ | × |
| MQP-80C-P01 | × | ○ |

○ : Available × : Not available

Note: For more information about each package, see section “■ Package Dimensions”.

■ DIFFERENCES AMONG PRODUCTS

1. Memory Size

Before evaluating using the piggyback product, verify its differences from the product that will actually be used. Take particular care on the following points:

- The stack area, etc., is set at the upper limit of the RAM.
- The external area is used.

2. Current Consumption

- In the case of the MB89PV920, add the current consumed by the EPROM which is connected to the top socket.
- When operated at low speed, the product with an OTPROM (one-time PROM) or an EPROM will consume more current than the product with a mask ROM.

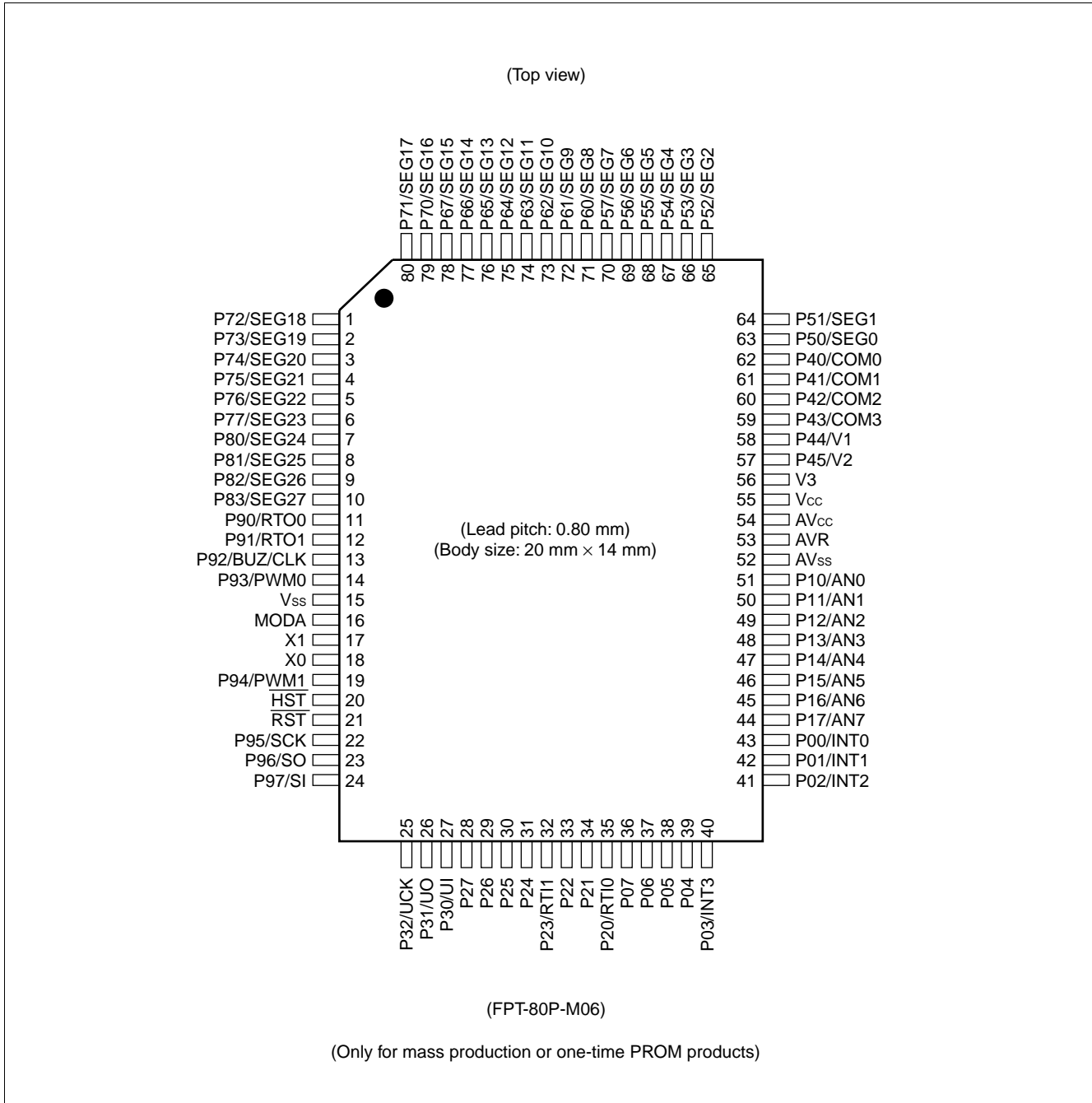
However, the current consumption in sleep/stop modes is the same. (For more information, see section “■ Electrical Characteristics”.)

3. Mask Options

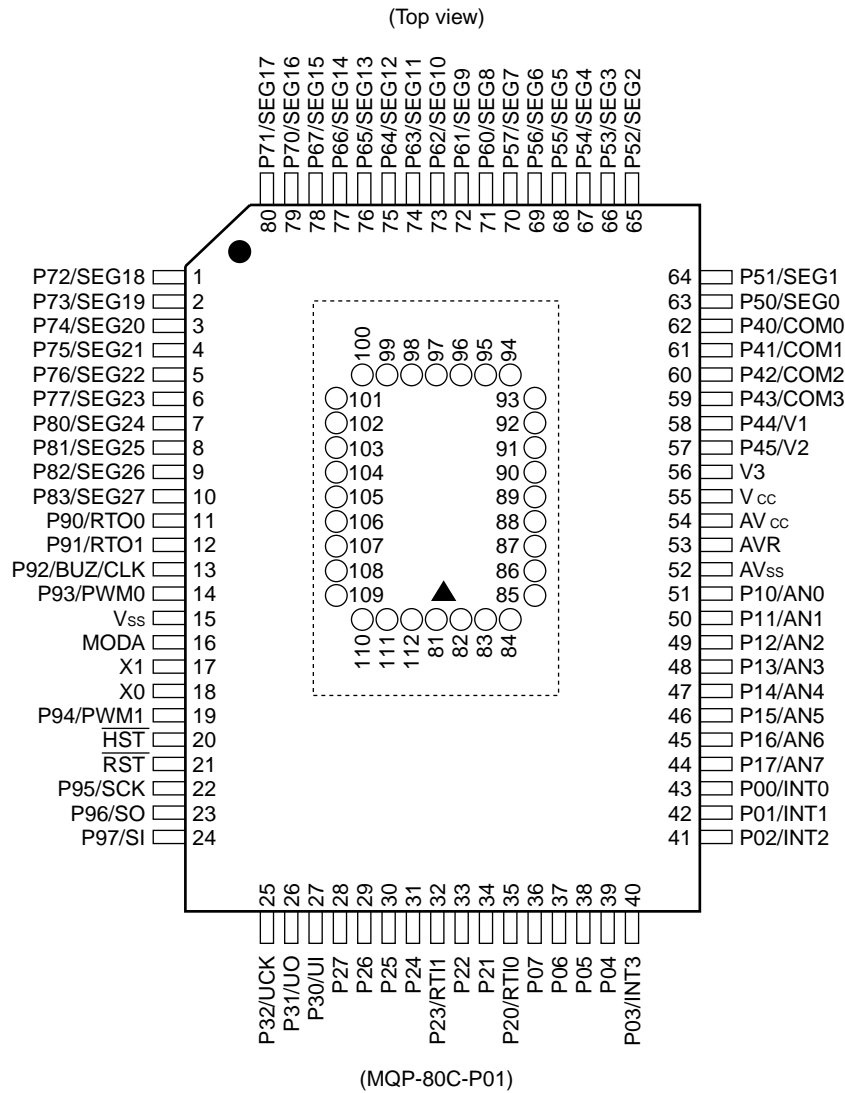
Functions that can be selected as options and how to designate these options vary by the product.

Before using options check section “■ Mask Options”.

■ PIN ASSIGNMENT



MB89920 Series



• Pin assignment on package top (only for piggyback/evaluation product)

| Pin no. | Pin name | Pin no. | Pin name | Pin no. | Pin name | Pin no. | Pin name |
|---------|----------|---------|-----------------|---------|-----------------|---------|------------------------|
| 81 | N.C. | 89 | A2 | 97 | N.C. | 105 | \overline{OE}/V_{PP} |
| 82 | A15 | 90 | A1 | 98 | O4 | 106 | N.C. |
| 83 | A12 | 91 | A0 | 99 | O5 | 107 | A11 |
| 84 | A7 | 92 | N.C. | 100 | O6 | 108 | A9 |
| 85 | A6 | 93 | O1 | 101 | O7 | 109 | A8 |
| 86 | A5 | 94 | O2 | 102 | O8 | 110 | A13 |
| 87 | A4 | 95 | O3 | 103 | \overline{CE} | 111 | A14 |
| 88 | A3 | 96 | V _{SS} | 104 | A10 | 112 | V _{CC} |

N.C.: Internally connected. Do not use.

(Only for piggyback/evaluation product)

■ PIN DESCRIPTION

| Pin no. | Pin name | Circuit type | Function |
|-----------|-------------------------|--------------|--|
| 17 | X1 | A | Clock oscillator pins |
| 18 | X0 | | |
| 16 | MODA | B | Operation mode selection input pin Connect this pin to V _{SS} (GND). |
| 20 | $\overline{\text{HST}}$ | B | Hardware standby input pin |
| 21 | $\overline{\text{RST}}$ | C | Reset I/O pin This pin is an N-ch open-drain output type with a pull-up resistor, and a hysteresis input type. “L” is output from this pin by an internal reset source. The internal circuit is initialized by the input of “L”. |
| 11, 12 | P90/RTO0, P91/RTO1 | D | General-purpose I/O ports A pull-up resistor option is provided. Also serve as an output compare data output. |
| 13 | P92/BUZ/CLK | D | General-purpose I/O port Also serves as a buzzer/clock output. |
| 14 | P93/PWM0 | D | General-purpose I/O port A pull-up resistor option is provided. Also serves as an 8-bit PWM output. |
| 19 | P94/PWM1 | D | General-purpose I/O port A pull-up resistor option is provided. Also serves as an 8-bit PWM output. |
| 22 | P95/SCK | E | General-purpose I/O port A pull-up resistor option is provided. Also serves as the clock I/O (SCK) for the serial I/O. The SCK input is a hysteresis input. The output type can be switched between N-ch open-drain and CMOS. |
| 23 | P96/SO | D | General-purpose I/O port A pull-up resistor option is provided. Also serves as the data output (SO) for the serial I/O. The output type can be switched between N-ch open-drain and CMOS. |
| 24 | P97/SI | E | General-purpose I/O port A pull-up resistor option is provided. Also serves as the data input (SI) for the serial I/O. |
| 25 | P32/UCK | E | General-purpose I/O port A pull-up resistor option is provided. Also serves as a UART clock I/O (UCK). The UCK input is hysteresis input. The output type can be switched between N-ch open-drain and CMOS. |
| 26 | P31/UO | D | General-purpose I/O port A pull-up resistor option is provided. Also serves as a UART data output (UO). The output type can be switched between N-ch open-drain and CMOS. |

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MB89920 Series

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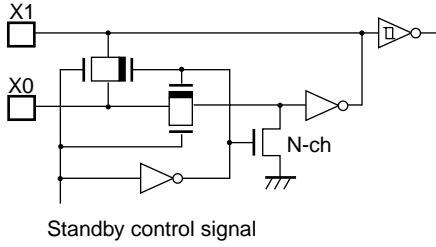
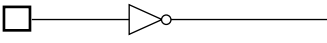
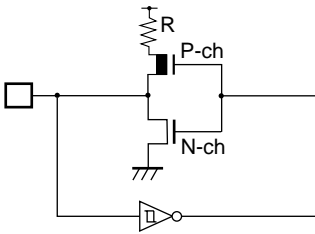
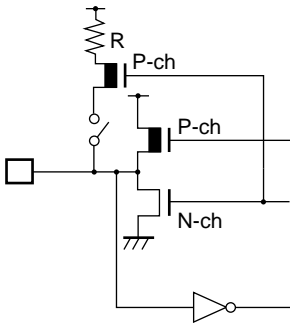
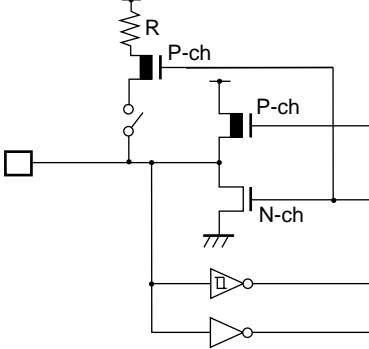
| Pin no. | Pin name | Circuit type | Function |
|-----------|---------------------------|--------------|---|
| 27 | P30/UI | E | General-purpose I/O port A pull-up resistor option is provided. Also serves as a UART data input (UI). |
| 28 to 31 | P27 to P24 | D | General-purpose I/O ports A pull-up resistor option is provided. |
| 32 | P23/RT11 | E | General-purpose I/O port A pull-up resistor option is provided. Also serves as an input capture data input. |
| 33, 34 | P22, P21 | D | General-purpose I/O ports A pull-up resistor option is provided. |
| 35 | P20/RT10 | E | General-purpose I/O port A pull-up resistor option is provided. Also serves as an input capture data input. |
| 36 to 39 | P07 to P04 | D | General-purpose I/O ports A pull-up resistor options is provided. |
| 40 to 43 | P03/INT3 to P00/INT0 | E | General-purpose I/O ports A pull-up resistor options is provided. Also serve as an external interrupt input (INT0 to INT3). |
| 44 to 51 | P17/AN7 to P10/AN0 | G | CMOS I/O ports Also serve as an A/D converter analog input. |
| 57, 58 | P45/V2, P44/V1 | F | LCD driving power supply pins These pins can be used as an N-ch open-drain general-purpose I/O when not used as an LCD driving power supply. |
| 59 to 62 | P43/COM3 to P40/COM0 | F | LCD common output pins These pins can be used as an N-ch open-drain general-purpose I/O when not used as an LCD common output. |
| 63 to 70 | P50/SEG0 to P57/SEG7 | F | LCD segment output pins These pins can be used as an N-ch open-drain general-purpose I/O when not used as an LCD segment output. |
| 71 to 78 | P60/SEG8 to P67/SEG15 | F | LCD segment output pins These pins can be used as an N-ch open-drain general-purpose I/O when not used as an LCD segment output. |
| 79, 80 | P70/SEG16, P71/SEG17 | F | LCD segment output pins These pins can be used as an N-ch open-drain general-purpose I/O when not used as an LCD segment output. |
| 1 to 6 | P72/SEG18 to P77/SEG23 | F | LCD segment output pins These pins can be used as an N-ch open-drain general-purpose I/O when not used as an LCD segment output. |
| 7 to 10 | P80/SEG24 to P83/SEG27 | F | LCD segment output pins These pins can be used as an N-ch open-drain general-purpose I/O when not used as an LCD segment output. |
| 52 | AV _{ss} | — | A/D converter power supply (GND) pin |
| 53 | AVR | — | A/D converter reference power supply pin |
| 54 | AV _{cc} | — | A/D converter power supply pin |
| 55 | V _{cc} | — | Power supply pin |
| 56 | V3 | — | LCD driving power supply pin |
| 15 | V _{ss} | — | Power supply (GND) pin |

• External EPROM pins (the MB89PV920 only)

| Pin no. | Pin name | I/O | Function |
|--|--|-----|--|
| 82 83 84 85 86 87 88 89 90 91 | A15 A12 A7 A6 A5 A4 A3 A2 A1 A0 | O | Address output pins |
| 93 94 95 | O1 O2 O3 | I | Data input pins |
| 96 | V _{SS} | O | Power supply (GND) pin |
| 98 99 100 101 102 | O4 O5 O6 O7 O8 | I | Data input pins |
| 103 | \overline{CE} | O | ROM chip enable pin Outputs "H" during standby. |
| 104 | A10 | O | Address output pin |
| 105 | \overline{OE}/V_{PP} | O | ROM output enable pin Outputs "L" at all times. |
| 107 108 109 | A11 A9 A8 | O | Address output pins |
| 110 | A13 | O | Address output pin |
| 111 | A14 | O | Address output pin |
| 112 | V _{CC} | O | EPROM power supply pin |
| 81 92 97 106 | N.C. | — | Internally connected pins Be sure to leave them open. |

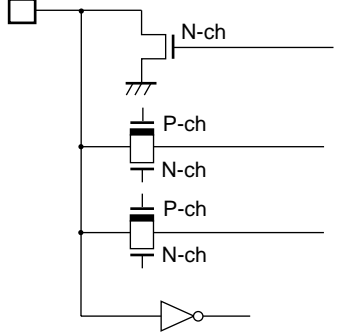
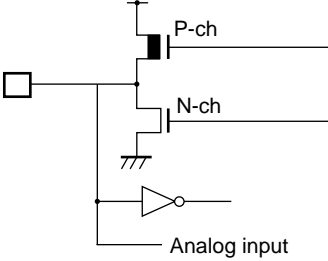
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■ I/O CIRCUIT TYPE

| Type | Circuit | Remarks |
|------|---|---|
| A |  <p>Standby control signal</p> | <ul style="list-style-type: none"> • At an oscillation feedback resistor of approximately 1 MΩ (1 to 8 MHz) |
| B |  | <ul style="list-style-type: none"> • CMOS input |
| C |  | <ul style="list-style-type: none"> • At an output pull-up resistor of approximately 50 KΩ (5.0 V) • Hysteresis input |
| D |  | <ul style="list-style-type: none"> • CMOS output • CMOS input • Pull-up resistor optional |
| E |  | <ul style="list-style-type: none"> • CMOS output • CMOS input • Hysteresis input (peripheral input) • Pull-up resistor optional |

(Continued)

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| Type | Circuit | Remarks |
|------|--|--|
| F |  | <ul style="list-style-type: none"> • N-ch open-drain I/O • Also serves as LCD controller/driver common/segment output. |
| G |  | <ul style="list-style-type: none"> • CMOS I/O • Analog input |

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- to high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in section “■ Electrical Characteristics” is applied between V_{CC} and V_{SS} .

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog power supply (AV_{CC} and AVR) and analog input from exceeding the digital power supply (V_{CC}) when the analog system power supply is turned on and off.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

3. Treatment of Power Supply Pins on Microcontrollers with A/D Converter

Connect to be $AV_{CC} = V_{CC}$ and $AV_{SS} = AVR = V_{SS}$ even if the A/D converter is not in use.

4. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

5. Power Supply Voltage Fluctuations

Although V_{CC} power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

6. Precautions when Using an External Clock

Even when an external clock is used, oscillation stabilization time is required for power-on reset (optional) and wake-up from stop mode.

■ PROGRAMMING TO THE EPROM ON THE MB89P928

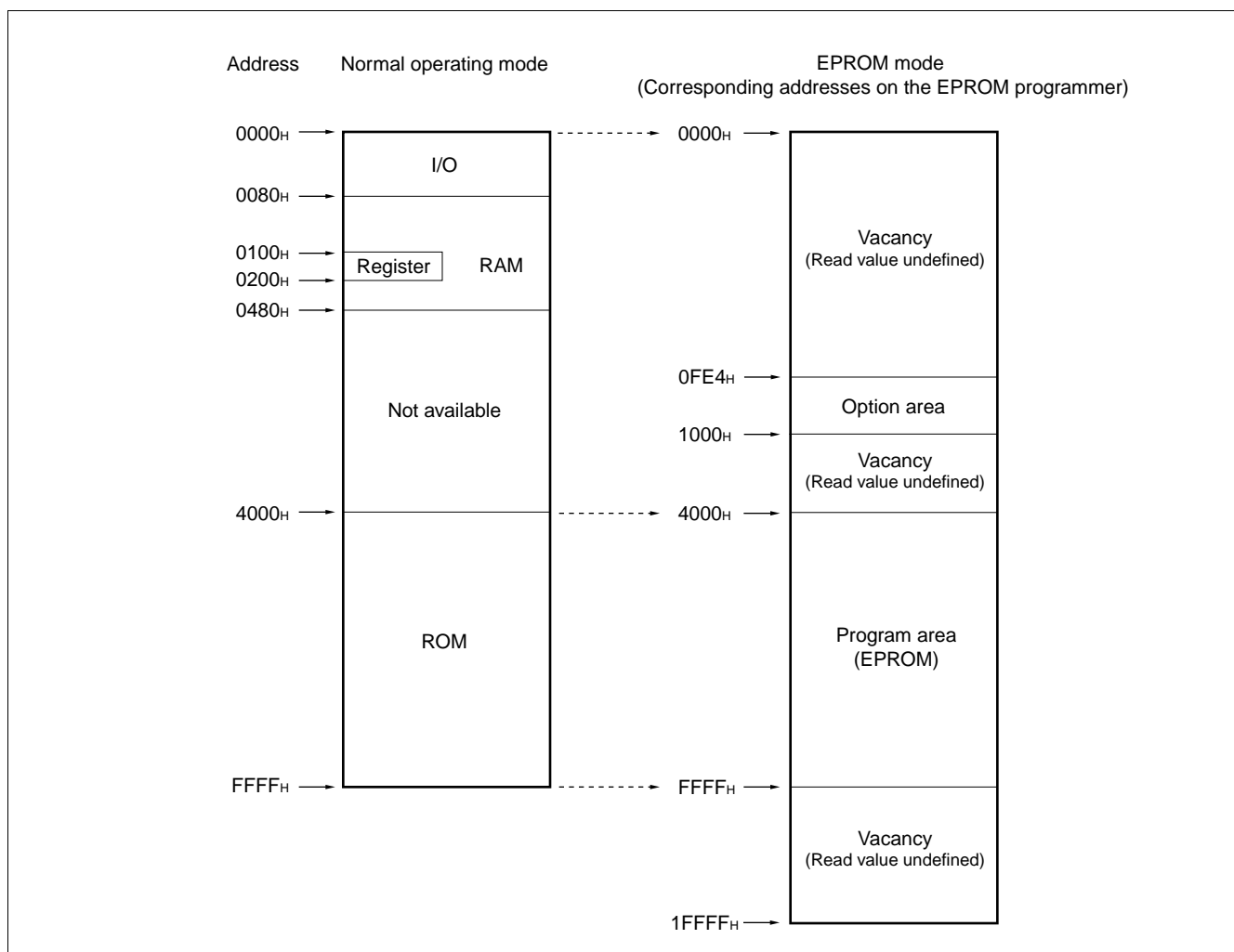
The MB89P928 is an OTPROM version of the MB89920 series.

1. Features

- 48-Kbyte PROM on chip
- Options can be set using the EPROM programmer.
- Equivalency to the MBM27C1001A in EPROM mode (when programmed with the EPROM programmer)

2. Memory Space

Memory space in the EPROM mode is diagrammed below.



MB89920 Series

3. Programming to the PROM

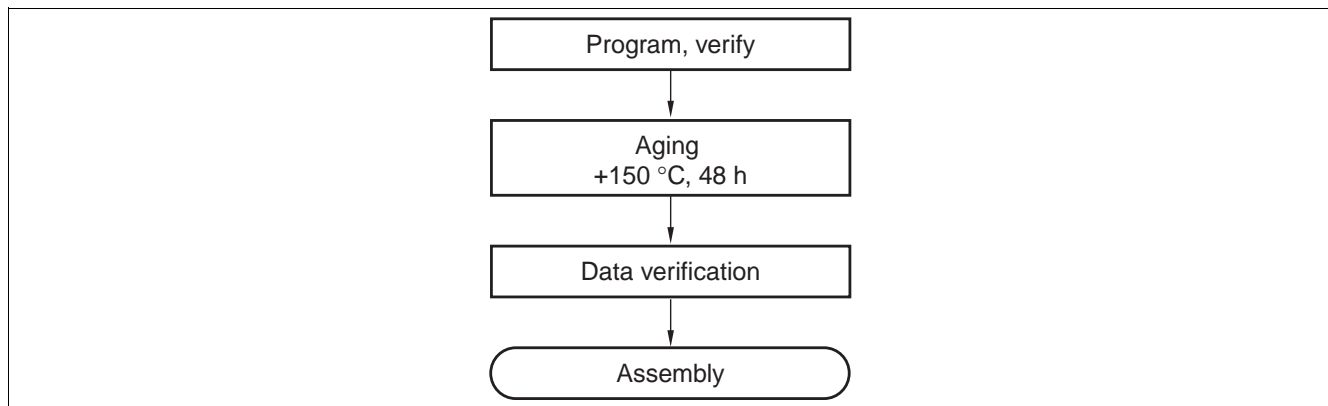
In EPROM mode, the MB89P928 functions equivalent to the MBM27C1001A. This allows the PROM to be programmed with a general-purpose EPROM programmer (the electronic signature mode cannot be used) by using the dedicated socket adapter.

• Programming procedure

- (1) Set the EPROM programmer to the MBM27C1001A.
- (2) Load program data into the EPROM programmer at 0FE4_H to FFFF_H.
- (3) Program with the EPROM programmer.

4. Recommended Screening Conditions

High-temperature aging is recommended as the pre-assembly screening procedure for a product with a blanked OTPROM microcomputer program.



5. Programming Yield

All bits cannot be programmed at Fujitsu shipping test to a blanked OTPROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

6. PROM Option Bit Map

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------------|--------------------------------|--------------------------------|---|---|-------------------------------------|--------------------------------------|--|---|
| 0FE4 _H | Vacancy Readable | Vacancy Readable | Vacancy Readable | Oscillation stabilization time 1: Crystal 0: Ceramic | Reset pin output 1: Yes 0: No | Power-on reset 1: Yes 0: No | Vacancy Readable | Vacancy Readable |
| 0FE8 _H | P07 Pull-up 1: No 0: Yes | P06 Pull-up 1: No 0: Yes | P05 Pull-up 1: No 0: Yes | P04 Pull-up 1: No 0: Yes | P03 Pull-up 1: No 0: Yes | P02 Pull-up 1: No 0: Yes | P01 Pull-up 1: No 0: Yes | P00 Pull-up 1: No 0: Yes |
| 0FEC _H | P27 Pull-up 1: No 0: Yes | P26 Pull-up 1: No 0: Yes | P25 Pull-up 1: No 0: Yes | P24 Pull-up 1: No 0: Yes | P23 Pull-up 1: No 0: Yes | P22 Pull-up 1: No 0: Yes | P21 Pull-up 1: No 0: Yes | P20 Pull-up 1: No 0: Yes |
| 0FF0 _H | Vacancy Readable | Vacancy Readable | Vacancy Readable | Vacancy Readable | Vacancy Readable | P32 Pull-up 1: No 0: Yes | P31 Pull-up 1: No 0: Yes | P30 Pull-up 1: No 0: Yes |
| 0FF4 _H | P97 Pull-up 1: No 0: Yes | P96 Pull-up 1: No 0: Yes | P95 Pull-up 1: No 0: Yes | P94 Pull-up 1: No 0: Yes | P93 Pull-up 1: No 0: Yes | P92 Pull-up 1: No 0: Yes | P91 Pull-up 1: No 0: Yes | P90 Pull-up 1: No 0: Yes |
| 0FF8 _H | Vacancy Readable | Vacancy Readable | WDT/low-voltage control 1: Register 0: Option EPROM | Low-voltage detection voltage 00: — 01: 3.3 V 10: 3.6 V 11: 4.0 V | | Low-voltage reset 1: Yes 0: No | Low-voltage detection 1: Automatic 0: Prohibited | Watchdog timer (WDT) 1: Automatic 0: Prohibited |
| 0FFC _H | Vacancy Readable | Vacancy Readable | Vacancy Readable | Vacancy Readable | Vacancy Readable | Vacancy Readable | Vacancy Readable | Vacancy Readable |

- The initial value of each bit is “1”.

Notes: • Do not write 0 to the vacant bit.

The read value of the vacant bit is 1, unless 0 is written to it.

- Write the same value as each option register to the 3-byte vacant address that follows above option registers.

Example: In the case of 0FE4_H, write the same value to 0FE5_H, 0FE6_H and 0FF7_H.

- This optional information is taken into the OTPROM while the oscillation is being reset. Therefore, if the hardware state is initially shifted to standby state after the power supply is turned on, the optional information will not be valid during the transition (in a state of the initial value 1).

After the hardware standby state is cleared, the oscillation starts and the optional information becomes valid.

Note that if the hardware is shifted to the standby or stop state in the course of a normal operation (oscillation), the contents of the optional register are valid since the option data has already been taken into the OTPROM.

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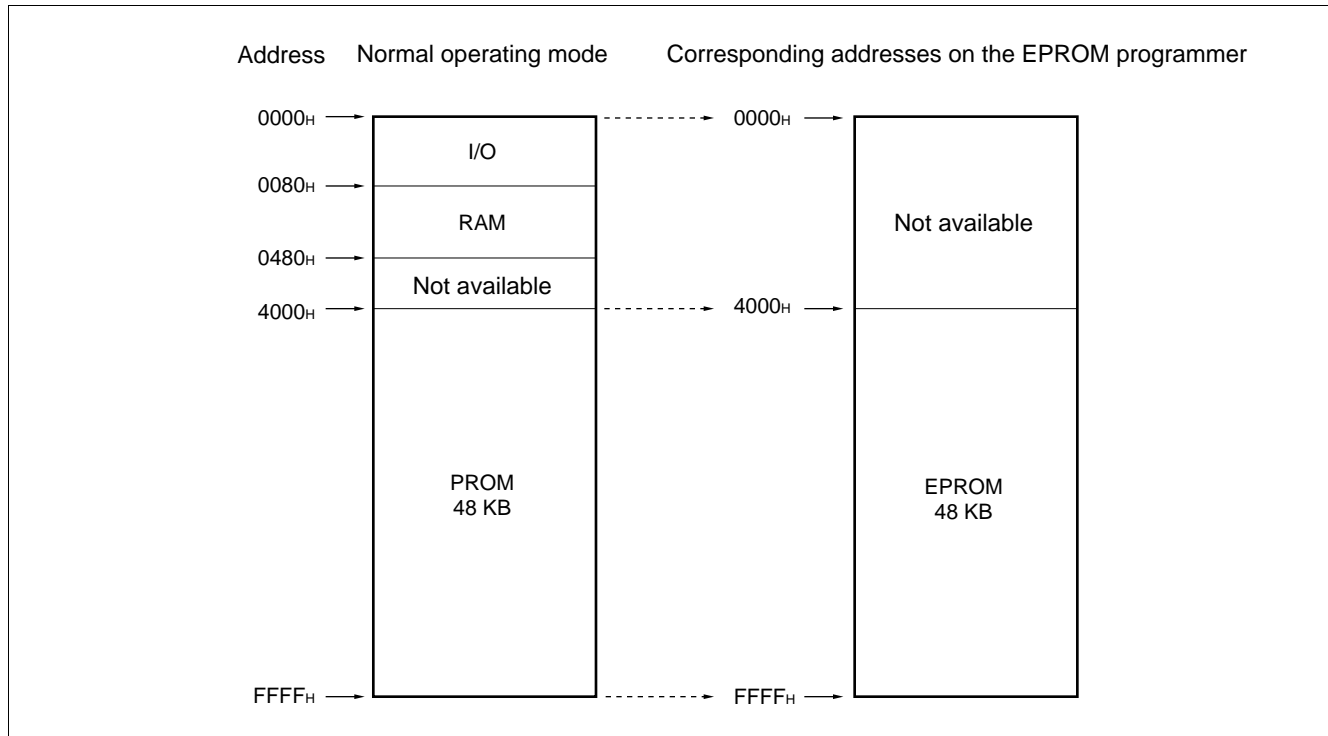
■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

1. EPROM for Use

MBM27C512-20TV

2. Memory Space

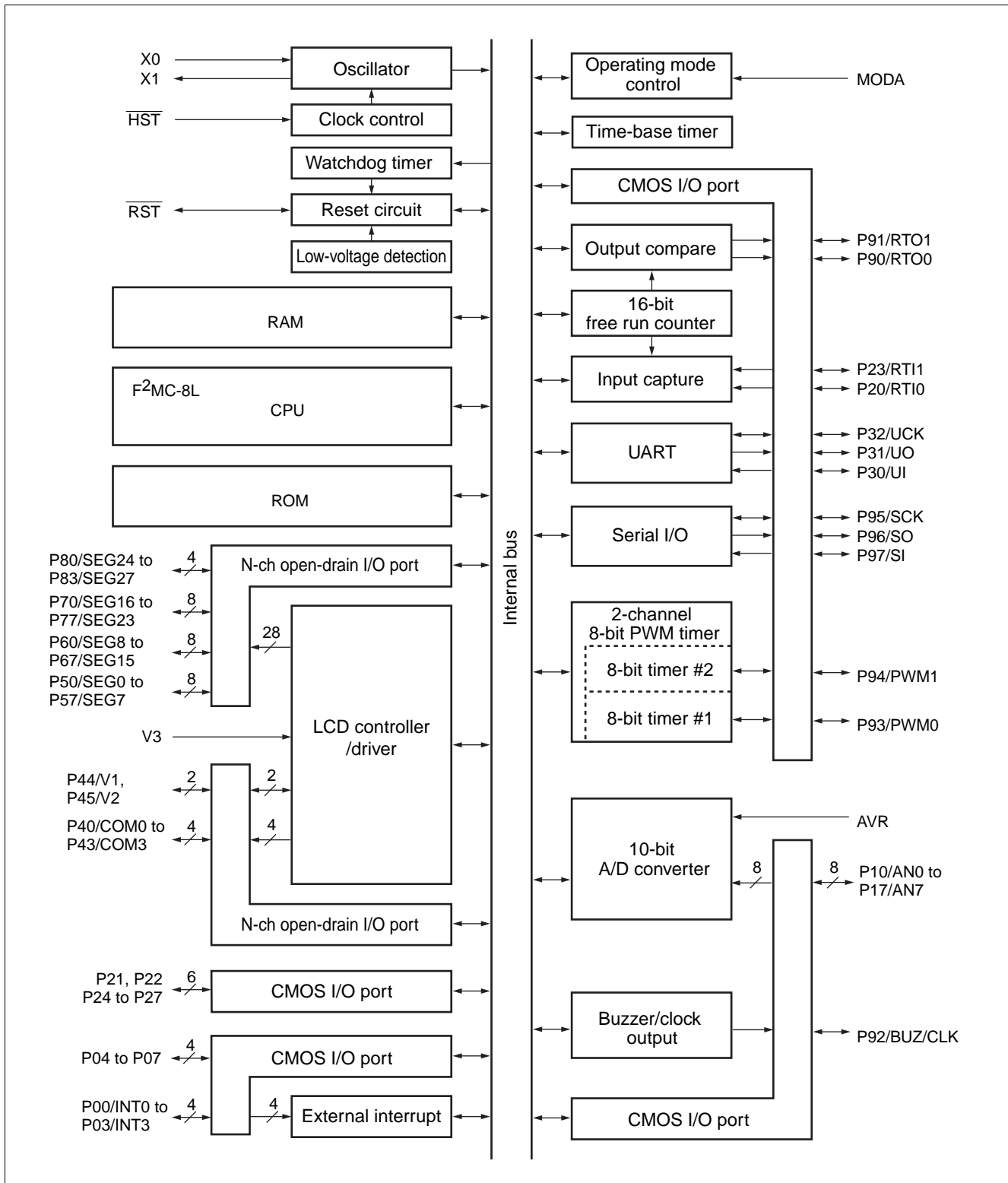
Memory space in each mode is diagrammed below.



3. Programming to the EPROM

- (1) Set the EPROM programmer to the MBM27C512.
- (2) Load program data into the EPROM programmer at 4000_H to FFFF_H.
- (3) Program to 4000_H to FFFF_H with the EPROM programmer.

■ BLOCK DIAGRAM

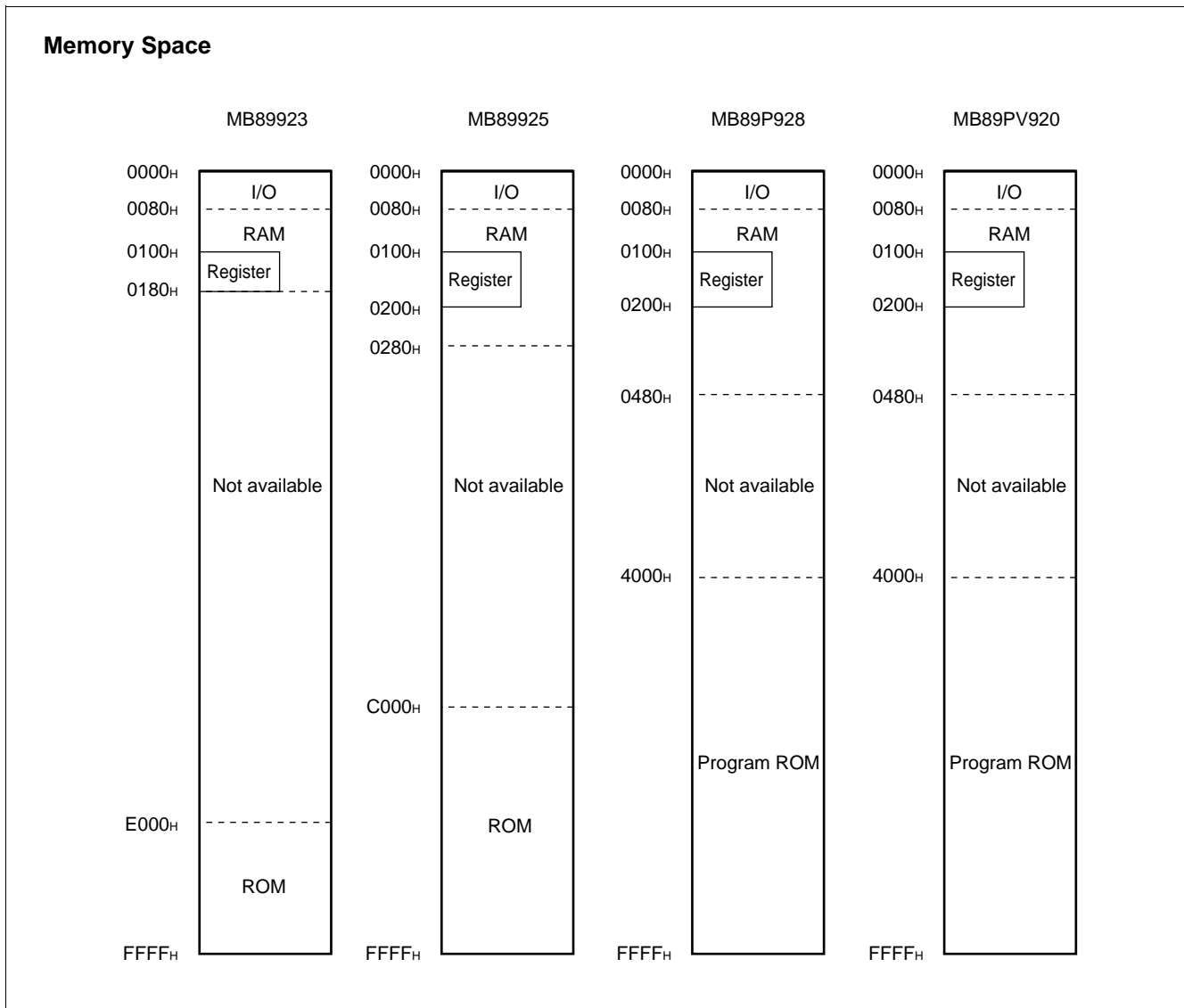


MB89920 Series

■ CPU CORE

1. Memory Space

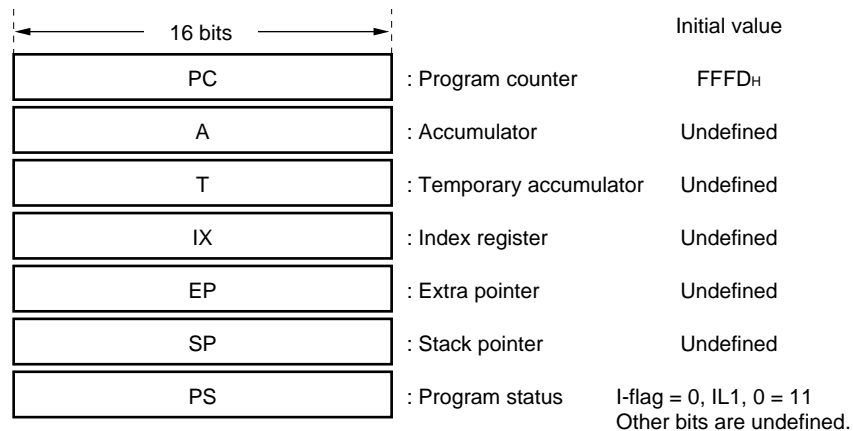
The microcontrollers of the MB89920 series offer a memory space of 64 Kbytes for storing all of I/O, data, and program areas. The I/O area is located at the lowest address. The data area is provided immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is located at exactly the opposite end, that is, near the highest address. Provide the tables of interrupt reset vectors and vector call instructions toward the highest address within the program area. The memory space of the MB89920 series is structured as illustrated below.



2. Registers

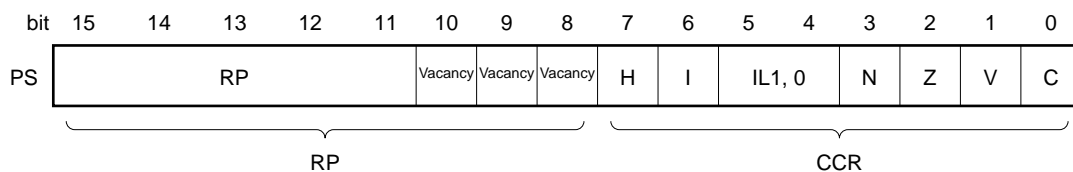
The F²MC-8L family has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following dedicated registers are provided:

| | |
|----------------------------|--|
| Program counter (PC): | A 16-bit register for indicating instruction storage positions |
| Accumulator (A): | A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used. |
| Temporary accumulator (T): | A 16-bit register which performs arithmetic operations with the accumulator When the instruction is an 8-bit data processing instruction, the lower byte is used. |
| Index register (IX): | A 16-bit register for index modification |
| Extra pointer (EP): | A 16-bit pointer for indicating a memory address |
| Stack pointer (SP): | A 16-bit register for indicating a stack area |
| Program status (PS): | A 16-bit register for storing a register pointer, a condition code |



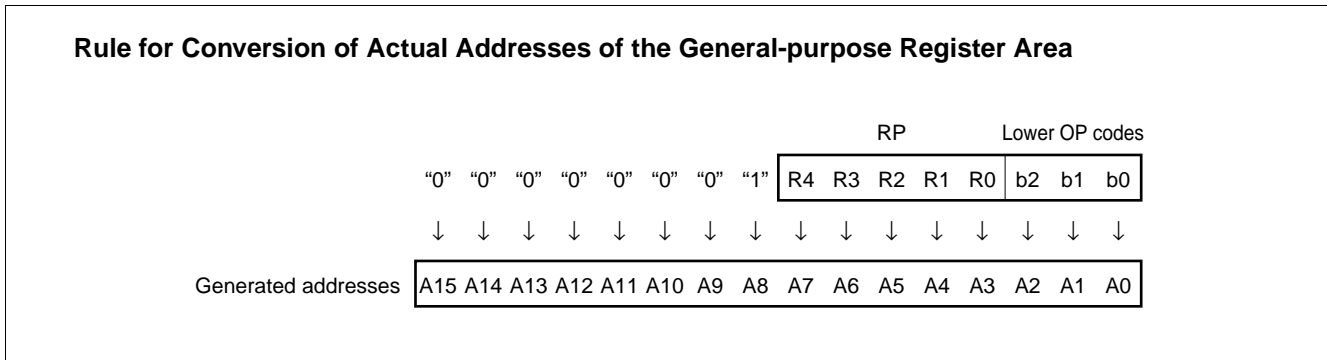
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)

Structure of the Program Status Register



MB89920 Series

The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.



The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

- H-flag: Set when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared otherwise. This flag is for decimal adjustment instructions.
- I-flag: Interrupt is allowed when this flag is set to 1. Interrupt is prohibited when the flag is set to 0. Set to 0 when reset.
- IL1, 0: Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

| IL1 | ILO | Interrupt level | High-low |
|-----|-----|-----------------|--------------------------------------|
| 0 | 0 | 1 | High ↑ ↓ Low = no interrupt |
| 0 | 1 | | |
| 1 | 0 | 2 | |
| 1 | 1 | 3 | |

- N-flag: Set if the MSB is set to 1 as the result of an arithmetic operation. Cleared when the bit is set to 0.
- Z-flag: Set when an arithmetic operation results in 0. Cleared otherwise.
- V-flag: Set if the complement on 2 overflows as a result of an arithmetic operation. Reset if the overflow does not occur.
- C-flag: Set when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared otherwise. Set to the shift-out value in the case of a shift instruction.

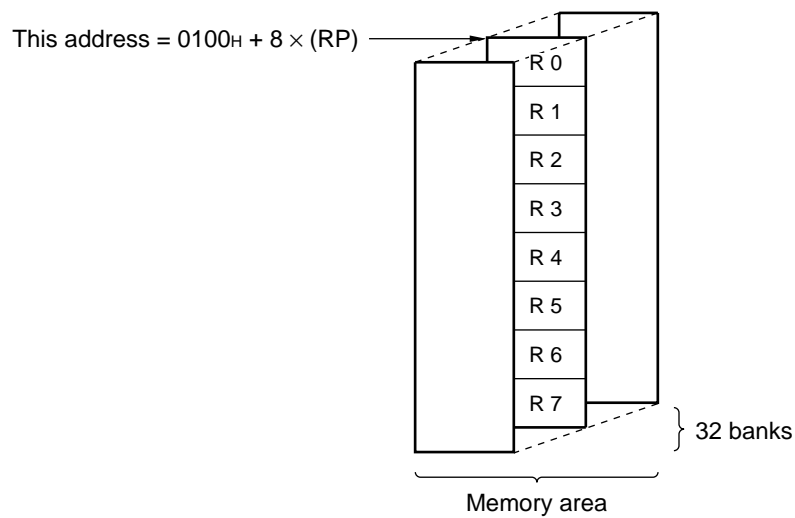
The following general-purpose registers are provided:

General-purpose registers: An 8-bit register for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers and up to a total of 16 banks can be used on the MB89925. Up to a total of 16 banks can be used on the MB89923. The bank currently in use is indicated by the register bank pointer (RP).

Note: The number of register banks that can be used varies with the RAM size.

Register Bank Configuration



MB89920 Series

■ I/O MAP

| Address | Read/write | Register | Register description | Initial value |
|---------|------------|----------|--|------------------------------|
| 00H | (R/W) | PDR0 | Port 0 data register | X X X X X X X X _B |
| 01H | (W) | DDR0 | Port 0 data direction register | 0 0 0 0 0 0 0 0 _B |
| 02H | (R/W) | PDR1 | Port 1 data register | X X X X X X X X _B |
| 03H | (W) | DDR1 | Port 1 data direction register | 0 0 0 0 0 0 0 0 _B |
| 04H | | | Vacancy | |
| 05H | | | Vacancy | |
| 06H | | | Vacancy | |
| 07H | | | Vacancy | |
| 08H | (R/W) | STBC | Standby control register | 0 0 0 1 X X X X _B |
| 09H | (R/W) | WDTE | Watchdog timer control register | X X X X X X X X _B |
| 0AH | (R/W) | TBCR | Time-base timer control register | X X X 0 0 0 0 0 _B |
| 0BH | (R/W) | LVRC | Low-voltage detection reset control register | 0 X 1 1 X 0 0 X _B |
| 0CH | (R/W) | PDR3 | Port 3 data/peripheral I/O control register | 0 0 0 0 – X X X _B |
| 0DH | (W) | DDR3 | Port 3 data direction register | – – – – – 0 0 0 _B |
| 0EH | (R/W) | PDR4 | Port 4 data register | – – 1 1 1 1 1 1 _B |
| 0FH | (R/W) | PDR5 | Port 5 data register | 1 1 1 1 1 1 1 1 _B |
| 10H | (R/W) | PDR6 | Port 6 data register | 1 1 1 1 1 1 1 1 _B |
| 11H | (R/W) | PDR7 | Port 7 data register | 1 1 1 1 1 1 1 1 _B |
| 12H | (R/W) | PDR8 | Port 8 data register | – – – – 1 1 1 1 _B |
| 13H | (R/W) | PDR9 | Port 9 data register | X X X X X X X X _B |
| 14H | (W) | DDR9 | Port 9 data direction register | 0 0 0 0 0 0 0 0 _B |
| 15H | (R/W) | PDR2 | Port 2 data register | X X X X X X X X _B |
| 16H | (R/W) | DDR2 | Port 2 data direction register | 0 0 0 0 0 0 0 0 _B |
| 17H | (R/W) | BUZR | Buzzer control register | X X X X 0 0 0 0 _B |
| 18H | (R/W) | ADC1 | AD converter control register 1 | 0 0 0 0 0 0 0 0 _B |
| 19H | (R/W) | ADC2 | AD converter control register 2 | X 0 0 0 0 0 0 1 _B |
| 1AH | (R/W) | ADCH | AD converter data register “H” | – – – – – X X _B |
| 1BH | (R/W) | ADCL | AD converter data register “L” | X X X X X X X X _B |
| 1CH | (R/W) | SMR | Serial mode register | 0 0 0 0 0 0 0 0 _B |
| 1DH | (R/W) | SDR | Serial data register | X X X X X X X X _B |
| 1EH | | | Vacancy | |
| 1FH | (W) | ICR1 | Port 1 input control register | 0 0 0 0 0 0 0 0 _B |

–: Unused X: Undefined

(Continued)

Note: Do not use vacancies

MB89920 Series

| Address | Read/write | Register | Register description | Initial value |
|-----------------|------------|----------|--|------------------------------|
| 20 _H | (R/W) | CNTR1 | PWM timer control register 1 | 0 0 0 0 0 0 0 0 _B |
| 21 _H | (R/W) | CNTR2 | PWM timer control register 2 | 0 0 0 0 0 0 0 0 _B |
| 22 _H | (R/W) | CNTR3 | PWM timer control register 3 | 0 0 0 X 0 0 0 0 _B |
| 23 _H | (W) | COMR2 | PWM timer compare register 2 | X X X X X X X X _B |
| 24 _H | (W) | COMR1 | PWM timer compare register 1 | X X X X X X X X _B |
| 25 _H | | | Vacancy | |
| 26 _H | | | Vacancy | |
| 27 _H | | | Vacancy | |
| 28 _H | (R/W) | TMCR | Timer control register | 0 0 X X 0 0 0 0 _B |
| 29 _H | (R) | TCHR | Timer count register (H) | 0 0 0 0 0 0 0 0 _B |
| 2A _H | (R) | TCLR | Timer count register (L) | 0 0 0 0 0 0 0 0 _B |
| 2B _H | (R/W) | OPCR | Output control register | 0 0 0 0 0 0 0 0 _B |
| 2C _H | (R/W) | CPR0H | Output compare register 0 (H) | 0 0 0 0 0 0 0 0 _B |
| 2D _H | (R/W) | CPR0L | Output compare register 0 (L) | 0 0 0 0 0 0 0 0 _B |
| 2E _H | (R/W) | CPR1H | Output compare register 1 (H) | 0 0 0 0 0 0 0 0 _B |
| 2F _H | (R/W) | CPR1L | Output compare register 1 (L) | 0 0 0 0 0 0 0 0 _B |
| 30 _H | (R/W) | ICCR | Input capture control register | X 0 0 0 X 0 0 0 _B |
| 31 _H | (R/W) | ICIC | Input capture interrupt control register | X 0 0 0 0 X 0 0 _B |
| 32 _H | (R) | ICR0H | Input capture register 0 (H) | X X X X X X X X _B |
| 33 _H | (R) | ICR0L | Input capture register 0 (L) | X X X X X X X X _B |
| 34 _H | (R) | ICR1H | Input capture register 1 (H) | X X X X X X X X _B |
| 35 _H | (R) | ICR1L | Input capture register 1 (L) | X X X X X X X X _B |
| 36 _H | | | Vacancy | |
| 37 _H | | | Vacancy | |
| 38 _H | (R/W) | EIC1 | External interrupt control register 1 | 0 0 0 0 0 0 0 0 _B |
| 39 _H | (R/W) | EIC2 | External interrupt control register 2 | 0 0 0 0 0 0 0 0 _B |
| 3A _H | | | Vacancy | |
| 3B _H | | | Vacancy | |
| 3C _H | | | Vacancy | |
| 3D _H | | | Vacancy | |
| 3E _H | | | Vacancy | |
| 3F _H | | | Vacancy | |

–: Unused X: Undefined

(Continued)

Note: Do not use vacancies

MB89920 Series

(Continued)

| Address | Read/write | Register | Register description | Initial value |
|-----------------------|------------|----------|--|------------------------------|
| 40 _H | (R/W) | USMR | UART mode register | 0 0 0 0 0 0 0 0 _B |
| 41 _H | (R/W) | USCR | UART control register | 0 0 0 0 0 0 0 0 _B |
| 42 _H | (R/W) | USTR | UART status register | 0 0 0 0 1 X X X _B |
| 43 _H | (R) (W) | RXDR | UART receiver data register | X X X X X X X X _B |
| | | TXDR | UART transmitter data register | X X X X X X X X _B |
| 44 _H | Vacancy | | | |
| 45 _H | (R/W) | RRDR | Baud rate generator/reload data register | X X X X X X X X _B |
| 46 _H | Vacancy | | | |
| 47 _H | Vacancy | | | |
| 48 to 5F _H | Vacancy | | | |
| 60 to 6D _H | (R/W) | VRAM | Display data RAM | X X X X X X X X _B |
| 70 _H | (R/W) | LCR1 | LCD controller/driver control register 1 | 0 0 0 0 0 0 0 0 _B |
| 71 _H | (R/W) | LCR2 | LCD controller/driver control register 2 | 0 0 0 – – – – – _B |
| 72 _H | (R/W) | LCR3 | LCD controller/driver control register 3 | 0 0 0 0 0 0 0 0 _B |
| 73 to 7B _H | Vacancy | | | |
| 7C _H | (W) | ILR1 | Interrupt level setting register 1 | 1 1 1 1 1 1 1 1 _B |
| 7D _H | (W) | ILR2 | Interrupt level setting register 2 | 1 1 1 1 1 1 1 1 _B |
| 7E _H | (W) | ILR3 | Interrupt level setting register 3 | 1 1 1 1 1 1 1 1 _B |
| 7F _H | Vacancy | | | |

–: Unused X: Undefined

Note: Do not use vacancies

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(V_{SS} = 0.0 V)

| Parameter | Symbol | Value | | Unit | Remarks |
|--|--------------------|-----------------------|-----------------------|------|--|
| | | Min. | Max. | | |
| Power supply voltage | V _{CC} | V _{SS} - 0.3 | V _{SS} + 7.0 | V | *1 |
| | AV _{CC} | V _{SS} - 0.3 | V _{CC} + 0.3 | V | *1 |
| | AVR | V _{SS} - 0.3 | V _{SS} + 7.0 | V | AVR must not exceed AV _{CC} + 0.3 V. |
| LCD power supply voltage | V1 to V3 | V _{SS} - 0.3 | V _{SS} + 7.0 | V | V1 ≤ V2 ≤ V3 *2 |
| Input voltage | V _{I1} | V _{SS} - 0.3 | V _{CC} + 0.3 | V | |
| Output voltage | V _{O1} | V _{SS} - 0.3 | V _{CC} + 0.3 | V | P00 to P07, P10 to P17, P20 to P27, P30 to P32, P90 to P97 |
| | V _{O2} | V _{SS} - 0.3 | V _{SS} + 7.0 | V | P40 to P45, P50 to P57, P60 to P67, P70 to P77, P80 to P83 Must not exceed "V3 + 0.3 V" |
| "L" level maximum output current | I _{OL} | — | 20 | mA | Peak value |
| "L" level average output current | I _{OLAV} | — | 4 | mA | Average value |
| "L" level total maximum output current | ∑I _{OL} | — | 100 | mA | Peak value |
| "L" level total average output current | ∑I _{OLAV} | — | 40 | mA | Average value |
| "H" level maximum output current | I _{OH} | — | -20 | mA | Peak value |
| "H" level average output current | I _{OHAV} | — | -4 | mA | Average value |
| "H" level total maximum output current | ∑I _{OH} | — | -50 | mA | Peak value |
| "H" level total average output current | ∑I _{OHAV} | — | -20 | mA | Average value |
| Power consumption | P _D | — | 300 | mW | |
| Operating temperature | T _A | -40 | +85 | °C | |
| Storage temperature | T _{stg} | -55 | +150 | °C | |

*1: Use AV_{CC} and V_{CC} set at the same voltage.

Take care so that AV_{CC} does not exceed V_{CC}, such as when power is turned on.

*2: V_{CC} must not exceed V3. Unless LCD is used, the same setting must be executed.

Precautions: Permanent device damage may occur if the above "Absolute Maximum Ratings" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MB89920 Series

2. Recommended Operating Conditions

(V_{SS} = 0.0 V)

| Parameter | Symbol | Value | | Unit | Remarks |
|---------------------------------------|-----------------|-------------------|-----------------------|------|------------------------------------|
| | | Min. | Max. | | |
| Power supply voltage | V _{CC} | 2.2* ¹ | 6.0 | V | Normal operation assurance range |
| | | 2.7* ¹ | 6.0 | V | MB89PV920/P928 |
| | | 1.5 | 6.0 | V | Retains the RAM state in stop mode |
| A/D converter reference input voltage | AVR | 3.0 | AV _{CC} | V | |
| LCD power supply voltage | V1 to V3 | V _{SS} | V _{SS} + 6.0 | V | V1 ≤ V2 ≤ V3* ² |
| Operating temperature | T _A | -40 | +85 | °C | |

*1: These values vary with the operating frequency, instruction cycle, and analog assurance range. See Figure 1 and "5. A/D Converter Electrical Characteristics".

*2: V_{CC} must not exceed V3.

Figure 1 Operating Voltage vs. Clock Operating Frequency

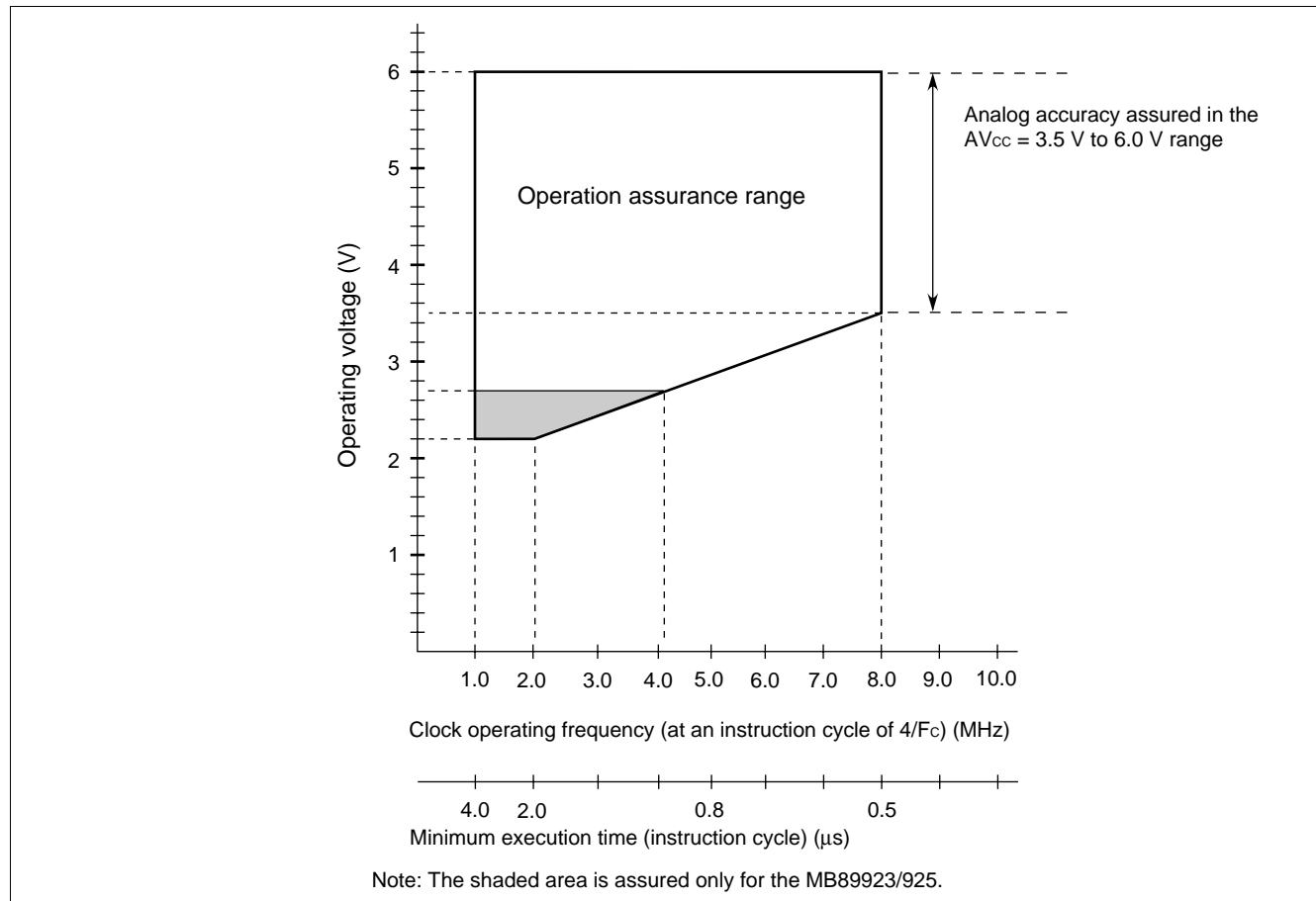


Figure 1 indicates the operating frequency of the external oscillator at an instruction cycle of 4/F_C. Since the operating voltage range is dependent on the instruction cycle, see minimum execution time if the operating speed is switched using a gear.

3. DC Characteristics

($V_{CC} = 5.0\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

| Parameter | Symbol | Pin | Condition | Value | | | Unit | Remarks |
|---|------------|--|--------------------------------|----------------|------|----------------|---------------|---|
| | | | | Min. | Typ. | Max. | | |
| “H” level input voltage | V_{IH} | P00 to P07, P10 to P17, P20 to P27, P30 to P32, P40 to P45, P50 to P57, P60 to P67, P70 to P77, P80 to P83, P90 to P97 | — | $0.7 V_{CC}$ | — | $V_{CC} + 0.3$ | V | |
| | V_{IHS} | \overline{RST} , MODA, \overline{HST} P00 to P03, P20, P23, P30, P32, P95, P97 | — | $0.8 V_{CC}$ | — | $V_{CC} + 0.3$ | V | Peripheral input of the port 0, 2, 3, and 9 |
| “L” level input voltage | V_{IL} | P00 to P07, P10 to P17, P20 to P27, P30 to P32, P40 to P45, P50 to P57, P60 to P67, P70 to P77, P80 to P83, P90 to P97 | — | $V_{SS} - 0.3$ | — | $0.3 V_{CC}$ | V | |
| | V_{ILS} | \overline{RST} , MODA, \overline{HST} P00 to P03, P20, P23, P30, P32, P95, P97 | — | $V_{SS} - 0.3$ | — | $0.2 V_{CC}$ | V | Peripheral input of the port 0, 2, 3, and 9 |
| Open-drain output pin application voltage | V_D | P40 to P45, P50 to P57, P60 to P67, P70 to P77, P80 to P83 ¹⁾ | — | $V_{SS} - 0.3$ | — | $V_{SS} + 6.0$ | V | |
| “H” level output voltage | V_{OH1} | P00 to P07, P10 to P17, P30 to P32, P90 to P97 | $I_{OH} = -2.0\text{ mA}$ | 4.0 | — | — | V | |
| | V_{OH2} | P20 to P27 | $I_{OH} = -5.0\text{ mA}$ | 2.4 | — | — | V | |
| “L” level output voltage | V_{OL1} | P00 to P07, P10 to P17, P30 to P32, P40 to P45, P50 to P57, P60 to P67, P70 to P77, P80 to P83, P90 to P97 | $I_{OL} = 4.0\text{ mA}$ | — | — | 0.4 | V | |
| | V_{OL2} | P20 to P27 | $I_{OL} = 5.0\text{ mA}$ | — | — | 0.4 | V | |
| | V_{OL3} | \overline{RST} | $I_{OL} = 4.0\text{ mA}$ | — | — | 0.4 | V | |
| Input leakage current (Hi-Z output leakage current) | I_{LI1} | P00 to P07, P10 to P17, P20 to P27, P30 to P32, P40 to P45, P50 to P57, P60 to P67, P70 to P77, P80 to P83, P90 to P97, MODA | $0.45\text{ V} < V_I < V_{CC}$ | — | — | ± 5 | μA | Without pull-up resistor |
| Pull-up resistance | R_{PULU} | P00 to P07, P20 to P27, P30 to P32, P90 to P97 | $V_I = 0.0\text{ V}$ | 25 | 50 | 100 | k Ω | With pull-up resistor |

(Continued)

MB89920 Series

(Continued)

($V_{CC} = 5.0\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

| Parameter | Symbol | Pin | Condition | Value | | | Unit | Remarks |
|---------------------------------------|------------|--|---|-------|------|---------|---------------|---|
| | | | | Min. | Typ. | Max. | | |
| Power supply current*2 | I_{CC} | V_{CC} | $V_{CC} = 5.0\text{ V}$ | — | 12 | 20 | mA | $t_{inst} = 0.5\ \mu\text{s}$ |
| | I_{CCS} | | $V_{CC} = 5.0\text{ V}$ | — | 3 | 7 | mA | Sleep mode $t_{inst} = 0.5\ \mu\text{s}$ |
| | I_{CCH} | | $T_A = +25^\circ\text{C}$ | — | — | 1 | μA | Stop mode |
| | I_A | AV_{CC} | when A/D conversion is activated | — | 6 | 8 | mA | |
| | I_{AH} | | when A/D conversion is stopped $T_A = +25^\circ\text{C}$ | — | — | 1 | μA | |
| LCD divided resistance | R_{LCD} | Between V3 and V_{SS} | | 200 | 300 | 450 | k Ω | |
| COM0 to 3 output impedance | R_{VCOM} | COM0 to COM3 | $V1$ to $V3 = 5.0\text{ V}$ | — | — | 2.5 | k Ω | |
| SEG0 to 27 output impedance | R_{VSEG} | SEG0 to SEG27 | $V1$ to $V3 = 5.0\text{ V}$ | — | — | 15 | k Ω | |
| LCD controller/driver leakage current | I_{LCDL} | V1 to V3, COM0 to COM3, SEG0 to SEG27 | $V1$ to $V3 = 5.0\text{ V}$ | — | — | ± 1 | μA | |
| Input capacitance | C_{IN} | Other than AV_{CC} , AV_{SS} , V_{CC} , and V_{SS} | $f = 1\text{ MHz}$ | — | 10 | — | pF | |

*1: V_D must not exceed V3.

*2: The measurement conditions of power supply current are as follows: the external clock and $T_A = +25^\circ\text{C}$.
In the case of the MB89PV920, the current consumed by the connected EPROM and ICE is not included.

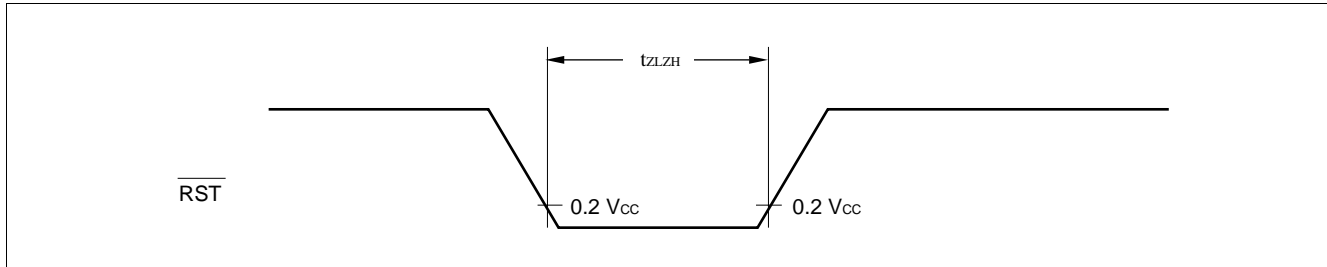
Note: For pins which serve as the LCD and ports (P40 to P45, P50 to P57, P60 to P67, P70 to P77, and P80 to P83), see the port parameter when these pins are used as ports and the LCD parameter when they are used as LCD pins.

5. AC Characteristics

(1) Reset Timing

($A_{V_{SS}} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

| Parameter | Symbol | Condition | Value | | Unit | Remarks |
|---|------------------|-----------|---------------------|------|------|---------|
| | | | Min. | Max. | | |
| $\overline{\text{RST}}$ "L" pulse width | t_{LZH} | — | $48 t_{\text{CYL}}$ | — | ns | |



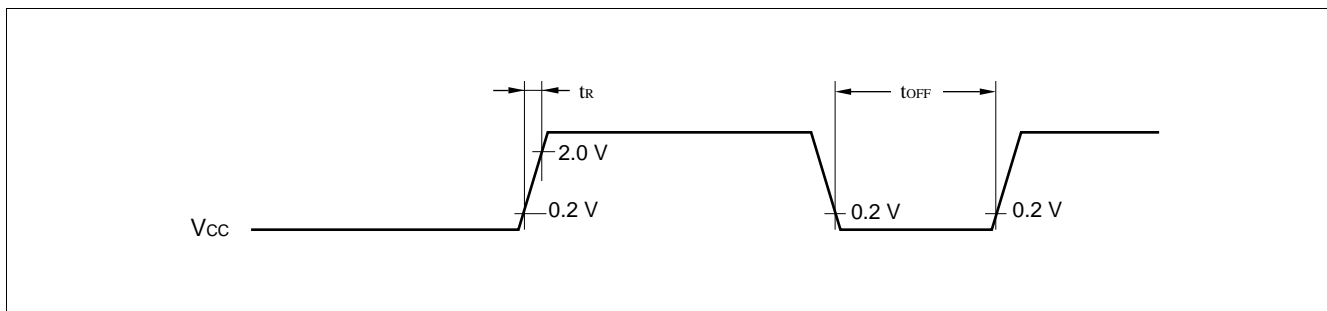
(2) Power-on Reset

($A_{V_{SS}} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

| Parameter | Symbol | Condition | Value | | Unit | Remarks |
|---------------------------|------------------|-----------|-------|------|------|------------------------------|
| | | | Min. | Max. | | |
| Power supply rising time | t_r | — | — | 50 | ms | Power-on reset function only |
| Power supply cut-off time | t_{OFF} | | 1 | — | ms | Due to repeated operations |

Note: Make sure that power supply rises within the selected oscillation stabilization time.

If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.



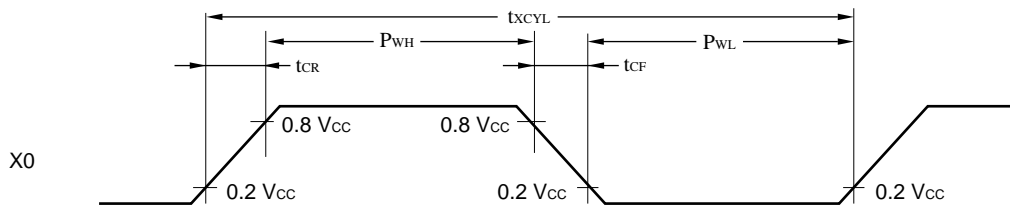
MB89920 Series

(3) Clock Timing

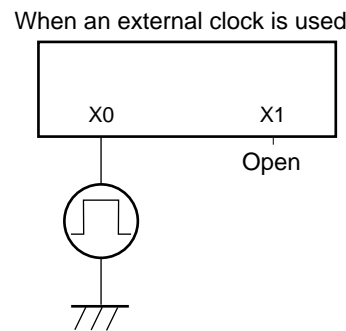
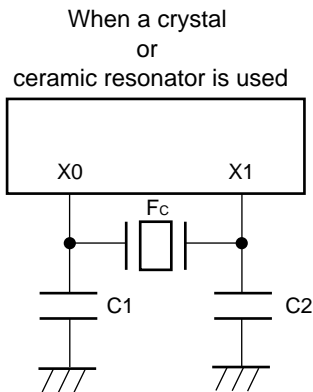
($A_{V_{SS}} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

| Parameter | Symbol | Pin | Condition | Value | | Unit | Remarks |
|---------------------------------|----------------------|--------|-----------|-------|------|------|----------------|
| | | | | Min. | Max. | | |
| Clock frequency | F_C | X0, X1 | — | 1 | 8 | MHz | |
| Clock cycle time | t_{XCYL} | X0, X1 | | 125 | 1000 | ns | |
| Input clock pulse width | P_{WH} P_{WL} | X0 | | 20 | — | ns | External clock |
| Input clock rising/falling time | t_{CR} t_{CF} | X0 | | — | 10 | ns | External clock |

X0 and X1 Timing and Conditions



Clock Conditions



(4) Instruction Cycle

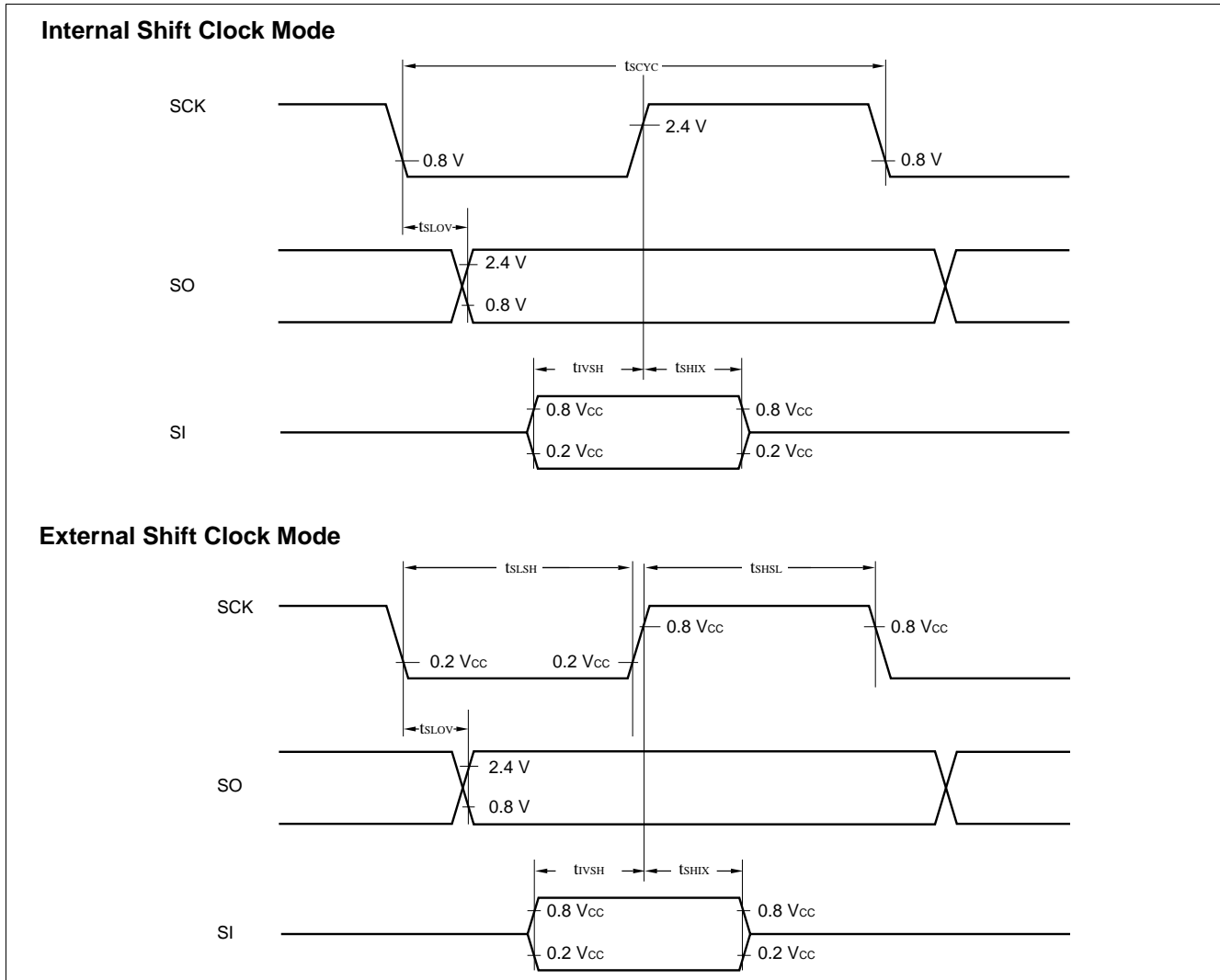
| Parameter | Symbol | Value (typical) | Unit | Remarks |
|--|------------|-----------------|---------------|---|
| Instruction cycle (minimum execution time) | t_{inst} | $4/F_C$ | μs | $(4/F_C) t_{inst} = 0.5\ \mu\text{s}$ when operating at $F_C = 8\ \text{MHz}$ |

(5) Serial I/O Timing

($AV_{CC} = V_{CC} = +5.0 V \pm 10\%$, $AV_{SS} = V_{SS} = 0.0 V$, $T_A = -40^\circ C$ to $+85^\circ C$)

| Parameter | Symbol | Pin | Condition | Value | | Unit | Remarks |
|---|------------|---------|---------------------------|------------------|---------|---------|---------|
| | | | | Min. | Max. | | |
| Serial clock cycle time | t_{SCYC} | SCK | Internal shift clock mode | $2 t_{inst}^*$ | — | μs | |
| SCK $\downarrow \rightarrow$ SO time | t_{SLOV} | SCK, SO | | -200 | 200 | ns | |
| Valid SI \rightarrow SCK \uparrow | t_{IVSH} | SI, SCK | | $1/2 t_{inst}^*$ | — | μs | |
| SCK $\uparrow \rightarrow$ valid SI hold time | t_{SHIX} | SCK, SI | | $1/2 t_{inst}^*$ | — | μs | |
| Serial clock "H" pulse width | t_{SHSL} | SCK | External shift clock mode | $1 t_{inst}^*$ | — | μs | |
| Serial clock "L" pulse width | t_{LSLH} | SCK | | $1 t_{inst}^*$ | — | μs | |
| SCK $\downarrow \rightarrow$ SO time | t_{SLOV} | SCK, SO | | 0 | 200 | ns | |
| Valid SI \rightarrow SCK \uparrow | t_{IVSH} | SI, SCK | | $1/2 t_{inst}^*$ | — | μs | |
| SCK $\uparrow \rightarrow$ valid SI hold time | t_{SHIX} | SCK, SI | $1/2 t_{inst}^*$ | — | μs | | |

* : For information on t_{inst} , see "(4) Instruction Cycle".



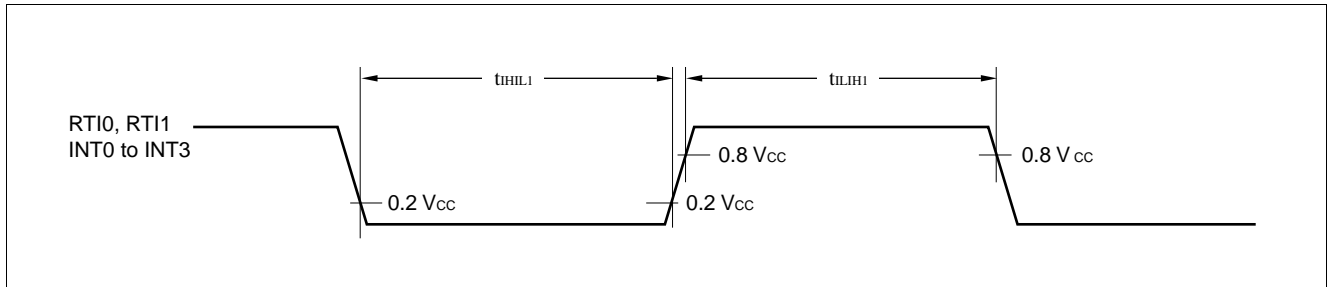
MB89920 Series

(6) Peripheral Input Timing

($V_{CC} = +5.0 V \pm 10\%$, $A_{V_{SS}} = V_{SS} = 0.0 V$, $T_A = -40^\circ C$ to $+85^\circ C$)

| Parameter | Symbol | Pin | Value | | Unit | Remarks |
|------------------------------------|-----------|--------------------------|----------------|------|------|---------|
| | | | Min. | Max. | | |
| Peripheral input "H" pulse width 1 | t_{LH1} | INT0 to INT3, RTI0, RTI1 | $2 t_{inst}^*$ | — | — | |
| Peripheral input "L" pulse width 1 | t_{HL1} | INT0 to INT3, RTI0, RTI1 | $2 t_{inst}^*$ | — | — | |

* : For information on t_{inst} , see "(4) Instruction Cycle".



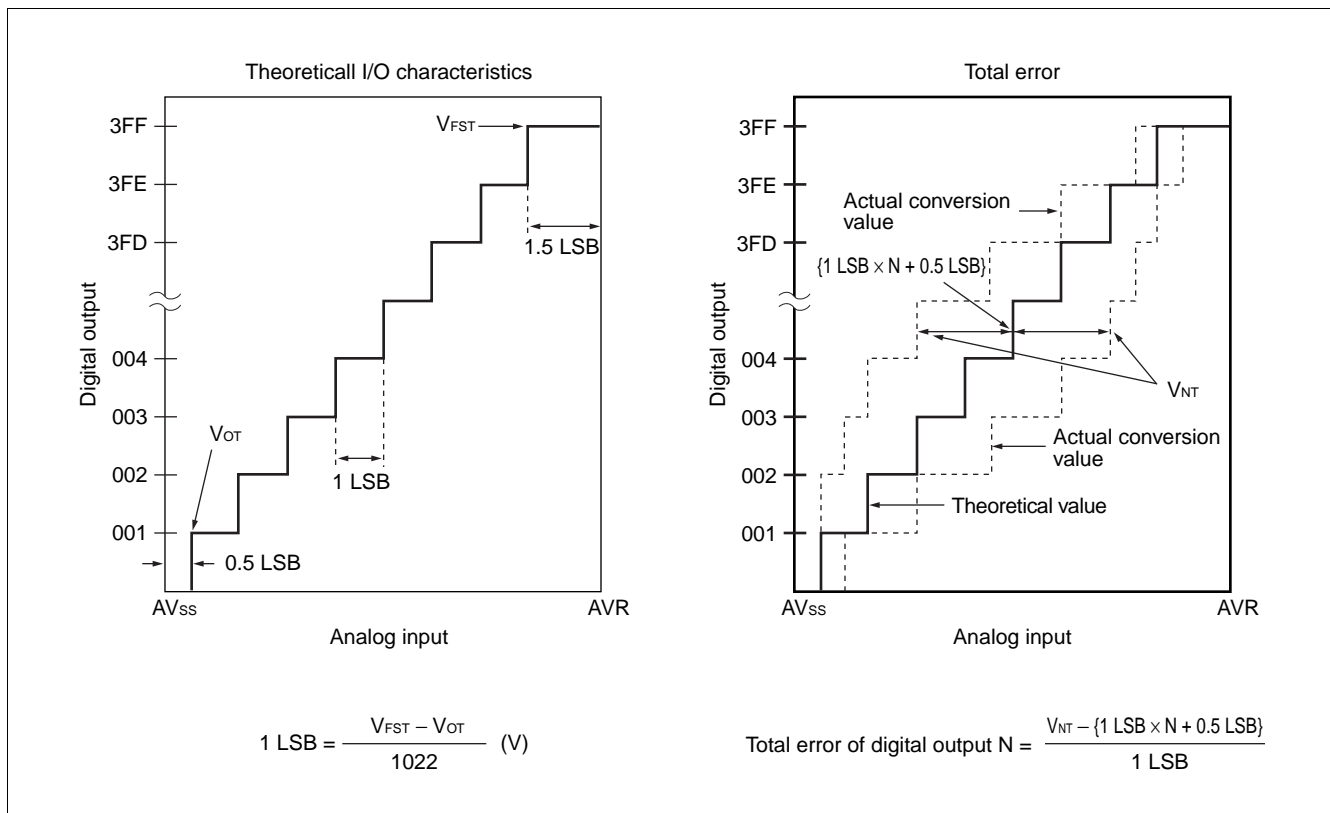
(7) A/D Converter Electrical Characteristics

($AV_{CC} = V_{CC} = +3.5 \text{ V to } +6.0 \text{ V}$, $F_C = 8 \text{ MHz}$, $AV_{SS} = V_{SS} = 0.0 \text{ V}$, $T_A = -40^\circ\text{C to } +85^\circ\text{C}$)

| Parameter | Symbol | Pin | Condition | Value | | | Unit |
|----------------------------------|-----------|------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|---------------|
| | | | | Min. | Typ. | Max. | |
| Resolution | — | — | | — | — | 10 | bit |
| Linearity error | | | | — | — | ± 2.0 | LSB |
| Differential linearity error | | | | — | — | ± 1.5 | LSB |
| Differential total error | | | | — | — | ± 3.0 | LSB |
| Zero transition voltage | V_{OT} | AN0 to AN7 | $AV_{CC} = AVR = V_{CC}$ | $AV_{SS} - 1.5 \text{ LSB}$ | $AV_{SS} + 0.5 \text{ LSB}$ | $AV_{SS} + 2.5 \text{ LSB}$ | V |
| Full-scale transition voltage | V_{FST} | AN0 to AN7 | | $AVR - 3.5 \text{ LSB}$ | $AVR - 1.5 \text{ LSB}$ | $AVR + 0.5 \text{ LSB}$ | V |
| Interchannel disparity | — | — | | — | — | 4 | LSB |
| A/D mode conversion time | | | | — | — | 16.5 | μs |
| Analog port input current | V_{AIN} | AN0 to AN7 | Source oscillation at 8 MHz | — | — | 10 | μA |
| Analog input voltage | — | AN0 to AN7 | — | 0.0 | — | AVR | V |
| Reference voltage | | AVR | — | 0.0 | — | AV_{CC} | V |
| Reference voltage supply current | I_R | AVR | $AVR = 5.0 \text{ V}$ | — | 200 | — | μA |

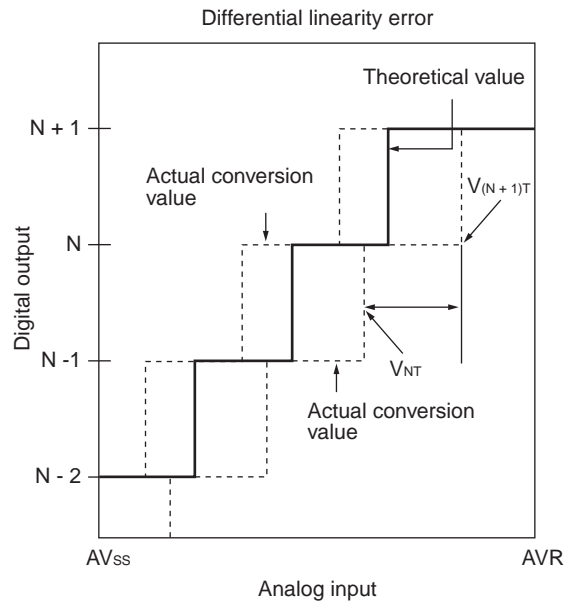
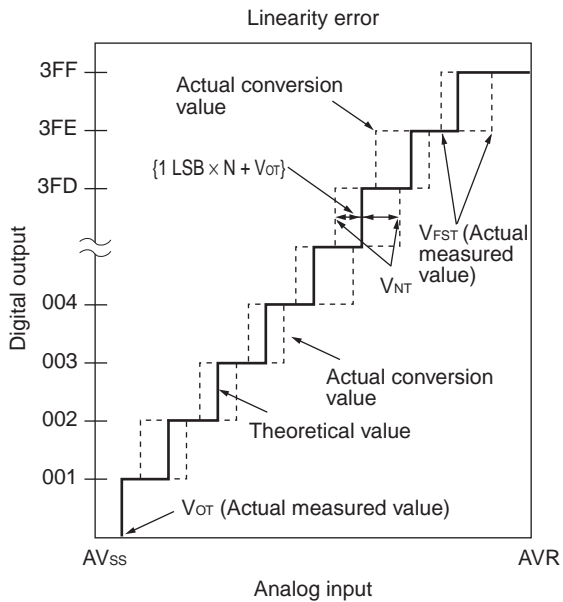
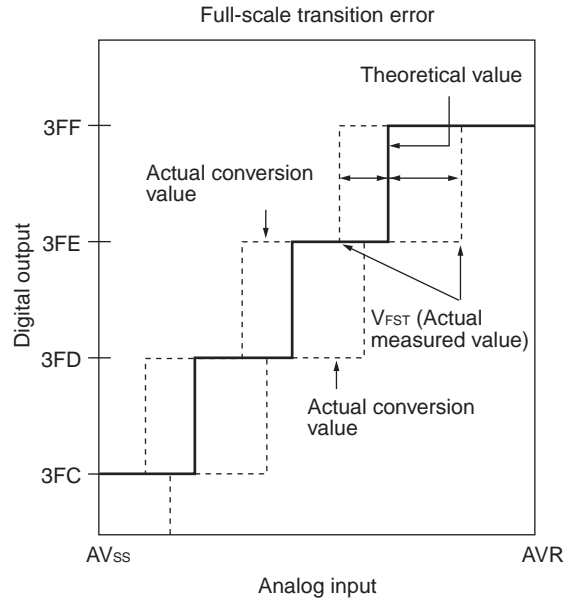
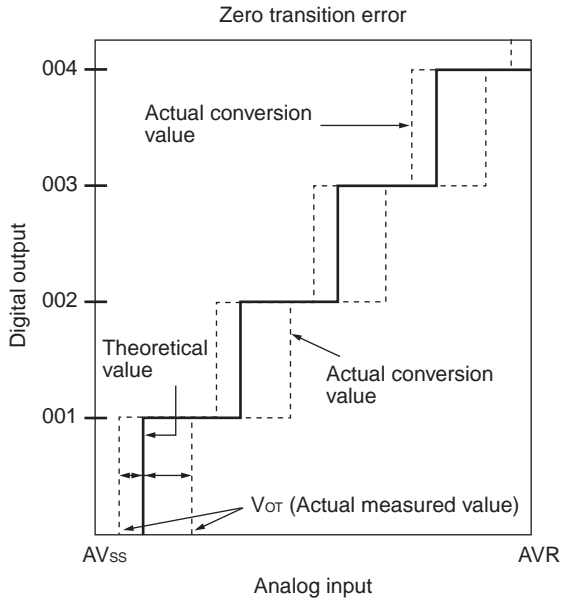
6. A/D Converter Glossary

- Resolution
Analog changes that are identifiable with the A/D converter.
- Linearity error
The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1111” ↔ “11 1111 1110”) from actual conversion characteristics
- Differential linearity error
The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value
- Total error
The difference between theoretical and actual conversion values, caused by the zero transition error, full-scale transition error, linearity error, quantization error, and noise.



(Continued)

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Linearity error of digital output $N = \frac{V_{NT} - \{1 \text{ LSB} \times N + V_{OT}\}}{1 \text{ LSB}}$

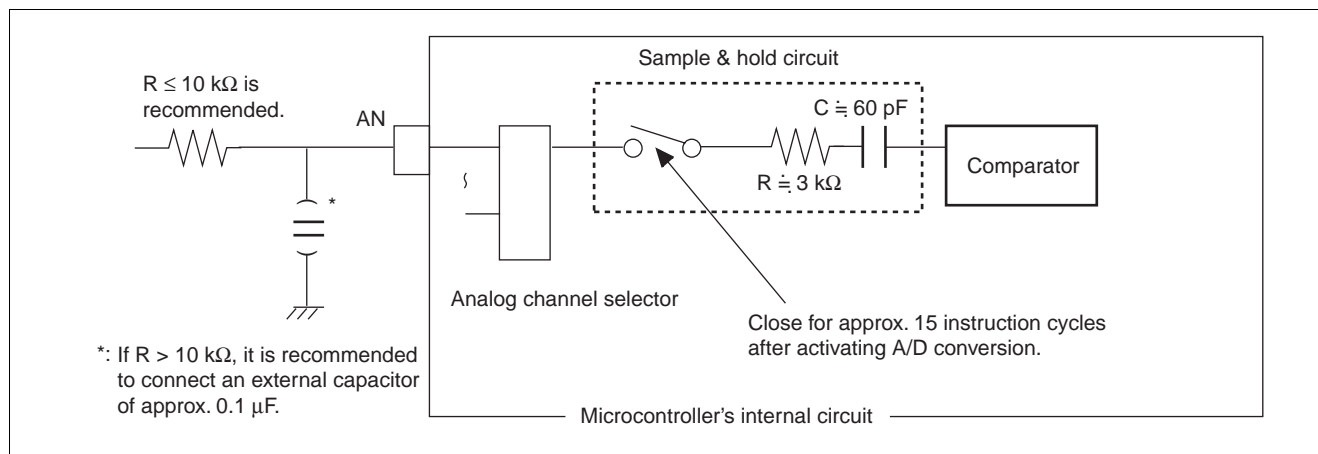
Differential linearity error of digital output $N = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}} - 1$

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7. Notes on A/D Converter

- The smaller $|AVR - AV_{SS}|$, the greater the error would become relatively.
- The output impedance of the external circuit for the analog input must satisfy the following conditions:
Output impedance of the external circuit < Approx. $10\text{ k}\Omega$
If the output impedance of the external circuit is too high, an analog voltage sampling time might be insufficient (sampling time = $7.5\text{ }\mu\text{s}$ at 8 MHz oscillation).

An analog input equivalent circuit is shown below.



Since the A/D converter contains sample & hold circuit, the level of the analog input pin might not stabilize within the sampling period after A/D activation, resulting in inaccurate A/D conversion values, if the input impedance to the analog pin is too high. Be sure to maintain an appropriate input impedance to the analog pin.

It is recommended to keep the input impedance to the analog pin not exceed $10\text{ k}\Omega$. If it exceeds $10\text{ k}\Omega$, it is recommended to connect a capacitor of approx. $0.1\text{ }\mu\text{F}$ for the analog input pin.

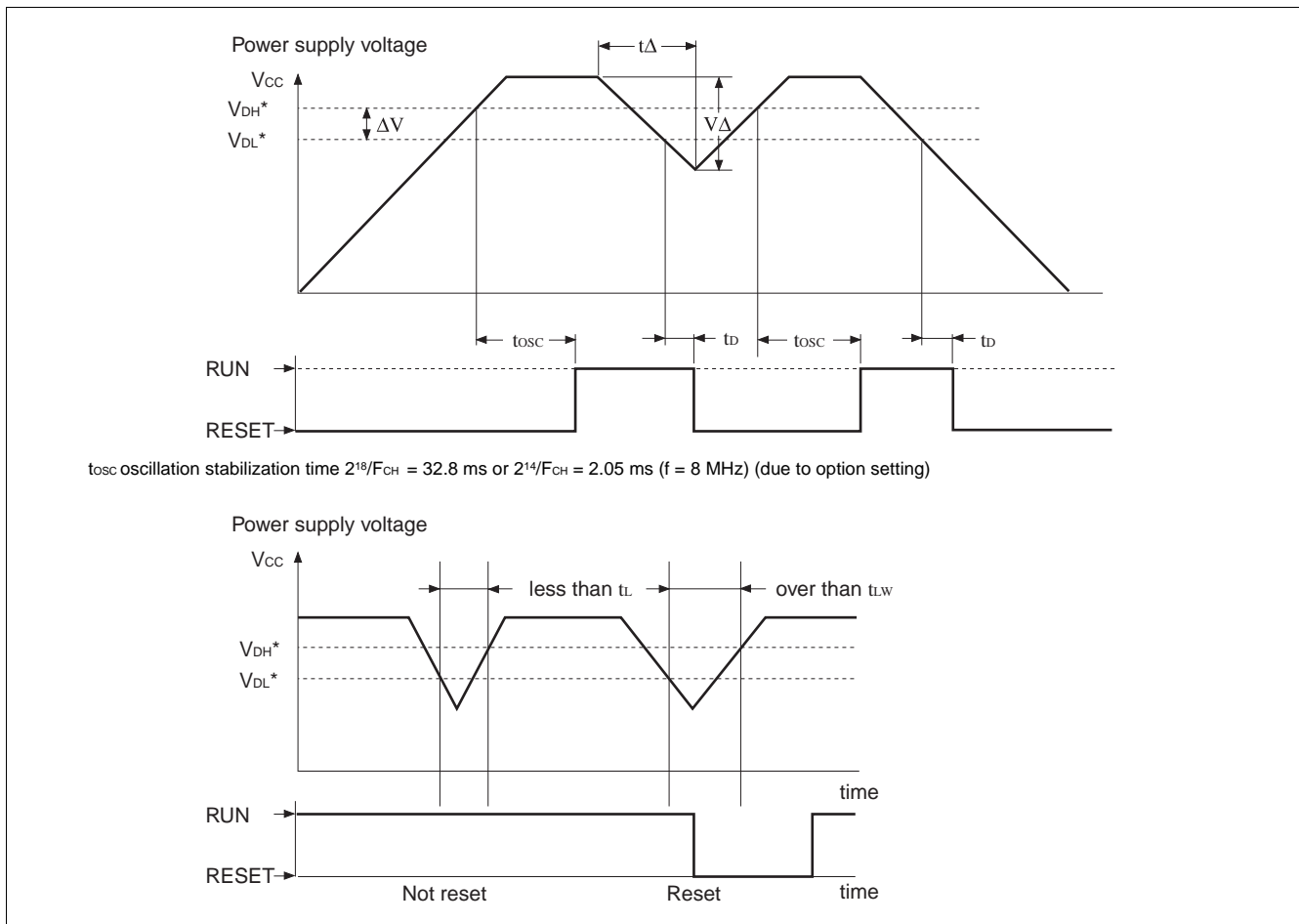
Except for the sampling period after A/D activation, the input leakage current of the analog input pin is less than $10\text{ }\mu\text{A}$.

8. Low-voltage Detection Reset

($V_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

| Parameter | Symbol | Condition | Value | | Unit | Remarks |
|---|------------|-----------|--------------|------|------------------------|---------|
| | | | Min. | Max. | | |
| Voltage detected at power supply voltage drop | V_{DL1} | | 3.00 | 3.60 | V | *1 |
| | V_{DL2} | | 3.30 | 3.90 | V | |
| | V_{DL3} | | 3.70 | 4.30 | V | |
| Voltage detected at power supply voltage rise | V_{DH1} | | 3.10 | 3.80 | V | |
| | V_{DH2} | | 3.40 | 4.10 | V | |
| | V_{DH3} | | 3.80 | 4.50 | V | |
| Hysteresis width | ΔV | | 0.10 | — | V | |
| Reset ignore time | t_L | | 0.3 | — | μs | |
| Reset sense time | t_{LW} | | 16 t_{CYL} | — | ns | |
| Reset detection delay time | t_D | | — | 2.0 | μs | |
| Voltage regulation ($V\Delta/t\Delta$) | VCR | | — | 0.10 | $\text{V}/\mu\text{s}$ | |

*1: V_{DH} and V_{DL} can be set for the MB89923 and MB89925 by mask options; for the MB89PV920 and MB89P928 by registers.



MB89920 Series

■ MASK OPTIONS

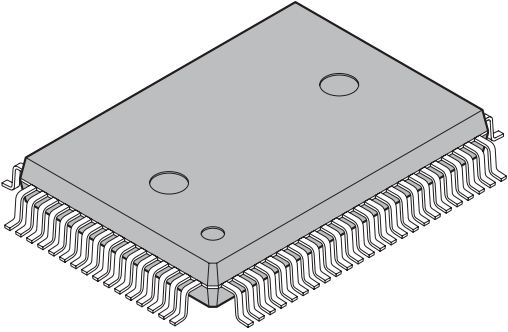
| No. | Part number | MB89923 MB89925 | MB89P928 | MB89PV920 |
|-----|--|--|---|--|
| | Specifying procedure | Specify when ordering masking | Set with EPROM programmer | Setting not possible |
| 1 | Pull-up resistors <ul style="list-style-type: none"> ┌ P00 to P07, P20 to P27, └ P30 to P32, P90 to P97 | P00 to P07, P20 to P27, P30 to P32, P90 to P97 : Selectable by pin | P00 to P07, P20 to P27, P30 to P32, P90 to P97 : Can be set per pin | No pull-up resistor |
| 2 | Power-on reset <ul style="list-style-type: none"> ┌ Power-on reset provided └ No power-on reset | Selectable | Can be set | With power-on reset |
| 3 | Oscillation stabilization time selection (at 8 MHz) <ul style="list-style-type: none"> ┌ Crystal oscillator (32.8 ms/8MHz) └ Ceramic oscillator (2.05 ms/8 MHz) | Selectable | Can be set | Crystal oscillator (32.8 ms/8 MHz) |
| 4 | Reset pin output <ul style="list-style-type: none"> ┌ Reset output provided └ No reset output | Selectable | Can be set | With reset output |
| 5 | Watchdog timer <ul style="list-style-type: none"> ┌ Activation prohibited └ Automatic activation | Selectable | Can be set | Inactive by default (Can be activated by software) |
| 6 | Low-voltage detection reset circuit <ul style="list-style-type: none"> ┌ Activation prohibited └ Automatic activation | Selectable | Can be set | Inactive by default (Can be activated by software) |
| 7 | Low-voltage detection reset output <ul style="list-style-type: none"> ┌ Output disabled └ Output enabled | Selectable | Can be set | Inactive by default (Can be activated by software) |
| 8 | Low-voltage detection voltage <ul style="list-style-type: none"> ┌ 3.3 V ± 0.3 V └ 3.6 V ± 0.3 V 4.0 V ± 0.3 V | Selectable | Can be set | Register setting |
| 9 | Low-voltage detection reset/watchdog timer function selection <ul style="list-style-type: none"> ┌ Register setting valid └ Option setting valid | Selectable | Can be set | Fixed to register setting |

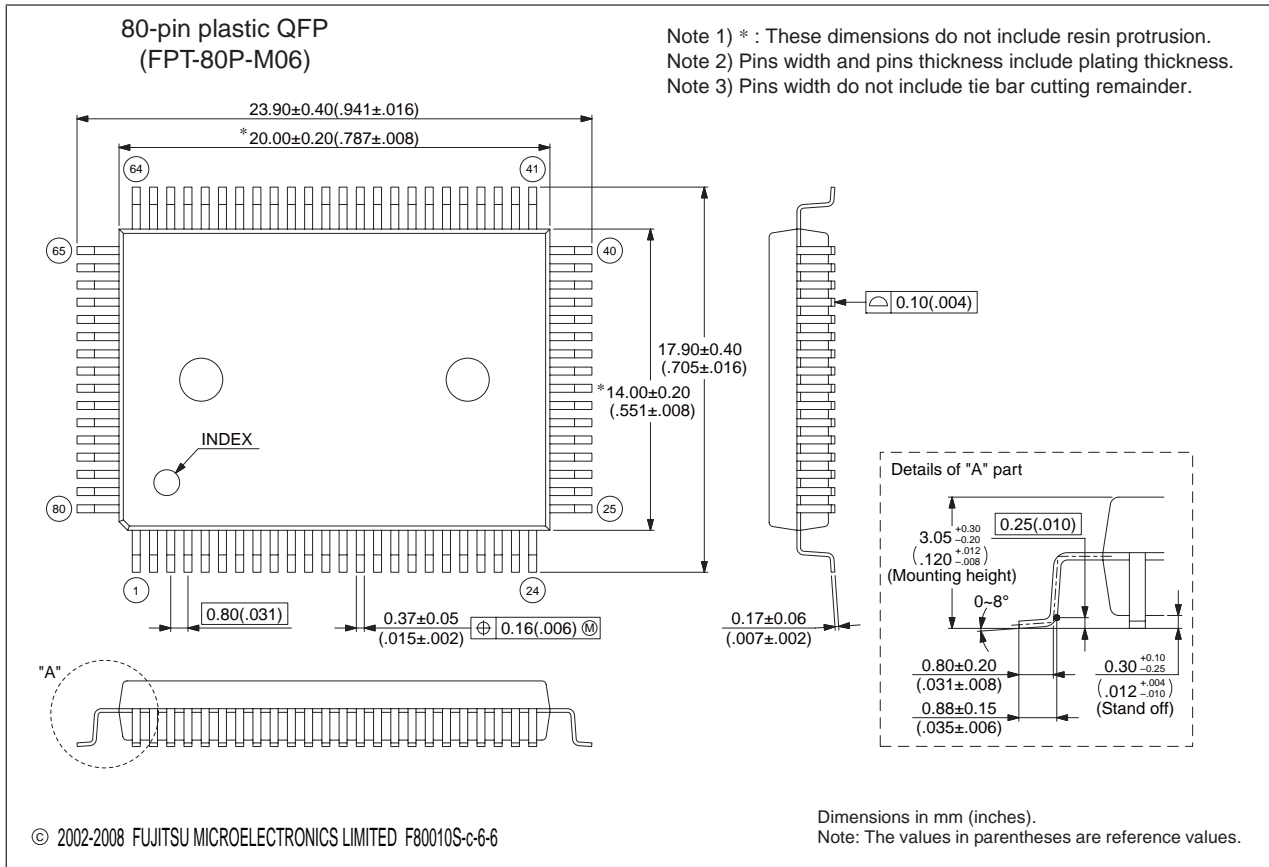
■ ORDERING INFORMATION

| Part number | Package | Remarks |
|--------------------------------------|--------------------------------------|---------|
| MB89923PF MB89925PF MB89P928PF | 80-pin Plastic QFP (FPT-80P-M06) | |
| MB89PV920CF | 80-pin Ceramic MQFP (MQP-80C-P01) | |

MB89920 Series

■ PACKAGE DIMENSIONS

| | | |
|--|--------------------------------|--------------------|
|  <p>80-pin plastic QFP</p> <p>(FPT-80P-M06)</p> | Lead pitch | 0.80 mm |
| | Package width × package length | 14.00 × 20.00 mm |
| | Lead shape | Gullwing |
| | Sealing method | Plastic mold |
| | Mounting height | 3.35 mm MAX |
| | Code (Reference) | P-QFP80-14×20-0.80 |
| | | |

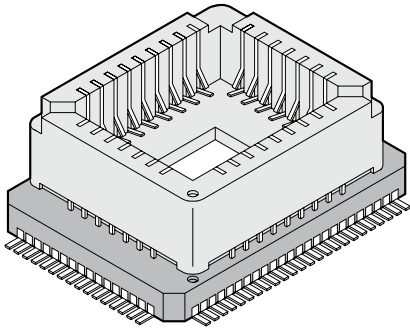


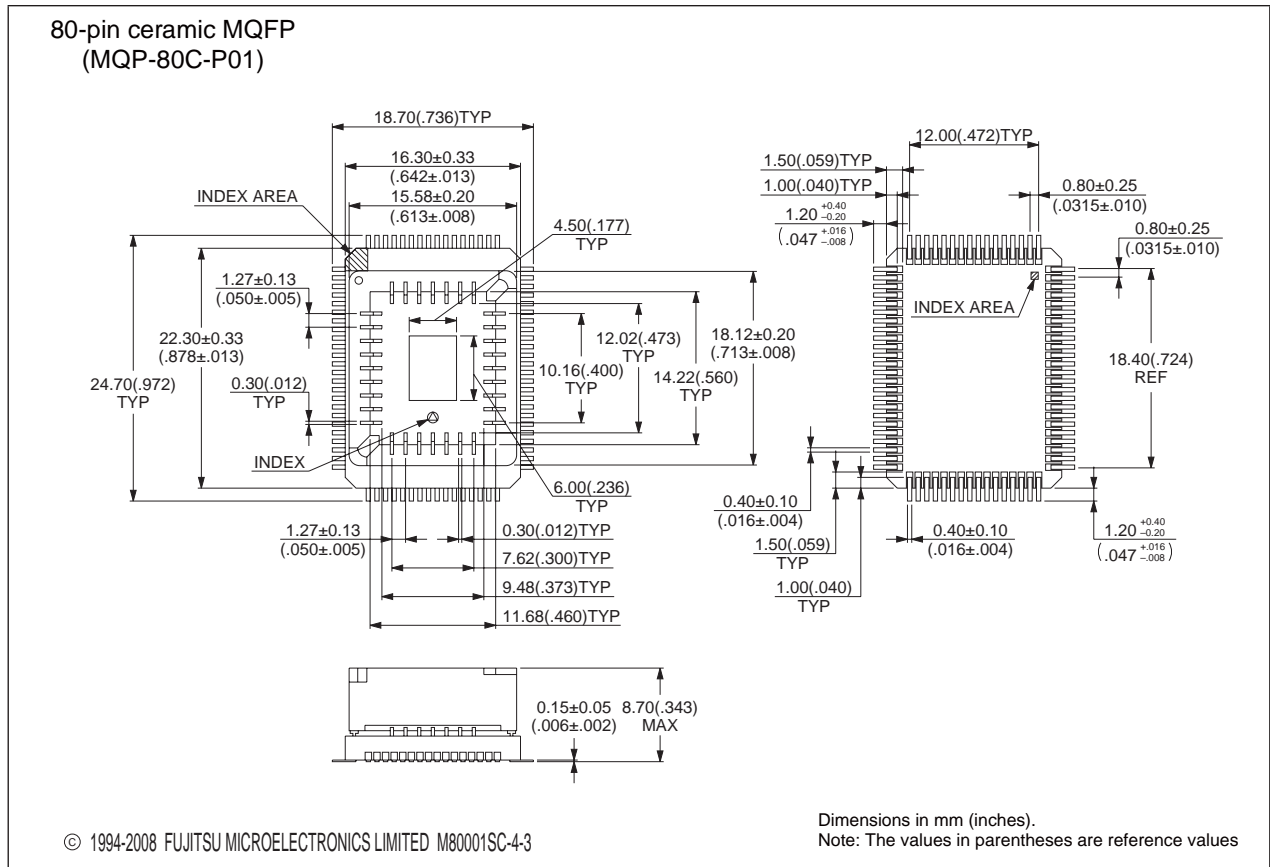
Please confirm the latest Package dimension by following URL.
<http://edevice.fujitsu.com/package/en-search/>

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MB89920 Series

(Continued)

| | | | |
|---|--------------------------|----------|--|
|  <p>80-pin ceramic MQFP</p> <p>(MQP-80C-P01)</p> | Lead pitch | 0.8 mm | |
| | Lead shape | Straight | |
| | Motherboard material | Ceramic | |
| | Mounted package material | Plastic | |
| | | | |
| | | | |



Please confirm the latest Package dimension by following URL.
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■ MAIN CHANGES IN THIS EDITION

| Page | Section | Change Results |
|------|---|---|
| 5, 6 | PIN ASSIGNMENT | Changed the pin name of pin 13. P92/CLK → P92/BUZ/CLK |
| 6 | | Changed the pin name of pin 86 to pin 91. AD7 to AD0 → A7 to A0 |
| 8 | PIN DESCRIPTION | Changed a pin no.. 7 to 11 → 7 to 10 |
| 14 | ■ PROGRAMMING TO THE EPROM ON THE MB89P928 | Deleted the “6. EPROM Programmer Socket Adapter”. |
| 16 | ■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE | Deleted the “2. Programming Socket Adapter”. |
| 17 | ■ BLOCK DIAGRAM | Changed a pin name in bottom right corner. |
| 29 | ■ ELECTRICAL CHARACTERISTICS 4. AC. Characteristics | (1) Reset Timing Changed the Value Min. 48 t _{HCYL} → 48 t _{XYL} |
| 33 | ■ ELECTRICAL CHARACTERISTICS 5. A/D Converter Electrical Characteristics | Changed the unit of “Zero transition voltage” and “Full-scale transition voltage” mV → V |
| — | ■ INSTRUCTIONS (136 INSTRUCTIONS) | Deleted the “INSTRUCTIONS (136 INSTRUCTIONS)” |
| — | ■ INSTRUCTION MAP | Deleted the “INSTRUCTION MAP” |

The vertical lines marked in the left side of the page show the changes.

MEMO

MB89920 Series

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