8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89120/120A Series

MB89121/123A/125A/P131/P133A/P135A
MB89PV130A

■ **DESCRIPTION**

The MB89120 series is a line of single-chip microcontrollers containing a compact instruction set and a great variety of peripheral functions such as a timer, serial interface, and external interrupt. The MB89120A series is an extended variant of the MB89120, with a remote control transmission function and wake-up interrupt function.

■ **FEATURES**

- F²MC-8L family CPU core
- Low-voltage operation
- Low current consumption (allowing for dual clock)
- Minimum execution time : 0.95 μs at 4.2 MHz
- 21-bit time-base counter
- I/O ports : Max. 36 ports
- External interrupts : 3 channels
- External interrupts (wake-up function) : 8 channels (only for the MB89120A series)
- 8-bit serial I/O : 1 channel
- 8/16-bit timer/counter : 1 channel
- Built-in remote-control transmitting frequency generator (only for the MB89120A series)
- Low-power consumption modes (stop mode, sleep mode, watch mode)
- Package : QFP-48
- CMOS technology

For the information for microcontroller supports, see the following web site.

http://edevice.fujitsu.com/micom/en-support/

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■ PRODUCT LINEUP

Part number Item	MB89121	MB89123A	MB89125A	MB89P133A	MB89P131
Classification	Mass-produced products (Mask ROM products)			One-time products	
ROM size	4 K × 8 bits (internal mask ROM)	8 K × 8 bits (internal mask ROM)	16 K × 8 bits (internal mask ROM)	8 K × 8 bits (Internal PROM to be programmed with a general-purpose EPROM programmer)	4 K × 8 bits (Internal PROM to be programmed with a general-purpose EPROM programmer)
RAM size	128 × 8 bits	256 × 8 bits			128 × 8 bits
CPU functions	The number of instructions : 136 Instruction bit length : 8 bits Instruction length : 1 to 3 bytes Data bit length : 1, 8, 16 bits Minimum execution time : 0.95 µs at 4.2 MHz Minimum interrupt processing time : 8.57 µs at 4.2 MHz				
Ports	Output ports (N-ch open-drain) : 4 (All also serves as peripherals.) Output ports (CMOS) : 8 I/O ports (CMOS) : 24 (8 ports also serve as peripherals.) Total : 36				
Timer/counter	8-bit timer/counter × 2 channels or 16-bit event counter × 1 channel				
Serial I/O	8 bits LSB/MSB first selectable				
External interrupt 1	3 independent channels (edge selection, interrupt vector, source flag) Rising edge/falling edge/both edges selectable Also for wake-up from stop/sleep mode (edge detection is also permitted in stop mode)				
External interrupt 2 (wake-up function)	—	8 channels (only for level detection)			—
Remote control transmitting frequency generator	—	1 channel (pulse width and frequency selectable by program)			—
Standby mode	Sleep mode, stop mode, watch mode				
Process	CMOS				
Operating voltage*	2.2 V to 4.0 V (with the dual clock option) 2.2 V to 6.0 V (with the single clock option)			2.7 V to 6.0 V	
EPROM for use	—				

* : Varies with conditions such as operating frequencies. (See "■ ELECTRICAL CHARACTERISTICS".)

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(Continued)

Part number / Item	MB89P135A	MB89PV130A
Classification	One-time PROM product	Piggyback/evaluation product
ROM size	16 K × 8 bits (internal PROM, to be programmed with general-purpose EPROM programmer)	32 K × 8 bits (external ROM)
RAM size	512 × 8 bits	1 K × 8 bits
CPU functions	The number of instructions : 136 Instruction bit length : 8 bits Instruction length : 1 to 3 bytes Data bit length : 1, 8, 16 bits Minimum instruction execution time : 0.95 μs at 4.2 MHz Minimum interrupt processing time : 8.57 μs at 4.2 MHz	
Ports	Output ports (N-ch open-drain ports) : 4 (All also serve as peripherals.) Output ports (CMOS) : 8 I/O ports (CMOS) : 24 (8 ports also serve as peripherals.) Total : 36	
Timer/counter	8-bit timer/counter × 2 channels or 16-bit event counter × 1 channel	
Serial I/O	8 bits LSB/MSB first selectable	
External interrupt 1	3 independent channels (edge selection, interrupt vector, source flag) Rising/falling/both edges selectable Used also for wake-up from stop/sleep mode. (Edge detection is also permitted in stop mode.)	
External interrupt 2 (wake-up function)	8 channels (only for level detection)	
Remote control transmitting frequency generator	1 channel (Pulse width and cycle selectable by program)	
Standby mode	Sleep mode, stop mode, and watch mode	
Process	CMOS	
Operating voltage	2.7 V to 6.0 V	2.7 V to 6.0 V
EPROM for use	—	MBM27C256A-20TVM

■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB89121	MB89123A	MB89125A	MB89P133A	MB89P131
FPT-48P-M13	○	○	○	○	○
MQP-48C-P01	×	×	×	×	×

Package	MB89P135A	MB89PV130A
FPT-48P-M13	○	×
MQP-48C-P01	×	○

○ : Available, × : Not available

Note : Package details of OTPROM products and piggyback/evaluation products are common to those of MB89130/130A series. Refer to the MB89130/130A series data sheet for details.

■ DIFFERENCES AMONG PRODUCTS

1. Memory Size

Before evaluating using the one-time ROM product, verify its difference from the product that will actually be used. Take particular care on the following points :
• The available number of register banks is different among the MB89121, the MB89123A/125A, and P135A/PV130A.
• The stack area, etc., is set at the upper limit of the RAM.

2. Current Consumption
• When operated at low-speed, a product with an OTPROM (EPROM) will consume more current than a product with a mask ROM. However, the current consumption in the sleep/stop mode is the same. (For more information, see "■ ELECTRICAL CHARACTERISTICS".)
• In the case of the MB89PV130A, added is the current consumed by the EPROM which is connected to the top socket.
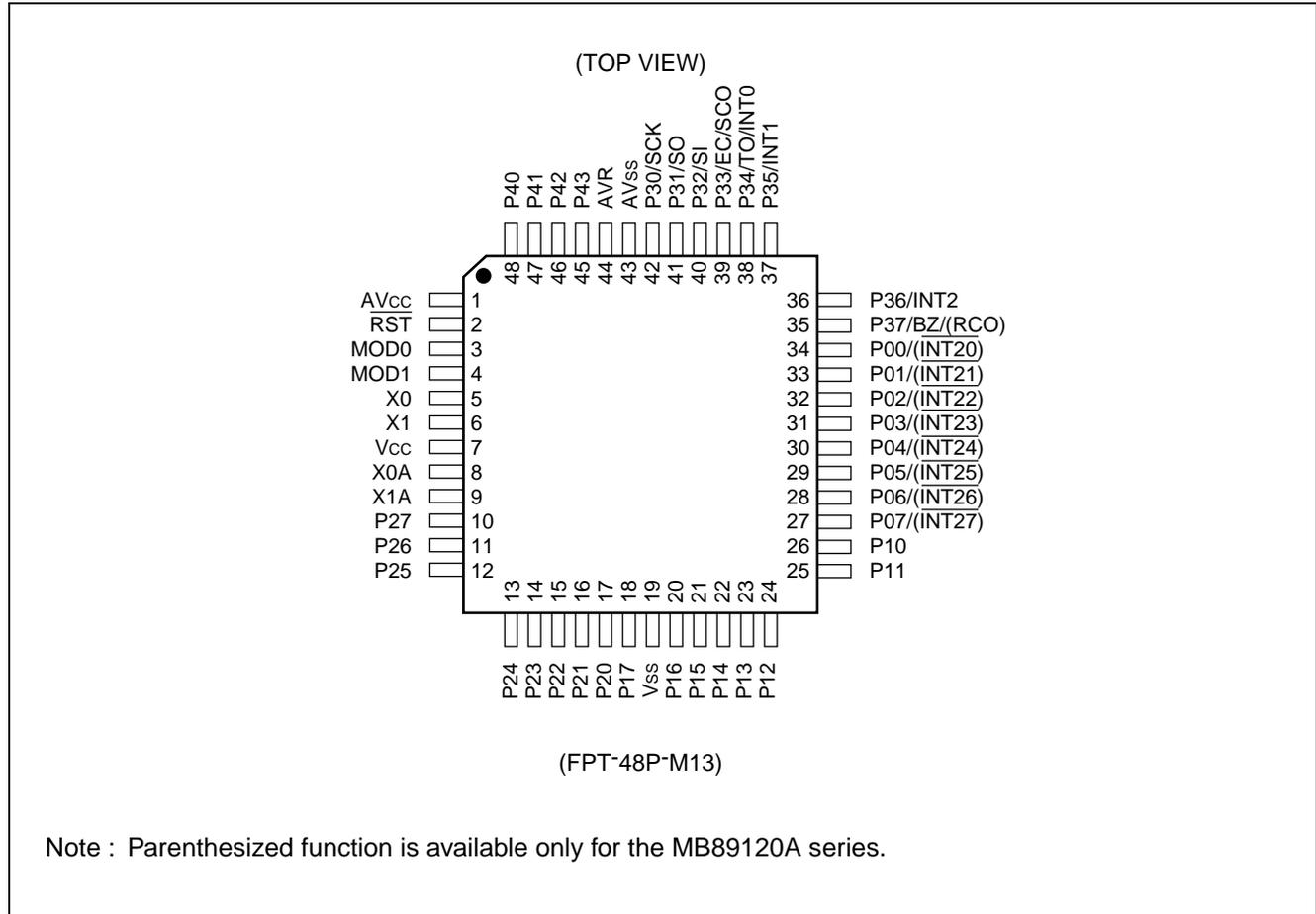
3. Mask Options

Functions that can be selected as options and how to designate these options vary with product.
Before using options, check "■ MASK OPTIONS".

Take particular care on the following point :
• Pull-up resistor cannot be set for P40 to P43 on the MB89P135A.
• Options are fixed on the MB89PV130A.

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■ **PIN ASSIGNMENT**

(TOP VIEW)

(FPT⁻48P⁻M13)

Note : Parenthesized function is available only for the MB89120A series.

■ PIN DESCRIPTION

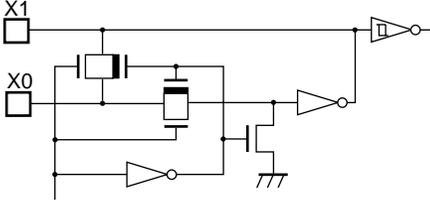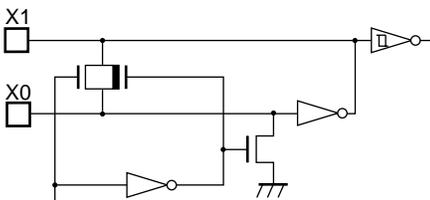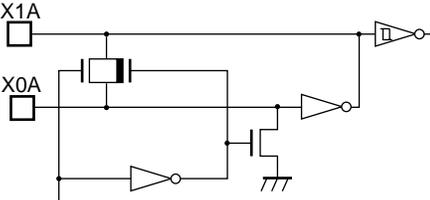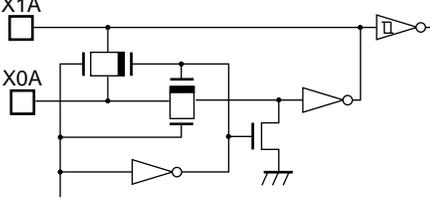| Pin no.	Pin name	Circuit type	Function
5	X0	A	Main clock crystal oscillator pins (max. 4.2 MHz)
6	X1		
8	X0A	B	Sub clock crystal oscillator pins (for 32.768 kHz)
9	X1A		
3	MOD0	C	Operation mode select pins Connect these pins directly to V_{SS}.
4	MOD1		
2	$\overline{RST}$	D	Reset I/O pin This port is of N-ch open-drain output type with pull-up resistor and a hysteresis input type. The internal circuit is initialized by the input of "L". "L" is output from this pin by an internal reset source as optional setting.
27 to 34	P07/ ($\overline{INT27}$) to P00/ ($\overline{INT20}$)	I	General-purpose I/O ports On the MB89120A series, these pins also serve as external interrupt input. External interrupt input pins are hysteresis input.
18, 20 to 26	P17 to P10	E	General-purpose I/O ports
10 to 17	P27 to P20	G	General-purpose output-only ports
42	P30/SCK	F	General-purpose I/O port Also serves as clock I/O for the 8-bit serial I/O interface. This port is of hysteresis input type.
41	P31/SO	F	General-purpose I/O port Also serves as a serial I/O data output. This port is hysteresis input type.
40	P32/SI	F	General-purpose I/O port Also serves as a serial I/O data input. This port is hysteresis input type.
39	P33/EC/SCO	F	General-purpose I/O port Also serves as the external clock input for the 8-bit timer/counter. This port is hysteresis input type. System clock output is optional.
38	P34/TO/INT0	F	General-purpose I/O port Also serves as the overflow output and external interrupt input for the 8-bit timer/counter. This port is hysteresis input type.
36, 37	P36/INT2, P35/INT1	F	General-purpose I/O ports Also serve as an external interrupt input. These ports are hysteresis input type.
35	P37/BZ/ (RCO)	F	General-purpose I/O port Also serves as a buzzer output. This port is hysteresis input type. On the MB89120A series, the pin also serves as a remote control output.

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Pin no.	Pin name	Circuit type	Function
45 to 48	P43 to P40	H	N-ch open-drain output ports
7	V$_{CC}$	—	Power supply pin
19	V$_{SS}$	—	Power supply (GND) pin
1	AV$_{CC}$	—	Power supply pin Use this pin at the same voltage as V$_{CC}$.
44	AVR	—	Reference voltage input pin
43	AV$_{SS}$	—	Power supply (GND) pin Use this pin at the same voltage as V$_{SS}$.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A	X1 X0 Standby control signal	• Crystal and ceramic oscillation type (main clock) Cricuit for the MB89P133A/P131/P135A/PV130A • External clock input select versions of MB89121/123A/125A At an oscillation feedback resistor of approximately 1 MΩ / 5 V
	X1 X0 Standby control signal	• Crystal and ceramic oscillation type (main clock) • Crystal or ceramic oscillator select versions of MB89121/123A/125A At an oscillation feedback resistor of approximately 1 MΩ / 5 V
B	X1A X0A Standby control signal	• Crystal and ceramic oscillation type (sub clock) Circuit for the MB89121/123A/125A At an oscillation feedback resistor of approximately 4.5 MΩ / 5 V
	X1A X0A Standby control signal	• Crystal and ceramic oscillation type (sub clock) Circuit for the MB89P131/P133A/P135A/PV130A At an oscillation feedback resistor of approximately 4.5 MΩ / 5 V
C		
D	R P-ch N-ch	• Output pull-up resistor (P-ch) of approximately 50 kΩ / 5 V • Hysteresis input
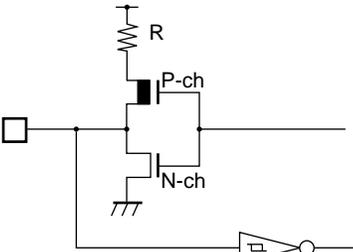
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Type	Circuit	Remarks
E		• CMOS output • CMOS input • Pull-up resistor optional
F		• CMOS output • Hysteresis input • Pull-up resistor optional
G		• CMOS output
H		• N-ch open-drain output • Pull-up resistor optional
I

Only for the MB89120A series | • CMOS output
• CMOS input
• The interrupt input is a hysteresis input (available only for the MB89120A series) .
• Pull-up resistor optional |

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■ HANDLING DEVICES

1.   Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- and high- withstand voltage pins, or if higher than the voltage which shows on "1. Absolute Maximum Ratings" in "■ ELECTRICAL CHARACTERISTICS" is applied between V_{CC} and V_{SS}.

When latchup occurs, power supply current increases rapidly, and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog power supply (AV_{CC} and AVR) and analog input from exceeding the digital power supply (V_{CC}) when the analog system power supply is turned on and off.

2.   Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to pull-up or pull-down resistor.

3.   Treatment of N.C. Pins

Be sure to leave N.C. (internally connected) pins open.

4.   Power Supply Voltage Fluctuations

Although operation is assured within the rated range of V_{CC} power supply voltage, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

5.   Precautions when Using an External Clock

When an external clock is used, oscillation stabilization time is required even for power-on reset (optional) and release from stop mode.

6.   Turning on the supply voltage (only for the MB89P135A)

When the power supply is turned on if MB89P135A is used, power on sharply up to 2.0 V within 13 clock cycles after starting of oscillation.
Further, various options may not be set , if power supply is turned on without the above condition.
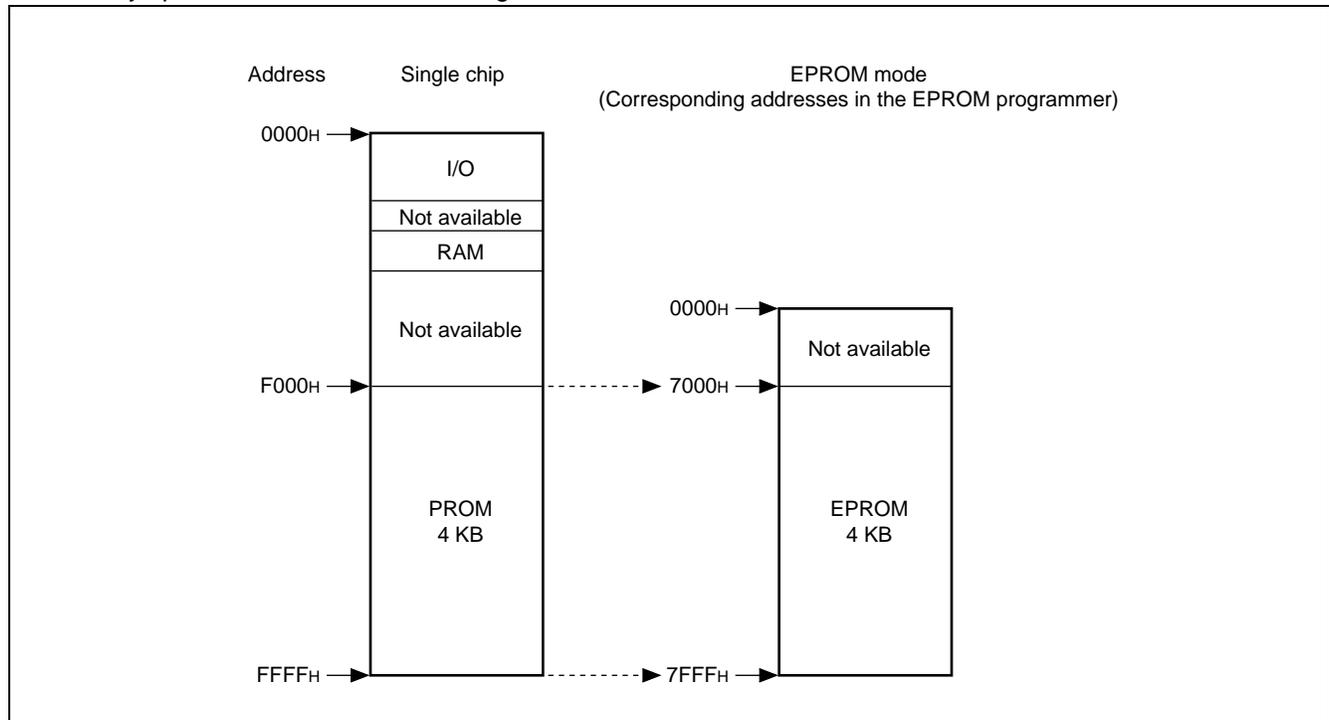
■ PROGRAMMING TO THE PROM ON THE MB89P131

The MB89P131 is a one-time PROM version of the MB89121.

1.   Features
• 4-Kbyte PROM on chip
• Equivalency to the MBM27C256A in EPROM mode (when programmed with the EPROM programmer)

2.   Memory Space

Memory space in EPROM mode is diagrammed below :

3.   Programming to the PROM

In EPROM mode the MB89P131 functions equivalent to the MBM27C256A. This allows the PROM to be programmed with a general-purpose EPROM programmer by using the dedicated socket adapter. Note, however, that the electronic signature mode cannot be used.

• **Programming procedure**
(1)   Set the EPROM programmer to MBM27C256A.
(2)   Load program data into the EPROM programmer at 7000_H to $7FFF_H$ (note that addresses $F000_H$ to $FFFF_H$ while operating as a single chip correspond to 7000_H to $7FFF_H$ in EPROM mode) .
(3)   Program with the EPROM programmer.
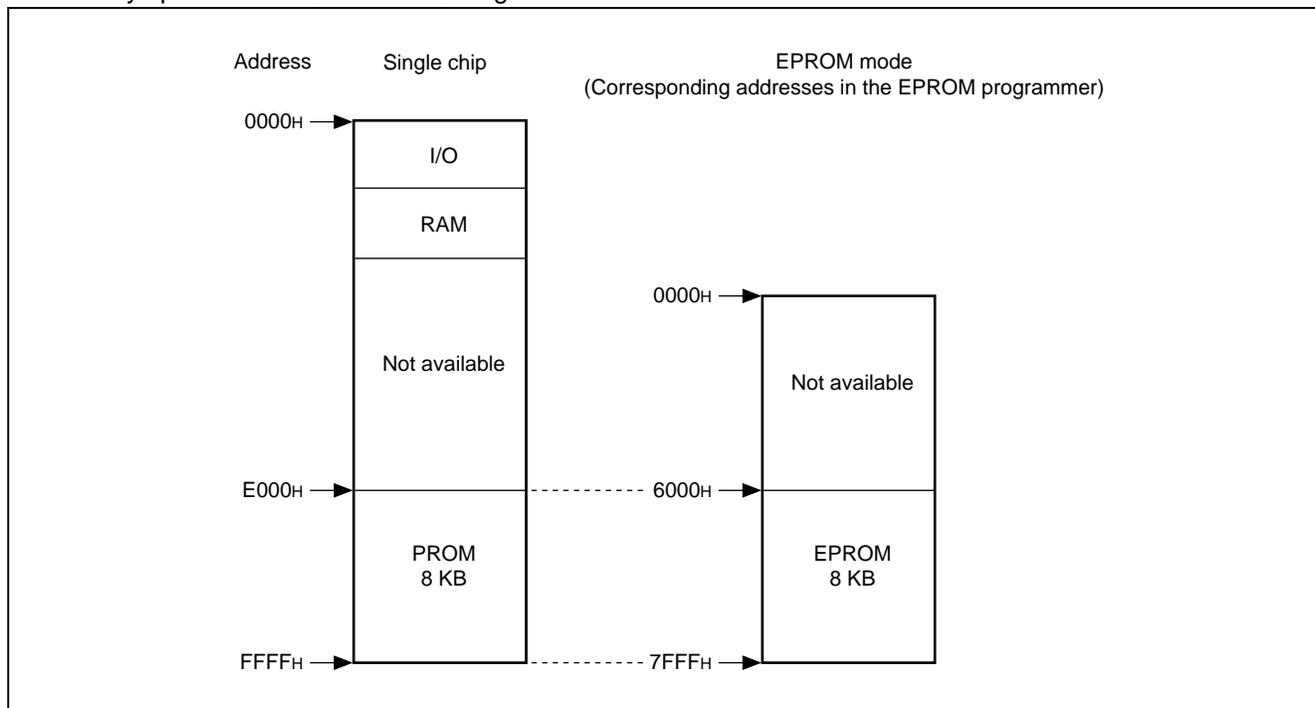
■ PROGRAMMING TO THE PROM ON THE MB89P133A

The MB89P133A is a one-time PROM version of the MP89123A.

1. Features
- 8-Kbyte PROM on chip
- Equivalency to the MBM27C256A in EPROM mode (when programmed with the EPROM programmer)

2. Memory Space

Memory space in EPROM mode is diagrammed below :

3. Programming to the PROM

In EPROM mode the MB89P133A functions equivalent to the MBM27C256A, This allows the PROM to be programmed with a general-purpose EPROM programmer by using the dedicated socket adapter. Note, however, that the MB89P133A cannot use the electronic signature mode.

- **Programming procedure**
  (1) Set the EPROM programmer to MBM27C256A.
  (2) Load program data into the EPROM programmer at 6000_H to $7FFF_H$ (note that addresses $E000_H$ to $FFFF_H$ while operating as a single chip correspond to 6000_H to $7FFF_H$ in EPROM mode) .
  (3) Program with the EPROM programmer.
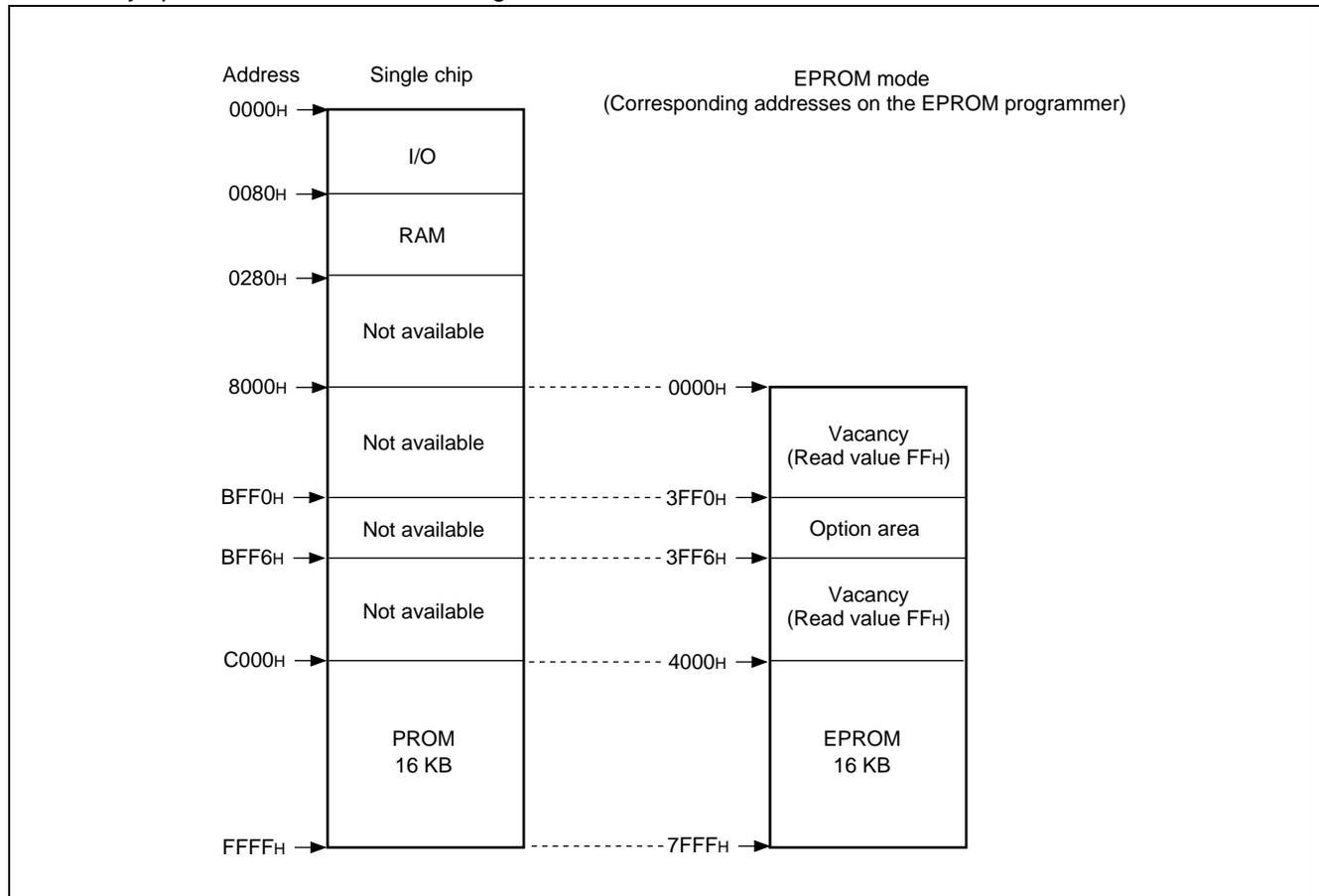
■ PROGRAMMING TO THE PROM ON THE MB89P135A

The MB89P135A is an OTPROM version of the MB89123A/125A.

1. Features
- 16-Kbyte PROM on chip
- Equivalency to the MBM27C256A in EPROM mode (when programmed with the EPROM programmer)

2. Memory Space

Memory space in EPROM mode is diagrammed below.

3. Programming to the PROM

In EPROM mode, the MB89P135A functions equivalent to the MBM27C256A. This allows the PROM to be programmed with a general-purpose EPROM programmer (the electronic signature mode cannot be used) by using the dedicated socket adapter.

- **Programming procedure**
  (1) Set the EPROM programmer to the MBM27C256A.
  (2) Load program data into the EPROM programmer at 4000$_H$ to 7FFF$_H$ (note that addresses C000$_H$ to FFFF$_H$ while operating as a single chip correspond to 4000$_H$ to 7FFF$_H$ in EPROM mode) .
  (3) Load option data into the EPROM programmer at 3FF0$_H$ to 3FF6$_H$.
  (4) Program with the EPROM programmer.

4. Setting PROM Options (MB89P135A Only)

The programming procedure is the same as that for the PROM. Options can be set by programming values at the addresses shown on the memory map. The relationship between bits and options is shown on the following bit map :
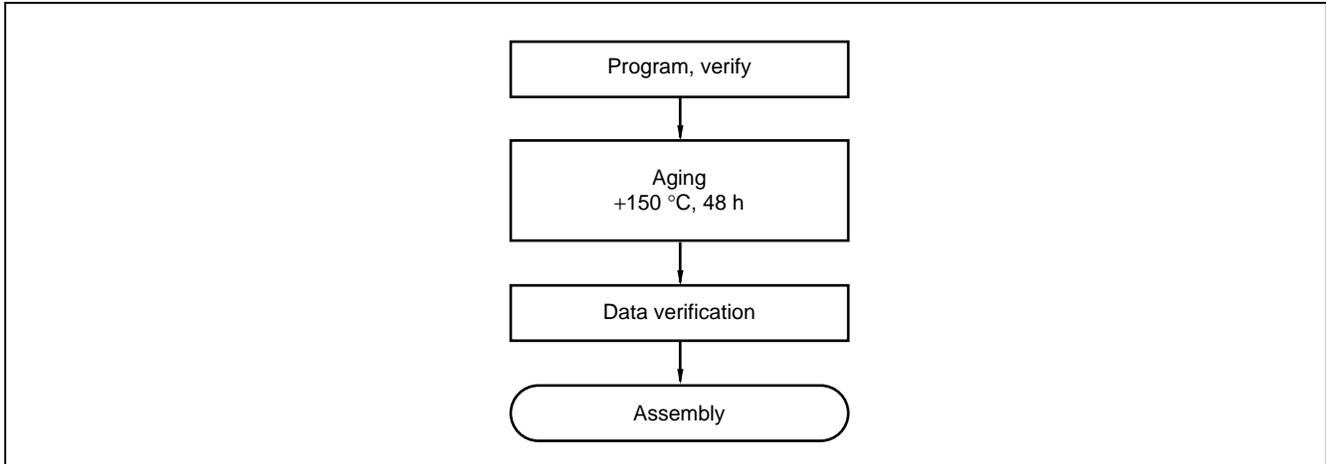
• **PROM option bit map**

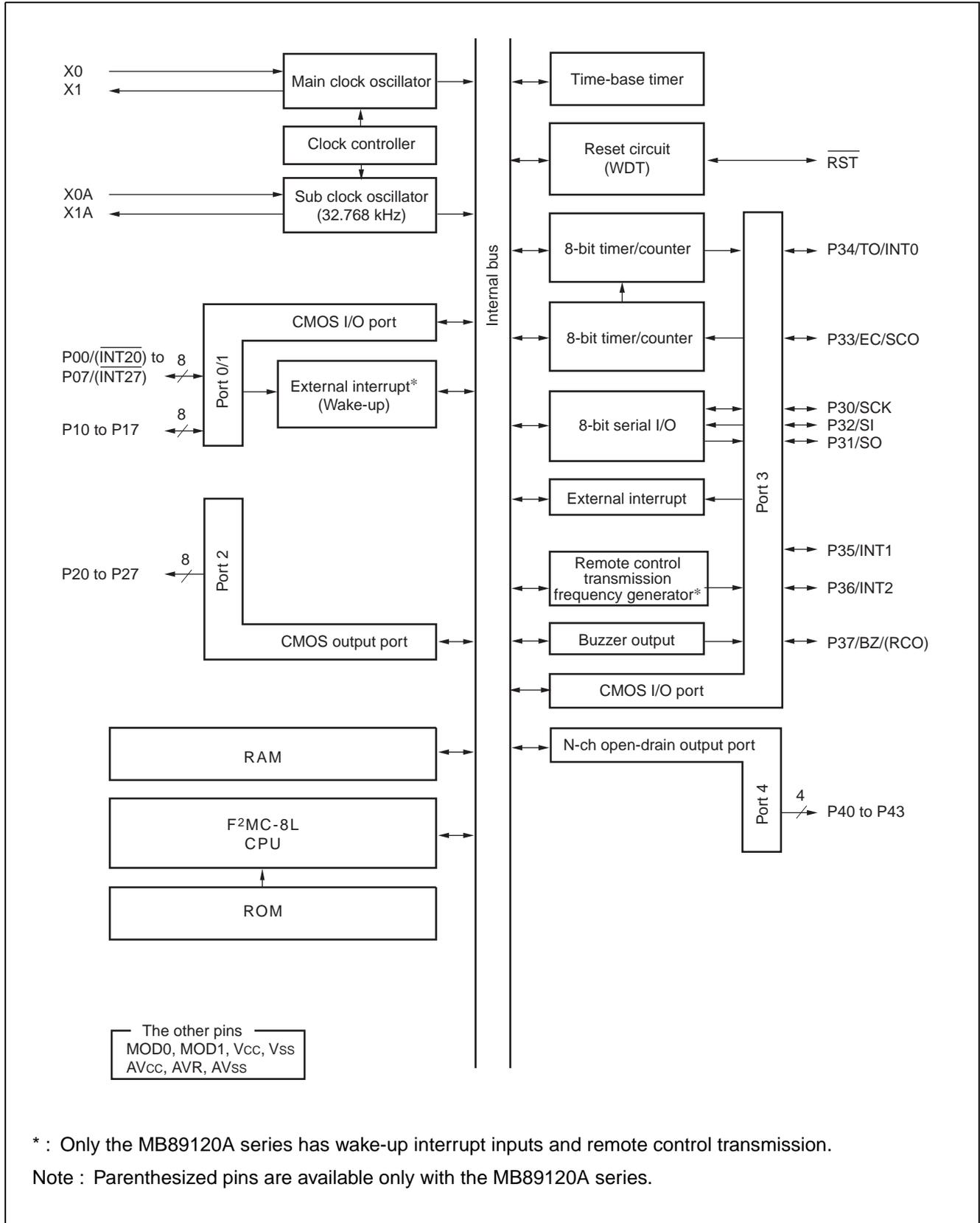| Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
3FF0$_H$	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Clock mode selection 1 : Single clock 0 : Dual clock	Reset pin output 1 : Yes 0 : No	Power-on reset 1 : Yes 0 : No	Oscillation stabilization time	
							00 : 2^2/F_{CH} 01 : 2^{12}/F_{CH}	10 : 2^{16}/F_{CH} 11 : 2^{18}/F_{CH}
3FF1$_H$	P07 Pull-up 1 : Yes 0 : No	P06 Pull-up 1 : Yes 0 : No	P05 Pull-up 1 : Yes 0 : No	P04 Pull-up 1 : Yes 0 : No	P03 Pull-up 1 : Yes 0 : No	P02 Pull-up 1 : Yes 0 : No	P01 Pull-up 1 : Yes 0 : No	P00 Pull-up 1 : Yes 0 : No
3FF2$_H$	P17 Pull-up 1 : Yes 0 : No	P16 Pull-up 1 : Yes 0 : No	P15 Pull-up 1 : Yes 0 : No	P14 Pull-up 1 : Yes 0 : No	P13 Pull-up 1 : Yes 0 : No	P12 Pull-up 1 : Yes 0 : No	P11 Pull-up 1 : Yes 0 : No	P10 Pull-up 1 : Yes 0 : No
3FF3$_H$	P37 Pull-up 1 : Yes 0 : No	P36 Pull-up 1 : Yes 0 : No	P35 Pull-up 1 : Yes 0 : No	P34 Pull-up 1 : Yes 0 : No	P33 Pull-up 1 : Yes 0 : No	P32 Pull-up 1 : Yes 0 : No	P31 Pull-up 1 : Yes 0 : No	P30 Pull-up 1 : Yes 0 : No
3FF4$_H$	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable
3FF5$_H$	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable
3FF6$_H$	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable

Note : Each bit is set to "1" as the initialized value, therefore the pull-up option is selected.

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■ HANDLING MB89P131/P133A/P135A

1. Recommended Screening Conditions

High-temperature aging is recommended as the pre-assembly screening procedure.

```
┌─────────────────────────┐
│     Program, verify     │
└─────────────────────────┘
             │
             ▼
┌─────────────────────────┐
│          Aging          │
│      +150 °C, 48 h      │
└─────────────────────────┘
             │
             ▼
┌─────────────────────────┐
│    Data verification    │
└─────────────────────────┘
             │
             ▼
      (    Assembly    )
```

2. Programming Yield

Due to its nature, bit programming test cannot be conducted as Fujitsu delivery test. For this reason, a pro-gramming yeild of 100% cannot be assured at all times.

■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

1. EPROM for Use

MBM27C256A-20TVM

2. Memory Space

Memory space in each mode, such as 32-Kbyte EPROM is diagrammed below.
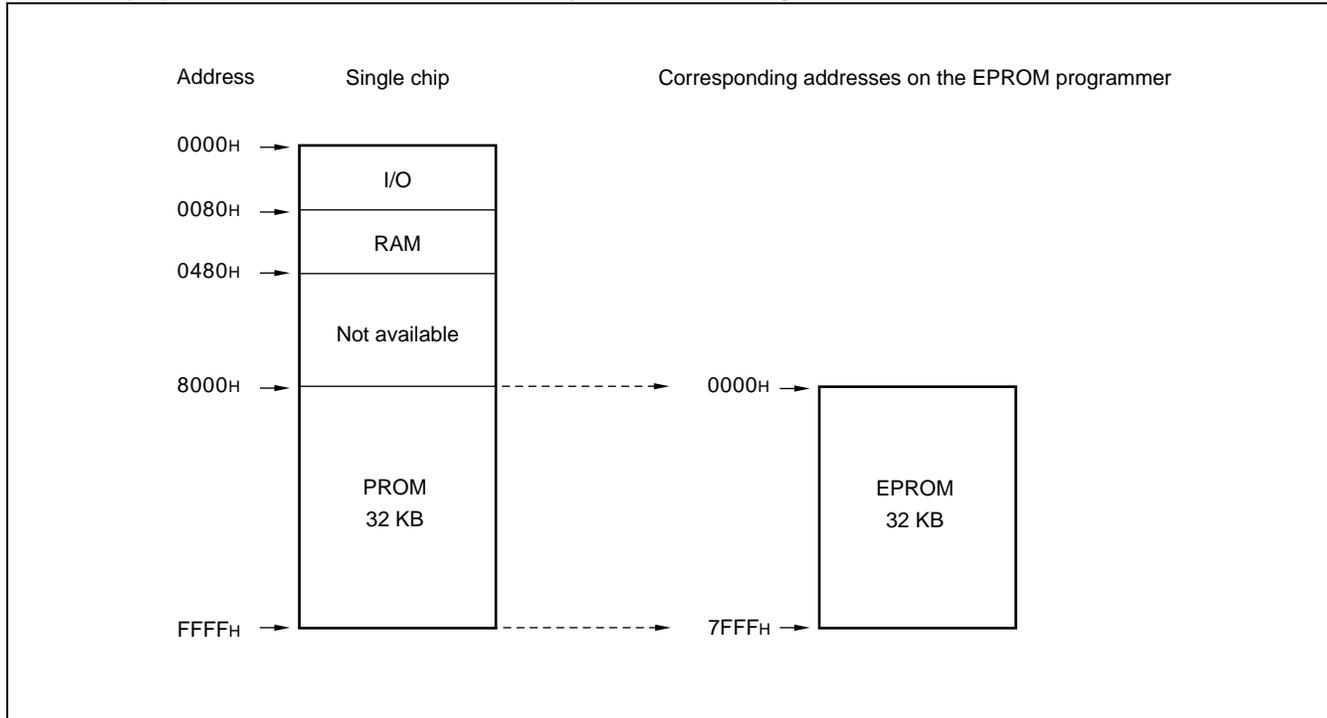
3. Programming to the EPROM
(1) Set the EPROM programmer for the MBM27C256A.
(2) Load program data into the EPROM programmer at 0000_H to $7FFF_H$.
(3) Program with the EPROM programmer.

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■ BLOCK DIAGRAM

* : Only the MB89120A series has wake-up interrupt inputs and remote control transmission.

Note : Parenthesized pins are available only with the MB89120A series.

■ CPU CORE

1. Memory Space

The microcontrollers of the MB89120/120A series offer 64 Kbytes of memory for storing all of I/O, data, and program areas. The I/O area is allocated from the lowest address. The data area is allocated immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is allocated from exactly the opposite end of I/O area, that is, near the highest address. The tables of interrupt reset vectors and vector call instructions are allocated from the highest address with the program area. The memory space of the MB89120/120A series is structured as illustrated below :

Memory Space
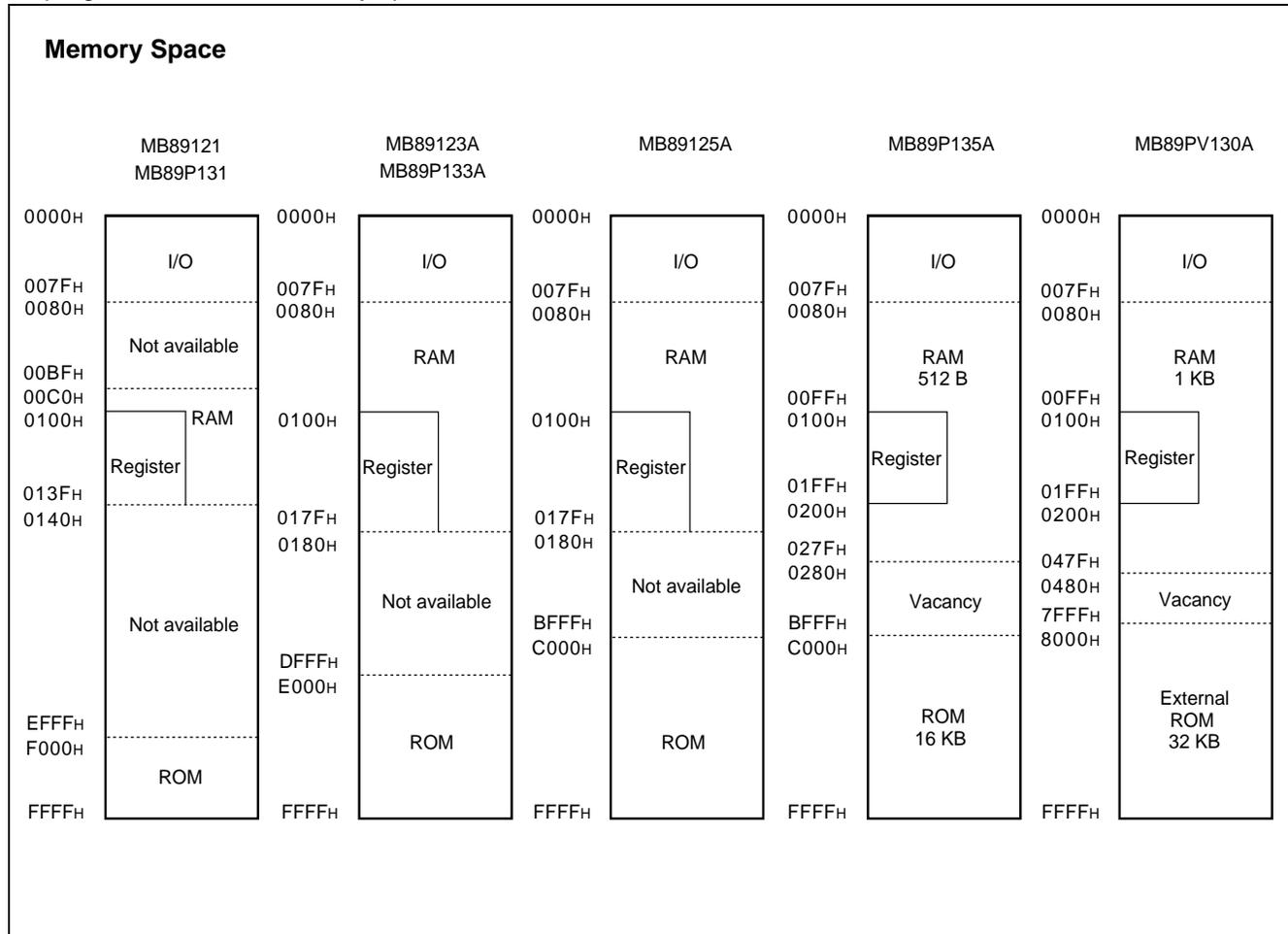
2. Registers

The F²MC-8L family has two types of registers; dedicated hardware registers and general-purpose memory registers. The following dedicated registers are provided :

Program counter (PC) :	A 16-bit register for indicating the instruction storage positions
Accumulator (A) :	A 16-bi temporary register for arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
Temporary accumulator (T) :	A 16-bit register which is used for arithmetic operations with the accumulator When the instruction is an 8-bit data processing instruction, the lower byte is used.
Index register (IX) :	A 16-bit register for index modification
Extra pointer (EP) :	A 16-bit pointer for indicating a memory address
Stack pointer (SP) :	A 16-bit pointer for indicating a stack area
Program status (PS) :	A 16-bit register for storing a register pointer, a condition code

		Initial value
16 bits		
PC	: Program counter	FFFD$_H$
A	: Accumulator	Indeterminate
T	: Temporary accumulator	Indeterminate
IX	: Index register	Indeterminate
EP	: Extra pointer	Indeterminate
SP	: Stack pointer	Indeterminate
PS	: Program status	I-flag = 0, IL1, IL0 = 11. The other bit values are Indeterminate.
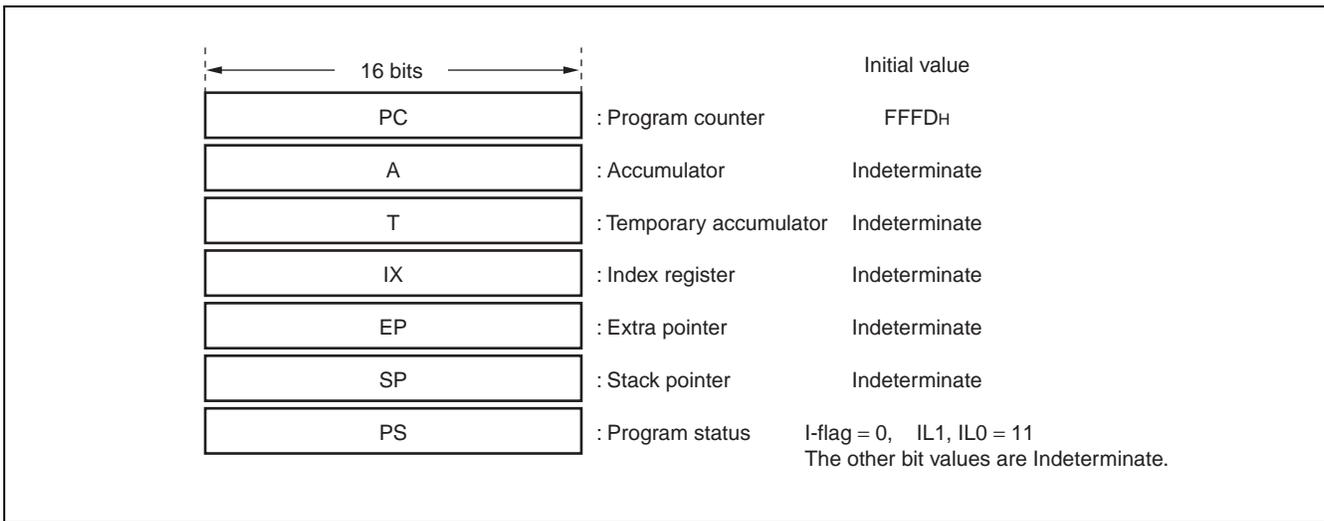
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR) (see the diagram below) .

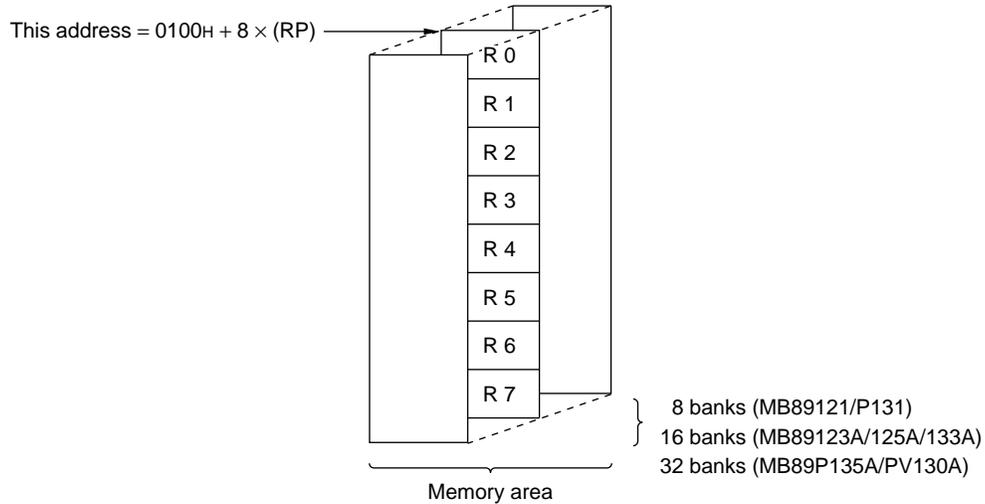**Structure of the Program Status Register**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PS	RP				Vacancy	Vacancy	Vacancy	H	I	IL1, IL0		N	Z	V	C

RP   CCR

The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

Rule for Conversion of Actual Addresses of the General-purpose Register Area

								RP					Lower OP codes		
"0"	"0"	"0"	"0"	"0"	"0"	"0"	"1"	R4	R3	R2	R1	R0	b2	b1	b0
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓

Generated addresses

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data, and bits for control of CPU operations at the time of an interrupt.

H-flag : Set to "1" when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared "0" otherwise. This flag is for decimal adjustment instructions.

I-flag : Interrupt is enabled when this flag is set to "1". Interrupt is disabled when the flag is cleared to "0". Cleared to "0" at the reset.

IL1, IL0 : Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	High-low
0	0	1	High
0	1		
1	0	2	↕
1	1	3	Low

N-flag : Set to "1" if the MSB becomes "1" as the result of an arithmetic operation. Cleared to "0" otherwise.

Z-flag : Set to "1" when an arithmetic operation results in 0. Cleared to "0" otherwise.

V-flag : Set to "1" if the twos complement overflows as a result of an arithmetic operation. Cleared to "0" if the overflow does not occur.

C-flag : Set to "1" when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared to "0" otherwise. Set to the shift-out value in the case of a shift instruction.

The following general-purpose registers are provided :

General-purpose registers : 8-bit registers for storing data

The general-purpose registers are of 8 bits and located in the register banks of the memory. One bank contains 8 registers and up to a total of 8 banks can be used on the MB89121/P131, and a total of 16 banks can be used on the MB89123A/125A/P133A and a total of 32 banks can be used on the MB89P135A/PV130A.

The bank currently in use is indicated by the register bank pointer (RP) .

Register Bank Configuration

This address $= 0100_H + 8 \times (RP)$

R 0
R 1
R 2
R 3
R 4
R 5
R 6
R 7

8 banks (MB89121/P131)
16 banks (MB89123A/125A/133A)
32 banks (MB89P135A/PV130A)

Memory area

FUJITSU

MBMB89120/120A Series

■ **I/O MAP**

Address	Read/Write	Register name	Register description
00$_H$	(R/W)	PDR0	Port 0 data register
01$_H$	(W)	DDR0	Port 0 data direction register
02$_H$	(R/W)	PDR1	Port 1 data register
03$_H$	(W)	DDR1	Port 1 data direction register
04$_H$	(R/W)	PDR2	Port 2 data register
05$_H$			Vacancy
06$_H$			Vacancy
07$_H$	(R/W)	SYCC	System clock control register
08$_H$	(R/W)	STBC	Standby control register
09$_H$	(R/W)	WDTC	Watchdog control register
0A$_H$	(R/W)	TBTC	Time-base timer control register
0B$_H$	(R/W)	WPCR	Watch prescaler control register
0C$_H$	(R/W)	PDR3	Port 3 data register
0D$_H$	(W)	DDR3	Port 3 data direction register
0E$_H$	(R/W)	PDR4	Port 4 data register
0F$_H$	(R/W)	BZCR	Buzzer register
10$_H$			Vacancy
11$_H$			Vacancy
12$_H$	(R/W)	SCGC	Peripheral control clock register
13$_H$			Vacancy
14$_H$	(R/W)	RCR1	Remote control transmission control register 1*
15$_H$	(R/W)	RCR2	Remote control transmission control register 2*
16$_H$			Vacancy
17$_H$			Vacancy
18$_H$	(R/W)	T2CR	Timer 2 control register
19$_H$	(R/W)	T1CR	Timer 1 control register
1A$_H$	(R/W)	T2DR	Timer 2 data register
1B$_H$	(R/W)	T1DR	Timer 1 data register
1C$_H$	(R/W)	SMR1	Serial mode register
1D$_H$	(R/W)	SDR1	Serial data register
1E$_H$			Vacancy
1F$_H$			Vacancy

(Continued)

(Continued)

Address	Read/write	Register name	Register description
20H	Vacancy		
21H	Vacancy		
22H	Vacancy		
23H	(R/W)	EIC1	External interrupt control register 1
24H	(R/W)	EIC2	External interrupt control register 2
25H	Vacancy		
26H to 31H	Vacancy		
32H	(R/W)	EIE2	External interrupt 2 enable register*
33H	(R/W)	EIF2	External interrupt 2 flag register*
34H to 7BH	Vacancy		
7CH	(W)	ILR1	Interrupt level register 1
7DH	(W)	ILR2	Interrupt level register 2
7EH	(W)	ILR3	Interrupt level register 3
7FH	Vacancy		

* : Only in the MB89120A series

Note : Do not use vacancies.

■ ELECTRICAL CARACTERISTICS

1. Absolute Maximum Ratings

$(AV_{SS} = V_{SS} = 0.0 \text{ V})$

Parameter	Symbol	Rating Min.	Rating Max.	Unit	Remarks
Power supply voltage	V_{CC} AV_{CC} AVR	$V_{SS} - 0.3$	$V_{SS} + 7.2$	V	Use V_{CC}, AV_{CC} , and AVR set to the same voltage.
Program voltage	V_{PP}	$V_{SS} - 0.6$	$V_{SS} + 13.0$	V	MOD1 pin on the MB89P131/P133A/P135A
Input voltage	V_I	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	
Output voltage	V_O	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	
"L" level maximum output current	I_{OL}	—	10	mA	
"L" level average output current	I_{OLAV}	—	4	mA	Avarage value (operating current $\times$ operating rate)
"L" level total maximum output current	ΣI_{OL}	—	100	mA	
"L" level total average output current	ΣI_{OLAV}	—	20	mA	Avarage value (operating current $\times$ operating rate)
"H" level maximum output current	I_{OH}	—	-10	mA	
"H" level average output current	I_{OHAV}	—	-2	mA	Avarage value (operating current $\times$ operating rate)
"H" level total maximum output current	ΣI_{OH}	—	-30	mA	
"H" level total average output current	ΣI_{OHAV}	—	-10	mA	Avarage value (operating current $\times$ operating rate)
Power consumption	P_D	—	200	mW	
Operating temperature	T_A	-40	$+85$	°C	
Storage temperature	Tstg	-55	$+150$	°C	

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2.   Recommended Operating Conditions

(AV$_{SS}$ = V$_{SS}$ = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V$_{CC}$	2.2	6.0	V	Normal operation assurance range * Applied to "Single-clock MB89121/123A/125A"
		2.2	4.0	V	Normal operation assurance range * Applied to "Dual-clock MB89121/123A/125A"
		2.7	6.0	V	Normal operation assurance range * Applied to "MB89P131/P133A/P135A/PV130A"
		1.5	6.0	V	Retains the RAM state in stop mode
Operating temperature	T$_A$	−40	+85	°C	

* : These values vary with the operating conditions. See "Operating Voltage vs. Main Clock Operating Frequency."

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

• Operating Voltage vs. Main Clock Operating Frequency

Dual-clock MB89121/123A/125A
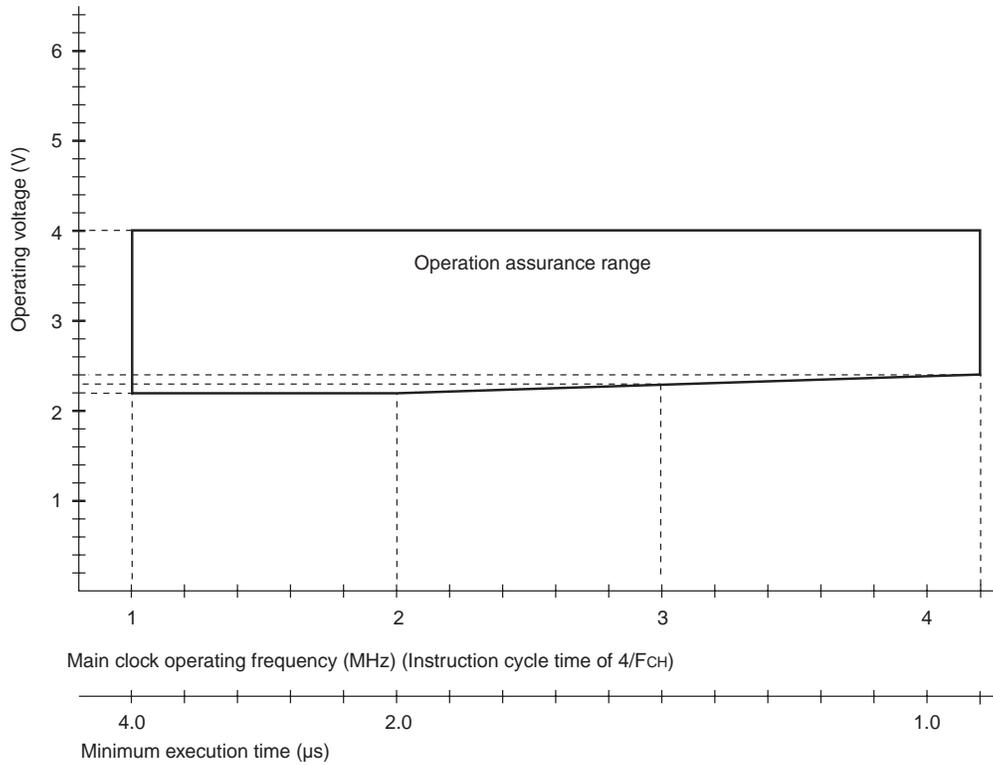
MB89P131/P133A/P135A/PV130A, and single-clock MB89121/123A/125A
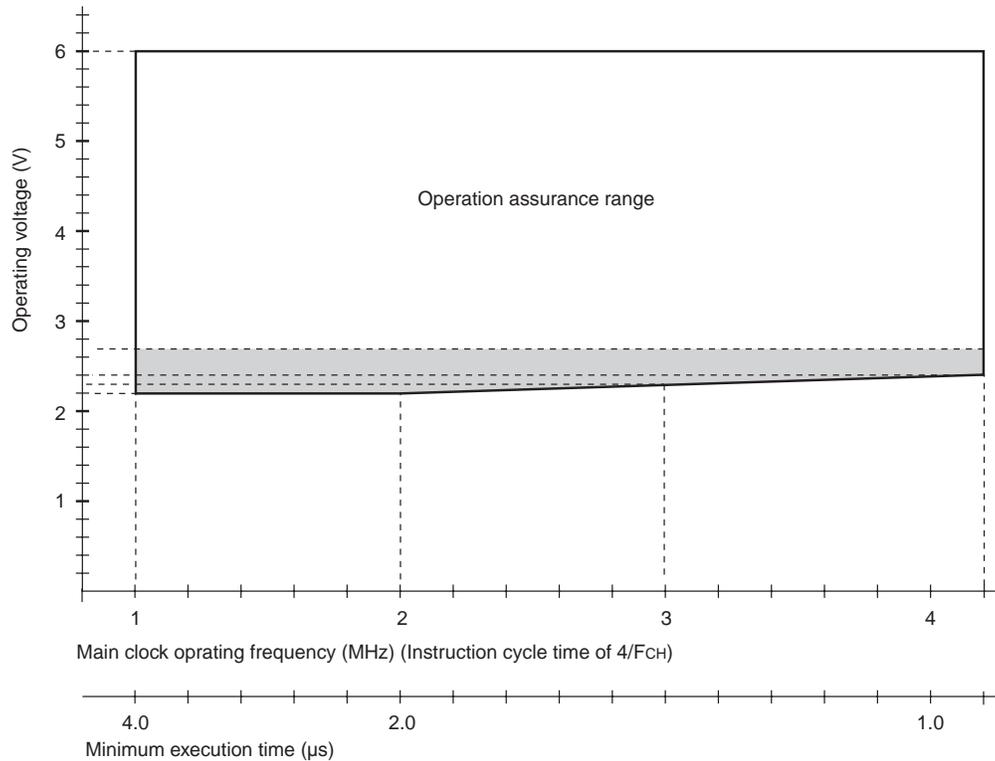
Note : The shaded area is assured only for the MB89121/123A/125A (instruction cycle time of 4/F$_{CH}$) .

3. DC Characteristics

$(AV_{CC} = V_{CC} = +5.0\ V,\ AV_{SS} = V_{SS} = 0.0\ V,\ T_A = -40\ °C\ to\ +85\ °C)$

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level input voltage	V_{IH}	P00 to P07, P10 to P17	—	$0.7\ V_{CC}$	—	$V_{CC} + 0.3$	V	
	V_{IHS}	$\overline{RST}$, P30 to P37, $\overline{INT20}$ to $\overline{INT27}$	—	$0.8\ V_{CC}$	—	$V_{CC} + 0.3$	V	$\overline{INT20}$ to $\overline{INT27}$ are available only for the MB89120A series.
"L" level input voltage	V_{IL}	P00 to P07, P10 to P17	—	$V_{SS} - 0.3$	—	$0.3\ V_{CC}$	V	
	V_{ILS}	$\overline{RST}$, P30 to P37, $\overline{INT20}$ to $\overline{INT27}$	—	$V_{SS} - 0.3$	—	$0.2\ V_{CC}$	V	$\overline{INT20}$ to $\overline{INT27}$ are available only for the MB89120A series.
Open-drain output pin applied voltage	V_D	P40 to P43	—	$V_{SS} - 0.3$	—	$V_{CC} + 0.3$	V	
"H" level output voltage	V_{OH}	P00 to P07, P10 to P17, P20 to P27, P30 to P37	$I_{OH} = -2.0\ mA$	2.4	—	—	V	
"L" level output voltage	V_{OL}	P00 to P07, P10 to P17 P20 to P27, P30 to P37, P40 to P43	$I_{OL} = 1.8\ mA$	—	—	0.4	V	
	V_{OL2}	$\overline{RST}$	$I_{OL} = 4.0\ mA$	—	—	0.6	V	
Input leakage current (Hi-Z output leakage current)	I_{LI}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P43, MOD0, MOD1	$0.45\ V < V_I < V_{CC}$	—	—	±5	µA	Without pull-up resistor
Pull-up resistance	R_{PULL}	P00 to P07, P10 to P17, P30 to P37, P40 to P43, $\overline{RST}$	$V_I = 0.0\ V$	25	50	100	kΩ	

(Continued)

(Continued)

$(AV_{CC} = V_{CC} = +5.0 \text{ V}, AV_{SS} = V_{SS} = 0.0 \text{ V}, T_A = -40 \text{ °C to } +85 \text{ °C})$

Parameter	Symbol	Pin	Condition	Value Min.	Value Typ.	Value Max.	Unit	Remarks
Power supply current[*1]	I_{CC1}	V_{CC} (External clock operation)	$V_{CC} = 5.0$ V, $F_{CH} = 4.00$ MHz, t_{inst}[*2] = 1.0 μs	—	4	7	mA	MB89121/123A/125A
				—	6	10	mA	MB89P131/P133A/P135A
	I_{CCS1}		$V_{CC} = 5.0$ V, $F_{CH} = 4.00$ MHz, Main sleep mode, t_{inst}[*2] = 1.0 μs	—	2	5	mA	
	I_{CCL}		$V_{CC} = 3.0$ V, $F_{CL} = 32.768$ kHz, Sub clock mode	—	50	100	μA	MB89121/123A/125A
				—	1	3	mA	MB89P131/P133A/P135A
	I_{CCLS}		$V_{CC} = 3.0$ V, $F_{CL} = 32.768$ kHz, Sub clock sleep mode	—	25	50	μA	
	I_{CCT}		$V_{CC} = 3.0$ V, $F_{CL} = 32.768$ kHz • Watch mode • Main clock stop mode at dual clock product	—	—	15	μA	
	I_{CCH}		$T_A = +25$ °C • Sub clock stop mode • Main clock stop mode at single clock product	—	—	1	μA	
Input capacitance	C_{IN}	Other than AV_{CC}, AV_{SS}, V_{CC}, and V_{SS}	$f = 1$ MHz	—	10	—	pF	

*1 : The measurement conditions of power supply current is external clock. ($V_{CC} = 5.0$ V, $V_{CC} = 3.0$ V)

*2 : For information on t_{inst}, see " (4) Instruction Cycle" in "4. AC Characteristics."

4. AC Characteristics

(1) Reset Timing

(V$_{CC}$ = +5.0 V ±10%, AV$_{SS}$ = V$_{SS}$ = 0.0 V, T$_A$ = −40 °C to +85 °C)

Parameter	Symbol	Condition	Value Min.	Value Max.	Unit	Remarks
$\overline{RST}$ "L" pulse width	t$_{ZLZH}$	—	48 t$_{HCYL}$*	—	ns	

* : t$_{HCYL}$ is the oscillation cycle (1/F$_{CH}$) input to the X0.
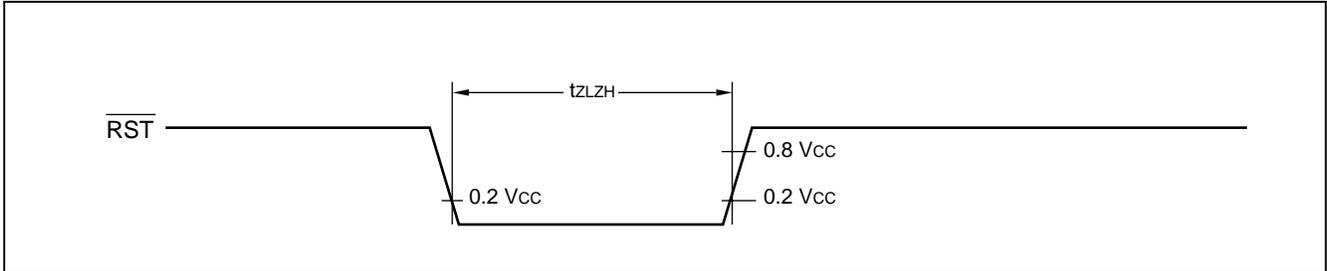
(2) Power-on Reset

(AV$_{SS}$ = V$_{SS}$ = 0.0 V, T$_A$ = −40 °C to +85 °C)

Parameter	Symbol	Condition	Value Min.	Value Max.	Unit	Remarks
Power supply rising time	t$_R$	—	—	50	ms	Power-on reset function only
Power supply cut-off time	t$_{OFF}$		1	—	ms	Due to repeated operations

Note : Make sure that power supply rises within the oscillation stabilization time selected.
For example, when the main clock is operating at F$_{CH}$ = 3 MHz and the oscillation stabilization time select option has been set to 2^{12}/F$_{CH}$, the oscillation stabilization wait time is 1.4 ms and accordingly the maximum value of power supply rising time is about 1.4 ms.
Keep in mind that rapid changes in power supply voltage may cause a power-on reset. If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.
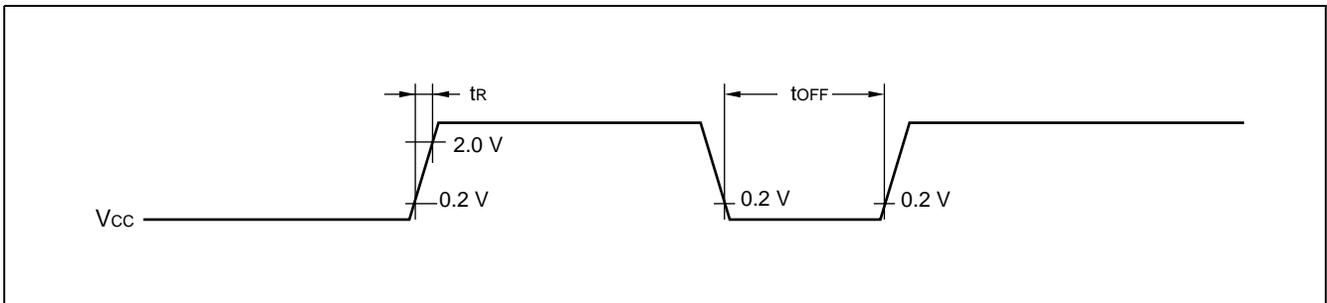
(3) Clock Timings

$(V_{SS} = 0.0\ V, T_A = -40\ °C\ to\ +85\ °C)$

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min.	Typ.	Max.		
Clock frequency	F_{CH}	X0, X1	1	—	4.2	MHz	Main clock
	F_{CL}	X0A, X1A	—	32.768	—	kHz	Sub clock
Clock cycle time	t_{HCYL}	X0, X1	238	—	1000	ns	Main clock
	t_{LCYL}	X0A, X1A	—	30.5	—	µs	Sub clock
Input clock pulse width	P_{WH1} P_{WL1}	X0	72	—	—	ns	External clock
Input clock rising/falling time	t_{CR1} t_{CF1}	X0	—	—	24	ns	External clock

X0, X1 Timings and Conditions of Applied Voltage
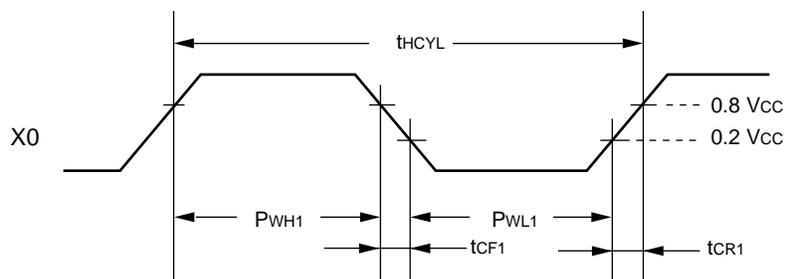
Main Clock Conditions of Applied Voltage

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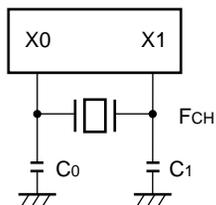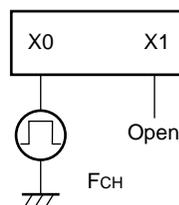
X0A, X1A Timings and Conditions of Applied Voltage
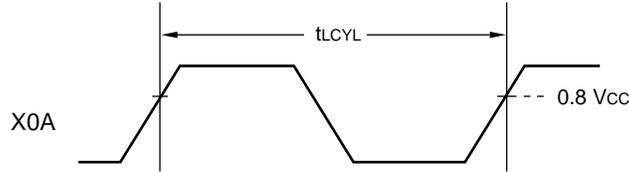
Sub clock Conditions of Applied Voltage
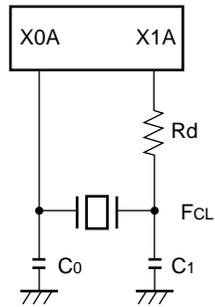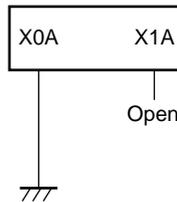
(4) Instruction Cycles

$(V_{SS} = 0.0\ V, T_A = -40\ °C\ to\ +85\ °C)$

Parameter	Symbol	Value (typical)	Unit	Remarks
Instruction cycle (minimum execution time)	t_{inst}	$4/F_{CH}$, $8/F_{CH}$, $16/F_{CH}$, $64/F_{CH}$	μs	$(4/F_{CH})\ t_{inst} = 1.0\ μs$ when operating at $F_{CH} = 4$ MHz
		$2/F_{CL}$	μs	$t_{inst} = 61.036\ μs$ when operating at $F_{CL} = 32.768$ kHz

(5) Serial I/O Timings

(V_{CC} = +5.0 V ±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

Parameter	Symbol	Pin	Condition	Value Min.	Value Max.	Unit	Remarks
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation	2 t_{inst}*	—	µs	
SCK ↓ → SO time	t_{SLOV}	SCK, SO	Internal clock operation	−200	200	ns	
Valid SI → SCK ↑	t_{IVSH}	SI, SCK	Internal clock operation	200	—	ns	
SCK ↑ → Valid SI hold time	t_{SHIX}	SCK, SI	Internal clock operation	200	—	ns	
Serial clock "H" pulse width	t_{SHSL}	SCK	External clock operation	t_{inst}*	—	µs	
Serial clock "L" pulse width	t_{SLSH}	SCK	External clock operation	t_{inst}*	—	µs	
SCK ↓ → SO time	t_{SLOV}	SCK, SO	External clock operation	0	200	ns	
Valid SI → SCK ↑	t_{IVSH}	SI, SCK	External clock operation	200	—	ns	
SCK ↑ → Valid SI hold time	t_{SHIX}	SCK, SI	External clock operation	200	—	ns	

* : For information on t_{inst}, see " (4) Instruction Cycles."

Internal Shift Clock Mode

External Shift Clock Mode

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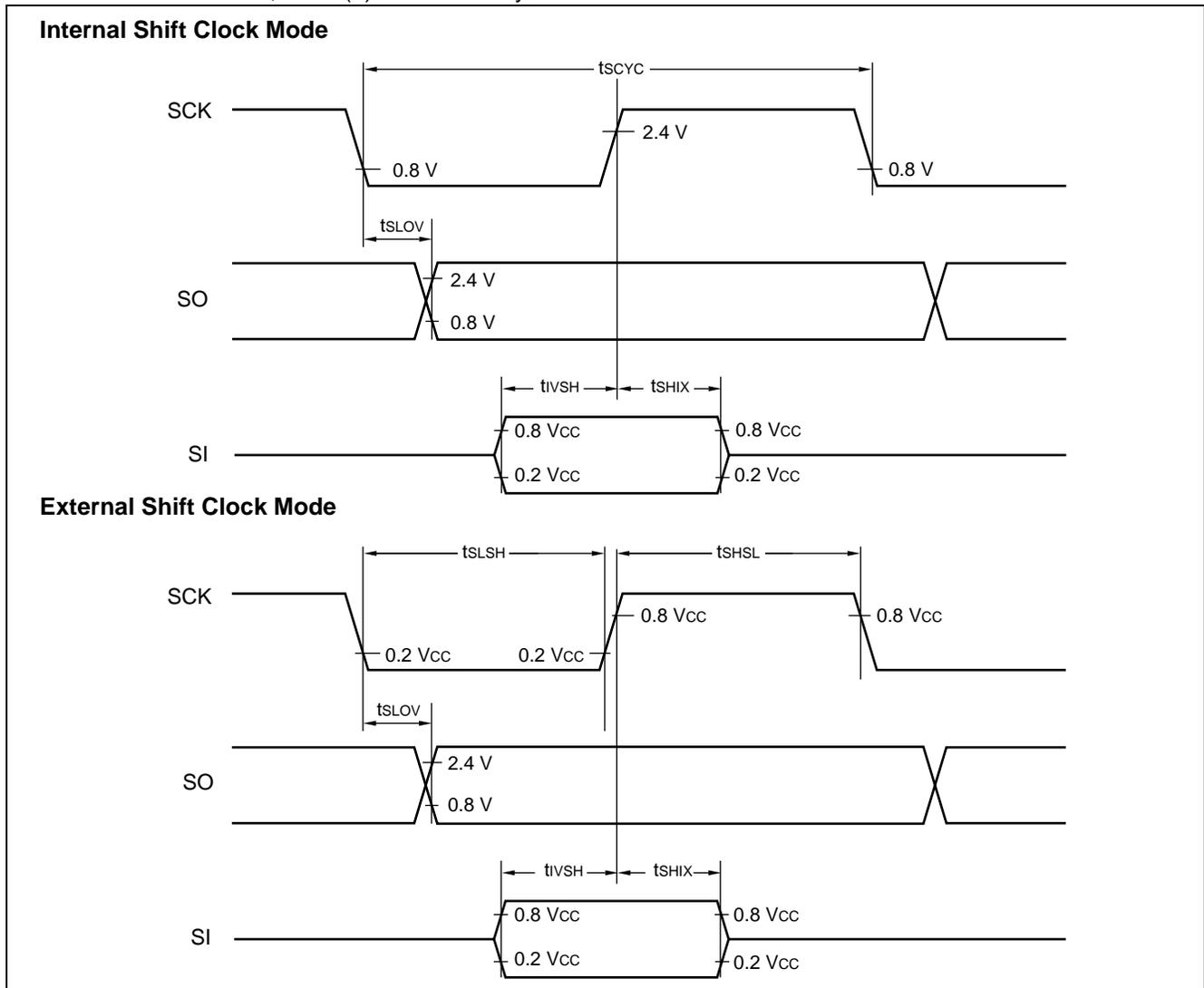
(6) Peripheral Input Timings

(V$_{CC}$ = +5.0 V ±10%, AV$_{SS}$ = V$_{SS}$ = 0.0 V, T$_A$ = −40 °C to +85 °C)

Parameter	Symbol	Pin	Value		Unit	Remarks
			Min.	Max.		
Peripheral input "H" pulse width	t$_{ILIH}$	EC, INT0 to INT2	2 t$_{inst}$*	—	µs	
Peripheral input "L" pulse width	t$_{IHIL}$		2 t$_{inst}$*	—	µs	

* : For information on t$_{inst}$, see " (4) Instruction Cycle."
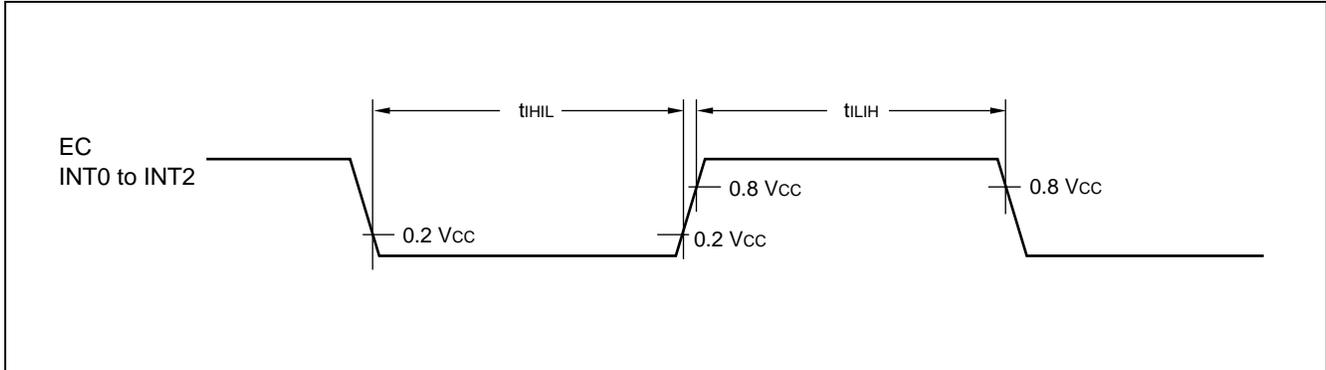
■ EXAMPLE CHARACTERISTICS

(1) "L" Level Output Voltage

V_{OL} vs. I_{OL}

V_{OL} (V)

$T_A = +25\ °C$
$V_{CC} = 2.5$ V
$V_{CC} = 2.2$ V
$V_{CC} = 3.0$ V
$V_{CC} = 4.0$ V
$V_{CC} = 5.0$ V
$V_{CC} = 6.0$ V

1.1
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0

0 1 2 3 4 5 6 7 8 9 10
I_{OL} (mA)

(2) "H" Level Output Voltage

$V_{CC} - V_{OH}$ vs. I_{OH}

$V_{CC} - V_{OH}$ (V)

$T_A = +25\ °C$
$V_{CC} = 2.5$ V
$V_{CC} = 2.2$ V
$V_{CC} = 3.0$ V
$V_{CC} = 4.0$ V
$V_{CC} = 5.0$ V
$V_{CC} = 6.0$ V

1.1
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0

0.0 −.5 −1.0 −1.5 −2.0 −2.5 −3.0
I_{OH} (mA)
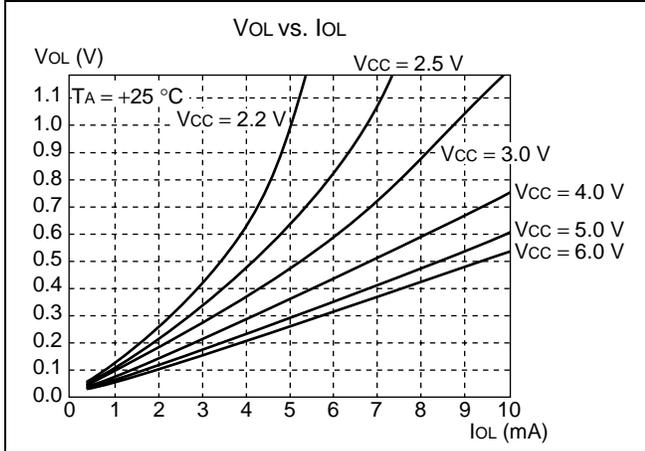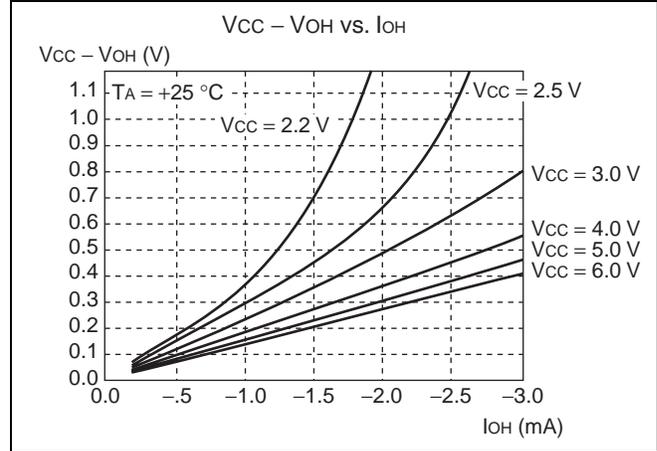
(3) "H" Level Input Voltage/"L" Level Input Voltage (CMOS Input)

V_{IN} vs. V_{CC}

V_{IN} (V)

$T_A = +25\ °C$

5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0

.00 1.00 2.00 3.00 4.00 5.00 6.00 7.00
V_{CC} (V)
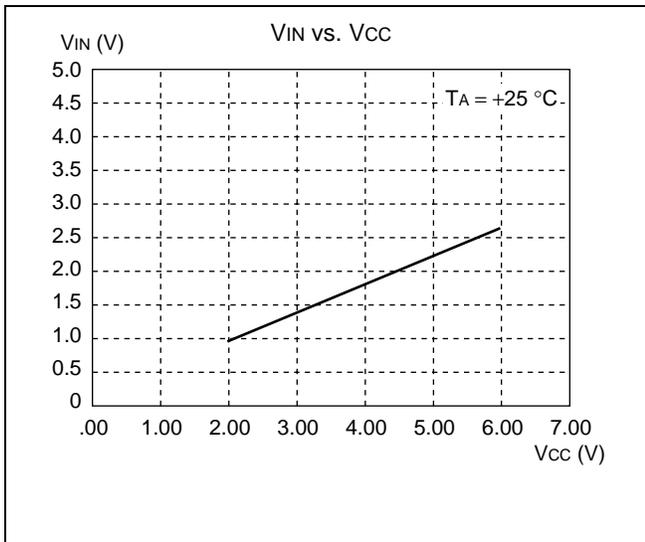
(4) "H" Level Input Voltage/"L" Level Input Voltage (Hysteresis Input)

V_{IN} vs. V_{CC}

V_{IN} (V)

$T_A = +25\ °C$
V_{IHS}
V_{ILS}

5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0

.00 1.00 2.00 3.00 4.00 5.00 6.00 7.00
V_{CC} (V)

V_{IHS} : Threshold when input voltage in hysteresis characteristics is set to "H" level

V_{ILS} : Threshold when input voltage in hysteresis characteristics is set to "L" level

(5) Pull-up Resistance

R_{PULL} vs. V_{CC}

R_{PULL} (kΩ)

$T_A = +25\ °C$

1000

300

100

50

10

0 1 2 3 4 5 6 7
V_{CC} (V)

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(6) Power Supply Current

ICC1 vs. VCC

ICC (mA)

FCH = 4.0 MHz
TA = +25 °C

Divide by 4 (ICC1)

Divide by 64

VCC (V)

ICCS1 vs. VCC

ICCS (mA)

FCH = 4.0 MHz
TA = +25 °C

Divide by 4 (ICCS1)

Divide by 64

VCC (V)

ICCL vs. VCC

ICCL (µA)

TA = +25 °C

VCC (V)

ICCLS vs. VCC

ICCLS (µA)

TA = +25 °C

VCC (V)

ICCT vs. VCC

ICCT (µA)

TA = +25 °C

VCC (V)

ICCH vs. VCC

ICCH (µA)

TA = +25 °C

VCC (V)

■ MASK OPTIONS

No.	Part number	MB89121 MB89123A MB89125A	MB89P131 MB89P133A	MB89P135A	MB89PV130A
	Specifying procedure	Specify when ordering masking		Set with EPROM programmer	Specification impossible
1	Pull-up resistors • P00 to P07, P10 to P17, • P30 to P37, P40 to P43	Selectable by pin	Selectable by pin (P40 to P43 must be set without a pull-up resistor.)		All pins fixed to no pull-up resistor optional
2	Power-on reset Power-on reset provided No power-on reset	Selectable	Selectable	Selectable	With power-on reset
3	Selection of oscillation stabilization wait time • The oscillation stabilization wait time initial value is selectable from 4 types given below. 0 : Oscillation stabilization $2^2/F_{CH}$ 1 : Oscillation stabilization $2^{12}/F_{CH}$ 2 : Oscillation stabilization $2^{16}/F_{CH}$ 3 : Oscillation stabilization $2^{18}/F_{CH}$	Selectable	Selectable	Selectable	Oscillation stabilization $2^{18}/F_{CH}$
4	Reset pin output • Reset output provided • No reset output	Selectable	Selectable	Selectable	With reset output
5	Clock mode selection • Single-clock mode • Dual-clock mode	Selectable	Selectable	Selectable	Dual-clock mode
6	Main clock oscillation circuit type • External clock input • Oscillation resonator	Selectable	Not required*1		
7	Peripheral control clock output function*2 • Not used • Used	Selectable	Not required*3		

*1 : Can be used as either crystal or ceramics oscillation.

*2 : "Used" must be selected when P33 (39 pin) is used as SCO for the peripheral control clock output.

*3 : The peripheral control clock function can be used only by software.

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■ MB89P131/P133A STANDARD OPTIONS

No.	Product option	MB89P131-101	MB89P133A-201
1	Pull-up resistor	Not provided for any port	Not provided for any port
2	Power-on reset	Provided	Provided
3	Selection of oscillation stabilization time	2 : Oscillation stabilization $2^{16}/F_{CH}$	2 : Oscillation stabilization $2^{16}/F_{CH}$
4	Reset pin output	Provided	Provided
5	Clock mode selection	Dual-clock mode	Dual-clock mode

■ ORDERING INFORMATION

Part number	Package	Remarks
MB89121PFM MB89123APFM MB89125APFM	48-pin Plastic QFP (FPT-48P-M13)	
MB89P131-101PFM MB89P133A-201PFM MB89P135A-101PFM		
MB89PV130ACF-ES	48-pin Ceramic MQFP (MQP-48C-P01)	

■ PACKAGE DIMENSION
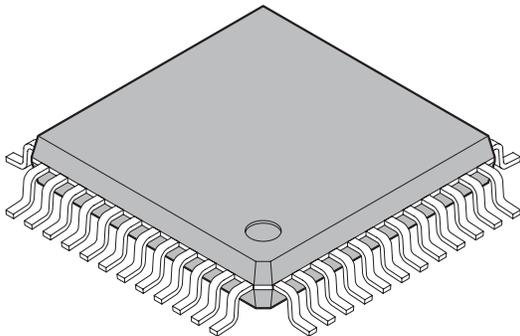
Lead pitch	0.80 mm
Package width × package length	10 × 10 mm
Lead shape	Gullwing
Sealing method	Plastic mold
Mounting height	2.35 mm MAX
Code (Reference)	P-QFP44-10×10-0.80

48-pin plastic QFP

(FPT-48P-M13)

48-pin plastic QFP
(FPT-48P-M13)

Note 1) ∗ : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.

13.10±0.40(.516±.016)SQ

∗10.00±0.20(.394±.008)SQ

0.17±0.06
(.007±.002)

0.10(.004)

INDEX

0.80(.031)

0.32±0.05
(.013±.002)

0.20(.008) Ⓜ

Details of "A" part

1.95 $^{+0.40}_{-0.20}$ (Mounting height)
(.077 $^{+.016}_{-.008}$)

0.25(.010)

0~8°

0.80±0.20
(.031±.008)

0.88±0.15
(.035±.006)

0.20 $^{+0.10}_{-0.20}$
(.008 $^{+.004}_{-.008}$)
(Stand off)

"A"
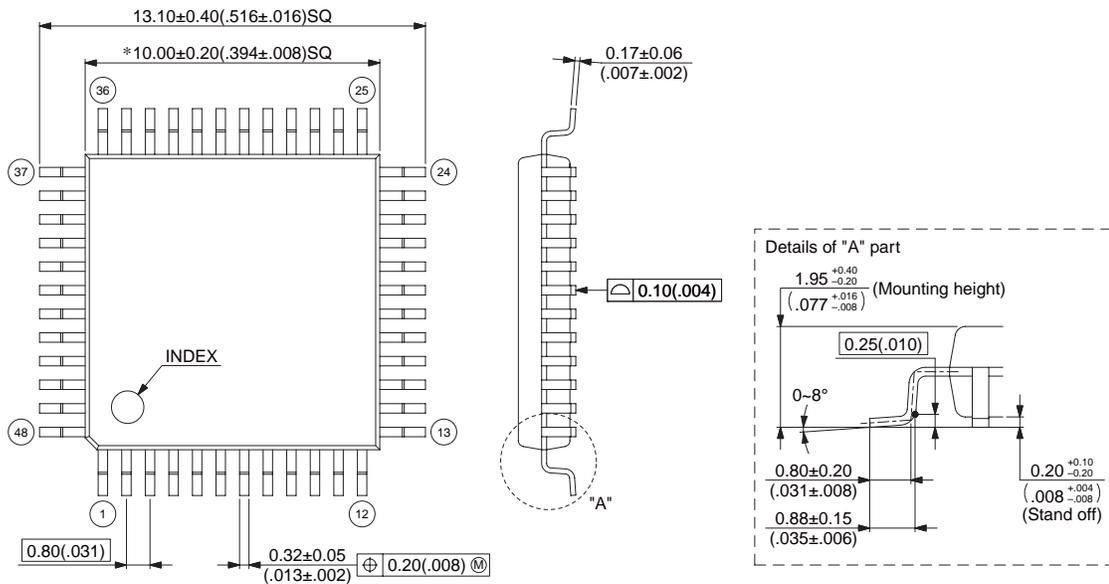
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Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimensions at the following URL.
http://edevice.fujitsu.com/package/en-search/

■ MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
7	■ PIN DESCRIPTION	Changed the function description of AVCC pin (pin no. 1). Power supply(GND) pin → Power supply pin
15	■ HANDLING MB89P131/P133A/ P135A	Deleted the item of "3. EPROM Programmer Socket Adapter".
16	■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE	Deleted the item of "2. Programming Socket Adapter".
31	■ ELECTRICAL CARACTERISTICS 4. AC Characteristics	Deleted the item of "(5) Recommended Resonator Manufacturers".
37	■ ORDERING INFORMATION	Changed the ordering information. MB89P131PFM-101 → MB89P131-101PFM MB89P133APFM-201 → MB89P133A-201PFM MB89P135APFM → MB89P135A-101PFM

The vertical lines marked in the left side of the page show the changes.

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