FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-29137-3E

Spread Spectrum Clock Generator

MB88163

■ DESCRIPTION

MB88163 is a clock generator for EMI (Electro Magnetic Interference) reduction. The peak of unnecessary radiation noise (EMI) can be attenuated by making the oscillation frequency slightly modulate periodically with the internal modulator.

■ FEATURES

- Package : SON8 (2.0 mm × 2.0 mm)
- Low current consumption : 3.6 mW@13 MHz (Typ-sample, no load)
- Power supply voltage : 1.8 V ± 0.15 V
- Modulation rate : Selectable from no modulation (0.0%), ± 0.25%, ± 0.5% and ± 1.0%
- Modulation clock output Duty : 40% to 60%
- Operating temperature : − 40 °C to + 85 °C

■ PRODUCT LINEUP

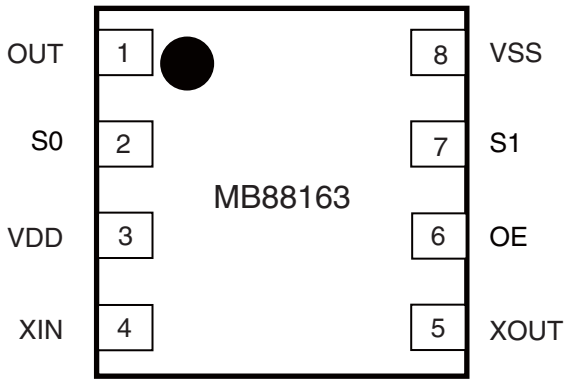
The MB88163 has the following two kinds of line-ups depending on the difference of the input frequency range.

Part number	Input frequency	Multiplication rate	Output frequency
MB881631B	12.5 MHz to 26 MHz	Multiplied by 1	12.5 MHz to 26 MHz
MB881631C	20 MHz to 42 MHz	Multiplied by 1	20 MHz to 42 MHz

2011.5

■ PIN ASSIGNMENT

(TOP VIEW)



(LCC-8P-M03)

■ PIN DESCRIPTION

Pin name	I/O	Pin no.	Description
OUT	O	1	Modulation clock output pin
S0	I	2	Modulation rate setting pin with pull-down resistance (18 kΩ)
VDD	—	3	Power supply voltage pin
XIN	I	4	Pin for connection to crystal oscillator / clock input pin
XOUT	O	5	Pin for connection to crystal oscillator
OE	I	6	Clock output enable pin with pull-up resistance (18 kΩ)
S1	I	7	Modulation rate setting pin with pull-up resistance (18 kΩ)
VSS	—	8	GND pin

■ PIN SETTING

- S0, S1 : Modulation rate setting

S1	S0	Modulation rate
L	L	No modulation (0.0%)
L	H	± 0.25%
H	L	± 0.5%
H	H	± 1.0%

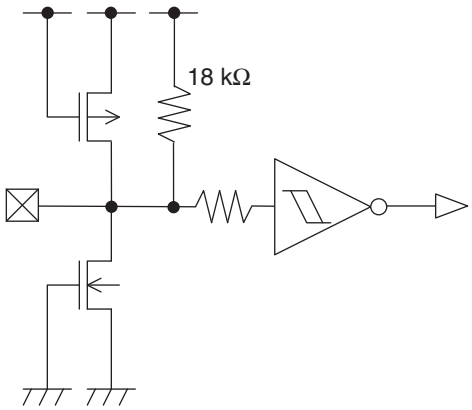
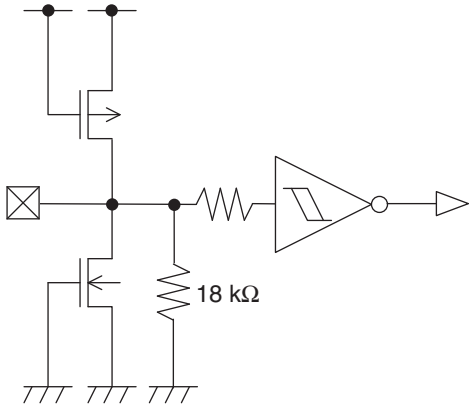
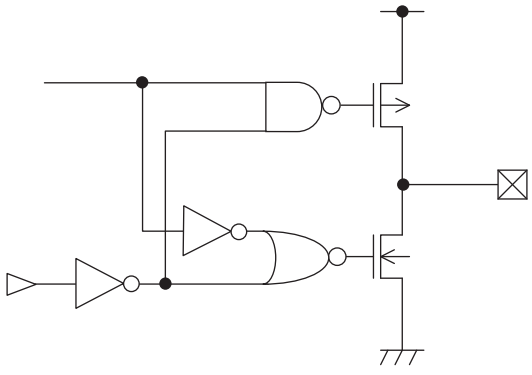
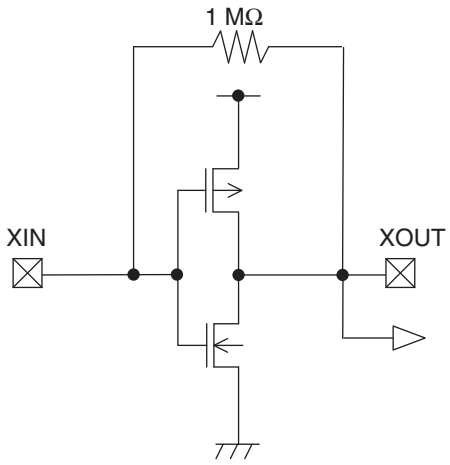
After turning the power on or when changing the S0 pin and the S1 pin setting, the stabilization wait time of the modulation clock is required.
The stabilization wait time of the modulation clock takes the maximum value of Lock-Up time in " ■ ELECTRICAL CHARACTERISTICS".

- OE : Clock output enable setting

OE	Condition
L	OUT pin : Hi-Z
H	Operating

When setting the OE pin to "L", the internal circuit is operating and only the output stops operating. When changing the OE pin from "L" to "H", the desired clock is obtained after T_{ZO} in "■ ELECTRICAL CHARACTERISTICS" Output start time after OE entry passes.

■ I/O CIRCUIT TYPE

Pin	Circuit type	Remarks
S1, OE		• With pull-up resistor (18 kΩ) • CMOS hysteresis input
S0		• With pull-down resistor (18 kΩ) • CMOS hysteresis input
OUT		• CMOS output • I_{OL} = 2 mA • Hi-Z output at OE= “L”
XIN, XOUT		• Oscillation circuit • Built-in feedback resistance : 1 MΩ (Typ)

■ HANDLING DEVICES

(1) Preventing Latch-up

A latch-up can occur if, on this device, (a) a voltage higher than power supply voltage or a voltage lower than GND is applied to an input or output pin or (b) a voltage higher than the rating is applied between power supply pin and GND pin. The latch-up, if it occurs, significantly increases the power supply current and may cause thermal destruction of an element. When you use this device, be very careful not to exceed the maximum rating.

(2) Handling unused pins

Do not leave an unused input pin open, since it may cause a malfunction. Handle by, using a pull-up or pull-down resistor.

(3) The attention when the external clock is used

Input the clock to XIN pin, and XOUT pin should be opened when you use the external clock.

Please pay attention so that an overshoot and an undershoot do not occur to an input clock of XIN pin.

(4) Power supply pins

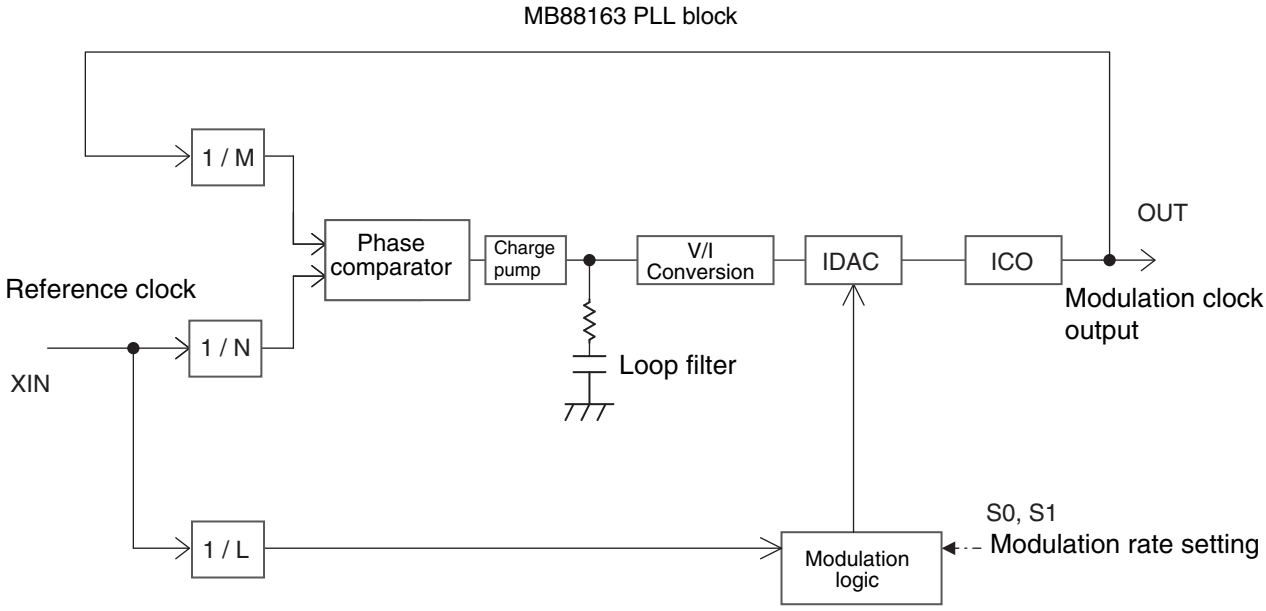
Please design connecting the power supply pin of this device by as low impedance as possible from the current supply source.

We recommend connecting electrolytic capacitor (about 10 μF) and the ceramic capacitor (about 0.01 μF) in parallel between power supply and GND near the device, as a bypass capacitor.

(5) Crystal oscillator circuit

Noise near the XIN and XOUT pins may cause the device to malfunction. Design printed circuit boards so that electric wiring of XIN or XOUT pin and resonator (or ceramic oscillator) do not intersect other wiring. Design the printed circuit board that surrounds the XIN and XOUT pins with ground.

■ BLOCK DIAGRAM



A glitch-less IDAC (current output D/A converter) provides precise modulation, thereby dramatically reducing EMI.

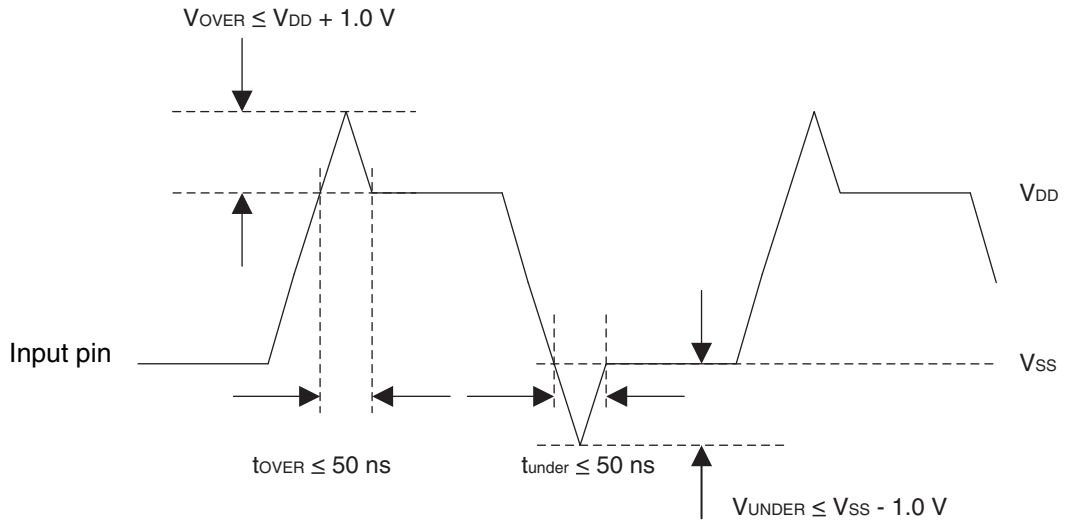
■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage*	V_{DD}	– 0.5	+ 2.5	V
Input voltage*	V_I	V_{SS} – 0.5	V_{DD} + 0.5	V
Output voltage*	V_O	V_{SS} – 0.5	V_{DD} + 0.5	V
Storage temperature	T_{ST}	– 55	+ 125	°C
Operation junction temperature	T_J	– 40	+ 125	°C
Output current	I_O	– 13	+ 13	mA
Overshoot	V_{OVER}	—	V_{DD} + 1.0 ($t_{OVER} \leq$ 50 ns)	V
Undershoot	V_{UNDER}	V_{SS} – 1.0 ($t_{UNDER} \leq$ 50 ns)	—	V

* : These parameters are based on the condition that V_{SS} = 0.0 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

Overshoot / Undershoot



■ RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0.0 V)

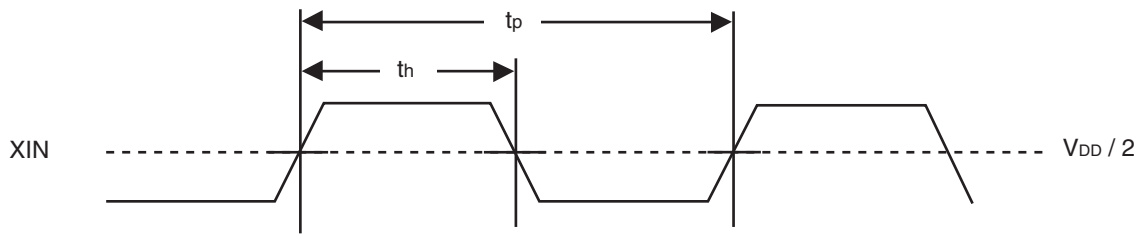
Parameter	Symbol	Pin	Condi-tions	Value			Unit
				Min	Typ	Max	
Power supply voltage	V_{DD}	VDD	—	1.65	1.8	1.95	V
"H" level input voltage	V_{IH}	S0, S1, OE, XIN	—	$V_{DD} \times 0.8$	—	$V_{DD} + 0.3$	V
"L" level input voltage	V_{IL}	S0, S1, OE, XIN	—	$V_{SS} - 0.3$	—	$V_{DD} \times 0.2$	V
Input clock duty cycle	t_{DCI}	XIN		40	50	60	%
Operating temperature	T_a	—	—	− 40	—	+ 85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

Input clock duty cycle ($t_{DCI} = t_h/t_p$)



■ ELECTRICAL CHARACTERISTICS

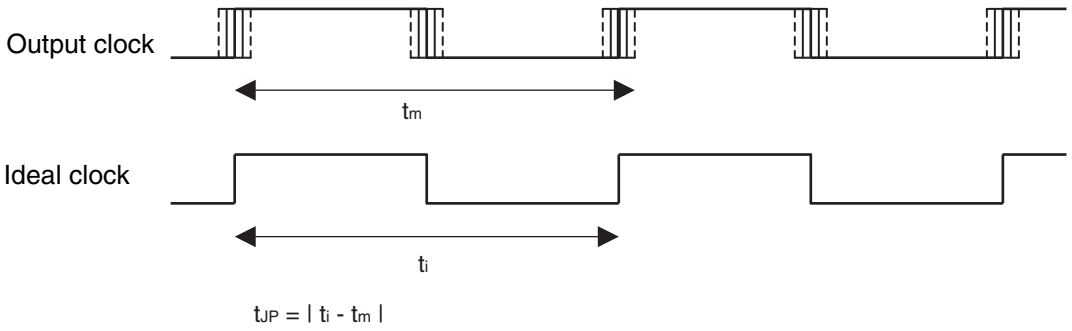
(T_a = − 40 °C to + 85 °C, V_{DD} = 1.8 V ± 0.15 V, V_{SS} = 0.0 V)

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Power supply current	I_{CC}	VDD	13 MHz output capacitance no load at external clock input	—	2.0	3.5	mA
Input frequency	f_{IN}	XIN	MB881631B	12.5	—	26	MHz
			MB881631C	20	—	42	
Output frequency	f_{OUT}	OUT	MB881631B	12.5	—	26	MHz
			MB881631C	20	—	42	
Output voltage	V_{OH}	OUT	"H" level output I_{OH} = − 2 mA	V_{DD} − 0.2	—	V_{DD}	V
	V_{OL}		"L" level output I_{OL} = 2 mA	V_{SS}	—	0.2	V
Output slew rate	SR	OUT	V_{OL}-V_{OH} C_L = 15 pF	0.4	—	3.0	V/ns
Output impedance	Z_O	OUT	—	—	30	—	Ω
Output clock duty cycle	t_{DCC}	OUT	V_{DD} / 2	40	—	60	%
Input capacitance	C_{IN}	S0, S1, OE, XIN	T_a = + 25 °C, V_{DD} = V_I = 0.0 V, f = 1 MHz	—	—	16	pF
Input pull-up resistance	R_{PU}	S1, OE	V_{OL} = 0.0 V	8	18	40	kΩ
Input pull-down resistance	R_{PD}	S0	V_{OH} = V_{DD}	8	18	40	kΩ
Load capacitance	C_L	OUT	—	—	—	15	pF
Modulation frequency (number of clocks per one modulation)	f_{MOD} (n_{MOD})	OUT	Depends on f_{IN}	f_{IN}/1232 (1232)	f_{IN}/1064 (1064)	f_{IN}/896 (896)	kHz (clks)
			f_{IN} = 13 MHz	10.5	12.2	14.5	
			f_{IN} = 26 MHz	21.1	24.4	29.0	
Lock-Up time	t_{LK}	OUT	Direct coupling	—	—	10	ms
			Capacitive coupling	—	—	40	
Output Hi-Z start time from OE exit	T_{OZ}	OUT		—	—	100	ns
Output start time after OE entry	T_{ZO}	OUT		—	—	100	ns
Cycle-Cycle jitter	t_{JC}	OUT	No load capacitance T_a = + 25 °C, V_{DD} = 1.8 V	—	—	100	ps-rms

Note: After turning the power on or when changing the S0 pin and the S1 pin setting, the stabilization wait time of the modulation clock is required. The stabilization wait time of the modulation clock takes the maximum value of Lock-Up time in "Lock-Up time" in "■ ELECTRICAL CHARACTERISTICS".

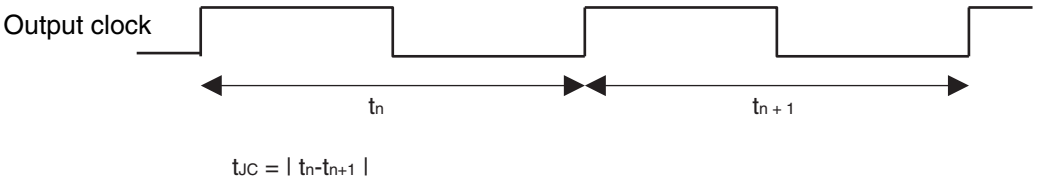
- Definition of jitter

  - Period jitter



Period jitter shows the difference between the ideal clock without jitter and the measurement clock.

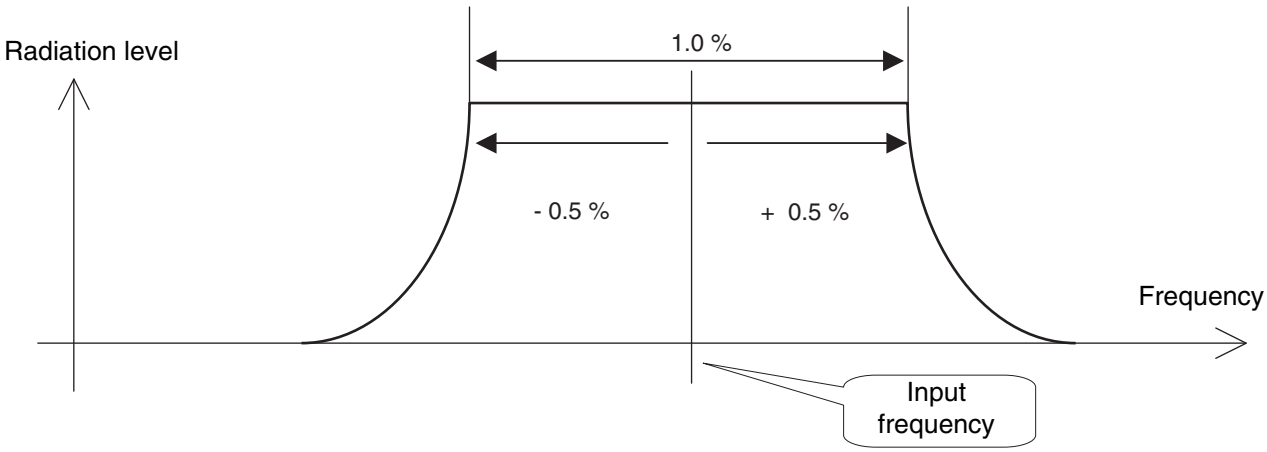
  - Cycle-cycle jitter



Cycle-cycle jitter indicates the difference between a certain cycle and the immediately succeeding (or preceding) cycle.

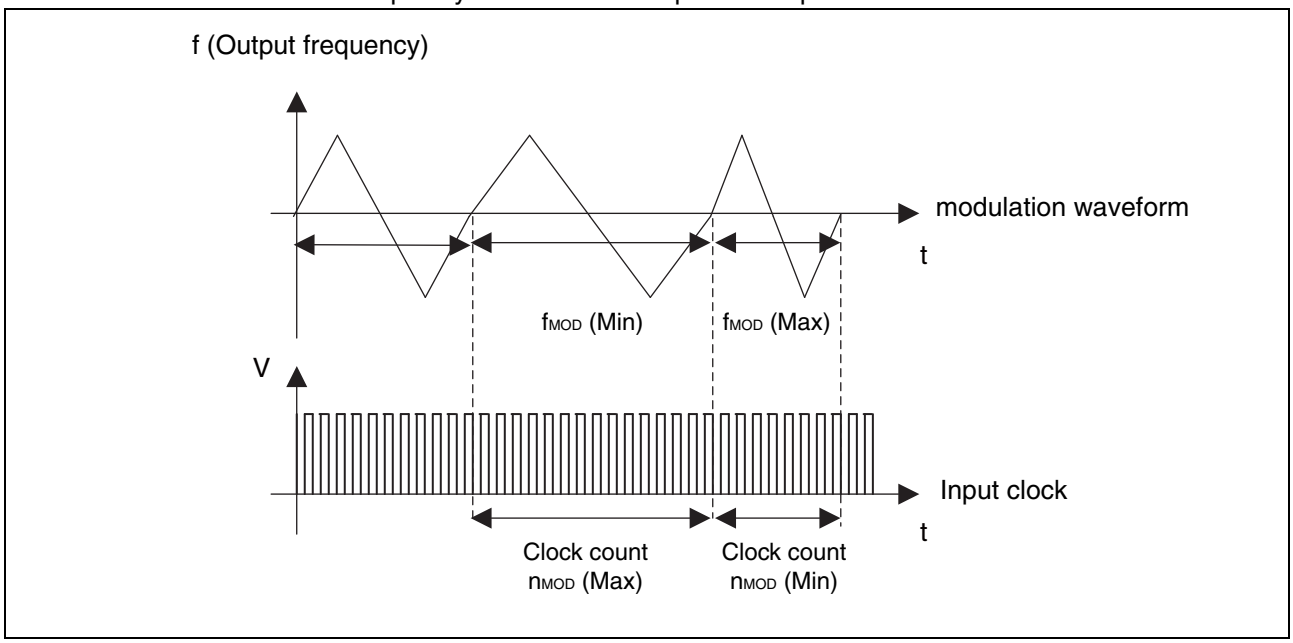
- Spectrum spread
  - Center spread

Spectrum is spread (modulated) by centering on the input frequency.



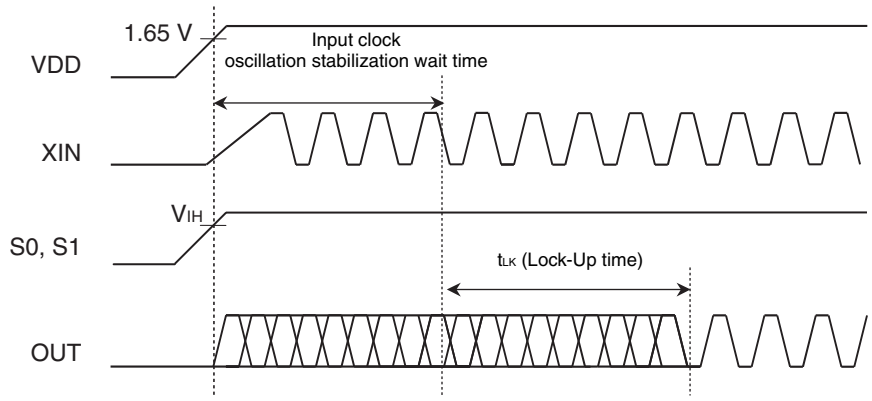
Example of center spread modulation rate ± 0.5% (1.0%)

• Definition of modulation frequency and number of input clocks per modulation

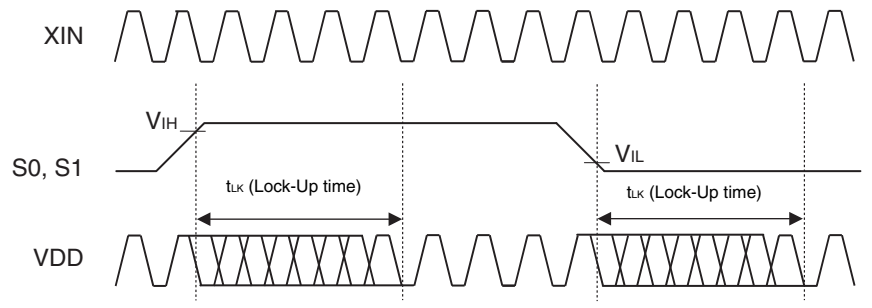


This product contains the modulation period to realize the efficient EMI reduction. The modulation period f_{MOD} depends on the input frequency and changes between f_{MOD} (Min) and f_{MOD} (Max). Furthermore, the average value of the modulation period f_{MOD} equals the typical value shown in "■ ELECTORICAL CHARACTERISTICS".

• Lock-Up time



If the setting pin is fixed at “H” level or “L” level, the maximum time after the power is turned on until the set clock is output from OUT is (the stabilization wait time of input clock to XIN pin) + (the Lock-Up time “t_{LK}”). For the input clock stabilization wait time, check the characteristics of the resonator or oscillator used.

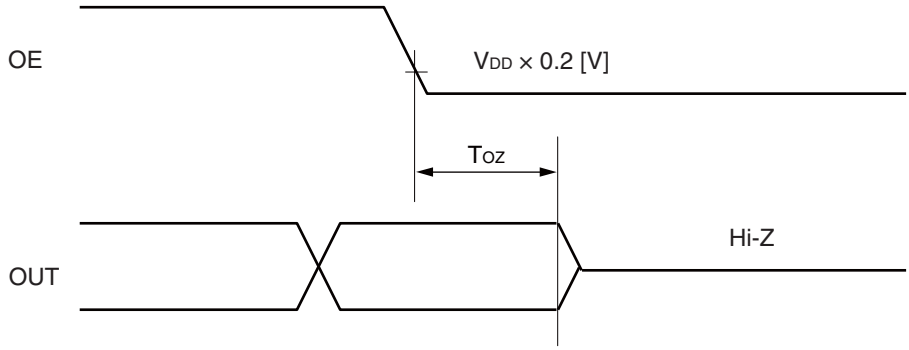


If the S0 pin and the S1 pin are used for modulation control during normal operation, the set clock is output from the OUT pin within the Lock-Up time “t_{LK}” after the level at the pin is determined.

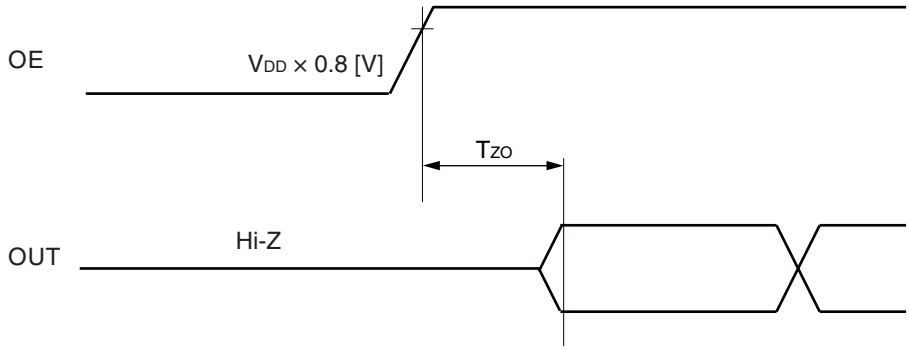
Note: The wait time for the clock signal output from the OUT pin to become stable is required after the IC is released from the S0 pin and the S1 pin are changed. During the period until the output clock signal becomes stable, the output frequency, output clock duty cycle, modulation period, and Cycle-Cycle jitter characteristic cannot be guaranteed. It is therefore advisable to perform processing such as cancelling a reset of the device at the succeeding stage after the Lock-Up time.

- Output timing at OE change

  - Output Hi-Z start time after OE exit



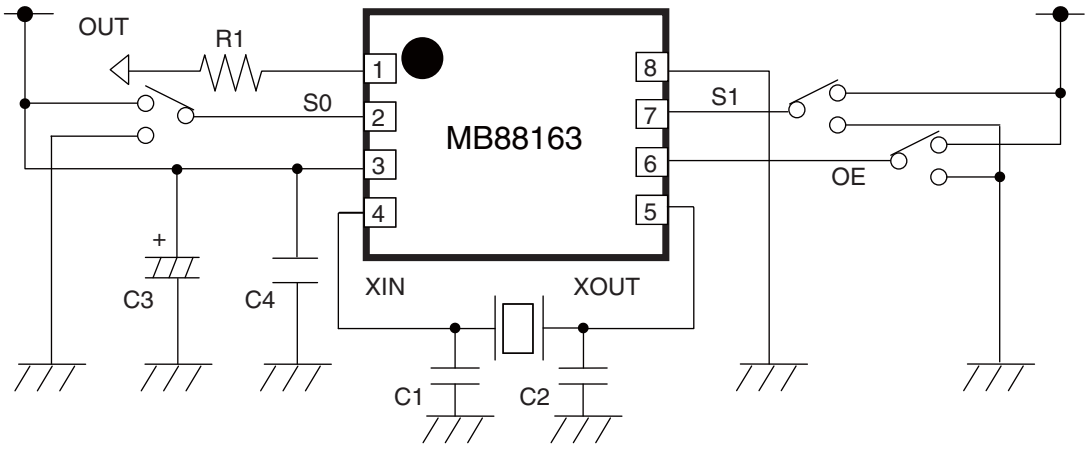
  - Output start time after OE entry



The first cycle after the OE entry does not output the correct frequency.

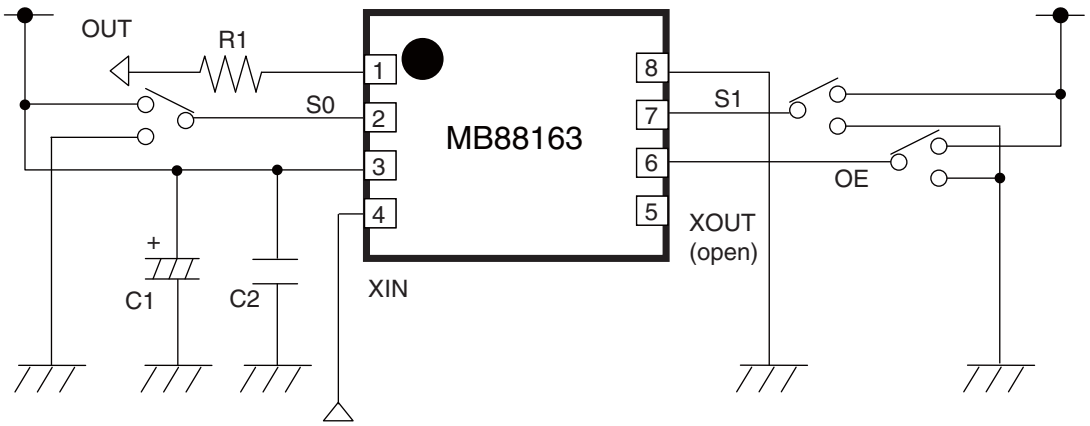
■ RECOMMENDED CIRCUIT

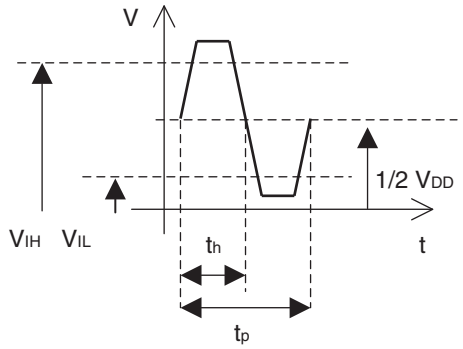
1. Crystal oscillation



C_1, C_2	: Oscillation stabilization capacitance (see "■ CRYSTAL OSCILLATION CIRCUIT".)
C_3	: Tantalized capacitor or electrolytic capacitor of 10 μF or higher
C_4	: Capacitor of about 0.01 μF (connect a capacitor of good high frequency property (ex. laminated ceramic capacitor) to close to this device)
R_1	: Impedance matching resistor for board pattern

2. External clock input (Direct coupling)

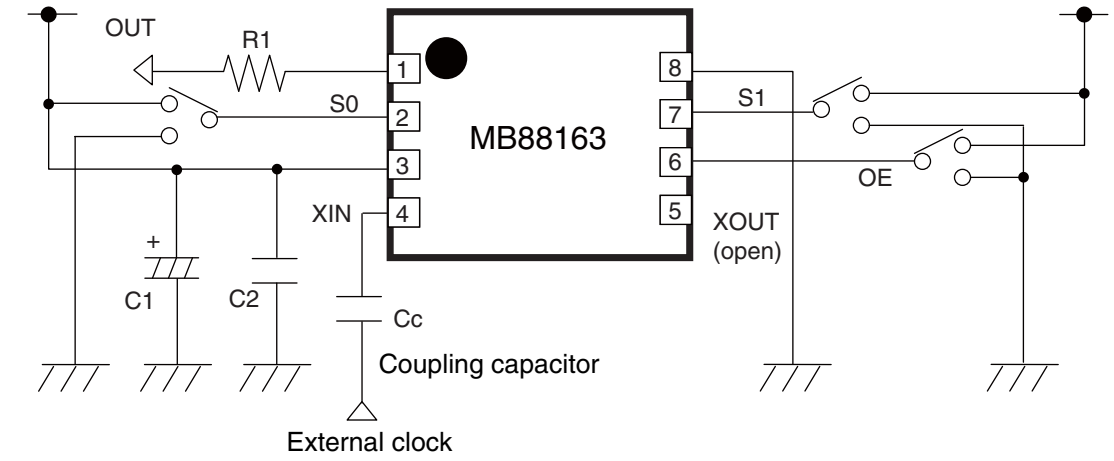


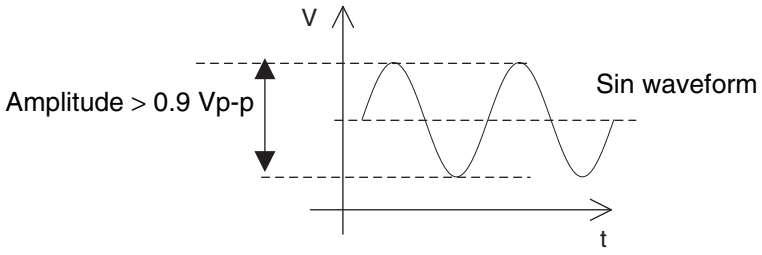


40% < Duty (T_{DCI} = t_h/t_p) < 60%

C_1	: Tantalized capacitor or electrolytic capacitor of 10 µF or higher The capacitance of 2.2 µF is available when the output impedance of the power supply source is 1Ω@10 kHz or less.
C_2	: Capacitor of about 0.01 µF (connect a capacitor of good high frequency property (ex. laminated ceramic capacitor) to close to this device)
R_1	: Impedance matching resistor for board pattern

3. External clock input (Capacitive coupling)

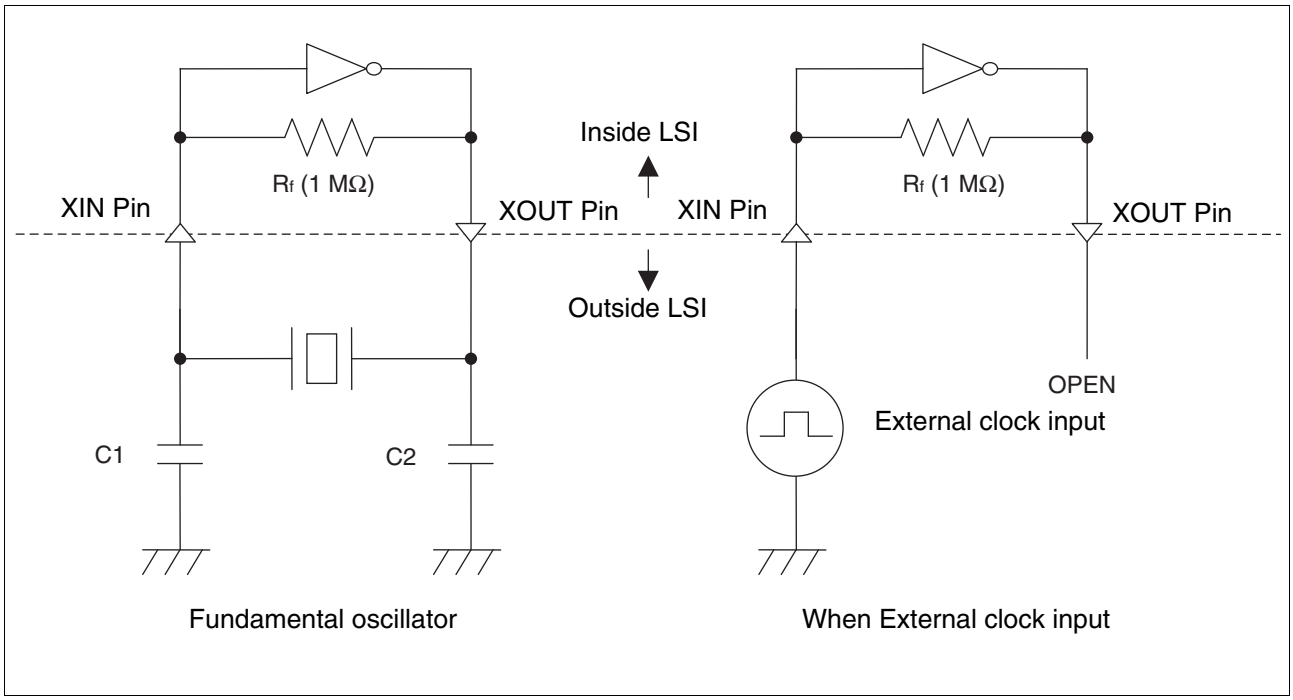




C_1	: Tantalized capacitor or electrolytic capacitor of 10 μF or higher
C_2	: Multi layer ceramic capacitor of about 0.01 μF (connect a capacitor of good high frequency property (ex. laminated ceramic capacitor) to close to this device)
C_C	: Multi layer ceramic capacitor of about 0.01 μF
R_1	: Impedance matching resistor for board pattern

■ CRYSTAL OSCILLATION CIRCUIT

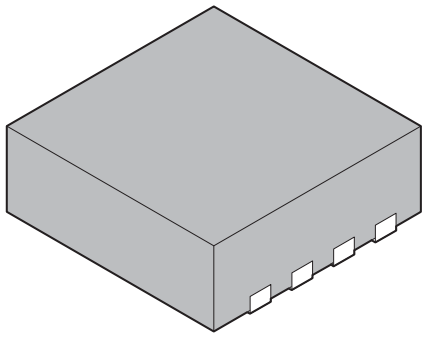
The figure below shows the connection example about general crystal oscillator. The oscillation circuit has the built-in feedback resistor (1 MΩ). It is necessary to adjust the capacity value (C1 and C2) to the most suitable value of an individual crystal oscillator. To use an external clock signal (without using the oscillator), input the clock signal to the XIN pin with the XOUT pin connected to nothing.



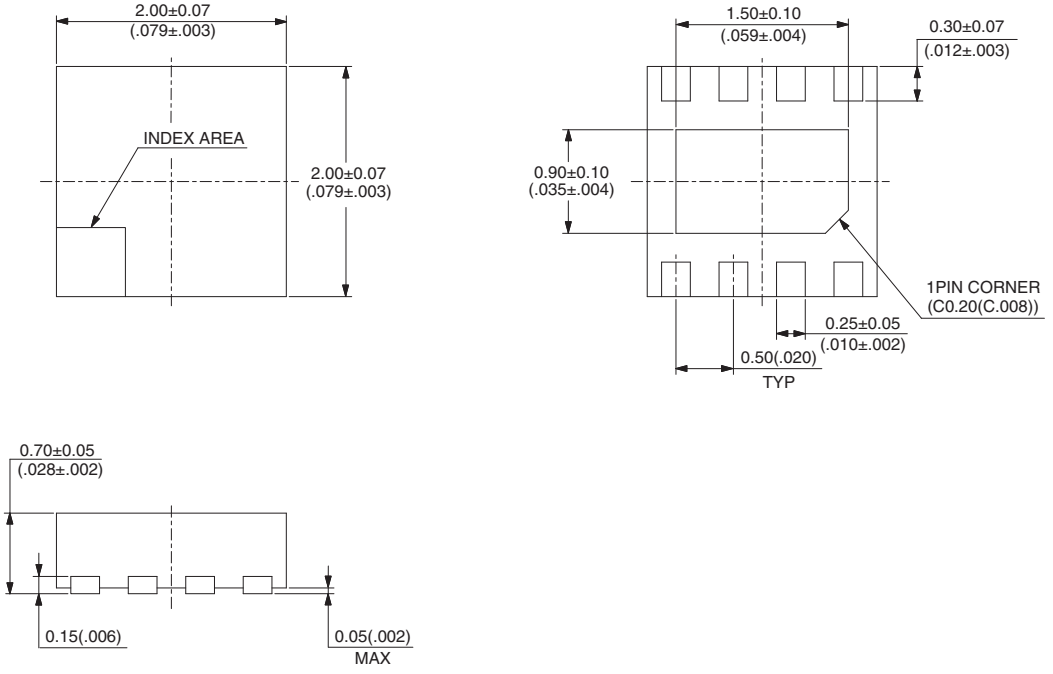
■ ORDERING INFORMATION

Part number	Package	Remark
MB881631BPN-G-EFE1 MB881631BPN-G-ERE1 MB881631CPN-G-EFE1 MB881631CPN-G-ERE1	8-pin plastic SON (LCC-8P-M03)	

■ PACKAGE DIMENSION

8-pin plastic SON		
	Lead pitch	0.50 mm
	Package width × package length	2.00 mm × 2.00 mm
	Sealing method	Plastic mold
	Mounting height	0.75 mm MAX
(LCC-8P-M03)		

8-pin plastic SON
(LCC-8P-M03)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

MEMO

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