FUJITSU MICROELECTRONICS
DATA SHEET

DS04–27277–1E

ASSP for Power Management Applications

2ch PFM/PWM DC/DC converter IC with synchronous rectification

MB39A145

■ DESCRIPTION

MB39A145 is a N-ch/ N-ch synchronous rectification type 2ch Buck converter IC equipped with a bottom detection comparator for low output voltage ripple. It supports low on-duty operation to allow stable output of low voltages when there is a large difference between input and output voltages. This IC offers stable operations regardless of the ESR or type of the output smoothing capacitor. It also allows the high switching frequency setting, enabling the downsized peripheral circuits and low-cost configuration. MB39A145 realizes ultra-rapid response and high efficiency with built-in enhanced protection features. It is most suitable for the power supply for ASIC or FPGA core, input/output devices, or memory.

■ FEATURES

- High efficiency
- Frequency setting by internal preset function : 310 kHz, 620 kHz, 1 MHz
- High accurate reference voltage : ±0.7 % (room temperature)
- Input voltage range : 6 V to 28 V
- Output voltage setting range : 0.7 V to 5.5 V
- Possible to select the PFM/PWM automatic switching mode or PWM-fixed mode
- PAF frequency limitation function (Prohibit Audio Frequency) : > 30 kHz (Min)
- Built-in boost diode, external fly-back diode not required
- Built-in discharge FET
- Built-in over voltage protection function
- Built-in under voltage protection function
- Built-in over temperature protection function
- Built-in over current limitation function
- Soft-start circuit without load dependence
- Current sense resistor not required
- Built-in synchronous rectification type output steps for N-ch MOS FET
- Standby current : 0 µA (Typ)
- Package : TSSOP24 (4.4 mm × 6.5 mm × 1.2 mm)

■ APPLICATIONS

- Digital TV
- Photocopiers
- STB
- BD, DVD players/recorders
- Projectors etc.

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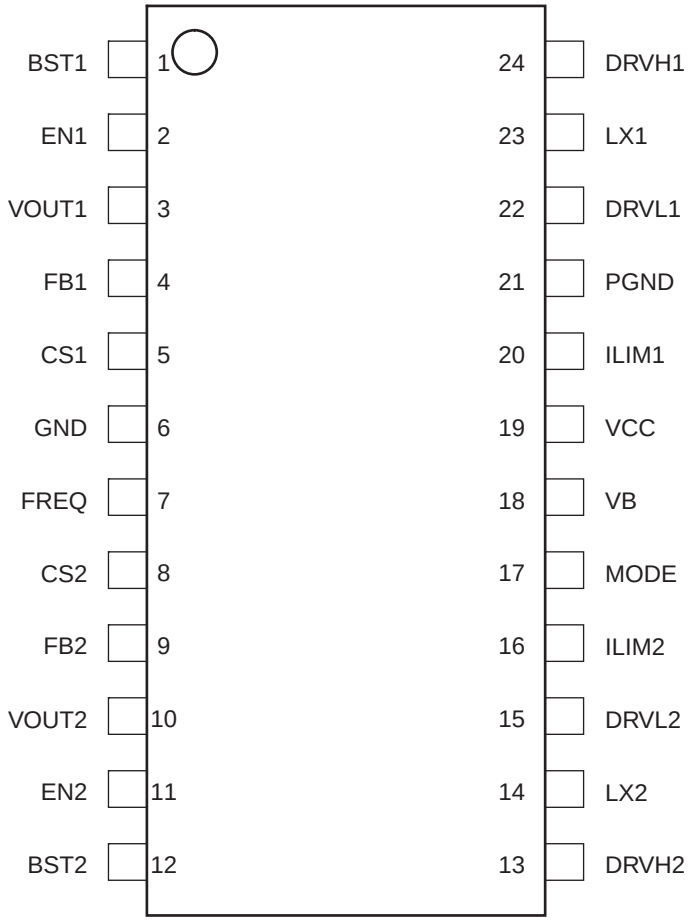
■ PIN ASSIGNMENT

(TOP VIEW)

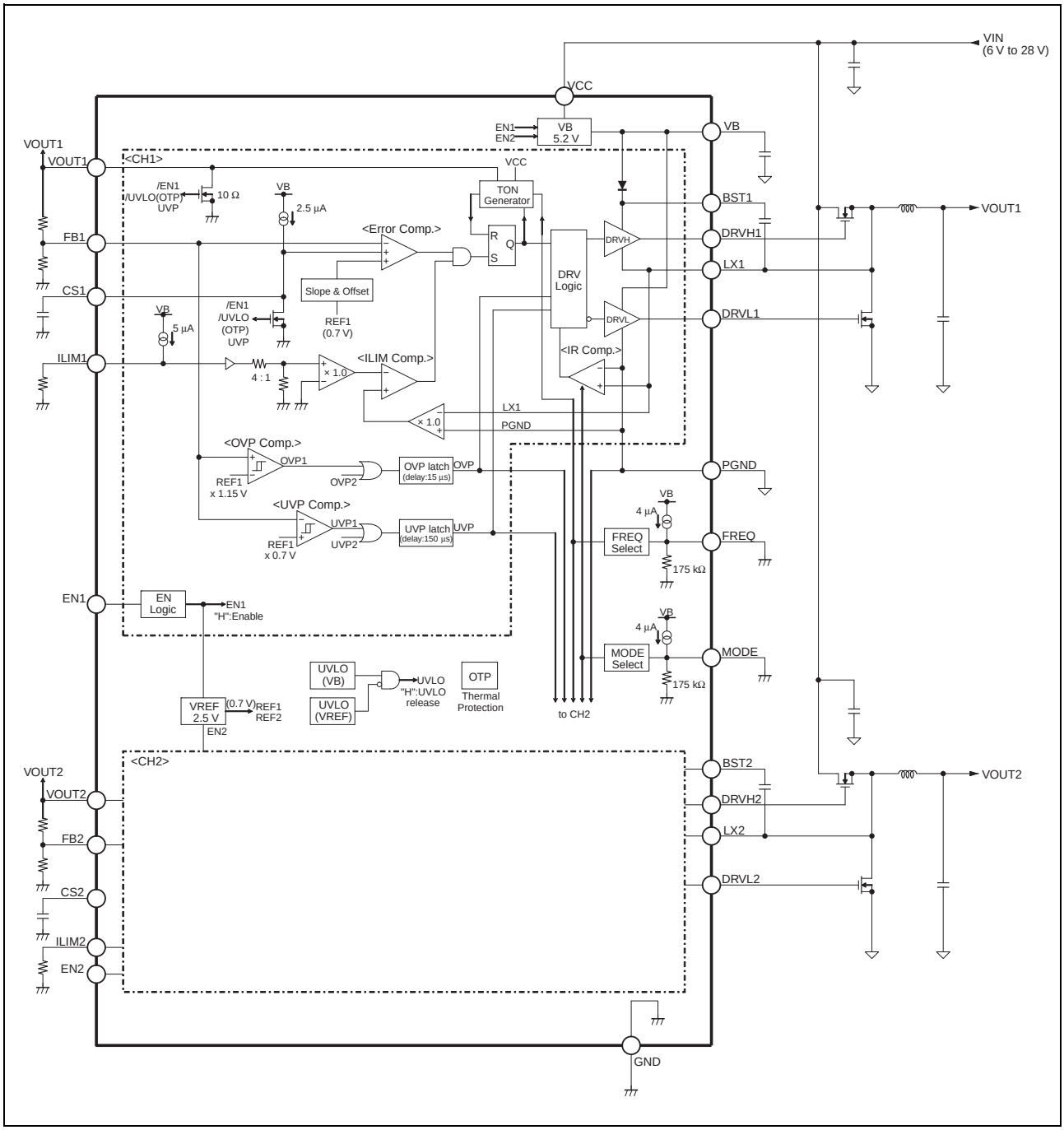


(FPT-24P-M09)

■ PIN DESCRIPTIONS

Pin No.	Pin Name	I/O	Description
1	BST1	—	CH1 boost capacitor connection pin.
2	EN1	I	CH1 enable pin.
3	VOUT1	I	CH1 input pin for DC/DC output voltage.
4	FB1	I	CH1 input pin for feedback voltage.
5	CS1	I	CH1 soft-start time setting capacitor connection pin.
6	GND	—	Ground pin.
7	FREQ	I	Frequency switching signal input pin. FREQ : GND Connection Switching frequency 310 kHz FREQ : Open Switching frequency 620 kHz FREQ : VB Connection Switching frequency 1 MHz
8	CS2	I	CH2 soft-start time setting capacitor connection pin.
9	FB2	I	CH2 input pin for feedback voltage.
10	VOUT2	I	CH2 input pin for DC/DC output voltage.
11	EN2	I	CH2 enable pin.
12	BST2	—	CH2 boost capacitor connection pin.
13	DRVH2	O	CH2 output pin for external high-side FET drive.
14	LX2	—	CH2 coil and external high-side FET source connection pin.
15	DRVL2	O	CH2 output pin for external low-side FET gate drive.
16	ILIM2	I	CH2 over current detection level setting voltage input pin.
17	MODE	I	DC/DC control mode switching signal input pin. MODE : GND Connection PFM/PWM MODE : Open PFM/PWM, PAF MODE : VB Connection PWM fixed
18	VB	O	Internal circuit bias output pin.
19	VCC	I	Power input pin for control and output circuits.
20	ILIM1	I	CH1 over current detection level setting voltage input pin.
21	PGND	—	Ground pin for output circuit.
22	DRVL1	O	CH1 output pin for external low-side FET gate drive.
23	LX1	—	CH1 coil and external high-side FET source connection pin.
24	DRVH1	O	CH1 output pin for external high-side FET drive.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating		Unit
			Min	Max	
VCC pin input voltage	V_{VCC}	VCC pin	− 0.3	+ 30	V
BST pin input voltage	V_{BST}	BST1, BST2 pins	− 0.3	+ 36	V
LX pin input voltage	V_{LX}	LX1, LX2 pins	− 1	+ 30	V
Voltage between BST and LX	V_{BST-LX}	—	− 0.3	+ 7	V
EN pin input voltage	V_{EN}	EN1, EN2 pins	− 0.3	+ 30	V
Input voltage	V_{FB}	FB1, FB2 pins	− 0.3	VB + 0.3	V
	V_{VOUT}	VOUT1, VOUT2 pins	− 0.3	+ 7	V
	V_{ILIM}	ILIM1, ILIM2 pins	− 0.3	VB + 0.3	V
	V_{CS}	CS1, CS2 pins	− 0.3	VB + 0.3	V
	V_{FREQ}	FREQ pin	− 0.3	VB + 0.3	V
	V_{MODE}	MODE pin	− 0.3	VB + 0.3	V
Output current	I_{OUT}	DRVH1, DRVH2 pins, DRVL1, DRVL2 pins	—	60	mA
Power dissipation	P_D	Ta ≤ + 25 °C	—	1602	mW
Storage temperature	T_{STG}	—	− 55	+ 125	°C

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
VCC pin input voltage	V_{VCC}	VCC pin	6	—	(28)	V
BST pin input voltage	V_{BST}	BST1, BST2 pins	—	—	(34)	V
EN pin input voltage	V_{EN}	EN1, EN2 pins	0	—	28	V
Input voltage	V_{FB}	FB1, FB2 pins	0	—	VB	V
	V_{VOUT}	VOUT1, VOUT2 pins	0	—	5.7	V
	V_{ILIM}	ILIM1, ILIM2 pins	0	—	2	V
	V_{FREQ}	FREQ pin	0	—	VB	V
	V_{MODE}	MODE pin	0	—	VB	V
Peak output current	I_{OUT}	DRVH1, DRVH2 pins, DRVL1, DRVL2 pins Duty ≤ 5 % ($t = 1/f_{OSC} \times$ Duty)	− 1200	—	+ 1200	mA
Operating ambient temperature	Ta	—	− 30	+ 25	+ 85	°C

Numbers with ( ) are target values.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

(Ta = + 25 °C, VCC pin = 12 V, EN1, EN2 pins = 5 V)

Parameter		Sym-bol	Pin No.	Condition	Target value			Unit
					Min	Typ	Max	
Bias Voltage Block [VB Reg.]	Output voltage	V_{VB}	18	VB pin = 0 A	5.04	5.20	5.36	V
	Input stability	LINE	18	VCC pin = 6 V to 28 V	—	10	100	mV
	Load stability	LOAD	18	VB pin = 0 A to –1 mA	—	10	100	mV
	Short-circuit output current	I_{OS}	18	VB pin = 0 V	–200	–140	–100	mA
Under voltage Lockout Protection Circuit Block [UVLO]	Threshold voltage	V_{TLH}	18	VB pin	4.0	4.2	4.4	V
		V_{THL}	18	VB pin	3.7	3.9	4.1	V
	Hysteresis width	V_H	18	VB pin	—	0.3	—	V
Soft-Start/ Discharge Block [Soft-Start, Discharge]	Charge current	I_{CS}	5, 8	CS1, CS2 pins = 0 V	—	–2.5	—	µA
	Electrical discharge resistance	R_D	3, 10	EN1, EN2 pins = 0 V, VOUT1, VOUT2 pins ≥ 0.15 V	—	20	—	Ω
	Discharge end voltage	V_{VOVTH}	3, 10	EN1, EN2 pins = 0 V, VOUT1, VOUT2 pins	—	0.15	—	V
ON/OFF Time Generator Block [t_{ON} Generator]	ON time (Preset value 1)	t_{ON11}	24	FREQ pin GND connection VCC = 12 V, VOUT1 = 1.0 V	322	358	394	ns
		t_{ON21}	13	FREQ pin GND connection VCC = 12 V, VOUT2 = 1.5 V	360	400	440	ns
	ON time (Preset value 2)	t_{ON12}	24	FREQ pin OPEN VCC = 12 V, VOUT1 = 1.0 V	157	175	193	ns
		t_{ON22}	13	FREQ pin OPEN VCC = 12 V, VOUT2 = 1.5 V	180	200	220	ns
	ON time (Preset value 3)	t_{ON13}	24	FREQ pin VB connection VCC = 12 V, VOUT1 = 1.0 V	97	108	119	ns
		t_{ON23}	13	FREQ pin VB connection VCC = 12 V, VOUT2 = 1.5 V	112	125	138	ns

(Continued)

(Ta = + 25 °C, VCC pin = 12 V, EN1, EN2 pins = 5 V)

Parameter		Sym-bol	Pin No.	Condition	Target value			Unit
					Min	Typ	Max	
ON/OFF Time Generator Block [t_{ON} Generator]	Minimum ON time (Preset value 1)	$t_{ONMIN11}$	24	FREQ pin GND connection VCC = 12 V, VOUT1 = 0 V	—	173	TBD	ns
		$t_{ONMIN21}$	13	FREQ pin GND connection VCC = 12 V, VOUT2 = 0 V	—	137	TBD	ns
	Minimum ON time (Preset value 2)	$t_{ONMIN12}$	24	FREQ pin OPEN VCC = 12 V, VOUT1 = 0 V	—	100	TBD	ns
		$t_{ONMIN22}$	13	FREQ pin OPEN VCC = 12 V, VOUT2 = 0 V	—	83	TBD	ns
	Minimum ON time (Preset value 3)	$t_{ONMIN13}$	24	FREQ pin VB connection VCC = 12 V, VOUT1 = 0 V	—	73	TBD	ns
		$t_{ONMIN23}$	13	FREQ pin VB connection VCC = 12 V, VOUT2 = 0 V	—	63	TBD	ns
	Minimum OFF time	t_{OFFMIN}	24, 13	—	—	400	520	ns
Error Comparison Block [Error Comp.]	Threshold voltage	V_{TH}	4, 9	Ta = + 25 °C	0.695	0.700	0.705	V
	FB pin input current	I_{FB}	4, 9	FB1, FB2 pins = 0.7 V	–0.1	0	+ 0.1	µA
	VOUT pin input current	I_{VO}	3, 10	VOUT1, VOUT2 pins = 1.5 V	—	6.3	8.4	µA
Over Current Detection Block [ILIM Comp.]	Over current limitation setting value	V_{ILIM}	21-23 21-14	PGND pin - LX1, LX2 pins R_{ILIM} = 100 kΩ	90	100	110	mV
	ILIM pin current	I_{ILIM}	20, 16	ILIM1, ILIM2 pins = 0 V	–6	–5	–4	µA
	ILIM pin current Temperature slope	T_{ILIM}	20, 16	Ta = + 25 °C	—	4500	—	ppm / °C
Over-voltage Protection Circuit Block [OVP Comp.]	Over-voltage detecting voltage	V_{OVP}	4, 9	Internal reference voltage	110	115	120	%
	Hysteresis width	V_{HOVP}	4, 9	—	—	5	—	%
	Detection delay time	t_{OVP}	—	—	—	15	—	µs

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(Ta = + 25 °C, VCC pin = 12 V, EN1, EN2 pins = 5 V)

Parameter		Sym-bol	Pin No.	Condition	Target value			Unit
					Min	Typ	Max	
Under-voltage Protection Circuit Block [UVP Comp.]	Under-voltage detecting voltage	V_{UVP}	4, 9	Internal reference voltage	65	70	75	%
	Hysteresis width	V_{HUVP}	4, 9	—	—	10	—	%
	Detection delay time	t_{UVP}	—	—	—	150	—	µs
Over-temperature Protection Circuit Block [OTP]	Protection temperature	T_{OTPH}	—	—	—	+ 150	—	°C
		T_{OTPL}	—	—	—	+ 125	—	°C
Output Block [DRV]	High-side output on-resistance	R_{OH}	24, 13	DRVH1, DRVH2 = –100 mA	—	4	6	Ω
		R_{OL}	24, 13	DRVH1, DRVH2 = 100 mA	—	1	2	Ω
	Low-side output on-resistance	R_{OH}	22, 15	DRVL1, DRVL2 = –100 mA	—	4	6	Ω
		R_{OL}	22, 15	DRVL1, DRVL2 = 100 mA	—	1	2	Ω
	Output source current	I_{SOURCE}	24, 13 22, 15	LX1, LX2 pins = 0 V, BST1, BST2 pins = VB pin DRVH1, DRVH2 pins = 2.5 V DUTY ≤ 5 %	—	–0.5	—	A
	Output sink current	I_{SINK}	24, 13 22, 15	LX1, LX2 pins = 0 V, BST1, BST2 pins = VB pin DRVH1, DRVH2 pins = 2.5 V DUTY ≤ 5 %	—	0.9	—	A
	Dead time	t_D	24-22 13-15	LX1, LX2 pins = 0 V, BST1, BST2 pins = VB pin	TBD	25	TBD	ns
	BSTSW ON resistance	R_{ONBST}	1, 12	VB pin = 5.2 V	70	100	130	Ω
	Leak current	I_{LEAK}	1, 12	BST1, BST2 pins = 36 V, LX1, LX2 pins = 30 V Ta = + 25 °C	—	0.1	1	µA

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(Ta = + 25 °C, VCC pin = 12 V, EN1, EN2 pins = 5 V)

Parameter		Sym-bol	Pin No.	Condition	Target value			Unit
					Min	Typ	Max	
Switching Frequency Control Block [FREQ]	Preset value 1 conditions	V_{FREQ1}	7	FREQ pin : GND connection	0	—	0.3	V
	Preset value 2 conditions	V_{FREQ2}	7	FREQ pin : OPEN	0.5	—	1.5	V
	Preset value 3 conditions	V_{FREQ3}	7	FREQ pin : VB connection	2.0	—	VB	V
	FREQ pin output voltage	V_{FREQ}	7	FREQ pin = OPEN	0.6	0.7	0.8	V
	FREQ pin input current	I_{FREQ}	7	FRRQ pin = 0 V	–5.6	–4.0	—	µA
PFM Control Circuit Block [MODE]	Reverse current detection Threshold voltage	V_{TH}	23, 14	LX1, LX2 pins	–4	–1	+ 2	mV
	PFM/PWM mode conditions PAF function disabled	V_{PFM1}	17	MODE pin: GND connection	0	—	0.3	V
	PFM/PWM mode conditions PAF function enabled	V_{PFM2}	17	MODE pin : OPEN	0.5	—	1.5	V
	PWM-fixed mode conditions	V_{PWM}	17	MODE pin : VB connection	2.0	—	VB	V
	PAF frequency	f_{PAF}	—	Ta = –30 °C to +85 °C	30	40	—	kHz
	MODE pin voltage	V_{MODE}	17	MODE = OPEN	0.6	0.7	0.8	V
	MODE pin input current	I_{MODE}	17	MODE = 0 V	–5.6	–4.0	—	µA
Enable Block [EN1, EN2]	ON condition	V_{ON}	2, 11	EN1, EN2 pins	2.64	—	—	V
	OFF condition	V_{OFF}	2, 11	EN1, EN2 pins	—	—	0.66	V
	Hysteresis width	V_H	2, 11	EN1, EN2 pins	—	0.4	—	V
	Input current	I_{EN}	2, 11	EN1, EN2 pins = 5 V	–0.1	0	+ 0.1	µA
General	Standby current	I_{CCS}	19	EN1, EN2 pins = 0 V	—	0	10	µA
	Power supply current	I_{CC}	19	LX1, LX2 pins = 0 V BST1, BST2 pins : VB connection	—	600	900	µA

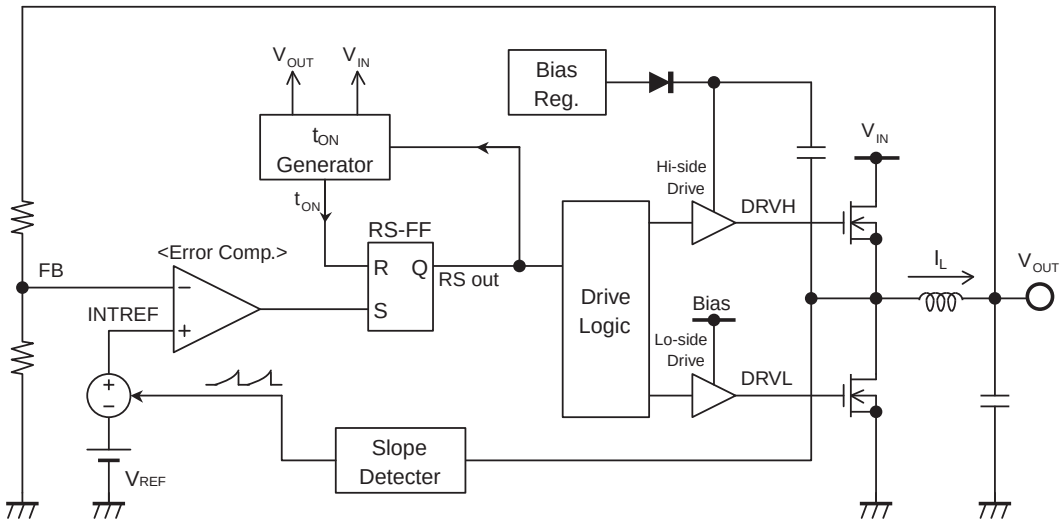
■ FUNCTION

1. Bottom detection comparator system for low output voltage ripple

The bottom detection comparator system for low output voltage ripple determines the ON time (t_{ON}) using the input voltage (V_{IN}) and output voltage (V_{OUT}) to hold the ON state for a specified period. During the OFF period, the reference voltage (INTREF) is compared with the feedback voltage (FB) using the error comparator (Error Comp.) . When the feedback voltage (FB) is below the reference voltage (INTREF) , RS-FF is set and the ON period starts again. Switching is repeated as described above. Error Comp. is used to compare the reference voltage (INTREF) with the feedback voltage (FB) to control the off-duty condition in order to stabilize the output voltage.

This system adds the coil current slope detected during the synchronous rectification period (t_{OFF}) to the reference voltage (INTREF) , and generates an output voltage slope during the OFF period, which is essential for the bottom detection comparator system, in the IC. This enables the stable control operations under the low output voltage ripple conditions.

<Circuit diagram>



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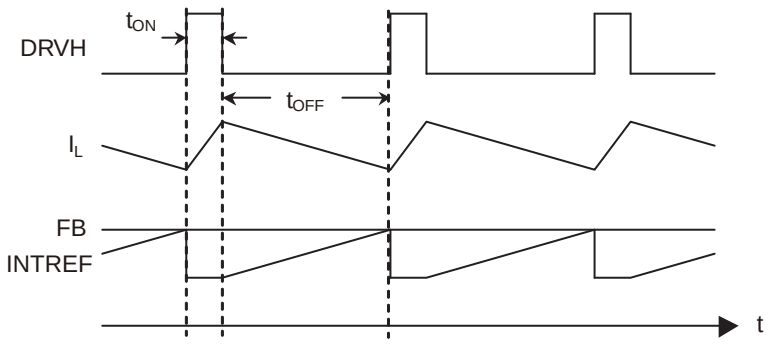


(1) Bias Voltage Block (VB Reg.)

The 5.2 V (Typ) bias voltage is generated from the VCC pin (pin 19) voltage for the control, output, and boost circuits. When either or both of the EN1 and EN2 pins (pins 2 and 11) are set to the “H” level, the system is restored from the standby state to supply the bias voltage from the VB pin (pin 18) .

(2) ON/OFF Time Generator Block (t_{ON} Generator)

This block contains a capacitor for timing setting and a resistor for timing setting and generates ON time (t_{ON}) which depends on input voltage and output voltage. The switching frequency can be switched by setting the FREQ pin (pin 7) to any one of GND connection, OPEN, and VB connection. ON time for each CH is obtained from the following formula.

<FREQ pin : GND connection>

$$t_{ON1}\ (ns) = \frac{V_{VOUT1}}{V_{VIN}} \times 4300 \quad (f_{OSC1} \fallingdotseq 230\ kHz)$$

$$t_{ON2}\ (ns) = \frac{V_{VOUT2}}{V_{VIN}} \times 3200 \quad (f_{OSC2} \fallingdotseq 310\ kHz)$$

<FREQ pin : OPEN>

$$t_{ON1}\ (ns) = \frac{V_{VOUT1}}{V_{VIN}} \times 2100 \quad (f_{OSC1} \fallingdotseq 460\ kHz)$$

$$t_{ON2}\ (ns) = \frac{V_{VOUT2}}{V_{VIN}} \times 1600 \quad (f_{OSC2} \fallingdotseq 620\ kHz)$$

<FREQ pin : VB connection>

$$t_{ON1}\ (ns) = \frac{V_{VOUT1}}{V_{VIN}} \times 1300 \quad (f_{OSC1} \fallingdotseq 750\ kHz)$$

$$t_{ON2}\ (ns) = \frac{V_{VOUT2}}{V_{VIN}} \times 1000 \quad (f_{OSC2} \fallingdotseq 1000\ kHz)$$

The switching frequency of CH2 is set to 1.33 times that of CH1 to prevent the beat by the frequency difference of channel to channel.

(3) Output Block (DRV1, DRV2)

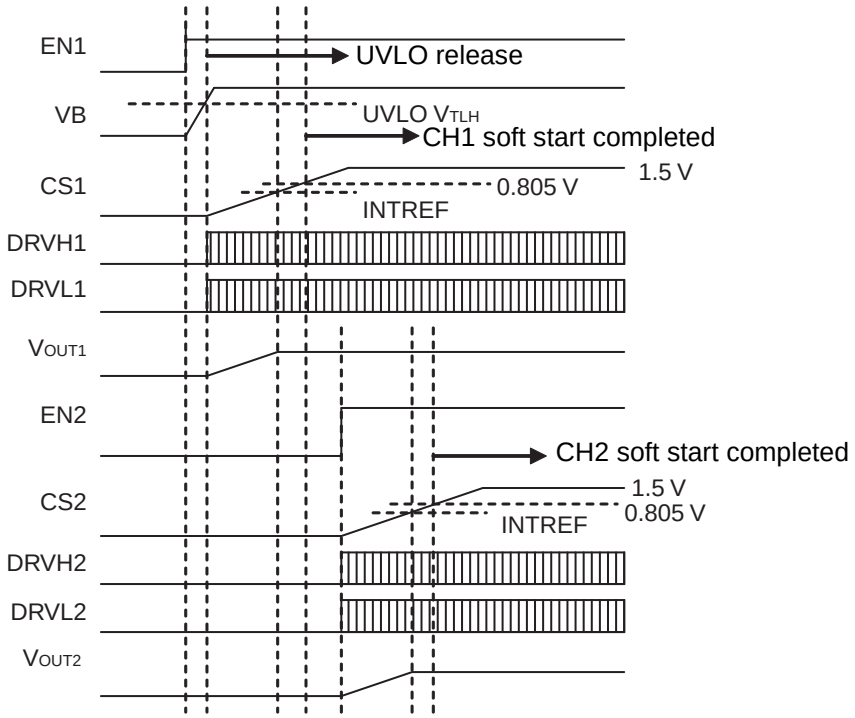
The output circuit is configured in CMOS type for both of the high-side and the low-side. It provides the 0.5 A (Typ) source current and 0.9 A (Typ) sink current, drive the external N-ch MOS FET. The output circuit of the high-side FET supplies the power from the boost circuit including the built-in boost diode. The output circuit of the low-side FET supplies the power from the VB pin. This circuit monitors the gate voltages of the high-side and low-side FETs. Until either FET is turned off, this circuit controls the ON timing of another FET, preventing the shoot-through current. The sink ON resistance of the output circuit is low 1 Ω (Typ) , helping to prevent the low-side FET from turning on by itself.

(4) Starting sequence

When the EN1 pin (pin 2) or EN2 pin (pin 11) is set to the “H” level, the bias voltage is supplied from the VB pin (pin 18). If the voltage of the VB pin exceeds the UVLO threshold voltage, the DC/DC converter starts operations and carries out the soft start. The soft start is a function used to prevent a rush current when the power is started.

Activating the soft start initiates charging of the capacitor connected to the CS1 and CS2 pins (pins 5 and 8) and inputs the lamp voltage to the error comparator (Error Comp.) of each channel. The DC/DC converter generates the output voltage according to that lamp voltage. This results in the soft start operation that does not depend on the output load. The over voltage protection (OVP) and under voltage protection (UVP) functions are disabled while the soft start is active.

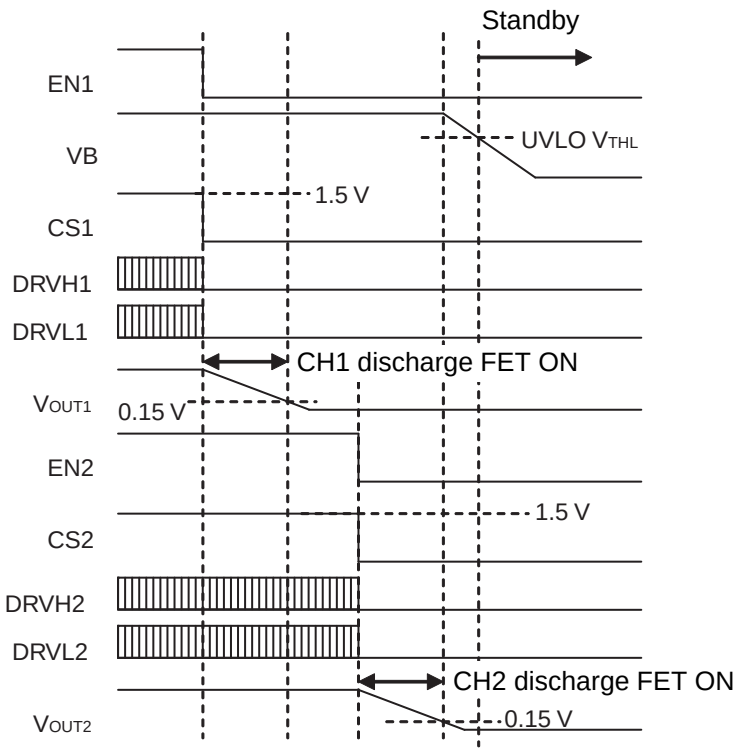
<Timing chart>



(5) DC/DC converter stop sequence (Discharge, standby)

When the EN1 pin (pin 2) or EN2 pin (pin 11) is set to the “H” level, the output capacitor is discharged using the discharge FET (R_{ON}≒ 20 Ω) in the IC. If the voltage of the VOUT1 and VOUT2 pin (pin 3 and 10) is below 0.15 V (Typ) by discharging the output capacitor, the IC stops discharge operation. Further, if both the EN1 and EN2 pins are set to the “L” level, the IC also stops the output of the VB pin (pin 18) and enters the standby state after detecting UVLO. The current of the VCC pin (pin19) (I_{VCC}) is then 10 μA (Max) .

<Timing chart>



(6) Under Voltage Lockout Protection (UVLO)

The under voltage lockout protection (UVLO) protects ICs from malfunction and protects the system from destruction/deterioration, according to the reasons mentioned below.

- Transitional state when the bias voltage (VB) or the reference voltage (VREF) starts.
- Momentary decrease

To prevent such a malfunction, this function detects a voltage drop of the VB pin (pin 18) using the comparator (UVLO Comp.), and stops IC operations.

When the VB pin exceeds the threshold voltage of the under voltage lockout protection circuit, the system is restored.

(7) Over Current Limitation (ILIM)

This function limits the output current when it has increased, and protects devices connected to the output. This function detects the coil current from the electromotive force of the low-side FET on-resistance, and compares this voltage with the 1/5-time value of the voltage of the LIM1 and LIM2 pins (pins 20 and 16) on a cyclically, using ILIM Comp. Until this voltage falls below the over current limit value, the high-side FET is held in the off state. After the voltage has fallen below the limit value, the high-side FET is placed into the on state. This limits the lower bound of the coil current and also restricts the over current. As a result, it becomes operation that the output voltage droop.

The over current limit value is set by connecting the resistor to the ILIM pin. The ILIM pin supplies the constant current of 5 μA (Typ) . However, the current value has a temperature slope up to 4500 ppm/ °C to compensate the temperature dependence characteristics of the low-side FET on-resistance.

(8) Over Voltage Protection (OVP)

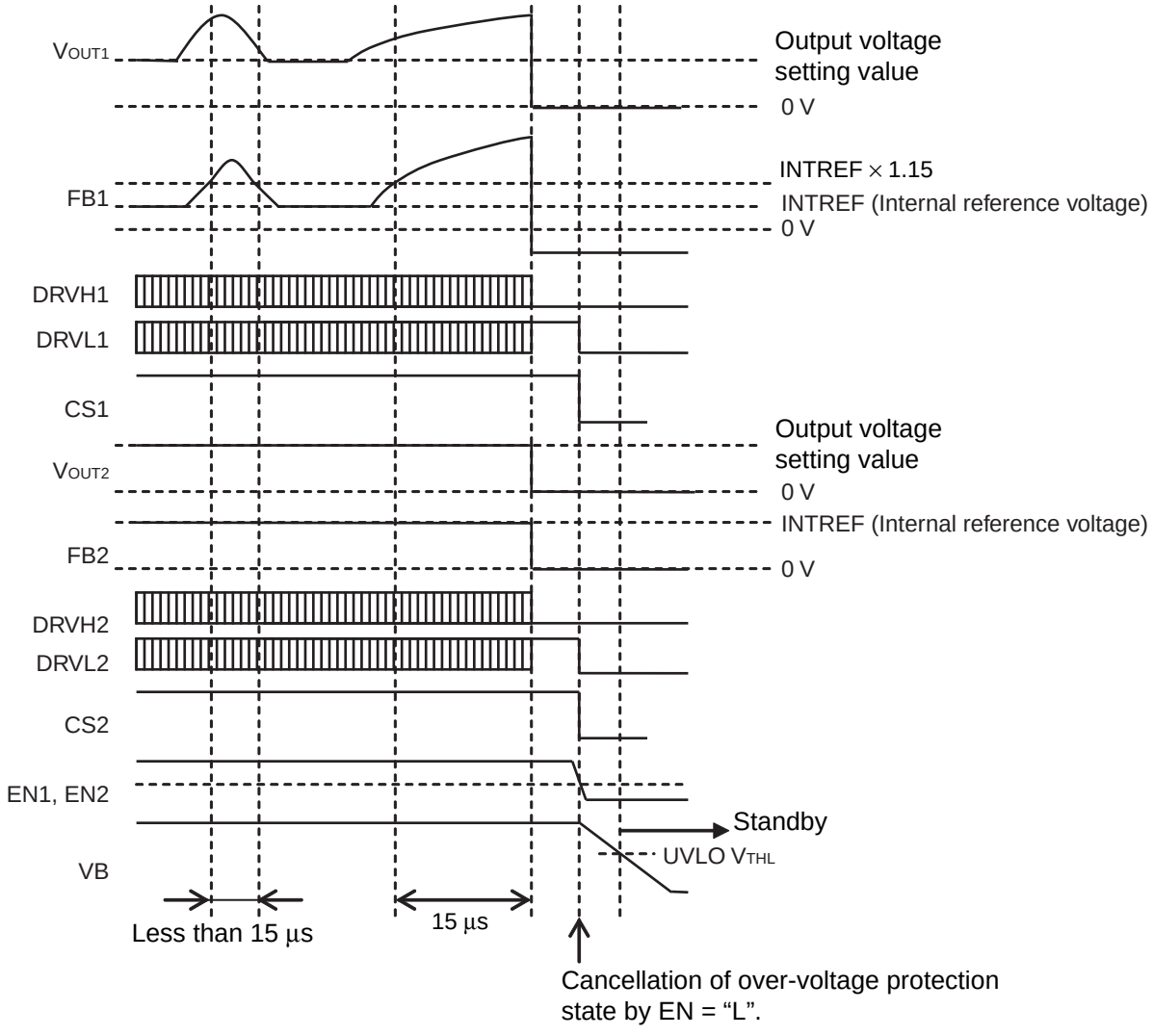
This function stops the power supply when the output voltage has increased, and protects devices connected to the output.

1. Using OVP Comp, this function makes a comparison between the voltage which is 1.15 times (Typ) of the internal reference voltage INTREF (0.7 V), and the feedback voltage for the FB1 and the FB2 pins (pins 4 and 9).
2. If the feedback voltage mentioned in 1 detects the higher state by 15 µs (Typ) or more, the operations below will be performed.
   - Set the RS latch.
   - Set the DRVH1 and the DRVH2 pins (pins 24 and 13) to the “L” level.
   - Set the DRVL1 and the DRVL2 pins (pins 22 and 15) to the “H” level.

These operations fix the high-side FET to the off state and the low-side FET to the on state for both channels of the DC/DC converter, and stops switching (latch stop).

The over-voltage protection state can be cancelled by setting both the EN1 and EN2 pins (pins 2 and 11) to the “L” level or reducing the VCC power once until the bias voltage (VB) falls below V_{THL} of UVLO.

<Timing chart>

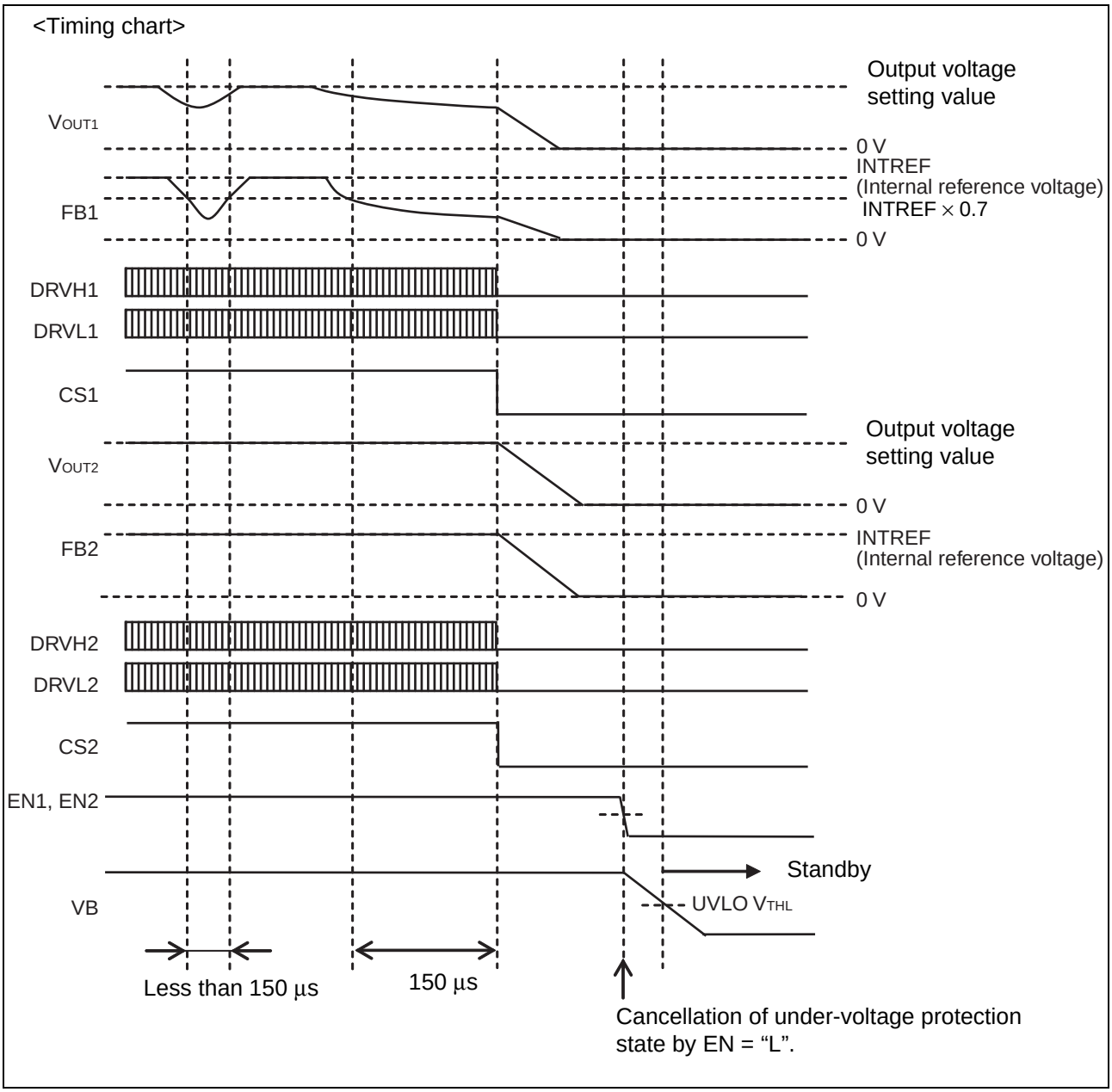


(9) Under Voltage Protection (UVP)

This function stops the power supply when the output voltage has lowered, and protects devices connected to the output. This function compares 0.7 time (Typ) of the internal reference voltage INTREF (0.7 V) with the feedback voltage of the FB1 and FB2 pins (pins 4 and 9) using UVP Comp. The RS latch is set and the DRVH1 and DRVH2 pins (pins 24 and 13) set to the “L” level, and the DRVL1 and DRVL2 pins (pins 22 and 15) set to the “L” level, when the feedback voltage detects a lower state at 150 µs (Typ) or more. This fixes the high-side and low-side FETs to the off-state, of both channels in the DC/DC converter, causing switching to be stopped (latch stopped) . The discharge operation is then carried out to discharge the output capacitor.

The under-voltage protection state can be cancelled by setting both the EN1 and EN2 pins (pins 2 and 11) to the “L” level or reducing the VCC power once until the bias voltage (VB) falls below V_{THL} of UVLO.

<Timing chart>



(10) Over Temperature Protection (OTP)

The over-temperature protection circuit block (OTP) provides a function that prevents the IC from a thermal destruction. If the junction temperature reaches + 150 °C, the DRVH1 and DRVH2 pins (pins 24 and 13) are set to the “L” level, and the DRVL1 and DRVL2 pins (pins 22 and 15) are set to the “L” level. This fixes the high-side and low-side FETs to the off-state, of both channels in the DC/DC converter, causing switching to be stopped. The discharge operation is then carried out to discharge the output capacitor. If the junction temperature drops to + 125 °C, the soft start is activated. (Restored automatically.)

(11) Operation mode

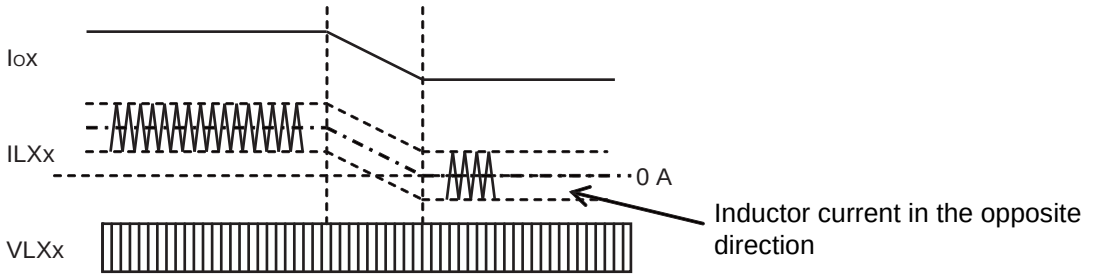
In the PWM-fixed mode, the system acts by the switching frequency specified with the FREQ pin (pin 7) regardless of the load.

In the PFM/PWM automatic switching mode, the switching frequency is reduced at low load, for enhancing the conversion efficiency characteristics. This function detects 0 A of the coil current from the electromotive force of the low-side FET ON resistance, and places the low-side FET into the off state. This results in the switching frequency being reduced automatically depending on the load current when the coil current is below the critical current. The system acts by the switching frequency specified with the FREQ pin, when the coil current exceeds the critical current.

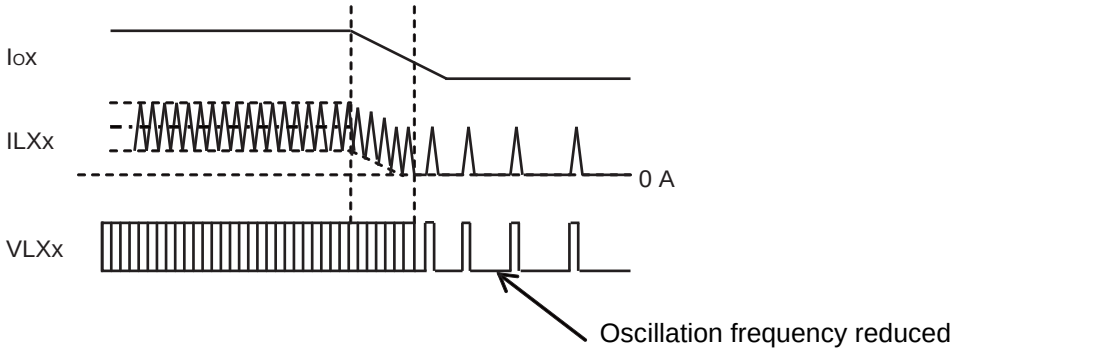
For PAF, the switching frequency at low load is held to 30 kHz (Min) or more.

The operation mode can be switched by setting the MODE pin (pin 17) to any one of GND connection, OPEN, and VB connection.

PWM-fixed mode



PFM/PWM automatic switching mode



X : Each channel number

ENABLE FUNCTION TABLE

EN1 pin	EN2 pin	DC/DC converter (CH1)	DC/DC converter (CH2)
L	L	OFF	OFF
H	L	ON	OFF
L	H	OFF	ON
H	H	ON	ON

DC/DC CONTROL MODE FUNCTION TABLE

MODE pin	DC/DC control
GND connection	PFM/PWM automatic switching mode
OPEN	PFM/PWM automatic switching mode with PAF function
VB connection	PWM-fixed mode

SWITCHING FREQUENCY CONTROL FUNCTION TABLE

FREQ pin	Switching frequency
GND connection	$f_{OSC1} \fallingdotseq$ 230 kHz, $f_{OSC2} \fallingdotseq$ 310 kHz
OPEN	$f_{OSC1} \fallingdotseq$ 460 kHz, $f_{OSC2} \fallingdotseq$ 620 kHz
VB connection	$f_{OSC1} \fallingdotseq$ 750 kHz, $f_{OSC2} \fallingdotseq$ 1 MHz

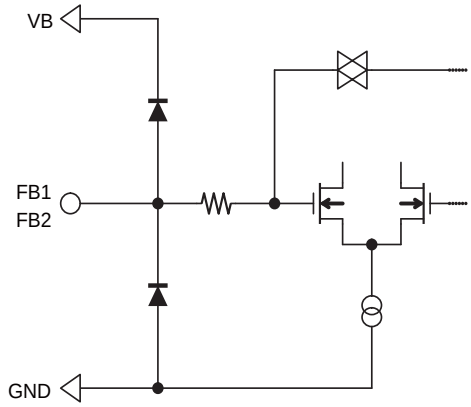
■ PROTECTION FUNCTION TABLE

The following table shows the state of VB pin (pin 18) , DRVH1, DRVH2 pins (pin 24, pin 13) , DRVL1 and DRVL2 pins (pin 22, pin 15) when each protection function operates.

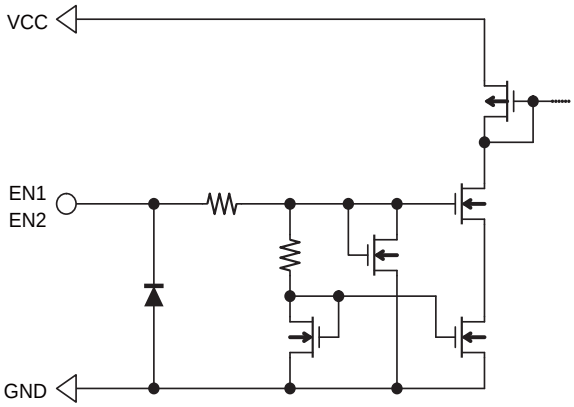
Protection function	Detection condition	Output of each pin after detection			DC/DC output dropping operation
		VB	DRVH1, DRVH2	DRVL1, DRVL2	
Under Voltage Lockout Protection (UVLO)	$VB < 3.9$ V	—	L	L	Electrical discharge by discharge function
Over-current limitation (ILIM)	$V_{PGND} - V_{LX1}$, $V_{LX2} > V_{ILIM1}$, V_{ILIM2}	5.2 V	switching	switching	The voltage is dropped by the constant current
Over Voltage Protection (OVP)	V_{FB1}, $V_{FB2} >$ INTREF1, INTREF2 $\times$ 1.15 (15 µs or more)	5.2 V	L	H	0 V clamping
Under Voltage Protection (UVP)	V_{FB1}, $V_{FB2} >$ INTREF1, INTREF2 $\times$ 0.7 (150 µs or more)	5.2 V	L	L	Electrical discharge by discharge function
Over Temperature Protection (OTP)	$Tj > +150$ °C	5.2 V	L	L	Electrical discharge by discharge function
Enable (EN)	EN1, EN2 : H $\rightarrow$ L (V_{OUT1}, $V_{OUT2} > 0.15$ V)	5.2 V	L	L	Electrical discharge by discharge function

■ I/O PIN EQUIVALENT CIRCUIT DIAGRAM

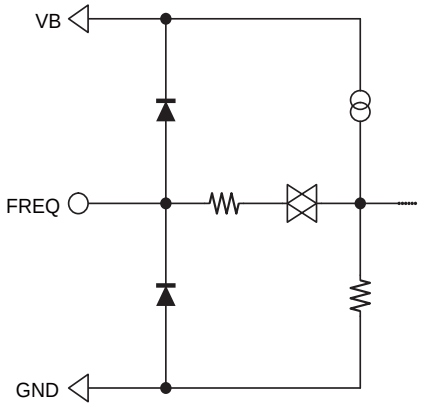
FB1, FB2 pins



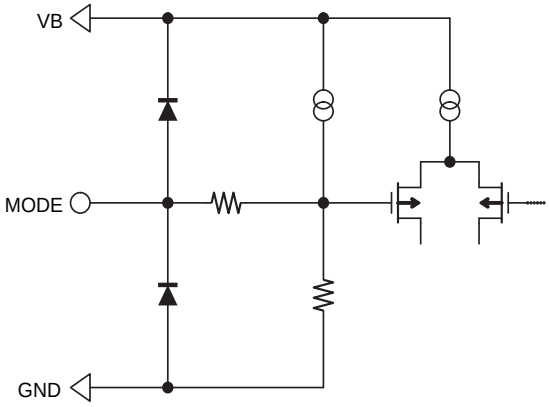
EN1, EN2 pins



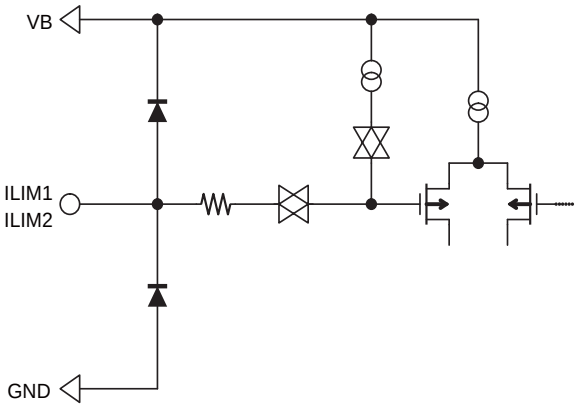
FREQ pin



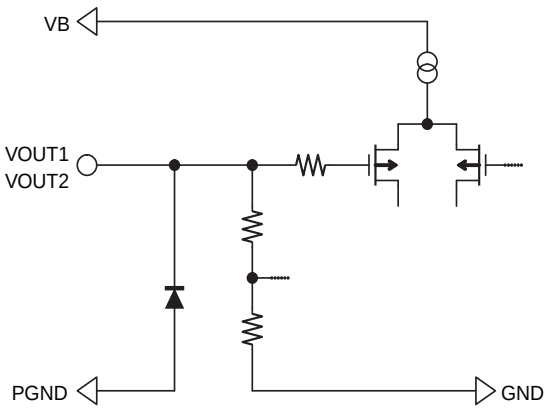
MODE pin



ILIM1, ILIM2 pins



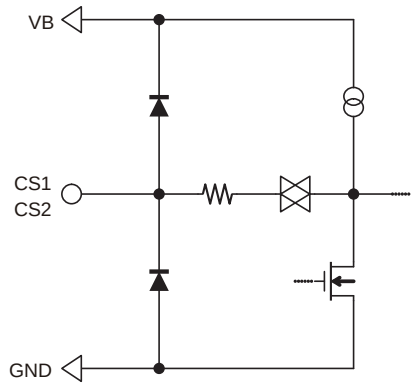
VOUT1, VOUT2 pins



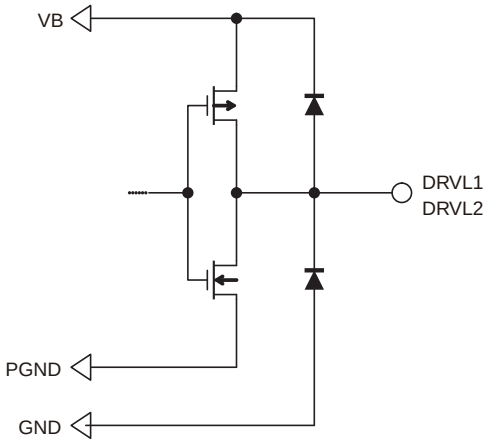
(Continued)

(Continued)

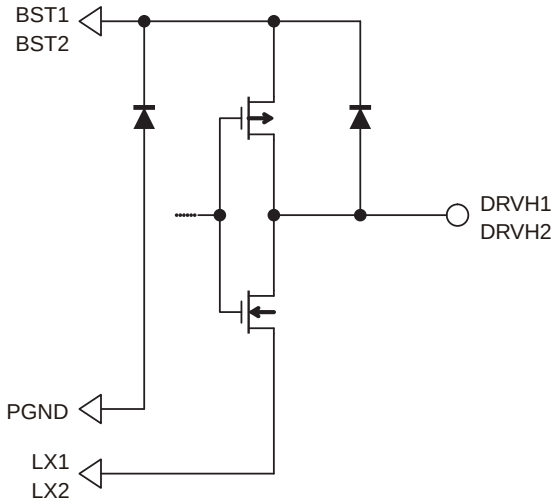
CS pin



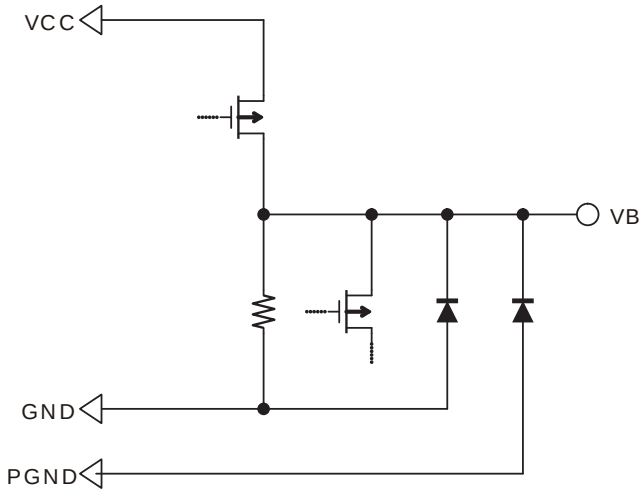
DRVL1, DRVL2 pins



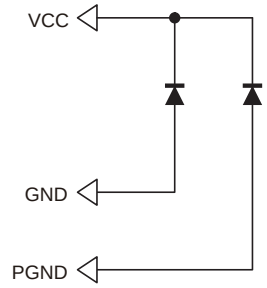
DRVH1, DRVH2, BST1, BST2 and LX1, LX2 pins



VB pin



VCC pin



■ USAGE PRECAUTION

1. Do not configure the IC over the maximum ratings.

If the IC is used over the maximum ratings, the LSI may be permanently damaged.
It is preferable for the device to normally operate within the recommended usage conditions. Usage outside of these conditions can have an adverse effect on the reliability of the LSI.

2. Use the device within the recommended operating conditions.

The recommended values guarantee the normal LSI operation under the recommended operating conditions. The electrical ratings are guaranteed when the device is used within the recommended operating conditions and under the conditions stated for each item.

3. Printed circuit board ground lines should be set up with consideration for common impedance.

4. Take appropriate measures against static electricity.

- Containers for semiconductor materials should have anti-static protection or be made of conductive material.
- After mounting, printed circuit boards should be stored and shipped in conductive bags or containers.
- Work platforms, tools, and instruments should be properly grounded.
- Working personnel should be grounded with resistance of 250 kΩ to 1 MΩ in serial body and ground.

5. Do not apply negative voltages.

The use of negative voltages below –0.3 V may make the parasitic transistor activated to the LSI, and can cause malfunctions.

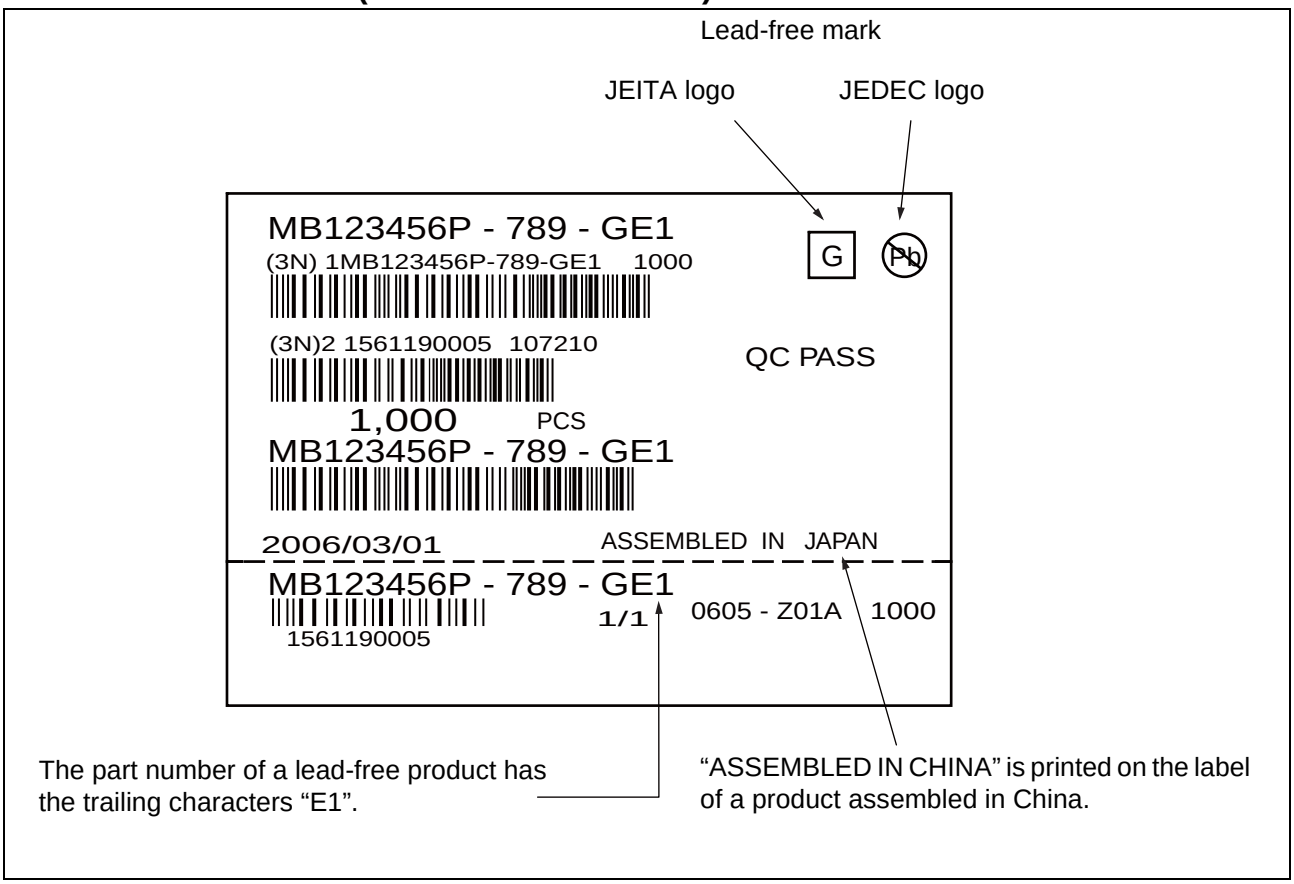
■ ORDERING INFORMATION

Part number	Package	Remarks
MB39A145PFT	24-pin plastic TSSOP (FPT-24P-M09)	

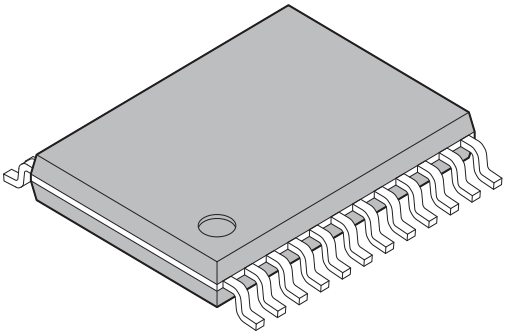
■ RoHS COMPLIANCE INFORMATION OF LEAD (Pb) FREE VERSION

The LSI products of Fujitsu Microelectronics with “E1” are compliant with RoHS Directive, and has observed the standard of lead, cadmium, mercury, Hexavalent chromium, polybrominated biphenyls (PBB) , and polybrominated diphenyl ethers (PBDE) . A product whose part number has trailing characters “E1” is RoHS compliant.

■ LABELING SAMPLE (LEAD FREE VERSION)

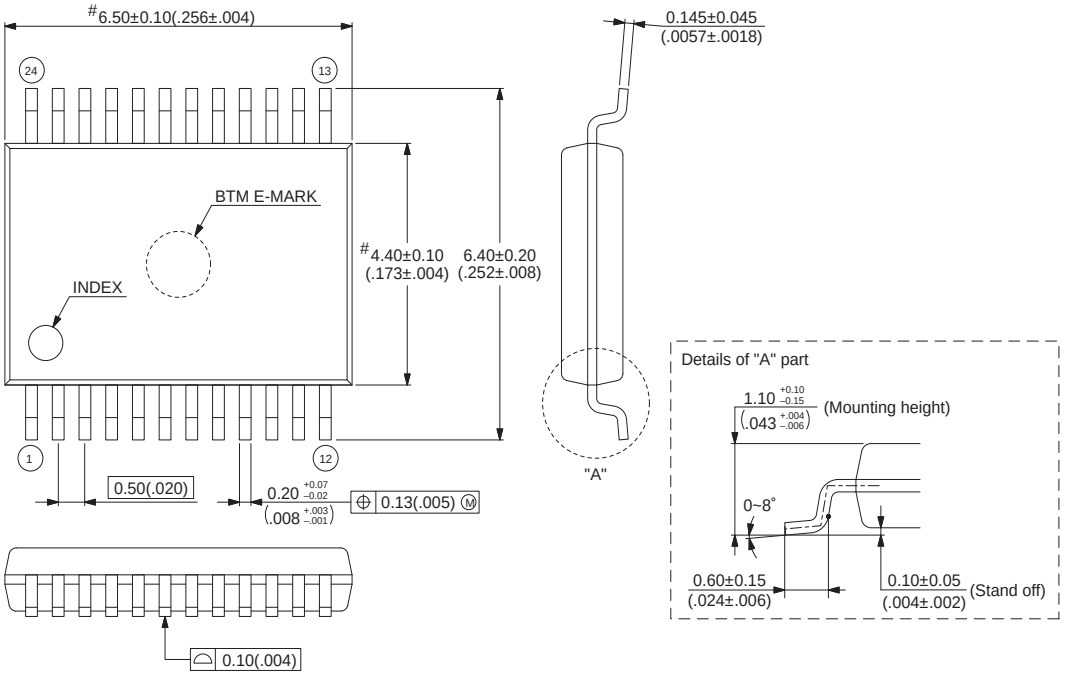


■ PACKAGE DIMENSIONS

24-pin plastic TSSOP		
 (FPT-24P-M09)	Lead pitch	0.50 mm
	Package width × package length	4.40 mm × 6.50 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.20 mm MAX
	Weight	0.08 g

24-pin plastic TSSOP
(FPT-24P-M09)

Note 1) Pins width and pins thickness include plating thickness.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) #: These dimensions do not include resin protrusion.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

■ CONTENTS

MEMO

FUJITSU MICROELECTRONICS LIMITED

Nomura Fudosan Shin-yokohama Bldg. 10-23, Shin-yokohama 2-Chome,
Kohoku-ku Yokohama Kanagawa 222-0033, Japan
Tel: +81-45-415-5858
http://jp.fujitsu.com/fml/en/

For further information please contact:

North and South America
FUJITSU MICROELECTRONICS AMERICA, INC.
1250 E. Arques Avenue, M/S 333
Sunnyvale, CA 94085-5401, U.S.A.
Tel: +1-408-737-5600 Fax: +1-408-737-5999
http://www.fma.fujitsu.com/

Europe
FUJITSU MICROELECTRONICS EUROPE GmbH
Pittlerstrasse 47, 63225 Langen, Germany
Tel: +49-6103-690-0 Fax: +49-6103-690-122
http://emea.fujitsu.com/microelectronics/

Korea
FUJITSU MICROELECTRONICS KOREA LTD.
206 Kosmo Tower Building, 1002 Daechi-Dong,
Gangnam-Gu, Seoul 135-280, Republic of Korea
Tel: +82-2-3484-7100 Fax: +82-2-3484-7111
http://kr.fujitsu.com/fmk/

Asia Pacific
FUJITSU MICROELECTRONICS ASIA PTE. LTD.
151 Lorong Chuan,
#05-08 New Tech Park 556741 Singapore
Tel : +65-6281-0770 Fax : +65-6281-0220
http://www.fmal.fujitsu.com/

FUJITSU MICROELECTRONICS SHANGHAI CO., LTD.
Rm. 3102, Bund Center, No.222 Yan An Road (E),
Shanghai 200002, China
Tel : +86-21-6146-3688 Fax : +86-21-6335-1605
http://cn.fujitsu.com/fmc/

FUJITSU MICROELECTRONICS PACIFIC ASIA LTD.
10/F., World Commerce Centre, 11 Canton Road,
Tsimshatsui, Kowloon, Hong Kong
Tel : +852-2377-0226 Fax : +852-2376-3269
http://cn.fujitsu.com/fmc/en/

Edited: Sales Promotion Department