FUJITSU MICROELECTRONICS
DATA SHEET

DS04-27224-2Ea

ASSP For Power Management Applications

8-ch DC/DC Converter IC with Synchronous Rectifier for Voltage Step-up and Step-down

MB3881

■ DESCRIPTION

The MB3881 a step-up/step-down type of 8-channel, DC/DC converter IC. It uses pulse width modulation (PWM) and synchronous rectification, designed for low voltage, high efficiency, and compactness. This IC is ideal for down conversion and up/down conversion (employing a step-up/step-down Zeta system enabling free I/O setting). The MB3881 can use channel 8 as its own power supply to provide a wide range of supply voltages, allowing itself to operate at low voltage.
In addition, the MB3881 contains a triangular wave oscillator which can operate in synchronization with an external device, allowing the switching timing to be controlled externally. This contributes to reduction in switching noise, facilitating system configuration.
The MB3881 is designed to be compact using the LQFP-64P package whose body size is 7 × 7 mm.
The IC is the best for the power supply for advanced portable equipment such as a camera integrated VTR.
This product is covered by US Patent Number 6,147,477.

■ FEATURES

- Supporting the step-up/step-down Zeta methods (CH1 to CH7)
- Supporting synchronous rectification (CH1, CH2)
- Low start-up voltage : 1.8 V (CH8)

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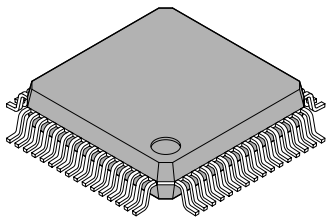
■ PACKAGE

64-pin plastic LQFP



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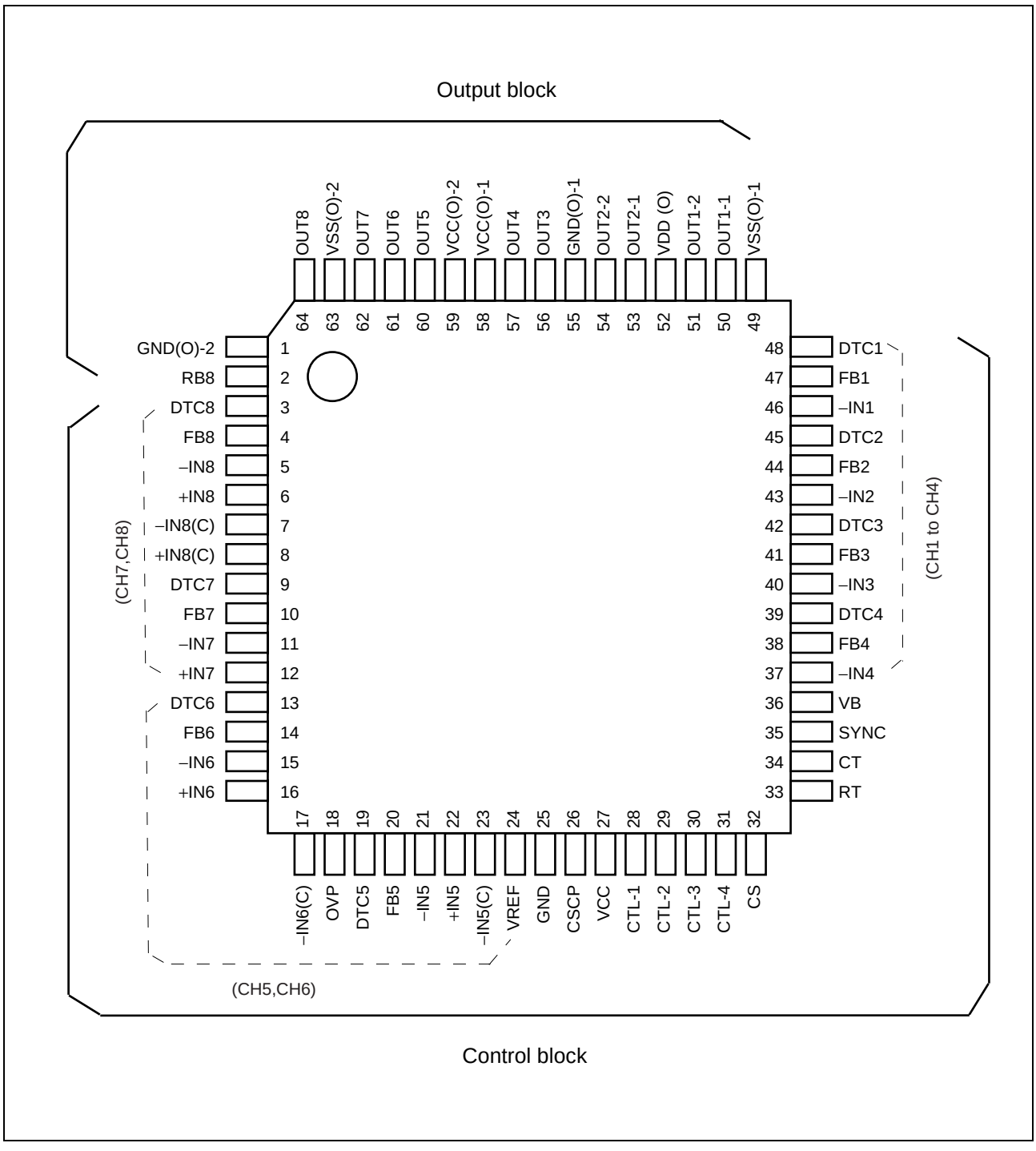
- Power-supply voltage range : 4 V to 13 V (CH1 to CH7)
- Built-in high-precision reference voltage generator : 2.5 V ± 1%
- Oscillation frequency range : 100 kHz to 800 kHz
- Built-in triangular wave oscillator capable of external synchronization
- Error amplifier output for soft-start (CH1 to CH4, CH7)

■ PIN ASSIGNMENT



■ PIN DESCRIPTION

Pin No.		Symbol	I/O	Descriptions
CH1	47	FB1	O	Error amplifier output pin.
	46	−IN1	I	Error amplifier inverted input pin.
	48	DTC1	I	Dead time control pin.
	50	OUT1-1	O	Main side output pin.
	51	OUT1-2	O	Synchronous rectifier side output pin.
CH2	44	FB2	O	Error amplifier output pin.
	43	−IN2	I	Error amplifier inverted input pin.
	45	DTC2	I	Dead time control pin.
	53	OUT2-1	O	Main side output pin.
	54	OUT2-2	O	Synchronous rectifier side output pin.
CH3	41	FB3	O	Error amplifier output pin.
	40	−IN3	I	Error amplifier inverted input pin.
	42	DTC3	I	Dead time control pin.
	56	OUT3	O	Output pin.
CH4	38	FB4	O	Error amplifier output pin.
	37	−IN4	I	Error amplifier inverted input pin.
	39	DTC4	I	Dead time control pin.
	57	OUT4	O	Output pin.
CH5	20	FB5	O	Error amplifier output pin.
	21	−IN5	I	Error amplifier inverted input pin.
	22	+IN5	I	Error amplifier non-inverted input pin.
	23	−IN5 (C)	I	Short detection comparator input pin.
	19	DTC5	I	Dead time control pin.
	60	OUT5	O	Output pin.
CH5, CH6	18	OVP	I	Output maximum voltage setting pin.
CH6	14	FB6	O	Error amplifier output pin.
	15	−IN6	I	Error amplifier inverted input pin.
	16	+IN6	I	Error amplifier non-inverted input pin.
	17	−IN6 (C)	I	Short detection comparator input pin.
	13	DTC6	I	Dead time control pin.
	61	OUT6	O	Output pin.
CH7	10	FB7	O	Error amplifier output pin.
	11	−IN7	I	Error amplifier inverted input pin.
	12	+IN7	I	Error amplifier non-inverted input pin.
	9	DTC7	I	Dead time control pin.
	62	OUT7	O	Output pin.

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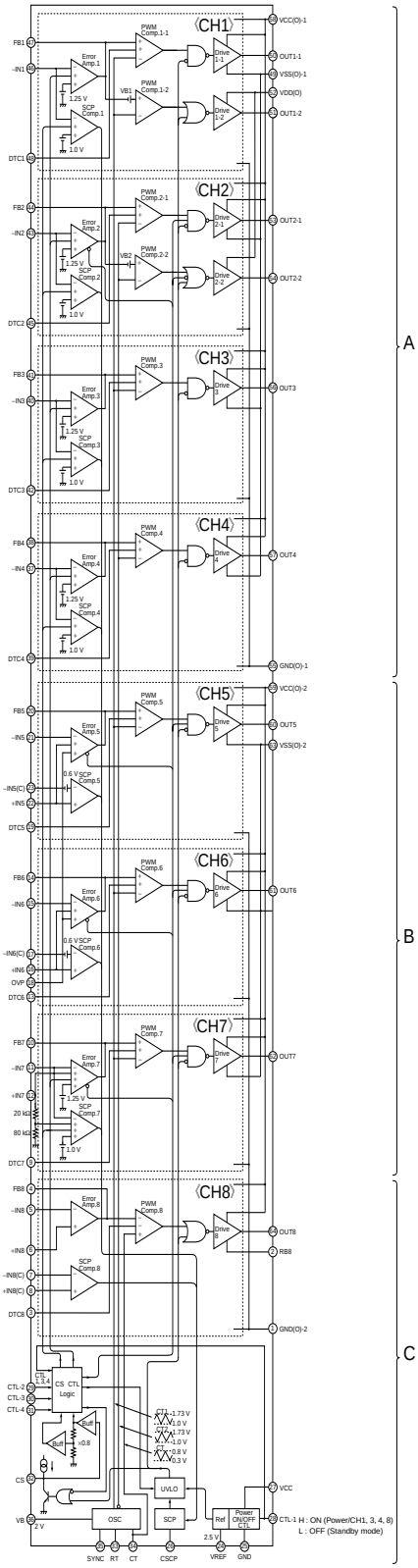
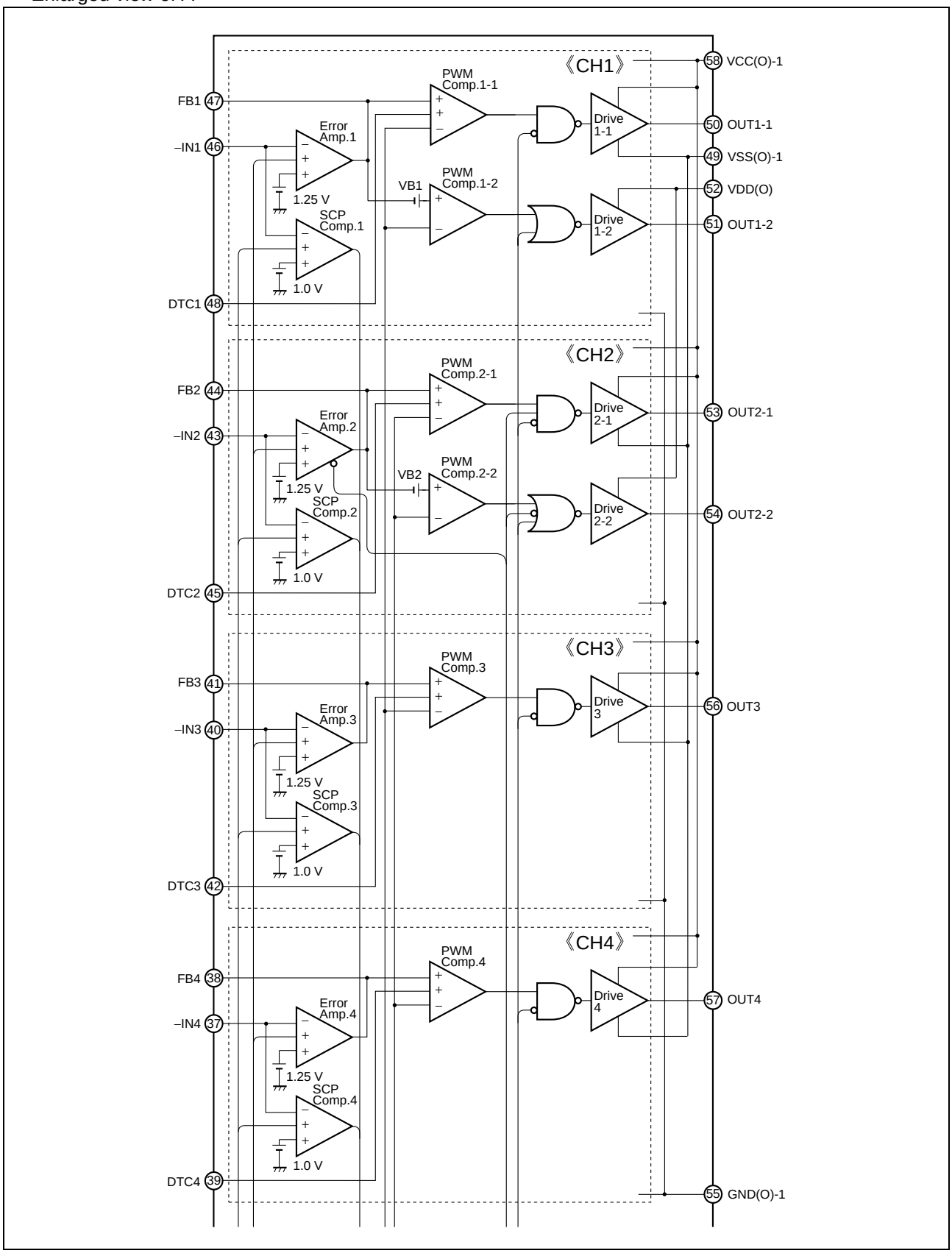
Pin No.		Symbol	I/O	Descriptions
CH8	4	FB8	O	Error amplifier output pin.
	5	−IN8	I	Error amplifier inverted input pin.
	6	+IN8	I	Error amplifier non-inverted input pin.
	7	−IN8 (C)	I	Short detection comparator inverted input pin.
	8	+IN8 (C)	I	Short detection comparator non-inverted input pin.
	3	DTC8	I	Dead time control pin.
	2	RB8	—	Output current setting pin.
	64	OUT8	O	Output pin.
OSC	33	RT	—	Triangular wave frquency setting resistor connection pin.
	34	CT	—	Triangular wave frquency setting capacitor connection pin
	35	SYNC	I	External synchronous signal input pin.
Control	28	CTL-1	I	Power supply, CH 1, 3, 4, 8 control circuit. “H” level : Power supply operating mode “L”level : Standby mode
	29	CTL-2	I	CH 2 control circuit. •CTL-1pin = “H” level “H” level : CH2 operating mode “L” level : CH2 OFF mode
	30	CTL-3	I	CH5, 6 control circuit. •CTL-1pin = “H” level “H” level : CH5, CH6 operating mode “L” level : CH5, CH6 OFF mode
	31	CTL-4	I	CH7 control circuit. •CTL-1pin = “H” level “H” level : CH7 operating mode “L” level : CH7 OFF mode
	26	CSCP	—	Short protection circuit capacitor connection pin.
	32	CS	—	CH1, 2, 3, 4, 7 soft-start circuit capacitor connection pin.
Power	27	VCC	—	Reference voltage and control circuit power supply pin.
	58	VCC (O) -1	—	CH1, 2, 3, 4 output circuit power supply pin.
	59	VCC (O) -2	—	CH5, 6, 7, 8 output circuit power supply pin.
	49	VSS (O) -1	—	CH1, 2, 3, 4 output circuit power supply pin.
	63	VSS (O) -2	—	CH5, 6, 7 output circuit power supply pin.
	52	VDD (O)	—	CH1, 2 synchronous rectifier side output circuit power supply pin.
	24	VREF	O	Refernce voltage output pin.
	36	VB	O	Triangular wave oscillator regulator output pin.
	25	GND	—	Ground pin.
	55	GND (O) -1	—	CH1, 2, 3, 4 output circuit ground pin.
	1	GND (O) -2	—	CH5, 6, 7, 8 output circuit ground pin.

■ BLOCK DIAGRAM

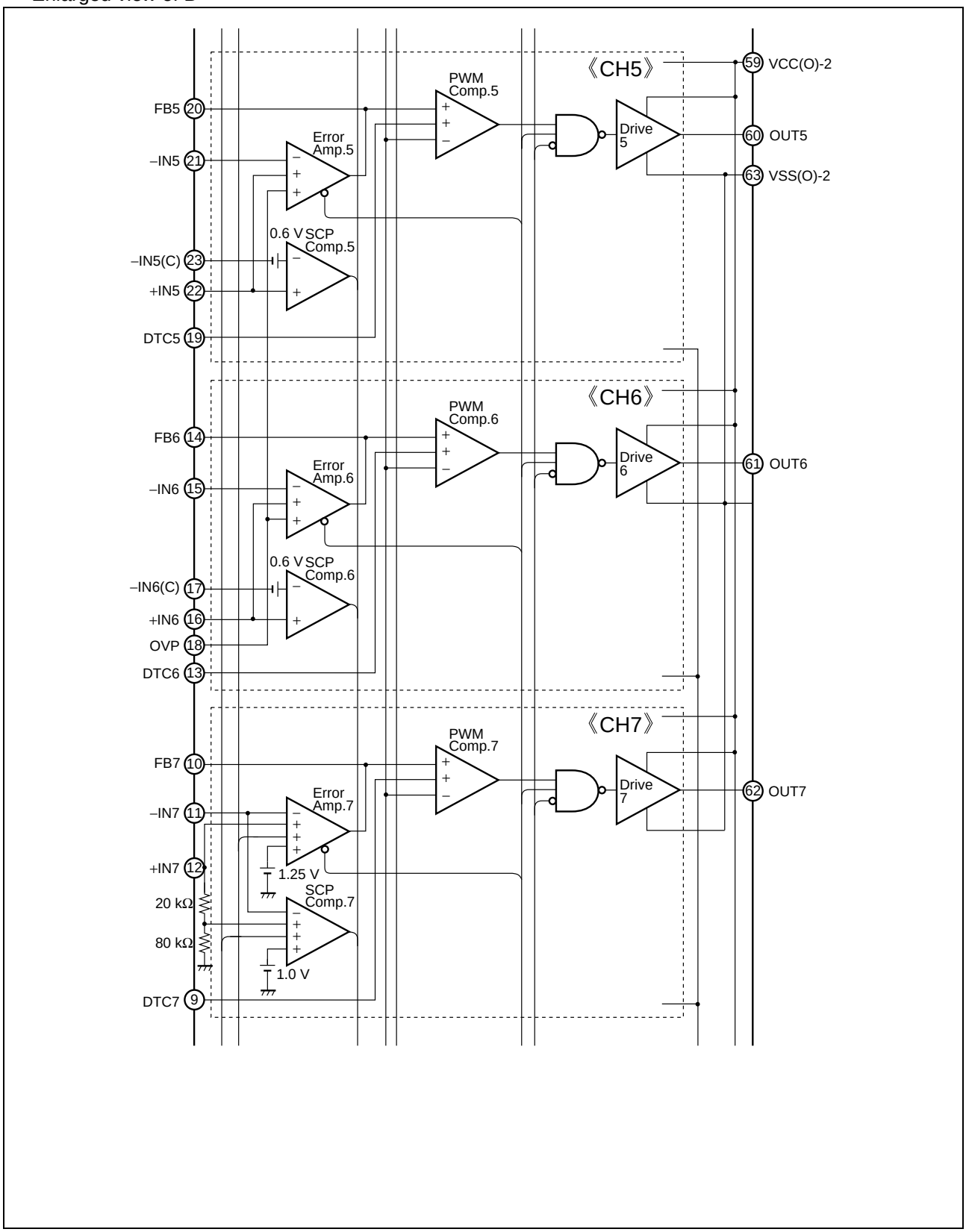
- General view



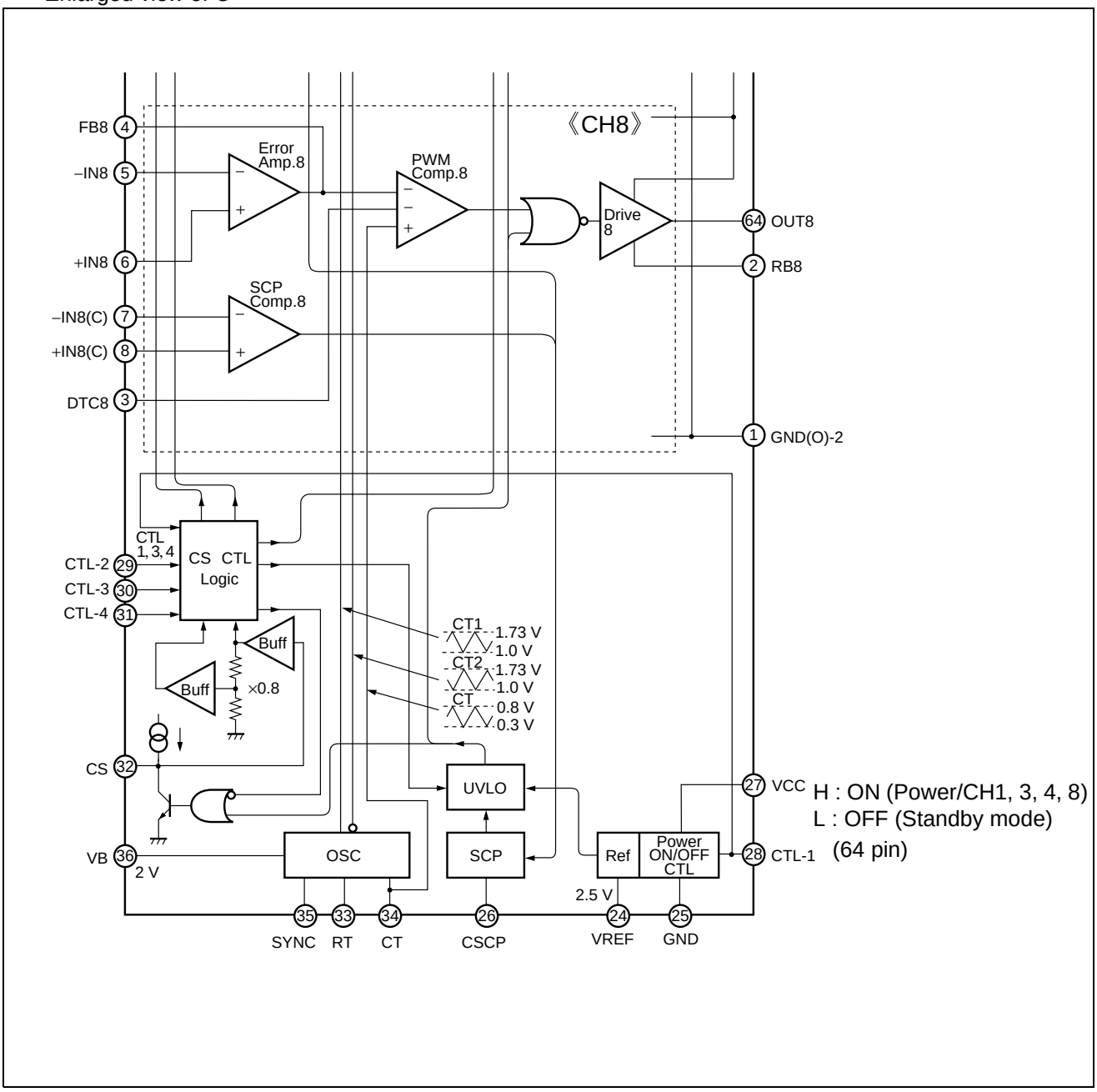
• Enlarged view of A



• Enlarged view of B



• Enlarged view of C



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating		Unit
			Min	Max	
Power supply voltage	V_{CC}	—	—	17	V
	V_{DD}	—	—	17	V
Output current	I_O	OUT pin	—	20	mA
Output peak current	I_O	OUT pin, Duty ≤ 5%	—	200	mA
Power dissipation	P_D	Ta ≤ +25 °C	—	800*	mW
Storage temperature	Tstg	—	–55	+125	°C

* : The packages are mounted on the epoxy board (10 cm × 10 cm).

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power supply voltage	V_{CC}	CH8	1.8	9	13	V
		CH1 to CH7, 4 V ≤ VCC(O)–VSS(O) ≤ 9 V	4	9	13	V
	V_{DD}	CH1	4	5	9	V
Reference voltage output current	I_{OR}	VREF pin	–1	—	0	mA
Reference voltage output current	I_B	VB pin	–0.5	—	0	mA
Input voltage	V_{IN}	+IN5, +IN6, –IN1 to –IN7, –IN5 (C) , –IN6 (C) , OVP pin	0	—	V_{CC} – 1.8	V
		+IN8, –IN8, –IN8 (C) , +IN8 (C) pin	0	—	V_{CC} – 0.9	V
		+IN7 pin	0.1	—	V_{CC} – 1.8	V
Control input voltage	V_{CTL}	CTL pin	0	—	V_{CC}	V
SYNC input voltage	V_{SYNC}	SYNC pin	0	—	V_{CC}	V
Output current	I_O	OUT pin	1	2	15	mA
Output current setting resister	R_B	RB8 pin	2.4	24	51	kΩ
Oscillator frequency	f_{OSC}	—	100	500	800	kHz
Timing capacitor	C_T	—	47	100	680	pF
Timing resistor	R_T	—	6.8	11	51	kΩ
VB pin capacitor	C_{VB}	—	0.22	0.39	—	µF
Soft-start capacitor	C_S	—	—	0.1	1.0	µF
Short detection capacitor	C_{SCP}	—	—	0.1	1.0	µF
Operating ambient temperature	Ta	—	–30	+25	+85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

(Ta = +25 °C, VCC = 9 V, VSS = 4.4 V, VDD = 5 V)

Parameter			Sym-bol	Pin No.	Conditions	Value			Unit
						Min	Typ	Max	
Reference voltage block		Reference voltage	V_{REF}	24	—	2.475	2.5	2.525	V
		Output voltage temperature stability	$\Delta V_{REF}/V_{REF}$	24	Ta = −30 °C to +85 °C	—	0.5*	—	%
		Input stability	Line	24	VCC = 4 V to 13 V	−10	—	10	mV
		Load stability	Load	24	VREF = 0 mA to −1 mA	−10	—	10	mV
		Short-circuit output current	Ios	24	VREF = 2 V	−20	−5	−1	mA
Under voltage lockout protection circuit block(U.V.L.O)	CH1 to CH7	Threshold voltage	V_{TH}	50	VCC = ↓	2.6	2.8	3.0	V
		Hysteresis width	V_H	50	—	—	0.2	—	V
		Reset voltage	V_{RST}	50	VCC = ↓	1.20	1.30	1.40	V
	CH8	Threshold voltage	V_{TH}	64	VCC = ↓	1.25	1.45	1.65	V
Soft-start block (CS)		Input standby voltage	V_{STB}	32	—	—	50	100	mV
		Charge current	I_{CS}	32	—	−1.4	−1.0	−0.6	μA
Short circuit detection block (SCP)		Threshold voltage	V_{TH}	26	—	0.65	0.70	0.75	V
		Input standby voltage	V_{STB}	26	—	—	50	100	mV
		Input latch voltage	V_I	26	—	—	50	100	mV
		Input source current	I_{CSCP}	26	—	−1.4	−1.0	−0.6	μA
Triangular wave oscillator block (OSC)		Oscillator frequency	f_{OSC}	50, 53, 56, 57, 60, 61, 62, 64, 51, 54	CT = 100 pF, RT = 11 kΩ VB = 2 V	450	500	550	kHz
		Frequency stability for voltage	Δf/fdv	50, 53, 56, 57, 60, 61, 62, 64, 51, 54	VCC = 4 V to 13 V	—	1	10	%
		Frequency stability for temperature	Δf/fdt	50, 53, 56, 57, 60, 61, 62, 64, 51, 54	Ta = −30 °C to +85 °C	—	1*	—	%
		Output voltage	V_B	36	—	1.980	2.000	2.020	V
		SYNC input condition	V_{IH}	50	Input “H” level	2.0	—	—	V
			V_{IL}	50	Input “L” level	0	—	0.8	V
		Input current	I_{SYNC}	35	SYNC = 5 V	—	50	100	μA

*: Standard design value.

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(Ta = +25 °C, VCC = 9 V, VSS = 4.4 V, VDD = 5 V)

Parameter		Sym-bol	Pin No.	Conditions	Value			Unit
					Min	Typ	Max	
Error amplifier block (CH1 to CH4, CH7)	Threshold voltage	V_{TH}	47, 44, 41, 38, 10	FB = 1.35 V	1.23	1.25	1.27	V
	V_T temperature stability	$\Delta V_T/V_T$	47, 44, 41, 38, 10	Ta = −30 °C to +85 °C	—	0.5*	—	%
	Input bias current	I_B	46, 43, 40, 37, 11	−IN = 0 V (CH1 to CH4, CH7)	−320	−60	—	nA
			12	+IN = 1 V (CH7)	8	10	15	μA
	Voltage gain	A_V	47, 44, 41, 38, 10	DC	60	100	—	dB
	Frequency bandwidth	B_W	47, 44, 41, 38, 10	A_V = 0 dB	—	1.2*	—	MHz
	Output voltage	V_{OH}	47, 44, 41, 38, 10	—	2.2	2.4	—	V
		V_{OL}	47, 44, 41, 38, 10	—	—	50	200	mV
	Output source current	I_{SOURCE}	47, 44, 41, 38, 10	FB = 1.35 V	—	−2.0	−1.0	mA
	Output sink current	I_{SINK}	47, 44, 41, 38, 10	FB = 1.35 V	70	140	—	μA
Error amplifier bolck (CH5, CH6)	Input offset voltage	V_{IO}	20, 21, 14, 15	FB = 1.35 V	—	—	10	mV
	V_T temperature stability	$\Delta V_T/V_T$	20, 21, 14, 15	Ta = −30 °C to +85 °C	—	0.5*	—	%
	Input bias current	I_B	22, 16	FB = 1.35 V	−260	−40	—	nA
			21, 15	−IN = 0 V	−120	−30	—	nA
			18	FB = 1.35 V	−120	−30	—	nA
	Common mode input voltage range	V_{CM}	20, 14	—	0	—	V_{CC} − 1.8	V
	Voltage gain	A_V	20, 14	DC	60	100	—	dB
	Frequency bandwidth	B_W	20, 14	A_V = 0 dB	—	1.2*	—	MHz
	Output voltage	V_{OH}	20, 14	—	2.2	2.4	—	V
		V_{OL}	20, 14	—	—	50	200	mV
	Output source current	I_{SOURCE}	20, 14	FB = 1.35 V	—	−2.0	−1.0	mA
	Output sink current	I_{SINK}	20, 14	FB = 1.35 V	70	140	—	μA

*: Standard design value.

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(Ta = +25 °C, VCC = 9 V, VSS = 4.4 V, VDD = 5 V)

Parameter		Sym-bol	Pin No.	Conditions	Value			Unit
					Min	Typ	Max	
Error amplifier bolck (CH8)	Input offset voltage	V_{IO}	4, 5	FB = 0.55 V	−15	0	15	mV
	Input bias current	I_B	6	+IN = 0 V	−100	−20	—	nA
			5	FB = 0.55 V	−50	−10	—	nA
	Common mode input voltage range	V_{CM}	4	—	0	—	V_{CC} − 0.9	V
	Voltage gain	A_V	4	DC	60	75	—	dB
	Frequency bandwidth	B_W	4	AV = 0 dB	—	1.2*	—	MHz
	Output voltage	V_{OH}	4	—	1.1	1.3	—	V
		V_{OL}	4	—	—	5	200	mV
	Output source current	I_{SOURCE}	4	FB = 0.55 V	—	−2.0	−1.0	mA
	Output sink current	I_{SINK}	4	FB = 0.55 V	60	140	—	µA
SCP Comp. block (CH1 to CH4, SCP)	Threshold voltage	V_{TH}	50, 53, 56, 57	CH1 to CH4	0.97	1.00	1.03	V
			62	+IN = 1 V (CH7)	0.77	0.80	0.83	V
	Input bias current	I_B	46, 43, 40, 11, 37	−IN = 0 V	−320	−60	—	nA
SCP Comp. block (CH5,CH6 SCP)	Input offset voltage	V_{IO}	60, 61	—	0.55	0.60	0.65	V
	Input bias current	I_B	23, 17	−IN (C) = 0 V	−200	−40	—	nA
	Common mode input voltage range	V_{CM}	60, 61	—	0	—	V_{CC} − 1.8	V
SCP Comp. block (CH8 SCP)	Input offset voltage	V_{IO}	64	—	−15	0	15	mV
	Input bias current	I_B	7	FB = 0.55 V	−50	−10	—	nA
	Common mode input voltage range	V_{CM}	64	—	0	—	V_{CC} − 0.9	V
PWM Comp. block (CH1 to CH7)	Threshold voltage	V_{T0}	50	Duty cycle = 0%	0.9	1.0	—	V
		V_{T100}	50	Duty cycle = 100%	—	1.73	1.83	V
	Input bias current	I_{DTC}	48, 45, 42, 39, 19, 13, 9	DTC = 0.4 V (CH1 to CH7)	−1.0	−0.3	—	µA

*: Standard design value.

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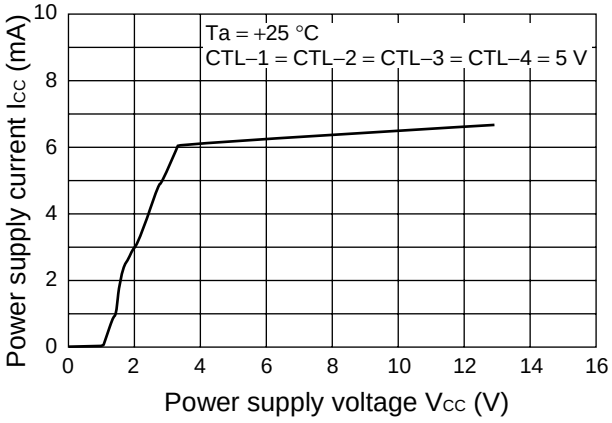
(Ta = +25 °C, VCC = 9 V, VSS = 4.4 V, VDD = 5 V)

Parameter		Sym-bol	Pin No.	Conditions	Value			Unit
					Min	Typ	Max	
PWM Comp. block(CH8)	Threshold voltage	V_{T0}	64	Duty cycle = 0%	0.2	0.3	—	V
		V_{T100}	64	Duty cycle = 100%	—	0.8	0.9	V
Output block (CH1 to CH7) (Drive-1)	Output source current	I_{SOURCE}	50, 53, 56, 57, 60, 61, 62	Duty ≤ 5%, OUT = 4.4 V	—	−100	—	mA
	Output sink current	I_{SINK}	50, 53, 56, 57, 60, 61, 62	Duty ≤ 5%, OUT = 9 V	—	80	—	mA
	Output ON resistor	R_{OH}	50, 53, 56, 57, 60, 61, 62	OUT = −15 mA	—	22	35	Ω
		R_{OL}	50, 53, 56, 57, 60, 61, 62	OUT = 15 mA	—	17	26	Ω
Output block (CH1, CH2) (Drive-2)	Output source current	I_{SOURCE}	51, 54	Duty ≤ 5%, OUT = 0 V	—	−110	—	mA
	Output sink current	I_{SINK}	51, 54	Duty ≤ 5%, OUT = 5 V	—	100	—	mA
	Output ON resistor	R_{OH}	51, 54	OUT = −15 mA	—	20	32	Ω
		R_{OL}	51, 54	OUT = 15 mA	—	16	25	Ω
Output block (CH8) (Drive)	Output source current	I_{SOURCE}	64	RB = 24 kΩ, OUT = 0.7 V	−2.6	−2.0	−1.4	mA
	Output sink current	I_{SINK}	64	Duty ≤ 5%, OUT = 0 V	—	40	—	mA
Output block (CTL-1 to CTL-4) (CTL)	CTL input condition	V_{IH}	28, 29, 30, 31	Active mode	1.5	—	13	V
		V_{IL}	28, 29, 30, 31	Standby mode	0	—	0.5	V
	Input current	I_{CTL}	28, 29, 30, 31	CTL = 5 V	—	100	200	μA
General	Standby current	I_{CCS}	27	CTL-1 = 0 V	—	—	10	μA
		$I_{CCS(O)}$	58, 59	CTL-1 = 0 V	—	—	10	μA
		I_{DDS}	52	CTL-1 = 0 V	—	—	10	μA
	Power supply current	I_{CC}	27, 58, 59	CTL-1 = CTL-2 = CTL-3 = CTL-4 = 5 V	—	7	11	mA
		I_{DD}	52	CTL-1 = CTL-2 = CTL-3 = CTL-4 = 5 V	—	—	10	μA

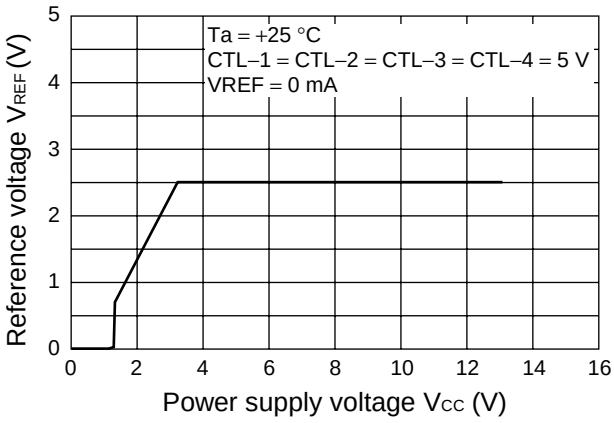
*: Standard design value.

■ TYPICAL CHARACTERISTICS

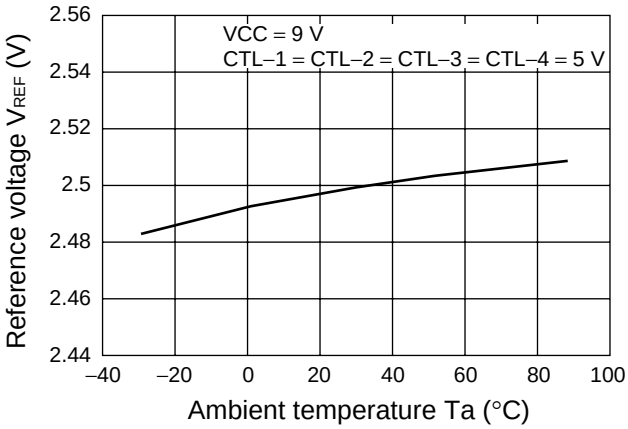
Power supply current vs. power supply voltage



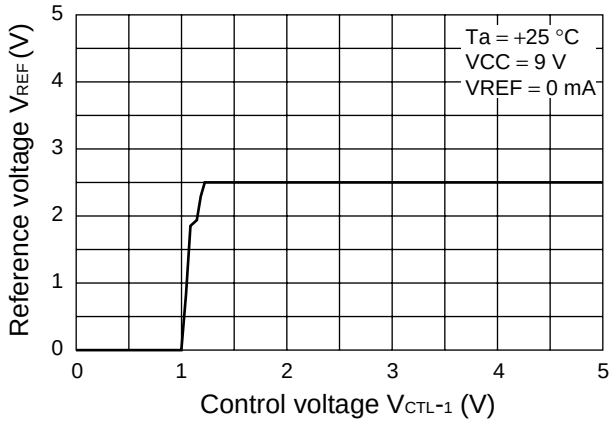
Reference voltage vs. power supply voltage



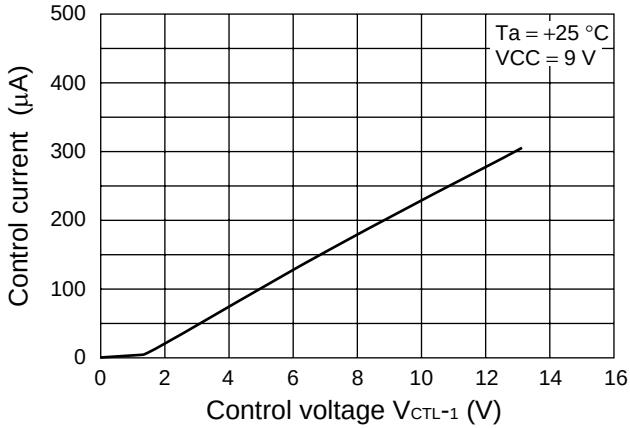
Reference voltage vs. ambient temperature



Reference voltage vs. control voltage



Control current vs. control voltage



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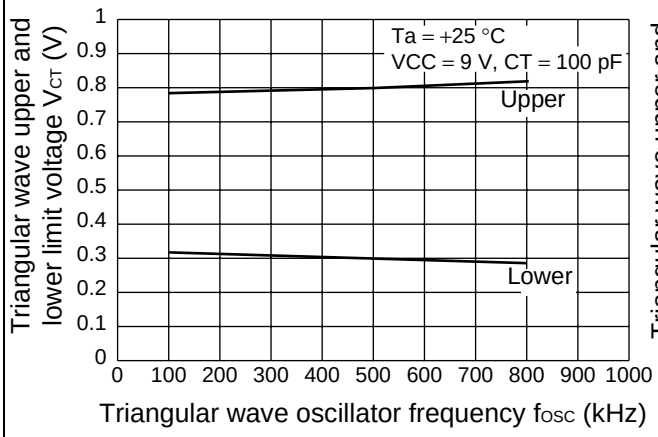
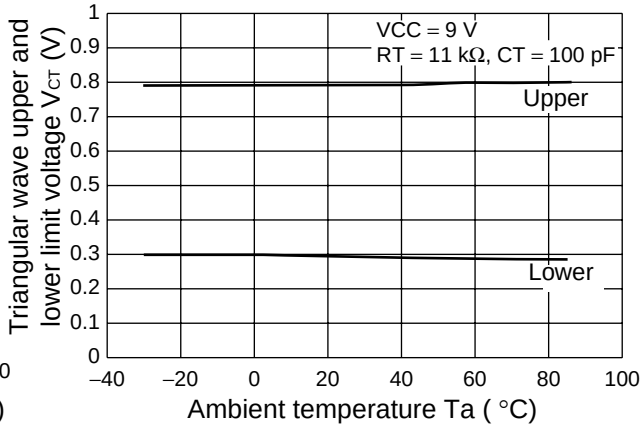
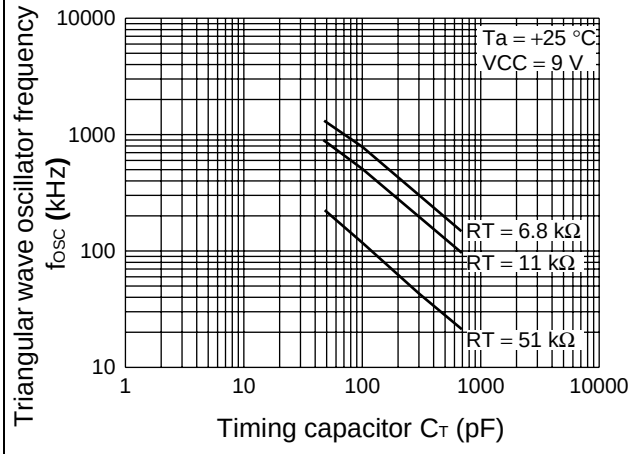
Triangular wave upper and lower limit voltage vs.triangular wave oscillator frequency



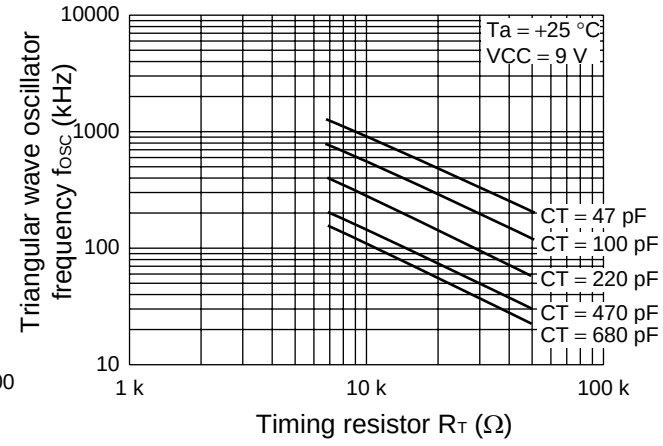
Triangular wave upper and lower limit voltage vs. ambient temperature



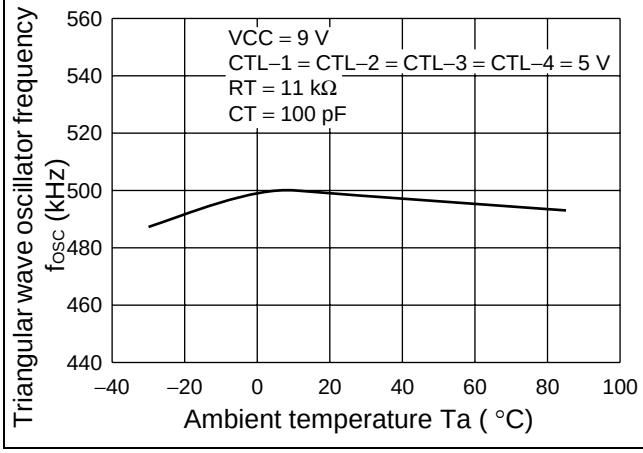
Triangular wave oscillator frequency vs. timing capacitor



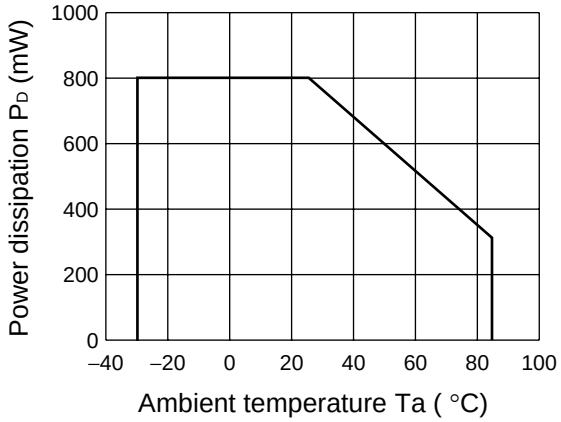
Triangular wave oscillator frequency vs. timing resistor



Triangular wave oscillator frequency vs. ambient temperature



Power dissipation vs. ambient temperature



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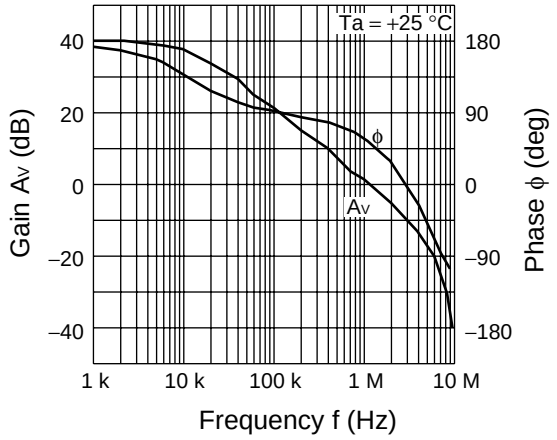
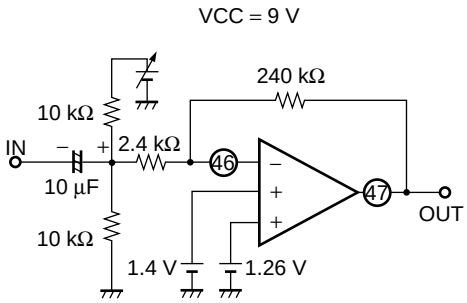
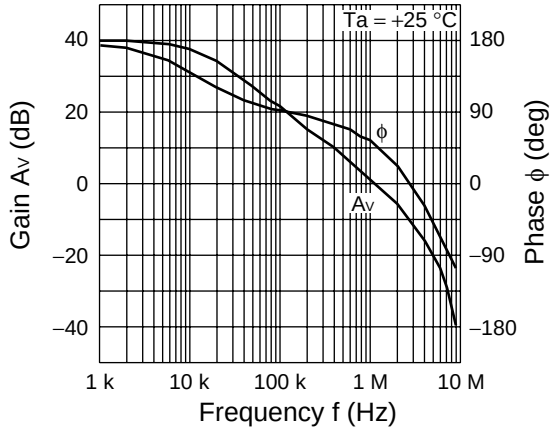
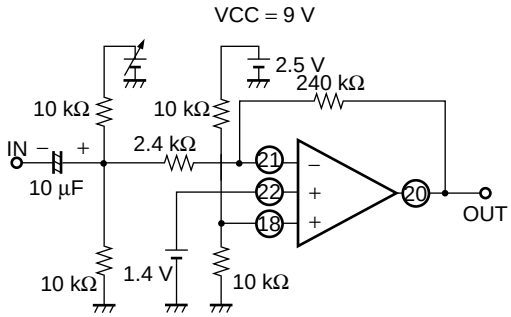
Error amplifier gain and phase vs. frequency (CH1)



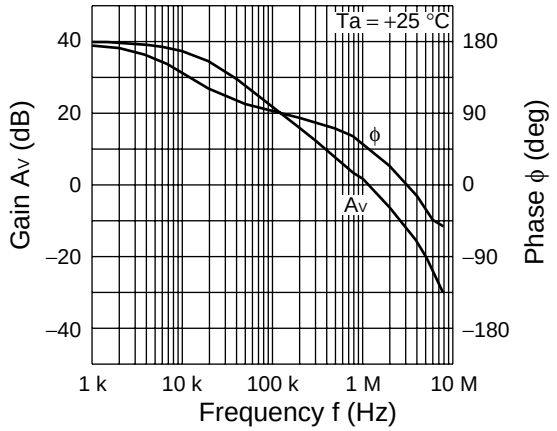


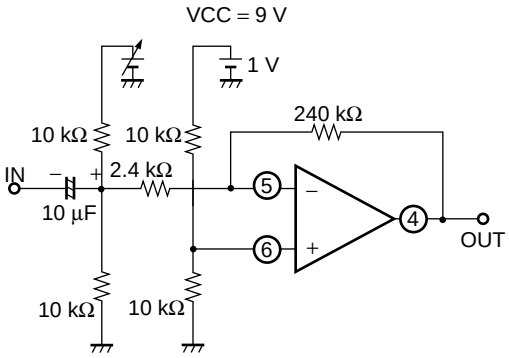
Error amplifier gain and phase vs. frequency (CH5)





Error amplifier gain and phase vs. frequency (CH8)





■ FUNCTIONS

1. DC-DC Converter Functions

(1) Reference voltage generator

The reference voltage generator generates a temperature-compensated reference voltage (typically ≒ 2.5 V) from the voltage supplied from the power supply terminal (pin 27). The voltage is used as the reference voltage for the IC's internal circuitry.
The reference voltage can supply a load current of up to 1 mA to an external device through the VREF terminal (pin 24).

(2) Triangular-wave oscillator circuit

The triangular wave oscillator incorporates a timing capacitor and a timing resistor connected respectively to the CT terminal (pin 34) and RT terminal (pin 33) to generate triangular oscillation waveform CT (amplitude of 0.3 to 0.8 V), CT1 (amplitude 1.0 to 1.73 V in phase with CT), or CT2 (amplitude 1.0 to 1.73 V in inverse phase with CT).
CT1 and CT2 are input to the PWM comparator in the IC.

(3) Error amplifier (Error Amp.)

The error amplifier detects the DC/DC converter output voltage and outputs PWM control signals. It supports a wide range of in-phase input voltages from 0 V to "V_{CC} - 1.8 V" (channels 1 to 7), allowing easy setting from the external power supply.
In addition, an arbitrary loop gain can be set by connecting a feedback resistor and capacitor from the output pin to inverted input pin of the error amplifier, enabling stable phase compensation to the system.

(4) PWM comparator (PWM Comp.)

The PWM comparator is a voltage-to-pulse width converter for controlling the output duty depending on the input voltage.

Channels 1, 2 main sides, channel 3 to 8 : The comparator keeps the output transistor on while the error amplifier output voltage and DTC voltage remain higher than the triangular wave voltage.

Channels 1, 2 synchronous rectification sides: The comparator keeps the output transistor on while the error amplifier output voltage remain lower than the triangular wave voltage.

(5) Output circuits

The output circuits on the main side and on the synchronous rectification side are both in the totem pole configuration, capable of driving an external PNP transistor (channels 1,2 main sides, channels 3 to 7), NPN transistor (channel 8), and N-channel MOSFET (channels 1,2 synchronous rectification sides).

2. Channel Control Function

Channels are turned on and off depending on the voltage levels at the CTL-1 terminal (pin 28), CTL-2 terminal (pin 29), CTL-3 terminal (pin 30),and CTL-4 terminal (pin 31).

Channel On/Off Setting Conditions

Voltage level at CTL pin				Channel on/off state				
CTL-1	**CTL-2**	**CTL-3**	**CTL-4**	**Power**	**CH8 CH1, 3, 4**	**CH2**	**CH5, 6**	**CH7**
L	×	×	×	OFF (Standby state)				
H	L	L	L	ON		OFF	OFF	OFF
			H					ON
		H	L				ON	OFF
			H					ON
	H	L	L			ON	OFF	OFF
			H					ON
		H	L				ON	OFF
			H					ON

× : Undefined

3. Protective Functions

(1) Timer-latch short-circuit protection circuit

The short-circuit detection comparator in each channel detects the output voltage level and, if any channel output voltage falls below the short-circuit detection voltage, the timer circuits is actuated to start charging the external capacitor C_{SCP} connected to the CSCP terminal (pin 26).
When the capacitor voltage reaches about 0.70 V, the circuit is turned off the output transistor and sets the dead time to 100%.
To reset the actuated protection circuit, turn the power supply on back. (See “SETTING TIME CONSTANT FOR TIMER-LATCH SHORT-CIRCUIT PROTECTION CIRCUIT”.)

(2) Undervoltage lockout protection circuit

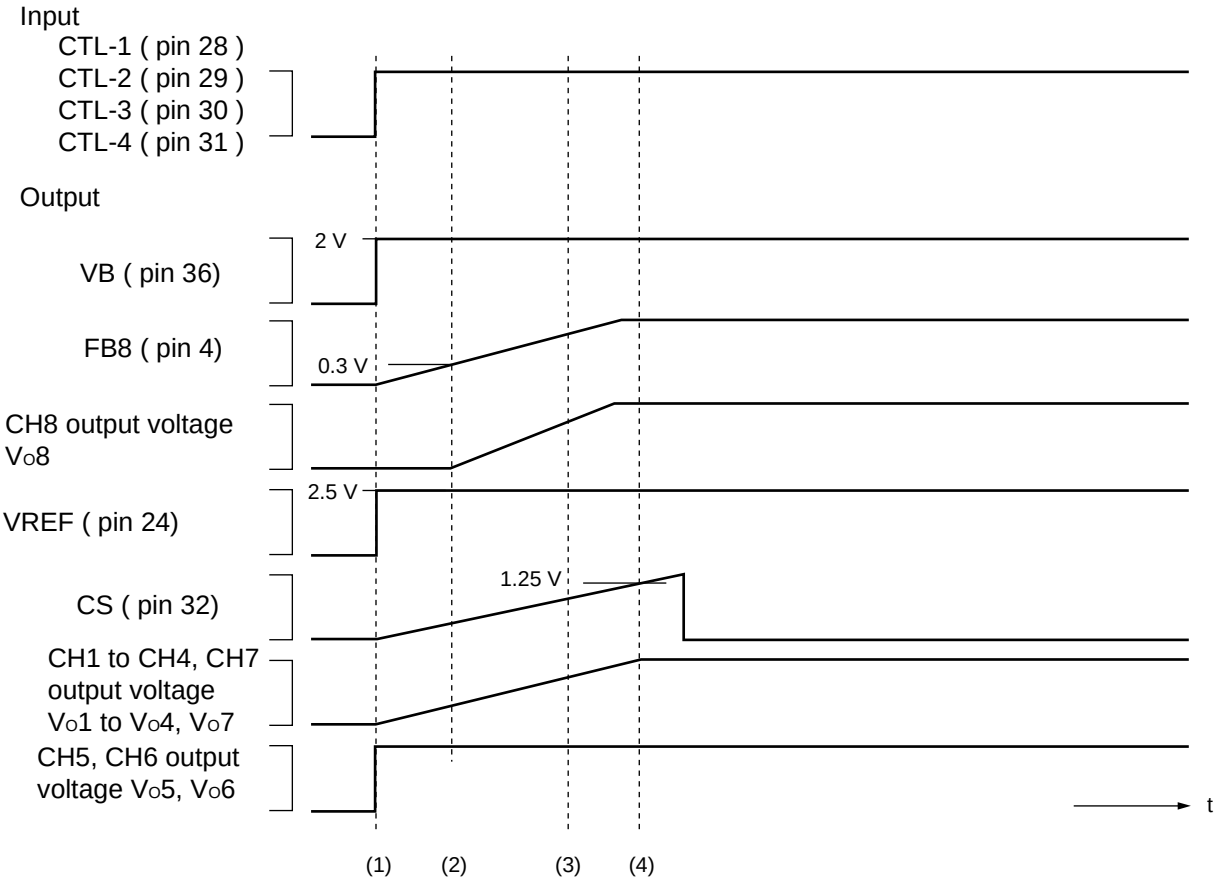
The transient state or a momentary decrease in supply voltage, which occurs when the power supply is turned on, may cause the IC to malfunction, resulting in breakdown or degradation of the system. To prevent such malfunctions, the undervoltage lockout protection circuit detects a decrease in internal reference voltage with respect to the power supply voltage, turns off the output transistor, and sets the dead time to 100% while holding the CSCP terminal (pin 26) at the “L” level.
The circuit restores the output transistor to normal when the supply voltage reaches the threshold voltage of the undervoltage lockout protection circuit.

4. Soft-Start Operation

(1) Description

- When the CTL-1 to CTL-4 pins are driven high (“H” level)

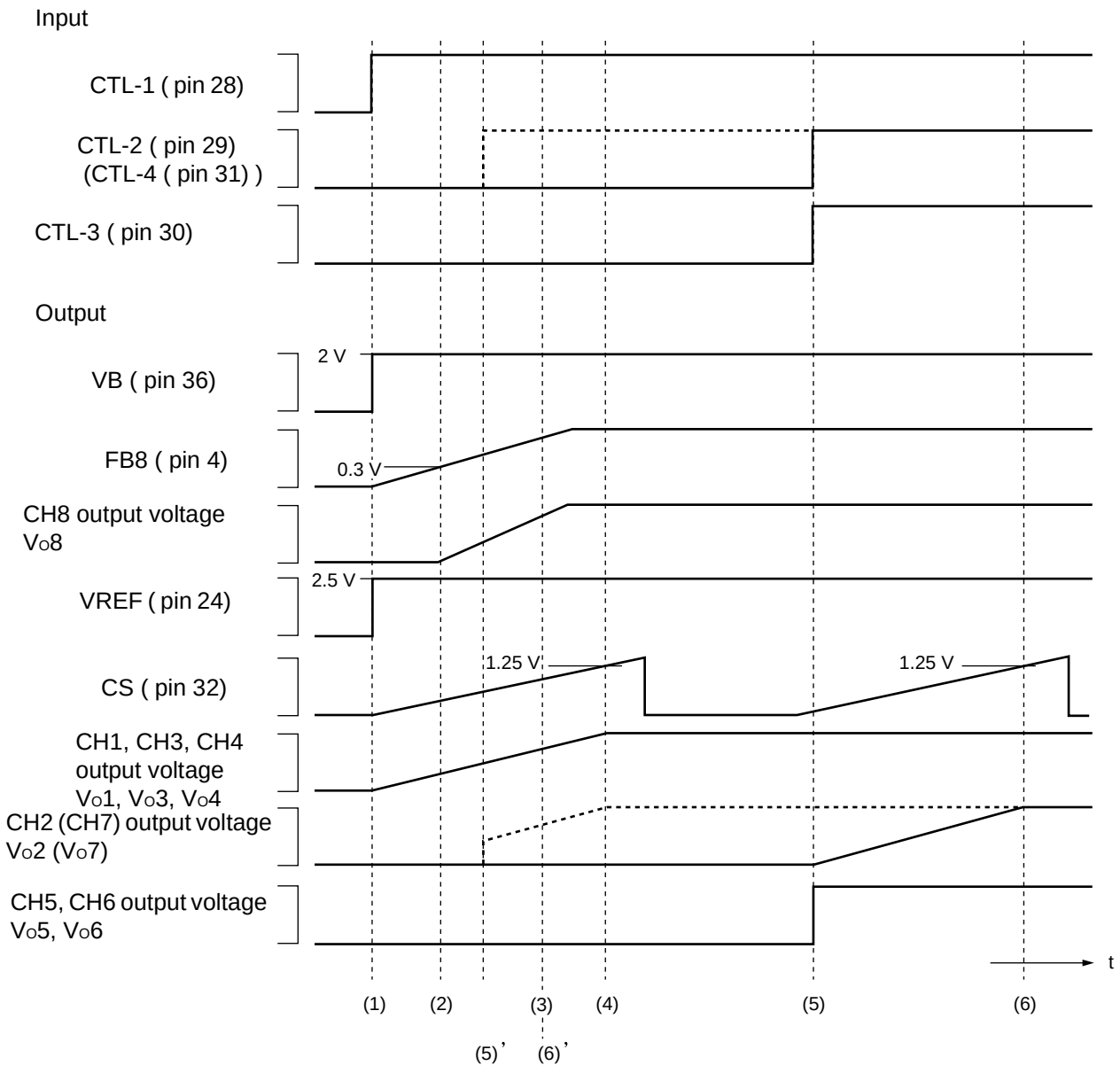
The channel-8 output voltage is soft-started by the capacitor (C_{+IN8}) connected to the +IN8 terminal (pin 6). The capacitor (Cs) connected to the CS terminal (pin 32) starts being charged and the output voltages of channels 1 to 4 and channel 8 are soft-started by the error amplifier in proportion to the CS pin voltage.



(1) to (4) : CH1 to CH4, CH7 soft-start interval
(2) to (3) : CH8 soft-start interval

• When the CTL-2 (CTL-4) terminal is driven low (“L” level) after channels 1, 3, 4, and 8 have been soft-started

The capacitor (Cs) connected to the CS terminal (pin 32) starts being charged. The channel-2 (channel-7) output voltage is soft-started by the error amplifier in proportion to the CS pin voltage.



(1) to (4) : Channel-1, 3, 4 soft-start interval
(2) to (3) : Channel-8 soft-start interval
(5) to (6) : Channel-2 (channel-7) soft-start interval
(5)’ to (6)’ : Channel-2 (channel-7) soft-start interval (waveform) as CTL-2 (CTL-4) goes “H” from “L” during channel-1, 3, 4 soft-start interval

(2) Setting Soft-start

- Channel-8 soft-start

Channel 8 can be soft-started by connecting a capacitor between the DTC8 terminal (pin 3) and GND. The soft-start time depends on the input voltage and load current.

- Channel 1 to 4 and channel 7 soft-start

Soft-start time

$ts[s] \fallingdotseq 1.25 \times Cs[\mu F]$

Note : The short-circuit detection function remains working even during soft-start operation of channels 1 to 4 and 7.

- Channel-5, 6 soft-start

Channel 5 can be soft-started by connecting a capacitor between the +IN5 terminal (pin 22) and GND.

Channel 6, like channel 5, can be soft-started by connecting a capacitor between the +IN6 terminal (pin 16) and GND.

■ SETTING THE OSCILLATION FREQUENCY

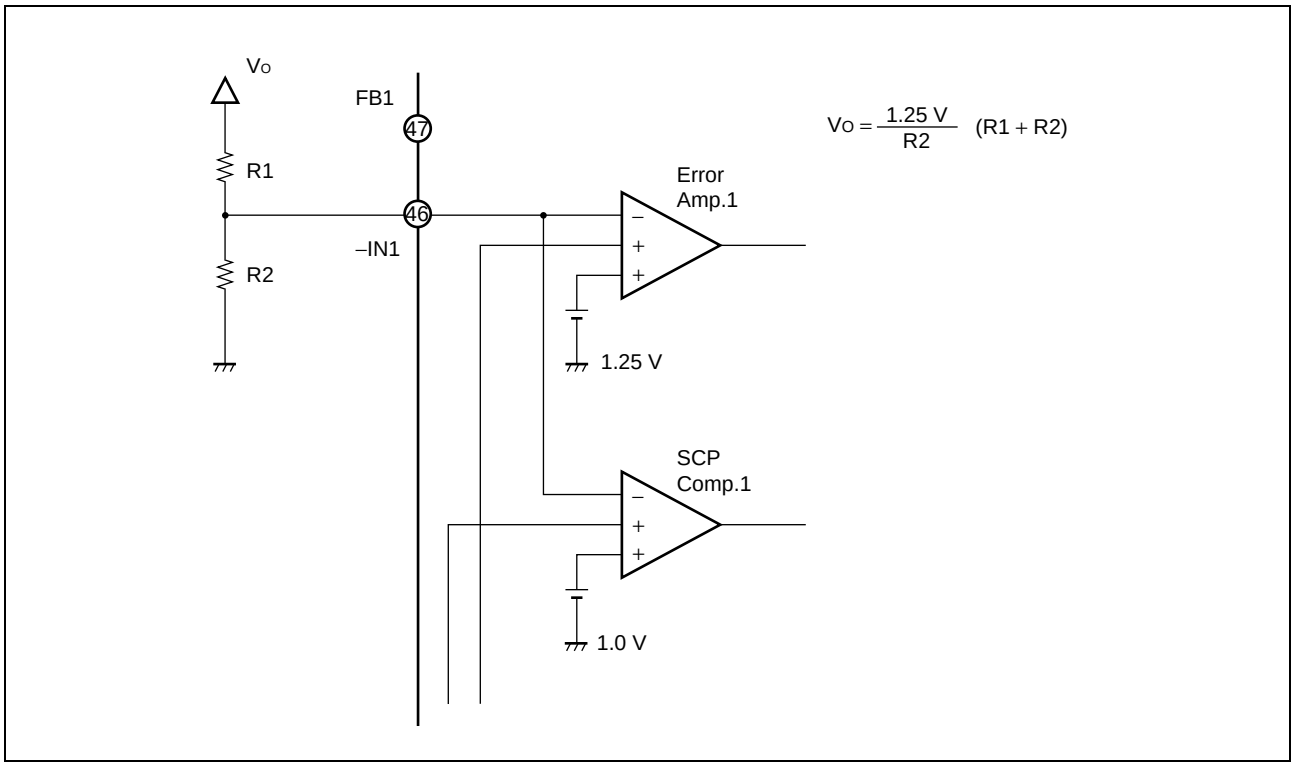
The oscillation frequency can be set by connecting the timing capacitor (C_T) to the CT terminal (pin 34) and the timing resistor (R_T) to the RT terminal (pin 33).

Oscillation frequency

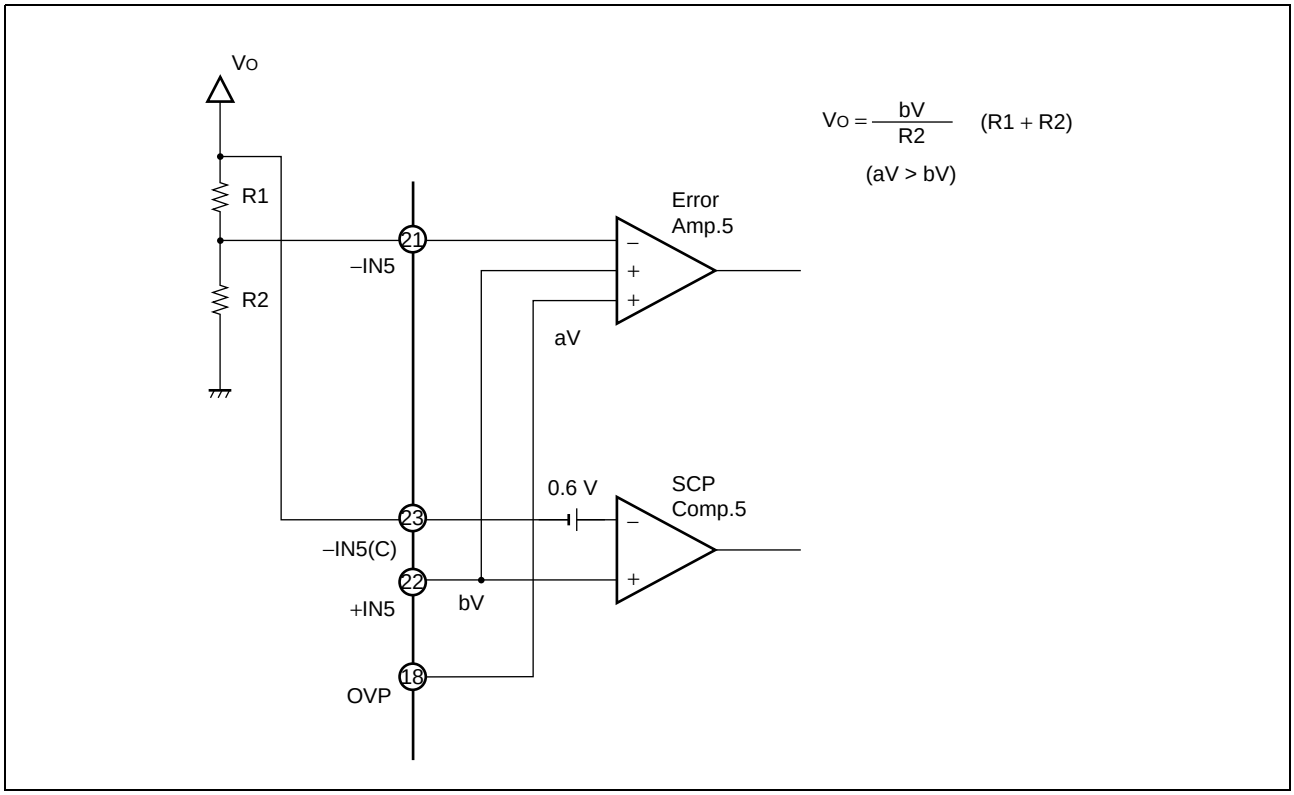
$$f_{OSC}\,(kHz) \fallingdotseq \frac{550000}{C_T\,(pF) \times R_T\,(k\Omega)}$$

■ SETTING THE OUTPUT VOLTAGE

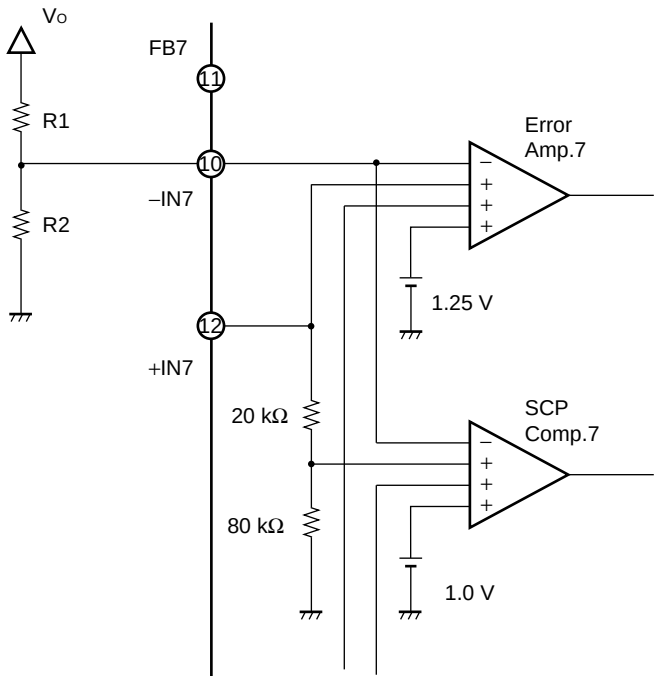
• CH1 to CH4



• CH5, CH6



• CH7



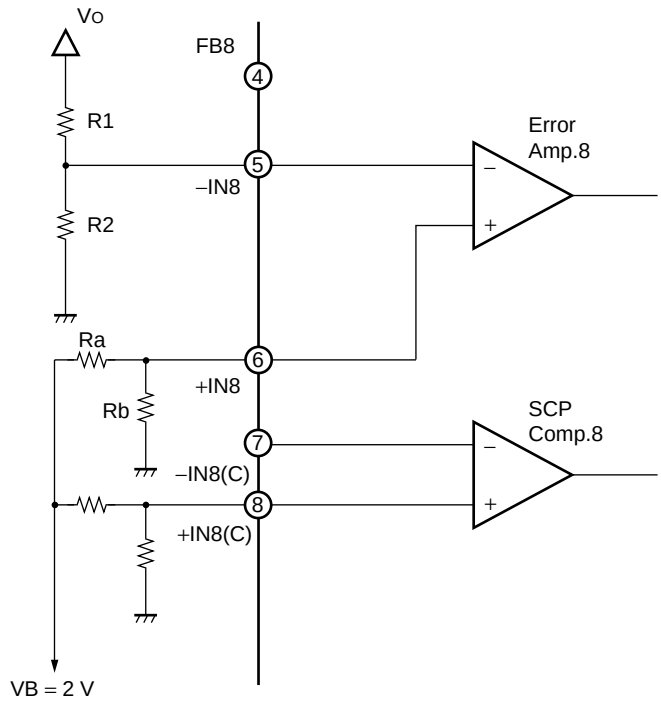
• +IN7 ≥ 1.25 V

$$V_O = \frac{1.25\ V}{R2}\ (R1 + R2)$$

• +IN7< 1.25 V

$$V_O = \frac{+IN7}{R2}\ (R1 + R2)$$

• CH8

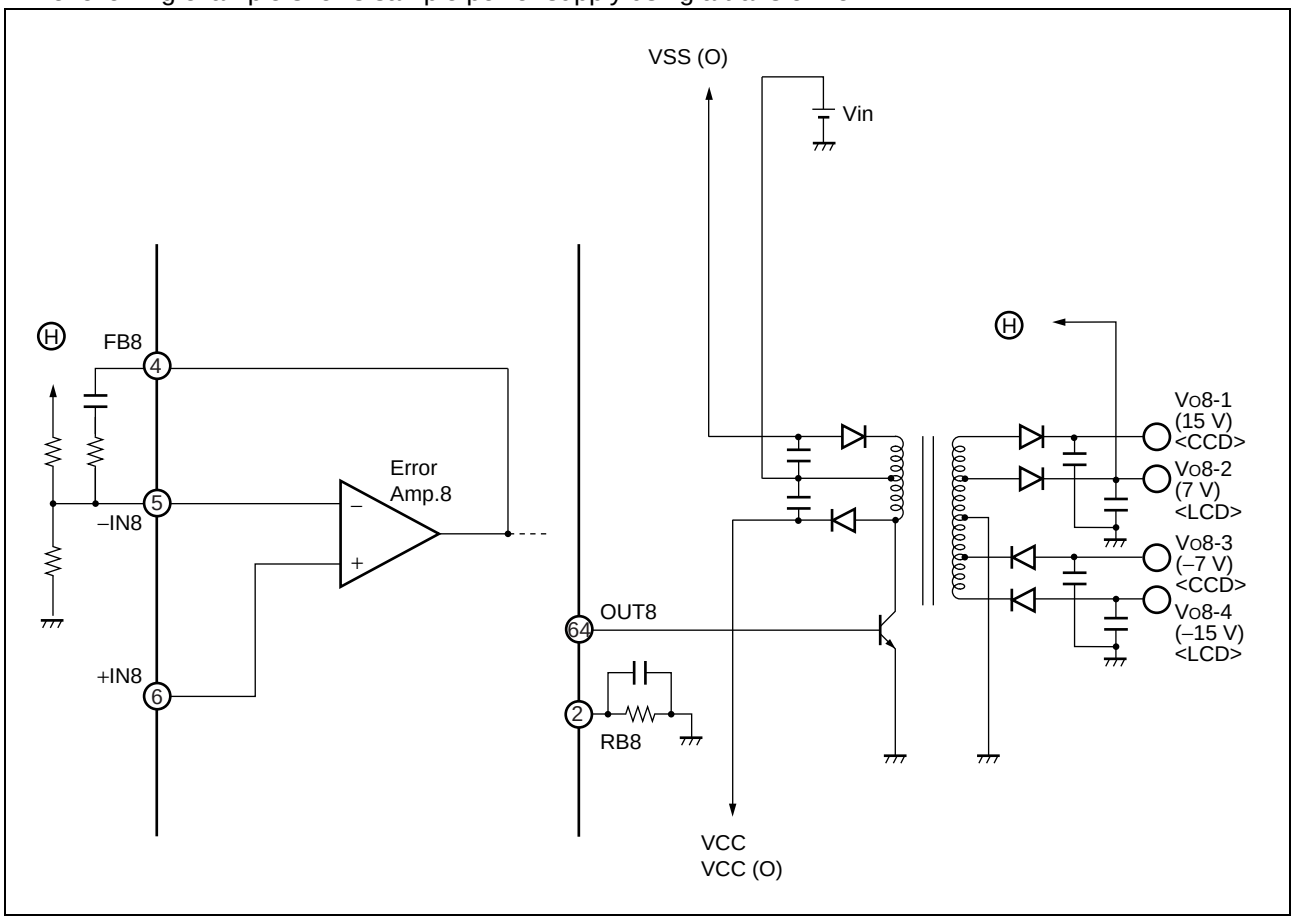


$$V_O = \frac{2Rb\ (R1 + R2)}{(Ra + Rb)\ R2}$$

■ SAMPLE POWER SUPPLY USING CHANNEL 8 AS SELF-POWER SUPPLY

Using channel 8 as the self-power supply, the MB3881 can support a wide range of supply voltages and operate at low input voltage (Vin ≥ 1.8 V).

The following example shows sample power supply using a transformer.



The following settings are used in “APPLICATION EXAMPLE”.

- VSS(O) is set to the number of turnings that produces Vin - 1.8 V.
- VCC and VCC(O) are set to the number of turnings that produces Vin + 2.2 V.

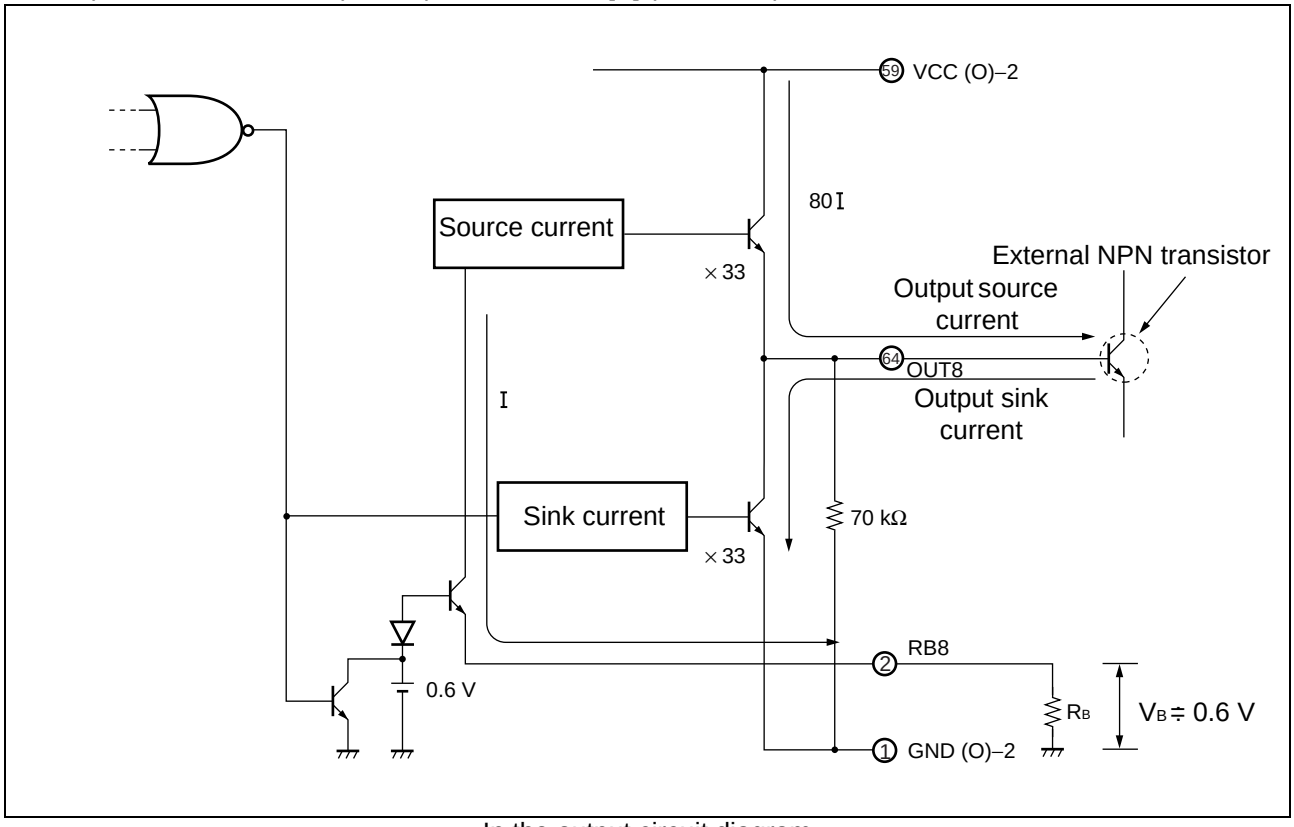
Note that, because channels 1 to 4 operate at VCC ≥ 4 V, they must be set to the number of turnings that produces Vin + 2.2 V or more so that they operate at Vin ≥ 1.8 V.

■ SETTING THE OUTPUT CURRENT

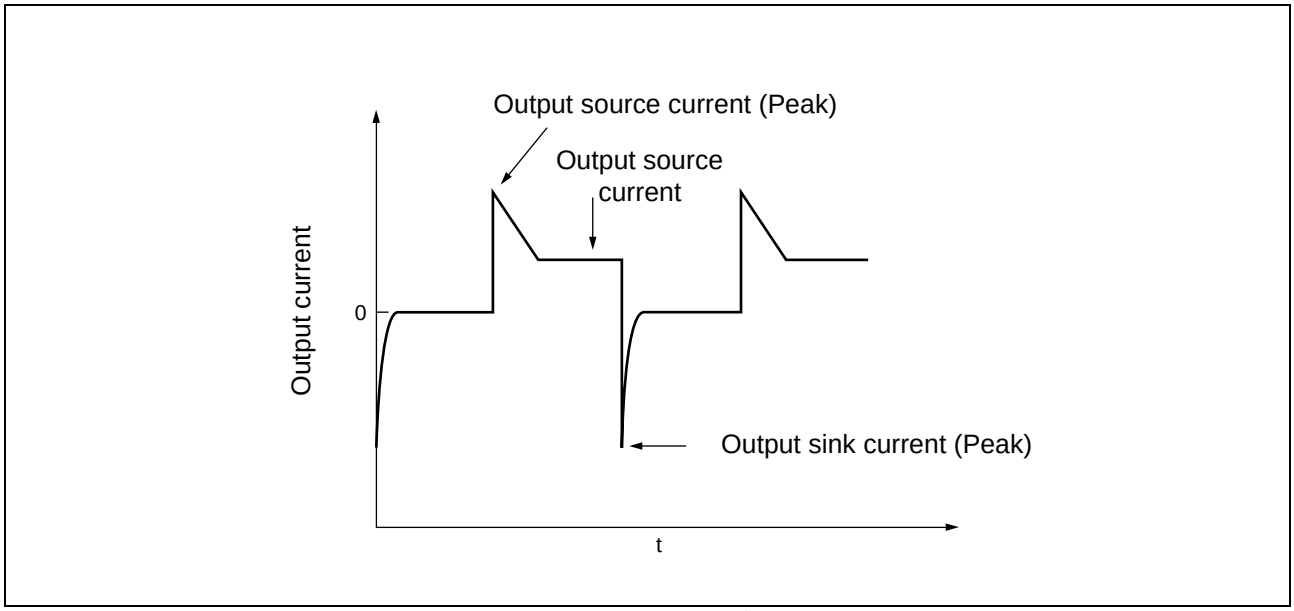
The output circuit (drive 8) is structured as illustrated below (in the output circuit diagram). As found in “Output Current Waveform” below, the source current value of the output current waveform has a constant current setting.

Note that the source current is set by the following equation:

Output source current : $(V_B / R_B) \times 80 \fallingdotseq 48 / R_B[A]$ ($V_B \fallingdotseq 0.6$ V)



In the output circuit diagram



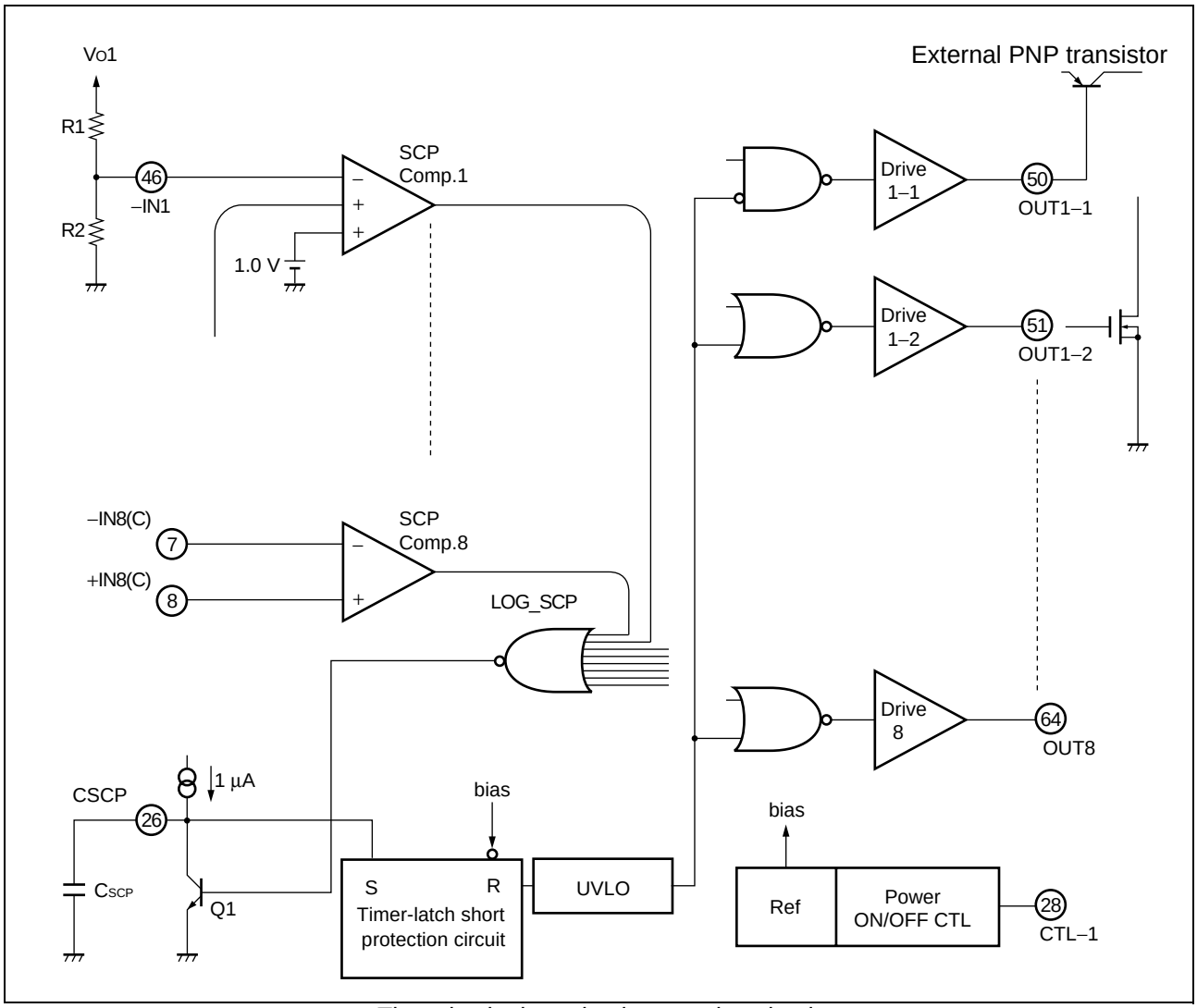
Output current waveform

■ SETTING TIME CONSTANT FOR TIMER-LATCH SHORT-CIRCUIT PROTECTION CIRCUIT

The short detection comparator (SCP comparator) in each channel monitors the output voltage.
While the switching regulator load conditions are stable on all channels, the LOG_SCP output remains at "H" level, transistor Q1 is turned on, and the CSCP terminal (pin 26) is held at “L” level.
If the load condition on a channel changes rapidly due to a short of the load, causing the output voltage to drop, the output of the short detection comparator on that channel goes to “H” level. This causes transistor Q1 to be turned off and the external short protection capacitor C_{SCP} connected to the CSCP terminal to be charged at 1.0 μA.
When the capacitor C_{SCP} is charged to the threshold voltage (VTH ≒ 0.70 V), the latch is set and the external FET is turned off (dead time is set to 100%). At this point, the latch input is closed and the CSCP terminal is held at “L” level.

Short detection time (t_{PE})

$$t_{PE}\ (s) \fallingdotseq 0.70 \times C_{SCP}\ (\mu F)$$

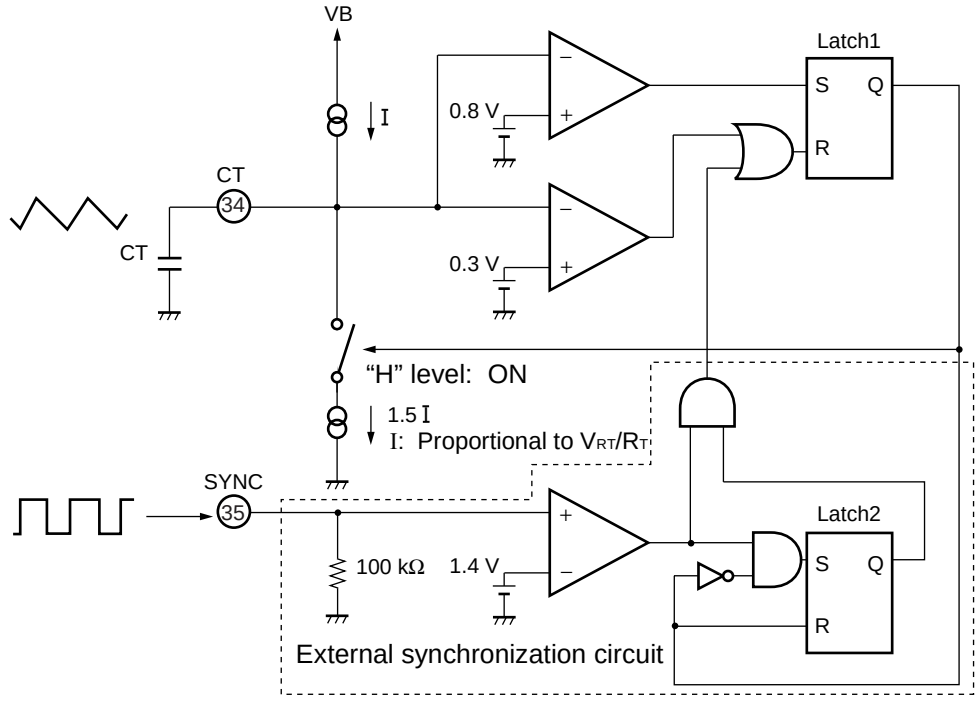


Timer-latch short circuit protection circuit

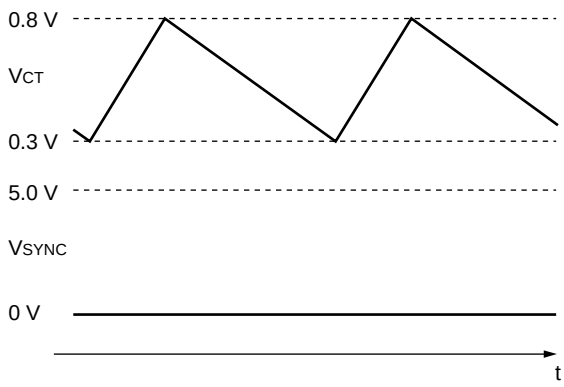
■ SETTING FOR EXTERNAL SYNCHRONOUS OSCILLATION

For external synchronous operation, connect the timing capacitor (C_T) to the CT terminal (pin 34) and the timing resistor (R_T) to the RT terminal (pin 33).
In this case, select the C_T and R_T so that the oscillation frequency is 5% to 10% lower than the frequency of the external synchronous signal excluding the setting error of the oscillation frequency.
The duty cycle (T1/T) of the external synchronous signal must be set within a range from 10% to 90%.

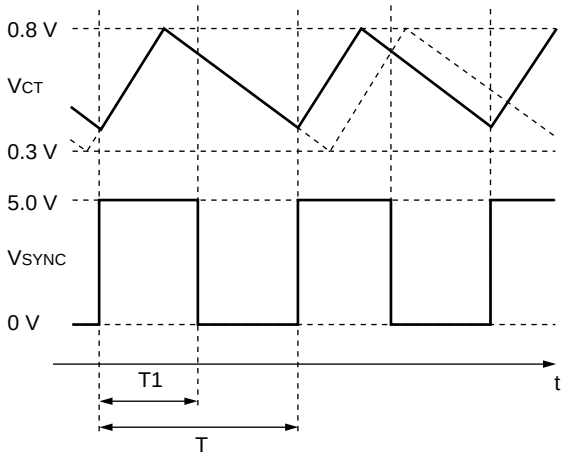
Triangular wave oscillator (OSC) equivalent circuit



Free-run oscillation



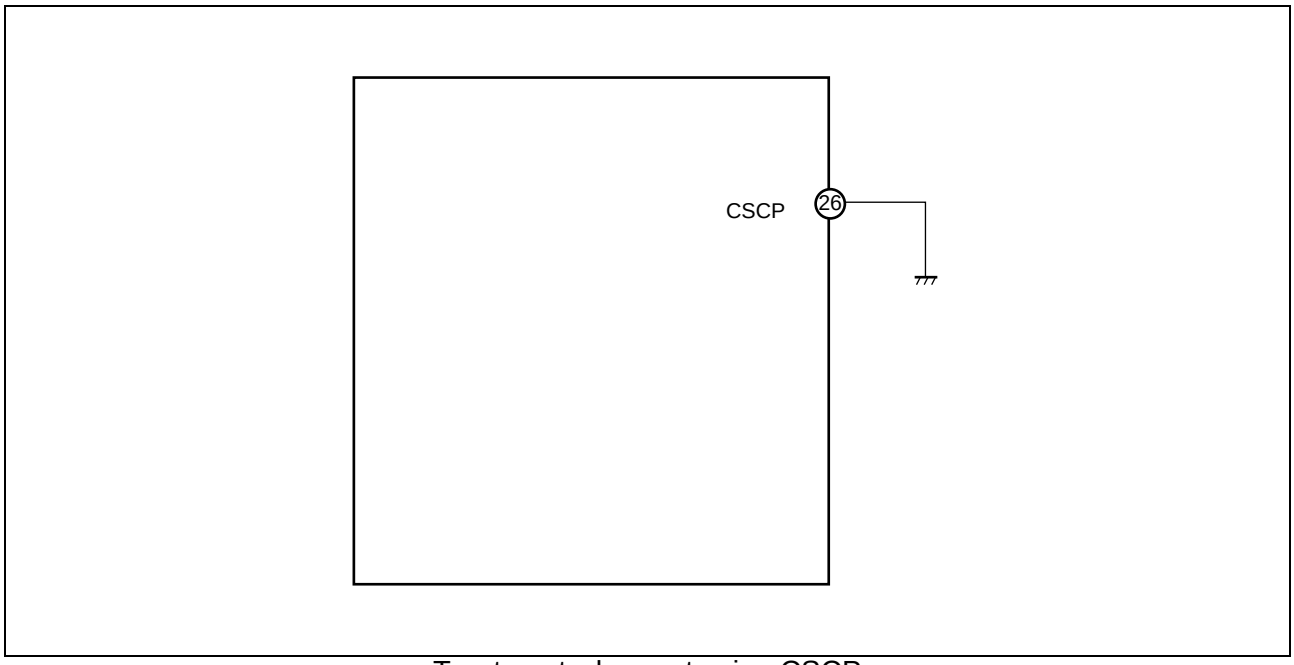
External synchronous oscillation



Note: If the external synchronous pulse is not input, the device is started with free-run oscillation.
For free-run oscillation, set the SYNC terminal (pin 35) to "Lo" or "HiZ" level.
The external synchronization circuit starts operation after a VREF rise.
The CT pin oscillation frequency at startup is 500 kHz when the voltage at the VB terminal (pin 36) is 2 V with CT = 100 pF and RT = 11 kΩ.
If the triangular wave has superimposed noise during external synchronous oscillation, insert a CR filter.

■ TREATMENT WITHOUT USING CSCP

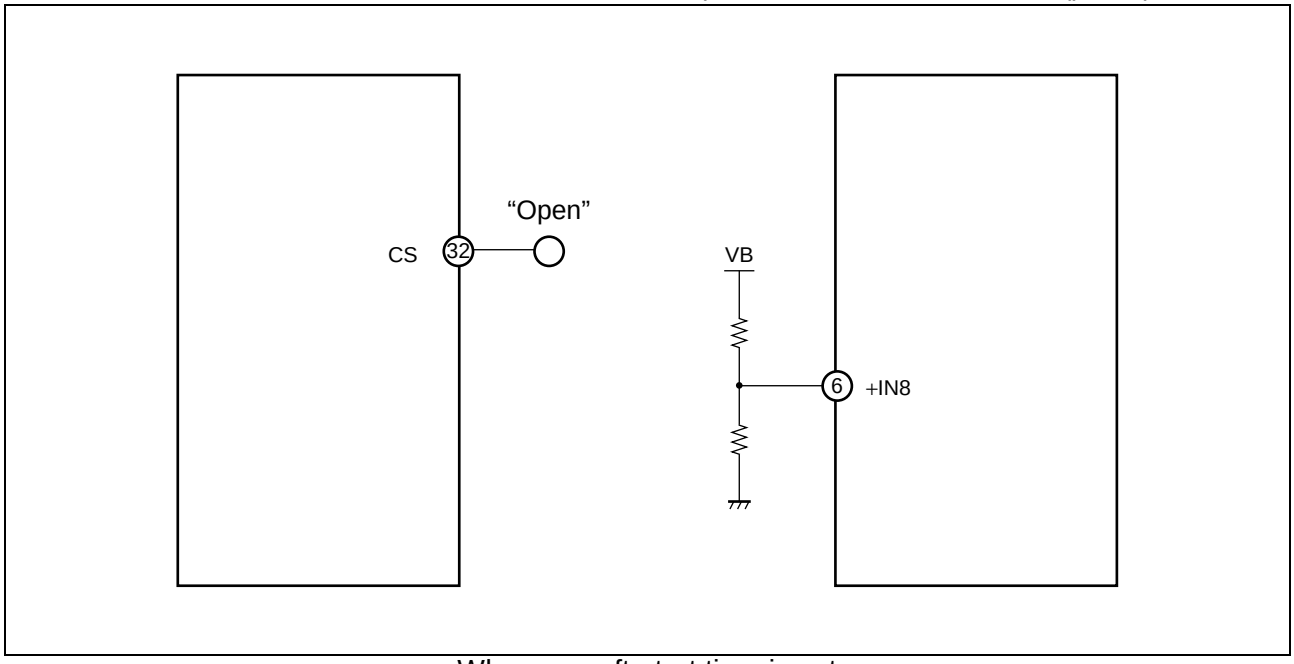
When you do not use the timer-latch short protection circuit, connect the CSCP terminal (pin 26) to GND with the shortest distance



Treatment when not using CSCP

■ TREATMENT FOR KILLING THE SOFT-START FEATURE

To disable the channel 1 to 4, 7 soft-start function, leave the CS terminal (pin 32) open.
To disable the channel 8 soft-start function, remove the capacitor from the +IN8 terminal (pin 16).



When no soft-start time is set

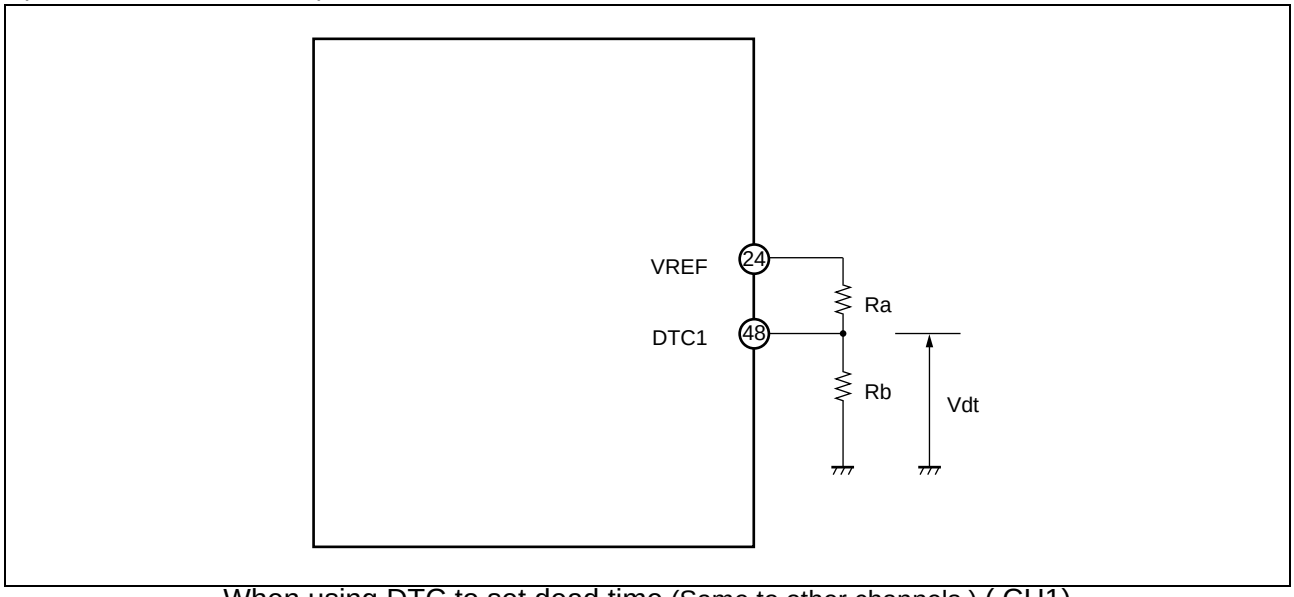
■ SETTING THE DEAD TIME

When the device is set for step-up inverted output based on the step-up or step-up/down Zeta method or flyback method, the FB pin voltage may reach and exceed the rectangular wave voltage due to load fluctuation. If this is the case, the output transistor is fixed to a full-ON state (ON duty = 100%). To prevent this, set the maximum duty of the output transistor. To set it, set the voltage at the DTC1 terminal (pin 48) by applying a resistive voltage divider to the VREF voltage as shown below.

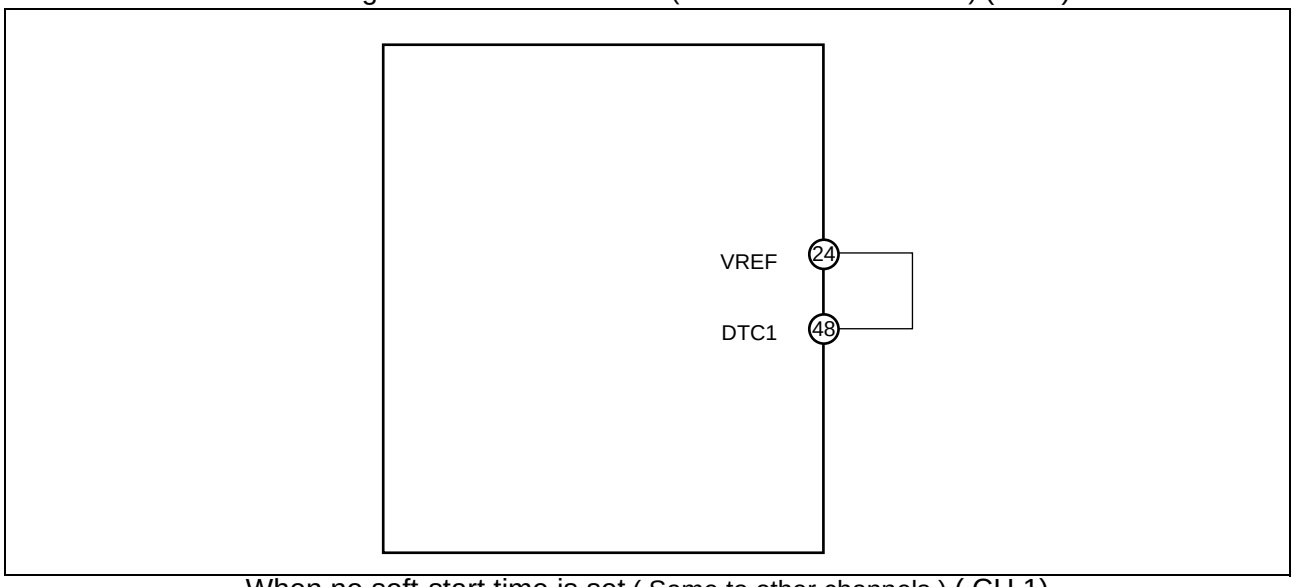
When the voltage at the DTC1 terminal (pin 48) is higher than the triangular wave voltage (CT1), the output transistor is turned on. The maximum duty calculation formula assuming that triangular wave amplitude ≒ 0.73 V and triangular wave minimum voltage ≒ 1.0 V is given below. (Same to other channels.)

$$\text{DUTY (ON) max} \fallingdotseq \frac{\text{Vdt} - 1.0\ \text{V}}{0.73\ \text{V}} \times 100[\%],\ \text{Vdt} = \frac{\text{Rb}}{\text{Ra} + \text{Rb}} \times \text{VREF}$$

When the DTC1 terminal (pin 48) is not used, connect it directly to the VREF terminal (pin 24) as shown below. (Same to other channels.)



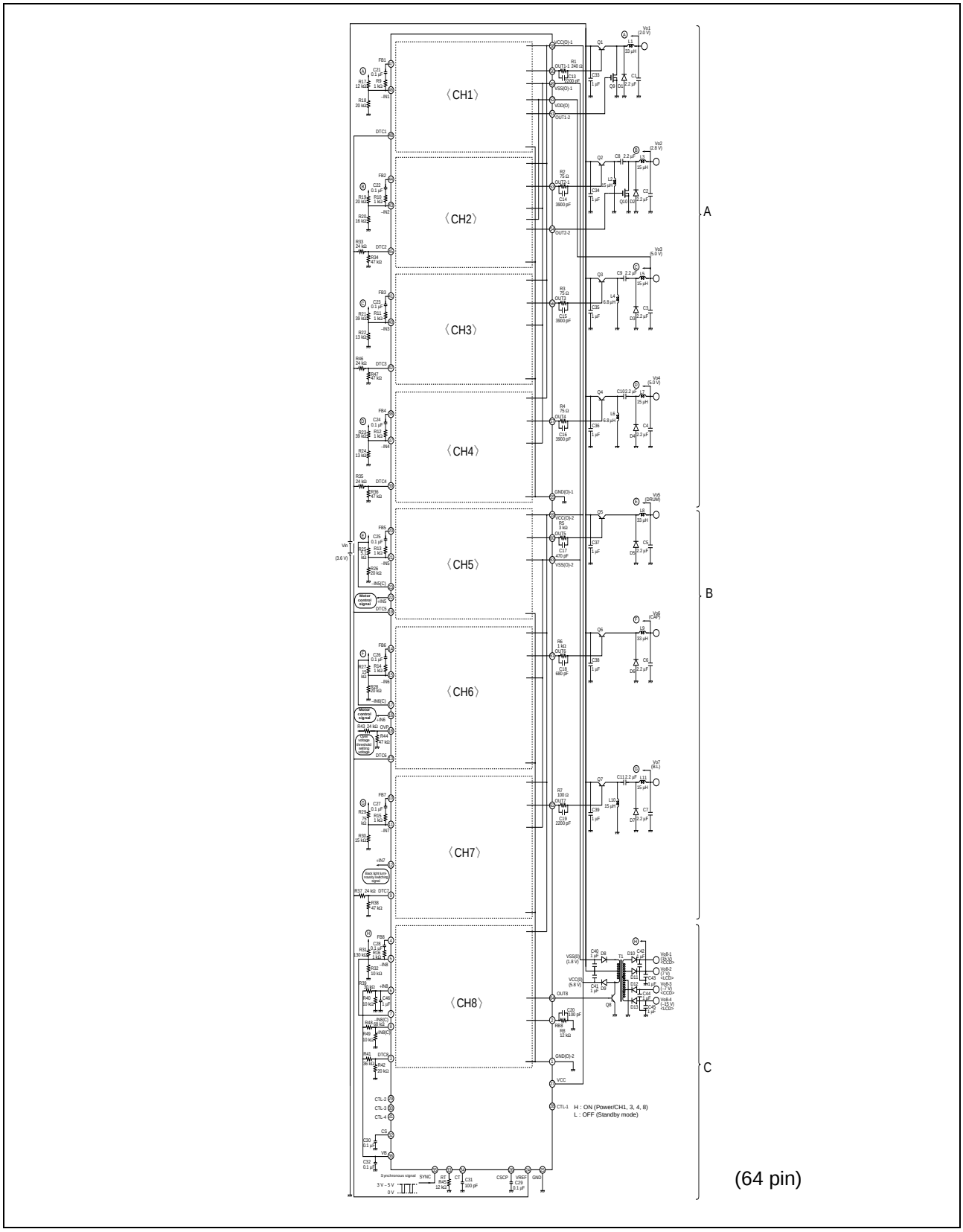
When using DTC to set dead time (Same to other channels.) (CH1)



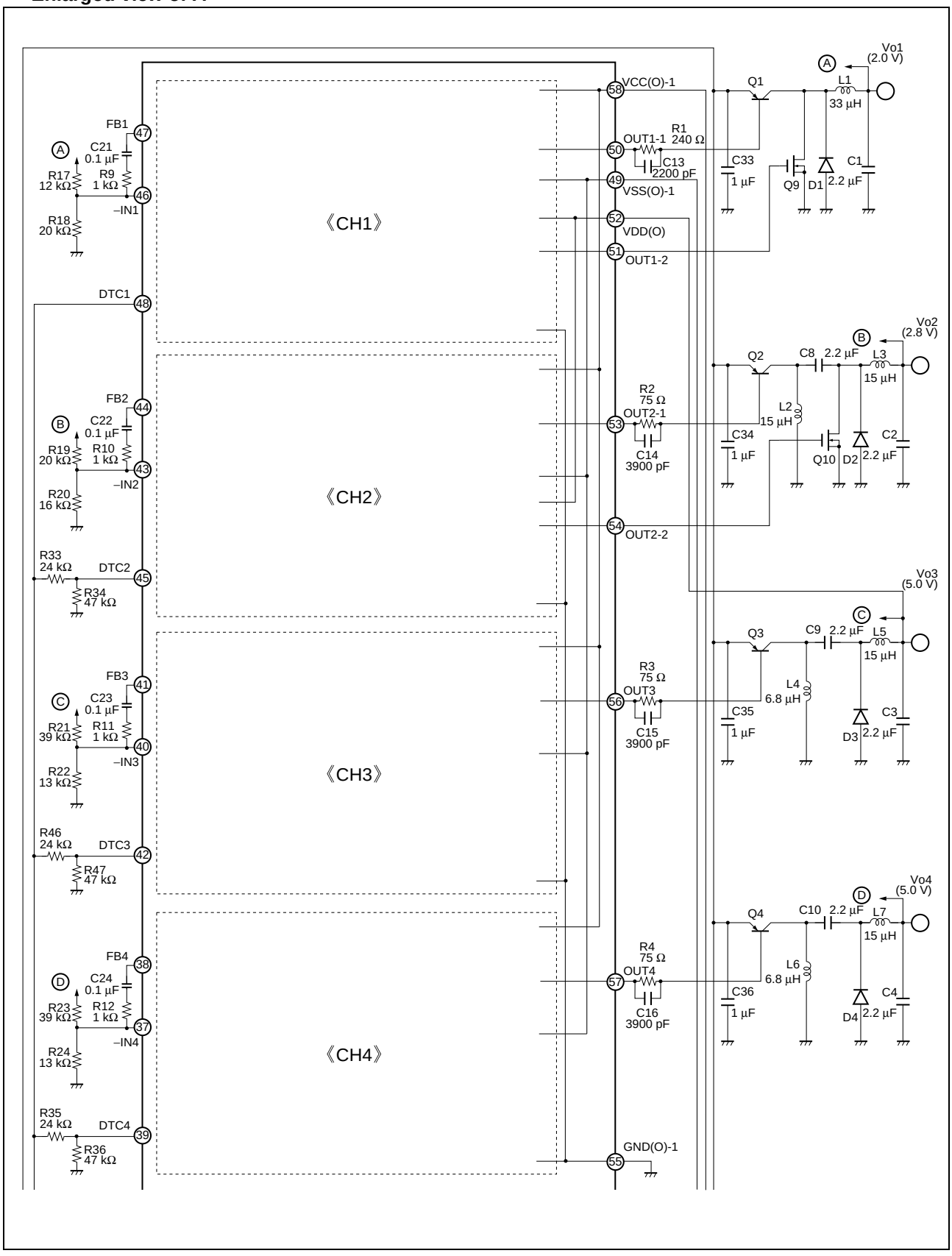
When no soft-start time is set (Same to other channels.) (CH 1)

■ APPLICATION EXAMPLE

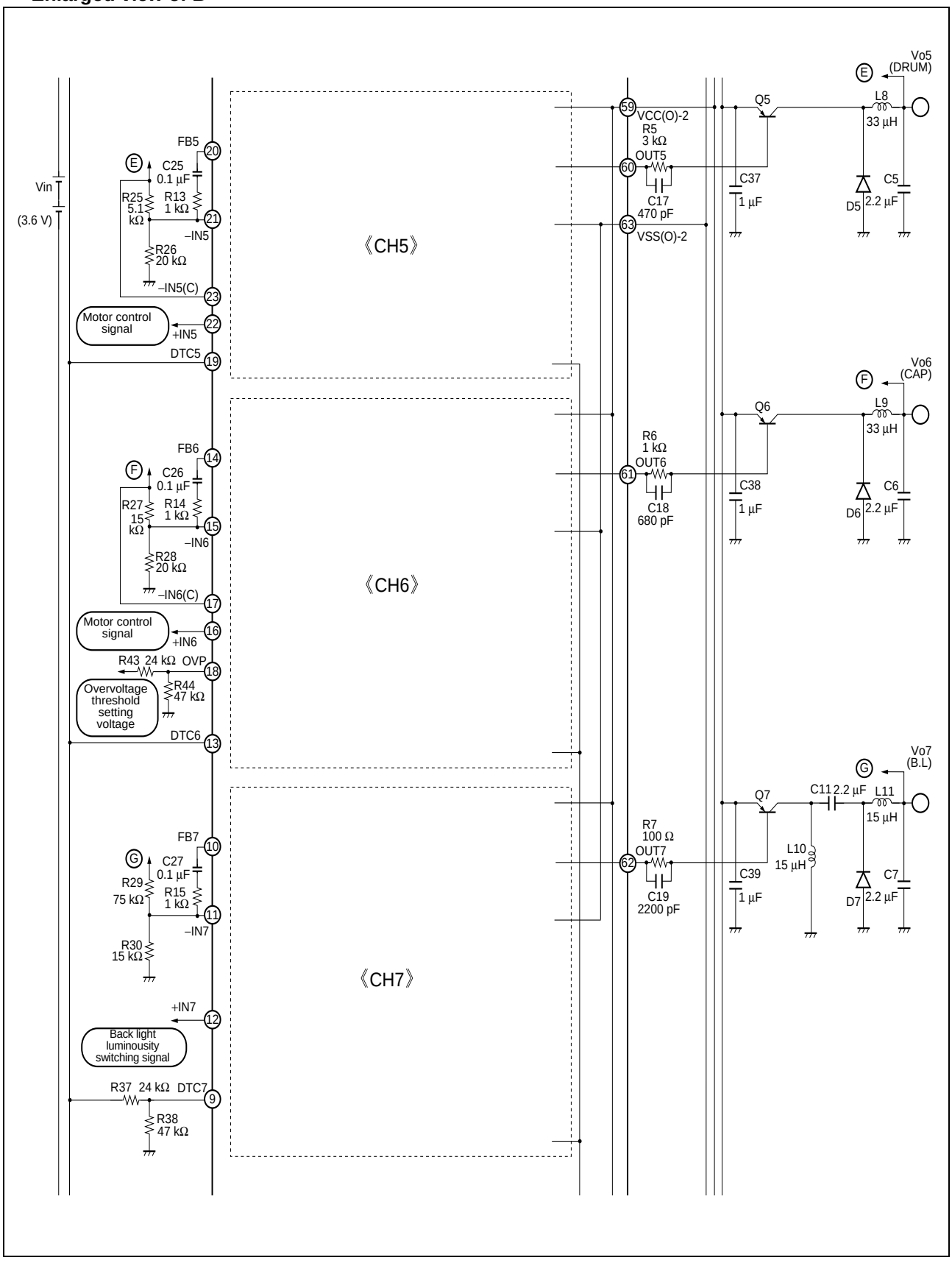
- **General view**



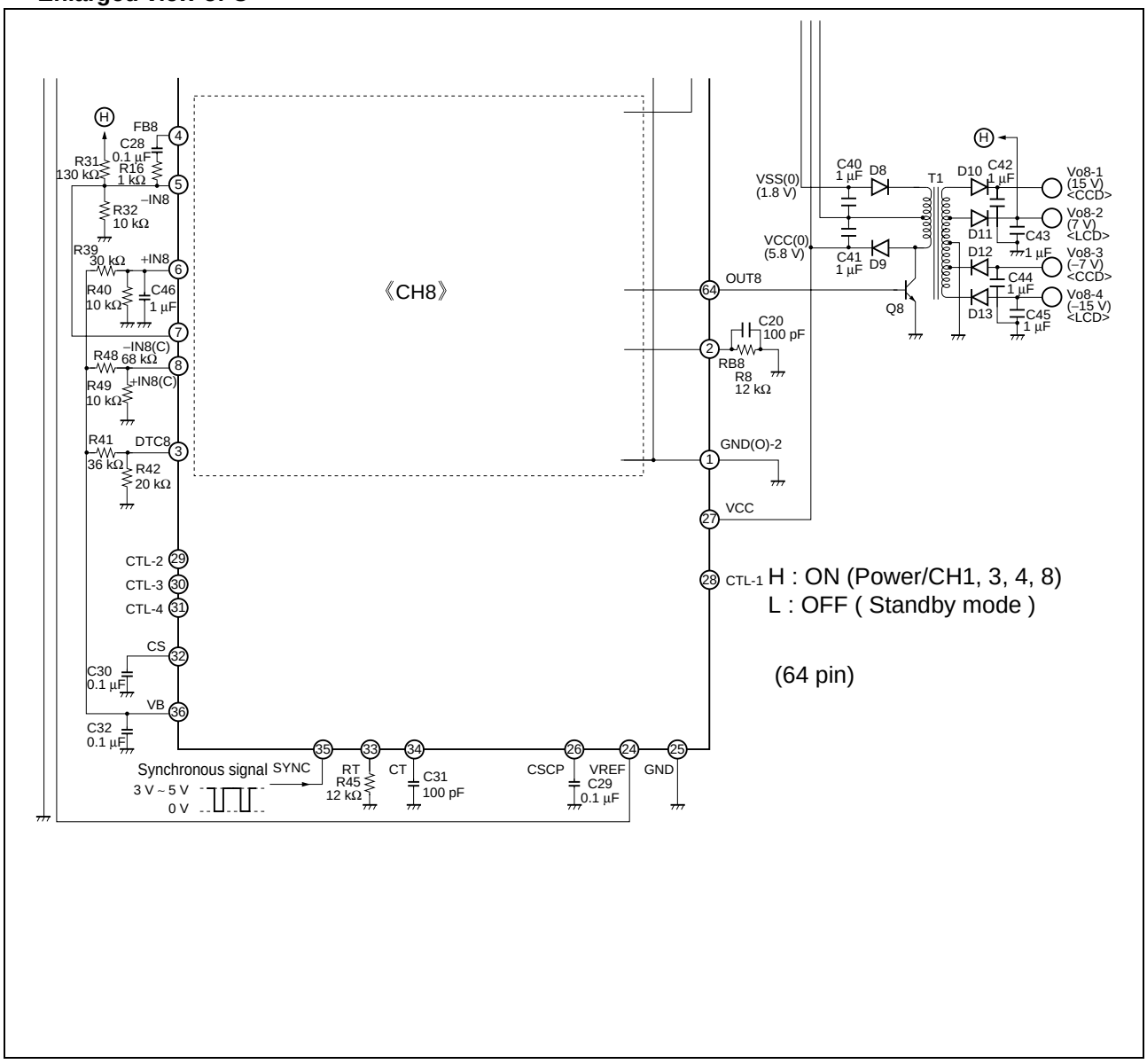
- **Enlarged view of A**



- **Enlarged view of B**



- **Enlarged view of C**



■ PARTS LIST

COMPONENT	ITEM	SPECIFICATION		VENDOR	PARTS No.
Q1 to Q7	PNP Tr	VCEO = −12 V		SANYO	CPH3106
Q8	NPN Tr	VCEO = 15 V		SANYO	CPH3206
Q9, Q10	FET	VDSS = 30 V		Fairchild	NDS355AN
D1 to D9	Diode	VF = 0.42 V (Max) , IR = 1 mA		ORIGIN	F1J2H
D10 to D13	Diode	VF = 0.77 V, IR = 10 μA (Max)		ORIGIN	F02J9
L1	Coil	33 μH	0.69 A, 148 mΩ	TDK	SLF6028T-330MR69
L2, L3	Coil	15 μH	1 A, 74.5 mΩ	TDK	SLF6028T-150M1R0
L4	Coil	6.8 μH	1.5 A, 35.4 mΩ	TDK	SLF6028T-6R8M1R5
L5	Coil	15 μH	1A, 74.5 mΩ	TDK	SLF6028T-150M1R0
L6	Coil	6.8 μH	1.5 A, 35.4 mΩ	TDK	SLF6028T-6R8M1R5
L7	Coil	15 μH	1 A, 74.5 mΩ	TDK	SLF6028T-150M1R0
L8, L9	Coil	33 μH	0.69 A, 148 mΩ	TDK	SLF6028T-330MR69
L10, L11	Coil	15 μH	1 A, 74.5 mΩ	TDK	SLF6028T-150M1R0
T1	Transformer			SUMIDA	CLQ72B
C1 to C11	Ceramics Condensor	2.2 μF	16 V		
C13	Ceramics Condensor	2200 pF	50 V		
C14 to C16	Ceramics Condensor	3900 pF	50 V		
C17	Ceramics Condensor	470 pF	50 V		
C18	Ceramics Condensor	680 pF	50 V		
C19	Ceramics Condensor	2200 pF	50 V		
C20	Ceramics Condensor	100 pF	50 V		
C21 to C30	Ceramics Condensor	0.1 μF	16 V		
C31	Ceramics Condensor	100 pF	50 V		
C32	Ceramics Condensor	0.1 μF	16 V		
C33 to C46	Ceramics Condensor	1 μF	25 V		
R1	Resistor	240 Ω	1/16 W		
R2 to R4	Resistor	75 Ω	1/16 W		
R5	Resistor	3 kΩ	1/16 W		
R6	Resistor	1 kΩ	1/16 W		
R7	Resistor	100 Ω	1/16 W		
R8	Resistor	12 kΩ	1/16 W		
R9 to R16	Resistor	1 kΩ	1/16 W		
R17	Resistor	12 kΩ	1/16 W		
R18, R19	Resistor	20 kΩ	1/16 W		
R20	Resistor	16 kΩ	1/16 W		
R21	Resistor	39 kΩ	1/16 W		
R22	Resistor	13 kΩ	1/16 W		
R23	Resistor	39 kΩ	1/16 W		
R24	Resistor	13 kΩ	1/16 W		
R25	Resistor	5.1 kΩ	1/16 W		
R26	Resistor	20 kΩ	1/16 W		
R27	Resistor	15 kΩ	1/16 W		
R28	Resistor	20 kΩ	1/16 W		
R29	Resistor	75 kΩ	1/16 W		
R30	Resistor	15 kΩ	1/16 W		
R31	Resistor	130 kΩ	1/16 W		
R32	Resistor	10 kΩ	1/16 W		

(Continued)

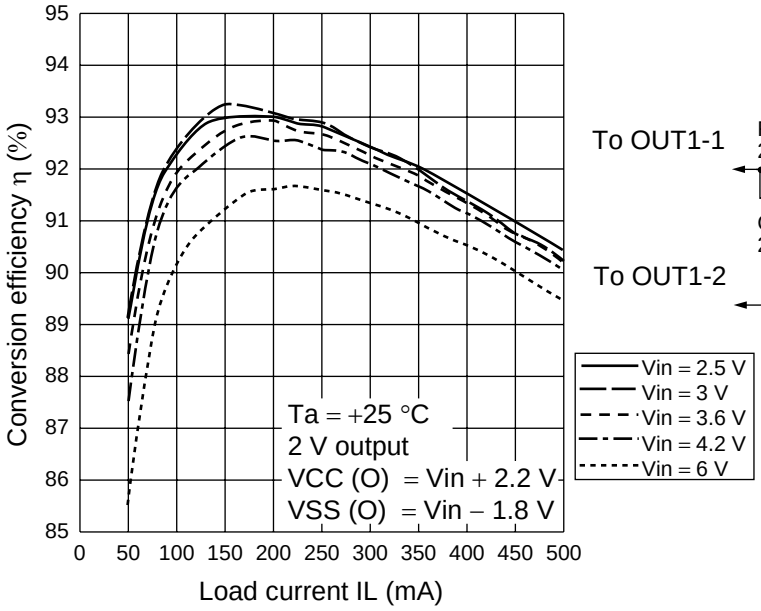
(Continued)

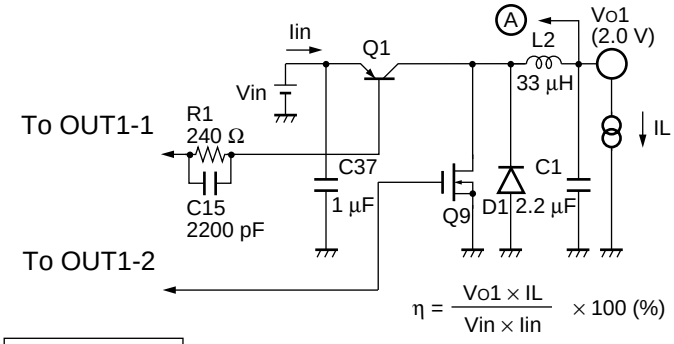
COMPONENT	ITEM	SPECIFICATION		VENDOR	PARTS No.
R33	Resistor	24 kΩ	1/16 W		
R34	Resistor	47 kΩ	1/16 W		
R35	Resistor	24 kΩ	1/16 W		
R36	Resistor	47 kΩ	1/16 W		
R37	Resistor	24 kΩ	1/16 W		
R38	Resistor	47 kΩ	1/16 W		
R39	Resistor	30 kΩ	1/16 W		
R40	Resistor	10 kΩ	1/16 W		
R41	Resistor	36 kΩ	1/16 W		
R42	Resistor	20 kΩ	1/16 W		
R43	Resistor	24 kΩ	1/16 W		
R44	Resistor	47 kΩ	1/16 W		
R45	Resistor	12 kΩ	1/16 W		
R46	Resistor	24 kΩ	1/16 W		
R47	Resistor	47 kΩ	1/16 W		
R48	Resistor	68 kΩ	1/16 W		
R49	Resistor	10 kΩ	1/16 W		

Note : SANYO : SANYO Electric Co., Ltd.
Fairchild : Fairchild Semiconductor Corporation
ORIGIN : Origin Electric Co., Ltd.
TDK : TDK Corporation
SUMIDA : Sumida Electric Co., Ltd.

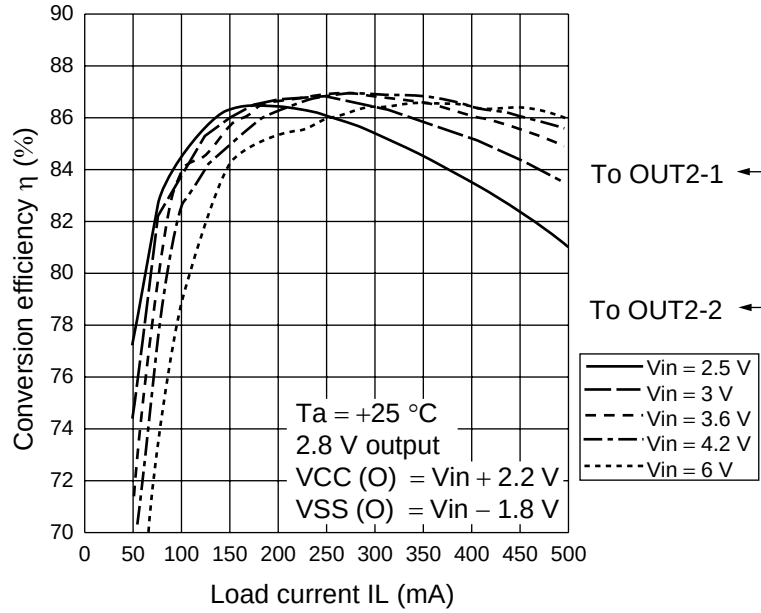
■ REFERENCE DATA

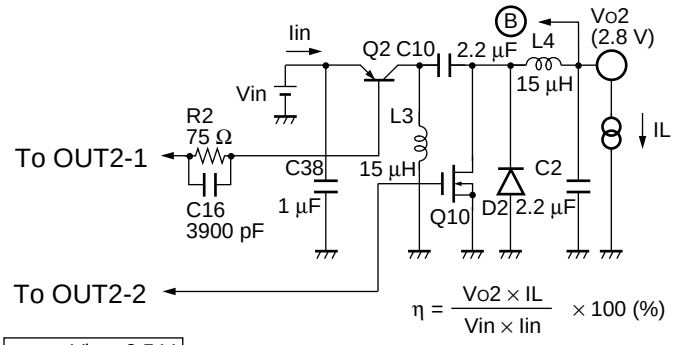
Conversion efficiency vs. load current
(CH1 : Down conversion method with synchronous rectification)





Conversion efficiency vs. load current
(CH2 : Zeta method with synchronous rectification)





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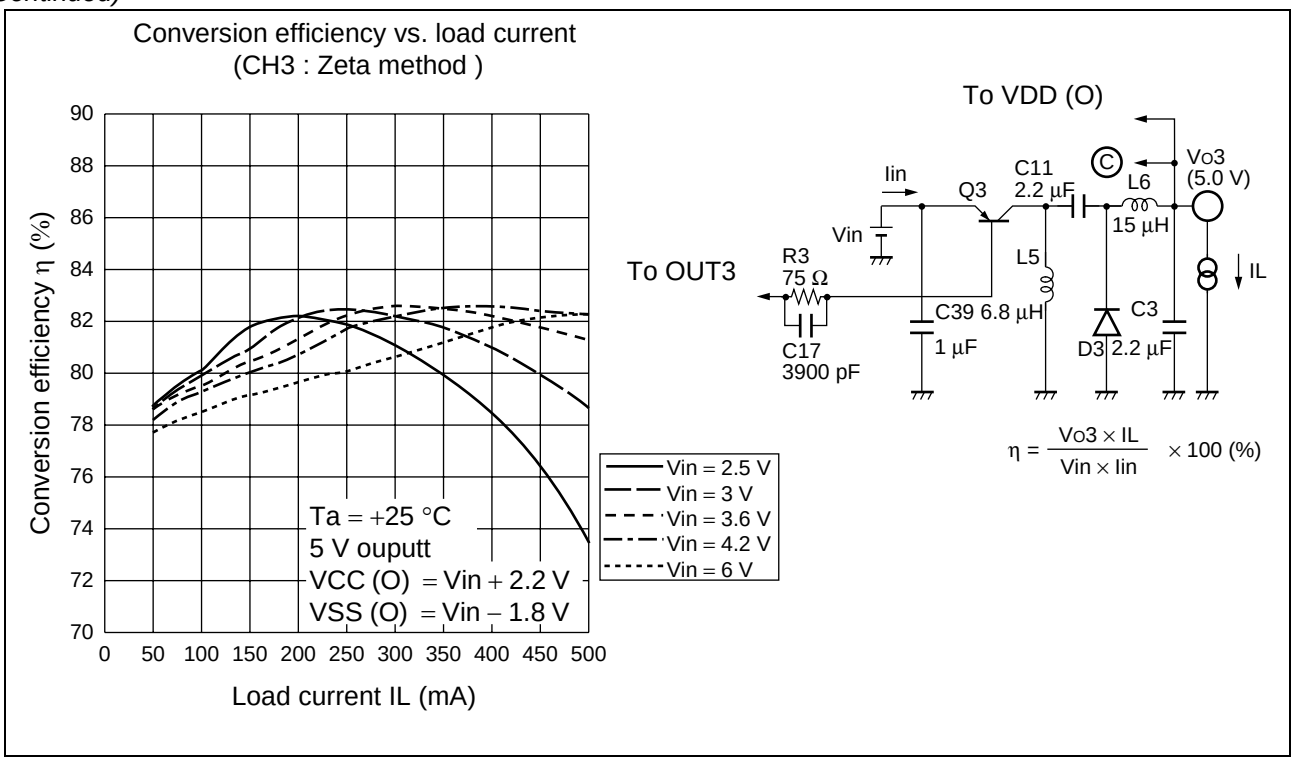

Conversion efficiency vs. load current
(CH3 : Zeta method)
Conversion efficiency η (%)
90
88
86
84
82
80
78
76
74
72
70
0 50 100 150 200 250 300 350 400 450 500
Load current IL (mA)
Ta = +25 °C
5 V ouputt
VCC (O) = Vin + 2.2 V
VSS (O) = Vin – 1.8 V
Vin = 2.5 V
Vin = 3 V
Vin = 3.6 V
Vin = 4.2 V
Vin = 6 V
To VDD (O)
To OUT3
Iin
Q3
C11
2.2 µF
L6
15 µH
VO3
(5.0 V)
Vin
R3
75 Ω
L5
IL
C17
3900 pF
C39 6.8 µH
1 µF
C3
D3
2.2 µF
η = VO3 × IL / Vin × Iin × 100 (%)

■ USAGE PRECAUTION

1. Never use setting exceeding maximum rated conditions.

Exceeding maximum rated conditions may cause permanent damage to the LSI.

Also, it is recommended that recommended operating conditions be observed in normal use. Exceeding recommended operating conditions may adversely affect LSI reliability.

2. Use this device within recommended operating conditions.

Recommended operating conditions are values within which normal LSI operation is warranted.

Standard electrical characteristics are warranted within the range of recommended operating conditions and within the listed conditions for each parameter.

3. Printed circuit board ground lines should be set up with consideration for common impedance.

4. Take appropriate static electricity measures.

- Containers for semiconductor materials should have anti-static protection or be made of conductive material.
- After mounting, printed circuit boards should be stored and shipped in conductive bags or containers.
- Work platforms, tools, and instruments should be properly grounded.
- Working personnel should be grounded with resistance of 250 kΩ to 1 MΩ between body and ground.

5. Do not apply negative voltages.

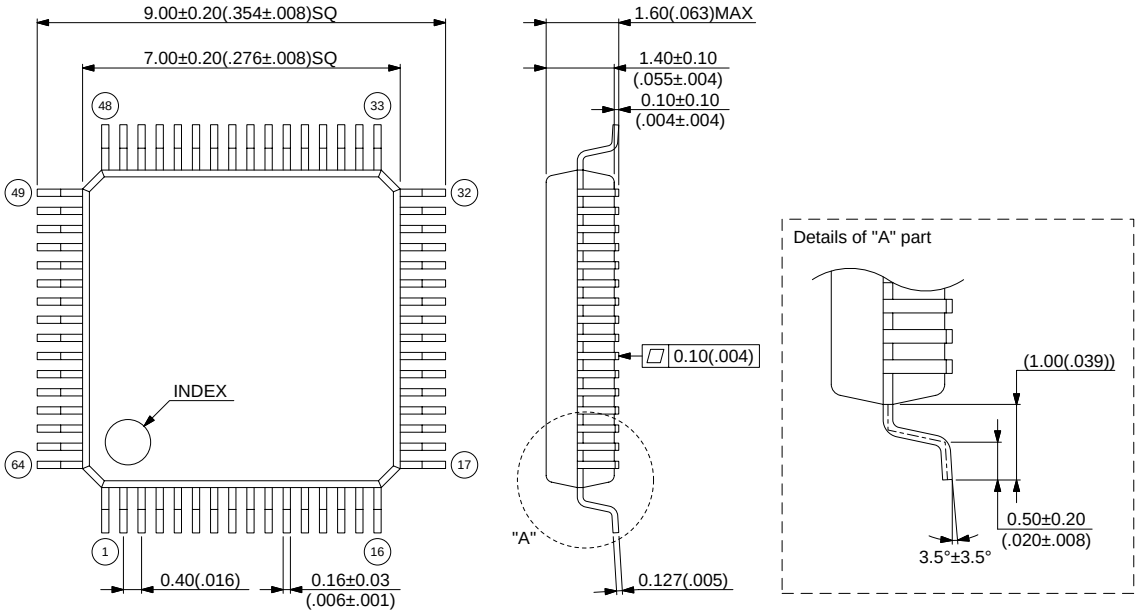
The use of negative voltages below –0.3 V may create parasitic transistors on LSI lines, which can cause abnormal operation.

■ ORDERING INFORMATION

Part number	Package	Remarks
MB3881PFF	64-pin plastic LQFP (FPT-64P-M20)	

■ PACKAGE DIMENSION

64-pin plastic LQFP
(FPT-64P-M20)



Dimensions in: mm (inches)

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