

Linear IC Converter

CMOS

A/D Converter

(With 24-Channel Input at 10-bit Resolution)

MB88111

■ DESCRIPTION

The MB88111 is an analog-to-digital converter that converts its analog input to a 10-bit digital value and outputs it as serial data.

The MB88111 employs a successive approximation method for A/D conversion. It has 24 input channels to be A/D converted selectively by setting in an internal register.

Since the MB88111 can input and output 16-bit serial data in synchronization with the clock, it can be easily connected to the serial I/O port in a 16-bit microcontroller.

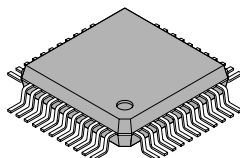
■ FEATURES

- 24-channel analog input
- RC-type successive approximation system with a sample-and-hole circuit
- 10-bit resolution
- Conversion speed within 50 μ s (at a system clock rate of 1 MHz)
- Digitally converted data output from the MSB
- Digitally converted data output as 16-bit serial data
- Clock-synchronous serial transfer system
- Internal extended serial interface
- Capable of triggering A/D conversion through an external pin
- Capable of input through an 8-channel port
- Serial data output format selectable using an external pin
- 10-bit monotonicity
- No missing code
- Power supply voltage ranging from 3.5 to 5.5 V

(Continued)

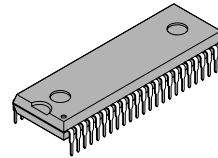
■ PACKAGES

44-pin, Plastic QFP



(FPT-44P-M11)

48 pin, Plastic SH-DIP



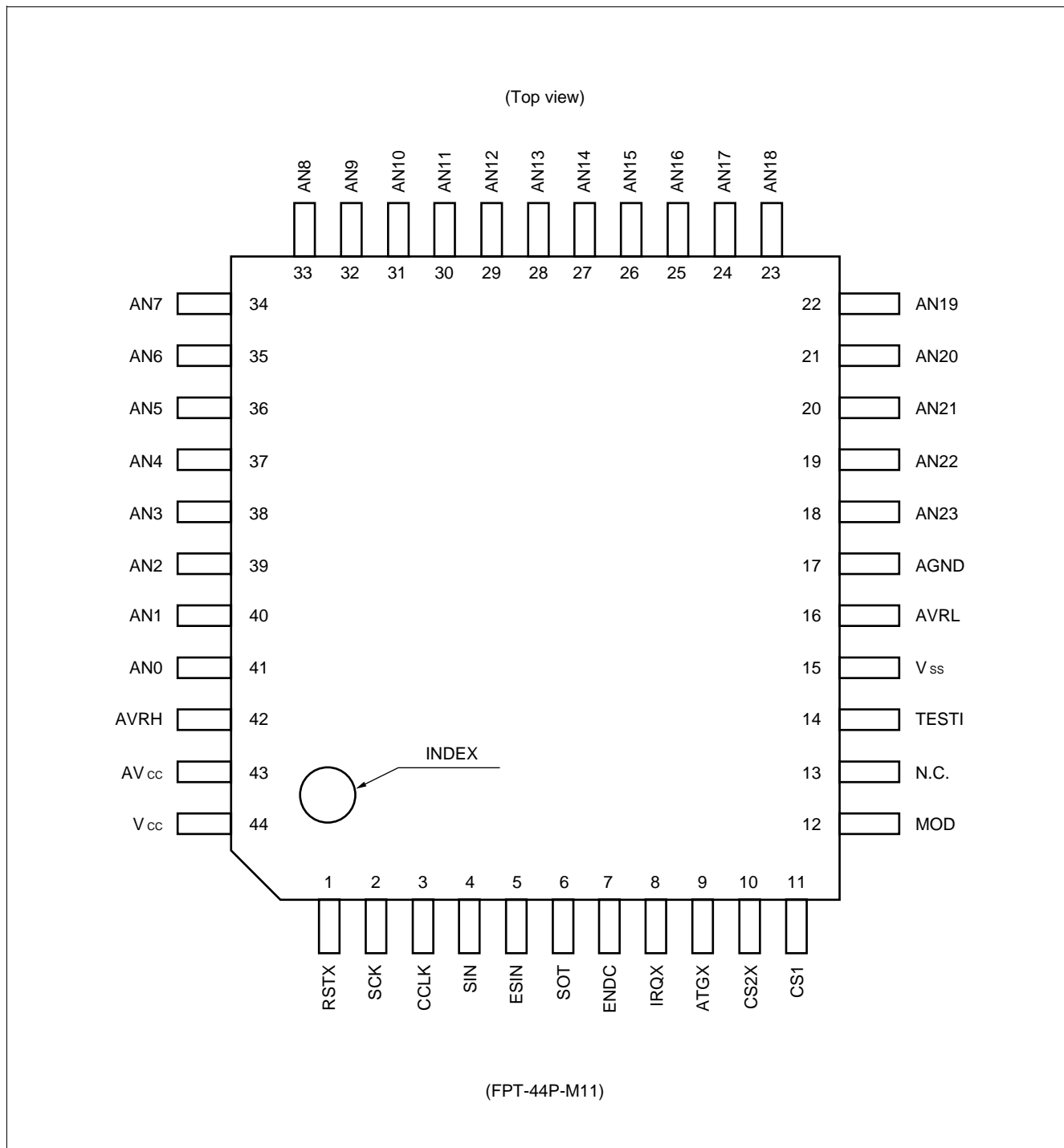
(DIP-48P-M01)

MB88111

(Continued)

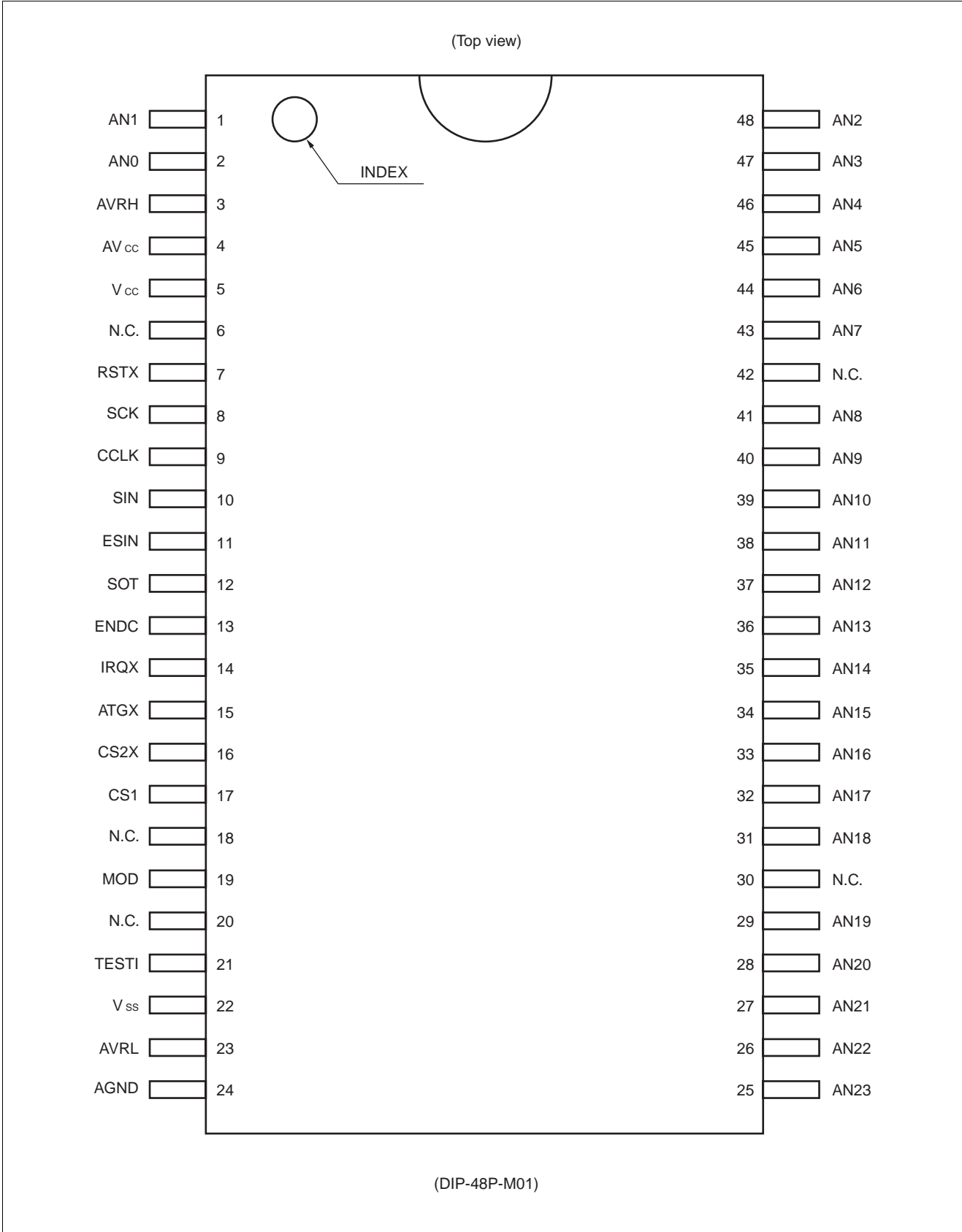
- Operating temperature ranging from -40 to $+50^{\circ}\text{C}$
- CMOS process
- Package options of 44-pin QFP and 48-pin SH-DIP

■ PIN ASSIGNMENT



(Continued)

(Continued)



■ PIN DESCRIPTION

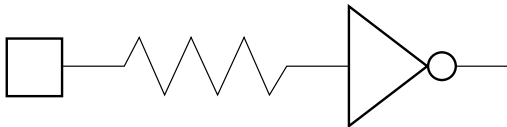
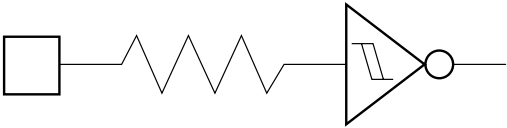
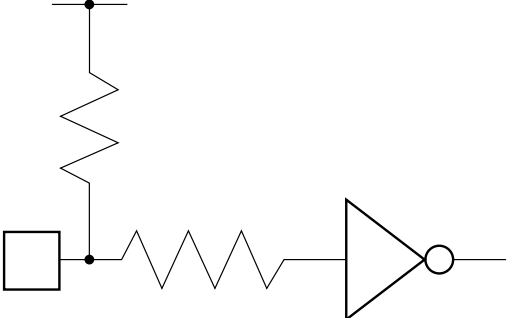
| Pin no. | | Symbol | I/O | Circuit type | Descriptions |
|----------|----------------------------------|-----------------|-----|--------------|--|
| QFP | DIP | | | | |
| 41 to 26 | 2 to 1, 48 to 43, 41 to 34 | AN0 to AN15 | I | F | Analog input pins. The pin to be subject to conversion is selected by the command input through the SIN pin. Also, a series of pins from AN16 to AN23 can be used as a port input. |
| 25 to 18 | 33 to 31, 29 to 25 | AN16 to AN23 | | G | |
| 12 | 19 | MOD | I | A | Pin for selecting a serial data output mode: "L": Mode A for output from the SOT pin in synchronization with the fall of the SCK signal. "H": Mode B for output from the SOT pin in synchronization with the rise of the SCK signal. |
| 11 10 | 17 16 | CS1 CS2X | I | A | Input pins for selecting an extended serial interface mode. Setting the CS1 level to "H" and the CS2X level to "L" enables A/D converted data transfer. Setting the CS1 level to "L" or the CS2X level to "H" clears the register command without affecting A/D conversion. Serial data input to the external extended serial input pin ESIN is output to the SOT pin as it is. (See Section 7 "Extended Serial Interface" in "■ OPERATION.") |
| 4 | 10 | SIN | I | B | Serial data input pin This pin is a hysteresis input with a filter. |
| 6 | 12 | SOT | O | H | Serial data output pin |
| 3 | 9 | CCLK | I | B | System clock input pin This pin is a hysteresis input. |
| 2 | 8 | SCK | I | B | Serial data transfer clock input pin This pin is a hysteresis input with a filter. |
| 9 | 15 | ATGX | I | C | External trigger input pin. This pin incorporates a pull-up resistor. The ATC command initiates A/D conversion at the rise of the signal at this pin. The pin is a hysteresis input. |
| 8 | 14 | IRQX | O | H | A/D conversion interrupt signal input pin. The signal level becomes "L" upon completion of A/D conversion; it becomes "H" upon reception of data to be converted. |
| 7 | 13 | ENDC | O | H | A/D conversion completion signal output pin. The signal level becomes "H" upon completion of A/D conversion; it becomes "L" upon reception of data to be converted. |
| 5 | 11 | ESIN | I | A | Serial input extension input pin. When the CS1 level is "L" or the CS2X level is "H," data input to the ESIN pin is output to the SOT pin as it is. |
| 1 | 7 | RSTX | I | D | Reset signal input pin. This pin incorporates a pull-up resistor. Setting the signal level to "L" initializes the internal circuit of the device. This pin is a hysteresis input with a filter. |

(Continued)

(Continued)

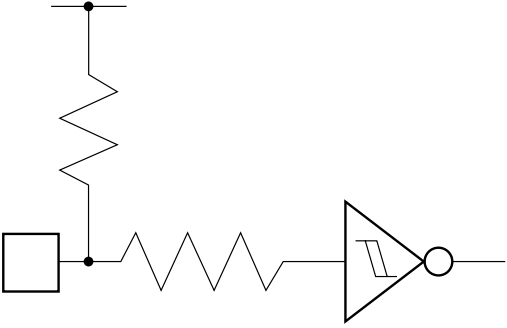
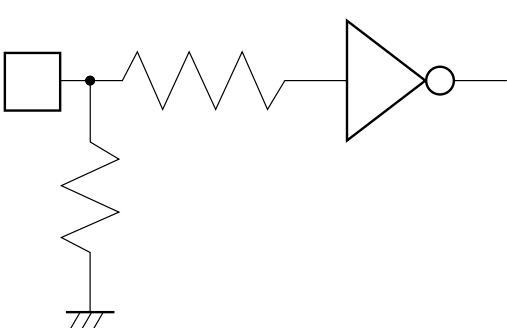

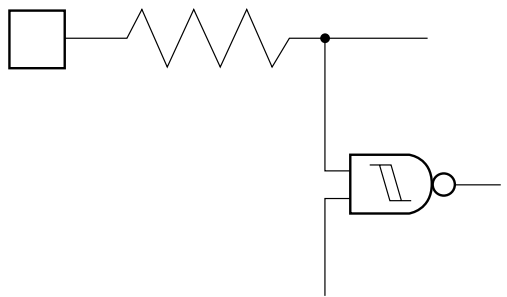
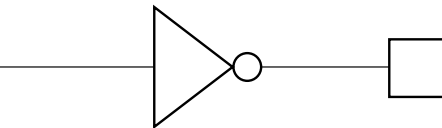
| Pin no. | | Symbol | I/O | Circuit type | Descriptions |
|---------|-------------------------|------------------|-----|--------------|--|
| QFP | DIP | | | | |
| 14 | 21 | TESTI | I | E | Test input pin. This pin incorporates a pull-down resistor. Maintain the pin at "L" level during normal use. |
| 44 | 5 | V _{cc} | — | — | Digital circuit power supply pin |
| 15 | 22 | V _{ss} | — | — | Digital circuit ground pin |
| 43 | 4 | AV _{cc} | — | — | Analog circuit power supply pin |
| 17 | 24 | AGND | — | — | Analog circuit ground pin |
| 42 | 3 | AVRH | — | — | Reference (high) voltage input pin |
| 16 | 23 | AVRL | — | — | Reference (low) voltage input pin |
| 13 | 6, 18, 20, 30, 42 | N.C. | — | — | Non-connection pin |

■ I/O CIRCUIT TYPE

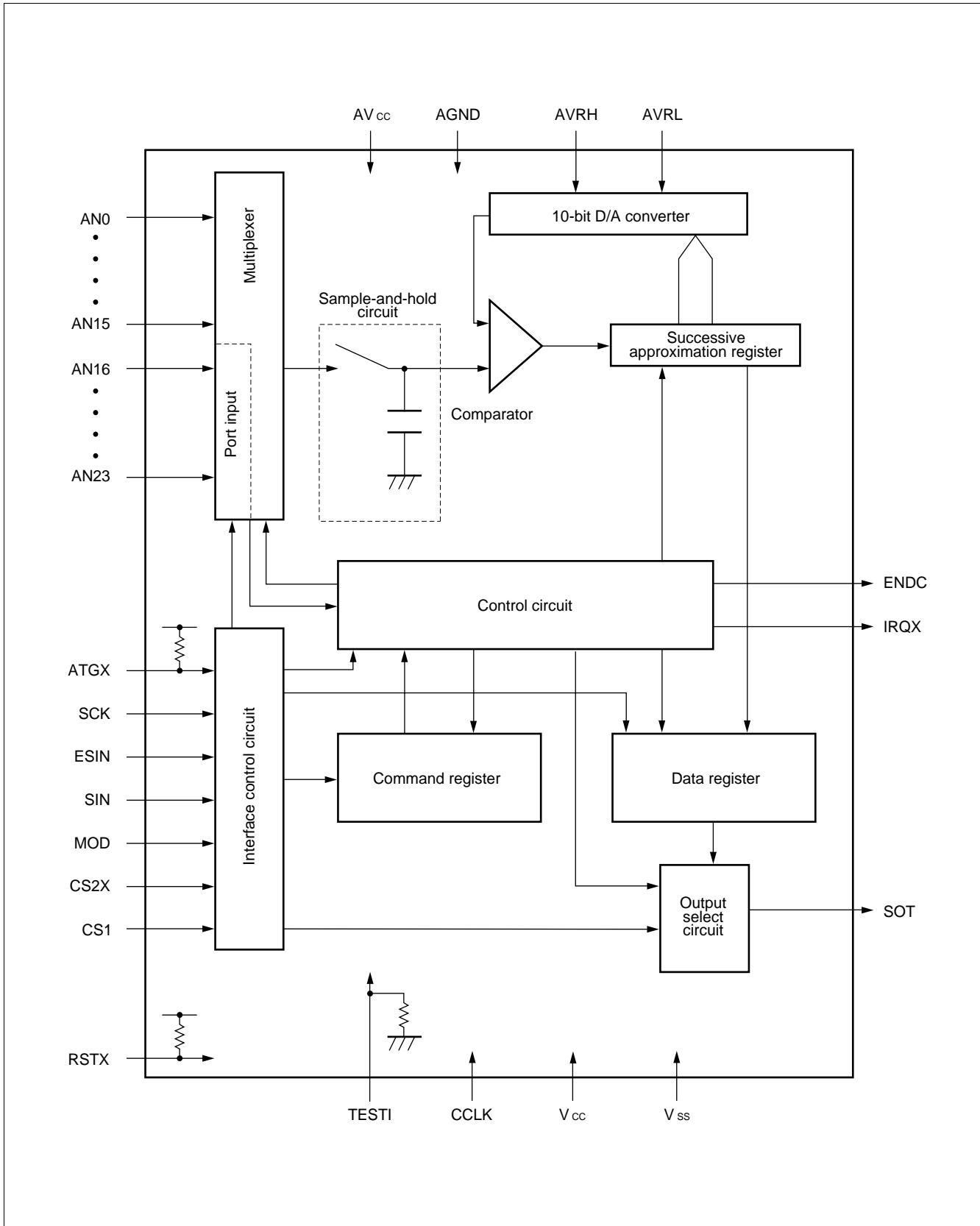
| Type | Circuit | Remarks |
|------|---|---|
| A |  | <ul style="list-style-type: none"> • CMOS input |
| B |  | <ul style="list-style-type: none"> • Hysteresis input • CMOS input |
| C |  | <ul style="list-style-type: none"> • Input with pull-up resistor • CMOS input |

(Continued)

(Continued)

| Type | Circuit | Remarks |
|------|---|---|
| D |  | <ul style="list-style-type: none"> • Input with pull-up resistor • Hysteresis input • CMOS input |
| E |  | <ul style="list-style-type: none"> • Input with pull-down resistor • CMOS input |
| F |  | <ul style="list-style-type: none"> • Analog input |
| G |  | <ul style="list-style-type: none"> • Analog input • Hysteresis input • CMOS input |
| H |  | <ul style="list-style-type: none"> • CMOS output |

■ BLOCK DIAGRAM



■ FUNCTIONAL DESCRIPTION

1. SC (Serial Command) Register (Reset status: 0000H)

The SC register contains an A/D converter command and an input channel identification. Accessing this register after releasing it from the reset status activates the A/D converter.

Note that this register accepts setting even during A/D conversion.

Note also that input of a command to the register must take an interval of at least 4 CCLKs after input of the previous command.

| | | | | | | | | | | | | | | | |
|---------|----|----|---------|----|----|----|----|------------|----|----|----|----|----|-----|----|
| MSB | | | | | | | | | | | | | | LSB | |
| bf | be | bd | bc | bb | ba | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| Command | | | Channel | | | | | Don't care | | | | | | | |

(1) Command bits

A string of command bits selects an A/D converter command such as STOP. Setting a command during execution of another command cancels the command currently being executed.

| bf | be | bd | Command name | Function |
|----|----|----|--------------|--|
| 0 | 0 | 0 | STOP | Stops A/D conversion (if it is being executed) and initializes the A/D converter. This command has the same effect as RSTX. |
| 0 | 0 | 1 | STC | Executes A/D conversion of the specified channel once. (See Section 3 "STC (Standard Conversion) Command.") |
| 0 | 1 | 0 | — | Unused (*) |
| 0 | 1 | 1 | — | Unused (*) |
| 1 | 0 | 0 | NOP | No-op command. Input of this command during A/D conversion does not affect operation. If followed by this command, the ATC command can transfer converted data while holding the NOP command. |
| 1 | 0 | 1 | ATC | The basic operation of this command is the same as that of the STC command. The ATC command can leave the A/D conversion start timing to the external trigger pin ATGX. (See Section 4 "ATC (Auto Trigger Conversion) Command.") |
| 1 | 1 | 0 | — | Unused (*) |
| 1 | 1 | 1 | — | Unused (*) |

* : These command settings cause the STOP command to be executed.

(2) Channel select bits

A string of channel select bits selects the pin to be subject to A/D conversion. This bit string is enabled only for the STC or ATC command.

| bc | bb | ba | b9 | b8 | Pin to be selected | bc | bb | ba | b9 | b8 | Pin to be selected |
|----|----|----|----|----|--------------------|----|----|----|----|----|---|
| 0 | 0 | 0 | 0 | 0 | AN0 | 1 | 0 | 0 | 0 | 0 | AN16 |
| 0 | 0 | 0 | 0 | 1 | AN1 | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ |
| 0 | 0 | 0 | 1 | 0 | AN2 | 1 | 0 | 1 | 1 | 1 | AN23 |
| 0 | 0 | 0 | 1 | 1 | AN3 | 1 | 1 | 0 | 0 | 0 | Undefined ^{(*)1} |
| 0 | 0 | 1 | 0 | 0 | AN4 | 1 | 1 | 0 | 0 | 1 | |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | 1 | 1 | 0 | 1 | 0 | |
| 0 | 1 | 0 | 1 | 1 | AN11 | 1 | 1 | 0 | 1 | 1 | |
| 0 | 1 | 1 | 0 | 0 | AN12 | 1 | 1 | 1 | 0 | 0 | |
| 0 | 1 | 1 | 0 | 1 | AN13 | 1 | 1 | 1 | 0 | 1 | |
| 0 | 1 | 1 | 1 | 0 | AN14 | 1 | 1 | 1 | 1 | 0 | |
| 0 | 1 | 1 | 1 | 1 | AN15 | 1 | 1 | 1 | 1 | 1 | Port input AN16 to AN23 ^{(*)2} |

*1: These settings of the bit string cause the STOP command to be executed.

*2: This setting is enabled only for the STC command. (See Section 5 “Port Input Command.”)
If this setting is made for the ATC command, the STOP command is executed.

2. Data Output Format

Upon completion of A/D conversion, the ENDC pin level becomes “H” and the IRQX pin level becomes “L.” Execution of serial transfer at this time outputs data in the format illustrated below. The data output timing can be selected by the MOD pin between the falling edge (mode A) or rising edge (mode B) of the SCK signal. When the ENDC pin level is “L,” 0000H is output.

| | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|------|-------------------|----|----|-----|----|--|--|
| MSB | | | | | | | | | | | | | | LSB | | | |
| Bf | Be | Bd | Bc | Bb | Ba | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | | |
| Converted data | | | | | | | | | | ENDC | A/D converted pin | | | | | | |

ENDC (A/D conversion completion flag): This bit is set to “1” upon completion of A/D conversion. It is set to “0” upon completion of serial transfer.

Note: SCK input upon low-to-high transition of the ENDC pin level should be avoided. Otherwise, data may not be output correctly.

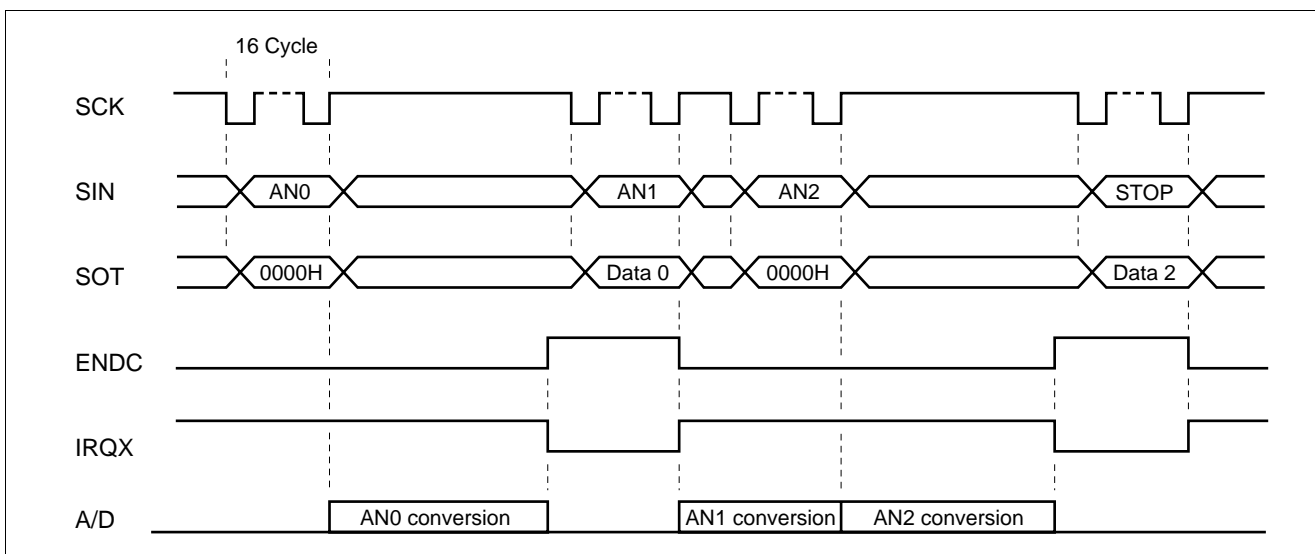
3. STC (Standard Conversion) Command

Input of the STC command executes A/D conversion of the specified channel once.

Implementation of A/D conversion, the ENDC signal rises while the IRQX signal falls. Clock input to the SCK pin after A/D conversion outputs data to the SOT pin. Upon completion of data output, the ENDC signal falls while the IRQX signal rises. If the next command is STOP or NOP, the A/D conversion is terminated. If the STC command is input during A/D conversion, the command currently being executed is cancelled and the STC command is executed.

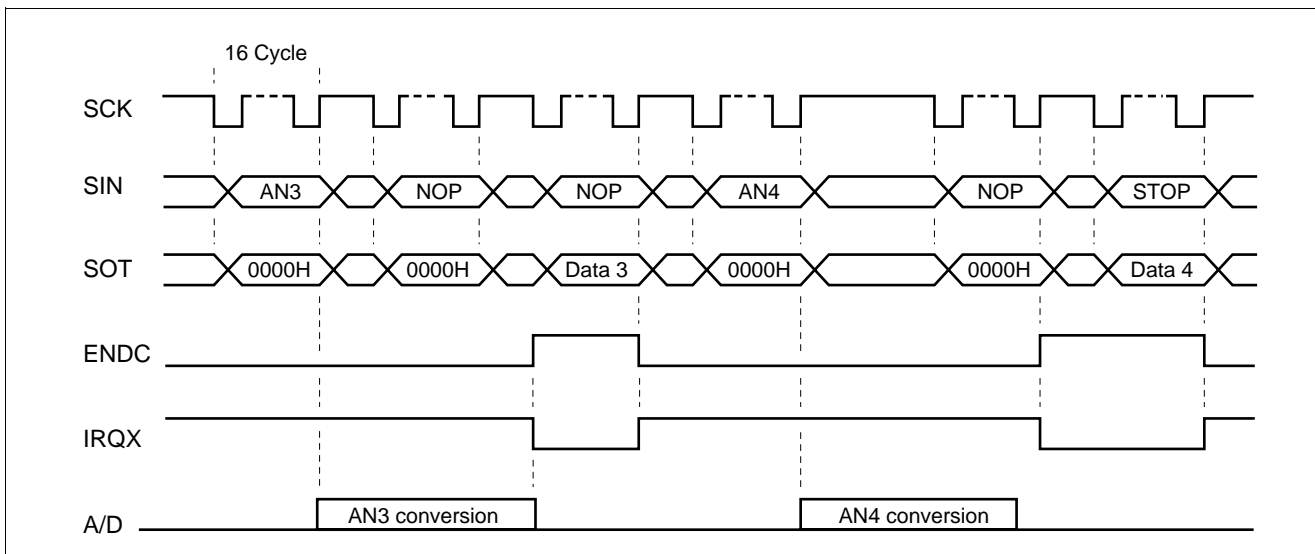
• Example of STC command execution (1)

STC command input during A/D conversion cancels the current command and executes A/D conversion of the new specified channel. Output data at this time is 0000H.



• Example of STC command execution (2)

NOP command input during A/D conversion does not affect operation. Output data at this time is 0000H. If A/D conversion is completed during NOP command input, the ENDC and IRQX pin levels become "H" and "L" respectively upon completion of the NOP command input.



4. ATC (Auto Trigger Conversion) Command

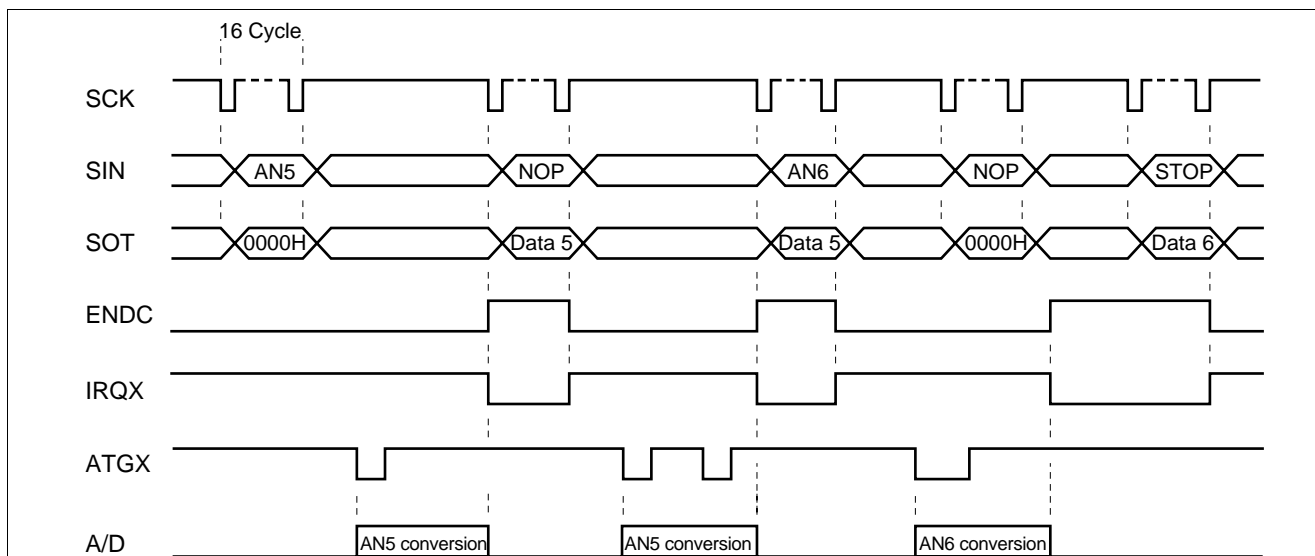
The ATC command is the same as the STC command in basic operation. This command can initiate A/D conversion using the external trigger pin ATGX. The external trigger signal is sampled by 1 μ s clock and filtered by 1 clock. The external trigger signal input during A/D conversion is ignored. If the next command is the STOP command, A/D conversion is terminated. If it is the NOP command, the ATC command is executed continuously. The channel cannot be changed at this time. To change the channel, input the ATC command to that effect.

• Example of ATC command execution (1)

NOP command input during A/D conversion enables the same channel to be A/D converted.

An attempt to set the ATGX signal low during A/D conversion is ignored.

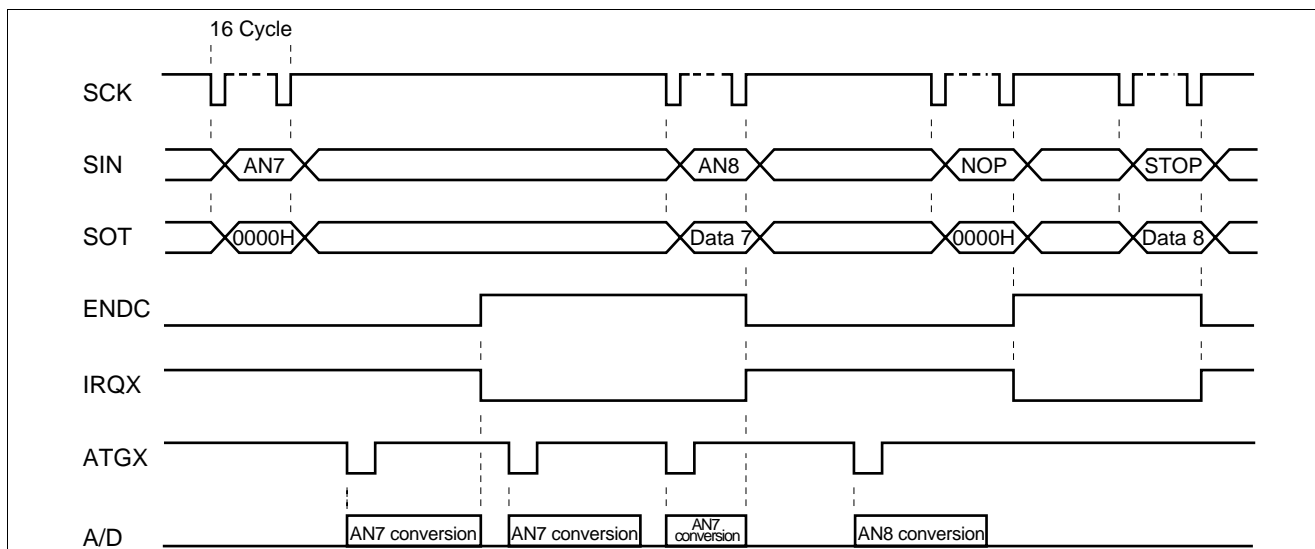
NOP command input during A/D conversion does not affect operation. Output data at this time is 0000H.



• Example of ATC command execution (2)

Setting the ATGX signal low again after A/D conversion restarts A/D conversion.

In data output mode B, however, do not use the ATC command in this way, or data will not be output correctly. If A/D conversion is completed during NOP command input, the ENDC and IRQX pin levels become "H" and "L" respectively upon completion of the NOP command input.



5. Port Input Command

The port input command executes I/O evaluation of 8-channel inputs from the AN16 to AN23 pins at a prescribed threshold in 10 clock cycles and outputs the results as port input data. The processing sequence is activated each time port input is selected by the STC command. Port input data is output in the following format:

| | | | | | | | | | | | | | | | |
|-----------------|----|----|----|----|----|----|----|-----|------|-----|-----|----|----|----|----|
| MSB | | | | | | | | | | | LSB | | | | |
| Bf | Be | Bd | Bc | Bb | Ba | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| Evaluation data | | | | | | | | "0" | ENDC | "1" | | | | | |

Evaluation data:

The evaluation values of AN23 to AN16 are output to bits Bf to B8.

Evaluation value

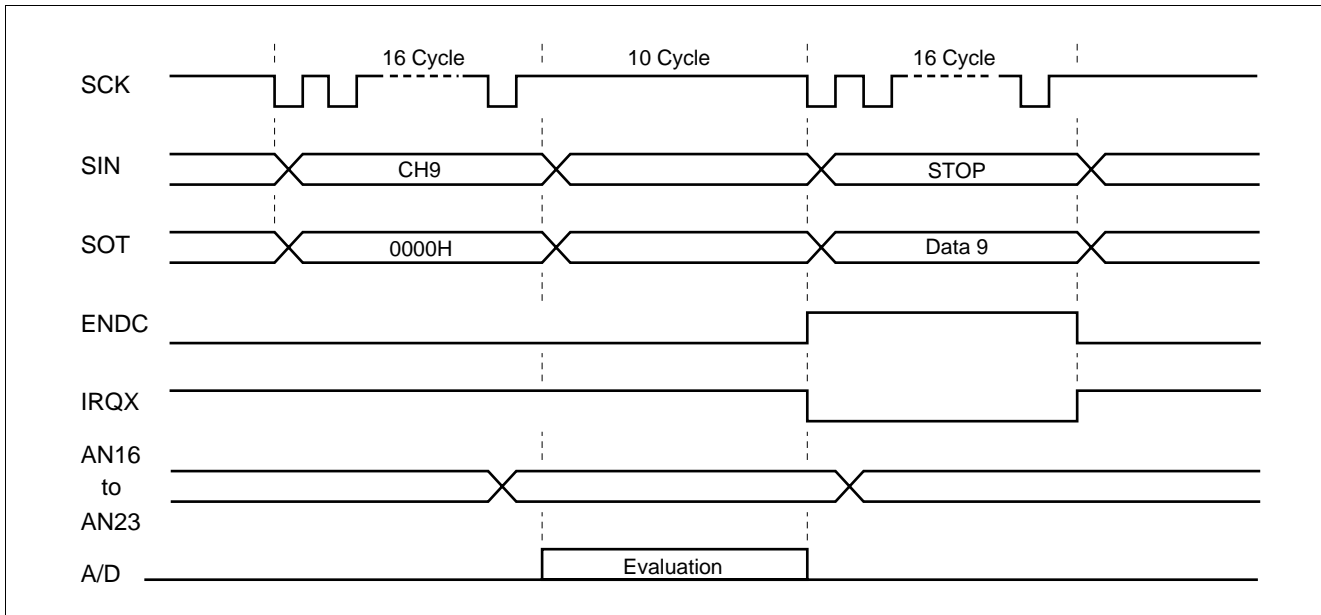
"H": $V_{in} \geq 0.8 \times V_{cc}$

"L": $V_{in} \leq 0.2 \times V_{cc}$

ENDC (A/D completion flag):

This bit is set to "1" upon completion of A/D conversion. It is set to "0" upon completion of serial transfer.

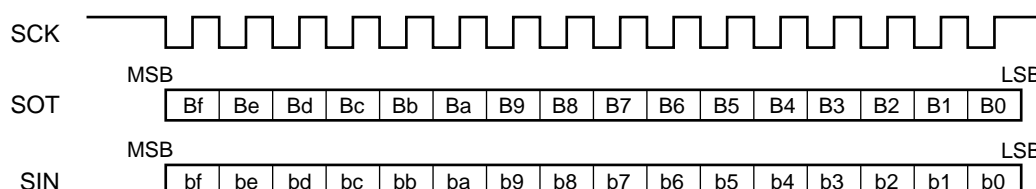
• Example of STC command execution (3) (Port input command)



6. Serial Output Select Function

The MB88111 can select the serial data output timing between the rising edge or falling edge of the clock signal according to the setting of the MOD pin.

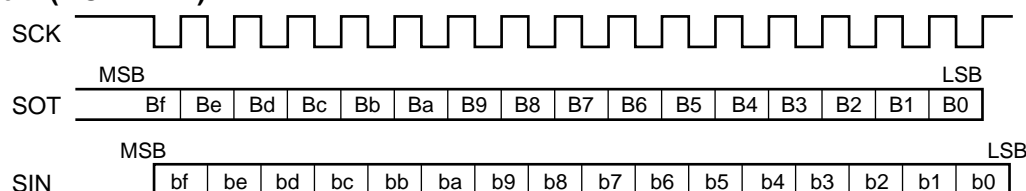
Mode A (MOD = "L")



Serial data is output at the falling edge of the SCK signal.

Note: A/D converted data is not guaranteed if the MOD pin is switched when the ENDC signal is active. Before changing the output mode, make the ENDC inactive or set the RSTX pin level to "L" after switching the MOD pin.

Mode B (MOD = "H")



Serial data is output at the rising edge of the SCK signal.

Note: A/D converted data is not guaranteed if the MOD pin is switched when the ENDC signal is active. Before changing the output mode, make the ENDC inactive or set the RSTX pin level to "L" after switching the MOD pin. The first bit is output when the ENDC signal becomes "H."

7. Extended Serial Interface

The MB88111 can select whether to output A/D converted data or to output data input to the ESIN pin by controlling the CS1 and CS2X pins.

| CS1 | CS2X | SOT pin |
|-----|------|----------------------------|
| H | L | A/D converted data |
| L | L | Connection to the ESIN pin |
| L | H | |
| H | H | |

Note: A/D converted data is not guaranteed if the CS1 or CS2X setting is changed during SCK input.

MB88111

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

($V_{SS} = AGND = 0\text{ V}$)

| Parameter | Symbol | Conditions | Ratings | | Unit |
|----------------------|-----------|--|---------|----------------|------------------|
| | | | Min. | Max. | |
| Power supply voltage | V_{CC} | Based on V_{SS} ($T_a = +25^\circ\text{C}$) | -0.3 | +7.0 | V |
| | AV_{CC} | | -0.3 | +7.0* | V |
| | AV_{RH} | | -0.3 | +7.0* | V |
| Input voltage | V_{IN} | | -0.3 | $V_{CC} + 0.3$ | V |
| Output voltage | V_{OUT} | | -0.3 | $V_{CC} + 0.3$ | V |
| Power consumption | P_D | — | — | 150 | mW |
| Storage temperature | T_{stg} | — | -55 | +150 | $^\circ\text{C}$ |

* : $V_{CC} \geq AV_{CC} \geq AV_{RH}$

2. Recommended Operating Conditions

| Parameter | Symbol | Values | | Unit |
|-----------------------|-----------------------|----------------------|----------------------|------------------|
| | | Min. | Max. | |
| Power supply voltage | V_{CC} AV_{CC} | 3.5* | 5.5* | V |
| | V_{CC} $AGND$ | 0 | 0 | V |
| | AV_{RH} | $AV_{CC} \times 0.8$ | AV_{CC} | V |
| | AV_{RL} | 0 | $AV_{CC} \times 0.2$ | V |
| Operation temperature | T_a | -40 | +105 | $^\circ\text{C}$ |

* : $V_{CC} \geq AV_{CC} \geq AV_{RH}$

3. DC Characteristics

(1) Digital section

($V_{CC} = +3.5\text{ V to }+5.5\text{ V}$, $V_{SS} = \text{AGND} = 0\text{ V}$, $T_a = -40^\circ\text{C to }+105^\circ\text{C}$)

| Parameter | Pin name | Symbol | Conditions | Value | | | Unit |
|----------------------------------|--|------------|---|----------------|------|----------------|---------------|
| | | | | Min. | Typ. | Max. | |
| Power supply voltage | | V_{CC} | — | 3.5 | 5.0 | 5.5 | V |
| Power supply current | V_{CC} | I_{CC} | Operation at CLK = 1 MHz (with no load) | — | 0.5 | 1.5 | mA |
| Low-level input leakage current | MOD, CCLK CS1, CS2X SCK, ESIN SIN | I_{IZL1} | $V_{IN} = V_{SS}$ | -2 | — | 2 | μA |
| | ATGX RSTX | I_{IZL2} | $V_{IN} = V_{SS}$ $V_{CC} = 5.0\text{ V}$ | -200 | -100 | -50 | μA |
| High-level input leakage current | MOD, CCLK CS1, CS2X SCK, ESIN SIN, ATGX RSTX | I_{IZL1} | $V_{IN} = V_{CC}$ | -2 | — | 2 | μA |
| Low-level input voltage | MOD, ESIN CS1, CS2X | V_{IL} | — | $V_{SS} - 0.3$ | — | $0.3 V_{CC}$ | V |
| | SCK, CCLK SIN, ATGX RSTX, * | V_{ILS} | — | $V_{SS} - 0.3$ | — | $0.2 V_{CC}$ | V |
| High-level input voltage | MOD, ESIN CS1, CS2X | V_{IH} | — | $0.7 V_{CC}$ | — | $V_{CC} + 0.3$ | V |
| | SCK, CCLK SIN, ATGX RSTX, * | V_{IHS} | — | $0.8 V_{CC}$ | — | $V_{CC} + 0.3$ | V |
| Hysteresis width | SCK, CCLK SIN, ATGX RSTX, * | V_{HYS} | — | $0.02 V_{CC}$ | — | $0.3 V_{CC}$ | V |
| Low-level output voltage | SOT | V_{OL} | $I_{OL} = 2.5\text{ mA}$ | — | — | 0.4 | V |
| High-level output voltage | IRQX ENDC | V_{OH} | $I_{OH} = -400\ \mu\text{A}$ | $V_{CC} - 0.4$ | — | — | V |

* : AN16 to AN23 (port input mode)

(2) Analog section

($AV_{CC}, V_{CC} = +3.5\text{ V to }+5.5\text{ V}$ ($V_{CC} \geq AV_{CC}$), $V_{SS} = AGND = 0\text{ V}$, $T_a = -40^\circ\text{C to }+105^\circ\text{C}$)

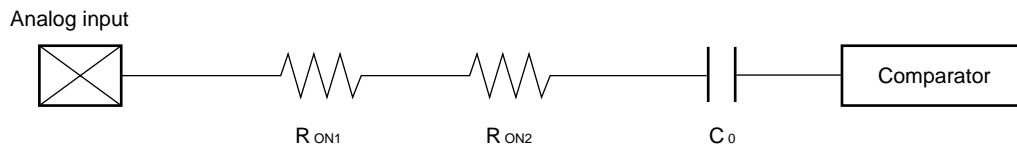
| Parameter | Pin name | Symbol | Conditions | Value | | | Unit | |
|----------------------------------|-------------|--------|--------------|---------------|------|---------------|---------------|-----|
| | | | | Min. | Typ. | Max. | | |
| Resolution | AN0 to AN23 | — | — | — | 10 | — | bits | |
| Monotonic increase | | — | — | — | 10 | — | bits | |
| Linearity error | | — | — | — | — | — | ± 1 | LSB |
| Differential linearity error | | — | — | — | — | — | ± 1 | LSB |
| Full-scale transition error | | — | — | — | — | — | $\pm 1/2$ | LSB |
| Zero-transition error | | — | — | — | — | — | $\pm 1/2$ | LSB |
| Total error | | — | — | — | — | — | ± 2 | LSB |
| Conversion time | — | — | CCLK = 1 MHz | — | — | 50 | μs | |
| Input clock frequency | CCLK | — | — | 800 | 1000 | 1200 | KHz | |
| Supply current | AV_{CC} | IA | — | — | 3.0 | 6.0 | mA | |
| Reference voltage supply current | AVRH | IR | — | — | 150 | 300 | μA | |
| Analog reference voltage | AVRH | — | — | $0.8 AV_{CC}$ | — | AV_{CC} | V | |
| | AVRL | — | — | 0 | — | $0.2 AV_{CC}$ | V | |
| Analog input voltage | AN0 to AN23 | — | — | AVRL | — | AVRH | V | |
| Multiplexer OFF-leakage current | | — | — | -200 | — | 200 | nA | |

- No missing code is guaranteed.

Notes: • If the output impedance of the external input is too high, the analog voltage sampling time may be insufficient.

- In the power-on sequence, turn the power supply for the digital system first before turning that for the analog system on.

Analog input equivalent circuit



- $R_{ON1} = \text{About } 1.5\text{ k}\Omega$
- $R_{ON2} = \text{About } 1.5\text{ k}\Omega$
- $C_0 = \text{About } 15\text{ pF}$

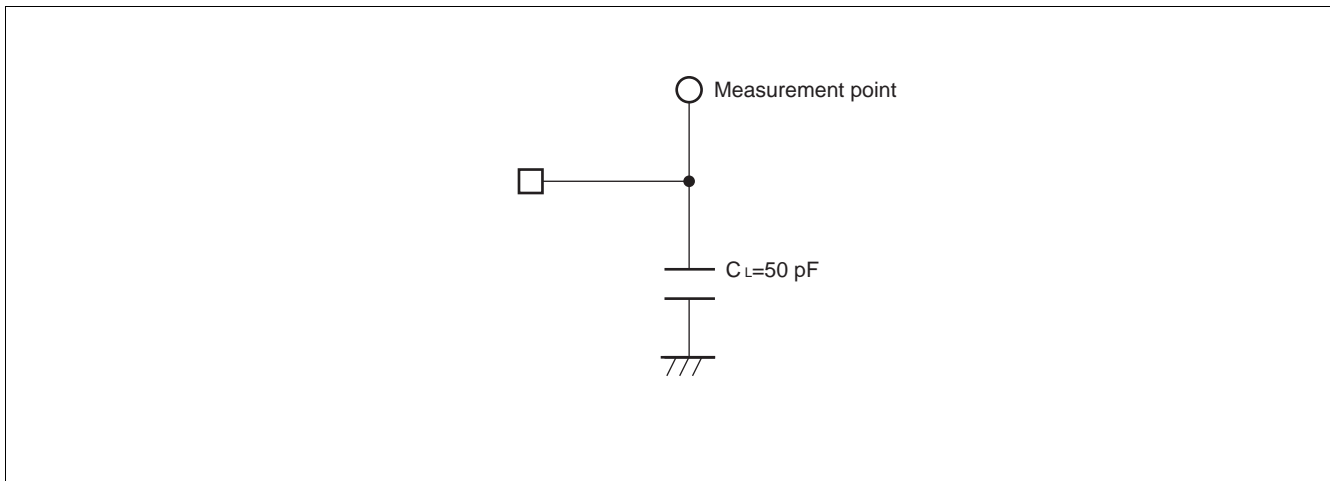
Note: The above values are reference values.

4. AC Characteristics

($V_{CC}, V_{CC} = +3.5\text{ V to }+5.5\text{ V}$ ($V_{CC} \geq AV_{CC}$), $V_{SS} = AGND = 0\text{ V}$, $T_a = -40^\circ\text{C to }+105^\circ\text{C}$)

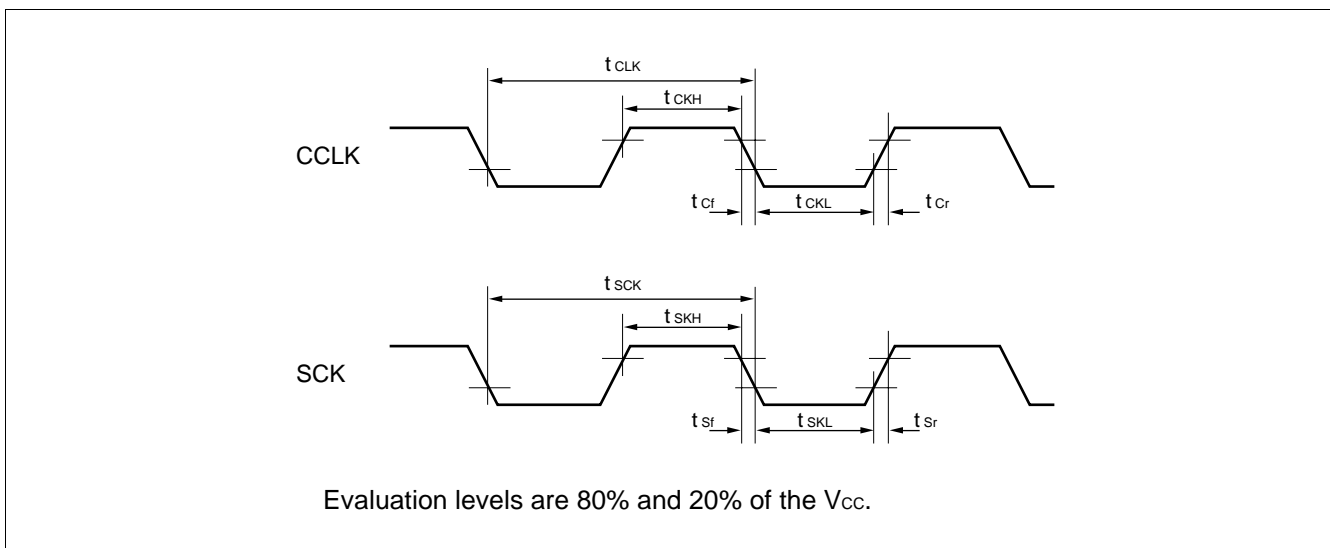
| Parameter | Symbol | Conditions | Values | | Unit |
|---|------------|------------------------|--------|------|---------------|
| | | | Min. | Max. | |
| CCLK clock cycle time | f_{CLK} | $f_{CLK} = 1/f_{CLK}$ | 800 | 1200 | KHz |
| Low-level CCLK clock pulse width | t_{CKL} | — | 400 | — | ns |
| High-level CCLK clock pulse width | t_{CKH} | — | 400 | — | ns |
| CCLK clock rise time | t_{Cr} | — | — | 10 | ns |
| CCLK clock fall time | t_{Cf} | | | | |
| SCK clock cycle time | f_{SCK} | $t_{SCK} = 1/f_{SCK}$ | 400 | 1200 | KHz |
| Low-level SCK clock pulse width | t_{SKL} | — | 400 | — | ns |
| High-level SCK clock pulse width | t_{SKH} | — | 400 | — | ns |
| SCK clock rise time | t_{Sr} | — | — | 10 | ns |
| SCK clock fall time | t_{Sf} | | | | |
| SIN setup time | t_{SIS} | — | 50 | — | ns |
| SIN hold time | t_{SIH} | — | 250 | — | ns |
| Command interval | t_{COM} | CCLK = 1 MHz | 4 | — | μs |
| ENDC reset time | t_{ENR} | See "Load conditions." | — | 1 | μs |
| RSTX pulse width | t_{RSH} | — | 100 | — | ns |
| RSTX $\uparrow \rightarrow$ SCK \downarrow time | t_{RSS} | — | 1 | — | μs |
| SCK $\uparrow \rightarrow$ CS1 \downarrow time SCK $\uparrow \rightarrow$ CS2X \uparrow time | t_{CSS} | — | 500 | — | ns |
| CS1 $\uparrow \rightarrow$ SCK \downarrow time CS2X $\downarrow \rightarrow$ SCK \downarrow time | t_{CSH} | — | 500 | — | ns |
| SOT output delay time (mode A) | t_{SODA} | See "Load conditions." | — | 300 | ns |
| SOT output delay time (mode B) | t_{SODB} | See "Load conditions." | — | 300 | ns |
| ENDC $\uparrow \rightarrow$ SOT output (mode B) | t_{SOHB} | See "Load conditions." | — | 200 | ns |
| STC command A/D conversion time | t_{STC} | CCLK = 1 MHz | — | 50 | μs |
| ATC command A/D conversion time | t_{SATC} | CCLK = 1 MHz | — | 50 | μs |
| ATGX setup time | t_{SATS} | CCLK = 1 MHz | 4 | — | μs |
| ATGX hold time | t_{SATH} | CCLK = 1 MHz | 2 | — | μs |
| Port input evaluation time | t_{POT} | CCLK = 1 MHz | — | 10 | μs |
| Port input setup time | t_{PTS} | — | 0 | — | ns |
| Port input hold time | t_{PTH} | — | 0 | — | ns |
| Extended serial HL propagation delay | t_{SHL} | See "Load conditions." | — | 100 | ns |
| Extended serial LH propagation delay | t_{SLH} | See "Load conditions." | — | 100 | ns |
| Noise filter width | t_{INF} | — | 15 | — | ns |

AC Test Condition

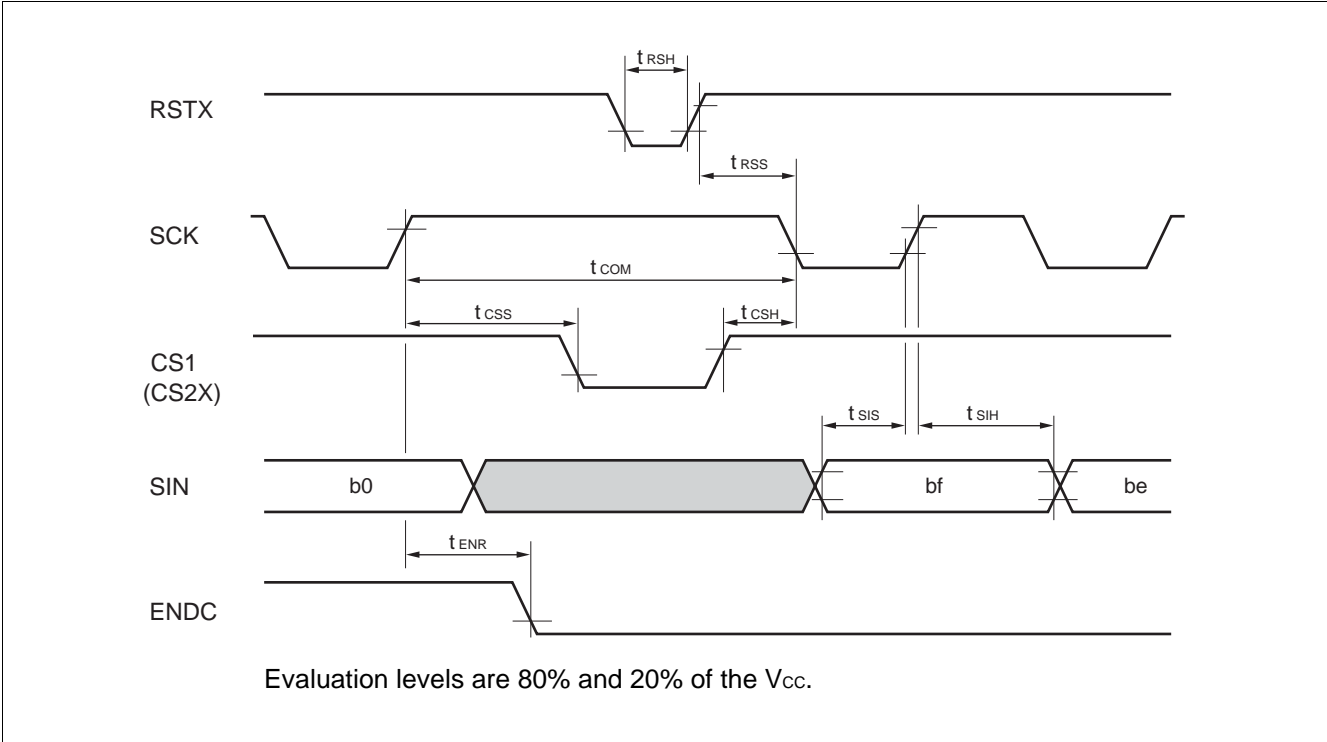


■ TIMING DIAGRAM

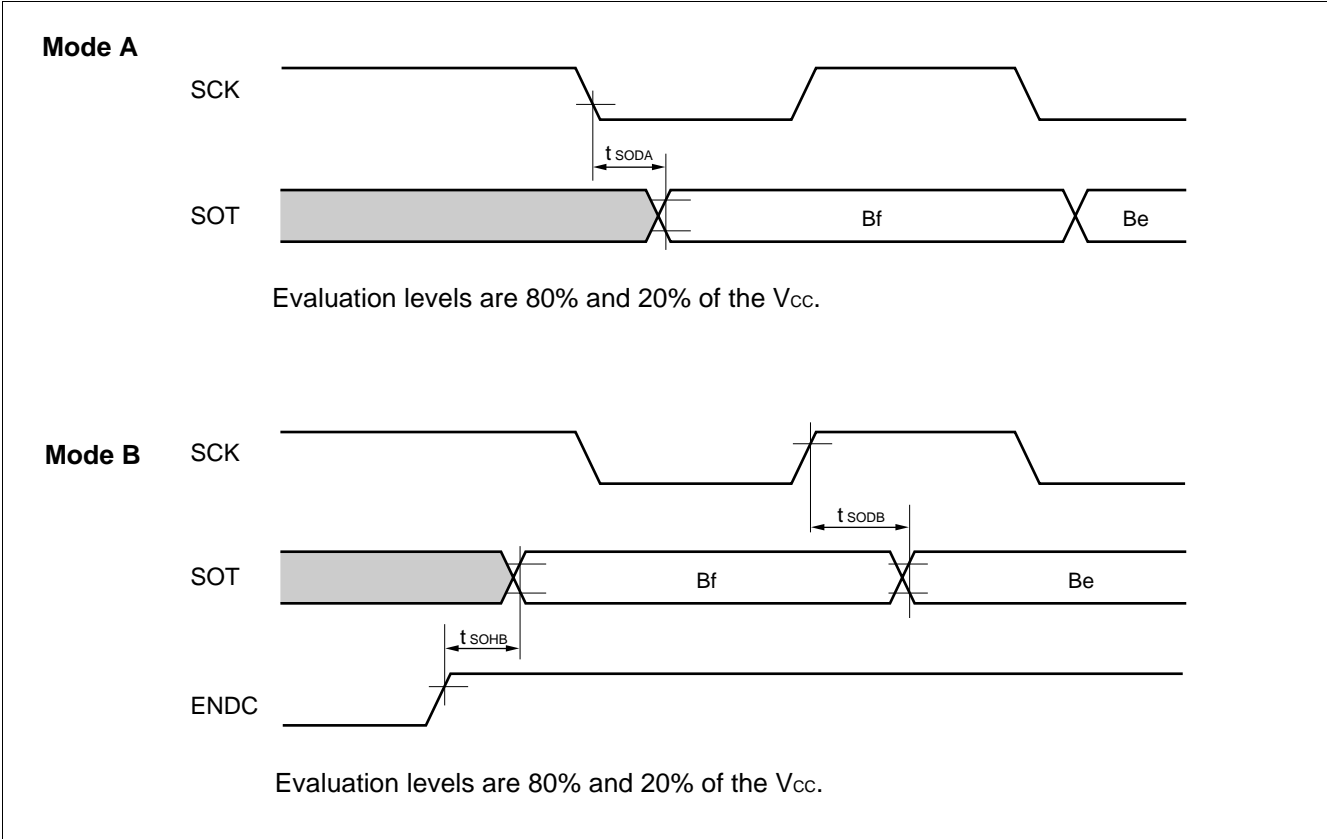
1. Input Clock Timing



2. Serial Data Input Timing

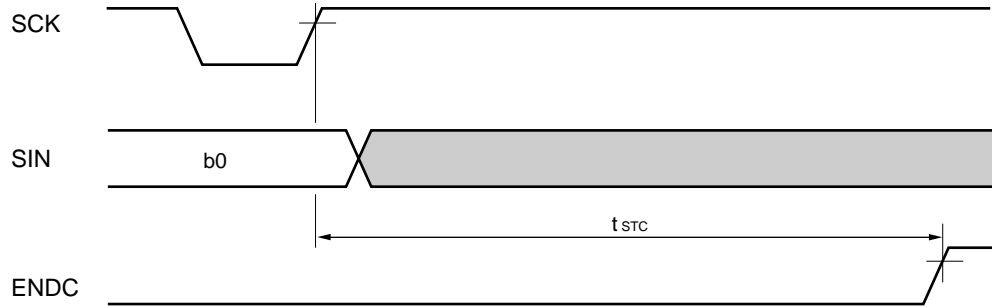


3. Serial Data Output Timing



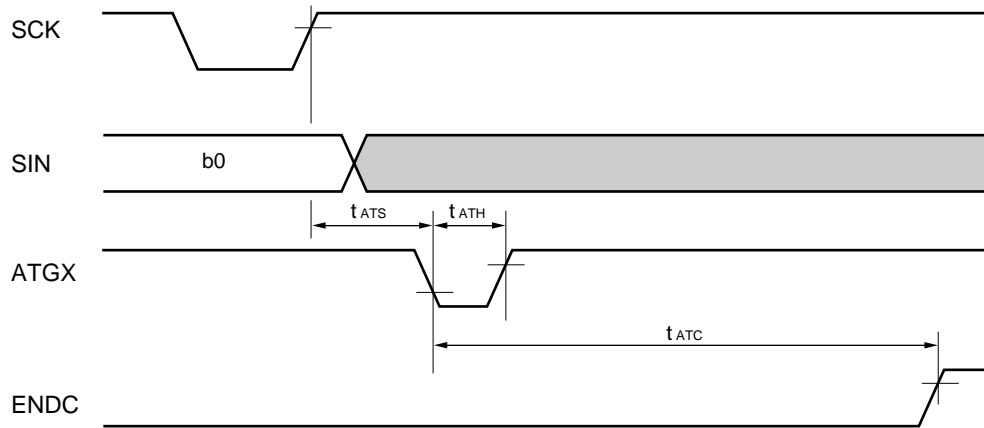
4. A/D Conversion and Port Input Evaluation

STC command (normal mode)



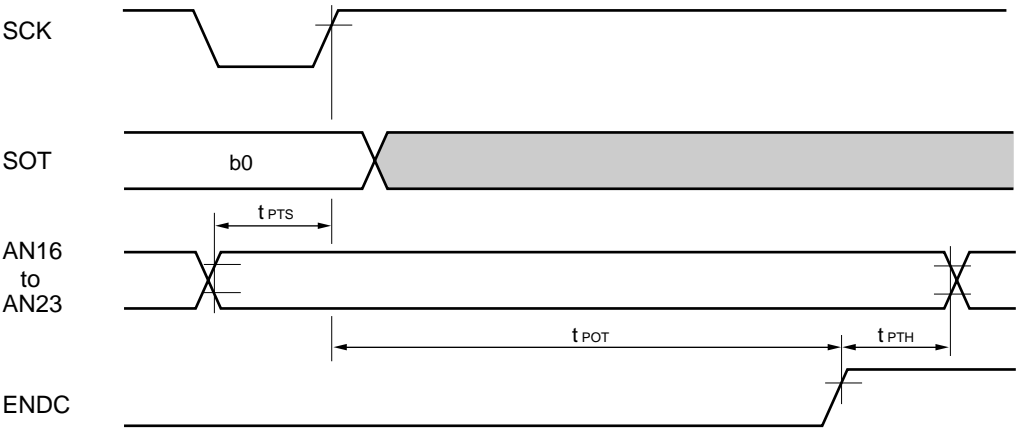
Evaluation levels are 80% and 20% of the V_{CC} .

ATC command



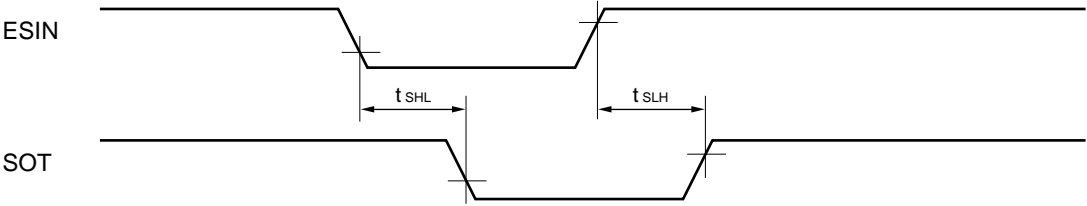
Evaluation levels are 80% and 20% of the V_{CC} .

STC command (port input mode)



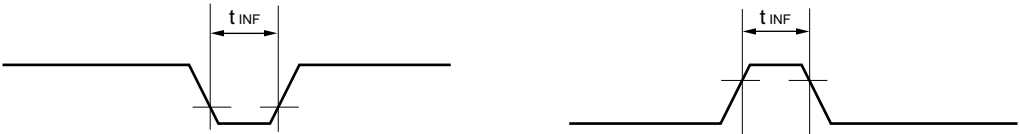
Evaluation levels are 80% and 20% of the V_{CC} .

5. Extended Serial Interface



Evaluation levels are 80% and 20% of the V_{CC} .

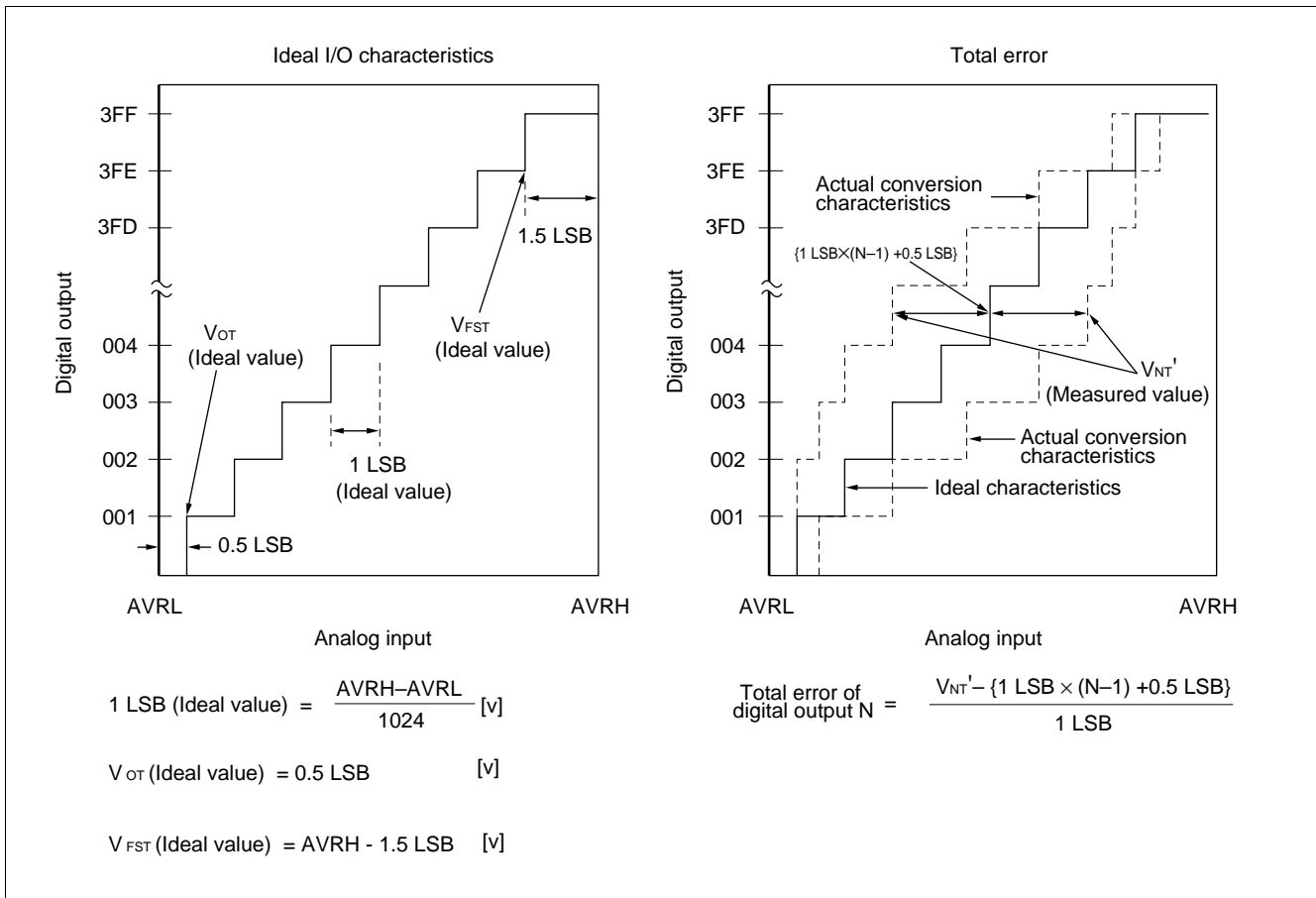
6. Noise Filter



Evaluation levels are 80% and 20% of the V_{CC} .

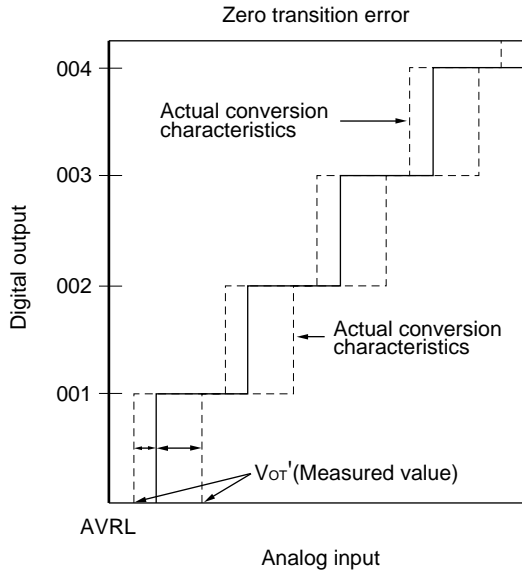
■ DEFINITIONS OF A/D CONVERTER TERMS

- Resolution
Analog transition identifiable by the A/D converter
- Linearity error
Deviation of the straight line drawn between the zero transition point (00 0000 0000 ↔ 00 0000 0001) and the full-scale transition point (11 1111 1110 ↔ 11 1111 1111) of the device from actual conversion characteristics
- Differential linearity error
Deviation from the ideal input voltage required to shift output code by one LSB
- Total error
Difference between actual and logical values. This error is caused by a zero transition error, full-scale transition error, linearity error, quantum error, and by noise.

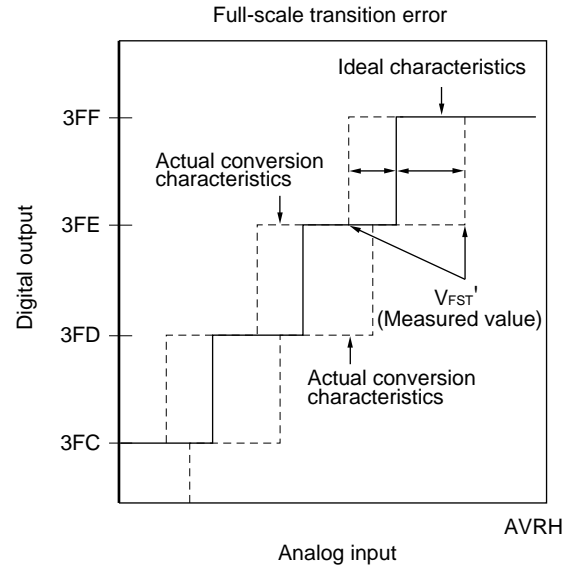


(Continued)

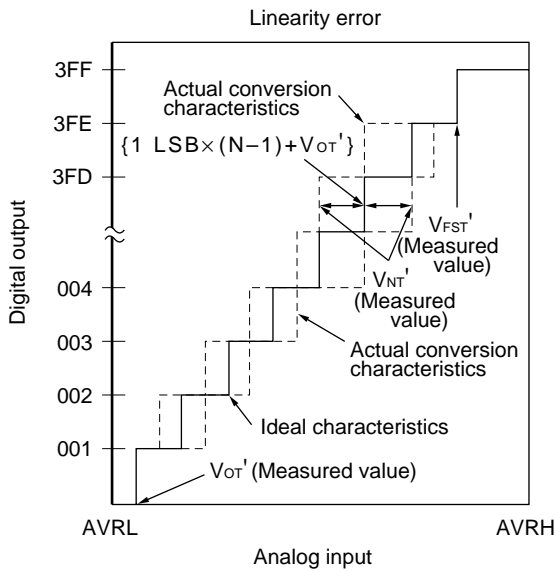
(Continued)



$$\text{Zero transition error} = \frac{V_{OT}' - 0.5 \text{ LSB}}{1 \text{ LSB}}$$

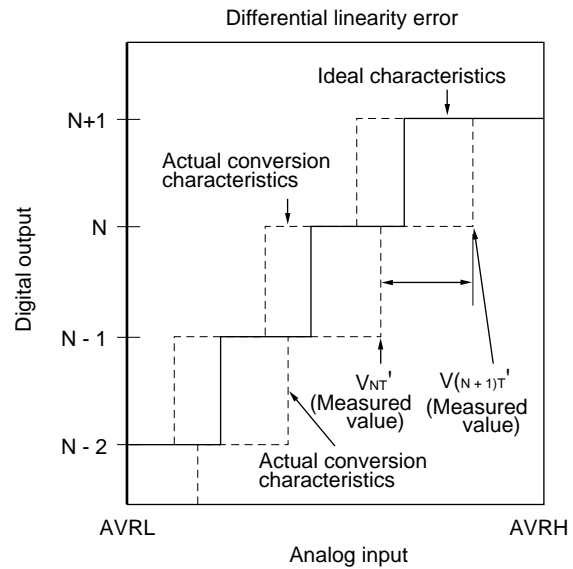


$$\text{Full scale transition error} = \frac{V_{FST}' - (\text{AVRH} - 1.5 \text{ LSB})}{1 \text{ LSB}}$$



$$\text{Linearity error of digital output } N = \frac{V_{NT}' - \{1 \text{ LSB}' \times (N-1) + V_{OT}'\}}{1 \text{ LSB}'}$$

$$1 \text{ LSB}' = \frac{V_{FST}' - V_{OT}'}{1022} [\text{V}]$$



$$\text{Differential linearity error of digital output } N = \frac{V_{(N+1)T}' - V_{NT}'}{1 \text{ LSB}'} - 1$$

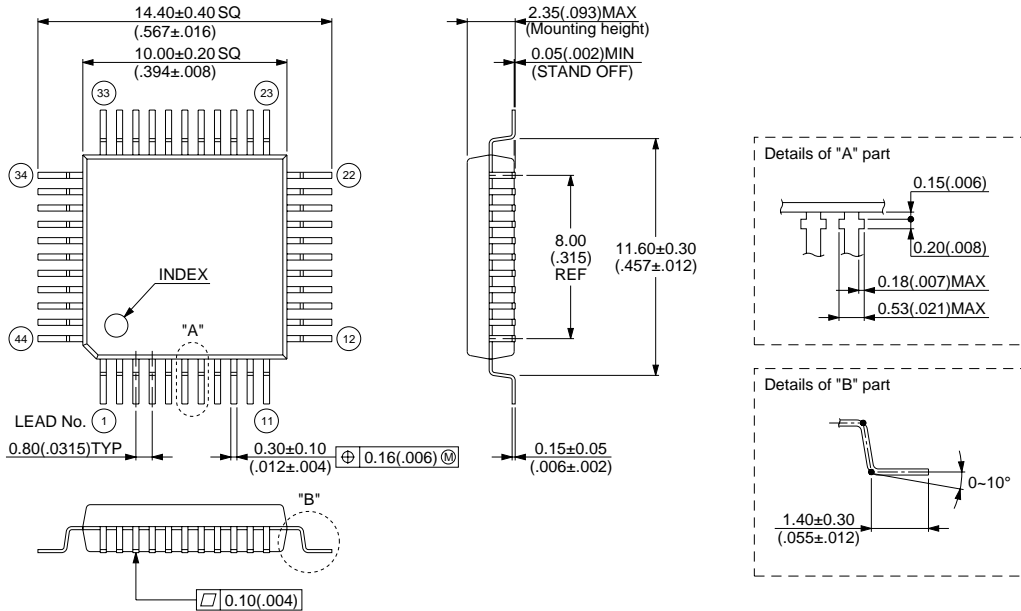
MB88111

■ ORDERING INFORMATION

| Part number | Package | Remarks |
|-------------|---|---------|
| MB88111PFQ | 44-pin, Plastic QFP (FPT-44P-M11) | |
| MB88111P-SH | 48-pin, Plastic SH-DIP (DIP-48P-M01) | |

■ PACKAGE DIMENSIONS

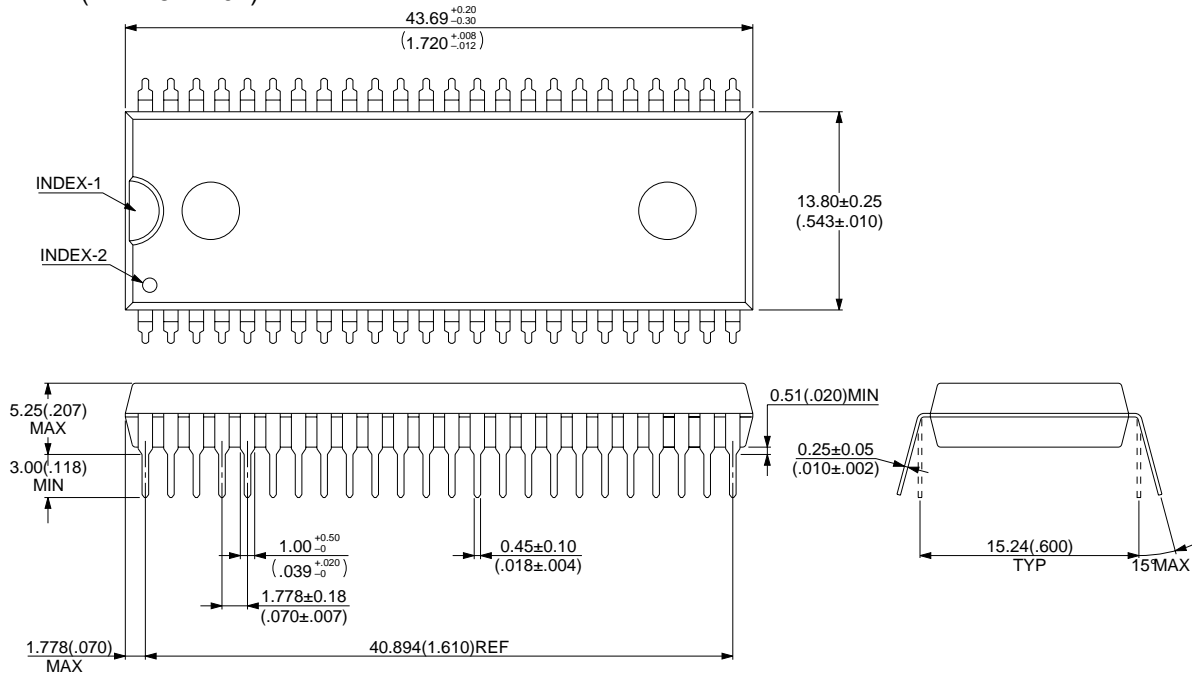
44-pin, Plastic QFP
(FPT-44P-M11)



© 1994 FUJITSU LIMITED F44018S-1C-1

Dimensions in mm (inches).

48-pin, Plastic SH-DIP
(DIP-48P-M01)



© 1994 FUJITSU LIMITED D48002S-3C-3

Dimensions in mm (inches).

MEMO

MEMO

FUJITSU MICROELECTRONICS LIMITED

Shinjuku Dai-Ichi Seimei Bldg. 7-1, Nishishinjuku 2-chome, Shinjuku-ku,
Tokyo 163-0722, Japan Tel: +81-3-5322-3347 Fax: +81-3-5322-3387
<http://jp.fujitsu.com/fml/en/>

For further information please contact:

North and South America

FUJITSU MICROELECTRONICS AMERICA, INC.
1250 E. Arques Avenue, M/S 333
Sunnyvale, CA 94085-5401, U.S.A.
Tel: +1-408-737-5600 Fax: +1-408-737-5999
<http://www.fma.fujitsu.com/>

Europe

FUJITSU MICROELECTRONICS EUROPE GmbH
Pittlerstrasse 47, 63225 Langen,
Germany
Tel: +49-6103-690-0 Fax: +49-6103-690-122
<http://emea.fujitsu.com/microelectronics/>

Korea

FUJITSU MICROELECTRONICS KOREA LTD.
206 KOSMO TOWER, 1002 Daechi-Dong,
Kangnam-Gu, Seoul 135-280
Korea
Tel: +82-2-3484-7100 Fax: +82-2-3484-7111
<http://www.fmk.fujitsu.com/>

Asia Pacific

FUJITSU MICROELECTRONICS ASIA PTE LTD.
151 Lorong Chuan, #05-08 New Tech Park,
Singapore 556741
Tel: +65-6281-0770 Fax: +65-6281-0220
<http://www.fujitsu.com/sg/services/micro/semiconductor/>

FUJITSU MICROELECTRONICS SHANGHAI CO., LTD.
Rm.3102, Bund Center, No.222 Yan An Road(E),
Shanghai 200002, China
Tel: +86-21-6335-1560 Fax: +86-21-6335-1605
<http://cn.fujitsu.com/fmc/>

FUJITSU MICROELECTRONICS PACIFIC ASIA LTD.
10/F., World Commerce Centre, 11 Canton Road
Tsimshatsui, Kowloon
Hong Kong
Tel: +852-2377-0226 Fax: +852-2376-3269
<http://cn.fujitsu.com/fmc/tw>

All Rights Reserved.

The contents of this document are subject to change without notice.

Customers are advised to consult with sales representatives before ordering.

The information, such as descriptions of function and application circuit examples, in this document are presented solely for the purpose of reference to show examples of operations and uses of FUJITSU MICROELECTRONICS device; FUJITSU MICROELECTRONICS does not warrant proper operation of the device with respect to use based on such information. When you develop equipment incorporating the device based on such information, you must assume any responsibility arising out of such use of the information.

FUJITSU MICROELECTRONICS assumes no liability for any damages whatsoever arising out of the use of the information.

Any information in this document, including descriptions of function and schematic diagrams, shall not be construed as license of the use or exercise of any intellectual property right, such as patent right or copyright, or any other right of FUJITSU MICROELECTRONICS or any third party or does FUJITSU MICROELECTRONICS warrant non-infringement of any third-party's intellectual property right or other right by using such information. FUJITSU MICROELECTRONICS assumes no liability for any infringement of the intellectual property rights or other rights of third parties which would result from the use of information contained herein.

The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for use requiring extremely high reliability (i.e., submersible repeater and artificial satellite).

Please note that FUJITSU MICROELECTRONICS will not be liable against you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products.

Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Exportation/release of any products described in this document may require necessary procedures in accordance with the regulations of the Foreign Exchange and Foreign Trade Control Law of Japan and/or US export control laws.

The company names and brand names herein are the trademarks or registered trademarks of their respective owners.