PUMA 84SV64000 - 012/015/020

Issue 1.1 November 2002

Description

The PUMA 84 range of devices provide a high density, surface mount memory solution with density up to twice that of standard monolithic devices.

The PUMA 84 may accomodate various memory technologies including SRAM, FLASH and EEPROM. The devices are designed to offer a defined upgrade path and may be user configured as 8, 16 or 32 bits wide using four Chip Selects (/CS1~4).

The PUMA84SV64000 is a 2Mx32 SRAM module housed in a JEDEC 84 pin surface mount J-leaded PLCC. Access times of 12, 15 or 20ns are available.

The device is available to commercial and industrial temperature grade.

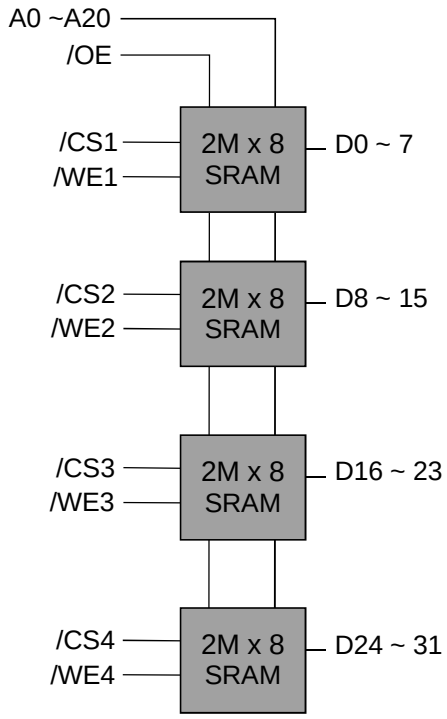
Features

ï Access times of 12/15/20 ns.
ï 3.3V ± 10%.
ï Comercial and Industrial temperature grades
ï JEDEC 84 ëJí Leaded surface mount package.
ï May be organised as 2M x 32, 4M x 16 and 8M X 8
ï Operating Power (32 Bit) 6.34W (max)
ï Low power standby. (CMOS) 90mW (max)
ï Completely Static Operation.

Package Details

PUMA 84 - Plastic 84 ëJí Leaded Package.
Max. Dimensions - 30.35 x 30.35 x 5.08 (max)
All Dimensions in mm.

Block Diagram



Pin Definition

See page 2.

Pin Functions

Description	Signal
Address Input	A0~A20
Data Input/Output	D0~D31
Chip Select	/CS1~4
Write Enable	/WE1~4
Output Enable	/OE
No Connect	NC
Power	V_{CC}
Ground	GND

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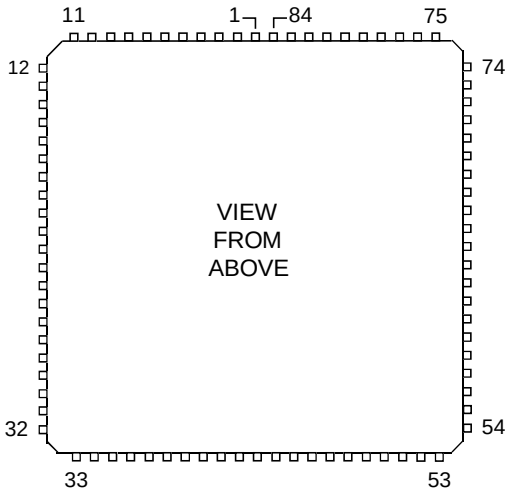
Pin Definition - PUMA84SV64000

Pin	Signal	Pin	Signal
1	V_{CC}	43	V_{CC}
2	/WE2	44	A13
3	/CS1	45	A12
4	/CS2	46	A11
5	/CS3	47	A10
6	/CS4	48	A9
7	A17	49	A8
8	A18	50	A7
9	D16	51	D0
10	A19	52	/WE4
11	A20	53	NC
12	NC	54	NC
13	NC	55	NC
14	D17	56	D1
15	D18	57	D2
16	D19	58	D3
17	GND	59	GND
18	D20	60	D4
19	D21	61	D5
20	D22	62	D6
21	D23	63	D7
22	V_{CC}	64	V_{CC}
23	D24	65	D8
24	D25	66	D9
25	D26	67	D10
26	D27	68	D11
27	GND	69	GND
28	D28	70	D12
29	D29	71	D13
30	D30	72	D14
31	NC	73	NC
32	NC	74	NC
33	NC	75	D15
34	/WE3	76	A14
35	D31	77	A15
36	A6	78	A16
37	A5	79	/WE1
38	A4	80	/OE
39	A3	81	NC
40	A2	82	NC
41	A1	83	NC
42	A0	84	NC



Absolute Maximum Ratings(1)

Parameter	Symbol	Min		Max	Unit
Voltage on any pin relative to V_{SS}	V_T	-0.5	to	+4.6	V
Power Dissipation	P_T		7.2		W
Storage Temperature	T_{STG}	-55	to	+125	^{O}C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	
Supply Voltage	V_{CC}	3.0	3.3	3.6	V	
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.3	V	
Input Low Voltage	V_{IL}	-0.3	-	0.8	V	
Operating Temperature	T_A	0	-	70	^{O}C	
	T_{AI}	-40	-	85	^{O}C	(I Suffix)

DC Electrical Characteristics

(V_{CC}=3.3V±10%, T_A=-40^{O}C to +85^{O}C)

Parameter		Symbol	Test Condition	Min	Typ	Max	Units
Input Leakage Current		I_{LI}	V_{IN} = GND to V_{CC}	-8	-	8	µA
Output Leakage Current		I_{LO}	/CS=V_{IH} or /OE=V_{IH} or /WE=V_{IL}, V_{OUT}= GND to V_{CC}	-8	-	8	µA
Operating Supply Current	32 Bit	I_{CC32}	Min. Cycle, 100% Duty /CS=V_{IL}, V_{IN}=V_{IH} or V_{IL}, I_{OUT}=0mA	-	-	1760	mA
	16 Bit	I_{CC16}	As Above.	-	-	1120	mA
	8 Bit	I_{CC8}	As Above.	-	-	800	mA
Standby Supply Current	TTL	I_{SB}	Min. Cycle, /CS=V_{IH}	-	-	480	mA
	CMOS	I_{SB1}	f=0MHz, /CS≥V_{CC}-0.2V, V_{IN}≥V_{CC}-0.2V or V_{IN}≤ 0.2V	-	-	25	mA
Output Voltage Low		V_{OL}	I_{OL}=2.0mA	-	-	0.4	V
			I_{OL}= 100µA			0.2	V
Output Voltage High		V_{OH}	I_{OH}= -2.0mA	2.4	-	-	V
			I_{OH}= -100µA	V_{CC}-0.2			V

Notes (1) /CS should be used in pairs for 16 bit mode or use /CS1~4 for 32 bit operation.

Capacitance

(V_{CC} = 3.3V ± 10%, T_A = 25°C)

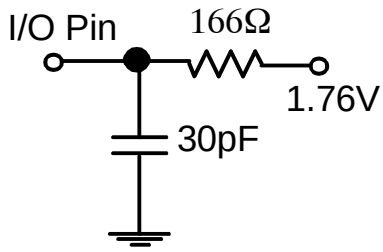
Parameter		Symbol	Test Condition	Min	Typ	Max	Unit
Input Capacitance	Address, /OE	C_{IN1}	V_{IN}=0V	-	-	34	pF
Input Capacitance	/CS1~4, /WE1~4	C_{IN2}	V_{IN}=0V	-	-	18	pF
Output Capacitance	8 bit mode (worst case)	$C_{I/O}$	$V_{I/O}$=0V	-	-	42	pF

Note : These Parameters are calculated not measured.

Test Conditions

- Input pulse levels : 0V to 3.0V
- Input rise and fall times : 2ns
- Input and Output timing reference levels : 1.5V
- Output Load : See Load Diagram.
- V_{CC} = 3.3V±10%

Output Load



Operation Truth Table

/CS	/OE	/WE	Data Pins	Supply Current	Mode
H	X	X	High Impedance	I_{SB},I_{SB1}	Standby
L	L	H	Data Out	I_{CC32},I_{CC16},I_{CC8}	Read
L	H	L	Data In	I_{CC32},I_{CC16},I_{CC8}	Write
L	L	L	Data In	I_{CC32},I_{CC16},I_{CC8}	Write
L	H	H	High Impedance	I_{CC32},I_{CC16},I_{CC8}	High Z

Notes : H = V_{IH} : L = V_{IL} : X = V_{IH} or V_{IL}

Read Cycle

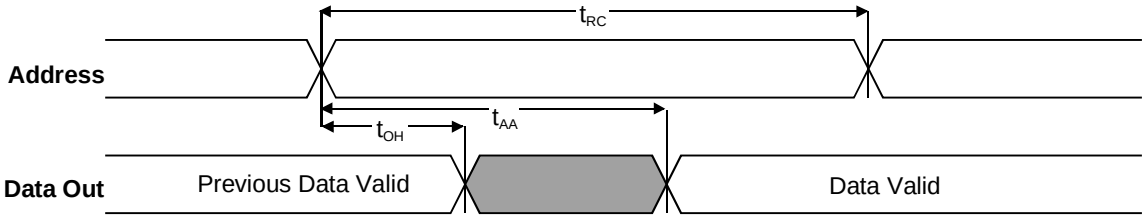
		012		015		020		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Units
Read Cycle Time	t_{RC}	12	-	15	-	20	-	ns
Address Access Time	t_{AA}	-	12	-	15	-	20	ns
Chip Select Access Time	t_{ACS}	-	12	-	15	-	20	ns
Output Enable to Output Valid	t_{OE}	-	6	-	8	-	10	ns
Output Hold From Address Change	t_{OH}	3	-	3	-	3	-	ns
Chip Selection to Output in Low Z	t_{CLZ}	3	-	3	-	3	-	ns
Output Enable to Output in Low Z	t_{OLZ}	0	-	0	-	0	-	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	7	0	8	0	9	ns
Output Disable to Output in High Z	t_{OHZ}	0	7	0	8	0	9	ns

Write Cycle

		012		015		020		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Units
Write Cycle Time	t_{WC}	12	-	15	-	20	-	ns
Chip Selection to End of Write	t_{CW}	10	-	12	-	15	-	ns
Address Valid to End of Write	t_{AW}	10	-	12	-	15	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	8	-	10	-	12	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Write to Output in High Z	t_{WHZ}	0	7	0	8	0	9	ns
Data to Write Time Overlap	t_{DW}	7	-	8	-	9	-	ns
Data Hold time from Write Time	t_{DH}	0	-	0	-	0	-	ns
Output Active from End of Write	t_{OW}	1	-	1	-	1	-	ns

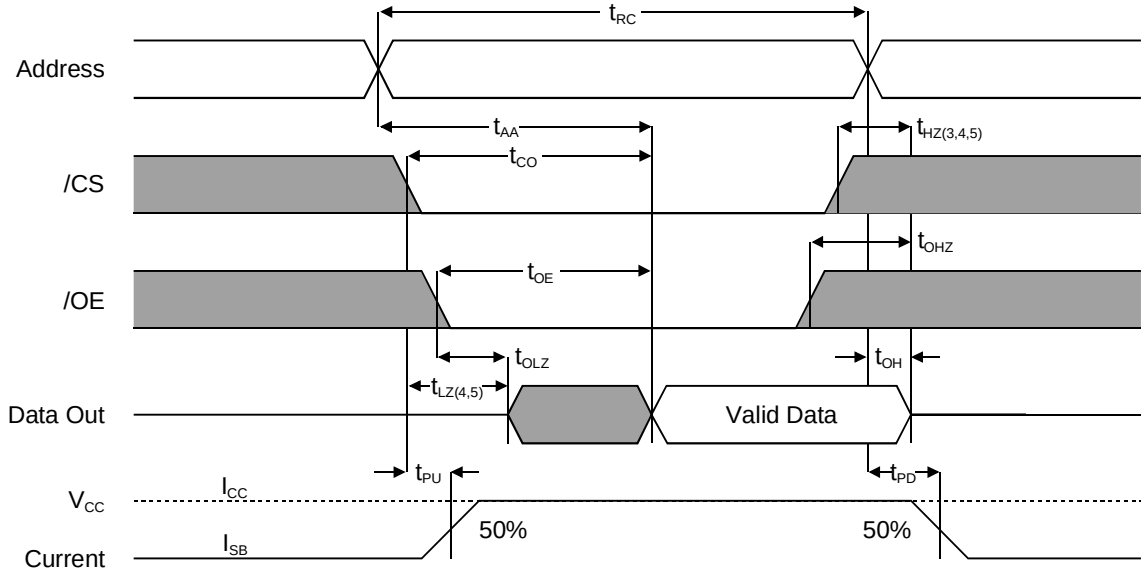
Read Cycle 1

(Address Controlled, /CS=/OE=V_{IL}, /WE=V_{IH})



Read Cycle 2

(/WE = V_{IH})

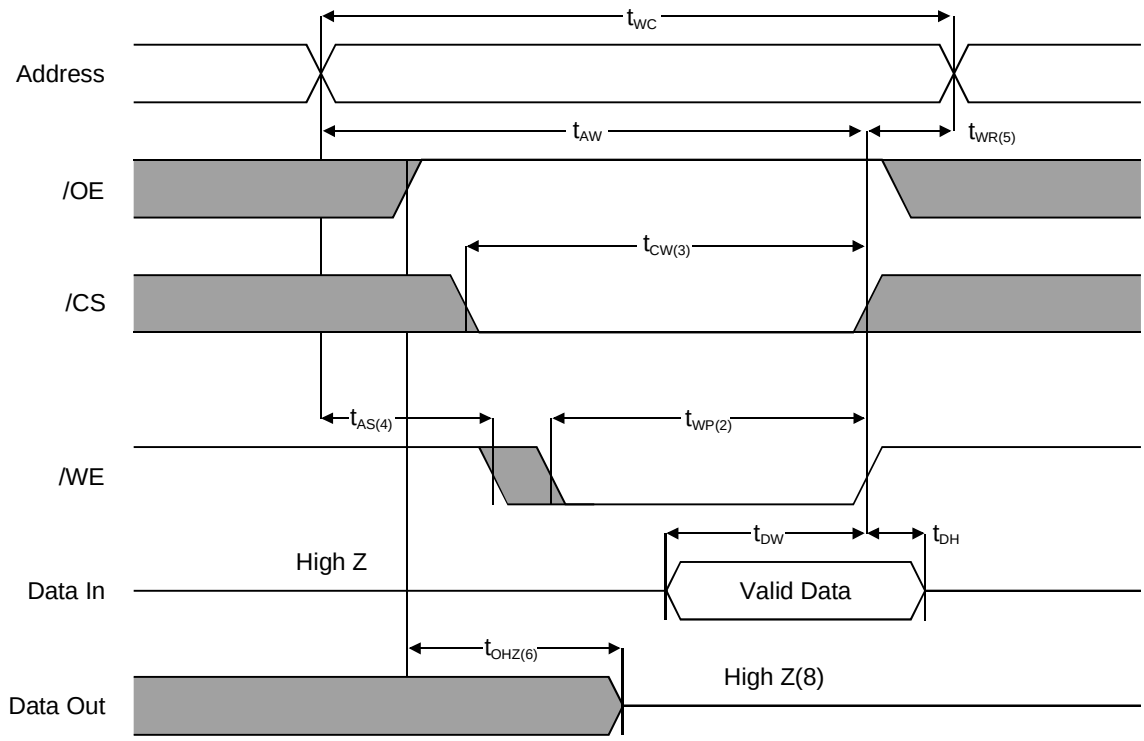


NOTES(READ CYCLE)
1. /WE is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device.
5. Transition is measured **±**200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with /CS=V_{IL}.
7. Address valid prior to coincident with /CS transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

Note: /CS = /CS1~4, /WE = /WE1~4

Write Cycle 1

(/OE = Clock)



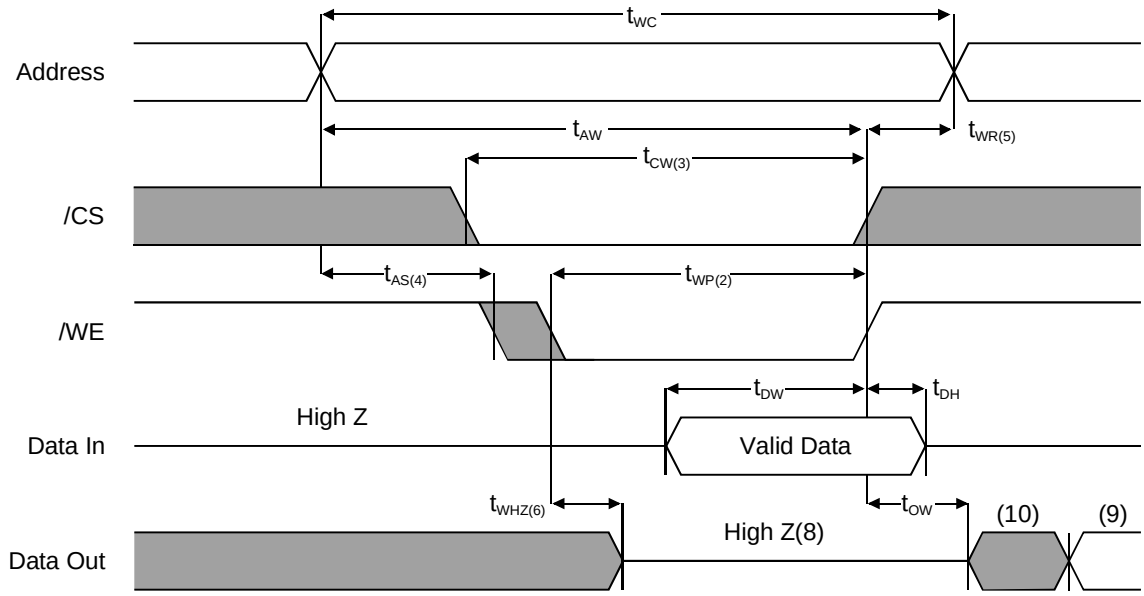
NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low /CS and /WE. A write begins at the latest transition /CS going low and /WE going low ; A write ends at the earliest transition /CS going high or /WE going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of /CS going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as /CS or /WE going high.
6. If /OE, /CS and /WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If /CS goes low simultaneously with /WE going or after /WE going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When /CS is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

Note: /CS = /CS1~4, /WE = /WE1~4

Write Cycle 2

(/OE = Low Fixed)



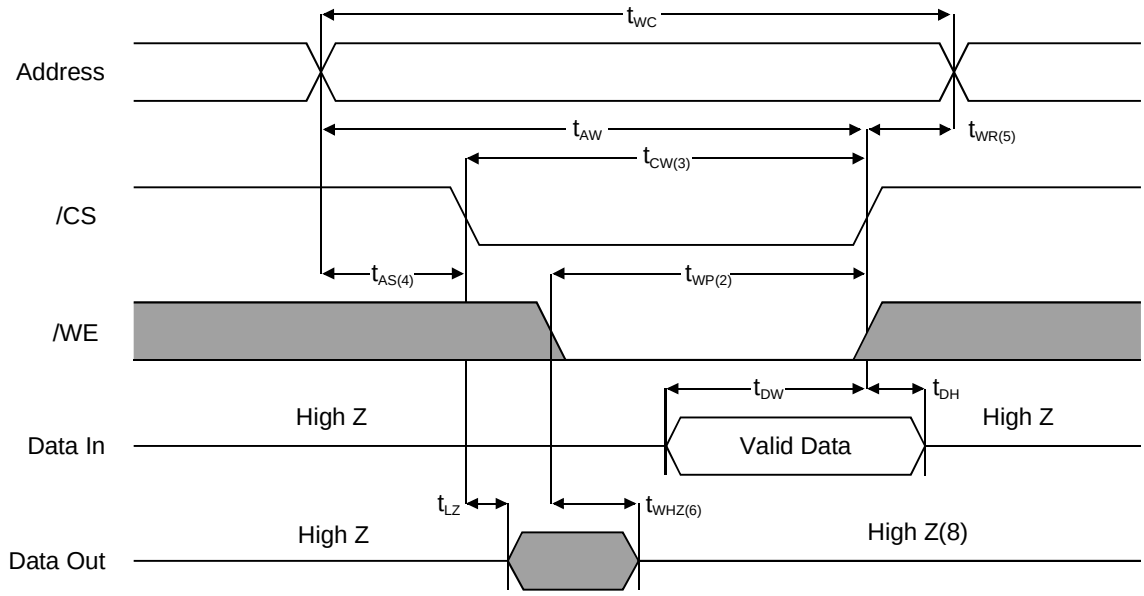
NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low /CS and /WE. A write begins at the latest transition /CS going low and /WE going low ; A write ends at the earliest transition /CS going high or /WE going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of /CS going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as /CS or /WE going high.
6. If /OE, /CS and /WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If /CS goes low simultaneously with /WE going or after /WE going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When /CS is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

Note: /CS = /CS1~4, /WE = /WE1~4

Write Cycle 3

(/CS = Controlled)

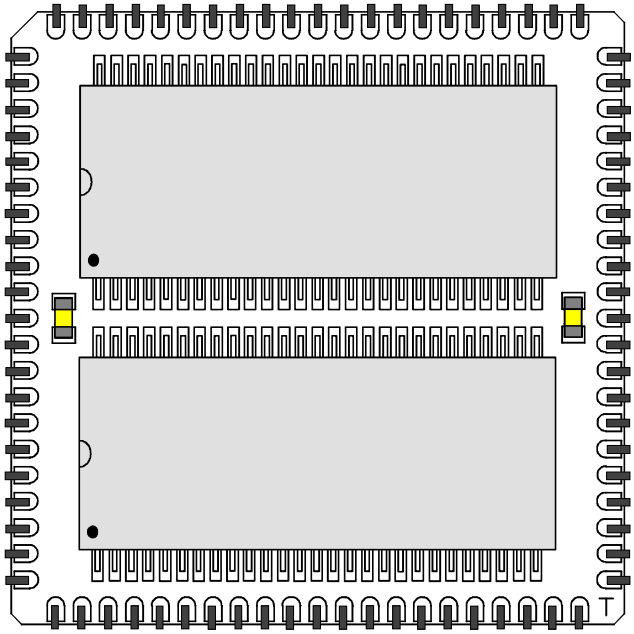


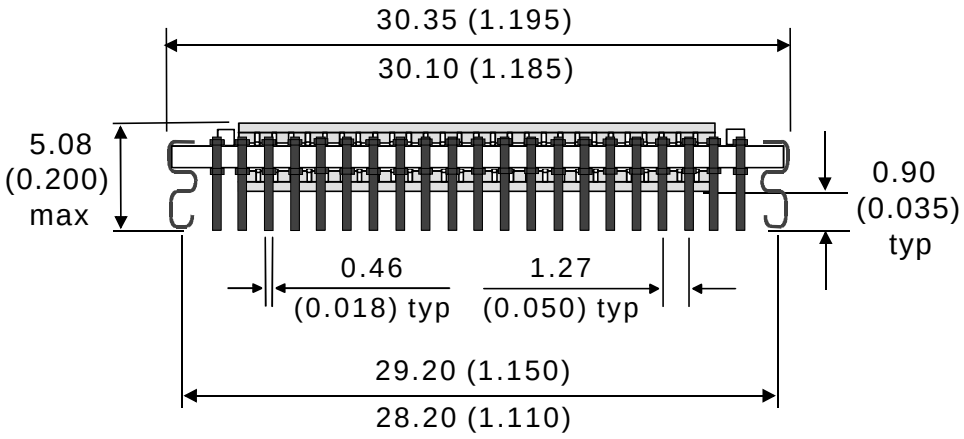
NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low /CS and /WE. A write begins at the latest transition /CS going low and /WE going low ; A write ends at the earliest transition /CS going high or /WE going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of /CS going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as /CS or /WE going high.
6. If /OE, /CS and /WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If /CS goes low simultaneously with /WE going or after /WE going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When /CS is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

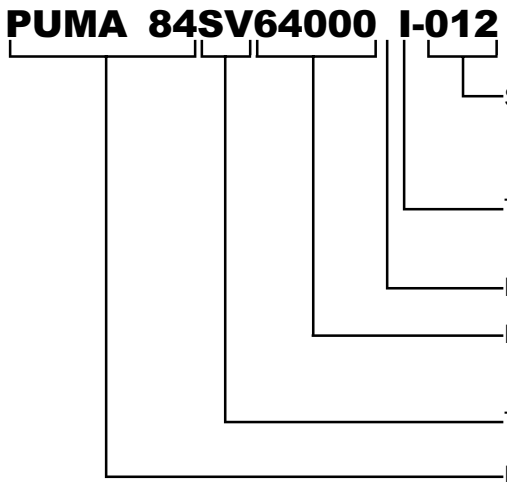
Note: /CS = /CS1~4, /WE = /WE1~4

PUMA 84 - Plastic 84 ëJí Leaded Package.





Ordering Information



Speed	012	=	12ns
	015	=	15ns
	020	=	20ns
Temp. Range/Screening	Blank	=	Commercial
	I	=	Industrial
Power Consumption	Blank	=	Standard
Memory Organisation	64000	=	2M x 32 configurable as 4M x 16 and 8M x 8
Technology	SV	=	SRAM 3.3V±10% V_{CC}
Package	PUMA 84	=	Plastic 84 ëJí Leaded Package.

Note :
Although this data is believed to be accurate the information contained herein is not intended to and does not create any warranty of merchantibility or fitness for a particular purpose.
Our products are subject to a constant process of development. Data may be changed without notice.
Products are not authorised for use as critical components in life support devices without the express written approval of a company director.