# TRAILING EDGE PRODUCT - MINIMUM ORDER APPLIES

Elm Road, West Chirton Industrial Estate, North Shields,
NE29 8SE, ENGLAND. TEL +44 191 2930519. FAX +44 191 2590997

# *64K x 16 SRAM MODULE*

## SYS1664FKE-70/85/10/12

Issue 1.1 : May 1996

## Description

The SYS1664FKE is a plastic 1Mbit Static RAM Module housed in a standard 40 pin Dual-In-Line package organised as 64K x 16 with access times of 70, 85,100, or 120 ns. The device has on-board decoding and supply decoupling capacitors.

The module is constructed using four 32Kx8 SRAMs in SOP packages mounted onto both sides of an FR4 epoxy substrate. This offers an extremely high PCB packing density.

The device is offered in standard and low power versions, with the -L module having a low voltage data retention mode for battery backed applications.

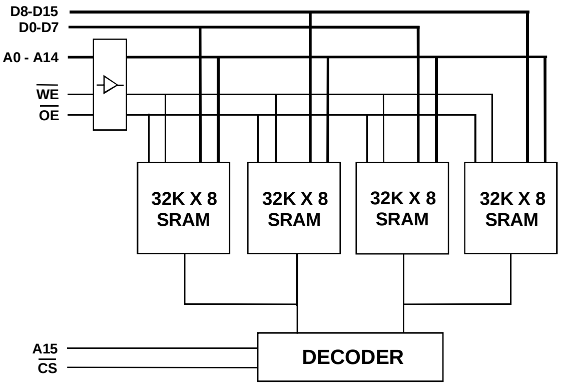
## Features

- Access Times of 70/85/100/120 ns.
- Low Power Disapation:

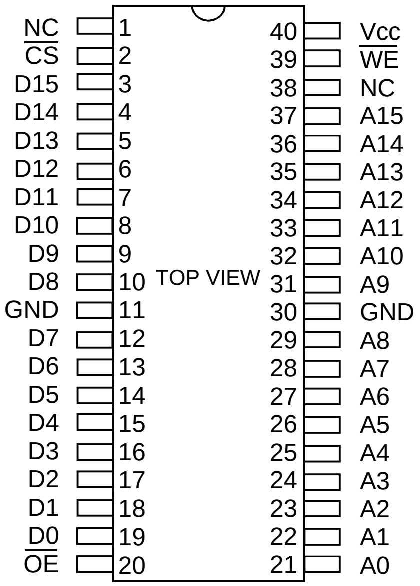
| | | |
|---|---|---|
| Operating | | 805 mW (Max) |
| Standby | -L version | 2.2 mW (Max) |

- Address & control inputs appear as a single load
- Completely Static Operation.
- Equal Access and Cycle Times.
- Low Voltage $V_{CC}$ Data Retention -L version.
- Directly TTL Compatible.
- 5 Volt Supply ± 10%.
- EPROM Compatible Pinout.
- Battery back-up capability.

## Block Diagram



## Pin Definition



## Pin Functions

| | |
|---|---|
| *Address Inputs* | **A0 - A15** |
| *Data Input/Output* | **D0 - D15** |
| *Chip Select* | **$\overline{CS}$** |
| *Write Enable* | **$\overline{WE}$** |
| *Output Enable* | **$\overline{OE}$** |
| *No Connect* | **NC** |
| *Power (+5V)* | **$V_{CC}$** |
| *Ground* | **GND** |

## Package Details

Plastic 40 Pin 0.6" DIP

## Absolute Maximum Ratings (1)

| | | | |
|---|---|---|---|
| Voltage on any pin relative to $V_{SS}$ | $V_T$ | -0.5V to +7.0 | V |
| Power Dissipation | $P_T$ | 2.0 | W |
| Storage Temperature | $T_{STG}$ | -55 to +125 | °C |

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of The device at those or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) Pulse Width: -3.0V for less than 50ns

## Recommended Operating Conditions

| *Parameter* | *Symbol* | *min* | *typ* | *max* | *Unit* |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| Input High Voltage | $V_{IH}$ | 2.2 | - | $V_{CC}$+0.3 | V |
| Input Low Voltage | $V_{IL}$ | -0.3 | - | 0.8 | V |
| Operating Temperature | $T_A$ | 0 | - | 70 | °C |
| | $T_{AI}$ | -40 | - | 85 | °C (1664I) |

## DC Electrical Characteristics ($T_A$=-40 to +85℃,$V_{CC}$=5V±10%,)

| *Parameter* | *Symbol* | *Test Condition* | *min* | *typ* | *max* | *Unit* |
|---|---|---|---|---|---|---|
| Input Leakage Current | $I_{IL}$ | $V_{IN}$=0V to $V_{CC}$ | -2 | - | 2 | µA |
| Output Leakage Current | $I_{OL}$ | $V_{I/O}$=Gnd to $V_{cc}$ | -1 | - | 1 | µA |
| Average Supply Current | $I_{CC1}$ | Min. Cycle,duty=100%,$I_{I/O}$=0mA | - | - | 146 | mA |
| Standby Supply Current | $I_{SB1}$ | $\overline{CS}\geq V_{CC}$-0.2V, $V_{IN}\geq$0V | - | - | 12 | mA |
| (-L part) | $I_{SB2}$ | $\overline{CS}\geq V_{CC}$-0.2V, $V_{IN}\geq$0V | - | - | 400 | µA |
| Output LowVoltage | $V_{OL}$ | $I_{OL}$=2.1mA | - | - | 0.40 | V |
| Output HighVoltage | $V_{OH}$ | $I_{OH}$=-400µA | 2.4 | - | - | V |

## Capacitance ($V_{CC}$=5V±10%,$T_A$=25°C)

| *Parameter* | *Symbol* | *Test Condition* | *typ* | *max* | *Unit* |
|---|---|---|---|---|---|
| Input Capacitance: | $C_{IN}$ | $V_{IN}$ = 0V | - | 10 | pF |
| I/O Capacitance: | $C_{I/O}$ | $V_{I/O}$= 0V | - | 10 | pF |

Note: This parameter is calculated not measured.

## AC Test Conditions

* Input pulse levels: 0V to 3.0V
* Input rise and fall times: 5ns
* Input and Output timing reference levels: 1.5V
* Output load: 1 TTL gate + 100pF
* $V_{CC}$=5V±10%

## OperationTruth Table

| $\overline{\text{CS}}$ | $\overline{\text{OE}}$ | $\overline{\text{WE}}$ | Mode | Outputs | Supply Current |
|---|---|---|---|---|---|
| H | X | X | Standby | High Z (D0-D15) | $I_{SB1}$, $I_{SB2}$ |
| L | L | H | Read | Dout (0-15) | Icc |
| L | X | L | Write | Din (0-15) | Icc |
| L | H | H | Output Disable | High Z (D0-D15) | Icc |

Notes : H = $V_{IH}$ : L = $V_{IL}$ : X = $V_{IH}$ or $V_{IL}$

## Low $V_{CC}$ Data Retention Characteristics - L Version Only

| *Parameter* | *Symbol* | *Test Condition* | *min* | *typ* | *max* | *Unit* |
|---|---|---|---|---|---|---|
| $V_{CC}$ for Data Retention | $V_{DR}$ | $\overline{CS} \geq V_{CC}$-0.2V | 2.0 | - | - | V |
| Data Retention Current | $I_{CCDR1}$ | $V_{CC}$=3.0V,$\overline{CS} \geq$2.8V,$T_{OP}=T_A$ | - | 280 | 380 | µA |
| | $I_{CCDR2}$ | $V_{CC}$=3.0V,$\overline{CS} \geq$2.8V,$T_{OP}=T_{AI}$ | - | - | 460 | µA |
| Chip Deselect to Data Retention Time | $t_{CDR}$ | See Retention Waveform | 0 | - | - | ns |
| Operation Recovery Time | $t_R$ | See Retention Waveform | $t_{RC}$(1) | - | - | ns |

Notes: (1) $t_{RC}$=Read Cycle Time

# AC OPERATING CONDITIONS

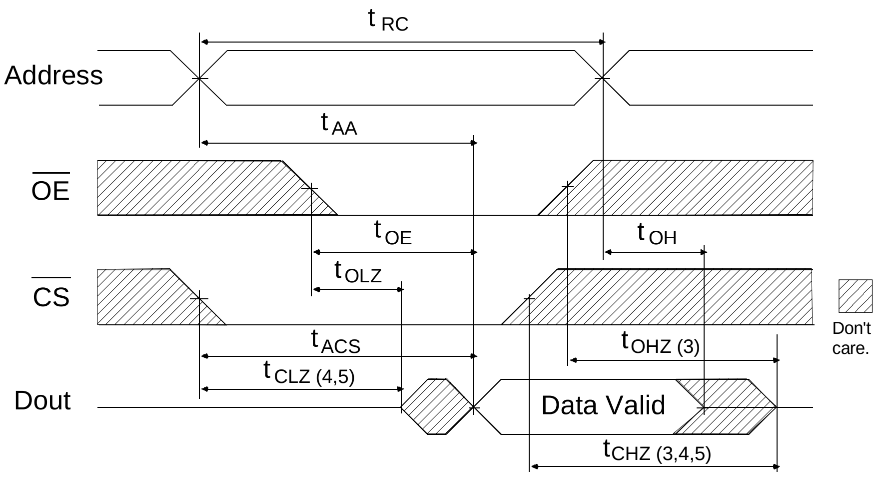
## Read Cycle

| | | *-70* | | *-85* | | *-10* | | *-12* | | |
|---|---|---|---|---|---|---|---|---|---|---|
| *Parameter* | *Symbol* | *min* | *max* | *min* | *max* | *min* | *max* | *min* | *max* | *Unit* |
| Read Cycle Time | $t_{RC}$ | 70 | - | 85 | - | 100 | - | 120 | - | ns |
| Address Access Time | $t_{AA}$ | - | 70 | - | 85 | - | 100 | - | 120 | ns |
| Chip Select Access Time | $t_{ACS}$ | - | 70 | - | 85 | - | 100 | - | 120 | ns |
| Output Enable to Output Valid | $t_{OE}$ | - | 40 | - | 45 | - | 50 | - | 60 | ns |
| Output Hold from Address Change | $t_{OH}$ | 5 | - | 5 | - | 10 | - | 10 | - | ns |
| Chip Selection to Output in Low Z | $t_{CLZ}$ | 5 | - | 5 | - | 10 | - | 10 | - | ns |
| Output Enable to Output in Low Z | $t_{OLZ}$ | 5 | - | 5 | - | 5 | - | 5 | - | ns |
| Chip Deselection to Output in High Z | $t_{CHZ}$ | 0 | 30 | 0 | 30 | 0 | 40 | 0 | 50 | ns |
| Output Disable to Output in High Z | $t_{OHZ}$ | 0 | 30 | 0 | 30 | 0 | 40 | 0 | 40 | ns |

## Write Cycle

| | | *-70* | | *-85* | | *-10* | | *-12* | | |
|---|---|---|---|---|---|---|---|---|---|---|
| *Parameter* | *Symbol* | *min* | *max* | *min* | *max* | *min* | *max* | *min* | *max* | *Unit* |
| Write Cycle Time | $t_{WC}$ | 70 | - | 85 | - | 100 | - | 120 | - | ns |
| Chip Selection to End of Write | $t_{CW}$ | 65 | - | 75 | - | 80 | - | 100 | - | ns |
| Address Valid to End of Write | $t_{AW}$ | 65 | - | 75 | - | 80 | - | 100 | - | ns |
| Address Setup Time | $t_{AS}$ | 0 | - | 0 | - | 0 | - | 0 | - | ns |
| Write Pulse Width | $t_{WP}$ | 55 | - | 65 | - | 70 | - | 80 | - | ns |
| Write Recovery Time | $t_{WR}$ | 5 | - | 5 | - | 5 | - | 5 | - | ns |
| Write to Output in High Z | $t_{WHZ}$ | 0 | 25 | 0 | 30 | 0 | 40 | 0 | 50 | ns |
| Data to Write Time Overlap | $t_{DW}$ | 30 | - | 40 | - | 40 | - | 50 | - | ns |
| Data Hold from Write Time | $t_{DH}$ | 0 | - | 0 | - | 0 | - | 0 | - | ns |
| Output Disable to Output in High Z | $t_{OHZ}$ | 0 | 30 | 0 | 30 | 0 | 40 | 0 | 40 | ns |
| Output Active from End of Write | $t_{OW}$ | 5 | - | 5 | - | 5 | - | 5 | - | ns |

## Read Cycle Timing Waveform (1,2)



## AC Read Characteristics Notes

(1) $\overline{WE}$ is High for Read Cycle.

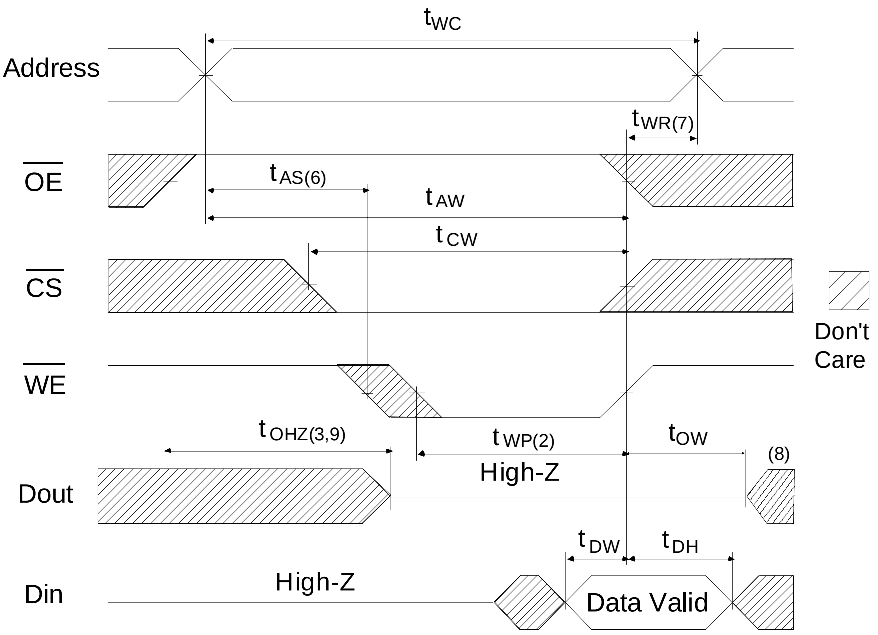
(2) All read cycle timing is referenced from the last valid address to the first transition address.

(3) $t_{CHZ}$ and $t_{OHZ}$ are defined as the time at which the outputs achieve open circuit conditions and are not referenced to output voltage levels.

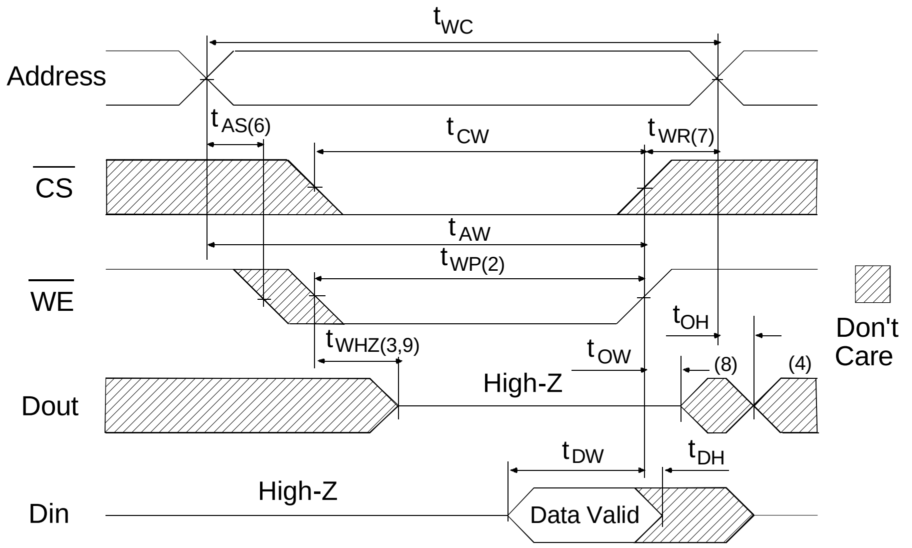
(4) At any given temperature and voltage condition, $t_{CHZ}$ (max) is less than $t_{CLZ}$ (min) both for a given module and from module to module.

(5) These parameters are sampled and not 100% tested.

## Write Cycle No.1 Timing Waveform (1,4)



## Write Cycle No.2 Timing Waveform (1,5)



### AC Write Characteristics Notes

(1) All write cycle timing is referenced from the last valid address to the first transition address.

(2) All writes occur during the overlap of $\overline{CS}$ and $\overline{WE}$ low.

(3) If $\overline{OE}$, $\overline{CS}$, and $\overline{WE}$ are in the Read mode during this period, the I/O pins are low impedance state. Inputs of opposite phase to the output must not be applied because bus contention can occur.

(4) Dout is the Read data of the new address.

(5) $\overline{OE}$ is continuously low.

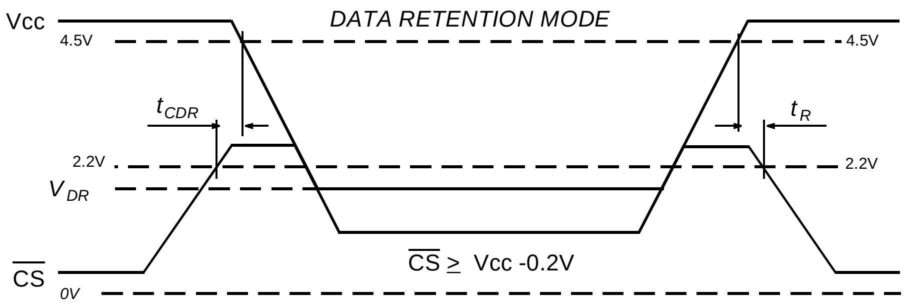
(6) Address is valid prior to or coincident with $\overline{CS}$ and $\overline{WE}$ low, too avoid inadvertant writes.

(7) $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.

(8) When $\overline{CS}$ is low : I/O pins are in the output state. Input signals of opposite phase leading to the output should not be applied.

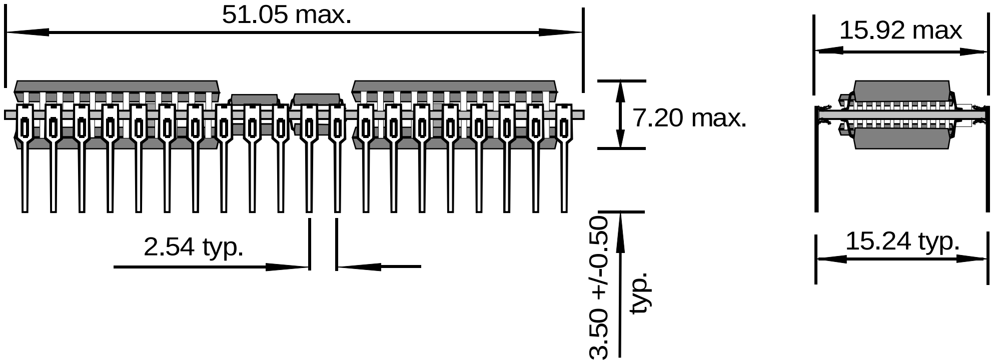
(9) Defined as the time at which the outputs achieve open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.

## Data Retention Waveform



## **Package Details.** Dimensions in mm

### 40 Pin 0.6" Dual-In-Line Package.



## Ordering Information

**SYS1664FKELI-10**

| | | |
|---|---|---|
| Speed | 70<br>85<br>10<br>12 | = 70 ns<br>= 85 ns<br>= 100 ns<br>= 120 ns |
| Temperature range | Blank<br>I | = Commercial Temp.<br>= Industrial Temp. |
| Power Consumption | Blank<br>L | = Standard Part<br>= Low Power Part |
| Package | FKE | = Plastic 40 Pin 0.6" DIP |
| Organisation | 1664 | = 64K x 16 |
| Memory Type | SYS | = Static RAM |