TRAILING EDGE PRODUCT - MINIMUM ORDER APPLIES

64K x 16 SRAM MODULE

SYS1664FK-70/85/10/12

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Description

The SYS1664FK is a plastic 1M Static RAM Module housed in a standard 40 pin Dual-In-Line package organised as 64K x 16 with access times of 70, 85,100, or 120 ns. The device has on-board decoding and capacitors.

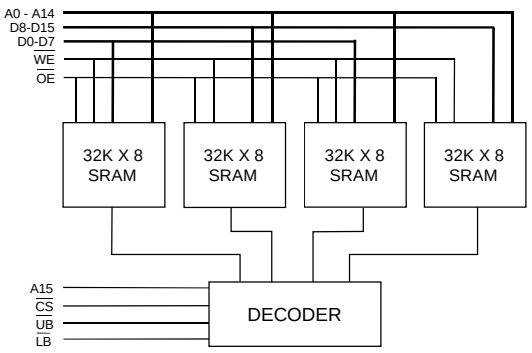
The module is constructed using four 32Kx8 SRAMs in SOP packages mounted onto both sides of an FR4 epoxy substrate. This offers an extremely high PCB packing density.

The device is offered in standard and low power versions, with the -L module having a low voltage data retention mode for battery backed applications.

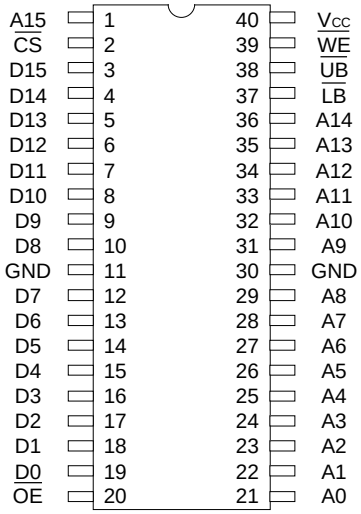
Features

- Access Times of 70/85/100/120 ns.
- Low Power Disapation:
  Operating (16 bit mode) 1.6 W (Max)
  Standby -L CMOS 1.38 mW (Max)
- Upper and Lower Byte Select Control
- Completely Static Operation.
- Equal Access and Cycle Times.
- Low Voltage V_{CC} Data Retention -L version.
- Directly TTL Compatible.
- 5 Volt Supply ± 10%.
- JEDEC approved 40 Pin Dual-In-Line package.

Block Diagram



Pin Definition



Pin Functions

Address Inputs	**A0 - A15**
Data Input/Output	**D0 - D15**
Chip Select	**$\overline{CS}$**
Write Enable	**$\overline{WE}$**
Output Enable	**$\overline{OE}$**
Upper Byte Select	**$\overline{UB}$**
Lower Byte Select	**$\overline{LB}$**
Power (+5V)	**V_{cc}**
Ground	**GND**

Package Details

Plastic 40 Pin 0.6" DIL

Absolute Maximum Ratings (1)

Voltage on any pin relative to V_{SS}	V_T	-0.5V to +7	V
Power Dissipation	P_T	1.6	W
Storage Temperature	T_{STG}	-55 to +150	˚C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of The device at those or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) Pulse Width:-1.0V for 50ns

Recommended Operating Conditions

Parameter	*Symbol*	*min*	*typ*	*max*	*Unit*
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	-	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	-0.3	-	0.8	V
Operating Temperature	T_A	0	-	70	˚C
	T_{AI}	-40	-	85	˚C (1664I)

DC Electrical Characteristics (T_A=-40 to +85℃,V_{CC}=5V±10%,)

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
Input Leakage Current	I_{IL}	V_{IN}=0V to V_{CC}	-	-	±8	µA
Output Leakage Current	I_{OL}	$V_{I/O}$=Gnd to V_{cc}	-	-	±8	µA
Average Supply Current(1)	I_{CC1}	Min. Cycle,duty=100%,$I_{I/O}$=0mA	-	-	70	mA
(16 bit)	I_{CC2}	Min. Cycle,duty=100%,$I_{I/O}$=0mA	-	-	140	mA
Standby Supply Current	I_{SB1}	$\overline{CS}$≥V_{CC}-0.2V, V_{IN}≥0V	-	-	8	mA
(-L part)	I_{SB2}	$\overline{CS}$≥V_{CC}-0.2V, V_{IN}≥0V	-	-	250	µA
Input Low Voltage(2)	V_{IL}		-0.3	-	0.8	V
Input High Voltage(3)	V_{IH}		2.2	-	V_{CC}+0.3	V
Output LowVoltage	V_{OL}	I_{OL}=2.1mA	-	-	0.45	V
Output HighVoltage	V_{OH}	I_{OH}=-400µA	2.4	-	-	V

Notes (1) For these currents min and max values are given for 8 and 16 bit mode operation respectively. Each individual value shown is a maximum.

(2) -1.0V for pulse width - 50 ns

(3) V_{CC}+1.5V for -20 ns. If V_{IH} is over the specified max. value, READ operation cannot be guaranteed.

Capacitance (V_{CC}=5V±10%,T_A=25°C)

Parameter	*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance:	C_{IN}	V_{IN} = 0V	-	40	pF
I/O Capacitance:	$C_{I/O}$	$V_{I/O}$= 0V	-	40	pF

Note: This parameter is calculated not measured.

AC Test Conditions

* Input pulse levels: 0V to 3.0V
* Input rise and fall times: 5ns
* Input and Output timing reference levels: 1.5V
* Output load: 1 TTL gate + 100pF
* V_{CC}=5V±10%

OperationTruth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	Mode	Outputs	Supply Current
H	X	X	X	X	Standby	High Z (D0-D15)	Isb1, Isb2
L	X	X	H	H	Standby	HighZ (D0-D15)	Isb1, Isb2
L	L	H	H	L	Read 8bit	Dout (8-15)	Icc1
L	L	H	L	H	Read 8bit	Dout (0-7)	Icc1
L	L	H	L	L	Read 16bit	Dout (0-15)	Icc2
L	X	L	H	L	Write 8bit	Din (8-15)	Icc1
L	X	L	L	H	Write 8bit	Din(0-7)	Icc1
L	X	L	L	L	Write 16bit	Din (0-15)	Icc2
L	H	H	L	L	Output Disable	High Z (D0-D15)	Icc2
L	H	H	H	L	Output Disable	High Z (D0-D15)	Icc2
L	H	H	L	H	Output Disable	High Z (D0-D15)	Icc2

Notes : H = V_{IH} : L = V_{IL} : X = V_{IH} or V_{IL}

Low V_{CC} Data Retention Characteristics - L Version Only

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
V_{CC} for Data Retention	V_{DR}	$\overline{CS}\geq V_{CC}$-0.2V	2.0	-	-	V
Data Retention Current	I_{CCDR1}	V_{CC}=3.0V,$\overline{CS}\geq$2.8V,$T_{OP}=T_A$	-	280	380	µA
	I_{CCDR2}	V_{CC}=3.0V,$\overline{CS}\geq$2.8V,$T_{OP}=T_{AI}$	-	-	460	µA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R	See Retention Waveform	t_{RC} (1)	-	-	ns

Notes: (1) t_{RC}=Read Cycle Time

AC OPERATING CONDITIONS

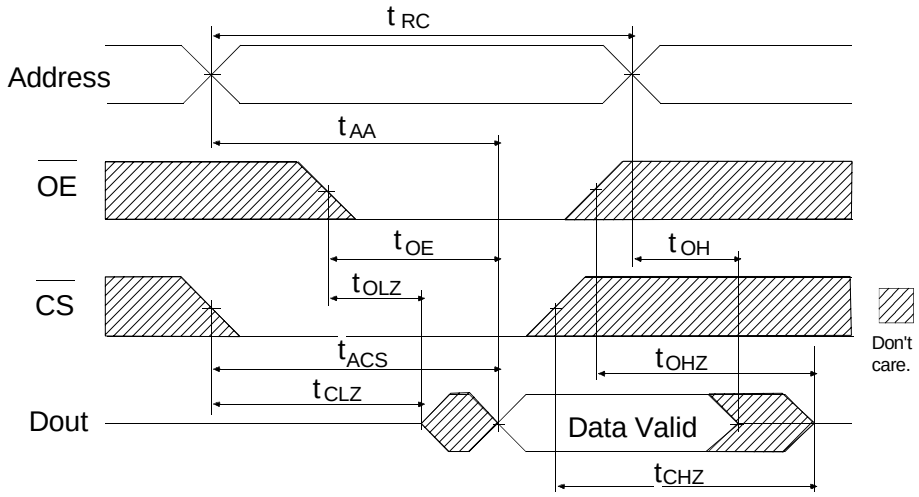
Read Cycle

		-70		-85		-10		-12		
Parameter	*Symbol*	*min*	*max*	*min*	*max*	*min*	*max*	*min*	*max*	*Unit*
Read Cycle Time	t_{RC}	70	-	85	-	100	-	120	-	ns
Address Access Time	t_{AA}	-	70	-	85	-	100	-	120	ns
Chip Select Access Time	t_{ACS}	-	70	-	85	-	100	-	120	ns
Output Enable to Output Valid	t_{OE}	-	35	-	45	-	50	-	60	ns
Output Hold from Address Change	t_{OH}	10	-	10	-	10	-	10	-	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	-	10	-	10	-	10	-	ns
Output Enable to Output in Low Z	t_{OLZ}	5	-	5	-	5	-	5	-	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	30	0	30	0	35	0	40	ns
Output Disable to Output in High Z	t_{OHZ}	0	30	0	30	0	35	0	40	ns

Write Cycle

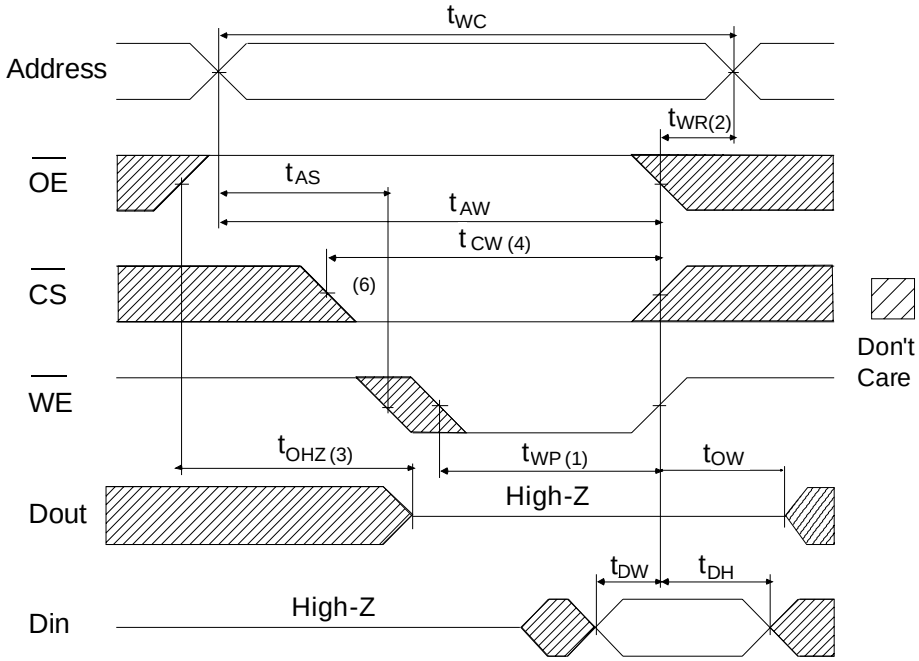
		-70		-85		-10		-12		
Parameter	*Symbol*	*min*	*max*	*min*	*max*	*min*	*max*	*min*	*max*	*Unit*
Write Cycle Time	t_{WC}	70	-	85	-	100	-	120	-	ns
Chip Selection to End of Write	t_{CW}	65	-	70	-	80	-	85	-	ns
Address Valid to End of Write	t_{AW}	65	-	70	-	80	-	85	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	55	-	60	-	70	-	80	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	0	-	ns
Write to Output in High Z	t_{WHZ}	0	25	0	30	0	35	0	40	ns
Data to Write Time Overlap	t_{DW}	30	-	35	-	40	-	50	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	0	-	ns
Output Disable to Output in High Z	t_{OHZ}	0	30	0	30	0	35	0	40	ns
Output Active from End of Write	t_{OW}	10	-	10	-	10	-	10	-	ns

Read Cycle Timing Waveform (1,2))

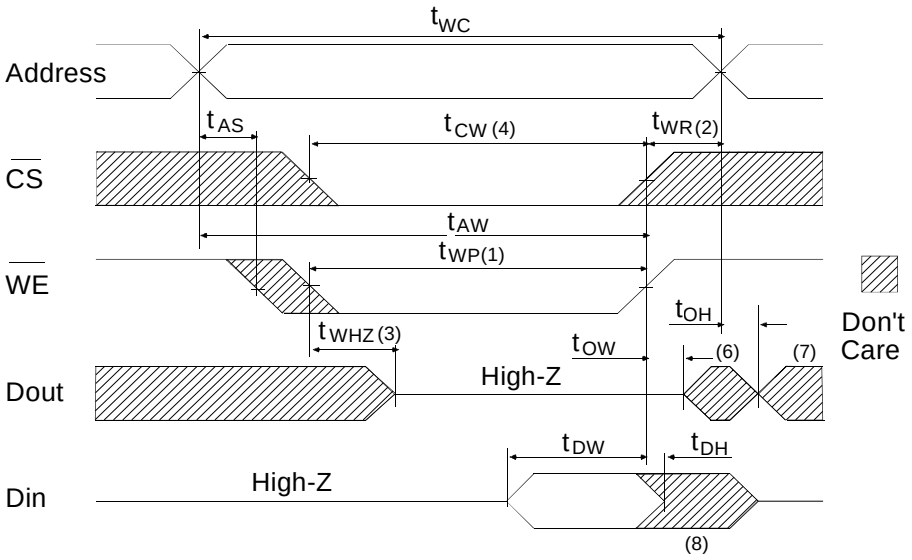


Notes:
1. $\overline{WE}$ is High for Read Cycle.
2. Address valid prior to or coincident with $\overline{CS}$ transition Low.

Write Cycle No.1 Timing Waveform



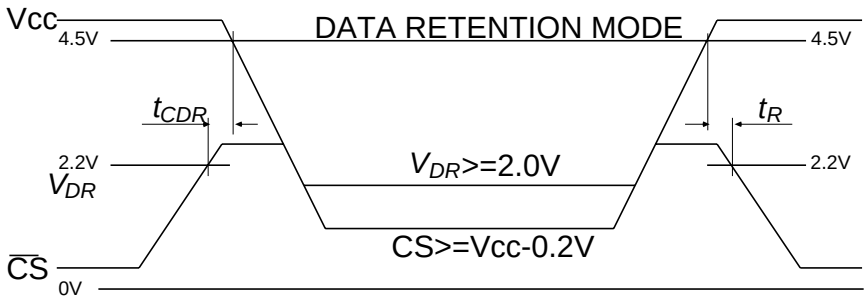
Write Cycle No.2 Timing Waveform (5)



Notes:

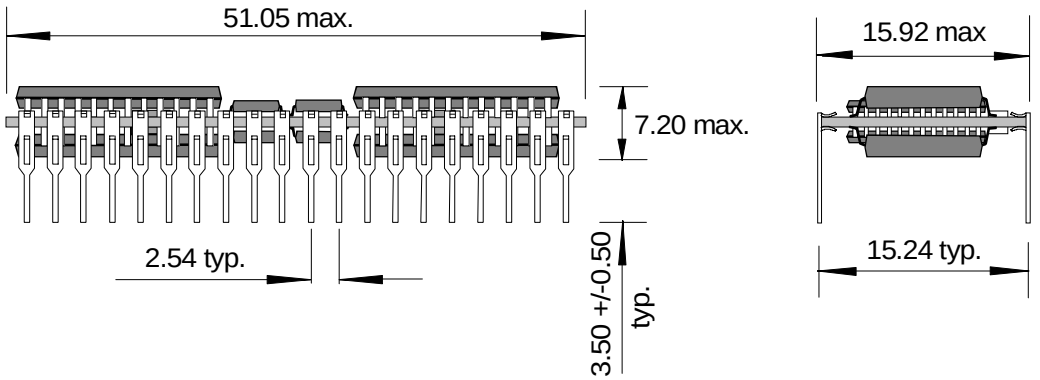
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state. Input signals out of phase must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.
5. $\overline{OE}$ is continuously low. ($\overline{OE}$=V_{IL})
6. Dout is in the same phase as written data of this write cycle.
7. Dout is the read data of next address.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Input signals out of phase must not be applied to I/O pins.

Data Retention Waveform



Package Details. Dimensions in mm(inches)

40 Pin 0.6" Dual-In-Line Package.



Ordering Information

SYS1664FKLI-10

Speed	70	= 70 ns
	85	= 85 ns
	10	= 100 ns
	12	= 120 ns
Temperature range	Blank	= Commercial Temp.
	I	= Industrial Temp.
Power Consumption	Blank	= Standard Part
	L	= Low Power Part
Package	FK	= Plastic 0.6" DIP
Organisation	1664	= 64K x 16
Memory Type	SYS	= Static RAM

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