

# TRAILING EDGE PRODUCT - MINIMUM ORDER APPLIES



## 1M x 8 SRAM SIL MODULE

### SYS81000RKXB - 85/10/12

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#### Description

The SYS81000RKXB is a plastic 8M Static RAM Module housed in a standard 36 pin Single In-Line package organised as 1M x 8. This offers an extremely high PCB packing density.

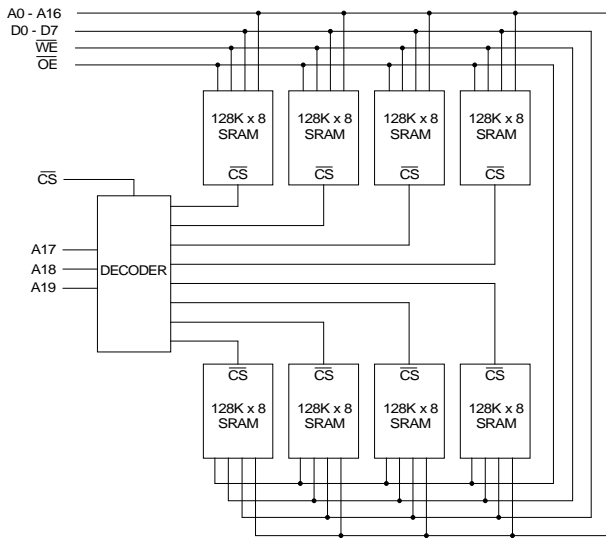
The module is constructed using eight 128Kx8 SRAMs in TSOP packages mounted onto both sides of an FR4 epoxy substrate. Access times are 85, 100 and 120ns.

The SYS81000RKXB is offered in standard and low power versions, with the -L module having a low voltage data retention mode for battery backed applications.

#### Features

- Access Times of 85/100/120ns.
- 36 Pin Industry Standard Single-In-Line package.
- 5 Volt Supply  $\pm 10\%$ .
- Low Power Dissipation 100/120ns :  
 Average (min cycle) 501 mW (max).  
 Standby (CMOS, -L) 4.4mW (max).
- Low Voltage  $V_{CC}$  Data Retention.
- Directly TTL Compatible.
- On-board Decoding & Capacitors.
- Upgradeable.

#### Block Diagram



#### Pin Definition

NC	1
$V_{CC}$	2
WE	3
D2	4
D3	5
D0	6
A1	7
A2	8
A3	9
A4	10
GND	11
D5	12
A10	13
A11	14
A5	15
A13	16
A14	17
A19	18
$\overline{CS}$	19
A15	20
A16	21
A12	22
A18	23
A6	24
D1	25
GND	26
A0	27
A7	28
A8	29
A9	30
D7	31
D4	32
D6	33
A17	34
$V_{CC}$	35
OE	36

#### Pin Functions

Address Inputs	A0 ~ A19
Data Input/Output	D0 ~ D7
Chip Select Input	$\overline{CS}$
Read/Write Input	WE
Output Enable Input	OE
No Connect	NC
Power (+5V)	$V_{CC}$
Ground	GND

## DC OPERATING CONDITIONS

### Absolute Maximum Ratings

Voltage on any pin relative to $V_{SS}$	$V_T$	-0.5V to +7.0	V
Power Dissipation	$P_T$	700	mW
Storage Temperature	$T_{STG}$	-55 to +125	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### Recommended Operating Conditions

		<i>min</i>	<i>typ</i>	<i>max</i>	
Supply Voltage	$V_{CC}$	4.5	5.0	5.5	V
Input High Voltage	$V_{IH}$	2.2	-	$V_{CC}+0.3$	V
Input Low Voltage	$V_{IL}$	-0.3	-	0.8	V
Operating Temperature	$T_A$	0	-	70	°C
	$T_{AI}$	-40	-	85	°C (I)

### DC Electrical Characteristics

( $V_{CC} = 5V \pm 10\%$ ,  $T_A = 0$  to  $70^\circ\text{C}$ )

Parameter	Sym	Test Condition	<i>min</i>	<i>typ</i> <sup>(1)</sup>	<i>max</i>	Unit
I/P Leakage Current	A0~A16, $\overline{OE}$ , $\overline{WE}$	$I_{LI1}$ 0V - $V_{IN}$ - $V_{CC}$	-8	-	8	$\mu\text{A}$
I/P Leakage Current	A17~A19, $\overline{CS}$	$I_{LI2}$ 0V - $V_{IN}$ - $V_{CC}$	-1	-	1	$\mu\text{A}$
Output Leakage Current	D0~D7	$I_{LO}$ $\overline{CS} = V_{IH}$ , $V_{IO} = \text{GND to } V_{CC}$	-8	-	8	$\mu\text{A}$
Average Supply Current		$I_{CC}$ $\overline{CS} = V_{IL}$ , $V_{IN} = V_{IL}/V_{CC}-2.1V$	-	52	91	mA
Standby Supply Current	TTL levels	$I_{SB}$ $\overline{CS} = V_{IH}$ , A17~A19 = $V_{IH}$ or $V_{IL}$	-	8	24	mA
	-L, CMOS levels	$I_{SB1}$ $\overline{CS} = V_{CC}-0.2V$ , A17~A19 = $V_{CC}-0.2V$ or $0.2V$	-	-	0.8	mA
Output Low Voltage		$V_{OL}$ $I_{OL} = 2.1\text{mA}$	-	-	0.4	V
Output High Voltage		$V_{OH}$ $I_{OH} = -1.0\text{mA}$	2.4	-	-	V

(1) Typical values are at  $V_{CC} = 5.0V$ ,  $T_A = 25^\circ\text{C}$  and specified loading.

### Capacitance

( $V_{CC} = 5V \pm 10\%$ ,  $T_A = 25^\circ\text{C}$ )

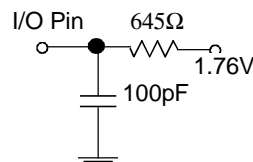
Parameter	Symbol	Test Condition	<i>typ</i>	<i>max</i>	Unit
Input Capacitance ( $\overline{CS}$ , A17~A19)	$C_{IN1}$	$V_{IN} = 0V$	-	10	pF
Input Capacitance (other)	$C_{IN2}$	$V_{IN} = 0V$	-	64	pF
I/O Capacitance	$C_{IO}$	$V_{IO} = 0V$	-	80	pF

Capacitance calculated, not measured

### AC Test Conditions

- \* Input pulse levels:  $V_{SS}$  to 3.0V
- \* Input rise and fall times: 5ns
- \* Input and Output timing reference levels: 1.5V
- \* Output load: see diagram
- \*  $V_{CC} = 5V \pm 10\%$

### Output Load



### AC OPERATING CONDITIONS

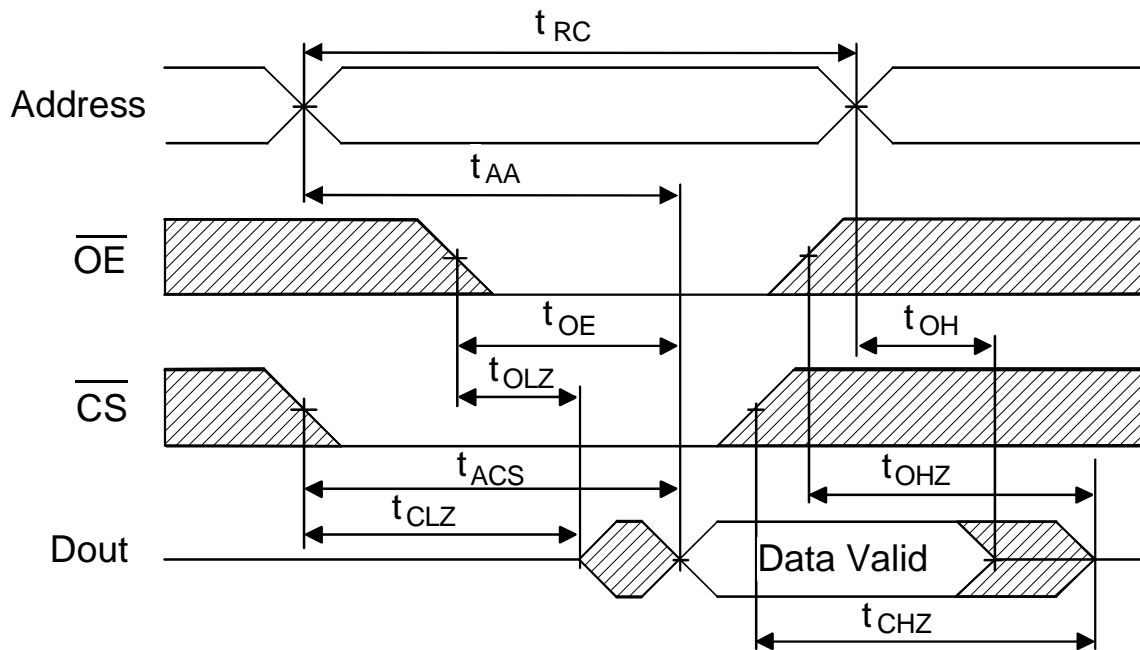
#### Read Cycle <sup>(1,2)</sup>

Parameter	Symbol	-85		-10		-12		Unit
		min	max	min	max	min	max	
Read Cycle Time	$t_{RC}$	85	-	100	-	120	-	ns
Address Access Time	$t_{AA}$	-	85	-	100	-	120	ns
Chip Select Access Time	$t_{ACS}$	-	85	-	100	-	120	ns
Output Enable to Output Valid	$t_{OE}$	-	45	-	50	-	60	ns
Output Hold from Address Change	$t_{OH}$	10	-	10	-	10	-	ns
Chip Selection to Output in Low Z <sup>(2)</sup>	$t_{CLZ}$	10	-	10	-	10	-	ns
Output Enable to Output in Low Z <sup>(2)</sup>	$t_{OLZ}$	5	-	5	-	5	-	ns
Chip Deselection to O/P in High Z <sup>(2)</sup>	$t_{CHZ}$	0	30	0	35	0	40	ns
Output Disable to Output in High Z <sup>(2)</sup>	$t_{OHZ}$	0	30	0	35	0	40	ns

Notes (1)  $\overline{WE}$  is High for Read Cycle.

(2)  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.

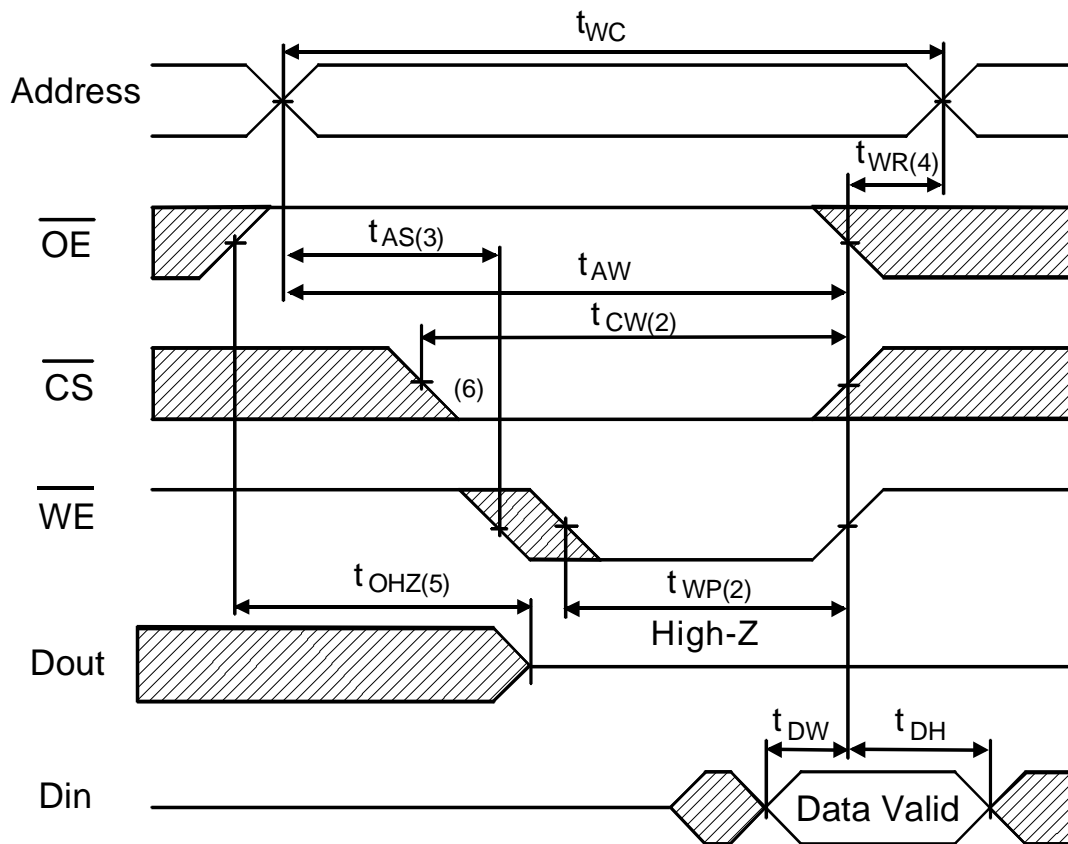
#### Read Cycle Timing Waveform <sup>(1,2)</sup>



**Write Cycle**

Parameter	Symbol	-85		-10		-12		Unit
		min	max	min	max	min	max	
Write Cycle Time	$t_{WC}$	85	-	100	-	120	-	ns
Chip Selection to End of Write	$t_{CW}$	75	-	85	-	100	-	ns
Address Valid to End of Write	$t_{AW}$	75	-	85	-	100	-	ns
Address Setup Time	$t_{AS}$	0	-	0	-	0	-	ns
Write Pulse Width	$t_{WP}$	65	-	75	-	85	-	ns
Write Recovery Time	$t_{WR}$	0	-	0	-	0	-	ns
Write to Output in High Z <sup>(11)</sup>	$t_{WHZ}$	0	30	0	35	0	40	ns
Data to Write Time Overlap	$t_{DW}$	35	-	40	-	45	-	ns
Data Hold from Write Time	$t_{DH}$	0	-	0	-	0	-	ns
Output active from end of write <sup>(10)</sup>	$t_{OW}$	5	-	5	-	5	-	ns

**Write Cycle No.1 Timing Waveform**



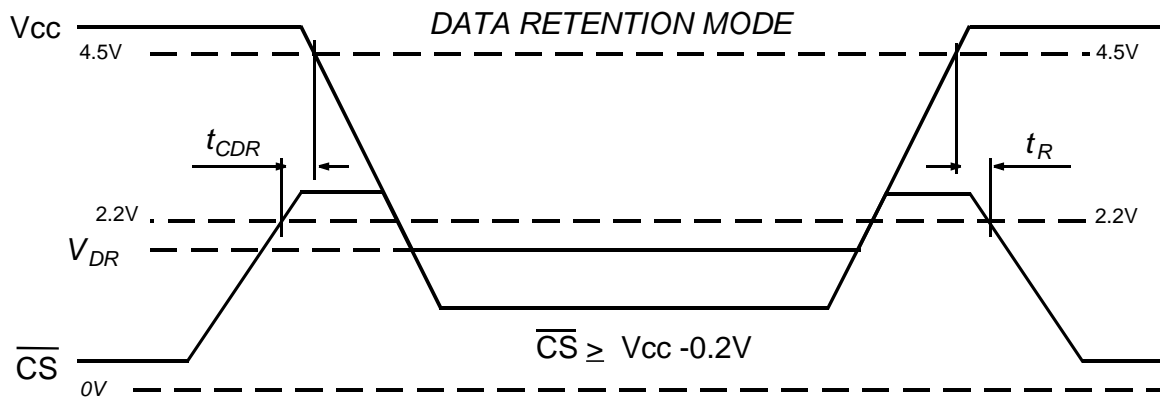


**Low  $V_{cc}$  Data Retention Characteristics - L Version Only ( $T_A = 0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ )**

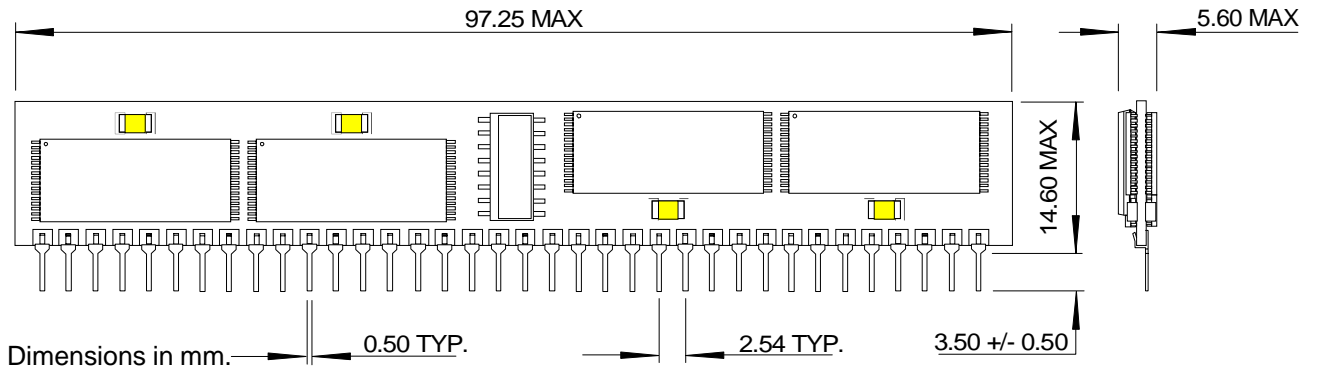
Parameter	Sym	Test Condition	min	-L Part typ <sup>(1)</sup>	max	Unit
$V_{cc}$ for Data Retention	$V_{DR}$	$\overline{CS} = V_{cc} - 0.2V$	2.0	-	-	V
Data Retention Current		$V_{cc} = 3.0V,$ $I_{CCDR1}^{(2)}$ $\overline{CS} = V_{cc} - 0.2V, A17-A19 = V_{cc} - 0.2V$ or $0.2V$	-	-	400	mA
Data Retention Time	$t_{CDR}$	See Retention Waveform	0	-	-	ns
Operation Recovery Time	$t_R$	See Retention Waveform	5	-	-	ms

Notes (1) Typical figures are measured at 25°C.  
 (2) This parameter is guaranteed not tested.

**Data Retention Waveform**

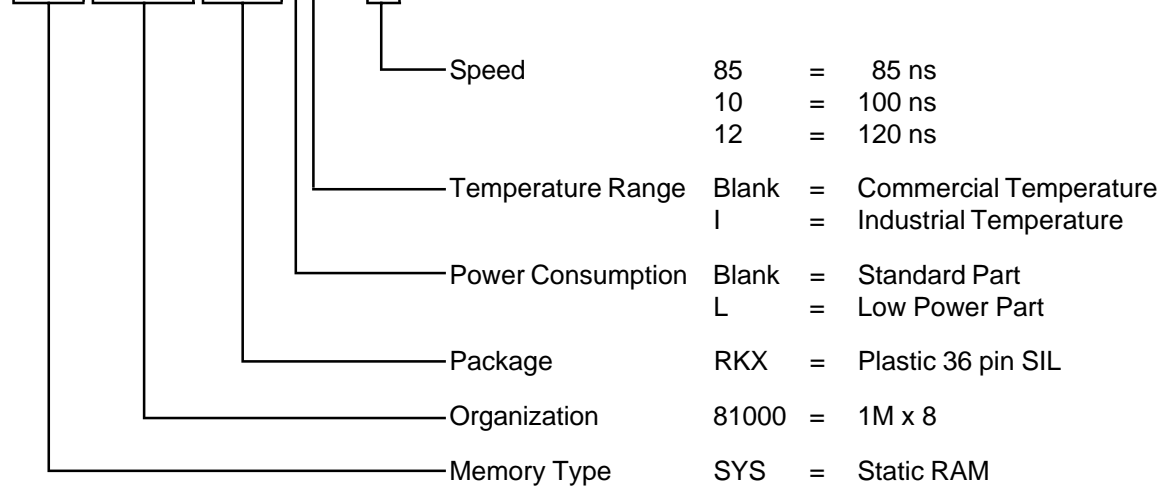


**Package Information**



**Ordering Information**

**SYS81000RKXLI - 10**



**Note :**

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