TRAILING EDGE PRODUCT - MINIMUM ORDER APPLIES

1M x 16 SRAM MODULE

MS161000FKXA-10/12/15

Issue 1.0 : January 1992

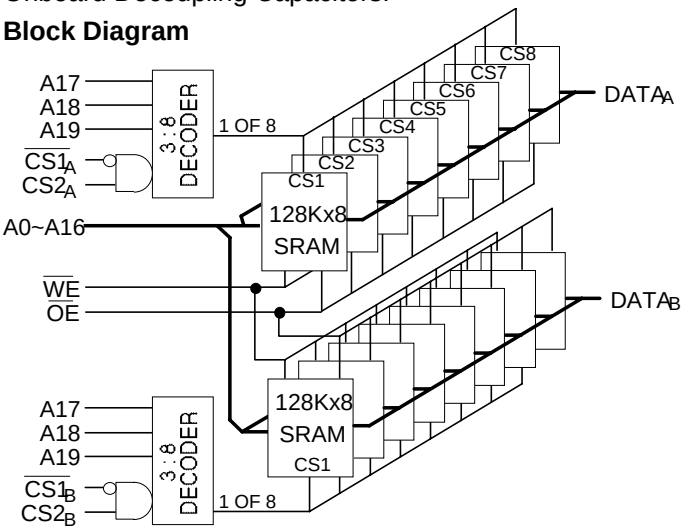
PRELIMINARY

1,048,576 x 16 CMOS High Speed Static RAM

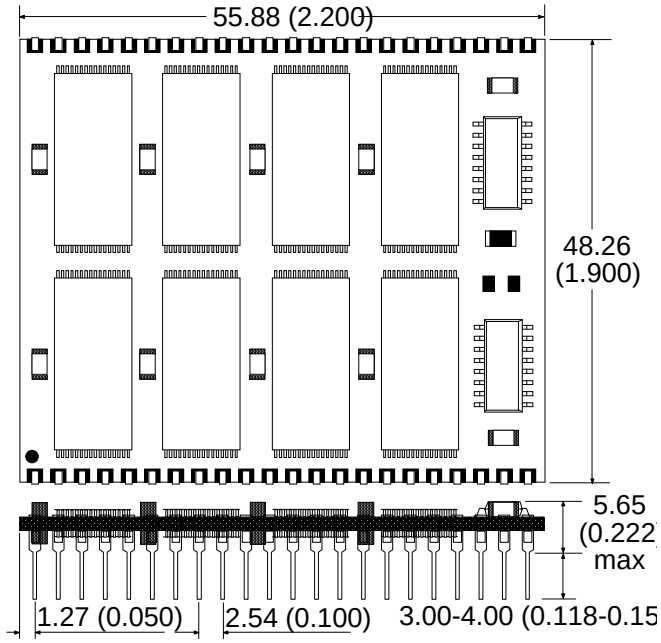
Features

Access Times of 100/120/150 ns.
Configurable as 8 / 16 bit wide outputs.
Operating Power 550 / 600 mW (typical).
Low Power Standby 1.68 mW (typical) -L version.
Completely Static Operation.
Battery back-up capability.
Directly TTL compatible.
Onboard Decoupling Capacitors.

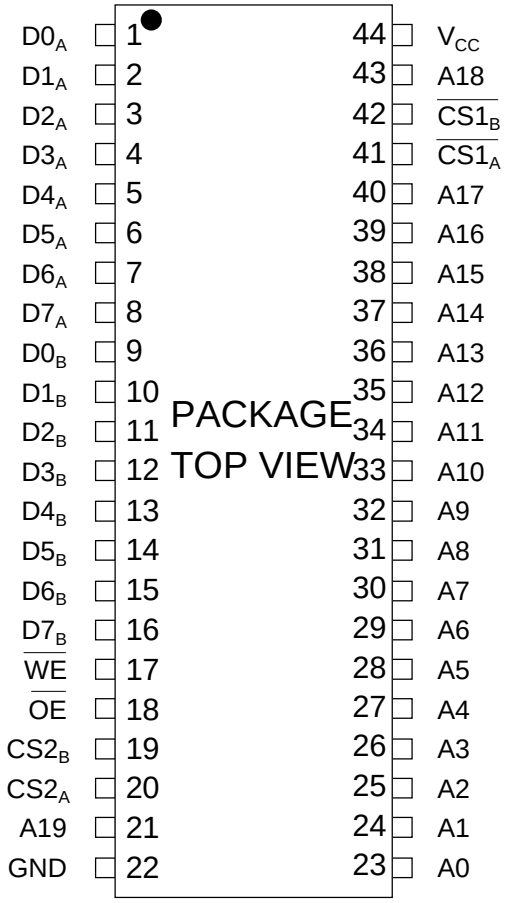
Block Diagram



Package Details Dimensions in mm (inches).



Pin Definition



Pin Functions

A0 ~A19	Address Inputs
$D0_A$ ~$D7_A$	Data A Input/Output
$D0_B$ ~$D7_B$	Data B Input/Output
$\overline{CS1}_A$	Chip Select Data A (active low)
$\overline{CS1}_B$	Chip Select Data B (active low)
$CS2_A$	Chip Select Data A (active high)
$CS2_B$	Chip Select Data B (active high)
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Power (+5V)
GND	Ground

Absolute Maximum Ratings

Voltage on any pin relative to V_{SS}	V_T	-0.5V to +7	V
Power Dissipation	P_T	16	W
Storage Temperature	T_{STG}	-55 to +125	˚C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) V_T can be -3.5V pulse of less than 20ns.

Recommended Operating Conditions

		min	*typ*	*max*	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	-	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	-0.3	-	0.8	V
Operating Temperature	T_A	0	-	70	˚C
	T_{AI}	-40	-	85	˚C (**-I** suffix)

DC Electrical Characteristics (V_{CC}=5V±10%,T_A=0˚C to +70˚C)

Parameter		*Symbol*	*Test Condition*	*min*	*typ*(1)	*max*	*Unit*
Input Leakage Current	$\overline{CS}$	I_{LI1}	V_{IN}=0V to V_{CC}	-	-	±1	µA
	A17~A19	I_{LI2}	V_{IN}=0V to V_{CC}	-	-	±2	µA
	A0~A16, $\overline{WE}$, $\overline{OE}$	I_{LI3}	V_{IN}=0V to V_{CC}	-	-	±32	µA
Output Leakage Current	16 bit	I_{LO}	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL}, $V_{I/O}$ = 0V to V_{CC}	-	-	±16	µA
Operating Supply Current	16 bit	I_{CC016}	$\overline{CS1}$ = V_{IL}, CS2 = V_{CC}-2.1, $I_{I/O}$ = 0mA, I/P's Static	-	52	107	mA
	8 bit	I_{CC08}	As above	-	37	60	mA
Average Supply Current	16 bit	I_{CCA16}	$\overline{CS1}$=V_{IL}, CS2=V_{CC}-2.1, V_{IL}•V_{IN}•V_{CC}-2.1, min.cycle	-	112	187	mA
	8 bit	I_{CCA8}	As above	-	67	92	mA
Standby Supply Current	TTL	I_{SB}	$\overline{CS1}$ = V_{CC}-2.1 or CS2 = V_{IL} , min. cycle	-	-	48	mA
	CMOS	I_{SB1}	$\overline{CS1}$•V_{CC}-0.2V or CS2-0.2V, 0.2V•V_{IN}•V_{CC}-0.2V	-	0.64	32	mA
-L part	CMOS	I_{SB2}	As above	-	0.40	2	mA
Output Voltage Low		V_{OL}	I_{OL}=2.1mA	-	-	0.4	V
Output Voltage High		V_{OH}	I_{OH}=-1.0mA	2.4	-	-	V

Notes (1) $\overline{CS1}$ and CS2 above are accessed through $\overline{CS1}_A$, $\overline{CS1}_B$, $CS2_A$ and $CS2_B$ as shown in the Operating Modes Truth Table on page 6 to obtain 8 and 16 bit operation.

(2) Typical values are measured at 25˚C and V_{CC} = 5.0V.

Capacitance (V_{CC} = 5V ± 10%,T_A = 25˚C, f = 1MHz) These parameters are calculated, not measured.

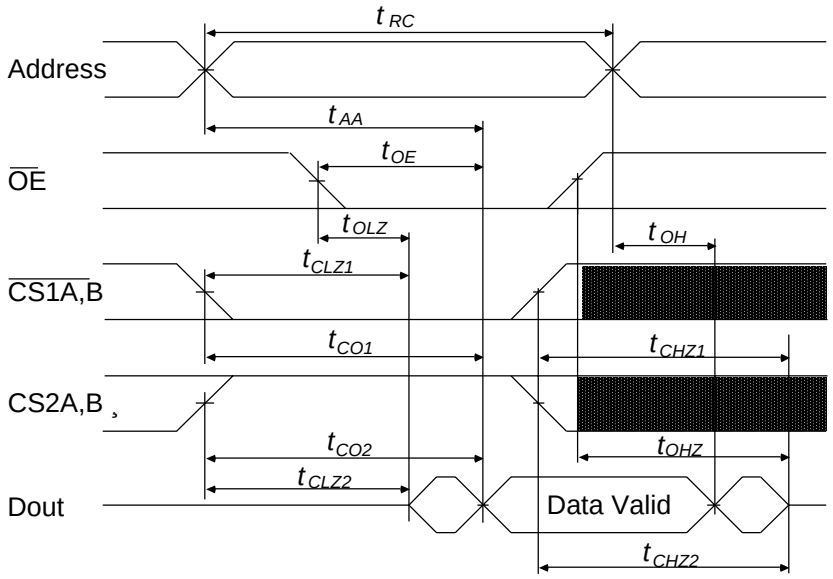
Parameter		*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance	Chip Selects	C_{IN1}	V_{IN}=0V	-	10	pF
	A17~A19	C_{IN2}	V_{IN}=0V	-	12	pF
	A0~A16, $\overline{WE}$, $\overline{OE}$	C_{IN3}	V_{IN}=0V	-	160	pF
Output Capacitance	16 bit	C_{OUT}	V_{OUT}=0V	-	80	pF

Recommended AC Operating Conditions

Read Cycle

Parameter	Symbol	-10 min	-10 max	-12 min	-12 max	-15 min	-15 max	Unit
Read Cycle Time	t_{RC}	100	-	120	-	150	-	ns
Address Access Time	t_{AA}	-	100	-	120	-	150	ns
Chip Select to Output ($CS1_{A,B}$)	t_{CO1}	-	100	-	120	-	150	ns
Chip Select to Output ($CS2_{A,B}$)	t_{CO2}	-	100	-	120	-	150	ns
Output Enable to Output Valid	t_{OE}	-	50	-	60	-	70	ns
Output Hold from Address Change	t_{OH}	10	-	10	-	10	-	ns
Chip Select to Output in Low Z ($CS1_{A,B}$)	t_{CLZ1}	10	-	10	-	10	-	ns
Chip Select to Output in Low Z ($CS2_{A,B}$)	t_{CLZ2}	10	-	10	-	10	-	ns
Output Enable to Output in Low Z	t_{OLZ}	5	-	5	-	5	-	ns
Chip Select to Output in High Z ($CS1_{A,B}$) (2)	t_{CHZ1}	0	35	0	45	0	50	ns
Chip Select to Output in High Z ($CS2_{A,B}$) (2)	t_{CHZ2}	0	35	0	45	0	50	ns
Output Enable to Output in High Z (2)	t_{OHZ}	0	35	0	45	0	50	ns

Read Cycle



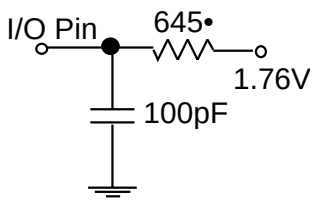
Notes: (1) $\overline{WE}$ is High for Read Cycle.

(2) t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. At any given temperature and voltage condition, t_{CHZ} max is less than t_{CLZ} min both for a given device and from device to device. This parameter is sampled and not 100% tested.

AC Test Conditions

* Input pulse levels: 0V to 3.0V.
* Input rise and fall times: 5ns.
* Input and Output timing reference levels: 1.5V.
* Output load: see diagram.
* Module is tested in 16 bit mode.

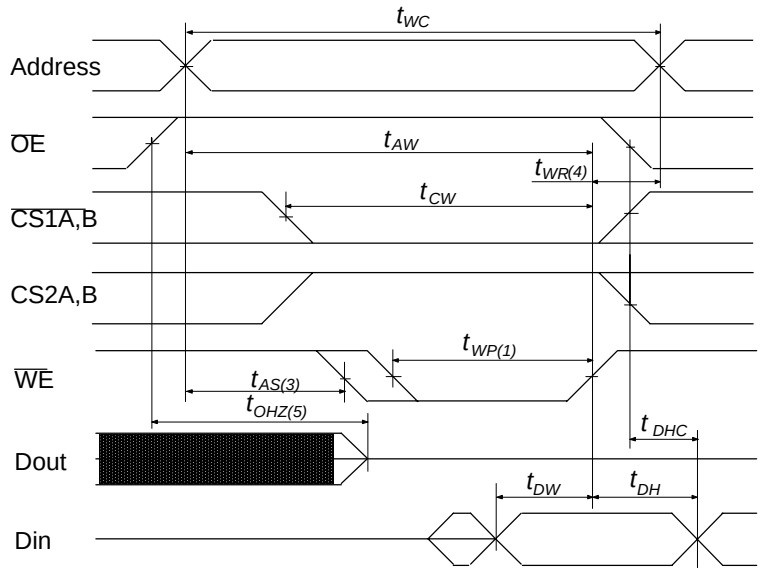
Output Load



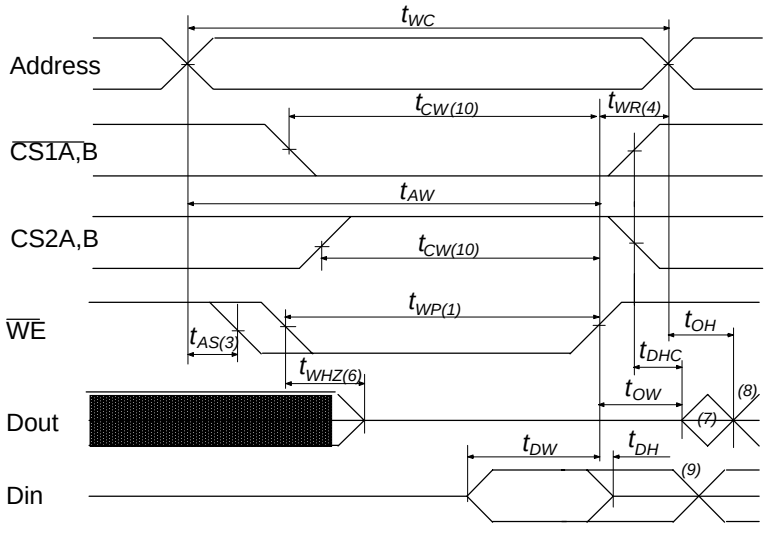
Write Cycle

Parameter	Symbol	-10 min	-10 max	-12 min	-12 max	-15 min	-15 max	Unit
Write Cycle Time	t_{WC}	100	-	120	-	150	-	ns
Chip Selection to End of Write	t_{CW}	90	-	100	-	120	-	ns
Address Valid to End of Write	t_{AW}	90	-	100	-	120	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	75	-	85	-	95	-	ns
Write Recovery Time	t_{WR}	10	-	15	-	20	-	ns
Write to Output in High Z (11)	t_{WHZ}	0	35	0	40	0	50	ns
Data to Write Time Overlap	t_{DW}	40	-	45	-	50	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns
Output Active from End of Write	t_{OW}	5	-	5	-	5	-	ns

Write Cycle No. 1 Timing Waveform



Write Cycle No. 2 Timing Waveform (5)



Write Cycle Timing Waveform Notes

(1) A write occurs during the overlap (t_{WP}) of $\overline{CS1_{A/B}}$ low, $CS2_{A/B}$ high and $\overline{WE}$ low.

(2) If a bank becomes selected ($\overline{CS1_{A/B}}$ low and $CS2_{A/B}$ high) simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low,the outputs remain in a high impedance state.

(3) If $\overline{CS1_{A/B}}$ or $CS2_{A/B}$ goes inactive simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

(4) t_{WR} is measured from the earlier of $\overline{CS1_{A/B}}$, $CS2_{A/B}$ and $\overline{WE}$ becoming inactive to the address change.

(5) $\overline{OE}$ is continuoulsy low. ($\overline{OE}$=V_{IL})

(6) During this period, I/O pins are in the output state. Input signals out of phase must not be applied.

(7) D_{OUT} is in the same phase as written data of this write cycle.

(8) D_{OUT} is the read data of next address.

(9) If $\overline{CS1_{A/B}}$ or $CS2_{A/B}$ go inactive during this period, I/O pins are in the output state, input signals out of phase must not be applied to I/O pins.

(10) t_{CW} is measured from the later of $\overline{CS1_{A/B}}$ and $CS2_{A/B}$ becoming active to end of write.

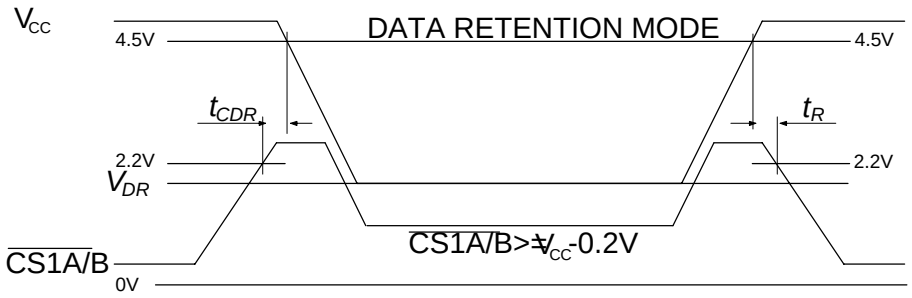
(11) t_{WHZ} is defined as the time at which the outputs achieve the open circuit condition and is not referenced to output voltage levels. This parameter is sampled and not 100% tested.

Low V_{cc} Data Retention Characteristics - L Version Only (T_A=-0℃ to +70℃)

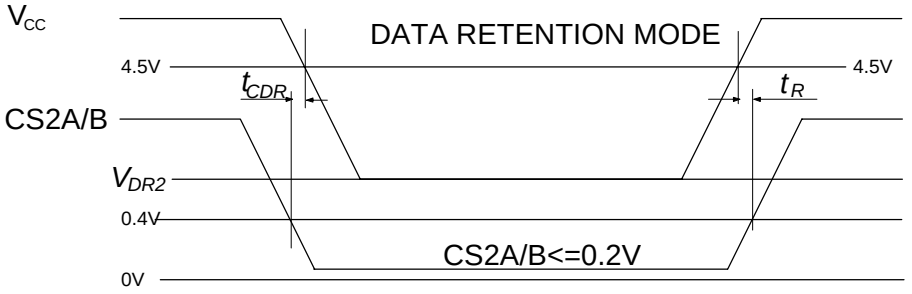
Parameter	*Symbol*	*Test Condition*	*min*	*typ (1)*	*max*	*Unit*
V_{CC} for Data Retention	V_{DR}	$\overline{CS1}_{A/B}$ • V_{CC}-0.2V or $CS2_{A/B}$ - 0.2V, 0.2V • V_{IN} • V_{CC}-0.2V	2.0	-	-	V
Data Retention Current	I_{CCDR}	V_{CC}=3.0V,V_{IN} • 0V, $\overline{CS1}_{A/B}$ •V_{CC}-0.2V or $CS2_{A/B}$ - 0.2V.	-	32	2000	µA
Chip Deselect to Data Retention	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R	See Retention Waveform	5	-	-	ms

Note (1) Typical figures are measured at 25℃ and specified loading.

Data Retention - $\overline{CS1_{A/B}}$ Controlled



Data Retention - $CS2_{A/B}$ Controlled



Operating Modes

The Truth Table below defines the logic inputs required to operate the MS161000FKXA in all valid modes. Refer to the DCElectrical Characteristics for the correct values of I_{SB} and I_{CC} for 8 bit or 16 bit operation.

MODE	$\overline{CS1_A}$	$CS2_A$	$\overline{CS1_B}$	$CS2_B$	$\overline{WE}$	$\overline{OE}$	*Data A*	*Data B*	*Current*
STANDBY	1	X	1	X	X	X	HIGH Z	HIGH Z	$I_{SB,1,2}$
STANDBY	X	0	X	0	X	X	HIGH Z	HIGH Z	$I_{SB,1,2}$
O/P DISABLE	0	1	0	1	1	1	HIGH Z	HIGH Z	I_{CCO}
8 BIT READ A	0	1	1	0	1	0	D_{OUT}	HIGH Z	I_{CCA8}
8 BIT READ B	1	0	0	1	1	0	HIGH Z	D_{OUT}	I_{CCA8}
16 BIT READ	0	1	0	1	1	0	D_{OUT}	D_{OUT}	I_{CCA16}
8 BIT WRITE A	0	1	1	0	0	1	D_{IN}	HIGH Z	I_{CCA8}
8 BIT WRITE B	1	0	0	1	0	1	HIGH Z	D_{IN}	I_{CCA8}
16 BIT WRITE	0	1	0	1	0	1	D_{IN}	D_{IN}	I_{CCA16}

1 = V_{IH} 0 = V_{IL} X = Don't Care.

Ordering Information

MS161000FKXALI-10

Speed	10	= 100 ns
	12	= 120 ns
	15	= 150 ns
Temperature range	Blank	= Commercial Temperature
	I	= Industrial Temperature
Power Consumption	Blank	= Standard Power Part
	L	= Low Power Part
Package	FKXA	= Plastic 44 pin 1.9" DIL.
Memory Organisation	16000	= 1M x 16 bit, user configurable as 2M x 8 bit.