TRAILING EDGE PRODUCT - MINIMUM ORDER APPLIES

hmp

256K x 32 SRAM

MS32256FKX-35/45/55

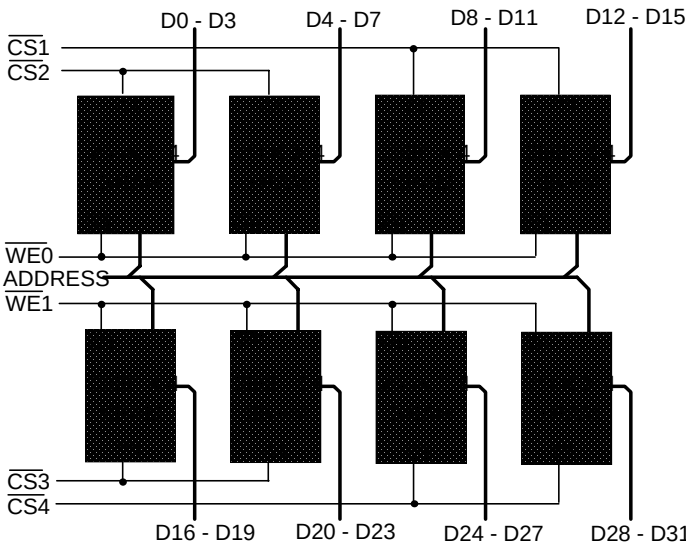
Issue 1.1 : October 1990

262,144 x 32 CMOS High Speed Static RAM

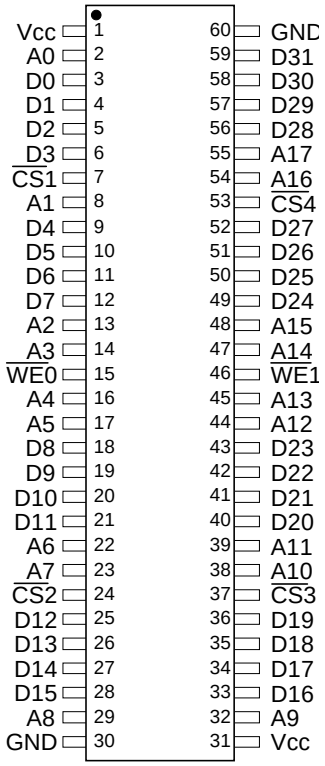
Features

Very Fast Access Times of 35/45/55 ns.
60 Pin 0.6" DIP Package.
Output Configurable as 32 / 16 / 8 bit
Operating Power 2.8 / 2.0 / 1.6 W (typ).
Low Power Standby 800 µW (typ).
160 µW (typ) -L Version.
Completely Static Operation.
Equal Access and Cycle times.
Battery back-up capability.
Directly TTL compatible.

Block Diagram



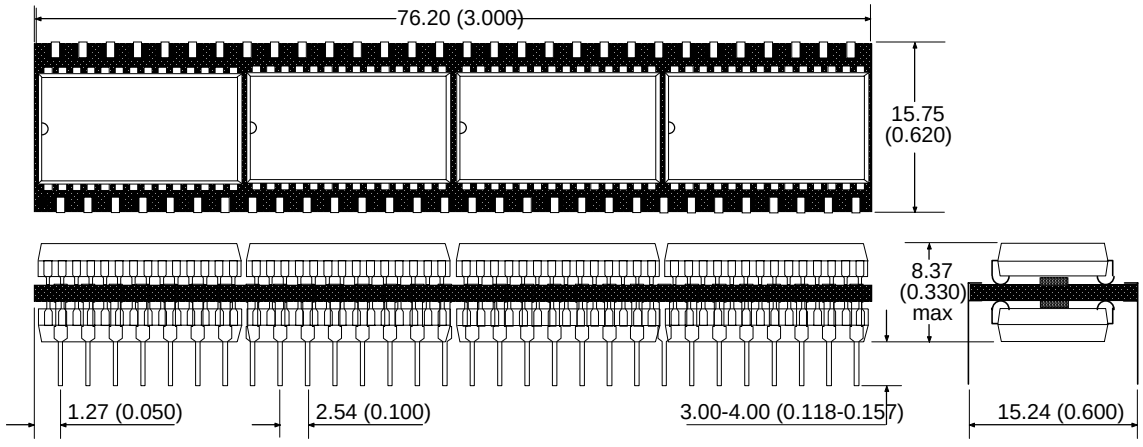
Pin Definition



Pin Functions

A0-A17	Address Inputs
D0-31	Data Inputs/Outputs
$\overline{\text{CS1-4}}$	Chip Selects
$\overline{\text{WE0-1}}$	Write Enables
V_{cc}	Power
GND	Ground

Package Details Dimensions in mm (inches) Tolerance on all dimensions ±0.254(0.010).



Absolute Maximum Ratings (1)

Voltage on any pin relative to GND	V_{IN}	-0.5 to +7.0	V
Power Dissipation	P_D	5.5	W
Storage Temperature	T_{STG}	-55 to +150	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
(2) Pulse width:- 2.0 V for less than 10ns.

Recommended Operating Conditions

		min	*typ*	*max*		
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input High Voltage	V_{IH}	2.2	-	V_{CC}+0.5	V	
Input Low Voltage	V_{IL}	-0.5	-	0.8	V	
Operating Temperature	T_A	0	-	70	°C	
	T_{AI}	-40	-	85	°C	(I Suffix)

DC Electrical Characteristics (T_A= -40℃ to +85℃,V_{CC}=5V+10%)

Parameter	*Symbol*	*Test Condition*	*min*	*typ (1)*	*max*	*Unit*
Input Leakage Current A0-A17	I_{LI1}	V_{CC}=5.5V,V_{IN}=GND to V_{CC}	-	-	16	µA
$\overline{WE0}$,$\overline{WE1}$	I_{LI2}	As above	-	-	8	µA
$\overline{CS1}$-$\overline{CS4}$	I_{LI3}	As above	-	-	4	µA
Output Leakage Current 8 BIT	I_{LO}	$\overline{CS}$'s=V_{IH},V_{OUT}=GND to V_{CC}	-	-	8	µA
Operating Supply Current 32 BIT	I_{CC32}	$\overline{CS}$'s=V_{IL},$I_{I/O}$=0mA, min. cycle	-	560	960	mA
16 BIT	I_{CC16}	As above	-	400	720	mA
8 BIT	I_{CC8}	As above	-	320	600	mA
Standby Supply Current TTL	I_{SB1}	$\overline{CS}$'s=V_{IH}	-	240	480	mA
CMOS	I_{SB2}	CS's•V_{CC}-0.2, 0.2V•V_{IN}•V_{CC}-0.2V	-	0.16	16	mA
-L Part CMOS	I_{SB3}	As above	-	32	1600	µA
Output Low Voltage	V_{OL}	I_{OL}=4.0 mA	-	-	0.4	V
Output High Voltage	V_{OH}	I_{OH}= -4.0 mA	2.4	-	-	V

Note (1) Typical limits are V_{CC}=5.0V and T_A=25℃ and specified loading

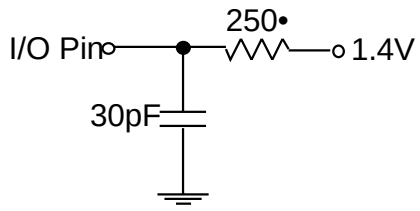
Capacitance (T_A=25°C,f=1MHz)

Parameter		*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance	A0 - A17,	C_{IN1}	V_{IN} =0V	-	48	pF
	$\overline{WE0}$, $\overline{WE1}$	C_{IN2}	V_{IN} =0V	-	24	pF
	$\overline{CE0}$ - $\overline{CE3}$	C_{IN3}	V_{IN} =0V	-	12	pF
Input/Output Capacitance:	8 BIT	$C_{I/O8}$	V_{OUT}=0V	-	44	pF
	16 BIT	CI/O16	VOUT=0V	-	22	pF
	32 BIT	CI/O32	VOUT=0V	-	11	pF

AC Test Conditions

* Input pulse levels: GND to 3.0V
* Input rise and fall times: 5ns
* Output Load : See Load Diagram
* Input/Output timing reference levels: 1.5V
* MS32256 tested in 32 bit mode.

Output Load

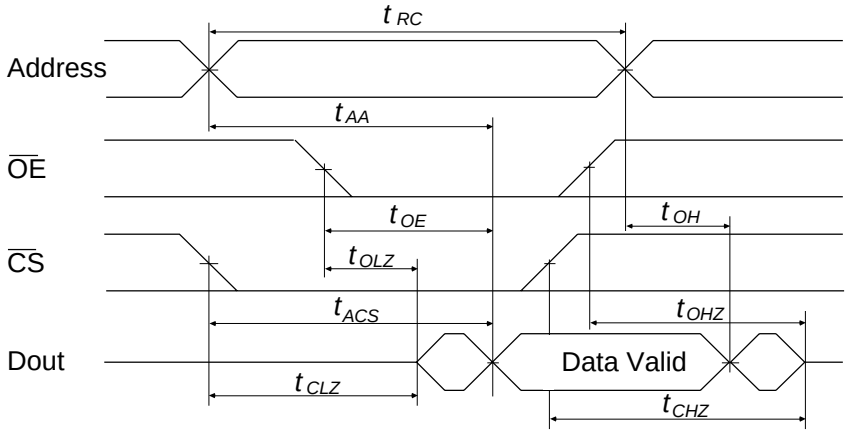


Electrical Characteristics & Recommended AC Operating Conditions

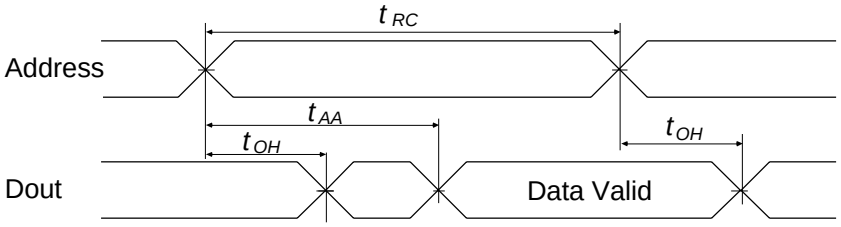
Read Cycle

Parameter	Symbol	-35 min	-35 max	-45 min	-45 max	-55 min	-55 max	Unit
Read Cycle Time	t_{RC}	35	-	45	-	55	-	ns
Address Access Time	t_{AA}	-	35	-	45	-	55	ns
Chip Select Access Time	t_{ACS}	-	35	-	45	-	55	ns
Output Enable to Output Valid	t_{OE}	-	18	-	23-	-	25	ns
Output Hold From Address Change	t_{OH}	5	-	5	-	5	-	ns
Chip Selection to Output in Low Z(1)	t_{CLZ}	10	-	10	-	10	-	ns
Output Enable to Output in Low Z(1)	t_{OLZ}	0	-	0	-	0	-	ns
Chip Deselection to Output in High Z(1)	t_{CHZ}	0	20	0	20	0	20	ns
Output Disable to Output in High Z(1)	t_{OHZ}	0	10	0	15	0	20	ns

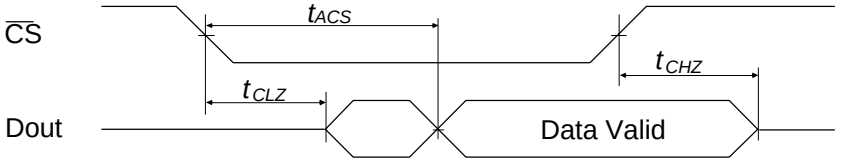
Read Cycle 1 Timing Waveform (1,2)



Read Cycle 2 Timing Waveform (1,2,3,5)



Read Cycle 3 Timing Waveform (1,2,4,5)

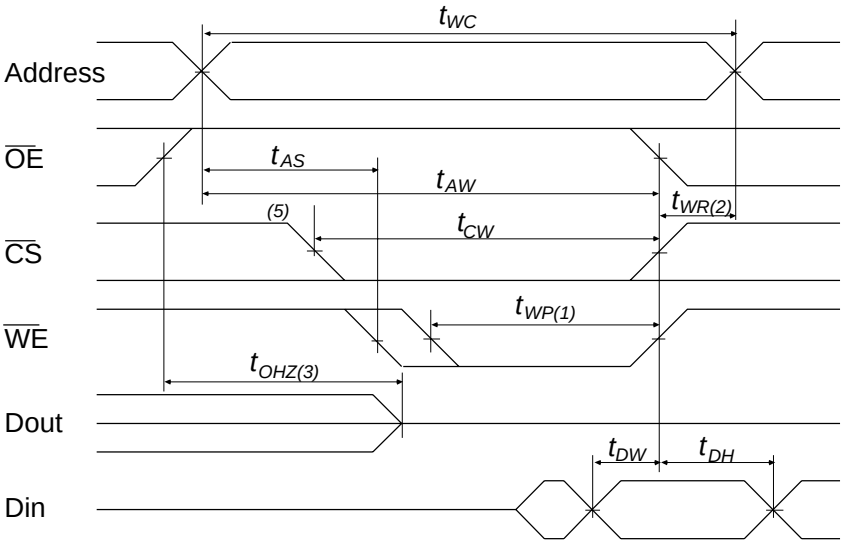


Notes: (1) t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.
(2) $\overline{WE}$ is High throughout a Read Cycle.
(3) Device is continuously selected, while $\overline{CS}$=$v_{IL.}$
(4) Address valid prior to or coincident with $\overline{CS}$ transition low.
(5) $\overline{OE}$=V_{IL}

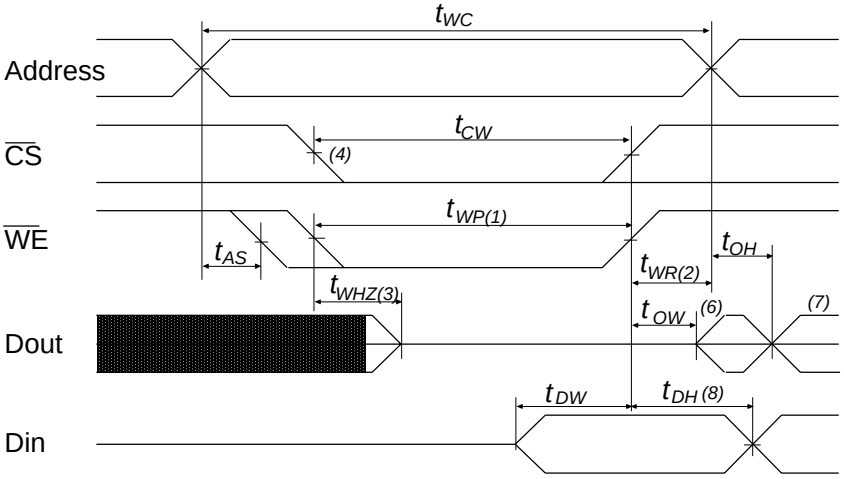
Write Cycle

Parameter	Symbol	-35 min	-35 max	-45 min	-45 max	-55 min	-55 max	Unit
Write Cycle Time	t_{WC}	35	-	45	-	55	-	ns
Chip Selection to End of Write	t_{CW}	30	-	40	-	50	-	ns
Address Valid to End of Write	t_{AW}	30	-	40	-	50	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	25	-	30	-	40	-	ns
Write Recovery Time	t_{WR}	3	-	3	-	3	-	ns
Data Valid to End of Write[9]	t_{WHZ}	0	10	0	15	0	20	ns
Data Valid to End of Write	t_{DW}	20	-	25	-	30	-	ns
Data Hold Time	t_{DH}	0	-	0	-	0	-	ns
Write Enabled to Output in High Z[9]	t_{OHZ}	0	10	0	15	0	20	ns
Output Active from End of Write[9]	t_{OW}	0	-	0	-	0	-	ns

Write Cycle 1 (WE Controlled)



Write Cycle 2 [5]



AC Characteristics Notes

(1) A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.

(2) t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.

(3) During this period, I/O pins are in the output state. Input signals out of phase must not be applied.

(4) If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.

(5) $\overline{OE}$ is continuously low. ($\overline{OE}$=V_{IL})

(6) Dout is in the same phase as written data of this write cycle.

(7) Dout is the read data of next address.

(8) If $\overline{CS}$ is low during this period, I/O pins are in the output state. Input signals out of phase must not be applied to I/O pins.

(9) t_{WHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.

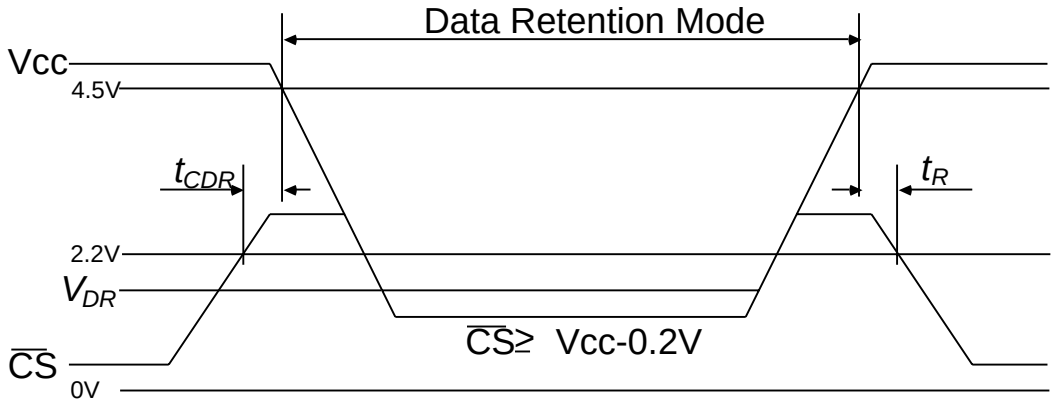
Low V_{cc} Data Retention Characteristics - L Version Only (T_A=0℃ to +70 °C)

Parameter	*Symbol*	*Test Condition*	*min*	*typ*(2)	*max*	*Unit*
V_{CC} for Data Retention	V_{DR}	$\overline{CS}$•V_{CC}-0.2V	2.0	-	-	V
Data Retention Current	I_{CCDR}	V_{CC}=3.0V, $\overline{CS}$•2.8V, 0.2V•V_{IN}•2.8V	-	16	800	µA
CS high to Data Retention Time	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R	See Retention Waveform	t_{RC*}(1)	-	-	ns

Notes: (1) t_{RC}=Read Cycle Time.

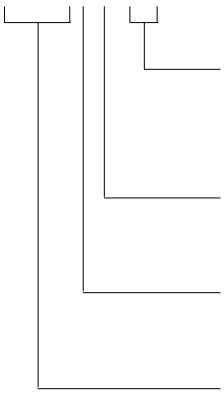
(2) Typical figures are measured at 25℃.

Low V_{CC} Data Retention Waveform - L Version only



Ordering Information

MS32256FKXLI-45



Speed	35 = 35 ns 45 = 45 ns 55 = 55 ns
Temperature Range	Blank = Commercial Temp. I = Industrial Temp.
Power Consumption	Blank = Standard Power Part L = Low Power Part
Package	FKX = Non Standard 0.6" Plastic DIL