

TRAILING EDGE PRODUCT - MINIMUM ORDER APPLIES
PRODUCT MAY BE MADE OBSOLETE WITHOUT NOTICE



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8K x 8 SRAM

MSM88 - 85/10

Issue 1.0 : February 2000

Description

The MSM88 is a Static RAM organised as 8K x 8 available with access times of 85 or 100ns. The device is available in two ceramic package options. It features completely static operation with a low power standby mode and is 3.0V battery back-up compatible. It is directly TTL compatible and has common data inputs and outputs.

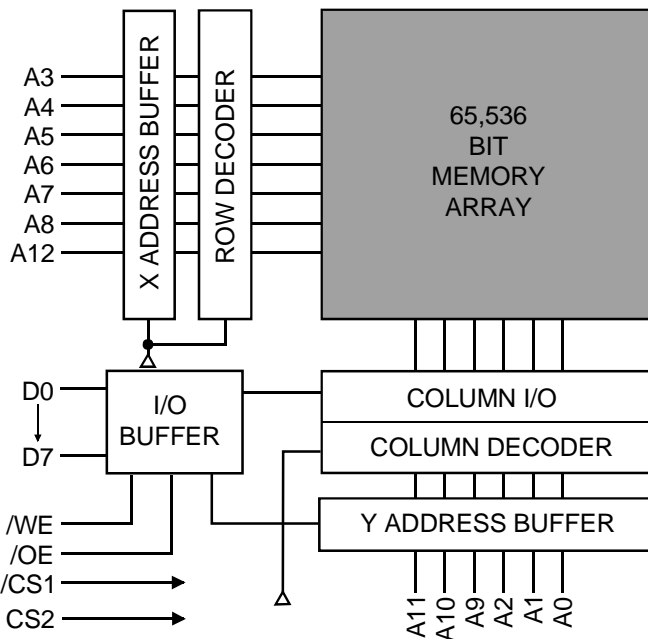
The device may be screened in accordance with MIL-STD-883.

8,192 x 8 CMOS Static RAM

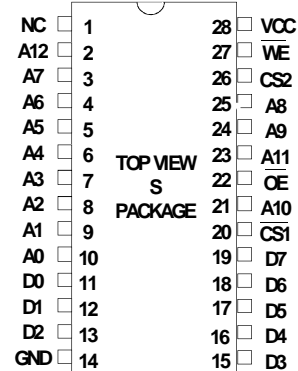
Features

- Fast Access Times of 85 or 100 ns.
- JEDEC Standard footprint.
- Low Power Operation : 550 mW (max)
- Low Power Standby : 27.5 mW (max) -L version.
- Low Voltage Data Retention.
- Directly TTL compatible.
- Completely Static Operation.

Block Diagram



Pin Definitions



Package Details

| Pin Count | Description | Package Type |
|-----------|-------------------------|--------------|
| 28 | 0.6" Dual-in-Line (DIP) | S |

Pin Functions

- A0~A12** Address inputs
- D0-7** Data Input/Output
- CS1, CS2** Chip Selects
- OE** Output Enable
- WE** Write Enable
- V_{cc}** Power(+5V)
- GND** Ground

DC OPERATING CONDITIONS**Absolute Maximum Ratings** ⁽¹⁾

| | | | |
|--|-----------|-------------|----|
| Voltage on any pin relative to V_{SS} ⁽²⁾ | V_T | -0.5V to +7 | V |
| Power Dissipation | P_T | 1 | W |
| Storage Temperature | T_{STG} | -65 to +150 | °C |

Notes : (1) Stresses above those listed may cause permanent damage. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) Pulse width:- -3.0V for less than 10ns.

Recommended Operating Conditions

| Parameter | Symbol | min | typ | max | Unit |
|-----------------------|----------|------|-----|--------------|---------------------|
| Supply Voltage | V_{CC} | 4.5 | 5.0 | 5.5 | V |
| Input High Voltage | V_{IH} | 2.2 | - | $V_{CC}+0.5$ | V |
| Input Low Voltage | V_{IL} | -0.5 | - | 0.8 | V |
| Operating Temperature | T_A | 0 | - | 70 | °C |
| | T_{AL} | -40 | - | 85 | °C (Suffix I) |
| | T_{AM} | -55 | - | 125 | °C (Suffix M, MB) |

DC Electrical Characteristics ($V_{CC} = 5.0V \pm 10\%$, $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$)

| Parameter | Symbol | Test Condition | min | typ | max | Unit |
|------------------------------|-----------|---|-----------|---|-----|---------------|
| Input Leakage Current | I_{LI} | $V_{IN} = 0V$ to V_{CC} | -10 | - | 10 | μA |
| Output Leakage Current | I_{LO} | $\overline{CS1} = V_{IH}$ or $CS2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$, $V_{I/O} = V_{SS}$ to V_{CC} | -10 | - | 10 | μA |
| Average Supply Current | I_{CC} | $\overline{CS1} = V_{IL}$, $CS2 = V_{IH}$, $I_{I/O} = 0\text{mA}$, $V_{IN} = V_{IL}$ or V_{IH} | - | - | 120 | mA |
| Standby Supply Current - TTL | I_{SB1} | $\overline{CS1} = V_{IH}$, $CS2 = V_{IL}$, Other input = V_{IL} or V_{IH} | - | - | 40 | mA |
| | | -L Version - CMOS | I_{SB2} | $\overline{CS1} \geq V_{CC} - 0.2V$, $CS2 \geq V_{CC} - 0.2V$ or $CS2 \leq 0.2V$ Other input = 0 ~ V_{CC} | - | - |
| Output Voltage | V_{OL} | $I_{OL} = 2.1\text{ mA}$ | - | - | 0.4 | V |
| | V_{OH} | $I_{OH} = -1.0\text{ mA}$ | 2.4 | - | - | V |

Typical values at $V_{CC} = 5.0V$, $T_A = 25^\circ\text{C}$ and specified loading

Capacitance ($V_{CC} = 5V \pm 10\%$, $T_A = 25^\circ\text{C}$)

| Parameter | Symbol | Test Condition | min | typ | max | Unit |
|-------------------|-----------|----------------|-----|-----|-----|------|
| Input Capacitance | C_{IN} | $V_{IN} = 0V$ | - | - | 8 | pF |
| I/O Capacitance | $C_{I/O}$ | $V_{I/O} = 0V$ | - | - | 10 | pF |

Note: This parameter is not 100% tested.

Operating Modes

The table below shows the logic inputs required to control the MSM88 SRAM.

| Mode | /CS1 | CS2 | /WE | /OE | I/O Pin | Power |
|---------|------|-----|-----|-----|------------------|---------|
| STANDBY | H | X | X | X | HIGH-Z | STANDBY |
| STANDBY | X | L | X | X | HIGH-Z | STANDBY |
| READ | L | H | H | L | D _{OUT} | ACTIVE |
| WRITE | L | H | L | X | D _{IN} | ACTIVE |

1 = V_{IH}, 0 = V_{IL}, X = Don't Care

Low V_{cc} Data Retention Characteristics - L Version Only (T_A = -55°C to +125°C)

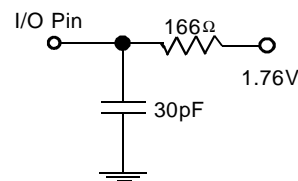
| Parameter | Symbol | Test Condition | min | typ | max | Unit |
|--------------------------------------|--------------------|---|-----|-----|-----|------|
| V _{cc} for Data Retention | V _{DR} | $\overline{CS1}^{(1)} \geq V_{cc} - 0.2V$ | 2.0 | - | 5.5 | V |
| Data Retention Current -L Version | I _{CCDR2} | V _{cc} = 3.0V, $\overline{CS1} \geq V_{cc} - 0.2V$, CS2 $\geq V_{cc} - 0.2V$ or CS2 $\leq 0.2V$ Other Input + 0 ~ V _{cc} | - | - | 800 | μA |
| Chip Deselect to Data Retention Time | t _{SDR} | See Retention Waveform | 0 | - | - | ns |
| Operation Recovery Time | t _{RDR} | See Retention Waveform | 5 | - | - | ms |

Notes (1) 1. $\overline{CS1} \geq V_{cc} - 0.2V$, CS2 $\geq V_{cc} - 0.2V$ ($\overline{CS1}$ controlled) or CS2 $\leq 0.2V$ (CS2 controlled)

AC Test Conditions

- * Input pulse levels: 0V to 3.0V
- * Input rise and fall times: 5ns
- * Input and Output timing reference levels: 1.5V
- * Output load: see diagram
- * V_{cc} = 5V ± 10%

Output Load

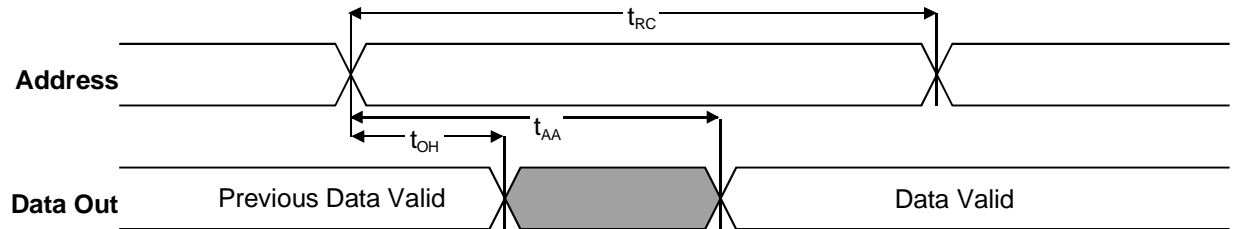
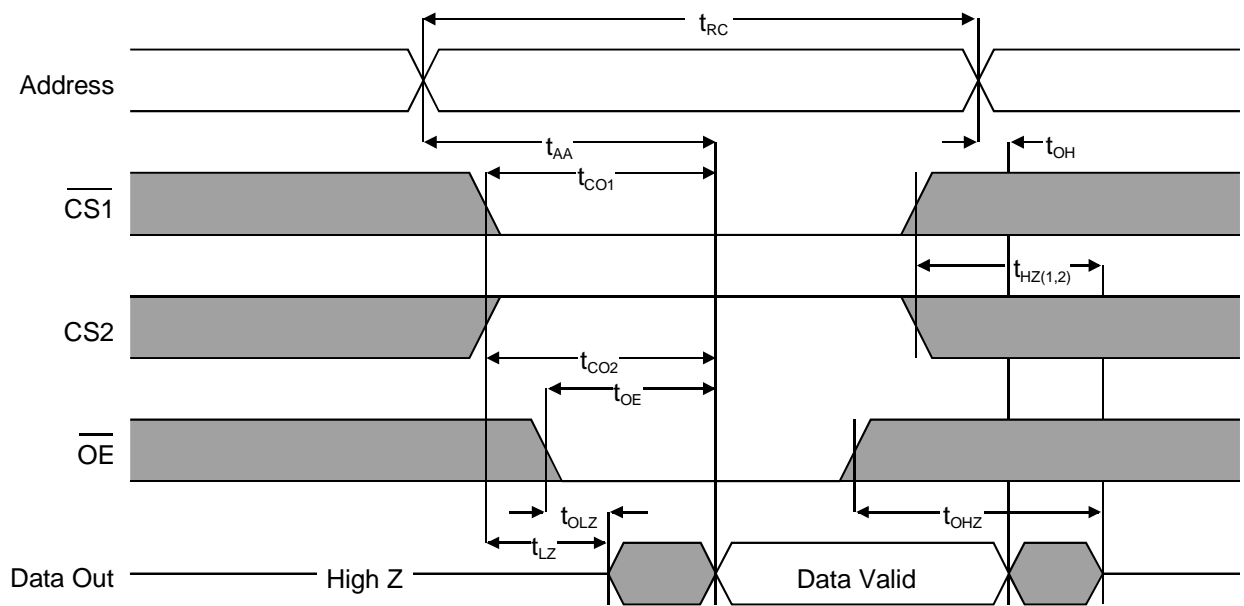


AC OPERATING CONDITIONS**Read Cycle**

| Parameter | Symbol | 85 | | 10 | | Unit |
|---|--------------------|-----|-----|-----|-----|------|
| | | min | max | min | max | |
| Read Cycle Time | t_{RC} | 85 | - | 100 | - | ns |
| Address Access Time | t_{AA} | - | 85 | - | 100 | ns |
| Chip Select Access Time - $\overline{CS1}, CS2$ | t_{CO1}, t_{CO2} | - | 85 | - | 50 | ns |
| Output Enable to Output Valid | t_{OE} | - | 45 | - | 45 | ns |
| Output Hold from Address Change | t_{OH} | 5 | - | 10 | - | ns |
| Chip Selection to Output in Low Z | t_{LZ} | 5 | - | 10 | - | ns |
| Output Enable to Output in Low Z | t_{OLZ} | 5 | - | 5 | - | ns |
| Chip Deselection to Output in High Z ⁽³⁾ | t_{HZ} | 0 | 35 | 0 | 35 | ns |
| Output Disable to Output in High Z ⁽³⁾ | t_{OHZ} | 0 | 35 | 0 | 35 | ns |

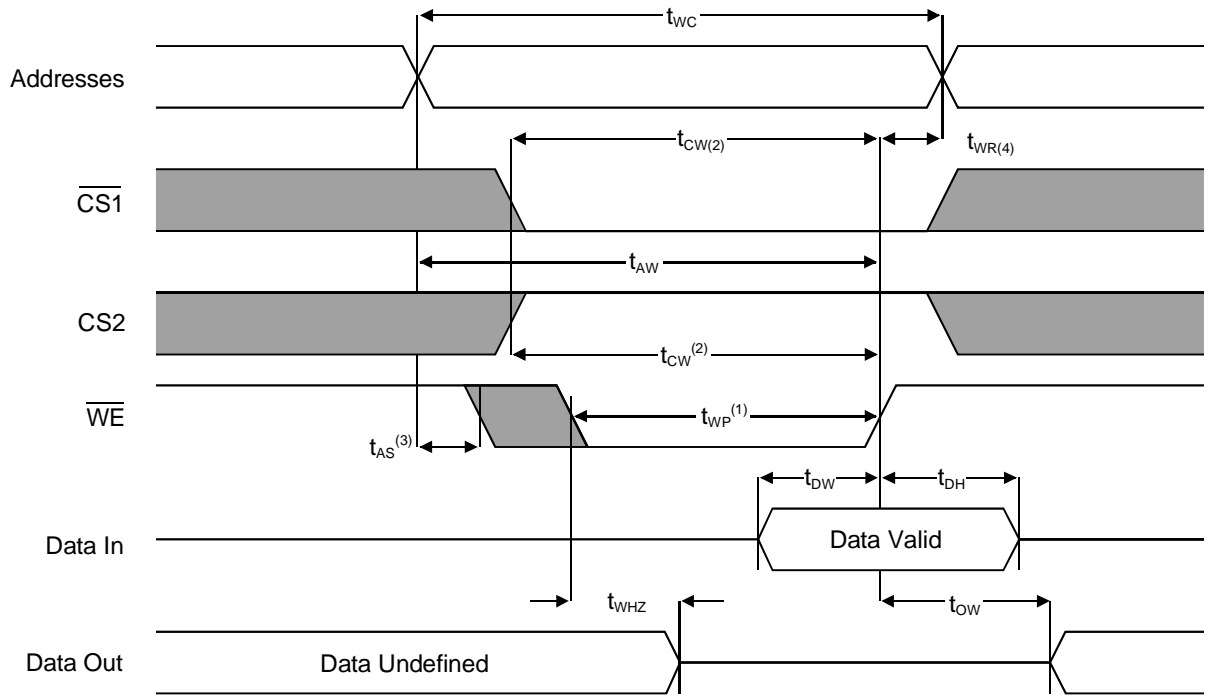
Write Cycle

| Parameter | Symbol | 85 | | 10 | | Unit |
|---------------------------------|-----------|------|-----|------|-----|------|
| | | min. | max | min. | max | |
| Write Cycle Time | t_{WC} | 85 | - | 100 | - | ns |
| Chip Selection to End of Write | t_{CW} | 75 | - | 80 | - | ns |
| Address Valid to End of Write | t_{AW} | 75 | - | 80 | - | ns |
| Address Setup Time | t_{AS} | 0 | - | 0 | - | ns |
| Write Pulse Width | t_{WP} | 60 | - | 60 | - | ns |
| Write Recovery Time | t_{WR} | 0 | - | 0 | - | ns |
| Write to Output in High Z | t_{WHZ} | 0 | 30 | 0 | 35 | ns |
| Data to Write Time Overlap | t_{DW} | 40 | - | 40 | - | ns |
| Data Hold from Write Time | t_{DH} | 0 | - | 0 | - | ns |
| Output Active from End of Write | t_{OW} | 5 | - | 5 | - | ns |

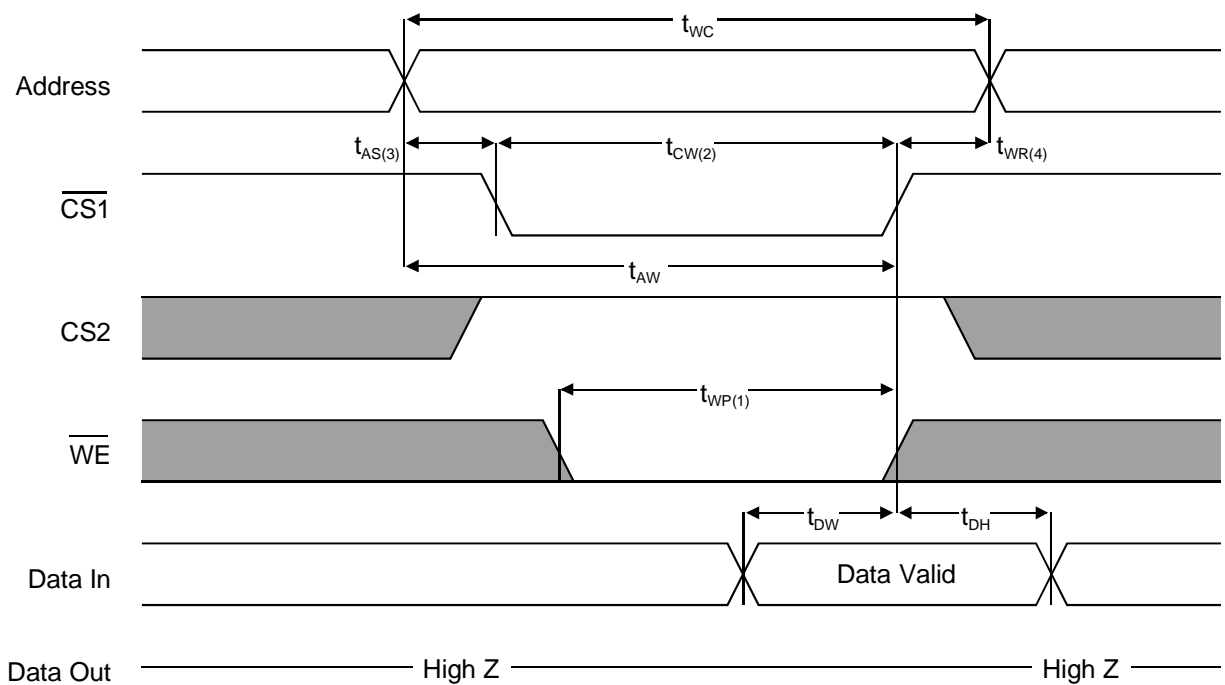
Read Cycle 1 Timing Waveform (Address Controlled, $\overline{CS1}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$)

Read Cycle 2 Timing Waveform ($\overline{WE}=V_{IH}$)

Notes : (Read Cycle)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve open circuit conditions, and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ} (max.) is less than t_{LZ} (min.) both for a given device and from device to device interconnection.

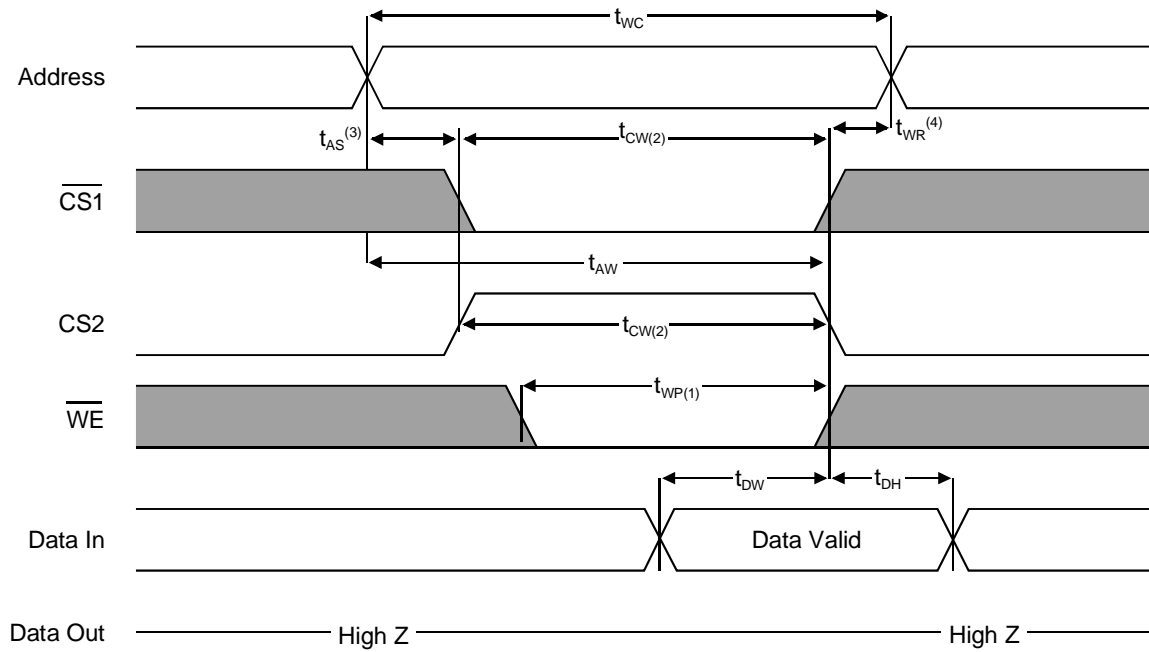
Write Cycle 1 Timing Waveform (\overline{WE} Controlled)



Write Cycle 2 Timing Waveform ($\overline{CS1}$ Controlled)



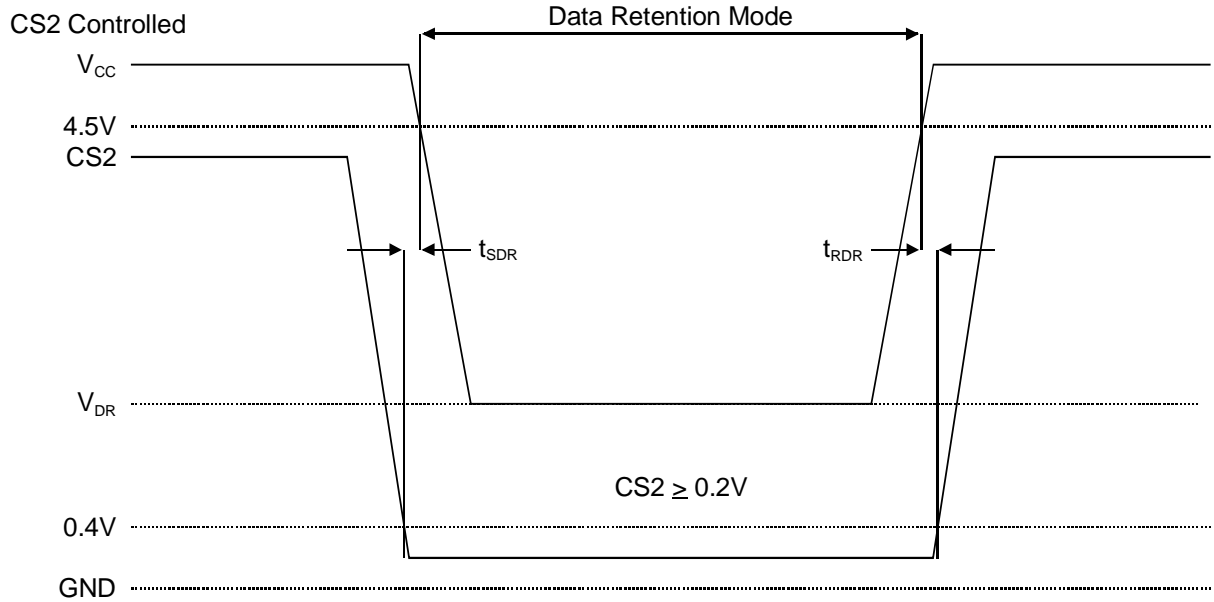
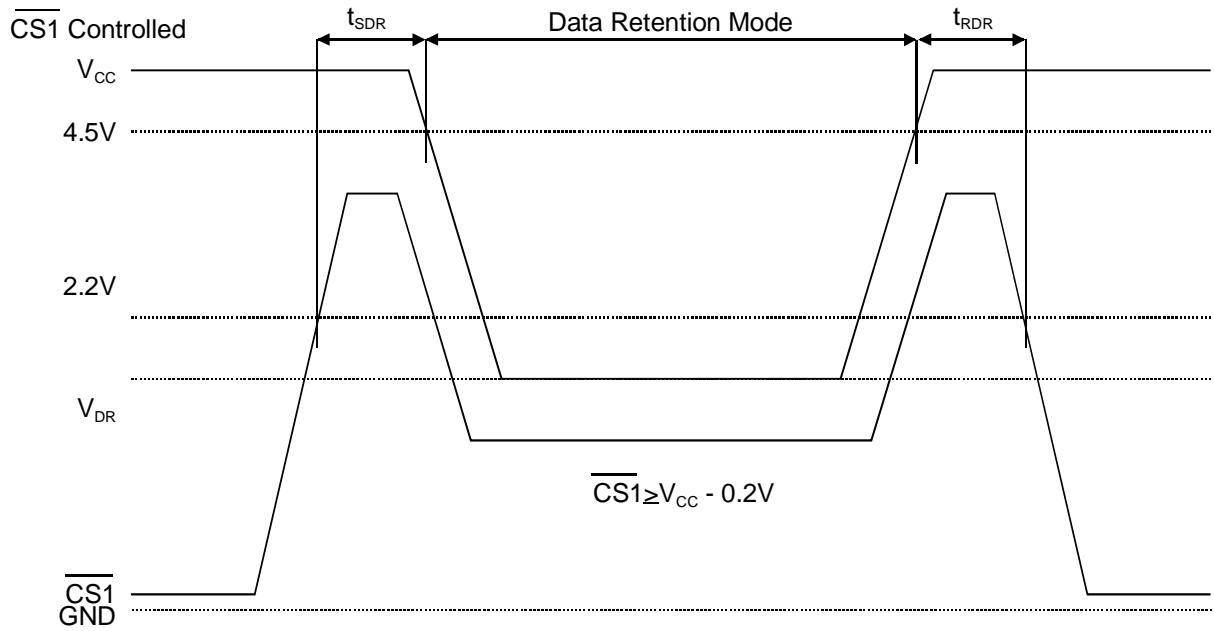
Write Cycle 3 Timing Waveform (CS2 Controlled)



Notes:

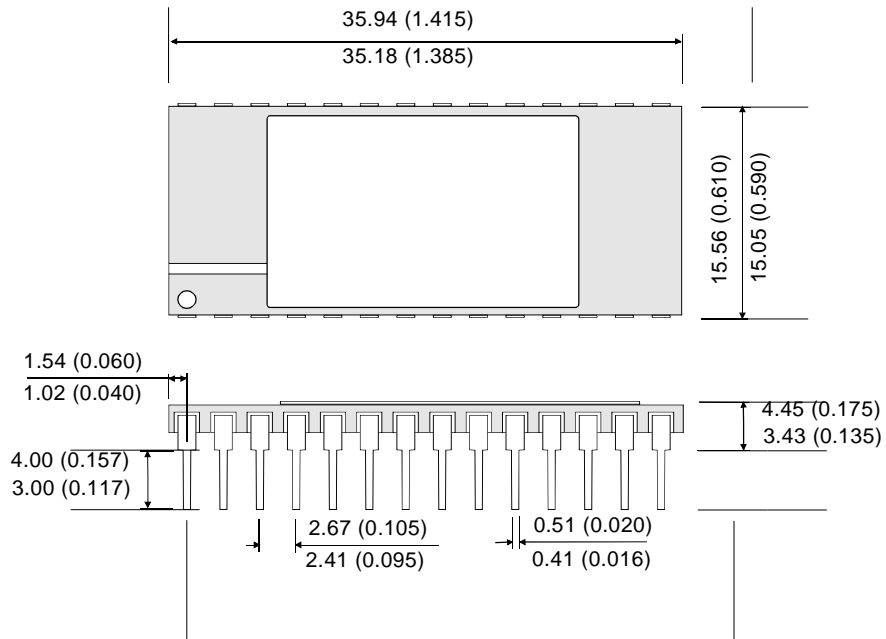
1. A Write occurs during the overlap of a low $\overline{CS1}$, a high $CS2$ and a low \overline{WE} . A Write begins at the latest transition among $\overline{CS1}$ goes low, $CS2$ going high and \overline{WE} going low : A Write end at the earliest transition among $\overline{CS1}$ going high, $CS2$ going low and \overline{WE} going high. t_{WP} is measured from the beginning of Write to the end of Write.
2. t_{CW} is measured from the $\overline{CS1}$ going low or $CS2$ going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. $t_{WR(1)}$ applied in case a write ends as $\overline{CS1}$ or \overline{WE} going high $t_{WR(2)}$ applied in case a write ends as $CS2$ going to low.

Data Retention Timing Waveforms



PACKAGE DETAILS dimensions in mm (inches)

28 pin 0.6" Dual-In-Line (DIL) - 'S' Package

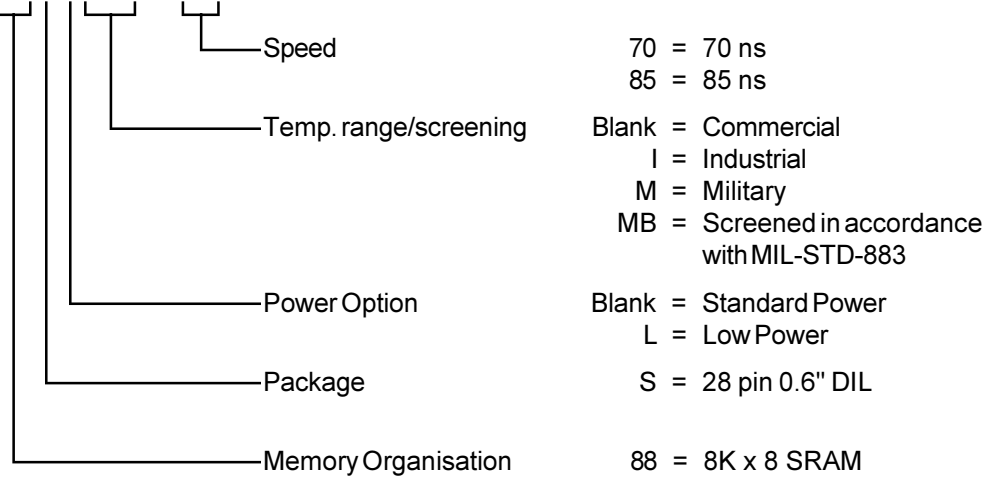


SCREENING**Military Screening Procedure**

The Component Screening Flow for high reliability parts in accordance with Mil-883 method 5004 is shown below:

| MB COMPONENT SCREENING FLOW | | |
|--|---|--------------|
| <i>SCREEN</i> | <i>TEST METHOD</i> | <i>LEVEL</i> |
| Visual and Mechanical | | |
| Internal visual | 2010 Condition B or manufacturers equivalent | 100% |
| Temperature cycle | 1010 Condition C (10 Cycles,-65°C to +150°C) | 100% |
| Constant acceleration | 2001 Condition E (Y, only) (30,000g) | 100% |
| Pre-Burn-in electrical | Per applicable device specifications at $T_A=+25^\circ\text{C}$ | 100% |
| Burn-in | Method 1015, Condition D, $T_A=+125^\circ\text{C}$, 160hrs min | 100% |
| Final Electrical Tests | Per applicable Device Specification | |
| Static (dc) | a) @ $T_A=+25^\circ\text{C}$ and power supply extremes | 100% |
| | b) @ temperature and power supply extremes | 100% |
| Functional | a) @ $T_A=+25^\circ\text{C}$ and power supply extremes | 100% |
| | b) @ temperature and power supply extremes | 100% |
| Switching (ac) | a) @ $T_A=+25^\circ\text{C}$ and power supply extremes | 100% |
| | b) @ temperature and power supply extremes | 100% |
| Percent Defective allowable (PDA) | Calculated at post-burn-in at $T_A=+25^\circ\text{C}$ | 5% |
| Hermeticity | 1014 | |
| Fine | Condition A | 100% |
| Gross | Condition C | 100% |
| External Visual | 2009 Per vendor or customer specification | 100% |

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|-----------------------------|
| ORDERING INFORMATION |
|-----------------------------|

MSM88SLMB - 85

THE MSM88S IS NOT RECOMMENDED FOR NEW DESIGNS AND MAY BE MADE OBSOLETE WITHOUT NOTICE....

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