

**TRAILING EDGE PRODUCT - MINIMUM ORDER APPLIES  
PRODUCT MAY BE MADE OBSOLETE WITHOUT NOTICE**



**128K x 8 SRAM**

**MSM8128A - 85/10/12**

Elm Road, West Chirton, NORTH SHIELDS, Tyne & Wear  
NE29 8SE, England Tel. +44 (0191) 2930500 Fax. +44 (0191) 2590997

Issue 1.0 April 2001

**Description**

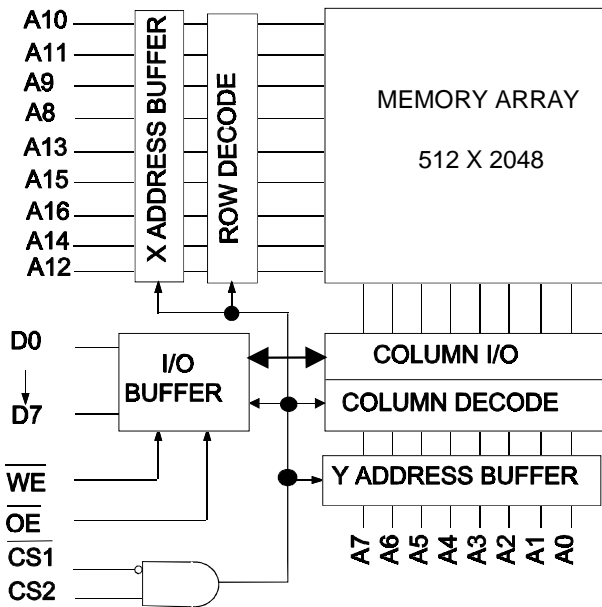
The MSM8128 is a 1Mbit monolithic SRAM organised as 128K x 8. It is available in with access times of 85, 100 & 120ns. It has a low power standby version and has 3.0V battery backup capability. It is directly TTL compatible and has common data inputs and outputs. Two pinout variants (single and dual CS) are available.  
All versions may be screened in accordance with MIL-STD-883.

131,072 x 8 CMOS Static RAM

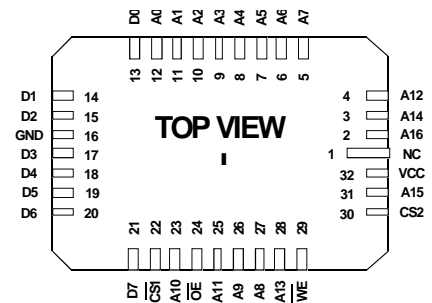
**Features**

- Access Times of 85/100/120 ns
- JEDEC standard Dual  $\overline{CS}$  footprints.
- Operating Power 605 mW (max)
- Low Power Standby (-L) 2.53 mW (max)
- Low Voltage Data Retention.
- Completely Static Operation
- Directly TTL compatible.
- May be processed in accordance with MIL-STD-883

**Block Diagram**



**Pin Definition**



See Page 9 for X pinout

**Pin Functions**

- A0-A16** Address Inputs
- D0-7** Data Input/Output
- CS1** Chip Select 1
- CS2** Chip Select 2
- OE** Output Enable
- WE** Write Enable
- NC** No Connect
- V<sub>cc</sub>** Power (+5V)
- GND** Ground

**Package Details**

Pin Count	Description	Package Type
32	LCC (0.45 x 0.55" nom)	W

Package details on pages 8 & 9.

**DC OPERATING CONDITIONS****Absolute Maximum Ratings**

Voltage on any pin relative to $V_{SS}$	$V_T$	-0.5V	to	+7.0	V
Power Dissipation	$P_T$			1	W
Storage Temperature	$T_{STG}$	-55	to	+150	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Recommended Operating Conditions**

		<i>min</i>	<i>typ</i>	<i>max</i>	
Supply Voltage	$V_{CC}$	4.5	5.0	5.5	V
Input High Voltage	$V_{IH}$	2.2	-	5.8	V
Input Low Voltage	$V_{IL}$	-0.3	-	0.8	V
Operating Temperature	$T_A$	0	-	70	°C
	$T_{AI}$	-40	-	85	°C ( <b>I</b> suffix)
	$T_{AM}$	-55	-	125	°C ( <b>M</b> , <b>MB</b> suffix)

**DC Electrical Characteristics** ( $V_{CC} = 5.0V \pm 10\%$ ,  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ )

<i>Parameter</i>	<i>Symbol</i>	<i>Test Condition</i>	<i>min</i>	<i>typ</i>	<i>max</i>	<i>Unit</i>
Input Leakage Current	$I_{LI}$	$\overline{V_{IH}}=0V$ to $V_{CC}$	-1	-	1	$\mu\text{A}$
Output Leakage Current	$I_{IO}$	$\overline{CS1}=V_{IH}$ , $CS2 = V_{IL}$ , $V_{IO}=0V$ to $V_{CC}$ , $\overline{OE}=V_{IH}$	-1	-	1	$\mu\text{A}$
Average Supply Current	$I_{CC1}$	Min. Cycle, $V_{IN}=V_{IL}$ or $V_{IH}$	-	-	110	mA
Standby Supply Current	$I_{SB1}$	$\overline{CS1}=V_{IH}$ , $CS2 = V_{IL}$ , I/P's static	-	-	3.5	mA
-L Part	$I_{SB2}$	$\overline{CS1} \geq V_{CC} - 0.2V$ , $0.2V \geq CS2 \geq V_{CC} - 0.2V$ , $V_{IN} \geq 0.2V$	-	-	460	$\mu\text{A}$
Output Voltage	$V_{OL}$	$I_{OL} = 2.1 \text{ mA}$	-	-	0.4	V
	$V_{OH}$	$I_{OH} = -1.0 \text{ mA}$	2.4	-	-	V

**Capacitance** ( $V_{CC}=5V \pm 10\%$ ,  $T_A=25^\circ\text{C}$ )

<i>Parameter</i>	<i>Symbol</i>	<i>Test Condition</i>	<i>typ</i>	<i>max</i>	<i>Unit</i>
I/P Capacitance	$C_{IN}$	$V_{IN}=0V$	-	8	pF
I/O Capacitance	$C_{IO}$	$V_{IO}=0V$	-	10	pF

Note: This parameter is sampled and not 100% tested.

## Operating Modes

The table below shows the logic inputs required to control the MSM8128 SRAM.

Mode	$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	$V_{CC}$ Current	I/O Pin	Reference Cycle
Not Selected	1	X	X	X	$I_{SB1}, I_{SB2}$	High Z	Power Down
Not Selected	X	0	X	X	$I_{SB}, I_{SB1}$	High Z	Power Down
Output Disable	0	1	1	1	$I_{CC}$	High Z	
Read	0	1	0	1	$I_{CC}$	$D_{OUT}$	Read Cycle
Write	0	1	X	0	$I_{CC}$	$D_{IN}$	Write Cycle

1 =  $V_{IH}$ ,      0 =  $V_{IL}$ ,      X = Don't Care

## Low $V_{CC}$ Data Retention Characteristics - L Version Only ( $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ )

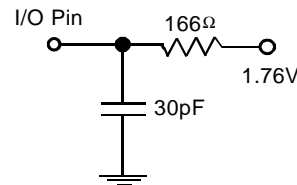
Parameter	Symbol	Test Condition	min	typ	max	Unit
$V_{CC}$ for Data Retention	$V_{DR}$	$\overline{CS1} \geq V_{CC} - 0.2\text{V}$ , $CS2 \geq V_{CC} - 0.2\text{V}$ or $0\text{V} \leq CS2 \leq 0.2\text{V}$ , $V_{IN} \geq 0\text{V}$	2.0	-	-	V
Data Retention Current	$I_{CCDR}$	$V_{CC} = 3.0\text{V}$ , $V_{IN} \geq 0\text{V}$ , $\overline{CS1} \geq V_{CC} - 0.2\text{V}$ , $CS2 \geq V_{CC} - 0.2\text{V}$ or $0\text{V} \leq CS2 \leq 0.2\text{V}$ .	-	-	700	$\mu\text{A}$
Chip Deselect to Data Retention	$t_{CDR}$	See Retention Waveform	0	-	-	ns
Operation Recovery Time	$t_R$	See Retention Waveform	5	-	-	ms

Notes (1) CS2 controls address buffer, WE buffer,  $\overline{CS1}$  buffer and  $\overline{OE}$  buffer. If CS2 controls data retention mode,  $V_{in}$  levels ( $\overline{WE}, \overline{OE}, \overline{CS1}, I/O$ ) can be in the high impedance state. If CS1 controls Data Retention mode, CS2 must be  $\geq V_{CC} - 0.2\text{V}$  or  $0\text{V} \leq CS2 \leq 0.2\text{V}$ . The other input levels (address,  $\overline{WE}, \overline{OE}, I/O$ ) can be in the high impedance state.

## AC Test Conditions

## Output Load

- \* Input pulse levels: 0V to 3.0V
- \* Input rise and fall times: 5ns
- \* Input and Output timing reference levels: 1.5V
- \* Output load: See Load Diagram
- \*  $V_{CC} = 5\text{V} \pm 10\%$

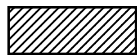


**AC OPERATING CONDITIONS****Read Cycle**

Parameter	Symbol	70		85		10		12		Unit
		min	max	min	max	min	max	min	max	
Read Cycle Time	$t_{RC}$	70	-	85	-	100	-	120	-	ns
Address Access Time	$t_{AA}$	-	70	-	85	-	100	-	120	ns
Chip Select ( $\overline{CS1}$ ) Access Time <sup>(2)</sup>	$t_{ACS1}$	-	70	-	85	-	100	-	120	ns
Chip Select ( $\overline{CS2}$ ) Access Time <sup>(2)</sup>	$t_{ACS2}$	-	70	-	85	-	100	-	120	ns
Output Enable to Output Valid	$t_{OE}$	-	35	-	45	-	50	-	60	ns
Output Hold from Address Change	$t_{OH}$	5	-	5	-	10	-	10	-	ns
Chip Selection ( $\overline{CS1}$ ) to Output in Low Z	$t_{CLZ1}$	10	-	10	-	10	-	10	-	ns
Chip Selection ( $\overline{CS2}$ ) to Output in Low Z	$t_{CLZ2}$	10	-	10	-	10	-	10	-	ns
Output Enable to Output in Low Z	$t_{OLZ}$	5	-	5	-	5	-	5	-	ns
Chip Disable ( $\overline{CS1}$ ) to Output in High Z <sup>(3)</sup>	$t_{CHZ1}$	0	35	0	35	0	35	0	45	ns
Chip Disable ( $\overline{CS2}$ ) to Output in High Z <sup>(3)</sup>	$t_{CHZ2}$	0	35	0	35	0	35	0	45	ns
Output Disable to Output in High Z <sup>(3)</sup>	$t_{OHZ}$	0	30	0	30	0	35	0	45	ns

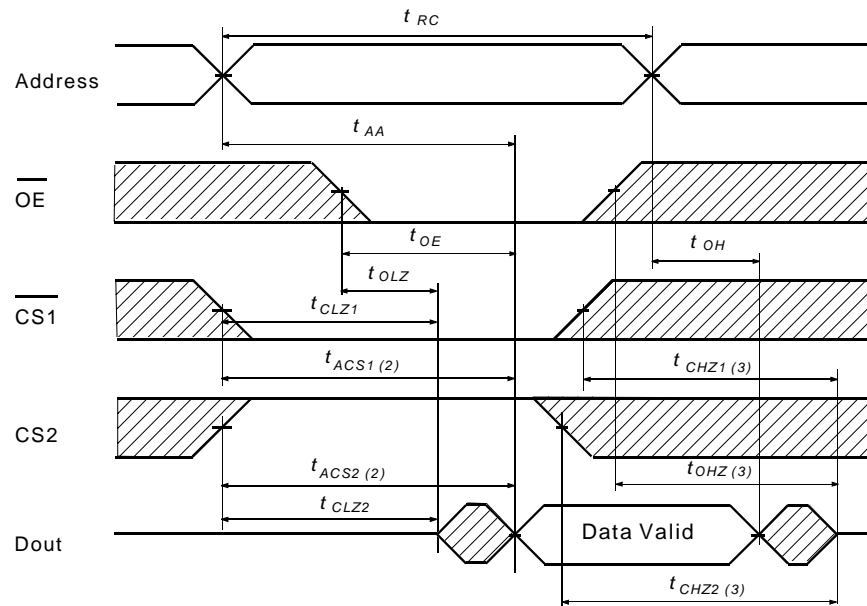
**Write Cycle**

Parameter	Symbol	70		85		10		12		Unit
		min	max	min	max	min	max	min	max	
Write Cycle Time	$t_{WC}$	70	-	85	-	100	-	120	-	ns
Chip Selection to End of Write	$t_{CW}$	60	-	75	-	85	-	100	-	ns
Address Valid to End of Write	$t_{AW}$	60	-	75	-	85	-	100	-	ns
Address Setup Time	$t_{AS}$	0	-	0	-	0	-	0	-	ns
Write Pulse Width	$t_{WP}$	50	-	60	-	70	-	70	-	ns
Write Recovery Time ( $\overline{WE}$ , $\overline{CS1}$ )	$t_{WR1}$	5	-	5	-	5	-	5	-	ns
( $\overline{CS2}$ )	$t_{WR2}$	5	-	5	-	5	-	5	-	ns
Write to Output in High Z	$t_{WHZ}$	0	30	0	30	0	35	0	40	ns
Data to Write Time Overlap	$t_{DW}$	30	-	35	-	40	-	45	-	ns
Data Hold from Write Time	$t_{DH}$	0	-	0	-	0	-	0	-	ns
Output Active from End of Write	$t_{OW}$	5	-	5	-	5	-	5	-	ns



Consult Factory

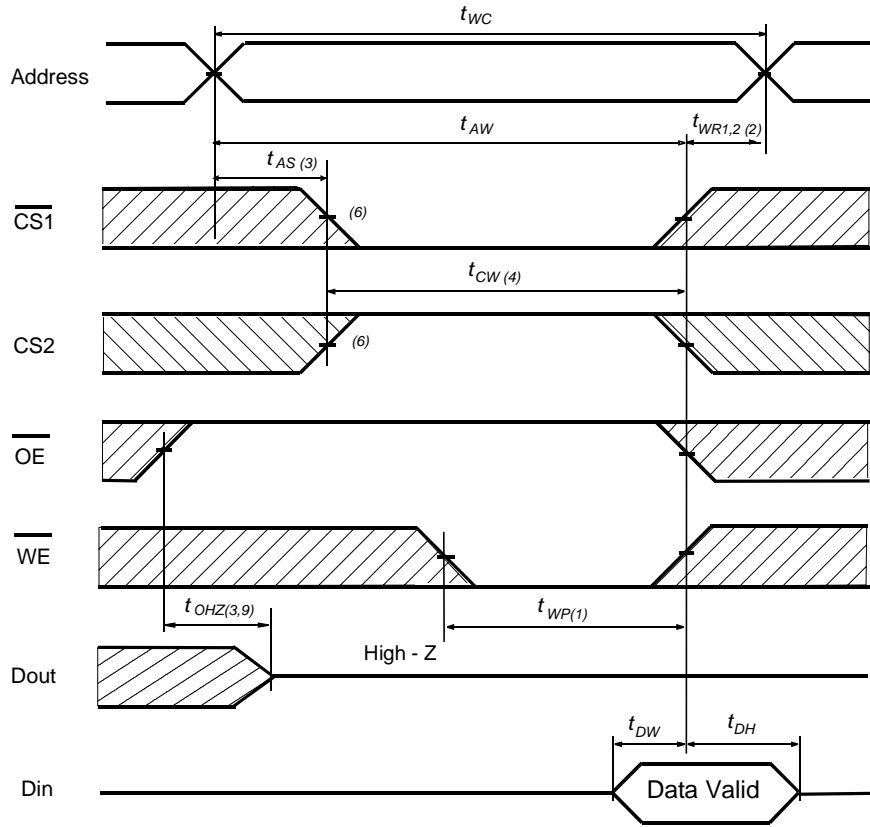
### Read Cycle Timing Waveform <sup>(1,2)</sup>



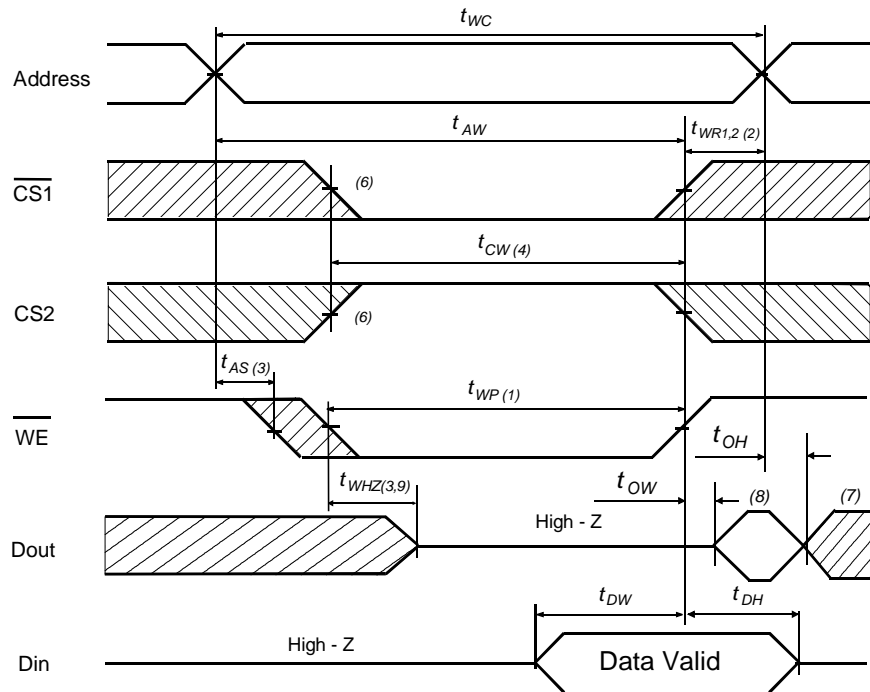
#### Notes:

- (1)  $\overline{WE}$  is High for Read Cycle.
- (2) Address valid prior to or coincident with  $\overline{CS1}$  transition low or CS2 high.
- (3)  $t_{CHZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. At any given temperature and voltage condition,  $t_{CHZ}$  max is less than  $t_{CLZ}$  min both for a given device and from device to device. This parameter is sampled and not 100% tested.

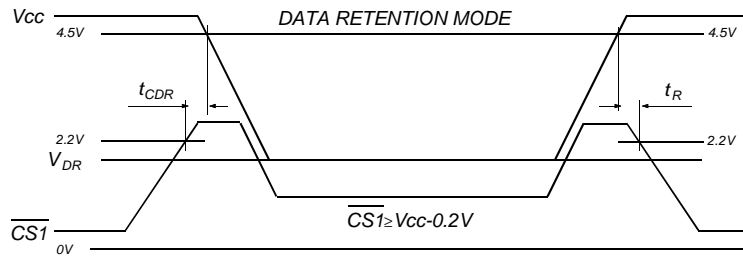
**Write Cycle No.1 Timing Waveform**



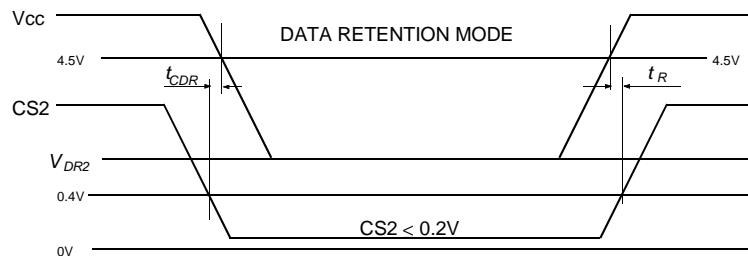
**Write Cycle No.2 Timing Waveform <sup>(5)</sup>**



### Low $V_{CC}$ Data Retention Timing Waveform 1 ( $\overline{CS1}$ controlled)



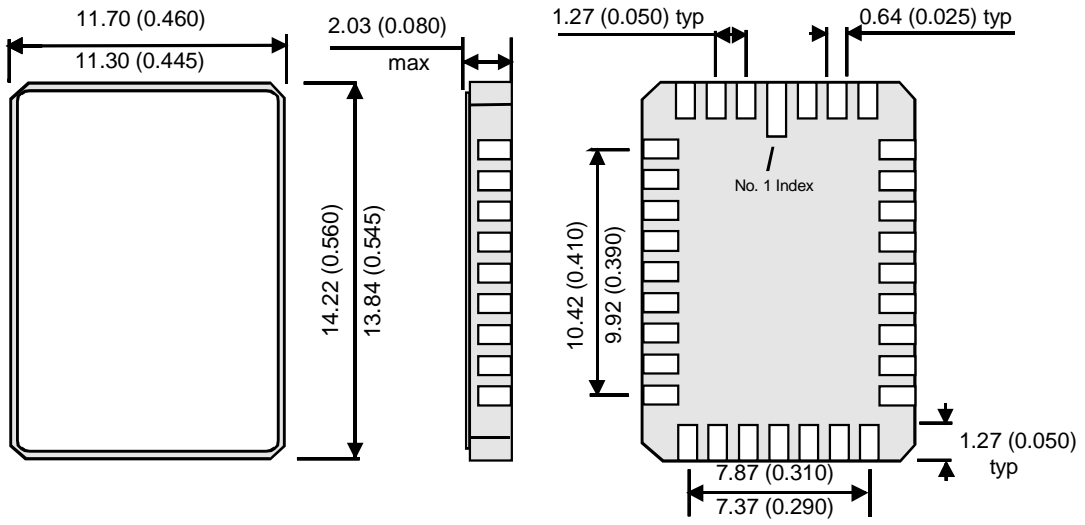
### Low $V_{CC}$ Data Retention Timing Waveform 2 (CS2 controlled)



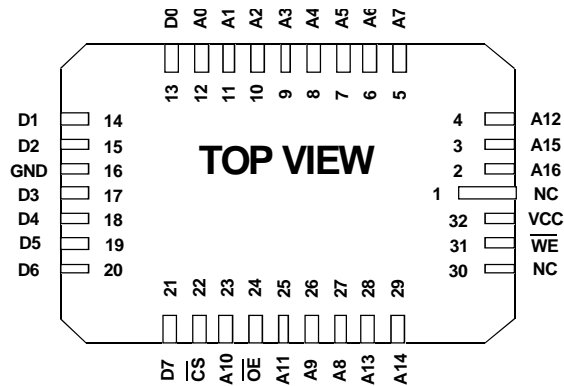
### AC Characteristics Notes

- (1) A write occurs during the overlap of a low  $\overline{CS1}$ , a high CS2 and a low  $\overline{WE}$ . A write begins at the latest transition among CS1 going low, CS2 going high and  $\overline{WE}$  going low. A write ends at the earliest transition among CS1 going high, CS2 going low and  $\overline{WE}$  going high.  $t_{WP}$  is measured from the beginning of write to the end of write.
- (2)  $t_{WR}$  is measured from the earlier of  $\overline{CS1}$  or  $\overline{WE}$  going high or CS2 going high to the end of write cycle.
- (3) During this period, I/O pins are in the output state. Input signals out of phase must not be applied.
- (4) If  $\overline{CS1}$  goes low simultaneously with  $\overline{WE}$  going low or after  $\overline{WE}$  going low, outputs remain in high impedance state.
- (5) OE is continuously low. ( $\overline{OE} = V_{IL}$ )
- (6) Dout is in the same phase as written data of this write cycle.
- (7) Dout is the read data of next address.
- (8) If  $\overline{CS1}$  is low and CS2 is high during this period, I/O pins are in the output state. Input signals out of phase must not be applied to I/O pins.
- (9)  $t_{WHZ}$  is defined as the time at which the outputs achieve the open circuit conditions and is not referenced to output voltage levels. These parameters are sampled and not 100% tested.

**32 pad LCC - 'W' Package**



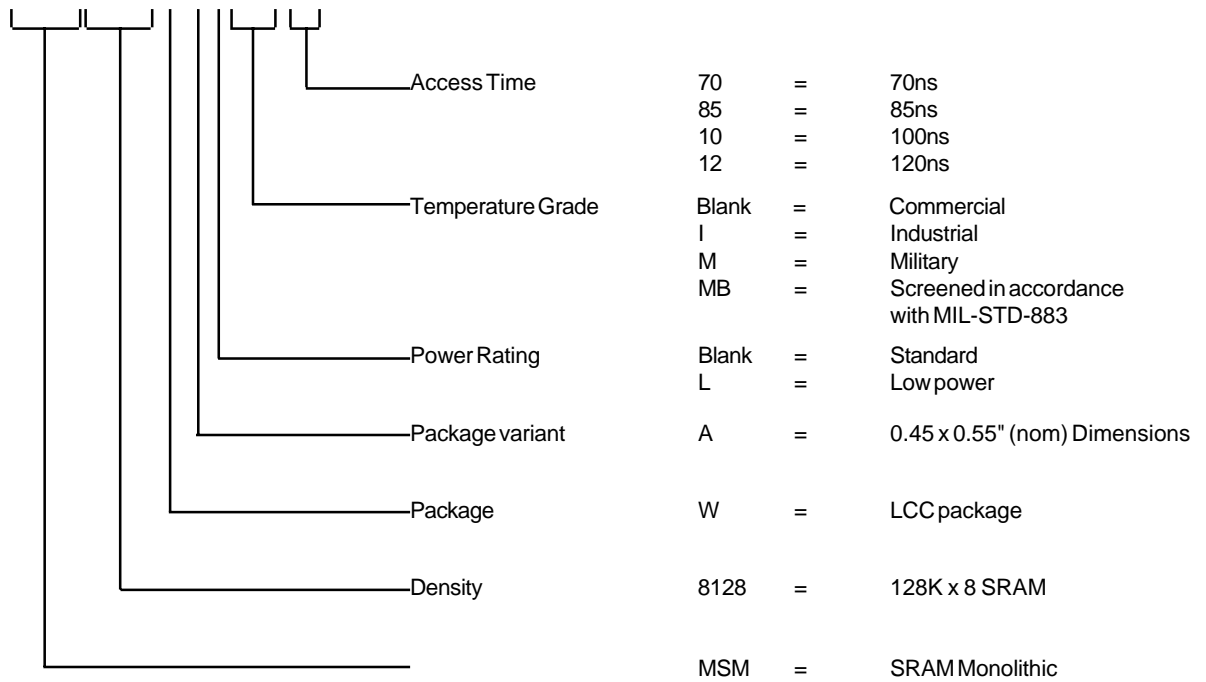
### Alternate Pin Definition - X variant



### Military Screening Procedure

Component Screening Flow for high reliability product is in accordance with Mil-883 method 5004

<b>MB COMPONENT SCREENING FLOW</b>		
<i>SCREEN</i>	<i>TEST METHOD</i>	<i>LEVEL</i>
<b>Visual and Mechanical</b> Internal visual Temperature cycle Constant acceleration Pre-Burn-in electrical Burn-in	2010 Condition B or manufacturers equivalent 1010 Condition C (10 Cycles, -65°C to +150°C) 2001 Condition E (Y, only) (30,000g) Per applicable device specifications at $T_A=+25^\circ\text{C}$ Method 1015, Condition D, $T_A=+125^\circ\text{C}$ , 160hrs min	100% 100% 100% 100% 100%
<b>Final Electrical Tests</b> Static (dc) Functional Switching (ac)	Per applicable Device Specification a) @ $T_A=+25^\circ\text{C}$ and power supply extremes b) @ temperature and power supply extremes a) @ $T_A=+25^\circ\text{C}$ and power supply extremes b) @ temperature and power supply extremes a) @ $T_A=+25^\circ\text{C}$ and power supply extremes b) @ temperature and power supply extremes	100% 100% 100% 100% 100%
<b>Percent Defective allowable (PDA)</b>	Calculated at post-burn-in at $T_A=+25^\circ\text{C}$	5%
<b>Hermeticity</b> Fine Gross	1014 Condition A Condition C	100% 100%
<b>External Visual</b>	2009 Per vendor or customer specification	100%

**MSM8128WALMB-85**

**THESE DEVICES ARE NOT RECOMMENDED FOR NEW DESIGNS AND MAY BE MADE OBSOLETE **WITHOUT NOTICE**....**

Although this data is believed to be accurate the information contained herein is not intended to and does not create any warranty of merchantability or fitness for a particular purpose.

Our products are subjected to a constant process of development. Data may be changed at any time without notice. Products are not authorised for use as critical components in life support devices without the express written approval of a company director.