1M x 32 FLASH MEMORY

PUMA 68FV32006/A - 90/12/15

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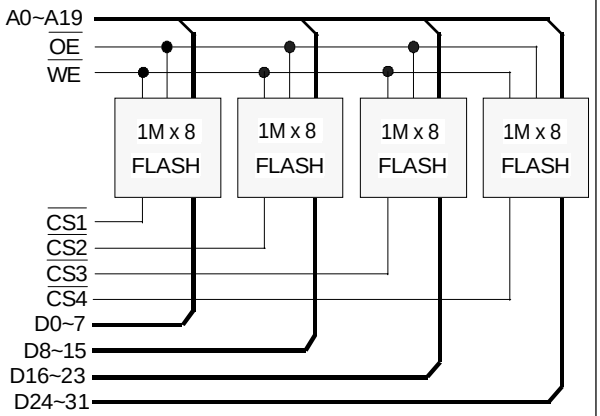
Description

The PUMA 68FV32006 is a high density 32Mbit CMOS 3.3V Only FLASH memory organised as 1M x 32 in a JEDEC 68 pin surface mount PLCC, with read access times of 90, 120, and 150ns. The plastic device is screened to ensure high reliability.
The output width is user configurable as 8 , 16 or 32 bits using four Chip Selects ($\overline{CS1}$~$\overline{4}$) for optimum application flexibility.
The device incorporates Embedded Algorithms for Program and Erase with Sector architecture (64K sector) and supports full chip erase.
The PUMA 68FV32006 also features hardware sector protection, which disables both program and erase operations in any of the 32 sectors on the device.

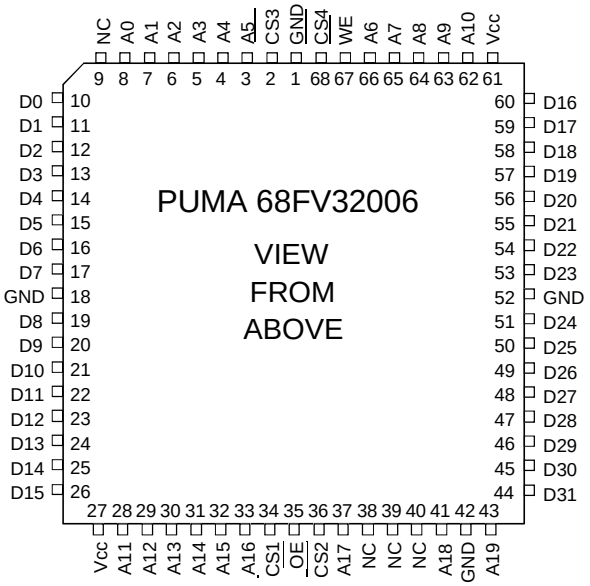
Features

- Fast Access Times of 90/120/150 ns.
- Output Configurable as 32 / 16 / 8 bit wide.
- Operating Power 660/330/165 mW (Max).
- Low Power Standby 1.1mA (Max).
- Industrial and Military (Restricted) grade parts.
- Automatic Write/Erase by Embedded Algorithm - end of Write/Erase indicated by DATA Polling and Toggle Bit.
- Flexible Sector Erase Architecture - 64K byte sector size, with hardware protection of any number of sectors.
- 3.3V operation, 3.3V program.
- Single Byte Program Time of 9µS (Typ).
- Sector Program Time of 1sec (Typ).
- Erase/Write Cycle Endurance 100,000 (Min).

Block Diagram (see page 20 for 'A' version)



Pin Definition (see page 20 for 'A' version)



Pin Functions

A0-A19	**Address Input**	**D0-D31**	**Data Inputs/Outputs**
$\overline{CS1}$-4	**Chip Enables**	**$\overline{WE}$**	**Write Enable**
$\overline{OE}$	**Output Enable**	**Vcc**	**Power (+3.3V)**
GND	**Ground**		

Absolute Maximum Ratings (1)

	Range	*unit*
Voltage on any pin w.r.t. Gnd	-0.5 to +Vcc+0.5	V
Supply Voltage (2)	-0.5 to +4.0	V
Voltage on A9, $\overline{OE}$, Reset w.r.t. Gnd (3)	-0.5 to +12.5	V
Storage Temperature	-65 to +150	℃

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operationof the device at those or any other conditions above those indicated in the operational sections of this specification is not implied.

(2) Minimum DC voltage on any input or I/O pin is -0.5V. Maximum DC voltage on output and I/O pins is Vcc+0.5V During transitions voltage may overshoot to Vcc +1.0V for periods of 10ns

(3) Minimum DC input voltage on A9,$\overline{OE}$, Reset is -0.5V during voltage transitions, A9,$\overline{OE}$, Reset may overshoot Vss to -1V for periods of up to 10ns, maximum DC input voltage on A9 is 12.5V which may overshoot to 14.0V for periods up to 10ns.

Recommended Operating Conditions

Parameter		*min*	*typ*	*max*	*unit*	
Supply Voltage	V_{CC}	3.0	3.3	3.6	V	
Input High Voltage	V_{IH}	$0.7V_{CC}$	-	V_{CC}+0.3	V	
Input Low Voltage	V_{IL}	-0.5	-	0.8	V	
Operating Temperature	T_A	0	-	70	℃	
	T_{AI}	-40	-	85	°C	(-I suffix)
	T_{AM}	-55	-	115	°C	(-M suffix)

DC Electrical Characteristic (T_A=-55°C to +115°C, Vcc=3.3V + 10%)

Parameter		*Symbol*	*Test Condition*	*min*	*typ*	*max*	*unit*
I/P Leakage CurrentAddress, $\overline{OE}$, $\overline{WE}$		I_{LI1}	V_{CC}=V_{CC} max, V_{IN}=0V or V_{CC}	-	-	±4	µA
A9 Input Leakage Current		I_{LI2}	V_{CC}=V_{CC} max, A9=12.5V	-	-	140	µA
Other Pins		I_{LI3}	V_{CC}=V_{CC} max, V_{IN}=0V or V_{CC}	-	-	±4	µA
Output Leakage Current		I_{LO}	V_{CC}=V_{CC} max, V_{OUT}=0V or V_{CC}	-	-	±4	µA
V_{CC} Read Current	32 bit	I_{CCO32}	$\overline{CS}$=V_{IL} (1), $\overline{OE}$=V_{IH}, I_{OUT}=0mA, *f*=5MHz	-	-	64	mA
	16 bit	I_{CCO16}	As above	-	-	32	mA
	8 bit	I_{CCO8}	As above	-	-	16	mA
V_{CC}Write Current	32 bit	I_{CCP32}	Programming in Progress	-	-	120	mA
	16 bit	I_{CCP16}	As above	-	-	60	mA
	8 bit	I_{CCP8}	As above	-	-	30	mA
Standby Supply Current		I_{SB1}	V_{CC}=V_{CC} max, $\overline{CS}$(1),Reset=V_{cc} + 0.3V	-	-	40	µA
Autoselect / Sector Unprotect Voltage		V_{ID}	V_{CC} = 3.3V	11.5	-	12.5	V
Output Low Voltage		V_{OL}	I_{OL}=4mA. V_{CC} = V_{CC} min.	-	-	0.45	V
Output High Voltage		V_{OH1}	I_{OH}=-2.0mA. V_{CC} = V_{CC} min.	0.85Vcc	-	-	V
Low V_{CC} Lock-Out Voltage		V_{LKO}		2.3	-	2.5	V

Notes (1) $\overline{CS}$ above are accessed through $\overline{CS1\text{-}4}$. These inputs must be operated simultaneously for 32 bit operation, in pairs in 16 bit mode and singly for 8 bit mode.

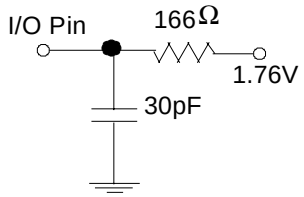
Capacitance (T_A=25°C,f=1MHz)

Parameter		*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance	Address, $\overline{OE}$, $\overline{WE}$	C_{IN1}	V_{IN}=0V	-	35	pF
	Other pins	C_{IN2}	V_{IN}=0V	-	10	pF
Output Capacitance	8 bit	C_{OUT8}	V_{OUT}=0V	-	52	pF

Note: These parameters are calculated, not measured.

AC Test Conditions

* Input pulse levels : 0.0V to 3.0V
* Input rise and fall times : 5 ns
* Input and output timing reference levels : 1.5V
* VCC = 3.3V +/- 10%
* Module tested in 32 bit mode



AC OPERATING CONDITIONS

Read Cycle

Parameter		90			120			150			
		min	typ	max	min	typ	max	min	typ	max	Unit
Read Cycle Time	t_{RC}	90	-	-	120	-	-	150	-	-	ns
Address to output delay	t_{ACC}	-	-	90	-	-	120	-	-	150	ns
Chip enable to output	t_{CE}	-	-	90	-	-	120	-	-	150	ns
Output enable to output	t_{OE}	-	-	40	-	-	50	-	-	55	ns
Output enable to output High Z	t_{DF}	-	-	30	-	-	35	-	-	40	ns
Output hold time from address	t_{OH}	0	-	-	0	-	-	0	-	-	ns
$\overline{CS}$ or $\overline{OE}$ whichever occurs first											

Write/Erase/Program

Parameter	Symbol	90			120			150			
		min	typ	max	min	typ	max	min	typ	max	unit
Write Cycle time (4)	t_{WC}	90	-	-	120	-	-	150	-	-	ns
Address Setup time	t_{AS}	0	-	-	0	-	-	0	-	-	ns
Address Hold time	t_{AH}	50	-	-	55	-	-	65	-	-	ns
Data Setup Time	t_{DS}	50	-	-	55	-	-	65	-	-	ns
Data hold Time	t_{DH}	0	-	-	0	-	-	0	-	-	ns
Output Enable Setup Time	t_{OES}	0	-	-	0	-	-	0	-	-	ns
Read Recover before Write	t_{GHWL}	0	-	-	0	-	-	0	-	-	ns
$\overline{CS}$ setup time	t_{CE}	0	-	-	0	-	-	0	-	-	ns
$\overline{CS}$ hold time	t_{CH}	0	-	-	0	-	-	0	-	-	ns
$\overline{WE}$ Pulse Width	t_{WP}	50	-	-	55	-	-	65	-	-	ns
$\overline{WE}$ Pulse Width High	t_{WPH}	30	-	-	30	-	-	35	-	-	ns
Programming operation	t_{WHWH1}	-	9	-	-	9	-	-	9	-	µs
Sector Erase operation (1)	t_{WHWH2}	-	1	-	-	1	-	-	1	-	sec
V_{CC} setup time (4)	t_{VCS}	50	-	-	50	-	-	50	-	-	µs

Notes: (1) This does not include the preprogramming time.
(2) Not 100% tested.Under Development.

Under Development.

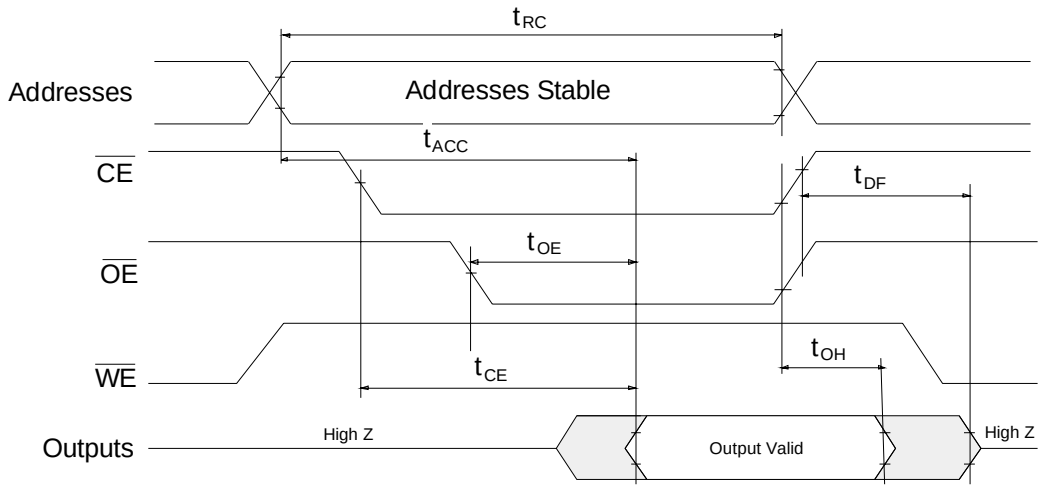
Write/Erase/Program Alternate $\overline{CS}$ controlled Writes

		90			120			150			
Parameter	Symbol	min	typ	max	min	typ	max	min	typ	max	Unit
Write Cycle time (2)	t_{WC}	90	-	-	120	-	-	150	-	-	ns
Address Setup time	t_{AS}	0	-	-	0	-	-	0	-	-	ns
Address Hold time	t_{AH}	50	-	-	55	-	-	65	-	-	ns
Data Setup Time	t_{DS}	50	-	-	55	-	-	65	-	-	ns
Data hold Time	t_{DH}	0	-	-	0	-	-	0	-	-	ns
Output Enable Setup Time	t_{OES}	0	-	-	0	-	-	0	-	-	ns
Read Recover before Write	t_{GHEL}	0	-	-	0	-	-	0	-	-	ns
$\overline{WE}$ setup time	t_{WS}	0	-	-	0	-	-	0	-	-	ns
$\overline{WE}$ hold time	t_{WH}	0	-	-	0	-	-	0	-	-	ns
$\overline{CS}$ Pulse Width	t_{CP}	50	-	-	55	-	-	65	-	-	ns
$\overline{CS}$ Pulse Width High	t_{CPH}	30	-	-	30	-	-	35	-	-	ns
Programming operation	t_{WHWH1}	-	9	-	-	9	-	-	9	-	us
Sector Erase operation (1)	t_{WHWH2}	-	1	-	-	1	-	-	1	-	sec

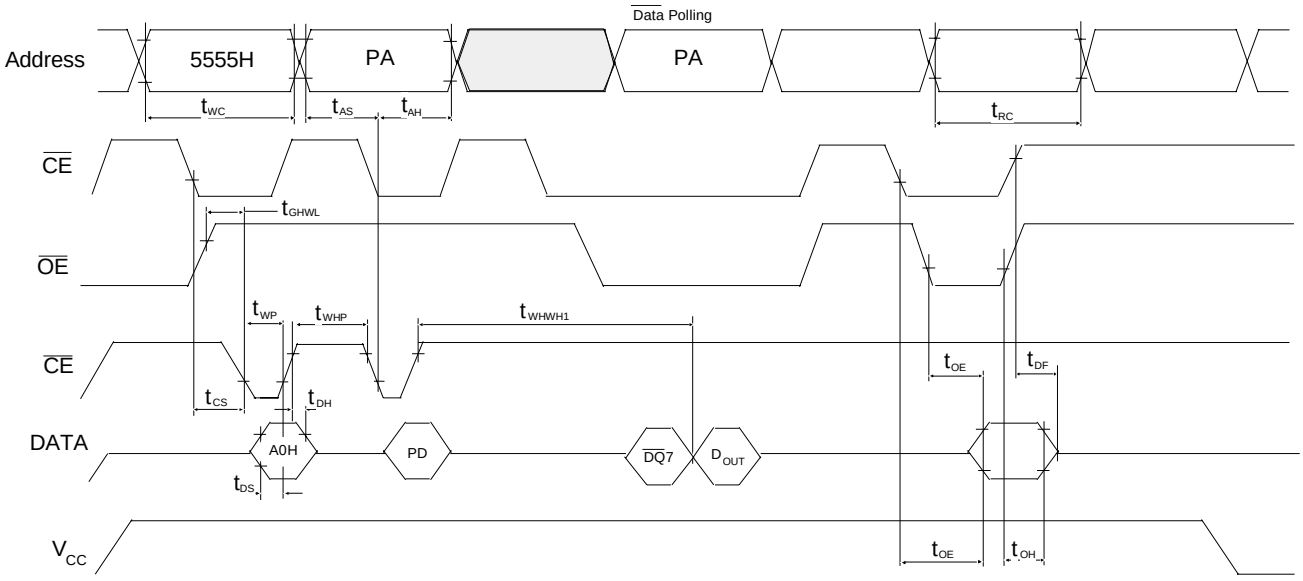
Note: (1) Does not include pre-programming time.
(2) Not 100% tested.

Under Development.

AC Waveforms for Read Operation



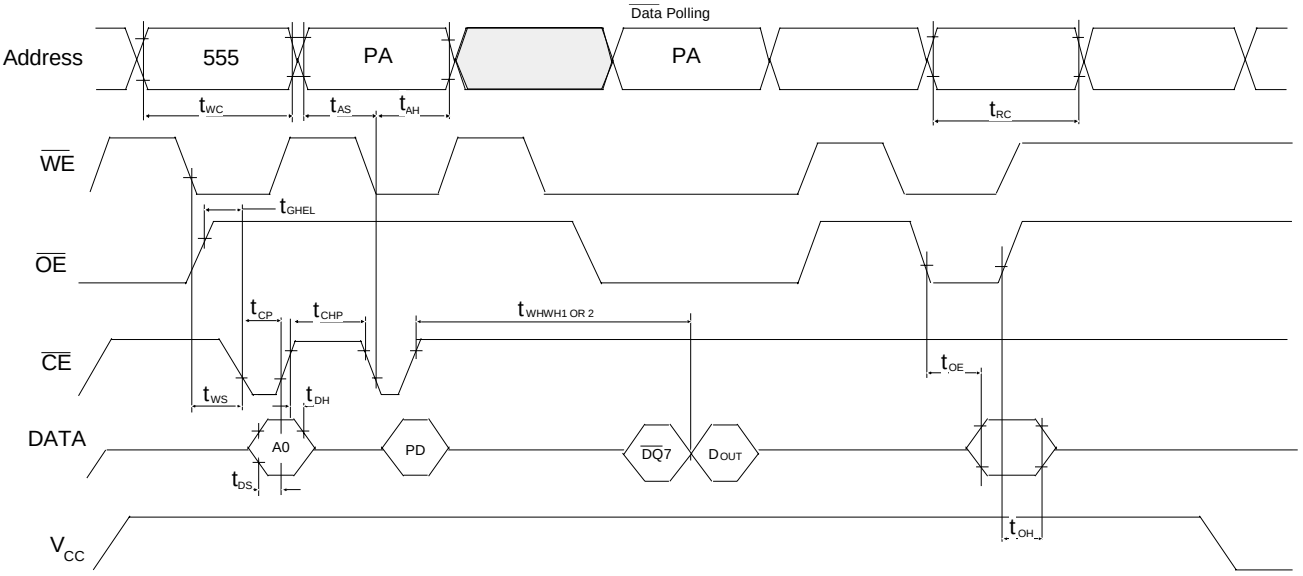
AC Waveforms Program



Notes:

1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. DQ7 is the out put of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

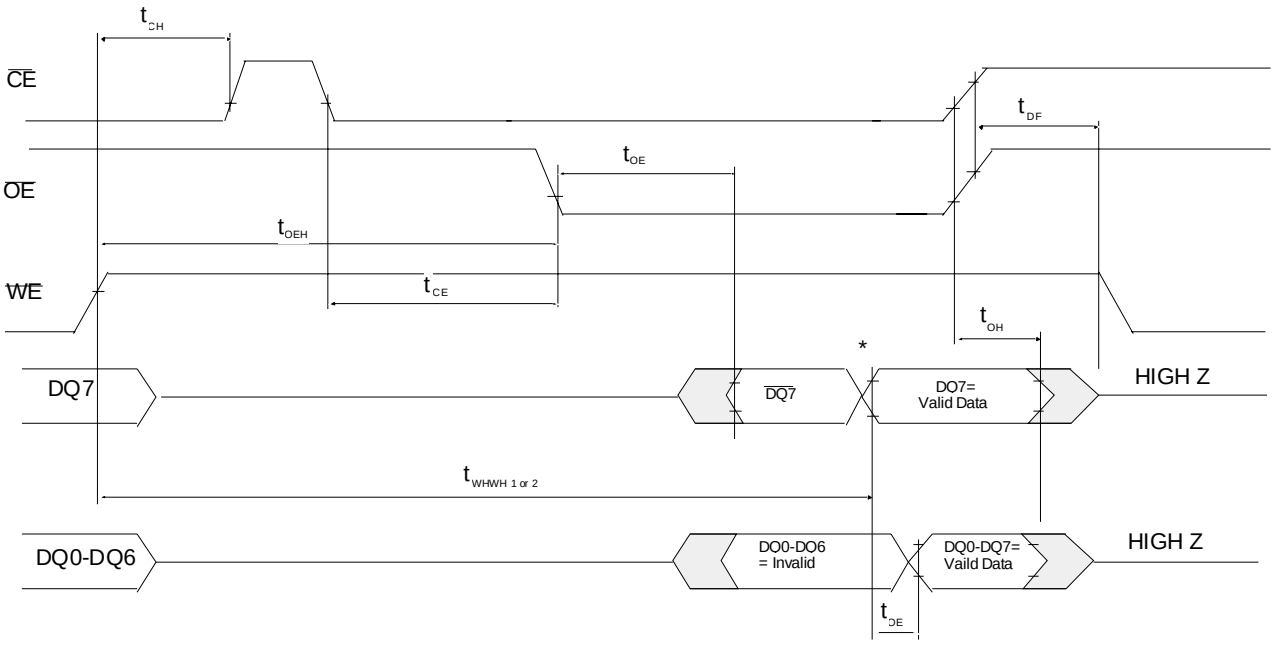
A.C Waveforms - Alternate $\overline{CS}$ controlled Program operation timings



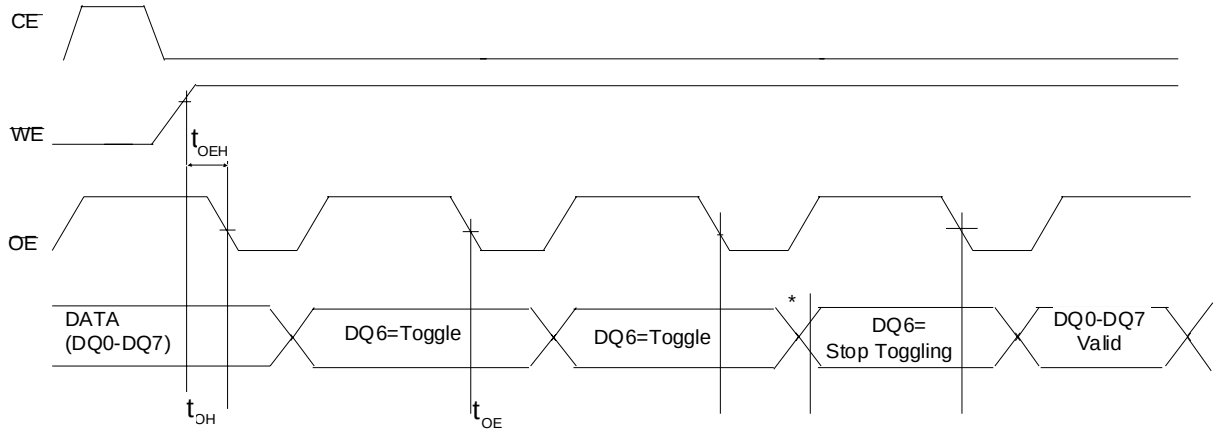
NOTES:

1. PA is address of memory location to be programmed.
2. PD is data to be programmed at byte address.
3. DQ7 is the output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

AC Waveforms for Data Polling During Embedded Algorithm Operations

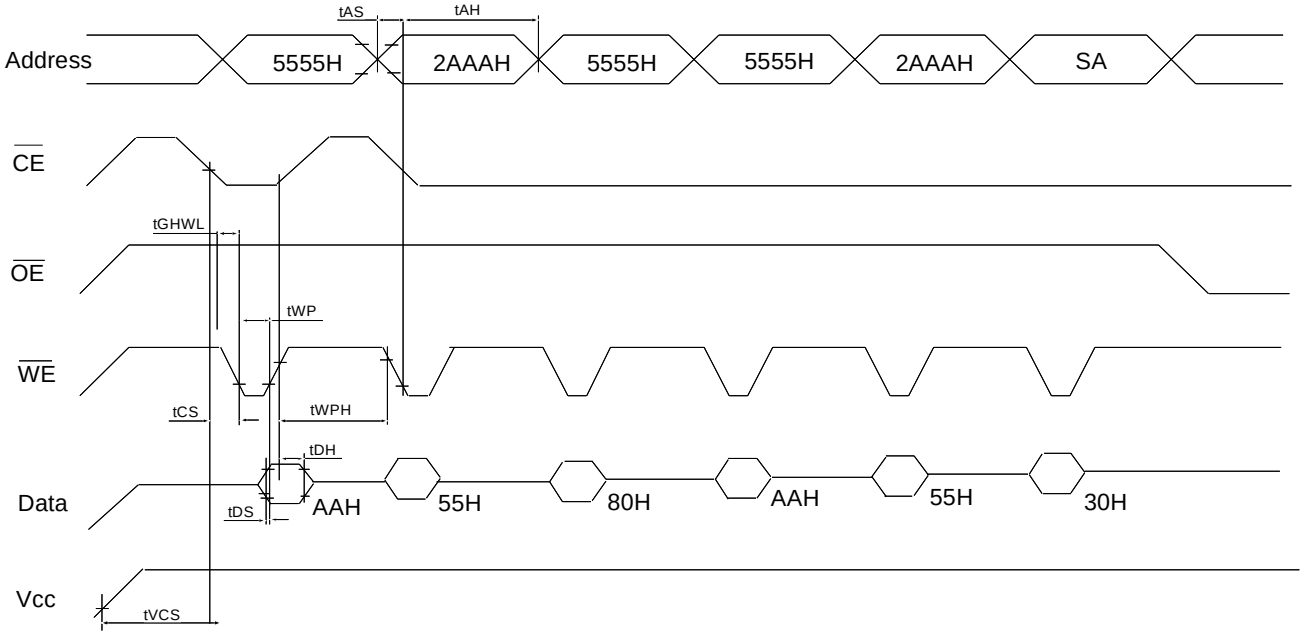


AC Waveforms for Toggle Bit During Embedded Algorithm Operations



* DQ6 stops toggling (the device has completed the embedded operations)

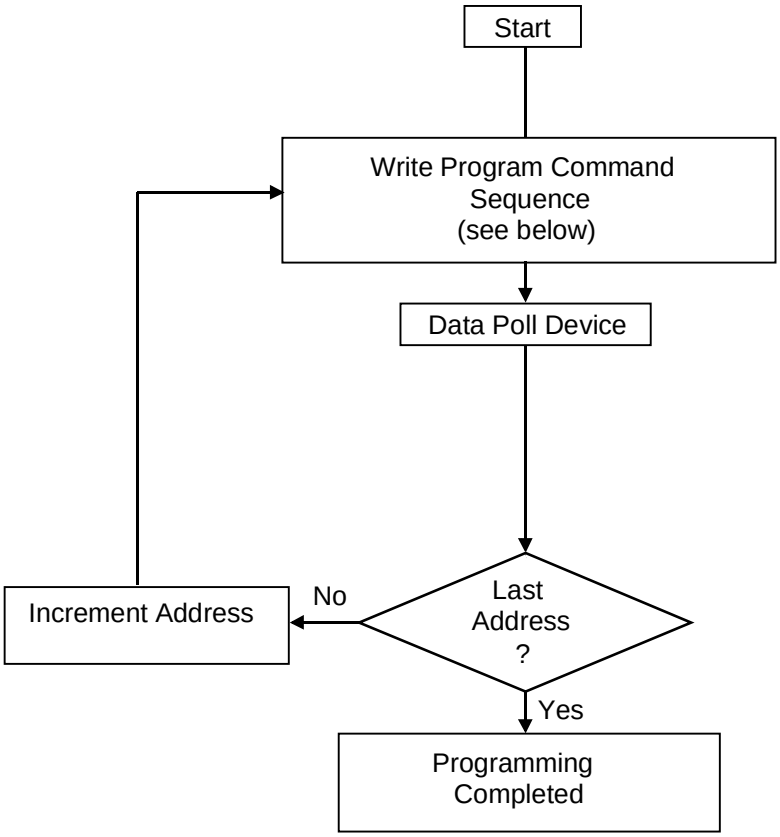
AC Waveforms Chip / Sector Erase



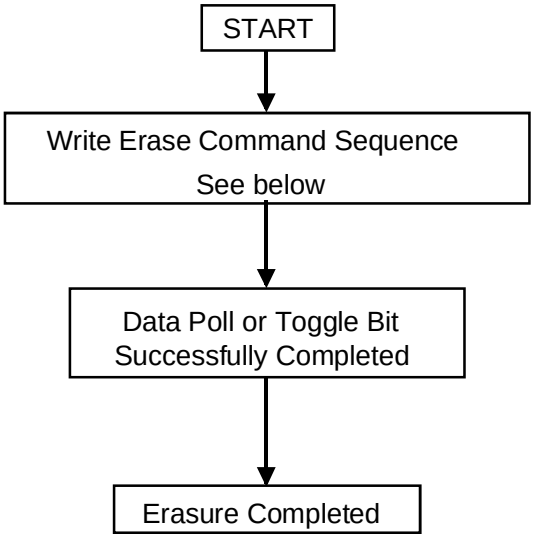
NOTES:

1. SA is the address for sector erase. Addresses = don't care for Chip Erase.

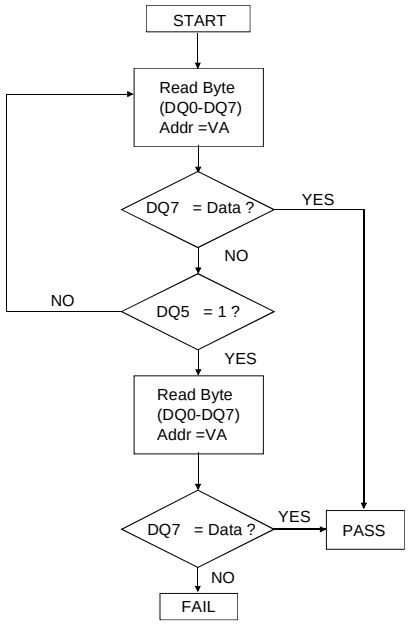
EMBEDDED PROGRAMMING ALGORITHM



EMBEDDED ERASE ALGORITHM

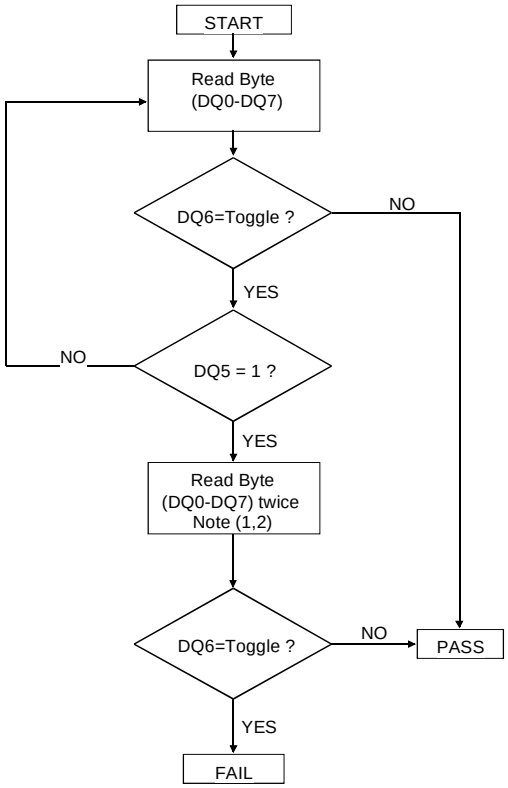


DATA POLLING ALGORITHM



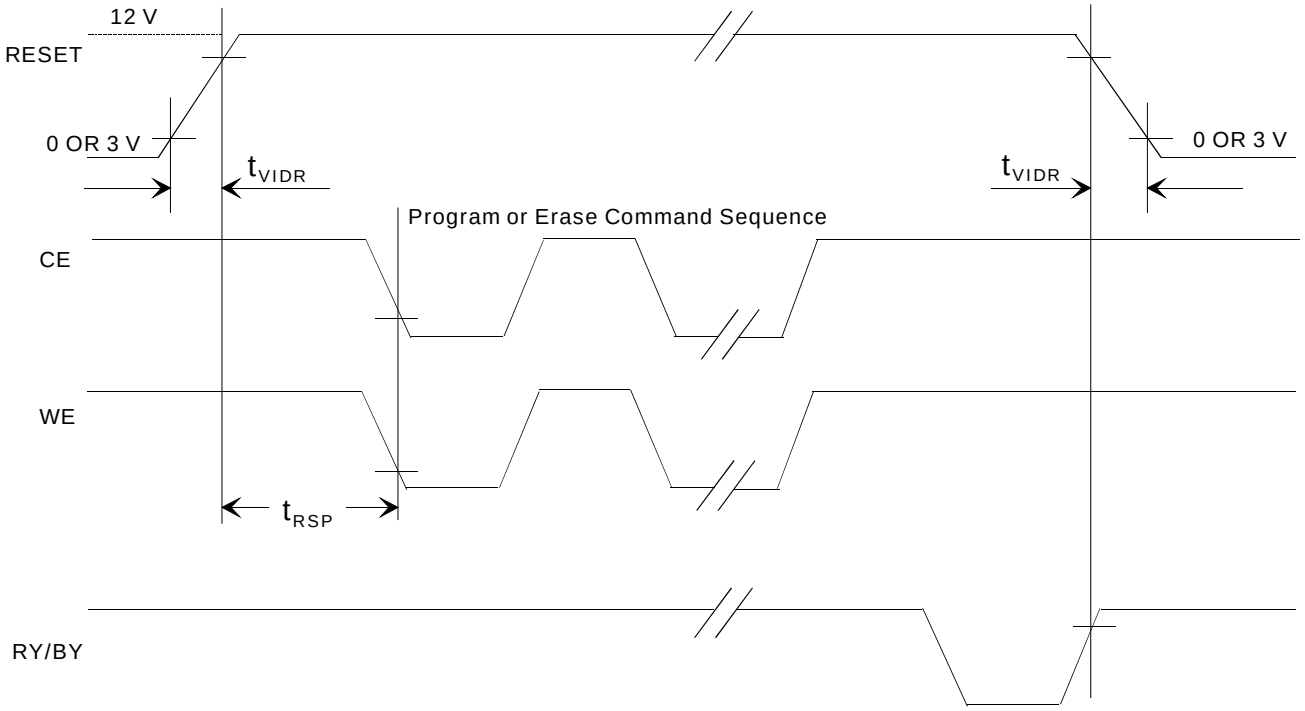
NOTE:
1. DQ7 is rechecked even if DQ5 = 1 because DQ7 may change simultaneously with DQ5.
2. VA = Byte address for programming.
   = Any of the sector addresses within the sector being erased during sector erase operation
   = XXXXXH during chip erase

TOGGLE BIT ALGORITHM



NOTES:
1. DQ6 is rechecked even if DQ5 = 1 because DQ6 may stop toggling at the same time as DQ5 changing to "1".
2 Read toggle bit twice to determin wether or not it is toggling.

TEMPORARY SECTOR UNPROTECT WAVEFORM



DEVICE OPERATION

The following description deals with the device operating in 8 bit mode accessed through $\overline{CS1}$, however status flag definitions shown apply equally to the corresponding flag for each device in the module.

Read Mode

The device has two control functions which must be satisfied in order to obtain data at the outputs
$\overline{CS1}$-4 is the power control and should be used for device selection
$\overline{OE}$ is the output control and should be used to gate data to the output pins if the device is selected.

Standby Mode

Two standby modes are available :
CMOS standby : $\overline{CS1}$-4 held at Vcc +/- 0.3V
TTL standby : $\overline{CS1}$-4 held at V_{IH}
In the standby mode the outputs are in a high impedance state independent of the $\overline{OE}$ input. If the device is deselected during erasure or programming the device will draw active current until the operation is completed.

Output Disable

With the $\overline{OE}$ input at a logic high level (V_{IH}), output from the device is disabled. This will cause the output pins to be in a high impedance state.

Autoselect

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ7 - DQ0. This mode is primarily intended for programing equipment to automaticly match a device to be programed with its corresponding programing algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} (11.5V to 12.5V) on address pin A9. Address pins A6, A1 and A0 must be as shown in the table below. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits. The table below shows the remaining address bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ7 - DQ0.

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in command definitions table. This method does not require V_{ID}.

Description	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A19 TO A13	A12 TO A10	A9	A8 TO A7	A6	A5 TO A2	A1	A0	DQ7 TO DQ0
Sector Protection Verification	L	L	H	SA	X	V_{ID}	X	L	X	H	L	01H (PROTECTED)
												00H (UNPROTECTED)

L = Logic Low = $V_{IL,}$ H = Logic High = VIH, SA = Sector Address, X = Don't care

Write

Device erasure and programming are accomplished via the command register. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. The register is a latch used to store the commands along with the address and data information required to execute the command. The command register is written by bringing $\overline{WE}$/$\overline{WE1}$-4 to V_{IL} while $\overline{CS1}$-4 is at V_{IL} and $\overline{OE}$ is at V_{IH}.Addresses are latched on the falling edge of $\overline{WE}$/$\overline{WE1}$-4 while data is latched on the rising edge.

COMMAND DEFINITIONS

Command Sequence	Bus Write Cycles Req'd	Bus Cycles (Notes 2-4)											
		First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 5)	1	RA	RD										
Reset	1	XXX	FO										
Autoselect (Note 7)	4	XXX	AA	XXX	55	XXX	90	(SA)	00				
Sector Protect Verify (Note 8)		XXX		XXX		XXX		X02	01				
Program	4	XXX	AA	XXX	55	XXX	A0	PA	PD				
Chip Erase	6	XXX	AA	XXX	55	XXX	80	XXX	AA	XXX	55	XXX	10
Sector Erase	6	XXX	AA	XXX	55	XXX	80	XXX	AA	XXX	55	SA	30
Sector Erase Suspend (Note 9)	1	Erase can be suspended during sector erase with Addr (don't care) Data (B0)											
Sector Erase Resume (Note 10)	1	Erase can be resumed after suspend with Addr (Don't Care), Data (30)											

NOTES:

2. All values are in hexadecimal.
3. Except when reading array or autoselect data, all bus cycles are write operations.
4. All address bits are don't cares for unlock and command cycles, except when SA or PA required.
5. No unlock or command cycles required when reading array data.
6. The reset command is required to return to reading array data when device is in the autoselect mode, or if DQ5 goes high (while device is providing status data.
7. The fourth cycle of the autoselect command sequence is a read cycle.
8. The data is 00h for an unprotected sector and 01h for a protected sector.
9. The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.
10. The Erase Resume command is valid only during the Erase Suspend mode.

Read / Reset Command

The read or reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The device remains enabled for reads until the command register contents are altered.

The device will automatically power-up in the read/reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of memory content occurs during the power transition. Refer to the AC Read

Characteristics and Waveforms for specific timing parameters.

Sector Unprotect

Sectors which have previously been protected from being programmed or erased may be unprotected using the Sector Unprotect Algorithm. All sectors must be placed in the protection mode using the protection algorithm before unprotection can proceed.

A special high voltage for unprotection V_{SP} is defined to be 12V+/-0.5V.

The unprotection mode is entered by setting $\overline{OE}$ to V_{ID} or V_{SP}, $\overline{WE}$ to V_{SP}, A5 to V_{IH} and A0=A9 to V_{IL}. Unprotect is invoked by applying to negative pulses on $\overline{CS}$ for a period of t_{WPP2}.

Sector Protection

The device features hardware sector protection. This feature will disable both program and erase operations in any sector. The sector protect feature is enabled using programming equipment at the users site. The device is shipped with all sectors unprotected.

To activate this mode, the programming equipment must force V_{ID} on address pin A_9 and control pin $\overline{OE}$, and $\overline{CS}=V_{IH.}$ The sector adresses (A19, A18, A17 and A16) should be set to the sector to be protected. Programming of the protection circuitry begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same. Sector addresses must be held constant during the $\overline{WE}$ pulse.

To verify programming of the protection equipment circuitry, the programming equipment must force V_{ID} on address pin A9 with $\overline{CE}$ and $\overline{OE}$ at V_{IL} and $\overline{WE}$ at V_{IH}. Reading the device at a particular sector address (A16, A17, A18 and A19) while (A6,A1,A0) = (0,1,0) will produce 01H at data output D0 for a protected sector. Otherwise the device will read 00H for unprotected sector. In this mode, the lower order addresses, except for A0, A_1 and A6 , are don't care. Address with $A1=V_{IL}$ are reserved for autoselect codes.

It is also possible to determine if a sector is protected in the system by writing the autoselect command. Performing a read operation at XX02H , where the higher order addresses (A16, A17, A18 and A19) are sector addresses,(other addresses are a don't care) will produce 01H data if those sectors are protected. Otherwise the devidce will read 00H for an unprotected sector.

Sector Address Table

	A19	A18	A17	A16	Address Range
SA0	0	0	0	0	00000h-0FFFFh
SA1	0	0	0	1	10000h-1FFFFh
SA2	0	0	1	0	20000h-2FFFFh
SA3	0	0	1	1	30000h-3FFFFh
SA4	0	1	0	0	40000h-4FFFFh
SA5	0	1	0	1	50000h-5FFFFh
SA6	0	1	1	0	60000h-6FFFFh
SA7	0	1	1	1	70000h-7FFFFh
SA8	1	0	0	0	80000h-8FFFFh
SA9	1	0	0	1	90000h9FFFFh
SA10	1	0	1	0	A0000h-AFFFFh
SA11	1	0	1	1	B0000h-BFFFFh
SA12	1	1	0	0	C0000h-CFFFFh
SA13	1	1	0	1	D0000h-DFFFFh
SA14	1	1	1	0	E0000h-EFFFFh
SA15	1	1	1	1	F0000h-FFFFFh

Autoselect Command

The Autoselect command sequence allows the host system to access the manufacturer and devices codes, and determine whether or not a sector is protected. See Command definitions table. This method is an alternative to that shown in the autoselect codes table, which is intended for PROM programmers and requires V_{ID} on address bit A9.

The autoselect command sequence is initiated by writing two unlock cycles, followed by the autoselect command. The device then enters the autoselect mode, and the system may read at any address any number of times, without initiating another command sequence.

A read cycle containing a sector address (SA) and the address 02h in it, returns 01h if that sector is protected, or 00h if it is unprotected. Refer to sector address table for valid sector address.

The system must write the reset command to exit the autoselect mode and return to reading array data.

Byte Programming

Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are writen next, which in turn initiate the Embeded Program Algorithm. The system is not required to provide further controls or timings. The device automaticlly provides internally generated program pulses and verify the programmed cell margin. Command definitions table shows the address and data requirements for the byte program command sequence.

When the Embedded Program algorithm is complete, the device then returns to reading array data and addresses are no longer latched. The system can determine the status of the program operation by using DQ7 or DQ6. See "Write Operation Status" for information on these status bits.

Any commands writen to the device during the Embedded Program Algorithm are ignored. Note that a hardware reset immediatly terminates the programming opperation. The program command sequence should be reinitiated once the device has reset to reading data, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. A bit cannot from a "0" back to a "1". Attempting to do so may halt the opperation and set DQ5 to "1", or cause the data Polling Algorithm to indicate the opperation was sucessful. However, a succeeding read will show that the data is still "0". Only erase operations can convert a "0" to a "1".

Chip Erase

Chip erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the chip erase command.
Chip erase doesn't require the user to program the device prior to erase. Upon executing the Embedded Erase Algorithm command sequence the device automatically will program and verify the entire memory for an all zero data pattern prior to electrical erase. The systems is not required to provide any controls or timings during these operations.

Any commands written to the chip during the Embeded Erase algorithm are ignored. Note that a hardware reset during the chip erase operation immediately terminates the operation. The chip Erase Command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

The system can determine the status of the erase operation by using DQ7, DQ6 or DQ2. See "Write Operation Status" for information on these status bits. When the Embeded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched.

Sector Erase

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the address of the sector to be erased, and the sector erase command. The command definitions table shows the addresses and data requirements for the sector erase command sequence.

The device does not require the system to preprogram the memory prior to erase. The Embeded Erase Algorithm automaticlly programs and verifies the sector for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of 50ms begins. During the time-out period, additional sector addresses and sector erase commands may be writen. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50ms, otherwise the last address and command might not be accepted, and erasure may begin. It is recommended that the processor interrupts be disabled during this time to ensure all commands are accepted. The interupts can be re-enabled after the last Sector Erase command is writen. If the time between additional sector erase commands can be assumed to be less than 50ms, the system need not monitor DQ3. **Any command other than Sector Erase Suspend during the time-out period resets the device to reading array data**. The system must rewrite the command sequence and any additional sector addresses and commands.

The system can monitor DQ3 to determine if the sector erase timer has timed out. The time-out begins from the rising edge of the final $\overline{WE}$ pulse in the command sequence.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. Note that a hardware reset during the sector erase operation immediately terminates the operation. The Sector Erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

When the Embeded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6 or DQ2.

Erase Suspend

The Erase Suspend Command allows the system to interupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation, including the 50µs time out period during the sector erase command sequence. The Erase Suspend Command is ignored if written during the chip erase operation or Embeded Program algorithm. Writing the Erase Suspend command during the sector erase time-out immediately terminates the time-out period and suspends the erase operation. Addresses are "don't-cares" when writing the Erase Suspend command.

When the Erase Suspend command is written during a sector erase operation, the device requires a maximum of 20µs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation has been suspended, the system can read array data from or program data to any sector not selected for erasure. (The device "erase suspends" all sectors selected for erasure.) Normal read and write timings and command definitions apply. Reading at any address within erase-suspended sectors produces status data on DQ7-DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase suspended.

After an erase-suspended program operation is complete, the system can once again read array data within non-suspended sectors. The system can determine the status of the program operation.

The system may also write the autoselect command sequence when the device is in the Erase Suspend mode. The device allows reading autoselect codes even at addresses within erasing sectors, since the codes are not stored in the memory array. When the device exits the autoselect mode, the device reverts to the Erase Suspend mode, and is ready for another valid operation.

The system must write the Erase Resume command (address bits are "don't care") to exit the erase suspend mode and continue the sector erase operation. Further writes of the resume command are ignored. Another Erase Suspend command can be writen after the device has resumed erasing.

WRITE OPERATIONS STATUS

Operation		DQ7[2]	DQ6	DQ5[1]	DQ3	DQ2[2]
Standard Mode	Embedded Program Algorithm	DQ7	Toggle	0	N/A	No Toggle
	Embedded Erase Algorithm	0	Toggle	0	1	Toggle
Erase Suspend Mode	Reading within Erase Suspended Sector	1	No Toggle	0	N/A	Toggle
	Reading within Non-Erase Suspended Sector	Data	Data	Data	Data	Data
	Erase Suspend Program	DQ7	Toggle	0	N/A	N/A

Notes:
1. DQ5 switches to '1' when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits.
2. DQ7 and DQ2 require a valid address when reading status information.

D7 Data Polling

The device features Data Polling as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During the Embedded Programming Algorithm, an attempt to read the device will produce complement data of the data last written to D7. Upon completion of the Embedded Programming Algorithm an attempt to read the device will produce the true data last written to D7. Data Polling is valid after the rising edge of the forth $\overline{WE}$ pulse in the four write pulse sequence.

During the Embedded Erase Algorithm, D7 will be "0" until the erase operation is completed. Upon completion the data at D7 is "1". For chip erase, the Data Polling is valid after the rising edge of the sixth $\overline{WE}$ pulse in the six write pulse sequence. For sector erase, Data Polling is valid after the last rising edge of the sector erase $\overline{WE}$ pulse.

The Data Polling feature is only active during the Embedded Programming Algorithm, Embedded Erase Algorithm, or sector erase time-out.

D_6 Toggle Bit

The device also features the "toggle bit" as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During an Embedded Program or Erase Algorithm cycle, successive attempts to read data from the device will result in D6 toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, D6 will stop toggling and valid data will be read on successive attempts. During programming, the Toggle bit is valid after the rising edge of the forth $\overline{WE}$ pulse in the four write command pulse sequence. For chip erase, the Toggle bit is valid after the last rising edge of the sector erase $\overline{WE}$ pulse. The Toggle Bit is active during the sector time-out.

D_5 Exceeding Time Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. under these conditions DQ5 produces a "1." This is a failure condition that indicates the program or erase cycle was not successfully completed.

The DQ5 failure condition may appear if the system tries to program a "1" to a location that is previously programmed to "0." **Only an erase operation can change a "0" back to a "1"**. Under this condition, the device halts the operation, and when the operation has exceeded the timing limits, DQ5 produces a "1."

Under both these conditions, the system must issue the reset command to return the device to reading array data.

D_3 Sector Erase Timer

After the completion of the initial sector erase command sequence the sector erase time-out will begin. D3 will remain low until the time-out is complete. Data Polling and Toggle Bit are valid after the initial sector erase command sequence.

If Data Polling or the Toggle Bit indicates the device has been written with a valid erase command, D3 may be used to determine if the sector erase timer window is still open. If D3 is high the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by Data Polling or Toggle Bit. If D3 is low , the device will accept additional sector erase commands. To insure the command has been accepted, the software should check the status of D3 prior to and following each subsequent sector erase command. If D3 were high on the second status check, the command may not have been accepted.

DATA PROTECTION

The device is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transition. During power up the device automatically resets the internal state machine in the Read mode. Also, with its controls register architecture , alteration of the memory contents only occurs after successful completion of specific multi-bus cycle command sequences. The device also incorporates several features to prevent inadvertent write cycles resulting from Vcc power up and power down transitions or system noise.

Low V_{CC} Write Inhibit

When Vcc is less than V_{LKO}, the device does not accept any write cycles. This protects data during Vcc power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets. Subsequent writes are ignored untill Vcc is greater than $V_{LKO.}$ The system must provide the proper signals to the control pins to prevent unintentional writes when Vcc is greater than V_{LKO}.

Write Pulse "Glitch" Protection

Noise pulses of less than 5ns (typical) on $\overline{OE}$, $\overline{CS}$, $\overline{WE}$ will not initiate a write cycle

Logical Inhibit

Writing is inhibited by holding any one of $\overline{OE}=V_{IL}$, $\overline{CS}=V_{IH}$ or $\overline{WE}=V_{IH}$. To initiate a write cycle $\overline{CS}$ and $\overline{WE}$ must be logical zero while $\overline{OE}$ is a logical one.

Power Up Write Inhibit

Power-up of the device with $\overline{WE}=\overline{CS}=V_{IL}$ and $\overline{OE}=V_{IH}$ will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to the read mode on power-up.

Sector Protect

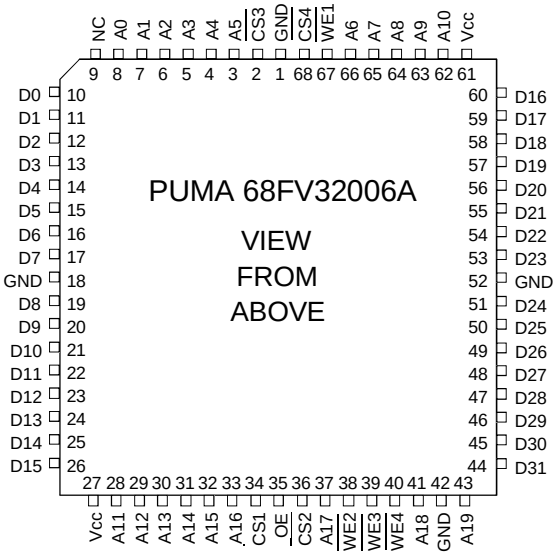
Sectors of the device may be hardware protected at the users factory. The protection circuitry will disable both program and erase functions for the protected sector(s). Requests to program or erase a protected sector will be ignored by the device.

ERASE AND PROGRAMMING PERFORMANCE

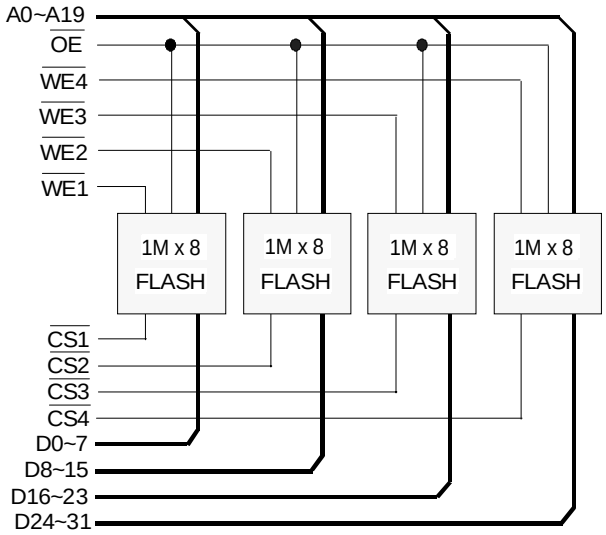
Parameter	Limits			Unit	Comments
	Min	Typ(1)	Max(2)		
Sector Erase Time		1	15	sec	Excludes 00H programming prior to erasure
Byte Programming Time		9	300	us	Excludes System level Overhead
Chip Programming Time		9	27	sec	Excludes System level Overhead
Erase/Program Time	100,000	1,000,000		cycles	10,000 Min.
Chip Erase Time		16		sec	

Notes : (1) 25°C, 3V V_{CC}, 100,000 cycles.
(2) Under work conditions 0f 90°C, V_{CC} 2.7V, 100,000 Cycles

Version 'A' Pin Definition

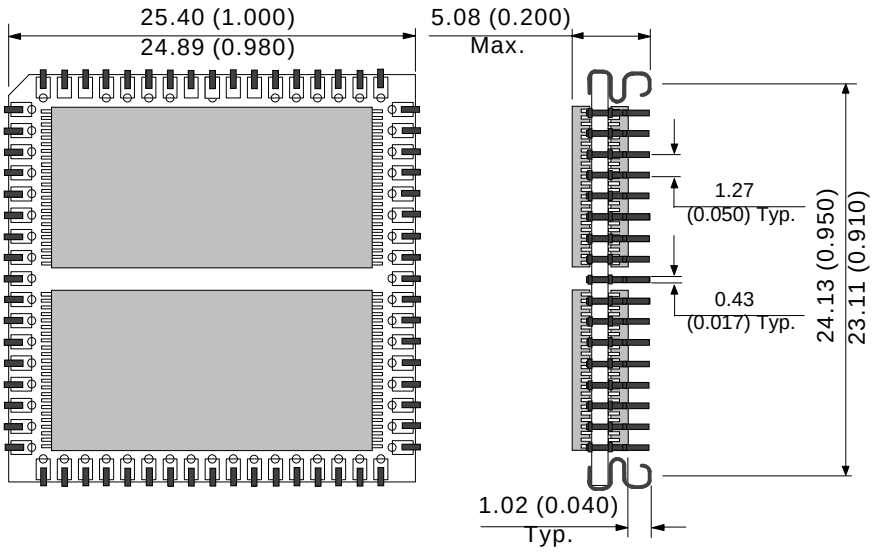


Version 'A' Block Diagram



Package Details

68 'J' Leaded Surface Mount Hi-Rel Plastic Package



Ordering Information

PUMA 68FV32006AM-90

Speed	90 = 90 ns 12 = 120 ns 15 = 150 ns
Temp. range/screening	Blank = Commercial Temperature I = Industrial Temperature M = Military Temperature (Restricted)
$\overline{WE}$ Option	Blank = Single $\overline{WE}$ A = $\overline{WE1}$~$\overline{WE4}$
Organisation	32006 = 1M x 32, user confiurable as 2M x 16 and 4M x 8
Technology	FV = FLASH MEMORY (3.3V Operation)
Package Type	PUMA 68= 68 pin "J" Leaded PLCC

Note :
Although this data is believed to be accurate the information contained herein is not intended to and does not create any warranty of merchantibility or fitness for aparticular purpose.
Our products are subject to a constant process of development. Data may be changed without notice.
Products are not authorised for use as critical components in life support devices without the express written approval of a company director.

Visual Inspection Standard

All devices inspected to ANSI/J-STD-001B Class 2 standard

Moisture Sensitivity

Devices are **moisture sensitive.**

Shelf Life in Sealed Bag 12 months at <40^{O}C and <90% relative humidity (RH).

After this bag has been opened, devices that will be subjected to infrared reflow, vapour phase reflow, or equivalent processing (peak package body temp 220^{O}C) **must be** :

A : Mounted within 72 Hours at factory conditions of <30^{O}C/60% RH

OR

B : Stored at <20% RH

If these conditions are not met or indicator card is >20% when read at 23^{O}C +/-5% devices **require baking** as specified below.

If baking is required, devices may be baked for :-

A : 24 hours at 125^{O}C +/-5% for high temperature device containers

OR

B : 192 hours at 40^{O}C +5^{O}C/-0^{O}C and <5% RH for low temperature device containers**.**

Packaging Standard

Devices packaged in dry nitrogen, JED-STD-020.

Packaged in trays as standard.

Tape and reel available for shipment quantities exceeding 200pcs upon request.

Soldering Recomendations

IR/Convection -	Ramp Rate	6^{O}C/sec max.
	Temp. exceeding 183^{O}C	150 secs. max.
	Peak Temperature	225^{O}C
	Time within 5^{O}C of peak	20 secs max.
	Ramp down	6^{O}C/sec max.
Vapour Phase -	Ramp up rate	6^{O}C/sec max.
	Peak Temperature	215 - 219^{O}C
	Time within 5^{O}C of peak	60 secs max.
	Ramp down	6^{O}C/sec max.

The above conditions must not be exceeded.

Note : The above recommendations are based on standard industry practice. Failure to comply with the above recommendations invalidates product warranty.