



**DC OPERATING CONDITIONS****Absolute Maximum Ratings** <sup>(1)</sup>

|  |           |                      |    |
|--|-----------|----------------------|----|
| Operating Temperature                                    | $T_{OPR}$ | -55 to +125          | °C |
| Storage Temperature                                      | $T_{STG}$ | -65 to +150          | °C |
| Input voltages (including N.C. pins) with Respect to GND | $V_{IN}$  | -0.6 to +6.25        | V  |
| Output voltages with respect to GND                      | $V_{OUT}$ | -0.6 to $V_{CC}+0.6$ | V  |

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Recommended Operating Conditions**

|                         |          | <i>min</i> | <i>typ</i> | <i>max</i> |               |
|-------------------------|----------|------------|------------|------------|---------------|
| DC Power Supply Voltage | $V_{CC}$ | 4.5        | 5.0        | 5.5        | V             |
| Input Low Voltage       | $V_{IL}$ | -1.0       | -          | 0.8        | V             |
| Input High Voltage      | $V_{IH}$ | 2.0        | -          | $V_{CC}+1$ | V             |
| Operating Temp Range    | $T_A$    | 0          | -          | 70         | °C            |
|                         | $T_{AI}$ | -40        | -          | 85         | °C (I Suffix) |
|                         | $T_{AM}$ | -55        | -          | 125        | °C (M Suffix) |

**DC Electrical Characteristics** ( $T_A=-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $V_{CC}=5\text{V} \pm 10\%$ )

| Parameter                | Symbol                | Test Condition  | <i>min</i> | <i>max</i> | Unit          |
|--------------------------|-----------------------|---|------------|------------|---------------|
| Input Leakage Current    | $I_{LI1}$             | $V_{IN} = \text{GND to } V_{CC} + 1$  | -          | 40         | $\mu\text{A}$ |
| Output Leakage Current   | 32 bit $I_{LO}$       | $V_{IO} = \text{GND to } V_{CC}$ , $\overline{\text{CS}}^{(1)} = V_{IH}$  | -          | 40         | $\mu\text{A}$ |
| Operating Supply Current | 32 bit $I_{CC32}$     | $\overline{\text{CS}}^{(1)} = \overline{\text{OE}} = V_{IL}$ , $\overline{\text{WE}} = V_{IH}$ , $I_{OUT} = 0\text{mA}$ , $f = 5\text{MHz}^{(2)}$ | -          | 320        | mA            |
|                          | 16 bit $I_{CC16}$     | As above  | -          | 166        | mA            |
|                          | 8 bit $I_{CC8}$       | As above  | -          | 89         | mA            |
| Standby Supply Current   | TTL levels $I_{SB1}$  | $\overline{\text{CS}}^{(1)} = 2.0\text{V to } V_{CC} + 1\text{V}$   | -          | 12         | mA            |
|                          | CMOS levels $I_{SB2}$ | $\overline{\text{CS}}^{(1)} = V_{CC} - 0.3\text{V to } V_{CC} + 1\text{V}$  | -          | 1.2        | mA            |
| Output Low Voltage       | $V_{OL}$              | $I_{OL} = 2.1\text{mA}$ .   | -          | 0.45       | V             |
| Output High Voltage      | $V_{OH}$              | $I_{OH} = -400\mu\text{A}$ .  | 2.4        | -          | V             |

Notes (1)  $\overline{\text{CS}}$  above are accessed through  $\overline{\text{CS}}1\text{-}4$ . These inputs must be operated simultaneously for 32 bit operation, in pairs in 16 bit mode and singly for 8 bit mode.

(2) Also for  $\overline{\text{WE}}1\text{-}4$  on the PUMA 68E4001A version. Additionally,  $\overline{\text{WE}}1\text{-}4$  are accessed as in note (1) above.

**Capacitance** ( $T_A=25^{\circ}\text{C}$ ,  $f=1\text{MHz}$ ) Note: These parameters are calculated, not measured.

| Parameter          | Symbol  | Test Condition        | <i>typ</i>           | <i>max</i> | Unit |    |
|--------------------|---|-----------------------|----------------------|------------|------|----|
| Input Capacitance  | $\overline{\text{CS}}1\text{-}4$ , $\overline{\text{WE}}1\text{-}4^{(1)}$ | $C_{IN1}$             | $V_{IN} = 0\text{V}$ | -          | 20   | pF |
|                    | Other Inputs  | $C_{IN2}$             | $V_{IN} = 0\text{V}$ | -          | 22   | pF |
| Output Capacitance | $C_{OUT}$   | $V_{OUT} = 0\text{V}$ | -                    | 22         | pF   |    |

Notes: (1) On the PUMA 68E4001A version only.

**AC OPERATING CONDITIONS****Read Cycle**

| Parameter                               | Symbol    | 12  |     | 15  |     | 20  |     | Unit |
|---|-----------|-----|-----|-----|-----|-----|-----|------|
|   |           | min | max | min | max | min | max |      |
| Read Cycle Time                         | $t_{RC}$  | 120 | -   | 150 | -   | 200 | -   | ns   |
| Address Access Time                     | $t_{AA}$  | -   | 120 | -   | 150 | -   | 200 | ns   |
| Chip Select Access Time                 | $t_{CS}$  | -   | 120 | -   | 150 | -   | 200 | ns   |
| Output Enable Access Time               | $t_{OE}$  | 0   | 60  | 0   | 70  | 0   | 80  | ns   |
| Chip Select High to High Z Output (1)   | $t_{HZ}$  | 0   | 50  | 0   | 50  | 0   | 50  | ns   |
| Output Enable High to High Z Output (1) | $t_{OHZ}$ | 0   | 50  | 0   | 50  | 0   | 50  | ns   |
| Chip Select Low to Active Output (1)    | $t_{LZ}$  | 0   | -   | 0   | -   | 0   | -   | ns   |
| Output Enable Low to Active Output (1)  | $t_{OLZ}$ | 0   | -   | 0   | -   | 0   | -   | ns   |
| Output Hold from Address Change         | $t_{OH}$  | 0   | -   | 0   | -   | 0   | -   | ns   |

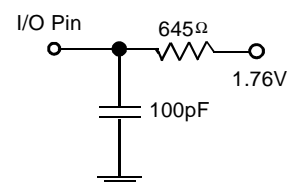
Notes: (1)  $t_{HZ}$  max. and  $t_{OLZ}$  max. are measured with  $C_L = 5pF$ , from the point when Chip Select or Output Enable return high (whichever occurs first) to the time when the outputs are no longer driven.  $t_{HZ}$  and  $t_{OHZ}$  are shown for reference only: they are characterized and not tested.

**Write Cycle**

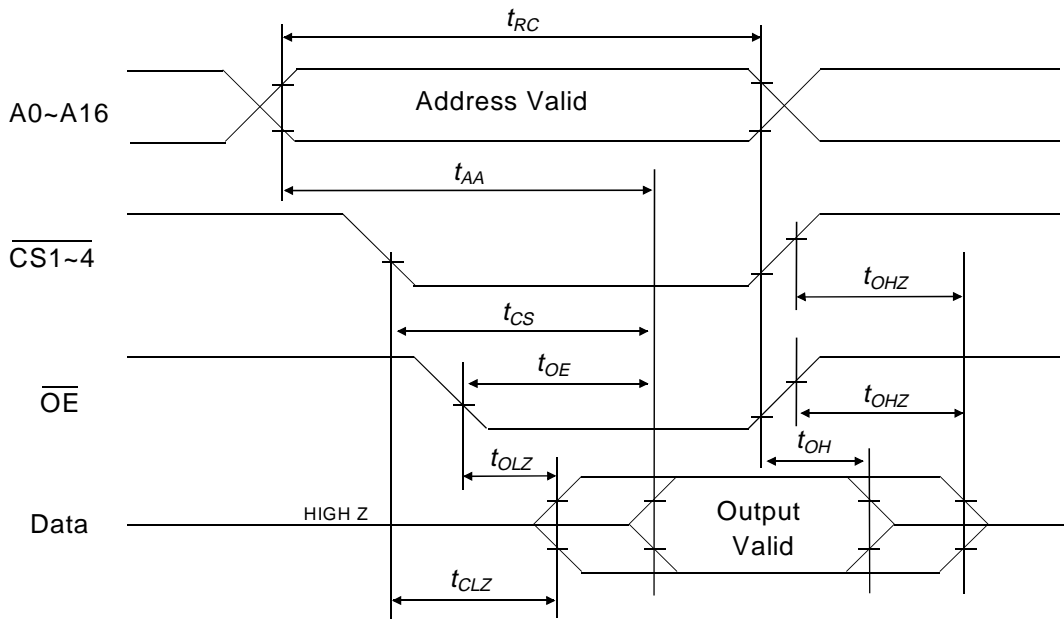
| Parameter                  | Symbol    | min | typ | max | Unit    |
|----------------------------|-----------|-----|-----|-----|---------|
| Write Cycle Time           | $t_{WC}$  | -   | -   | 10  | ms      |
| Address Set-up Time        | $t_{AS}$  | 0   | -   | -   | ns      |
| Address Hold Time          | $t_{AH}$  | 50  | -   | -   | ns      |
| Output Enable Set-up Time  | $t_{OES}$ | 0   | -   | -   | ns      |
| Output Enable Hold Time    | $t_{OEH}$ | 0   | -   | -   | ns      |
| Chip Select Set-up Time    | $t_{CS}$  | 0   | -   | -   | ns      |
| Chip Select Hold Time      | $t_{CH}$  | 0   | -   | -   | ns      |
| Write Pulse Width          | $t_{WP}$  | 100 | -   | -   | ns      |
| Write Enable High Recovery | $t_{WPH}$ | 50  | -   | -   | ns      |
| Data Set-up Time           | $t_{DS}$  | 50  | -   | -   | ns      |
| Data Hold Time             | $t_{DH}$  | 0   | -   | -   | ns      |
| Delay to Next Write        | $t_{DW}$  | 10  | -   | -   | $\mu s$ |
| Byte Load Cycle            | $t_{BLC}$ | -   | -   | 150 | $\mu s$ |

**AC Test Conditions****Output Test Load**

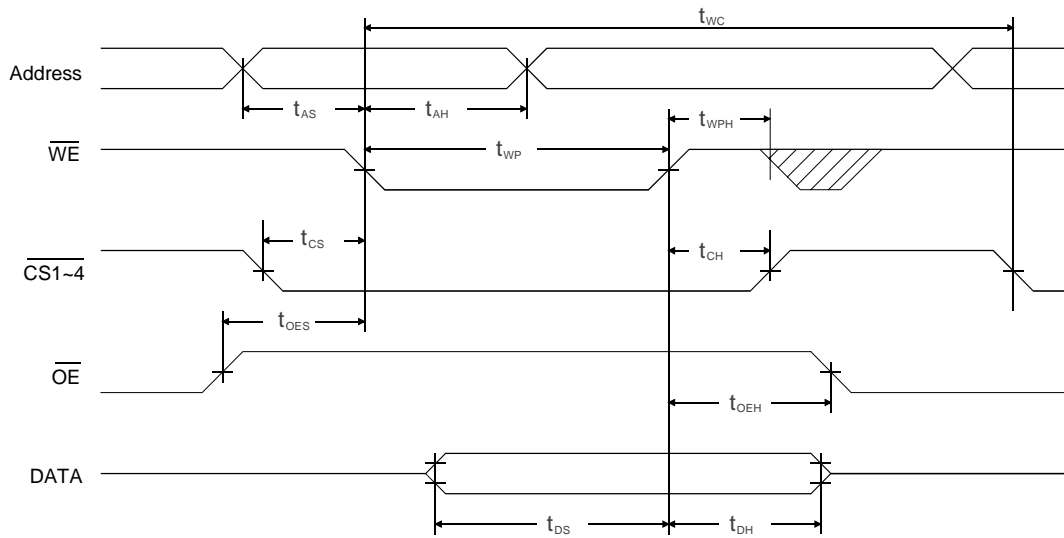
- \* Input pulse levels: 0V to 3.0V
- \* Input rise and fall times: 10ns
- \* Input and Output timing reference levels: 1.5V
- \* Output load: 1 TTL gate + 100pF
- \*  $V_{CC} = 5V \pm 10\%$



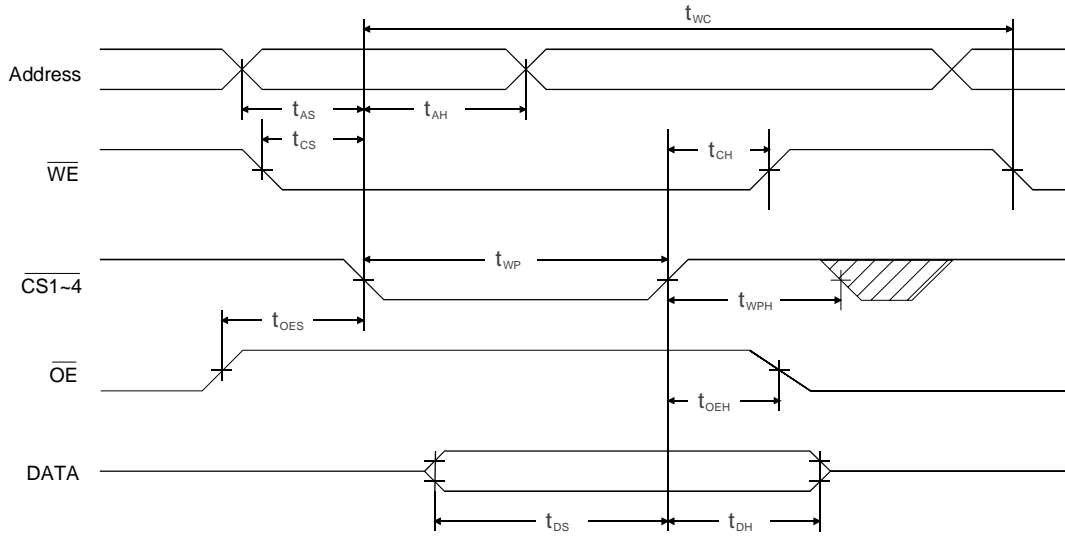
**Read Cycle Timing Waveform**



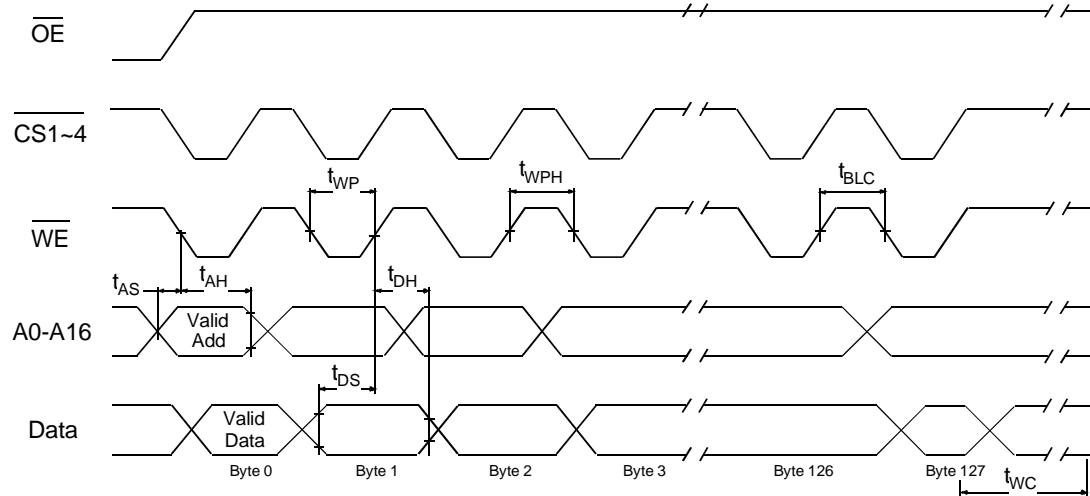
**AC Write Waveform - WE Controlled**



**AC Write Waveform -  $\overline{CS}$  Controlled**

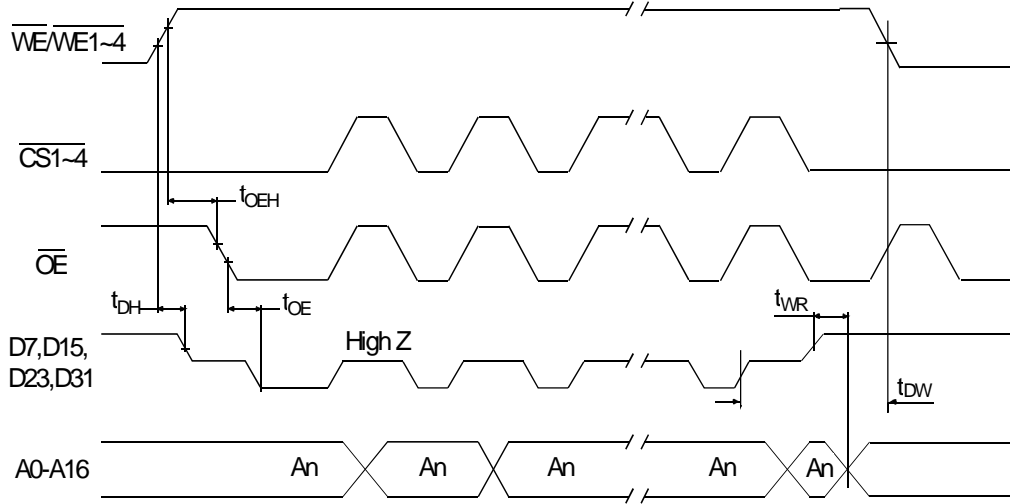


**Page Mode Write Waveform**

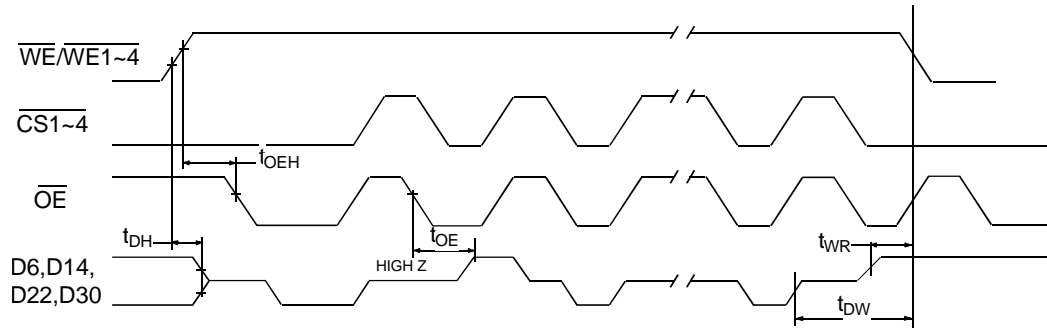


Note: A8 through A16 must specify the page address during each high to low transition of Write Enable (or Chip select). Output Enable must be high only when Write Enable and Chip Select are both low.

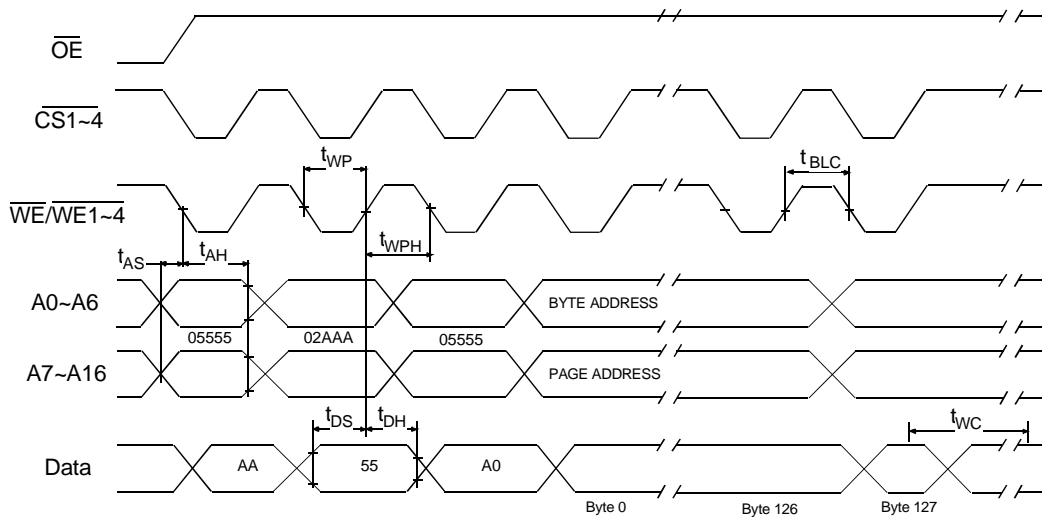
**DATA Polling Waveform**



**Toggle Bit Waveform**



**Software Protected Write Waveform**



## Device Operation

The following description deals with the PUMA 68E4001 device, with the references to  $\overline{WE}$  meaning  $\overline{WE1\sim4}$  on the PUMA 68E4001A part.

### Read

The PUMA 68E4001 read operations are initiated by both Output Enable and Chip Select LOW. The read operation is terminated by either Chip Select or Output Enable returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either Output Enable or Chip Select is HIGH.

### Write

Write operations are initiated when both Chip Select and Write Enable are LOW and Output Enable is HIGH. The PUMA 68E4001 supports both a Chip Select and Write Enable controlled write cycle. That is, the address is latched by the falling edge of either Chip Select or Write Enable, whichever occurs last. Similarly, the data is latched internally by the rising edge of either Chip Select or Write Enable, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms.

### Page Mode Write

The page write feature of the PUMA 68E4001 allows the entire memory to be written in 5 seconds. Page Write allows 128 bytes of data to be written prior to the internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address (A8 through A16) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write up to 128 bytes in the same manner as the first byte written. Each successive byte load cycle, started by the Write Enable HIGH to LOW transition, must begin within 150  $\mu$ s of the falling edge of the preceding Write Enable. If a subsequent Write Enable HIGH to LOW transition is not detected within 150  $\mu$ s, the internal automatic programming cycle will commence.

### DATA Polling

The PUMA 68E4001 features  $\overline{DATA}$  Polling to indicate if the write cycle is completed. During the internal programming cycle, any attempt to read the last byte written will produce the compliment of that data on D7. Once the programming is complete, D7 will reflect the true data. Note: If the PUMA 68E4001 is in a protected state and an illegal write operation is attempted  $\overline{DATA}$  Polling will not operate.

### TOGGLE bit

In addition to  $\overline{DATA}$  polling, another method is provided to determine the end of a Write Cycle. During a write operation successive attempts to read data will result in D6 toggling between 1 and 0. Once a write is complete, this toggling will stop and valid data will be read.

### Hardware Data Protection

The PUMA 68E4001 provides three hardware features to protect non-volatile data from inadvertent writes.

- Noise Protection - A Write Enable pulse less than 15 ns will not initiate a write cycle.
- Default  $V_{CC}$  Sence - All functions are inhibited when  $V_{CC} < 3.6$  V.
- Write Inhibit - Holding either Output Enable LOW, Write Enable HIGH or Chip Select HIGH will prevent an inadvertent write cycle during power on or power off, maintaining data integrity.

## Software Data Protection

The PUMA 68E4001 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protect feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the PUMA 68E4001 is also protected against inadvertent and accidental writes in that, the software algorithm must be issued prior to writing additional data to the device.

## Operating Modes

The table below shows the logic inputs required to control the operation of the PUMA 68E4001.

| MODE          | $\overline{\text{CS}}_{1-4}$ | $\overline{\text{OE}}$ | $\overline{\text{WE}}$ | OUTPUTS  |
|---------------|------------------------------|------------------------|------------------------|----------|
| Read          | 0                            | 0                      | 1                      | Data Out |
| Write         | 0                            | 1                      | 0                      | Data in  |
| Standby       | 1                            | X                      | X                      | Floating |
| Write Inhibit | X                            | X                      | 1                      |          |
|               | X                            | 0                      | X                      |          |

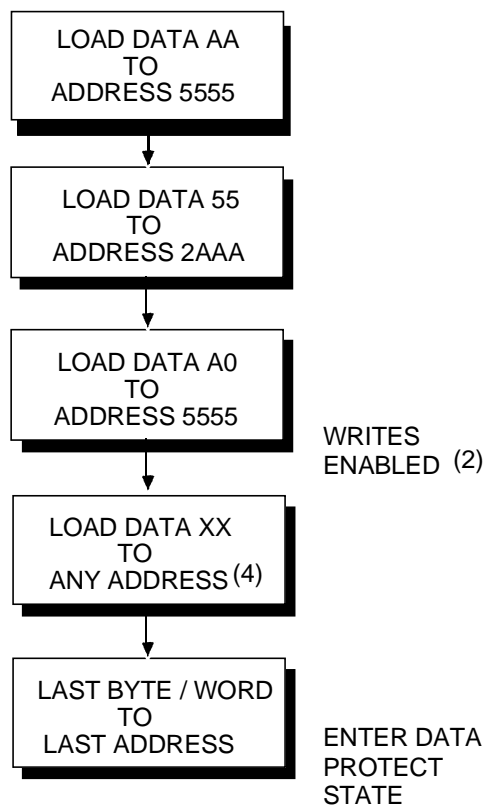
0 =  $V_{IL}$  : 1 =  $V_{IH}$  : X =  $V_{IH}$  or  $V_{IL}$

## Software Algorithms

Selecting the software data protection mode requires the host system to precede datawrite operations by a series of three write operations to three specific addresses. The three byte sequence opens the page write window enabling the host to write from 1 to 128 bytes of data. Once the page load cycle has been completed, the device will automatically be returned to the data protected state

## Software Data Protection Algorithm

Regardless of whether the device has been protected or not, once the software data protected algorithm is used and the data is written, the PUMA 68E4001 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the PUMA 68E4001 will be write protected during power-down and any subsequent power-up.

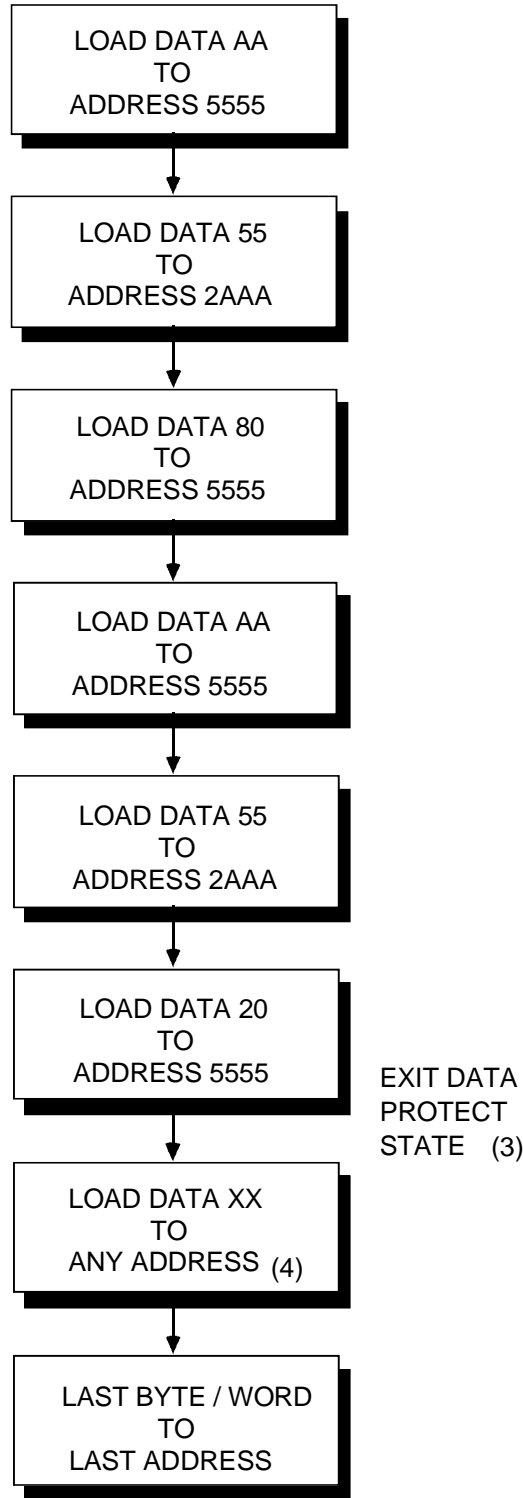


### Notes:

- (1) Data Format I/O7-I/O0 (Hex);  
**Once initiated, this sequence of write operations should not be interrupted.**
- (2) Enable Write Protect state will be initiated at end of write even if no other data is loaded.
- (3) Disable Write Protect state will be initiated at end of write period even if no other data is loaded.
- (4) 1 to 128 bytes of data may be loaded.

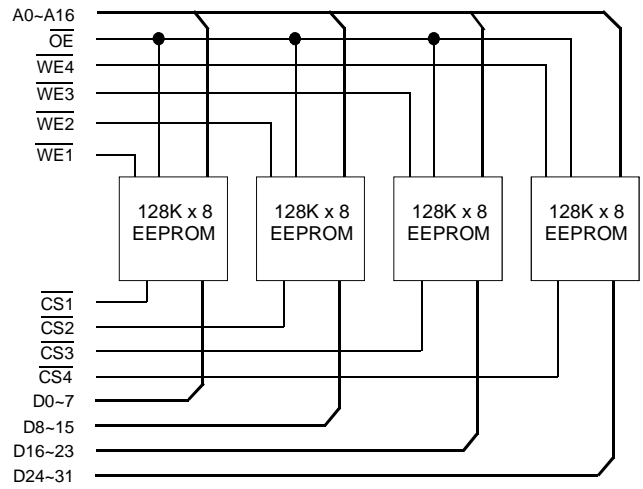
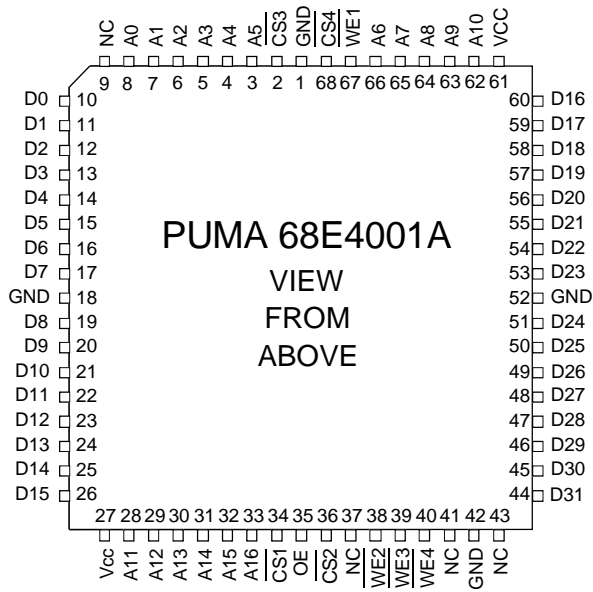
**Software Data Protect Disable**

In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E<sup>2</sup>PROM programmer. The following six step algorithm will reset the internal protection circuit. After  $t_{WC}$ , the PUMA 68E4001 will be in standard operating mode.



**Pin Definition 'A' version**

**Block Diagram 'A' version**





## Visual Inspection Standard

All devices inspected to ANSI/J-STD-001B Class 2 standard

## Moisture Sensitivity

Devices are **moisture sensitive**.

Shelf Life in Sealed Bag 12 months at <40°C and <90% relative humidity (RH).

After this bag has been opened, devices that will be subjected to infrared reflow, vapour phase reflow, or equivalent processing (peak package body temp 220°C) **must be** :

A : Mounted within 72 Hours at factory conditions of <30°C/60% RH

**OR**

B : Stored at <20% RH

If these conditions are not met or indicator card is >20% when read at 23°C +/-5% devices **require baking** as specified below.

If baking is required, devices may be baked for :-

A : 24 hours at 125°C +/-5% for high temperature device containers

**OR**

B : 192 hours at 40°C +5°C/-0°C and <5% RH for low temperature device containers.

## Packaging Standard

Devices packaged in dry nitrogen, JED-STD-020.

Packaged in trays as standard.

Tape and reel available for shipment quantities exceeding 200pcs upon request.

## Soldering Recommendations

|                 |                         |                |
|-----------------|-------------------------|----------------|
| IR/Convection - | Ramp Rate               | 6°C/sec max.   |
|                 | Temp. exceeding 183°C   | 150 secs. max. |
|                 | Peak Temperature        | 225°C          |
|                 | Time within 5°C of peak | 20 secs max.   |
|                 | Ramp down               | 6°C/sec max.   |
| Vapour Phase -  | Ramp up rate            | 6°C/sec max.   |
|                 | Peak Temperature        | 215 - 219°C    |
|                 | Time within 5°C of peak | 60 secs max.   |
|                 | Ramp down               | 6°C/sec max.   |

The above conditions must not be exceeded.

*Note : The above recommendations are based on standard industry practice. Failure to comply with the above recommendations invalidates product warranty.*