# NP-3

## 30-Gigabit Network Processor with Integrated Traffic Management

Product Brief


## Overview

EZchip's NP-3 is a highly-flexible network processor with integrated traffic managers providing wire-speed packet processing and advanced flow-based bandwidth control. The NP-3 offers the speed of an ASIC combined with the flexibility of a programmable microprocessor. It provides the silicon core of next-generation **Carrier Ethernet Switches and Routers (CESR).** Through programming the NP-3 delivers a variety of applications such as L2 switching, Q-in-Q, PBT, T-MPLS, VPLS, MPLS and IPv4/IPv6 routing. The integrated traffic management provides advanced QoS for flow-based service level agreements (SLA) and enabling triple-play services (voice, video, data).

The NP-3 is EZchip's fourth-generation network processor and builds on the architecture of the successful NP-2 network processor. The NP-3 integrates into a single chip several functions that would normally be found in separate chips:

- 30-Gigabit throughput
- Traffic managers
- Classification search engines
- OAM processing offload
- Ten 1-Gigabit and one 10-Gigabit Ethernet MACs, and two SPI4.2 interfaces

NP-3 provides exceptionally **flexible packet processing** enabling system designers to future proof their designs to support new protocols and features through s/w updates. Packet parsing is supported for any field anywhere in the packet. Various table lookup options are provided with support for long lookup keys and results. Flows are classified based on any combination of extracted packet information. Any packet header and content can be edited and packets can easily be replicated to support multicast applications. A 'run to completion' processing model guarantees support for processing scenarios of any complexity. Large code space is provided to support complex applications as well as true hitless code updates.

NP-3 offers extensive **traffic management** capabilities on the ingress and egress paths through a full-duplex queuing mechanism. This enables frame queuing and hierarchical scheduling of traffic on all NP-3 interfaces. Individual flows are assigned with specific QoS and are aggregated to enforce SLAs for services, users, virtual ports and ports.

NP-3 stores its **lookup tables** in **DRAM** to reduce power dissipation and cost while supporting large tables and providing extensive classification headroom.

On-chip **OAM** support tracks individual sessions and offloads the host CPU from the task of generating and monitoring OAM messages.

NP-3's flexibility and integration allows system vendors to deliver cost effective solutions that can easily adapt to changing market requirements. Typical applications include:

Line cards in modular chassis:

- Metro Switches
- Edge and Core Routers
- Aggregation Nodes
- Enterprise Backbone Switches

Stand-alone pizza box solutions:

- Access Nodes (GPON/EPON OLT, DSLAM, Wireless)
- Ethernet to SONET/SDH Switches
- Content Inspection and Network Monitoring
- Server Load Balancing Switches

## Features

- Single-chip, programmable, wire-speed network processor with 30-Gigabit aggregate throughput
- Line card and pizza box applications
- Three 10-Gigabit interfaces with simultaneous operation; one interface (XGMII) can operate in 20-Gigabit overspeed

EZCHIP

- Integrated Task Optimized Processors (TOPs) specifically designed for packet processing
- Flexible processing with programmable packet parsing, classifying, modifying and forwarding
- Ingress and egress traffic management with hierarchical scheduling
- Integrated search engines eliminating the need for external co-processors
- On-chip OAM protocol processing offload
- Two SPI 4.2 interfaces, ten 1-Gigabit Ethernet ports and one 10-Gigabit Ethernet port with integrated MACs
- Software compatible with NP-2 and NP-1c

## Integrated Traffic Managers

- Traffic management for traffic on ingress and egress paths
- Work conserving and non-work conserving schedulers
- Frame size from 1 byte to 16K bytes
- Up to 1 Gbyte total frame memory
- Per Flow Queuing (PFQ) with 4-level hierarchical scheduling
- Policing: Per-flow metering, marking and policing for millions of flows
- Configurable WRED profiles
- Shaping: Single and Dual leaky bucket controlling committed/peak rate/bursts (CIR, CIB, PIR, PIB) with IFG (Inter Frame Gap) emulation for accurate rate control
- Scheduling: WFQ and priority scheduling at each hierarchy level

## Integrated Search Engines

- Flexibly defined switching, routing, classification and policy lookup tables with millions of entries per table
- Programmable keys and results (associated information) per table with support for long keys and long results per table entry
- Table entries stored in DRAM to reduce power dissipation and cost and provide up to 1.5 Gbytes lookup tables headroom

## Stateful Classifying and Processing

- Off-loading control tasks from the control CPU
- Access to all 7 layers for classify and modify
- Maintain state of millions of sessions simultaneously
- On-chip state updates and learning of millions of sessions per second

## Programming

- Large code space memory for multiple and complex applications
- Single-image programming model with no parallel programming or multi-threading
- In-service software updates
- Automatic ordering of frames and allocation of resources
- Microcode compatible with EZchip's NP-1c and NP-2 network processors

## OAM Offload

- Keep-alive frame generation for precise and accurate session maintenance operations
- Keep-alive watchdog timers for fastest detection time

## Statistics and Counters

- Up to 16M 36-bit counters via external SRAM
- Auto implementation of token bucket per flow (srTCM, trTCM or MEF5)

## Physical Specifications

- Package: FCBGA 1517 pins, 1.00 mm pitch, 40x40 mm
- Process: IBM 90nm

# Sample Applications

Illustrated below are several sample solutions.

## Line Card Solutions

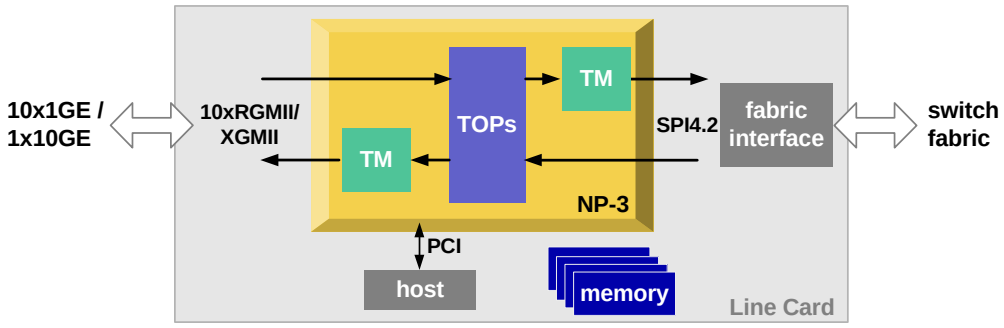


*Figure 1. 10x1GE (or 1x 10GE) ports using NP-3 integrated Ethernet MACs*

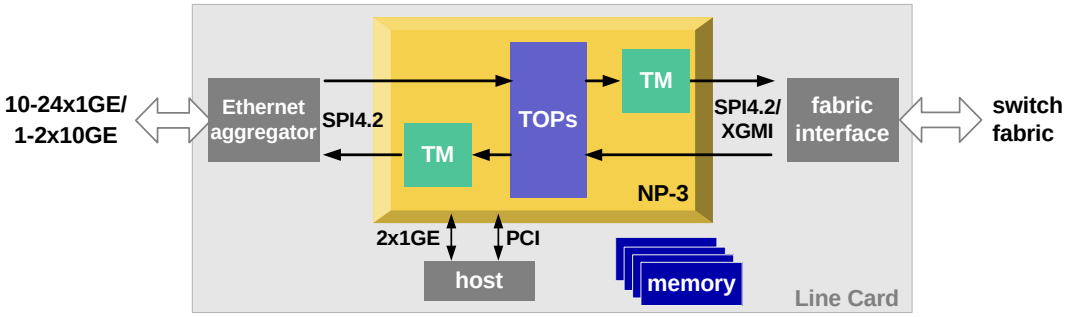


*Figure 2. Up to 24x1GE (or 2x 10GE) ports using an external Ethernet MAC*

## Stand-alone Solutions ("Pizza" Box)

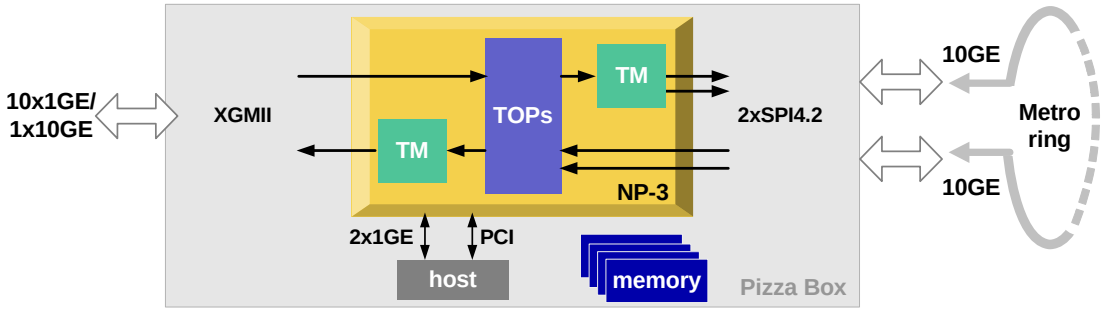


*Figure 3. 10GE ring application with 10GE add/drop and locally switched traffic*

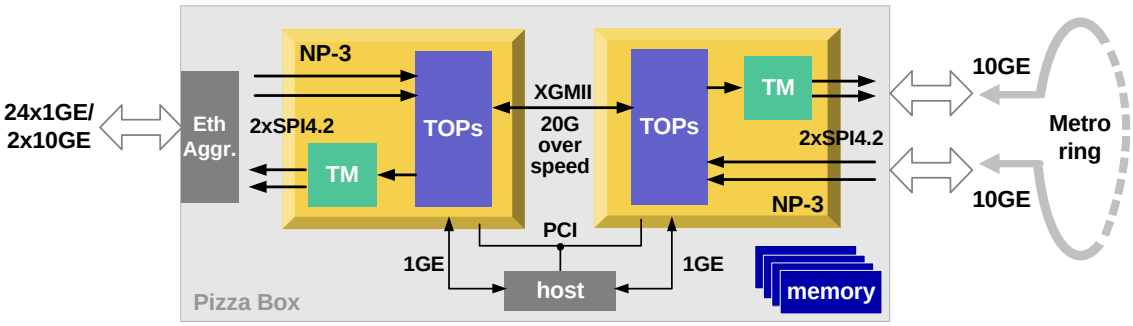


*Figure 4. 10GE ring application with 20GE add/drop and locally switched traffic.*

## About EZchip

EZchip Technologies is a fabless semiconductor company that provides Ethernet network processors. EZchip provides its customers with solutions that scale from 1-Gigabit to 100-Gigabits per second with a common architecture and software across all products. EZchip's network processors provide the flexibility and integration that enable triple-play data, voice and video services in systems that make up the new Carrier Ethernet networks. Flexibility and integration make EZchip's solutions ideal for building systems for a wide range of applications in telecom networks, enterprise backbones and data centers. Visit our web site at www.ezchip.com.

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