VAR-320SBC

Marvell Monahans-P (PXA320) based Single-Board-Computer

Table of Contents

1. Revision History

Revision No.	Draft Date	Remarks
1.0	31/Aug/2007	Initial draft
1.1	20/Sept/2007	Ethernet controller revised
2.0	11/Feb/2008	Mechanical change. Smaller form factor, 6x4cm

2. Overview

2.1. Basic

The VAR-320SBC is a rich feature set, Single-Board-Computer, ideal for cost and size effective embedded solutions where high-cpu performance and low power consumption are critical factors. The VAR-320SBC serves as a building block and easily integrates into any embedded solution. It includes all vital peripherals/interfaces and is ready to run any embedded operating system such as Linux, WinCE ™ and Windows Mobile™.

Supporting products:

- **Windows CE 5.0 / 6.0 BSP**. Contact support for further information.
- **VAR-3xxBASEBOARD** – Evaluation board.
  Package includes:
  - ✓ Base board. Compatible with VAR-320SBC.
  - ✓ Windows CE 5.0 / 6.0 run-time-image.
  - ✓ Schematics
  - ✓ Layout notes
  - ✓ Gerber files

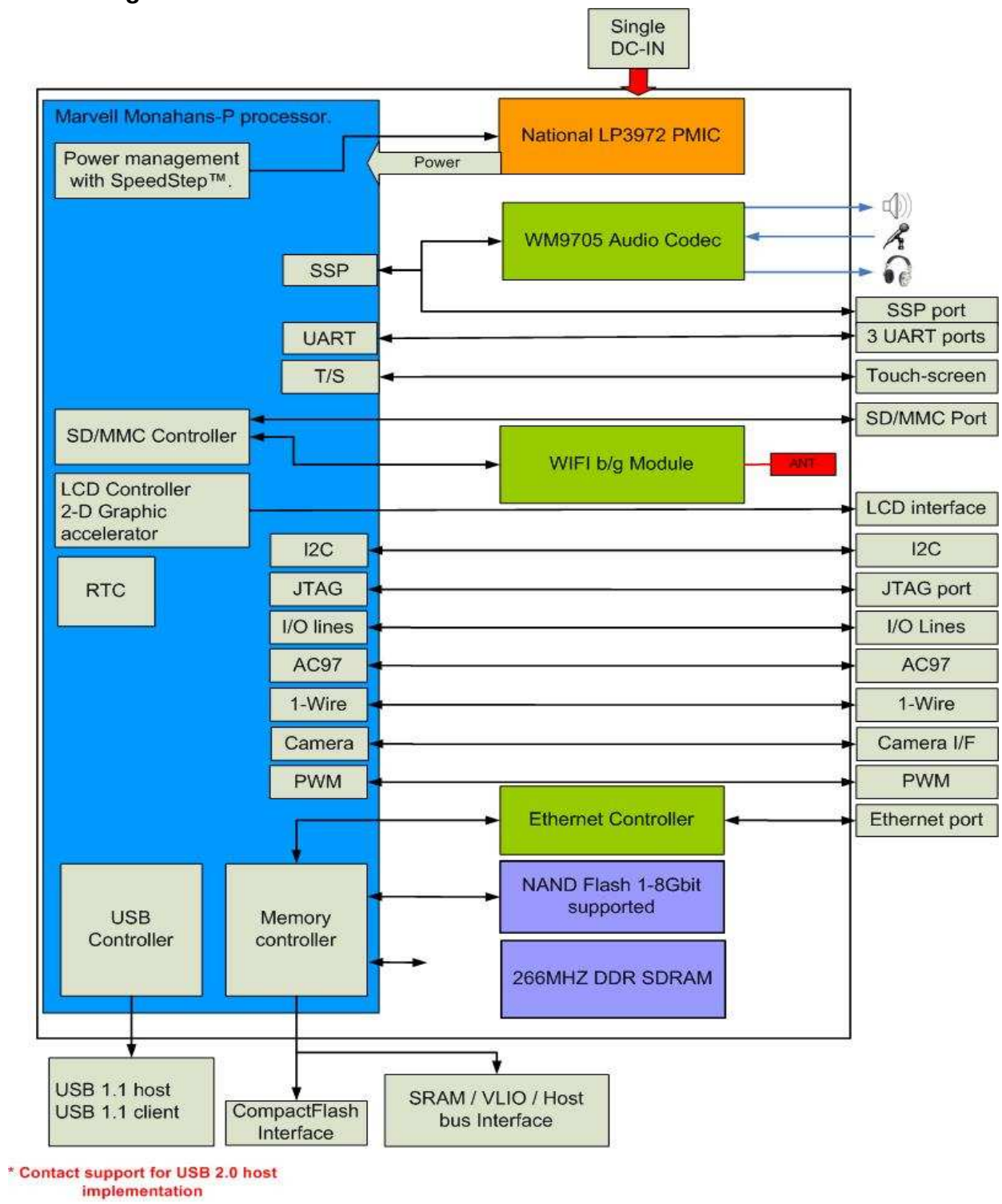
Contact support for further information. mailto:support@variscite.com

2.2. Features Summary

- Marvell Monahans-P (PXA320) CPU
  - **Up to 806 MHZ**
  - **2-D graphic accelerator**
  - 32kb/32kb Inst/ Data L1 cache
  - 256KB L2 cache
  - Internal 768kb SRAM
- 64-256MB **266MHZ DDR SDRAM**
- 128Mbytes - 1Gbytes Flash Disk
- **802.11 b/g WIFI module Built-In**
- CRT/LCD interface. Using 2-D graphic accelerator. Up to 800x600 resolution supported
- 2 SDcard/ SDIO/MMC card interfaces
- A/D - Up to 7 channels. 10KHZ, 10Bit resolution
- Power
  - National LP3972 management IC. Supports SpeedStep™ technology to achieve the most efficient power consumption
  - Lowest power solution, down to 3mw in sleep mode
  - Single 3.3 - 4.8V DC power supply
- Compact Flash interface
- Intel Quick Capture ™ Camera interface

- 3 UART ports to interfaces GSM/GPRS modem, Bluetooth, IRDA, Debug port
- 10/ 100 Mbit Ethernet controller
- General purpose I/O lines.
- Audio
  - HI - FI stereo decoder
  - Voice CODEC
  - Mono output for Speaker
  - Microphone input
  - Headphones output
- USB
  - 1 x full USB host interface
  - 1 x USB Client interface
  - Connects to an external USB 2.0 host controller
- Touch Screen interface
- Serial controller
  - 2 x SSP interfaces
  - 1 – Wire
  - I2C

2.3. Block Diagram



* Contact support for USB 2.0 host implementation

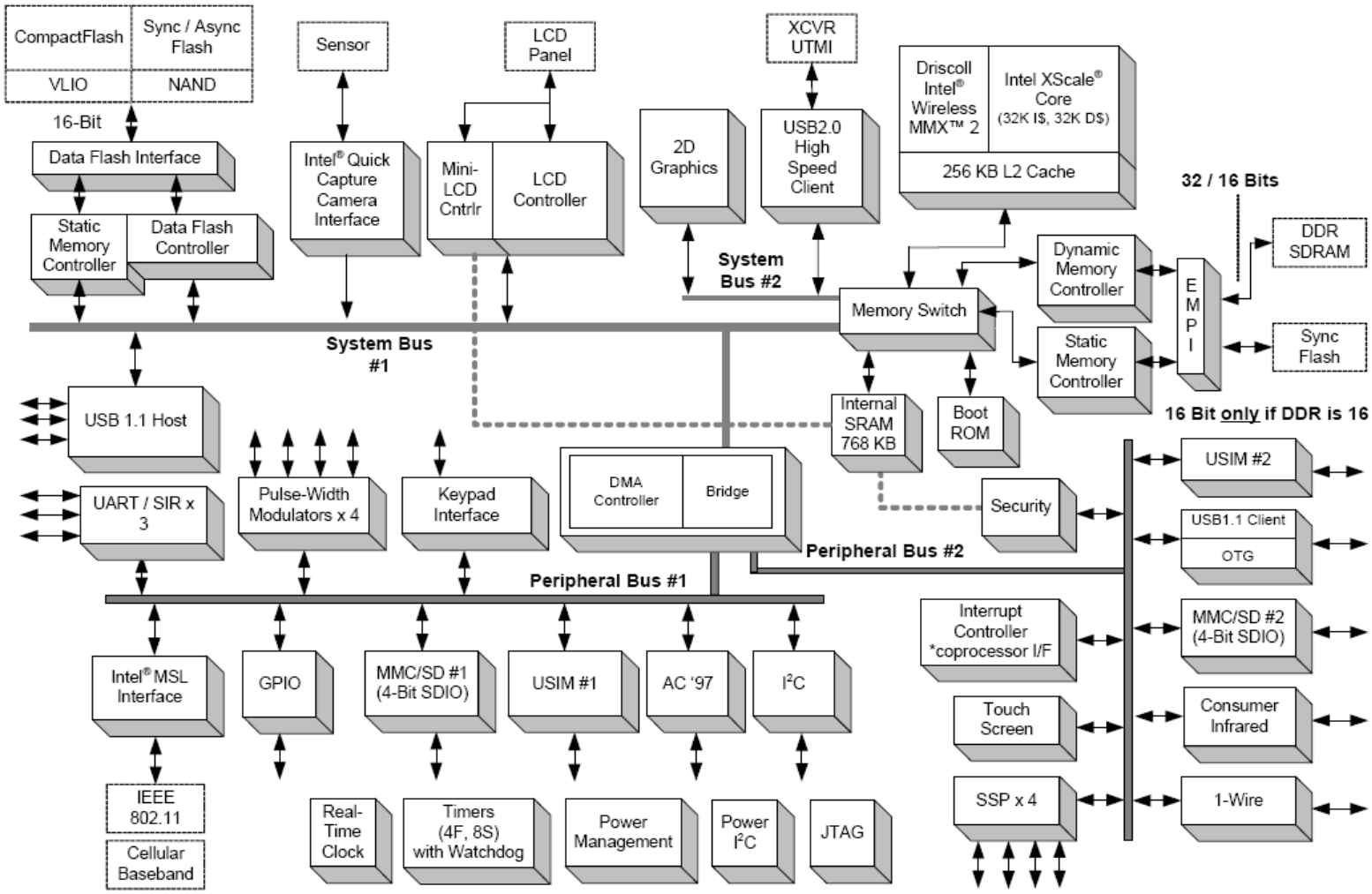
3. Components

3.1. MONAHANS-P CPU

3.1.1. Overview

The PXA320 processor is an integrated system-on-a-chip microprocessor for high-performance, low-power portable handheld and handset devices. It incorporates the Intel XScale® micro architecture with on-the-fly voltage and frequency scaling and sophisticated power management to provide industry leading MIPS/mW performance across its wide range of operating frequencies. The PXA320 processor complies with the ARM* Architecture V5TE instruction set (excluding floating point instructions) and follows the ARM* programmer's model. The PXA320 processor Multimedia coprocessor provides enhanced Intel® Wireless MMX 2 instructions to accelerate audio and video processing.

3.1.2. Monahans-P Block Diagram



3.1.3. Multimedia co-processor

The core integrates a Multimedia coprocessor to accelerate multimedia applications and 2-D graphics operations.
This coprocessor provides a 64-bit single-instruction multiple-data (SIMD) architecture and compatibility with the integer functionality of the Intel® Wireless MMX™ 2 technology and streaming SIMD extensions (SSE) instruction sets. Key features of this coprocessor include:

- 14 new media processing instructions
- 64-bit architecture including SIMD (up to eight simultaneous eight-bit operations)
- 16 x 64-bit register file
- SIMD PSR flags with group conditional execution support
- SIMD instruction support for sum-of-absolute-differences (SAD) and multiply-accumulate (MAC) operations
- Instruction support for alignment and video operations
- Intel® Wireless MMX™ 2 and SSE integer instruction compatibility
- Superset of existing core media processing instructions

3.1.4. Power Management

The PXA320 processor provides a rich set of flexible power-management controls for a wide range of usage models while enabling very low-power operation.

- Programmable frequency-change capability, with turbo settings without requiring the PLL to re-lock. Supported speeds are: 806 MHz, 624 MHz, 416 MHz, 312 MHz, 208 MHz, 104 MHz
- Five power modes to control power consumption

3.2. Memory

3.2.1. 266MHZ 32bit DDR SDRAM

The VAR-320SBC supports up to 128MB of DDR SDRAM with clock rate of 266 MHz.
The DDR SDRAM uses a double-data-rate architecture to achieve high-speed operation.

3.2.2. NAND flash

The VAR-320SBC supports NAND flashes up to the size of 8Gbit.
The NAND flash is used for Flash Disk purposes, operating system's run-time-image and the Bootloader (Boot from NAND).
The NAND flash can be Write-Protected with a dedicated WP# line.

3.3. Power Management IC, National LP3972

The PMIC uses a single 3.3-4.8V DC directly from battery or a regulated source. The PMIC provides stable, low-noise supplies for all core voltage domains, with additional regulators for supplying peripheral ICs. All supplies are fed by high-performance, low-dropout (LDO) voltage regulators and offering very low quiescent current consumption and high power supply rejection.
Three high-efficiency DC-DC buck converters provide high-current, low-voltage supplies to the processor core and memory. The main converter features Dynamic Voltage Management (DVM), with programmable voltage and slew rate control.

3.4. Wi2Wi WS2W0001 WIFI module

VAR-320SBC module includes a high-quality built-in 802.11 b/g WLAN module connected to the SDIO interface.
Chipset: Marvell 88W8686-B1.
Drivers for WinCE™, Linux are available.

3.5. Davicom® DM9000BEthernet controller

High-Performance Single-Chip 10/100 Ethernet controller with HP auto-MDIX and industrial temperature support

3.6. Connectors to base board

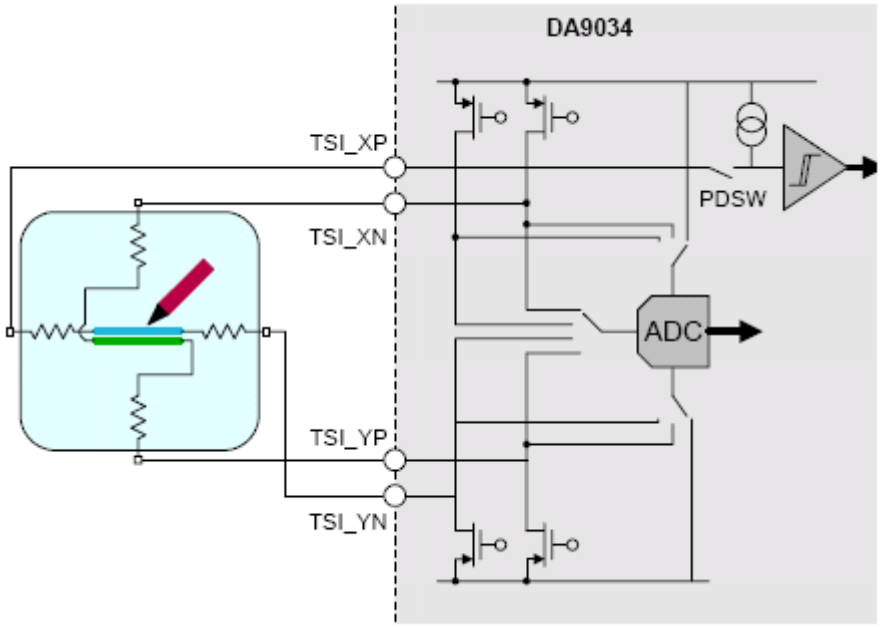
The VAR-320SBC connects to a base board using 2 140 pin Board-to-Board connectors.

Connector on VAR-320SBC:
Manufacturer: Tyco Electronics
P/N: 1-353190-0
Description: 0.6mm pitch Board-to-Board connector. 140 pin. Free height type.

Mating part to be used on base board:
Manufacturer: Tyco Electronics
P/N: 1-353180-0
Description: 0.6mm pitch Board-to-Board connector. 140 pin Free height type.

4. Interfaces

4.1. TouchScreen



Features:

- Compatible with 4-wire resistive Touch Screens
- Power is supplied by a dedicated LDO
- Pen-detection and nIRQ generation
- Supports several schemes of measurement averaging to filter noise
- Maximum X & Y sample rate (without averaging): 5 kHz

Signal	Pin number	Type	Description
TSPX	P2-88	Analog	TSI interface X Plus
TSMY	P2-90	Analog	TSI interface Y Minus
TSMX	P2-92	Analog	TSI interface X Minus
TSPY	P2-94	Analog	TSI interface Y Plus

4.2. SSP Interface

The VAR-320SBC outputs one SSP interface.

The SSP controllers support these protocols:

- ✓ Programmable serial protocol (PSP) with programmable frame sync and programmable start and stop delays
- ✓ Texas Instruments Synchronous Serial Protocol* (SSP)
- ✓ Motorola Serial Peripheral Interface* (SPI) protocol
- ✓ Inter-IC Sound (I2S) protocol

- Up to 13-Mbps transfer rate with internal clock generation
- Packed mode to 1w double-depth FIFOs if sample less than 16 bits wide
- Sample data formats from 8, 16, 18, and 32 bits of serial data
- Network mode for operation on a time-slotted bus
- Master or slave operation for both clock- and frame-sync signals
- Receive-without-transmit operation
- Flexible clock source selection from the 13-MHz master clock, the network clock input, or the dedicated SSP
- External clock input
- Audio clock control to provide a 4x or 8x output clock to support most standard audio frequencies

Signal	Pin number	Type	Description	GPIO
SSP4_SCLK	P2-54	I/O	Synchronous Serial Protocol Serial Clock	93
SSP4_SFRM	P2-56	I/O	Synchronous Serial Protocol Serial Frame Indicator	94
SSP4_TXD	P2-58	O	Synchronous Serial Protocol Transmit Data	95
SSP4_RXD	P2-60	I	Synchronous Serial Protocol Receive Data	96

4.3. UART Ports

The VAR-320SBC outputs 3 UARTs

- Full function UART (FFUART)
- Bluetooth UART (BTUART)
- Standard UART (STUART)

Each serial port contains a UART and a slow serial infrared transmit encoder and receive decoder that conform to the IrDA serial infrared specification.1
Each UART includes a programmable baud-rate generator. The supported baud rates are 9600, 19.2 K, 38.4 K, 57.6 K, 115.2 K, 230 K, 460 K, and 921 K.
Receive and transmit FIFO fill and drain operations can be done using programmed IO or DMA transfers. To minimize CPU overhead for UART communications, device driver software can setup interrupts and DMA for data transfers to/from memory.
All three UARTs support the 16550A and 167502 functions.

Full function UART (FFUART) signals:

Signal	Pin number	Type	Description	GPIO
FFRXD	P1-27	I	FFUART RXD	41
FFTXD	P1-29	O	FFUART TXD	42
FFDCD	P1-33	I	FFUART DCD	44
FFDTR	P1-35	O	FFUART DTR	47
FFDSR	P1-37	I	FFUART DSR	45
FFCTS	P1-39	I	FFUART CTS	43
FFRTS	P1-41	O	FFUART RTS	48
FFRI	P1-45	I	FFUART RI	46

Bluetooth UART (BTUART) signals:

Signal	Pin number	Type	Description	GPIO
BT_TXD	P1-22	O	BT UART TXD	111
BT_RXD	P1-24	I	BT UART RXD	110
BT_CTS	P1-28	I	BT UART CTS	112
BT_RTS	P1-30	O	BT UART RTS	109

Standard UART (STUART) signals:

Signal	Pin number	Type	Description	GPIO
STD_TXD	P1-42	O	ST UART TXD	107
STD_RXD	P1-44	I	ST UART RXD	108

4.4. SD/MMC Ports

The VAR-320SBC outputs 2 SD/MMC ports.

The MultiMediaCard (MMC) and Secure Digital (SD/SDIO) controller (MMC/SD/SDIO controller) provide a software-accessible hardware link between the PXA320 and the MMC stack (a set of memory cards). The MMC/SD/SDIO controller supports Multimedia Card, Secure Digital, and Secure Digital I/O communication protocols. The PXA320 contains two independent MMC/SD/SDIO controllers.

- 1-bit and 4-bit data transfers are supported for MMC, SD, and SDIO communication protocols
- Data transfer clock of 19.5 MHz
- Support for all valid MMC and SD/SDIO protocol data-transfer modes
- Interrupt-based application interface to control software interaction
- Multiple MMC cards are supported when using the MMC communications protocol
- Only one SD or SDIO card is supported when using the SD or SDIO communications protocol per controller.
- Up to two MMC or SD/SDIO cards are supported when using the SPI communications protocol. Mixed card types are supported only by the SPI communications protocol per controller.

Signal	Pin number	Type	Description	GPIO
MMC_CLK	P1-102	O	SD/MMC Bus clock	22
MMC_CMD_0	P1-104	O	SD/MMC Command	23
MMC_DAT_0	P1-112	I	SD/MMC Data	18
MMC_DAT_1	P1-114	I	SD/MMC Data	19
MMC_DAT_2	P1-116	O	SD/MMC Data	20
MMC_DAT_3	P1-118	O	SD/MMC Data	21
MMC2_CLK	P1-120	O	SD/MMC 2 Bus clock	28
MMC2_CMD	P1-124	O	SD/MMC 2 Command	29
MMC2_DAT_0	P1-126	I	SD/MMC 2 Data	24
MMC2_DAT_1	P1-128	I	SD/MMC 2 Data	25
MMC2_DAT_2	P1-130	O	SD/MMC 2 Data	26
MMC2_DAT_3	P1-132	O	SD/MMC 2 Data	27

4.5. LCD Interface

The LCD controller supports these key features:

- Support for active or passive single-panel displays of 8, 16, or 18 bpp
- Support for LCD panels with internal frame buffer; up to 24 bpp is supported
- Support display sizes up to 800x600 pixels.

Signal	Pin number	Type	Description	GPIO
L_PCLK	P2-1	O	LCD Pixel clock	16_2
L_FCLK	P2-3	O	LCD Frame clock	14_2
L_LCLK	P2-5	O	LCD Line clock	15_2
L_BIAS	P2-9	O	LCD AC bias/Data enable	17_2
L_DD_0	P2-11	O	LCD Data line	6_2
L_DD_1	P2-13	O	LCD Data line	7_2
L_DD_2	P2-15	O	LCD Data line	8_2
L_DD_3	P2-17	O	LCD Data line	9_2
L_DD_4	P2-21	O	LCD Data line	10_2
L_DD_5	P2-23	O	LCD Data line	11_2
L_DD_6	P2-25	O	LCD Data line	12_2
L_DD_7	P2-27	O	LCD Data line	13_2
L_DD_8	P2-29	O	LCD Data line	63
L_DD_9	P2-33	O	LCD Data line	64
L_DD_10	P2-35	O	LCD Data line	65
L_DD_11	P2-37	O	LCD Data line	66
L_DD_12	P2-39	O	LCD Data line	67
L_DD_13	P2-41	O	LCD Data line	68
L_DD_14	P2-45	O	LCD Data line	69
L_DD_15	P2-47	O	LCD Data line	70
L_DD_16	P2-16	O	LCD Data line	71
L_DD_17	P2-18	O	LCD Data line	72

4.6. JTAG Port

JTAG provides a way of driving and sampling the external pins of the device regardless of the core state, as well as a mechanism for device debug. JTAG logic includes a test-access port (TAP) controller, TAP pins, an instruction register, and Test Data registers (TDRs). The JTAG interface is controlled through five dedicated TAP pins that interface to the TAP controller: TDI, TMS, TCK, nTRST, and TDO.

Signal	Pin number	Type	Description
NTRST	P2-128	I	JTAG Test Reset
TDI	P2-130	I	JTAG Serial data input
TMS	P2-132	I	JTAG Test Mode Select
TDO	P2-136	O	JTAG Serial data output
TCK	P2-138	I	JTAG Test Clock

4.7. 1-Wire

The 1-Wire bus master interface controller is designed to receive and transmit 1-Wire bus data and provides complete control of the 1-Wire bus through eight-bit commands.
The 1-Wire bus serial operation uses an open-drain, wired-AND bus structure that allows multiple devices to drive the bus lines and to communicate status on events such as arbitration, wait states, and error conditions.

Signal	Pin number	Type	Description	GPIO
ONE_WIRE	P1-64	I/O	Open-drain 1-Wire bidirectional data bus.	0_2

4.8. Camera Interface

The Quick Capture Interface is intended for use in a PDA or mobile phone product that requires image-capture capability.
The PXA320 processor supports a variety of operating modes, data widths, formats, and clocking schemes.

Some common usage scenarios include:

- Capturing simple still images, sharing images using email, and sending images to a web photo finisher
- Using images for “pictures-as-information”
- Capturing video clips
- Providing a two-way video conference
- Performing “text imaging” (scanner/OCR)

Features:

- Supported vertical and horizontal resolutions of:
  – 176 x 144
  – 352 x 288
  – 320 x 240
  – 640 x 480
  – 1280 x 1024
  – 1600 x 1200
  – 2048 x 1536
  – 2048 x 2048
  – 2560 x 2048
- Programmable sensor clock output from 187 kHz to 52 MHz
- Pixel clock received from 187 kHz to 52 MHz
- Programmable interrupts for FIFO overflow, end of line, and end of frame
- Support for 8- and 10-bit RAW (RGGB, CMYG, etc.) capture modes
- Support for master-mode operation
- Programmable interface timing signals for external synchronization signaling
- Preprocessed YCbCr 4:2:2 planar-capture mode
- RAW (RGGB, CMYG) capture modes:
  – Support for packing of 8- and 10-bit RAW pixel data up to 2560x2048
  – Pixel processing preview chain supporting up to 1280x1024 resolution (SXGA)
- Three programmable 64-element look-up-tables (LUT)
  – Three independent mapping functions, (fR(x), fG(x), and fB(x)), supported
  – Companding from 10-bit to 8-bit RAW data
  – Programmable black-level clamp (BLC) offset
- Histogram unit generates statistics for image data

– Performs statistics on 8- or 10-bit data
– Incrementer saturates to avoid rollovers
– Supports up to 64 K pixels, (216) per data value
– Can perform statistics on 8-bit or 10-bit data stream with 32-bit result

- Dead-pixel substitution unit supports sensor resolutions up to 2560x2048
  – Up to 128 pixels of any color can be substituted
- Scaling support for 2:1 /4:1 image resizing for RAW RGGB or YCbCr 4:2:2 image data
  – Preprocessed YCbCr 2:1 and 4:1 scaling provided up to 704x576 resolution
  – RAW RGGB 2:1 up to 704x576 resolution and 4:1 scaling provided up to 1280x1024 resolution
- Color-management support for RAW digital viewfinder and video-clip capture
- Programmable coefficients for 3x3 matrix multiplication for color and tone correction
- Programmable coefficients for color space conversion from RGB to YCbCr 4:2:2

Signal	Pin number	Type	Description	GPIO
CIF_DD0	P1-66	I	Quick Capture Interface Data Signal	49
CIF_DD1	P1-68	I	Quick Capture Interface Data Signal	50
CIF_DD2	P1-70	I	Quick Capture Interface Data Signal	51
CIF_DD3	P1-72	I	Quick Capture Interface Data Signal	52
CIF_DD4	P1-76	I	Quick Capture Interface Data Signal	53
CIF_DD5	P1-78	I	Quick Capture Interface Data Signal	54
CIF_DD6	P1-80	I	Quick Capture Interface Data Signal	55
CIF_DD7	P1-82	I	Quick Capture Interface Data Signal	56
CIF_DD8	P1-84	I	Quick Capture Interface Data Signal	57
CIF_DD9	P1-96	I	Quick Capture Interface Data Signal	58
CIF_MCLK	P1-88	I	Quick Capture Interface Master Clock Signal	59
CIF_PCLK	P1-90	O	Pixel clock	60
CIF_LV	P1-92	I/O	Quick Capture Interface Line Synchronization Signal - Horizontal sync signal	61
CIF_FV	P1-94	I/O	Quick Capture Interface Frame Synchronization Signal - Vertical sync signal	62

4.9. PWM

The VAR-320SBC outputs 2 of the 4 PXA320 processor's pulse-width modulator (PWM) pins. Each can be configured to generate periodic output signals. Configuration of the PWMs is accomplished through software and is described in detail in Marvell® PXA320 Processor Serial Controller Configuration Developers Manual, Vol. IV, "Section 9:Pulse-Width Modulator Controller".

Signal	Pin number	Type	Description	GPIO
PWM_0	P2-4	O	Pulse-width modulated output signal	11
PWM_1	P1-108	O	Pulse-width modulated output signal	12

4.10. Ethernet port

The VAR-320SBC integrates one full-featured 10/100 Mbit Ethernet interface using Davicom DM9000B Ethernet controller.

Features:

- Fully compliant with IEEE 802.3/802.3u standards
- Integrated Ethernet MAC and PHY
- 10BASE-T and 100BASE-TX support
- Full- and Half-duplex support
- Full-duplex flow control
- Backpressure for half-duplex flow control
- Preamble generation and removal
- Automatic 32-bit CRC generation and checking
- Automatic payload padding and pad removal
- Auto-negotiation
- Automatic polarity detection and correction

Signal	Pin number	Type	Description
TPI_N	P1-3	I	Ethernet Twisted Pair Receive Negative
TPI_P	P1-1	I	Ethernet Twisted Pair Receive Positive
TPO_P	P1-2	O	Ethernet Twisted Pair Transmit Positive
TPO_N	P1-4	O	Ethernet Twisted Pair Transmit Negative
nLINK_ACK	P1-6	O	LED, Activity Indicator
nSPD_100	P1-5	O	LED, Speed Indicator
AGND	P1-8,10,12	O	Analog GND for Ethernet magnetics
ETH_V_1P8V	P1-16,18,20	O	Analog 1.8v supply for Ext. Ethernet magnetics

4.11. USB

4.11.1. USB 1.1 Full speed OTG and Client Controller

The UDC supports 24 endpoints (Endpoint 0 plus 23 programmable endpoints). The UDC is a USB revision 1.1 compliant, full-speed device that operates half-duplex at a baud rate of 12 Mbps (as a slave only, not a host or hub controller).

Signal	Pin number	Type	Description
USB_OTG_P	P1-136	I/O	USB_OTG Positive
USB_OTG_P	P1-138	I/O	USB OTG Negative

4.11.2. Universal Serial Bus Host Controller

The Universal Serial Bus (USB) supports serial data exchanges between a host computer and a variety of simultaneously-accessible peripherals. The attached peripherals share USB bandwidth through a host-scheduled, token-based protocol. Peripherals can be attached, configured, used, and detached, while the host and other peripherals continue operation.

Features:

- USB Rev. 1.1 compatible
- Supports both low-speed and full-speed USB devices
- Open Host Controller Interface (OHCI) Rev 1.0a compatible
- Root hub supports three downstream ports

Signal	Pin number	Type	Description
USBH_N	P2-64	I/O	USB Full Speed Host Port 1 Positive Line
USBH_P	P2-66	I/O	USB Full Speed Host Port 1 Negative Line

Static Memory interface (Compact Flash, Nand flash, host-bus, SRAM, VLIO)

Features:

- Connection to the DFI.
- Interface to SRAM-like devices, Variable Latency I/O (VLIO) devices, various types of XIP flash (including synchronous and asynchronous), and Compact Flash.
- NAND flash devices with NOR flash interfaces on the DFI. Read burst and write burst capabilities
- Support synchronous flash, asynchronous flash, SRAM, VLIO, and synchronous read/write flash-type companion chips on DFI.

Signal	Pin number	Type	Description	GPIO
DF_IO_0	P2-93	I/O	Data bus	n/a
DF_IO_1	P2-95	I/O	Data bus	n/a
DF_IO_2	P2-97	I/O	Data bus	n/a
DF_IO_3	P2-99	I/O	Data bus	n/a
DF_IO_4	P2-101	I/O	Data bus	n/a
DF_IO_5	P2-105	I/O	Data bus	n/a
DF_IO_6	P2-107	I/O	Data bus	n/a
DF_IO_7	P2-109	I/O	Data bus	n/a
DF_IO_8	P2-111	I/O	Data bus	n/a
DF_IO_9	P2-113	I/O	Data bus	n/a
DF_IO_10	P2-117	I/O	Data bus	n/a
DF_IO_11	P2-119	I/O	Data bus	n/a
DF_IO_12	P2-121	I/O	Data bus	n/a
DF_IO_13	P2-123	I/O	Data bus	n/a
DF_IO_14	P2-125	I/O	Data bus	n/a
DF_IO_15	P2-129	I/O	Data bus	n/a
DF_BA_0	P2-57	O	DFI bus address 0	n/a
DF_BA_1	P2-59	O	DFI bus address 1	n/a
DF_BA_2	P2-61	O	DFI bus address 2	n/a
DF_BA_3	P2-63	O	DFI bus address 3	n/a
DF_ALE_NWE	P2-53	O	Output write enable for static memory, muxed with DF ALE signal	n/a
DF_CLE_NOE	P2-51	O	Output enable for static memory, muxed with DF CLE signal.	n/a
nCS_2	P2-98	O	Chip select for static memory on the data flash interface.	3
nXCVREN	P2-49	O	External transceiver enable, Data flash interface	n/a
BE0_N	P2-72	O	Data byte enable. BE0_N corresponds to DF_IO<7:0>	n/a

BE1_N	P2-80	O	Data byte enable. BE1_N corresponds to DF_IO<8:15>	n/a
LLA_N	P2-69	O	DFIO Lower address latch	n/a
LUA_N	P2-71	O	DFIO Upper address latch	n/a

Compact Flash specific:

Signal	Pin number	Type	Description	GPIO
CF_nPIOR	P2-83	O	Card interface I/O space output enable	5
CF_nPIOW	P2-85	O	Card interface I/O space write enable	6
CF_nIOIS16	P2-87	I	0 = 16-bit I/O space, 1 = 8-bit I/O space	7
CF_nPWAIT	P2-89	I	Card interface input for inserting wait states.	8
CF_RESET	P2-112	I	CF card reset	n/a
CF_BVD1	P2-116	I	CF card BVD1	n/a
CF_RDY	P2-118	I	CF_RDY	n/a

4.12. Power

*See also Chapter 5: Power supply and management

Power signals:

Signal	Pin number	Type	Description
PWR_EN	P1-52	O	Active-high output from the PXA320 processor (input to the PMIC), which enables the low-voltage core and internal SRAM power supplies.
SYS_EN	P1-54	O	Active-high output from the PXA320 processor which enables the system (high-voltage) power supplies
RESET_IN_N	P2-20	I	Master reset input (active low) to force complete system reset
RESET_OUT_N	P2-124	I	Reset out line from PXA320 to peripheral devices
nONKEY	P2-22	I	On switch activates the LP3972 PMIC.
EXT_WAKEUP1	P2-40	I	Wake-up signal from Deep-Sleep
VDD_DDR_EXT	P1-34,36	I	DDR 1.8V supply for Deep-sleep
BACKUP BATTERY	P2-46,48	I	Backup battery charger output
V_BATT	P1: 7,19,31,43,55,67,79,91,103,115,127,139. P2: 7,19,31,43,55,67,79,91,103,115,127.	I	VAR-320SBC single DC-IN supply voltage. Voltage range: 3.3v – 4.8v
GND	P1: 8,14,26,38,50,62,74,86,98,110,122,134 P2: 2,14,26,38,50,62,74,86,110,122,134	I	

4.13. Audio

The VAR-320SBC uses the Wolfson WM9705 Audio codec

Audio signals:

Signal	Pin number	Type	Description
CODEC_MONO_OUT	P1-47	O	Loudspeaker mono output for Ext. Amp
HP_LOUT	P2-82	O	Headphones, Right.
HP_ROUT	P2-84	O	Headphones, Left.
CODEC_LINEOUTL	P2-32	O	Codec audio line out L
CODEC_LINEOUTR	P2-34	O	Codec audio line out R
CODEC_MIC	P2-131	I	Audio codec mic in
CODEC_BIAS	P2-133	O	Audio codec mic bias voltage
AUD_GND	P2-135,137,139	O	Audio low noise output GND for MIC

4.14. I2C Bus

The PXA320 processor has two I2C peripherals: the standard I2C interface and the Power I2C interface.
The standard I2C bus serves as the PXA320 processor interface to other I2C peripherals and microcontrollers, as well as a method of managing system functions. The standard I2C bus allows the PXA320 processor to serve as a master and slave device residing on the I2C bus. Control and status information is relayed through a set of memory-mapped registers.
The Power I2C interface contains a subset of the standard I2C interface and is dedicated for connection to an external voltage regulator for hard coded power management communication. If PWR_EN or SYS_EN change state (for example during a power state change), the appropriate I2C commands are transmitted to the PMIC as well. No configuration or software interaction is required. The Power I2C interface cannot be used as a general- purpose I2C interface. ***The Power I2C is used internally by the VAR-320SBC and cannot be used by the user***.
The standard I2C has a standard bus speed of 100 kbps and a fast-mode operation of 400 kbps.

*Both SDA and SCL lines are internally pulled up with a 1.2k resistor to 3.3v.

Signal	Pin number	Type	Description
SDA	P1-60	I/O	Serial data for the standard I2C controller.
SCL	P1-61	O	Serial clock for the standard I2C controller.

5. Power supply and management

5.1. Power Supply

The VAR-320SBC can operate from a single 3.3v - 4.8v DC supply.
Voltage supply can be connected directly to a Lio-ion battery, or external regulated DC supply.
The single DC supply must be connected to all V_BATT net pins:

V_BATT pins:
P1 :7,19,31,43,55,67,79,91,103,115,127,139.
P2 : 7,19,31,43,55,67,79,91,103,115,127,135

V_BATT is connected directly to the National LP3972 PMIC which provides stable, low-noise supplies for all core voltage domains, with additional regulators for supplying peripheral ICs. All supplies are fed by high-performance, low-dropout (LDO) voltage regulators.
Three high-efficiency DC-DC buck converters provide high-current, low-voltage supplies to the processor core and memory. The main converter features Dynamic Voltage Management (DVM), with programmable voltage and slew rate control.

5.2. Power consumption

VAR-320SBC power consumption depends on the active components and peripherals.
BSP implements Dynamic Voltage Management. Core changes its own frequency / Voltage according to CPU usage percentage. Frequency / Voltage control is automatic when enabled.

VAR-320SBC basic configuration:

- ✓ Marvell™ PXA320 624 MHz processor.
- ✓ 1Gbit NAND flash.
- ✓ 128MB DDR SDRAM.
- ✓ 3 UARTS
- ✓ I2C
- ✓ TOUCHSCREEN
- ✓ SRAM turned off after boot sequence.

Test conditions. DC_IN, V_BATT = 4v

Power loading configuration	Typical
VAR-320SBC basic configuration, running at 624mhz	0.9Watt
VAR-320SBC basic configuration, running at 406mhz	0.85Watt
VAR-320SBC basic configuration, running at 104mhz	0.75Watt
Deep-sleep	3 mW

6. Connectors

6.1. P1

Pin num	Signal	Type	Description	GPIO
1	TPI_P	O	Ethernet Twisted Pair Receive Positive	n/a
2	TPO_P	I	Ethernet Twisted Pair Transmit Positive	n/a
3	TPI_N	O	Ethernet Twisted Pair Receive Negative	n/a
4	TPO_N	I	Ethernet Twisted Pair Transmit Negative	n/a
5	nSPD_100	O	LED, Activity Indicator	n/a
6	nLINK_ACK	O	LED, Speed Indicator	n/a
7	V_BATT			n/a
8	AGND	O	Analog GND for Ethernet magnetics	n/a
9	NC			n/a
10	AGND	O	Analog GND for Ethernet magnetics	n/a
11	NC			n/a
12	AGND		Analog GND for Ethernet magnetics	n/a
13	GPIO0	I/O	General purpose IO pin	0
14	NC			n/a
15	GPIO1	I/O	General purpose IO pin	1
16	ETH_V_1P8V	O	Analog 1.8v for Ethernet magnetics	40
17	GPIO16	I/O	General purpose IO pin	16
18	ETH_V_1P8V	O	Analog 1.8v for Ethernet magnetics	34
19	V_BATT			n/a
20	ETH_V_1P8V	I	Analog 1.8v for Ethernet magnetics	39
21	NC			n/a
22	BT_TXD	O	BT UART TXD	111
23	NC			n/a
24	BT_RXD	I	BT UART RXD	110
25	NC			n/a
26	GND			n/a
27	FFRXD	I	FFUART RXD	41
28	BT_CTS	I	BT UART CTS	112
29	FFTXD	O	FFUART TXD	42
30	BT_RTS	O	BT UART RTS	109
31	V_BATT			n/a
32	NC			n/a
33	FFDCD	I	FFUART DCD	44
34	VDD_DDR_EXT	O	DDR 1.8V supply for Deep-sleep	37
35	FFDTR	O	DATA TERMINAL READY	47
36	VDD_DDR_EXT	I	DDR 1.8V supply for Deep-sleep	35
37	FFDSR	I	FFUART DSR	45
38	GND			n/a
39	FFCTS	I	FFUART CTS	43
40	N.C.			
41	FFRTS	O	FFUART RTS	48
42	STD_TXD	O	ST UART TXD	107

43	V_BATT			n/a
44	STD_RXD	O	ST UART RXD	108
45	FFRI	I	FFUART RI	46
46	GPIO126		General purpose IO pin	126
47	CODEC MONO OUT		Loudspeaker mono output for external Amplifier	n/a
48	GPIO127		General purpose IO pin	127
49	N.C.			
50	GND			n/a
51	N.C.			
52	PWR_EN	O	Active-high output, Enables low-voltage core and internal SRAM power supplies.	n/a
53	N.C.			
54	SYS_EN	O	Active-high output, enables system power supplies	n/a
55	V_BATT			n/a
56	N.C.			n/a
57	GPIO78		General purpose IO pin	78
58	N.C.			n/a
59	GPIO76	I/O	General purpose IO pin	76
60	I2C_SDA	I/O	Serial data for the Standard I2C controller.	n/a
61	I2C_SCL	O	Serial clock for the standard I2C controller.	n/a
62	GND			n/a
63	GPIO88		General purpose IO pin	88
64	ONE_WIRE	I/O	Open-drain 1-Wire bidirectional data bus.	0_2
65	GPIO75	I/O	General purpose IO pin	75
66	CIF_DD0	I	Quick Capture Data Signal	49
67	V_BATT	I		
68	CIF_DD1	I	Quick Capture Data Signal	50
69	NC			
70	CIF_DD2	I	Quick Capture Data Signal	51
71	NC			n/a
72	CIF_DD3	I	Quick Capture Data Signal	52
73	NC			n/a
74	GND			n/a
75	NC			n/a
76	CIF_DD4	I	Quick Capture Data Signal	53
77	NC			n/a
78	CIF_DD5	I	Quick Capture Data Signal	54
79	V_BATT			n/a
80	CIF_DD6	I	Quick Capture Data Signal	55
81	NC			n/a
82	CIF_DD7	I	Quick Capture Data Signal	56
83	NC			n/a
84	CIF_DD8	I	Quick Capture Data Signal	57
85	NC			n/a
86	GND	I		n/a
87	NC			n/a
88	CIF_MCLK	O	Quick Capture Master Clock Signal	59
89	NC			n/a
90	CIF_PCLK	O	Quick Capture Pixel clock	60
91	V_BATT			n/a

92	CIF_LV	O	Quick Capture Line Synchronization Signal	61
93	GPIO105	I/O	General purpose IO pin	105
94	CIF_FV	O	Quick Capture Frame Synchronization Signal	62
95	GPIO106	I/O	General purpose IO pin	106
96	CIF_DD9	I	Quick Capture Data Signal	58
97	GPIO113	I/O	General purpose IO pin	113
98	GND	I		n/a
99	GPIO114	I/O	General purpose IO pin	114
100	NC			n/a
101	GPIO115	I/O	General purpose IO pin	115
102	MMC_CLK	O	SD/MMC Bus clock	22
103	V_BATT			
104	MMC_CMD_0	O	SD/MMC Command	23
105	GPIO116	I/O	General purpose IO pin	116
106	GPIO1_2	I/O	General purpose IO pin	1_2
107	GPIO117	I/O	General purpose IO pin	117
108	PWM_1		Pulse-width modulated output signal	12
109	GPIO118	I/O	General purpose IO pin	118
110	GND			n/a
111	GPIO119	I/O	General purpose IO pin	119
112	MMC_DAT_0	I/O	SD/MMC Data	18
113	GPIO120	I/O	General purpose IO pin	120
114	MMC_DAT_1	I/O	SD/MMC Data	19
115	V_BATT	I		n/a
116	MMC_DAT_2	I/O	SD/MMC Data	20
117	GPIO121	I/O	General purpose IO pin	121
118	MMC_DAT_3	I/O	SD/MMC Data	21
119	GPIO122	I/O	General purpose IO pin	122
120	MMC2_CLK	O	SD/MMC Bus clock	28
121	GPIO123	I/O	General purpose IO pin	123
122	GND			n/a
123	GPIO124	I/O	General purpose IO pin	124
124	MMC2_CMD	O	SD/MMC Command	29
125	GPIO125	I/O	General purpose IO pin	125
126	MMC2_DAT_0	I/O	SD/MMC Data	24
127	V_BATT	I		n/a
128	MMC2_DAT_1	I/O	SD/MMC Data	25
129	GPIO_5_2	I/O	General purpose IO pin	5_2
130	MMC2_DAT_2	I/O	Data	26
131	N.C.			n/a
132	MMC2_DAT_3	I/O	SD/MMC Data	27
133	N.C.			n/a
134	GND			n/a
135	N.C.		.	n/a
136	USB_OTG_P	I/O	USB OTG Positive	n/a
137	N.C.			n/a
138	USB_OTG_N	I/O	USB OTG Negative	n/a
139	V_BATT	I		n/a
140	N.C.			n/a

6.2. P2

Pin num	Signal	Type	Description	GPIO
1	L_PCLK	O	LCD Pixel clock	16_2
2	GND			n/a
3	L_FCLK	O	LCD Frame clock	14_2
4	PWM_0	O	Pulse-width modulation output signal	11
5	L_LCLK	O	LCD Line clock	15_2
6	N.C.			n/a
7	V_BATT			n/a
8	N.C.			n/a
9	L_BIAS	O	LCD AC bias/Data enable	17_2
10	N.C.			n/a
11	L_DD_0	O	LCD Data line	6_2
12	N.C.			n/a
13	L_DD_1	O	LCD Data line	7_2
14	GND			n/a
15	L_DD_2	O	LCD Data line	8_2
16	L_DD_16	O	LCD Data line	71
17	L_DD_3	O	LCD Data line	9_2
18	L_DD_17	O	LCD Data line	72
19	V_BATT			n/a
20	RESET_IN_N	I	Master reset input.	
21	L_DD_4	O	LCD Data line	10_2
22	nONKEY	I	On switch. Activates the National PMIC.	n/a
23	L_DD_5	O	LCD Data line	11_2
24	N.C.			n/a
25	L_DD_6	O	LCD Data line	12_2
26	GND			n/a
27	L_DD_7	O	LCD Data line	13_2
28	ADC_IN1		A / D line input 1	n/a
29	L_DD_8	O	LCD Data line	63
30	ADC_IN2		A / D line input 2	n/a
31	V_BATT			n/a
32	CODEC_LINEOUTL		Codec audio line out L	n/a
33	L_DD_9	O	LCD Data line	64
34	CODEC_LINEOUTR	I	Codec audio line out R	
35	L_DD_10	O	LCD Data line	65
36	N.C.			n/a
37	L_DD_11	O	LCD Data line	66
38	GND			n/a
39	L_DD_12	O	LCD Data line	67
40	EXT_WAKEUP1	I	Wake-up signal to the PXA320.	
41	L_DD_13	O	LCD Data line	68

42	N.C.			n/a
43	V_BATT			n/a
44	N.C.			n/a
45	L_DD_14	O	LCD Data line	69
46	BACKUP BATTERY	O	Backup battery charger output	n/a
47	L_DD_15	O	LCD Data line	70
48	BACKUP BATTERY	O	Backup battery charger output	n/a
49	nXCVREN	O	External transceiver enable, Data flash interface.	n/a
50	GND			n/a
51	DF_CLE_NOE		Output enable for static memory, muxed with DF CLE.	n/a
52	N.C.			n/a
53	DF_ALE_NWE	O	Output write enable for static memory, muxed with DF ALE	n/a
54	SSP4_SCLK	I/O	Synchronous Serial Protocol Serial Clock	93
55	V_BATT			n/a
56	SSP4_SFRM	I/O	Synchronous Serial Protocol Serial Frame Indicator	94
57	DF_BA_0	O	DFI bus address 0	n/a
58	SSP4_TXD	O	Synchronous Serial Protocol Transmit Data	95
59	DF_BA_1	O	DFI bus address 1	n/a
60	SSP4_RXD	I	Synchronous Serial Protocol Receive Data	96
61	DF_BA_2	O	DFI bus address 2	n/a
62	GND			
63	DF_BA_3	O	DFI bus address 3	n/a
64	USBH_N	I/O	USB Full Speed Host Port 1 Positive Line	n/a
65	N.C.			n/a
66	USBH_P	I/O	USB Full Speed Host Port 1 Negative Line	n/a
67	V_BATT			n/a
68	USBH_PEN		USB Full speed host power control.	2_2
69	LLA_N	O	Lower address latch	n/a
70	USBH_OVERC		USB Full speed host over currant indicator	3_2
71	LUA_N	O	Upper address latch	n/a
72	BE0_N	O	Data byte enable. BE0_N corresponds to DF_IO<0:7>	n/a
73	RESET_N	I	PMU Reset	n/a
74	GND			n/a
75	N.C.			n/a
76	N.C.			n/a
77	N.C.			n/a
78	N.C.			n/a
79	V_BATT			n/a
80	BE1_N	O	Data byte enable. BE1_N corresponds to DF_IO<8:15>	n/a
81	N.C.			n/a
82	HP_LOUT		Headphones, Right.	n/a
83	CF_nPIOR	O	CF Card interface I/O space output enable	5
84	HP_ROUT	O	Headphones, Left.	n/a
85	CF_nPIOW	O	CF Card interface I/O space write enable	6
86	GND			n/a
87	CF_nIOIS16	I	CF interface. 0 = 16-bit I/O space, 1 = 8-bit I/O space	7
88	TSPX	I/O	TSI interface X Plus	n/a
89	CF_nPWAIT	I	Card interface input for inserting wait states.	8

90	TSMY	I/O	TSI interface Y Minus	n/a
91	V_BATT			n/a
92	TSMX	I/O	TSI interface X Minus	n/a
93	DF_IO_0	I/O	DFI Data bus	n/a
94	TSPY	I/O	TSI interface Y Plus	n/a
95	DF_IO_1	I/O	DFI Data bus	n/a
96	WL_ACTIVE	O	WLAN activity Bluetooth co-existence output line.	n/a
97	DF_IO_2	I/O	DFI Data bus	n/a
98	nCS_2	O	Chip select for static memory on the data flash interface.	3
99	DF_IO_3	I/O	DFI Data bus	n/a
100	N.C.			n/a
101	DF_IO_4	I/O	DFI Data bus	n/a
102	N.C.			n/a
103	V_BATT			n/a
104	BT_STATE	I	Bluetooth state WLAN co-existence input line.	
105	DF_IO_5	I/O	DFI Data bus	n/a
106	BT_PRIORITY	I	Bluetooth priority WLAN co-existence input line.	n/a
107	DF_IO_6	I/O	DFI Data bus	n/a
108	DF_CS1_N	O	DFI chip select 1	n/a
109	DF_IO_7	I/O	DFI Data bus	n/a
110	GND			n/a
111	DF_IO_8	I/O	DFI Data bus	n/a
112	CF_RESET	O	CF card reset	n/a
113	DF_IO_9	I/O	DFI Data bus	n/a
114	CF_CD_1n		CF card detect	n/a
115	V_BATT			n/a
116	CF_BVD1	O	CF card BVD1	n/a
117	DF_IO_10	I/O	DFI Data bus	n/a
118	CF_RDY			n/a
119	DF_IO_11	I/O	DFI Data bus	n/a
120	WLAN_WAKEUP			n/a
121	DF_IO_12	I/O	DFI Data bus	n/a
122	GND			n/a
123	DF_IO_13	I/O	DFI Data bus	n/a
124	RESET_OUT_N	O	Reset out line from PXA320 to peripheral devices	n/a
125	DF_IO_14	I/O	DFI Data bus	n/a
126	SOFT_RST	I	Soft (GPIO) reset	n/a
127	V_BATT			n/a
128	NTRST	I	JTAG Test Reset	n/a
129	DF_IO_15	I/O	DFI Data bus	n/a
130	TDI	I	JTAG Serial data input	n/a
131	CODEC_MIC	I	Audio codec mic in	n/a
132	TMS	I	JTAG Test Mode Select	n/a
133	CODEC_BIAS	O	Audio codec mic bias voltage	n/a
134	GND			n/a
135	AUD_GND	O	Audio low noise output GND for MIC	n/a
136	TDO	O	JTAG Serial data output	n/a
137	AUD_GND	O	Audio low noise output GND for MIC	n/a

138	TCK	I	JTAG Test Clock	n/a
139	AUD_GND	O	Audio low noise output GND for MIC	n/a
140	V_RTC	O	Permanent 2.9v output voltage	n/a

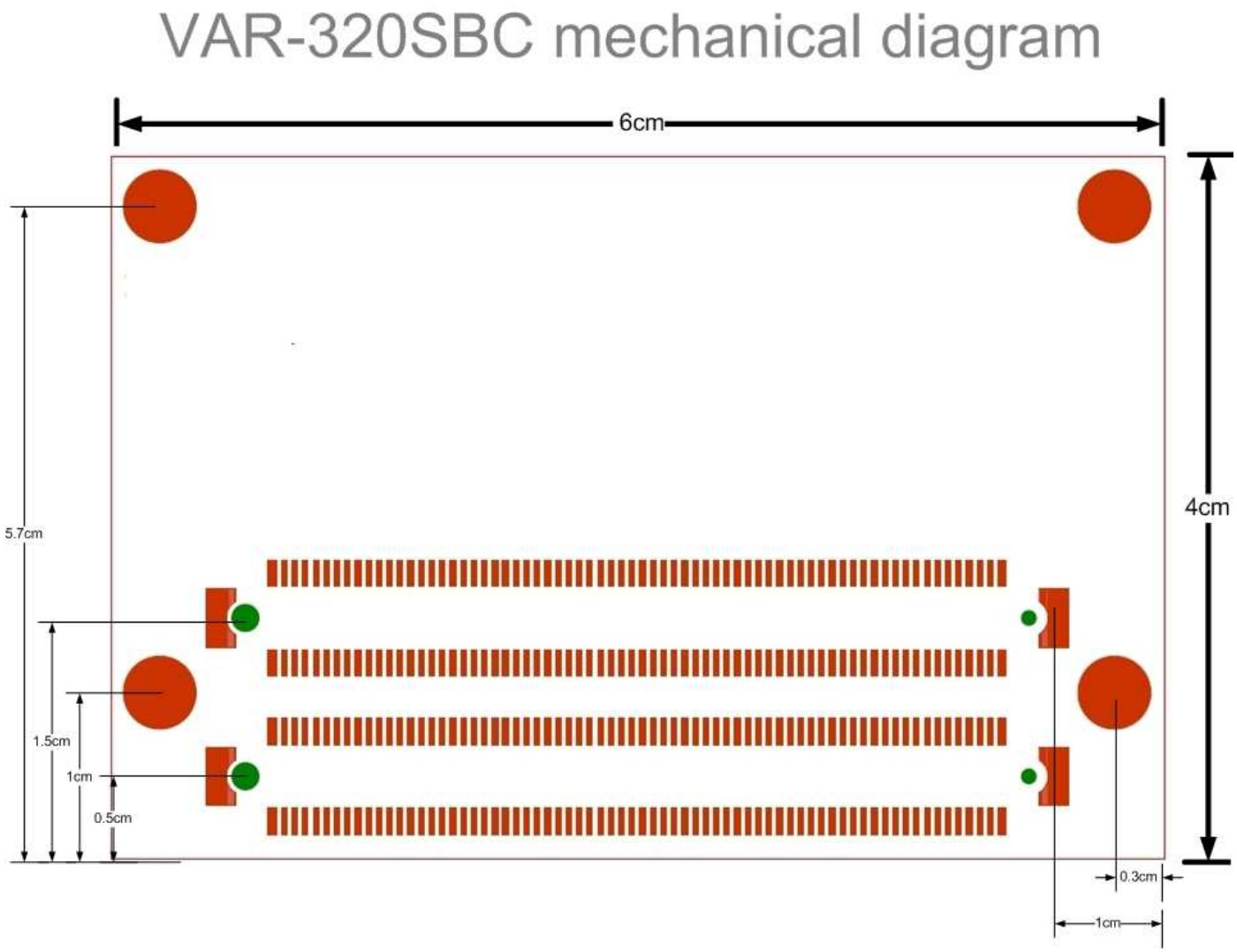
7. Operational Characteristics

Condition	Min	Max
Supply Voltage, V_BATT	-0.3V	5.5V
Commercial operating temperature range	-0°C	+65°C
Extended operating temperature range	-20Ẁ°C	+85°C

8. Absolute maximum Characteristics

	Min	Max
Supply Voltage, V_BATT	-0.3V	5.5V
Storage temperature range	-45°C	+165°C

9. Mechanical drawing



- SBC Height including BaseBoard connectors: 9mm

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