VARISCITE LTD.

VAR-SOM-OM35 Datasheet

Texas Instruments OMAP35xx based System-On-Module

VARISCITE LTD.

VAR-SOM-OM35 Data Sheet

Variscite Ltd.
60 Medinat Hayudim st.
Hertzelia Pituach
P.O.B 12598
46722, Israel
Phone +972 (9) 9562910 • Fax +972 (9) 9589477

Revision History

Revision	Date	Notes
1.1	01/05/2009	
1.2	16/09/2009	VAR-SOM-OM35 v1.2: Hardware Changes: 1. DF_IO_A10 (Pin 113) removed. Now GND 2. LB_LBE1 (Pin 162) removed. Now GND. 3. BT_STATE (Pin 191) removed. Now MMC2_DIR_CMD 4. WL_ACTIVE (Pin 193) removed. Now MMC2_DIR_DAT_0 5. BT_PIORITY (Pin195) removed. Now MMC2_CLKIN
1.3	20/10/2009	VAR-SOM-OM35 v1.3: Hardware support for Deep sleep mode added. Hardware Changes: 1. I2C2_SDA (Pin 81) removed. Now GND 2. I2C2_SCL (Pin 83) removed. Now GND 3. CLK_OUT2 (Pin 47) removed. Now GND. 4. CAM_XCLKB (Pin 51) removed. Now GND 5. LB_nCS7 (Pin 58) removed. Now GND 6. LB_nCS6 (Pin 48) removed. Now GND 7. TV_OUT1 (Pin 94) removed. Now VDD_DDR_EXT 8. TV_OUT2 (Pin 96) removed. Now VDD_DDR_EXT

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1 Overview

This chapter gives a short overview of the VAR-SOM-OM35

1.1 General Information

The VAR-SOM-OM35 is a low-power; high performance System-on-module which serves as a building block and easily integrates into any embedded solution. It includes all vital peripherals / interfaces and is ready to run any embedded operating system such as Linux and WinCE.

Supporting products:

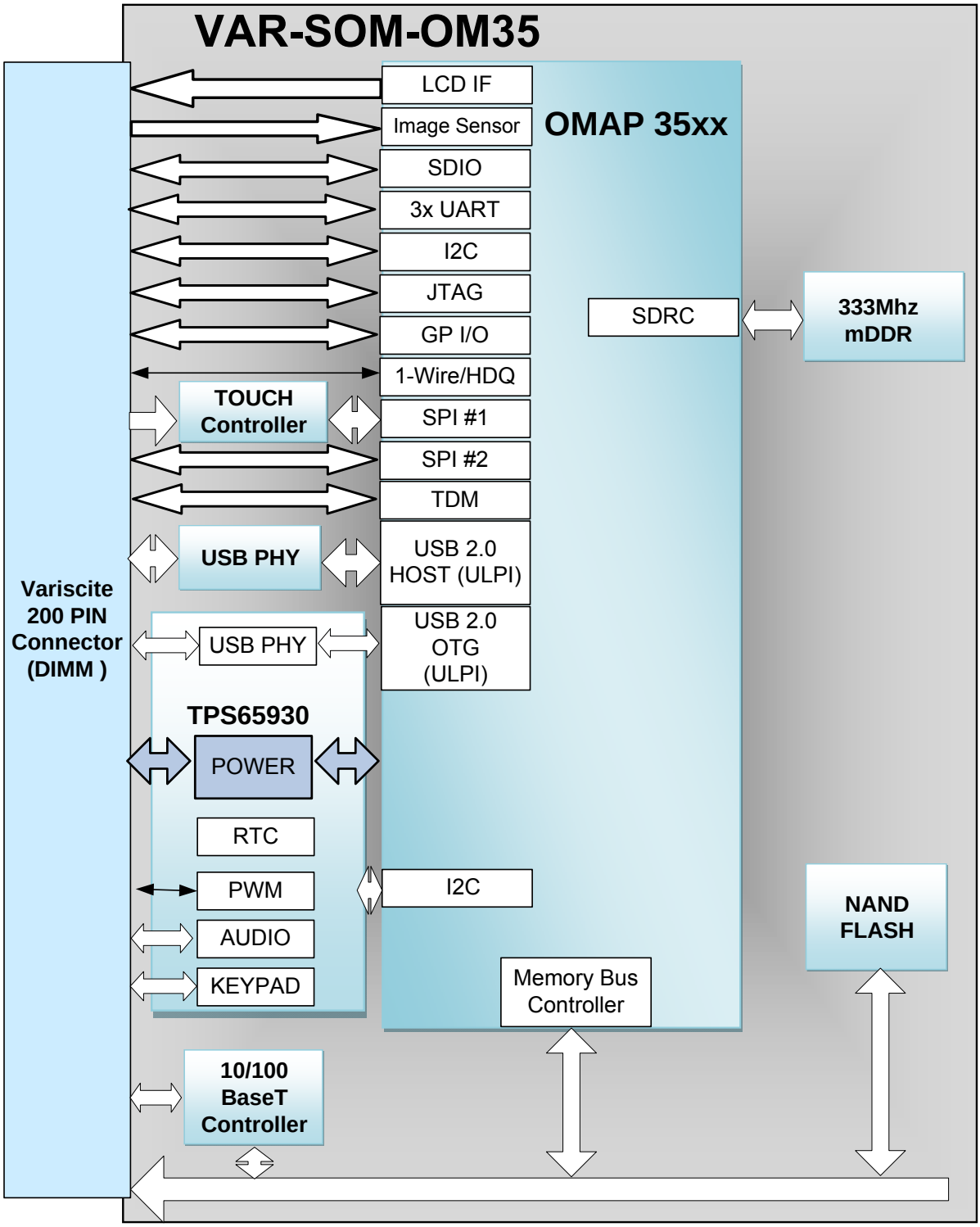
- Windows Embedded CE 6.0 R2 BSP
- Linux BSP based on kernel 2.6.32
- VAR-35xxCustomBoard – evaluation board
  - ✓ Base-Board, compatible with VAR-SOM-OM35
  - ✓ Windows CE 6.0 run-time image
  - ✓ Linux Kernel 2.6.32 sources files
  - ✓ Schematics

Contact support for further information: mailto:support@variscite.com.

1.2 Feature Summary

- Texas Instruments OMAP35xx CPU
  - Up to 720-MHz ARM Cortex™-A8 Core
  - NEON™ SIMD Coprocessor
  - High Performance Image, Video, Audio (IVA2.2™) Accelerator Subsystem (3530 Devices Only)
  - POWERVR SG™ 2D/3D Graphics Accelerator (3530 Device Only)
  - 16kB/16kB Inst/ Data L1 cache
  - 256kB L2 cache
  - Internal 64kB SRAM
- 128-256MB 333MHz DDR SDRAM.
- 256-512Mbytes Flash Disk
- LCD interface. HD Maximum Resolution
- 2 SD card/SDIO/MMC card interface
- Power
  - Single 3.3-4.5V DC-IN power supply.(One lithium-ion cell battery)
  - Typical power consumption: 1W
- RAW image-sensor module interface
- 3 UART ports
- 100Mbit Ethernet controller
- Audio
  - 16-bit linear audio stereo DAC (96, 48, 44.1, and 32 kHz and derivatives)
  - 16-bit linear audio stereo ADC (48, 44.1, and 32 kHz and derivatives)
  - Microphone input
  - Line In and Out
- USB
  - USB 2.0 Host interface.
  - USB 2.0 OTG interface.
- Touch Screen interface
- Keypad interface
- Serial controllers
  - TDM interface (over McBSP1)
  - SPI interface
  - I2C interface
  - 1 – Wire/ HDQ

1.3 Block Diagram



2 HW Components

This chapter shortly describes the VAR-SOM-OM35 HW components.

2.1 Texas Instruments OMAP35xx

2.1.1 Overview

The OMAP35xx family of high-performance applications processors, are based on the enhanced OMAP™ 3 architecture and are integrated on TI's advanced 65-nm process technology.

Note: The OMAP 3 architecture is configured with different sets of features in different devices. This technical reference manual details all of the features available in current and future OMAP35xx devices.

The architecture is designed to provide best-in-class video, image, and graphics processing sufficient to support the following:

- Streaming video
- 2D/3D mobile gaming
- Video conferencing
- High-resolution still image
- Video capture in 2.5G wireless terminals, 3G wireless terminals, and rich multimedia-featured handsets, and high-performance personal digital assistants (PDAs).

This OMAP device also features the M-Shield™ mobile security technology to enable secure e-commerce applications and the replay of copyright-protected digital media content. Security features integrated on the devices support applications designed for:

- Protection against malicious attacks
- M-commerce
- Content protection for recordable media (CPRM)
- Digital rights management (DRM)

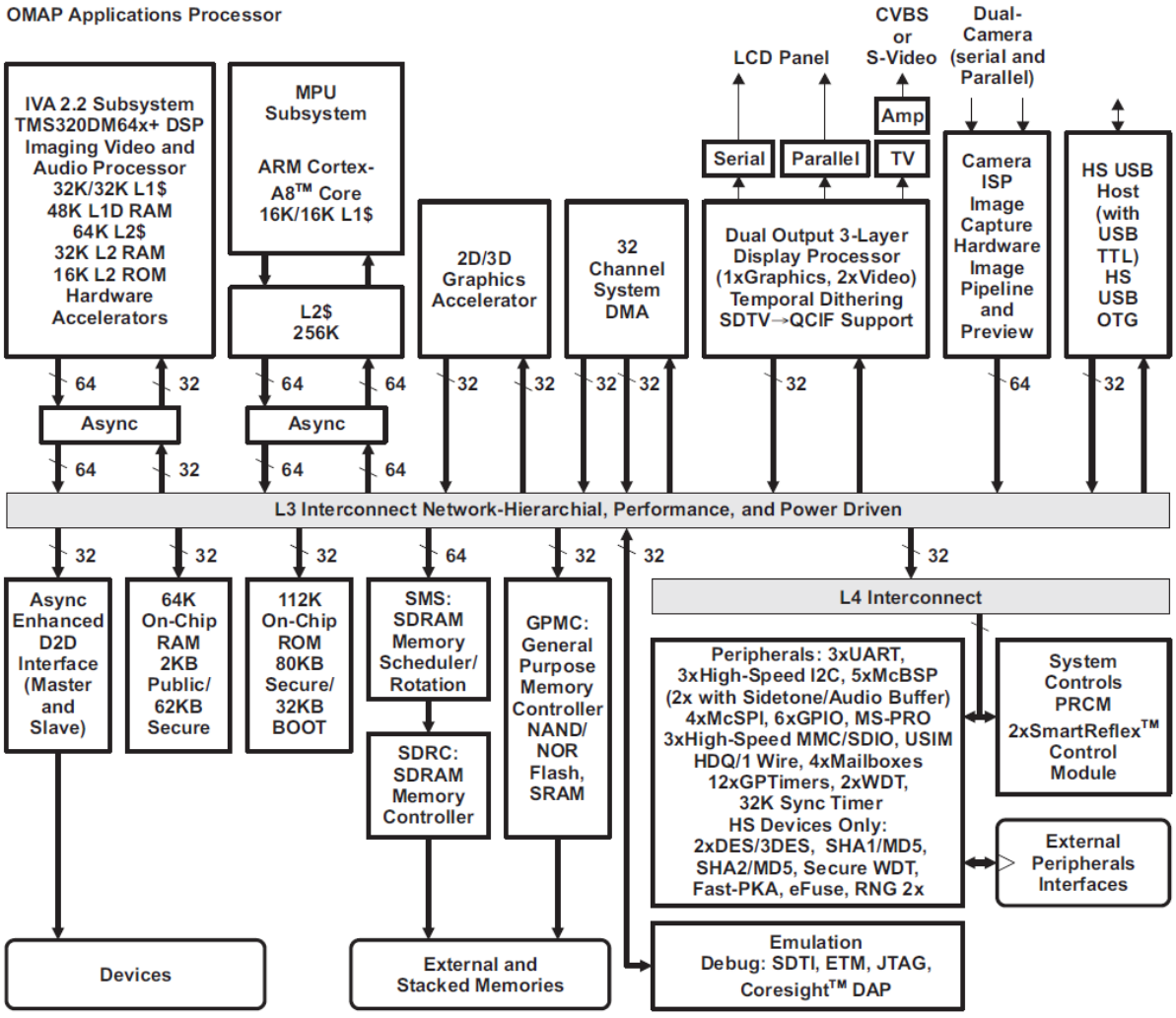
High-security (HS) devices rely on a security scheme based on hardware mechanisms and a secure read-only memory (ROM) code, ensuring that only trusted code can access the secure resources. These resources are in specific regions of memories as well as in peripherals, hardware cryptographic accelerators, and eFuse keys. General-purpose (GP) devices do not include a security feature.

The following subsystems are part of the device:

- Microprocessor unit (MPU) subsystem based on the ARM® Cortex™-A8 microprocessor
- IVA2.2 subsystem with a C64x+ digital signal processor (DSP) core
- SGX subsystem for 2D and 3D graphics acceleration to support display and gaming effects
- Camera image signal processor (ISP) that supports multiple formats and interfacing options connected

Note: IVA2.2 and SGX are not available on all devices.

2.1.2 OMAP 35xx Block Diagram



2.1.3 MPU Subsystem

The MPU subsystem integrates the following modules:

- ARM subchip

  – ARM® Cortex™-A8 core

  – ARM Version 7™ ISA: Standard ARM instruction set + Thumb®-2, Jazelle® RCT Java accelerator, and media extensions

  – NEON™ SIMD coprocessor (VFP lite + media streaming instructions)

- Cache memories

  –Level 1: 16KB instruction and 16KB data—4-way set associative cache, 64 bytes/line

  –Level 2: 256kB.

- Interrupt controller (MPU IN TC) of 96 synchronous interrupt lines
- Asynchronous interface with core logic
- Debug, trace, and emulation features: ICE-Crusher, ETM, ETB modules.

2.1.4 IVA2.2 Subsystem

The device includes a high-performance imaging video and audio (IVA2.2) accelerator based on the Texas Instruments TMS320DMC64x+ VLIW DSP core.

Read TI OMAP documentation for further information.

Note: IVA2.2 is not available on all devices.

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2.1.5 On-Chip Memory

On-chip memory configuration offers memory resources for program and data storage:

- 112KB ROM
- 64KB single-access static random access memory (SRAM)

2.1.6 External Memory Interfaces

The device includes two external memory interfaces:

- General-purpose memory controller (GPMC)
  – NOR flash, NAND flash (with ECC Hamming code calculation), SRAM and Pseudo-SRAM asynchronous and synchronous protocols
  – Flexible asynchronous protocol control for external ASIC or peripheral interfacing
  – 16-bit data, up to 8 chip-selects (CSs)
  – 128M-byte addressable per chip-select, 1G-byte total address space
  – Nonmultiplexed device with limited address (2K bytes)
- SDRAM controller (SDRC)
  – Mobile single data rate (M-SDR) SDRAM and low-power double data rate (LPDDR) SDRAM
  – 16-bit or 32-bit data, 2 chip-selects, configurations for a maximum of 1 G-byte address space per chip-select
  – Work in conjunction with the SDRAM memory scheduler (SMS) companion module

2.1.7 DMA Controllers

- The device embeds one generic DMA controller, the system DMA (sDMA) controller, used for memory-to-memory, memory-to-peripheral, and peripheral-to-memory transfers:
- One read port, one write port
- 32 prioritizable logical channels
- 96 hardware requests
- 256 x 32-bit FIFO dynamically allocable between active channels

2.1.8 Multimedia

The device also embeds three dedicated DMA controllers: enhanced DMA (EDMA), which is embedded in the IVA2.2 subsystem, display DMA, and USB HS DMA.

The device uses the following multimedia accelerators for display and gaming effects as well as high-end imaging and video applications:

- 2D and 3D graphics accelerator (SGX)
  – 2D and 3D graphics and video codecs supported on common hardware
  – Tile-based architecture
  – Universal scalable shader engine (USSE™) multithreaded engine incorporating pixel and vertex shader functionality reducing die area
  – Advanced shader feature set in excess of Microsoft VS3.0, PS3.0, and OGL2.0
  – Industry standard API support Direct3D mobile, OGL-ES 1.1 and 2.0, OpenVG 1.0, OpenMax
  – Fine-grained task switching, load balancing, and power management
  – Programmable high-quality image anti-aliasing
  – Advanced geometry DMA driven operation for minimum CPU interaction
  – Fully virtualized memory addressing for OS operation in a unified memory architecture
  – Advanced and standard 2D operations (that is, vector graphics, BLTs, ROPs, etc.)
  – Programmable video encode and decode support for H.264, H.263, MPEG4 (SP), WMV9, and JPEG

Note: Multimedia accelerators are not available on all devices.

- Camera interface
  – Supports most of the raw image sensors available in the market
  – Includes video processing hardware
  – 12-bit parallel interface supported
  – Pixel clock up to 83 MHz
- Display interface
  – Display controller
  – Color and monochrome displays up to 2048 x 2048 x 24-bpp resolution
  – 256 x 24-bit entries palette in red, green, blue (RGB)
  – 3,375 colors, 15 grayscales
  – Picture-in-picture (overlay), color-space conversion, rotation, color-phase rotation, and resizing support
  – Remote frame buffer interface
  – Liquid-crystal display (LCD) pixel interfaces (MIPI DPI 1.0) and LCD bus interfaces (MIPI DBI 1.0) supported
  – NTSC/PAL video encoder outputs with integrated digital-to-analog converters (DACs) output are supported on CVBS and S-video TV analog output signals
  – Serial display interface implements high-speed differential output buffers to support FlatLink3G™, Mobile CMADS and MIPI DSI 1.0 formats
  – Embedded DMA controller

2.1.9 Peripherals

The device supports a comprehensive set of peripherals to provide flexible and high-speed interfacing and on-chip programming resources. The following table provides a list and description of the peripherals available on the VAR-SOM-OM35 device.

Type	Name	Description
Serial Communication	Multi-channel Buffered	The McBSPs provide a full-duplex direct serial interface between Serial Ports (McBSPs) the device and other devices in a system such as audio and voice codecs and other application chips. McBSP1, McBSP2, and McBSP3 serve as general purpose serial ports while McBSP2 and McBSP3 include additional audio-loopback capability.
	Multi-channel Serial Port	The McSPIs provide a master/slave interface to SPI devices. Interface (McSPI)
	High-speed USB OTG	High-speed USB2.0 OTG controller that offers high-speed data Controller
	HDQ/1-Wire	The HDQ/1-Wire interface supports the Benchmark HDQ protocol and the Dallas Semiconductor 1-Wire protocol.
	Universal Asynchronous	Serial communication interfaces compatible to the industry Receiver/Transmitter standard TL16C550 asynchronous communications element. (UART) UART1 and UART 2 are general serial communication interfaces. UART3 provides additional support for infrared data association (IrDA) and consumer infrared (CIR) communications
	High-speed (HS) I2C	Master/slave I2C high-speed standard interfaces with support for Inter-integrated Circuit standard mode (up to 100K bits/s), fast mode (up to 400K (I2C) Controllers bits/s), and high-speed mode (up to 3.4M bits/s).
Removable Media	Multimedia Card/Secure Digital/Secure Digital IO (MMC/SDIO) Card Interface	MMC memory card, SD memory card, or SDIO cards interface.
Miscellaneous	GP timers	Twelve general-purpose timers
	Watchdog timers	Three watchdog timers (WDTs)
	32-kHz synchronization timer	32-kHz clock timer
	General-purpose input/output (GPIO)	General-purpose input/output pins controlled by six GPIO controllers.
	Mailbox	MPU/IVA2.2 inter-processor communications mailboxes. All six mailboxes are available in chassis mode, however, only two mailboxes are available in stand-alone mode.
	Control module	I/O multiplexing and chip-configuration control.
Security Modules		RNG, Fast PKA, 2xDES/3DES, SHA1/MD5, SHA2/MD5, 2xAES, Secure Watchdog Timer, and universal subscriber identity module (USIM).

2.2 TPS65930 PMIC

The VAR-SOM-OM35 uses the TI TPS65930 companion chip.

The TPS65930 is a power-management IC dedicated for the OMAP35xx. The TPS65930 includes: Power regulators, universal serial bus (USB) high-speed (HS) transceiver, analog-to-digital converter (ADC), real-time clock (RTC) and embedded power control (EPC). In addition, the TPS65930 includes an audio codec with two digital-to-analog converters (DACs) and two ADCs to implement dual voice channels and a stereo downlink channel that can play all standard audio sample rates, through a multiple format inter-integrated sound (I2S™)/time division multiplexing (TDM) interface.

The RTC can be powered by a backup battery when the main supply is not present.

2.3 Memory

2.3.1 333MHZ mDDR

The VAR-SOM-OM35 supports up to 256MB of DDR SDRAM with clock rate of 333MHz.

DDR memory is 32-bit wide

2.3.2 Non volatile storage memory

The VAR-SOM-OM35 supports up to 256MB of SLC NAND flash.

The NAND flash is used for Flash Disk implementation, O.S. run-time-image and the Bootloader (Boot from NAND).

2.4 SMSC LAN9220 Ethernet controller

The LAN9220 is a full-featured, single-chip 10/100 Ethernet controller. The LAN9220 is an IEEE 802.3 10BASE-T and 802.3u 100BASE-TX compliant, and supports HP Auto-MDIX.

Qualified and Suggested Magnetics:

Magnetics listed under “Qualified” title have been tested in order to verify the proper operation with LAN9220 device. Magnetics in “Suggested” category was evaluated on the vendor-supplied datasheet level, but have not been tested.

Qualified Magnetics:

Vendor	Part Number	Package	Cores	Temp	Configuration
Pulse	H1102	16-pin SOIC	4	0 -+70o C	HP Auto-MDX
Halo	TG110-RP55N5	16-pin SOIC	4	0 -+70o C	HP Auto-MDX
Halo	HFJ11-RP26E-L12RL	Integrated RJ45	4	0 -+70o C	HP Auto-MDX POE
Delta	RJSE1R5310A	Integrated RJ45	4	0 -+70o C	HP Auto-MDX

Suggested Magnetics:

Vendor	Part Number	Package	Cores	Temp	Configuration
Pulse	J0011D01B	Integrated RJ45	4	0 -+70o C	HP Auto-MDX
Midcom	TG110-RP55N5	Cardbus	4	0 -+70o C	HP Auto-MDX
Bothhand	HFJ11-RP26E-L12RL	16-pin SOIC	4	0 -+70o C	HP Auto-MDX
Bothhand	RJSE1R5310A	Integrated RJ45	4	0 -+70o C	HP Auto-MDX

3 SOM Connectors

The VAR-SOM-OM35 implements an SODIMM200 standard interface for base board interfacing. The VAR-35xxCustomBoard is equipped with a SODIMM200 slot.

SBC connector signal list:

Pin #	Signal	Type	Description	GPIO #
1	DSS_D1	O	LCD Data	71
2	DSS_D0	O	LCD Data	70
3	DSS_D3	O	LCD Data	73
4	DSS_D2	O	LCD Data	72
5	DSS_D5	O	LCD Data	75
6	DSS_D4	O	LCD Data	74
7	DSS_D7	O	LCD Data	77
8	DSS_D6	O	LCD Data	76
9	DSS_D9	O	LCD Data	79
10	DSS_D8	O	LCD Data	78
11	DSS_D11	O	LCD Data	81
12	DSS_D10	O	LCD Data	80
13	DSS_D13	O	LCD Data	83
14	DSS_D12	O	LCD Data	82
15	DSS_D15	O	LCD Data	85
16	DSS_D14	O	LCD Data	84

17	DSS_D17	O	LCD Data	87
18	CAM_D5	I	ISP Data	104
19	DSS_D19	O	LCD Data	89
20	DSS_D18	O	LCD Data	88
21	DSS_D21	O	LCD Data	91
22	DSS_D20	O	LCD Data	90
23	DSS_D23	O	LCD Data	93
24	DSS_D22	O	LCD Data	92
25	CAM_XCLKA	O	ISP External clock for the image-sensor module	96
26	DSS_HSYNC	O	LCD Horizontal Sync	67
27	MMC1_DAT4	IO	MMC#1 Data 4	126
28	DSS_PCLK	O	LCD Pixel Clock	66
29	UART3_CTS	I	UART#3 CTS	163
30	MMC1_DAT7	IO	MMC#1 Data 7	129
31	UART3_RTS	O	UART#3 RTS	164
32	MMC1_CLKO	O	MMC#1 Clock	120
33	UART3_RX	I	UART#3 RX	165
34	MMC1_DAT6	IO	MMC#1 Data 6	128
35	UART3_TX	O	UART#3 TX	166
36	MMC1_DAT0	IO	MMC#1 Data	122
37	MsSPI2_CLK	O	SPI#2 Clock	178
38	MMC1_DAT1	IO	MMC#1 Data 1	123
39	MsSPI2_SIMO	O	SPI#2 SIMO (TX)	179
40	MMC1_DAT2	IO	MMC#1 Data 2	124
41	MsSPI2_SOMI	I	SPI#2 SOMI (RX)	180
42	MMC1_DAT3	IO	MMC#1 Data 3	125
43	MMC1_CMD	IO	MMC#1 Command	121
44	CAM_D6	I	ISP Data	105
45	DSS_D16	O	LCD Data	86
46	DSS_VSYNC	O	LCD Vertical Sync	68
47	GND			N/A

48	GND			N/A
49	CLK_OUT1	O	General Purpose Clock Out 1	N/A
50	CAM_D4	I	ISP Data	103
51	GND			N/A
52	LB_nCS4	O	Local bus Chip Select 4	55
53	CAM_D7	I	ISP Data	106
54	MMC1_DAT5	O	MMC#1 Data 5	127
55	CAM_D3	I	ISP Data	102
56	CAM_D2	I	ISP Data	101
57	CAM_WEN	I	ISP External write-enable signal	167
58	GND			N/A
59	CAM_PCLK	I	ISP Parallel interface pixel clock	97
60	GND			N/A
61	I2C3_SDA	IO	I2C#3 SDA (data)	185
62	CAM_STROBE	O	ISP Flash strobe control signal	126
63	I2C3_SCL	O	I2C#3 SCL (clock)	184
64	DSS_ACBIAS	O	LCD AC bias/Data enable	69
65	UART2_CTS	I	UART#2 CTS	144
66	MsSPI2_CS0	O	SPI#2 Slave Select 0	181
67	UART2_RTS	O	UART#2 RTS	145
68	CAM_D11	I	ISP Data	110
69	UART2_TX	O	UART#2 TX	146
70	CAM_D10	I	ISP Data	109
71	UART2_RX	I	UART#2 RX	147
72	CAM_D9	I	ISP Data	108
73	TSPX	I	Touch Screen X Plus	N/A
74	CAM_D8	I	ISP Data	107
75	TSPY	I	Touch Screen Y Plus	N/A
76	CAM_VS	IO	ISP Frame trigger input/output signal	95
77	TSMX	I	Touch Screen X Minus	N/A
78	CAM_HS	IO	ISP Line trigger input/output signal	94
79	TSMY	I	Touch Screen Y Minus	N/A

80	CAM_FLD	IO	ISP Field identification input/output signal	98
81	GND			
82	HDQ	IO	HDQ / 1-Wire Line	170
83	GND			
84	UART1_TX	O	UART#1 TX	148
85	SYS_nDMAREQ	I	Local Bus SDMA Request 1	N/A
86	UART1_RTS	O	UART#1 RTS	149
87	LB_CLK	O	Local Bus clock	59
88	UART1_CTS	I	UART#1 CTS	150
89	LB_nCS3	O	Chip Select 3	54
90	UART1_RX	I	UART#1 RX	151
91	MMC1_CD	I	MMC#1 Card Detect	
92	SYS_BOOT5	I	Flash burning switch	N/A
93	CAM_D1	I	ISP Data	100
94	VDD_DDR_EXT		External power supply for DDR. Use only if Deep sleep is required. Consult support for further information.	N/A
95	CAM_D0	I	ISP Data	99
96	VDD_DDR_EXT		External power supply for DDR. Use only if Deep sleep is required. Consult support for further information.	N/A
97	RESET_OUT_N	O	Reset signal to base-board peripherals	N/A
98	McBSP1_CLKX	IO	McBSP#1 Transmit clock	162
99	nEN_USB_PWR	O	USB 2.0 Host Power Enable	N/A
100	McBSP1_FSX	IO	McBSP#1 Transmit frame	161
101	HOST_nOC	I	USB 2.0 Host Over Current indicator.	N/A
102	McBSP1_DR	I	McBSP#1 Receive serial data	159
103	USBHOST_DP	IO	USB 2.0 Host Data Positive	N/A
104	McBSP1_DX	(I)O	McBSP#1 Transmit serial data	158
105	USBHOST_DN	IO	USB 2.0 Host Data Negative	N/A
106	McBSP1_FSR	IO	McBSP#1 Receive Frame	157
107	USBHOST_VBUS	I	USB 2.0 Host VBUS 5v indicator	N/A

108	McBSP1_CLKR	IO	McBSP#1 Receive clock	156
109	GPIO28	IO	GPIO#28	28
110	VBAT	I	VAR-SOM-OM35 single DC-IN supply voltage. Voltage range: 3.3 – 4.5V	N/A
111	GPIO27	IO	GPIO#27	27
112	VBAT	I	VAR-SOM-OM35 single DC-IN supply voltage. Voltage range: 3.3 – 4.5V	N/A
113	GND			
114	VBAT	I	VAR-SOM-OM35 single DC-IN supply voltage. Voltage range: 3.3 – 4.5V	N/A
115	GND			N/A
116	VBAT	I	VAR-SOM-OM35 single DC-IN supply voltage. Voltage range: 3.3 – 4.5V	N/A
117	VCC18	O	Output Voltage. Up to 200ma	N/A
118	USB_OTG_VBUS	I	USB 2.0 OTG VBUS indicator	N/A
119	GPIO26	IO	GPIO#26	26
120	USB_OTG_DP	IO	USB 2.0 On-The-Go Data Positive	N/A
121	PWRON	I	Wake-up signal to PMIC	N/A
122	USB_OTG_DN	IO	USB 2.0 On-The-Go Data Negative	N/A
123	REGEN	O	Regulator Enable	
124	USB_OTG_ID	I	USB OTG Host/Client ID	N/A
125	LB_RE_OE_N	O	Output enable (active low). Also used as read enable (active low) for NAND protocol memories.	N/A
126	RTC_BACKUP	I	Coin battery input for RTC backup	N/A
127	RESET_IN_N	I	Hardware Reset	N/A
128	LB_IO_A9	O	Local bus address 9	42
129	LB_IO_10	IO	Local bus data	N/A
130	LB_IO_A8	O	Local bus address 8	41
131	LB_IO_9	IO	Local bus data	N/A
132	LB_IO_11	IO	Local bus data	N/A
133	LB_IO_8	IO	Local bus data	N/A
134	LB_IO_14	IO	Local bus data	N/A
135	LB_IO_7	IO	Local bus data	N/A
136	LB_IO_15	IO	Local bus data	N/A

137	LB_IO_6	IO	Local bus data	N/A
138	LB_IO_12	IO	Local bus data	N/A
139	LB_IO_5	IO	Local bus data	N/A
140	LB_IO_13	IO	Local bus data	N/A
141	LB_IO_4	IO	Local bus data	N/A
142	LB_IO_A1	O	Local bus address 1	34 *
143	LB_IO_3	IO	Local bus data	N/A
144	LB_IO_A2	O	Local bus address 2	35 *
145	LB_IO_2	IO	Local bus data	N/A
146	LB_IO_A3	O	Local bus address 3	36 *
147	LB_IO_1	IO	Local bus data	N/A
148	LB_WAIT0	I	Local bus wait	N/A
149	LB_IO_0	IO	Local bus data	N/A
150	LB_IO_A4	O	Local bus address 4	37 *
151	GND			N/A
152	LB_CLE	O	Local bus Output enable for static memory, muxed with CLE	N/A
153	LB_IO_A5	O	Local bus address 5	38 *
154	LB_ nADV_ALE	O	Local bus Address Latch Enable, muxed with Address Valid	N/A
155	LB_IO_A6	O	Local bus address 6	39 *
156	GND			N/A
157	LB_IO_A7	O	Local bus address 7	40 *
158	VCC33	O	Output voltage for general use. Up to 200ma	N/A
159	GND			N/A
160	LB_WE_N	O	Local bus Write enable (active low)	N/A
161	LINK_LED	O	Ethernet Link LED	N/A
162	GND			
163	SPEED_LED	O	Ethernet Speed LED	N/A
164	MMC2_CLK	IO	MMC2 Clock	130
165	ETH_TXN	O	Ethernet TX Negative	N/A
166	MMC2_CMD	IO	MMC2 CMD	131

167	ETH_TXP	O	Ethernet TX Positive	N/A
168	MMC2_DAT0	IO	MMC2 Data 0	132
169	VCC33A	O	3.3V Output to Ethernet Magnetics	N/A
170	MMC2_DAT1	IO	MMC2 Data 1	133
171	ETH_RXN	I	Ethernet RX Negative	N/A
172	MMC2_DAT2	IO	MMC2 Data 2	134
173	ETH_RXP	I	Ethernet RX Positive	N/A
174	MMC2_DAT3	IO	MMC2 Data 3	135
175	KPD.R5	IO	Keypad Row 5	N/A
176	KPD.R4	IO	Keypad Row 4	N/A
177	KPD.C0	IO	Keypad Column 0	N/A
178	KPD.R3	IO	Keypad Row 3	N/A
179	KPD.C1	IO	Keypad Column 1	N/A
180	KPD.R2	IO	Keypad Row 2	N/A
181	KPD.C2	IO	Keypad Column 2	N/A
182	KPD.R1	IO	Keypad Row 1	N/A
183	KPD.C3	IO	Keypad Column 3	N/A
184	KPD.R0	IO	Keypad Row 0	N/A
185	KPD.C4	IO	Keypad Column 4	N/A
186	CODEC_AUXADC1	I	AUX ADC in 1	N/A
187	KPD.C5	IO	Keypad Column 5	N/A
188	CODEC_AUXADC2	I	AUX ADC in 2	N/A
189	PWM0	O	PWM#0 signal	N/A
190	HP_LOUT	O	Pre-amped Headphones Left	N/A
191	MMC2_DIR_CMD	O	MMC2 CMD line direction. For External 1.8v -> 3.3v transceiver.	138
192	HP_ROUT	O	Pre-amped Headphones Right	N/A
193	MMC2_DIR_DAT_0	O	MMC2 Data lines direction. For External 1.8v -> 3.3v transceiver.	136
194	CODEC_LINEIN	I	Audio Line In	N/A
195	MMC2_CLKIN	I	MMC2 clock-in loopback	N/A
196	MIC_BIAS	I	Microphone Bias	N/A

197	MIC_N	I	Microphone Negative	N/A
198	AUD_GND		Audio Ground	N/A
199	MIC_P	I	Microphone Positive	N/A
200	AUD_GND		Audio Ground. Connect to GND if Audio not used!	N/A

- LB_IO Bus can be used only if Ethernet controller not assembled

4 Interfaces

4.1 Display interface

4.1.1 LCD Subsystem Interface

Supported display modes:

– Color and monochrome displays up to 2048 x 2048 x 24-bpp resolution
– 256 x 24-bit entries palette in red, green, blue (RGB)

LCD interface signals:

Signal	Pin #	Type	Description
DSS_PCLK	28	O	LCD Pixel clock
DSS_HSYNC	26	O	LCD Horizontal Sync
DSS_VSYNC	46	O	LCD Vertical Sync
DSS_ACBIAS	64	O	LCD AC bias/Data enable
DSS_D0	2	O	LCD Data line
DSS_D1	1	O	LCD Data line
DSS_D2	4	O	LCD Data line
DSS_D3	3	O	LCD Data line
DSS_D4	6	O	LCD Data line
DSS_D5	5	O	LCD Data line
DSS_D6	8	O	LCD Data line
DSS_D7	7	O	LCD Data line
DSS_D8	10	O	LCD Data line
DSS_D9	9	O	LCD Data line
DSS_D10	12	O	LCD Data line
DSS_D11	11	O	LCD Data line
DSS_D12	14	O	LCD Data line
DSS_D13	13	O	LCD Data line
DSS_D14	16	O	LCD Data line
DSS_D15	15	O	LCD Data line
DSS_D16	45	O	LCD Data line
DSS_D17	17	O	LCD Data line
DSS_D18	20	O	LCD Data line
DSS_D19	19	O	LCD Data line
DSS_D20	22	O	LCD Data line
DSS_D21	21	O	LCD Data line
DSS_D22	24	O	LCD Data line
DSS_D23	23	O	LCD Data line

4.2 Audio

The VAR-SOM-OM35 uses the TPS65930 built-in Audio codec

Audio signals:

Signal	Pin #	Type	Description
HP_LOUT	190	O	Pre-amped Headphones, Left out
HP_ROUT	192	O	Pre-amped Headphone, Right Out
CODEC_AUXADC1	186	I	Auxiliary ADC IN 1
CODEC_AUXADC2	188	I	Auxiliary ADC IN 2
CODEC_LINEIN	194	I	Line IN
MIC_BIAS	196	I	Mic Bias Voltage
MIC_N	197	I	Mic Negative In
MIC_P	199	I	Mic Positive In
AUD_GND	198, 200		Audio Ground. Connect to GND if Audio not used!

4.3 Camera Interface

The VAR-SOM-OM35 uses the OMAP3 Camera interface.

Image sensor:

- Interface with various image sensors:
  - R, G, B primary colors
  - Ye, Cy, Mg, G complementary colors
- Support for electronic rolling shutter (ERS) and global-release reset shutters

· **Parallel interface:** The parallel interface supports two modes:

- **SYNC mode:** In this mode, the image-sensor module provides horizontal and vertical synchronization signals to the parallel interface, along with the pixel clock. This mode works with 8-, 10-, 11-, and 12-bit data (above 10-bit RAW data, the processing pipe cannot be used; data must be transferred to memory). SYNC mode supports progressive and interlaced image-sensor modules.
- **ITU mode:** In this mode, the image-sensor module provides an ITU-R BT 656-compatible data stream. The horizontal and vertical synchronization signals are not provided to the interface. Instead, the data stream embeds start-of-active (SAV) and end-of-active video (EAV) synchronization code. This mode works in 8- and 10-bit configurations. It supports only progressive image-sensor modules.

Note:

- Up to 8-bit data at 130 MHz can be transferred to memory.

- Up to 10-bit data at 75 MHz can be processed by the image pipeline or transferred to memory.
- Up to 12-bit data at 75 MHz can be transferred to memory as is, or after processing inside the CCDC. It can also be internally converted to 10-bit data for full processing.

VAR-SOM-OM35 ISP signals:

Signal	Pin #	Type	Description
CAM _PCLK	59	I	Parallel interface pixel clock
CAM _HS	78	IO	Line trigger input/output signal
CAM _VS	76	IO	Frame trigger input/output signal
CAM _FLD	80	IO	Field identification input/output signal
CAM _WEN	57	I	External write-enable signal
CAM _XCLKA	25	O	External clock for the image-sensor module
CAM _STROBE	62	O	Flash strobe control signal
CAM_D0	95	I	ISP Data
CAM _D1	93	I	ISP Data
CAM _D2	56	I	ISP Data
CAM _D3	55	I	ISP Data
CAM _D4	50	I	ISP Data
CAM _D5	18	I	ISP Data
CAM _D6	44	I	ISP Data
CAM _D7	53	I	ISP Data
CAM _D8	74	I	ISP Data
CAM _D9	72	I	ISP Data
CAM _D10	70	I	ISP Data
CAM _D11	68	I	ISP Data

4.4 Ethernet

The VAR-SOM-OM35 provides one full-featured 10/100 Mbit Ethernet port using the SMSC LAN9220/1 Ethernet controller.

LAN9221 offers higher data throughput.

Features:

- Fully compliant with IEEE 802.3/802.3u standards
- Integrated Ethernet MAC and PHY
- 10BASE-T and 100BASE-TX support
- Full- and Half-duplex support
- Full-duplex flow control
- Backpressure for half-duplex flow control
- Preamble generation and removal
- Automatic 32-bit CRC generation and checking
- Automatic payload padding and pad removal
- Auto-negotiation
- Automatic polarity detection and correction

VAR-SOM-OM35 Ethernet Controller signals:

Signal	Pin #	Type	Description
ETH_TXN	165	O	Transmit Negative
ETH_TXP	167	O	Transmit Positive
ETH_RXN	171	I	Receive Negative
ETH_RXP	173	I	Receive Positive
LINK_LED	161	O	Activity Indicator
LINK_SPEED	163	O	Speed Indicator
VCC33A	169	O	3.3 V Output to Ethernet Magnetics

4.5 UARTs

The VAR-SOM-OM35 has 3 UART ports.

Each UART includes a programmable baud-rate generator. Each port supports baud rates up to 3.6Mbits.

Receive and transmit FIFO fill and drain operations can be done using programmed IO or DMA transfers. To minimize CPU overhead for UART communications, device driver software can setup interrupts and DMA for data transfers to/from memory.

All three UARTs support the 16550A and 167502 functions.

VAR-SOM-OM35 UART1 signals:

Signal	Pin #	Type	Description
UART1_TX	84	O	UART Transmit
UART1_RX	90	I	UART Receive
UART1_RTS	86	O	UART HW Flow Control RTS
UART1_CTS	88	I	UART HW Flow Control CTS

VAR-SOM-OM35 UART2 signals:

Signal	Pin #	Type	Description
UART2_TX	69	O	UART Transmit
UART2_RX	71	I	UART Receive
UART2_RTS	67	O	UART HW Flow Control RTS
UART2_CTS	65	I	UART HW Flow Control CTS

VAR-SOM-OM35 UART3 signals:

Signal	Pin #	Type	Description
UART3_TX	35	O	UART Transmit
UART3_RX	33	I	UART Receive
UART3_RTS	31	O	UART HW Flow Control RTS
UART3_CTS	29	I	UART HW Flow Control CTS

4.6 USB 2.0

4.6.1 USB 2.0 Host

The VAR-SOM-OM35 uses the OMAP3 USB 2.0 Host controller.

- The EHCI controller, based on the Enhanced Host Controller Interface (EHCI) specification for USB Release 1.0, is in-charge of high-speed traffic (480M bit/s), over the ULPI/UTMI interface

Note:
- USB1.1 devices can be connected to the USB2.0 host port only through a USB2.0 Hub.
- USB 1.1 devices can be connected directly to the USB OTG port.

VAR-SOM-OM35 USB 2.0 Host signals:

Signal	Pin #	Type	Description
USBHOST_DP	103	IO	USB Host Data Positive
USBHOST_DN	105	IO	USB Host Data Negative
USBHOST_VBUS	107	I	USB Host VBUS 5V indicator
HOST_nOC	101	I	USB Host over-current indicator
nEN_USB_PWR	99	O	USB 2.0 Host Power Enable

4.6.2 USB 2.0 On-The-Go

The VAR-SOM-OM35 uses the OMAP3 USB 2.0 OTG controller

Features:
- Supports USB 2.0 peripheral at High Speed (480 Mbps) and Full Speed (12 Mbps)
- Supports USB 2.0 host at High Speed (480 Mbps), Full Speed (12 Mbps), and Low Speed (1.5 Mbps)
- Operates either as the function controller of a high-/full-speed USB peripheral or as the host/peripheral in point-to-point or multipoint communications with other USB functions
- Complies the USB 2.0 standard for high-speed (480 Mbps) functions and with the on-the-go (OTG) supplement (Revision 1.0a)
- Each endpoint can support all transfer types (control, bulk, interrupt, and isochronous)
- Supports USB extensions for Session Request (SRP) and Host Negotiation (HNP)
- Supports suspend/resume and remote wakeup
- Supports high-bandwidth Isochronous and Interrupt Transfers
- Supports 15 Transmit and 15 Receive endpoints in addition to control endpoint 0
- Each endpoint has its own FIFO, with the following properties:
    - Implemented within a single, 16K-byte internal RAM

  - Can be dynamically sized by software
  - Can be configured to hold multiple packets (up to 8192 bytes per FIFO)
  - can be accessed either by direct access of by DMA controller
- Software connect/disconnect option for peripheral
- Performs all transaction scheduling in hardware

VAR-SOM-OM35 USB 2.0 OTG signals:

Signal	Pin #	Type	Description
USB_OTG_DN	122	IO	USB OTG Data Negative
USB_OTG_DP	120	IO	USB OTG Data Positive
USB_OTG_VBUS	118	I	USB OTG VBUS indicator
USB_OTG_ID	124	I	USB OTG nHost / Client ID Low : Host mode High: Client

TPS65930 PMIC supplies maximum of 100ma on USB_OTG_VBUS , therefore, external LDO is required in host mode.

- USB_OTG_VBUS functionality:

  Client mode: used as an indication of host presence.
  Host mode: not used.

4.7 McBSP

The multi-channel buffered serial port (McBSP) provides a full-duplex direct serial interface between the device and other devices in a system such as audio and voice codecs .

McBSP signals:

Signal	Pin #	Type	Description
McBSP1_CLKX	98	IO	McBSP Transmit Clock
McBSP1_FSX	100	IO	McBSP Transmit Frame Synchronization
McBSP1_DR	102	I	McBSP Receive Serial Data
McBSP1_DX	104	(I)O	McBSP Transmit Serial Data
McBSP1_FSR	106	IO	McBSP Receive Frame Synchronization
McBSP1_CLKR	108	IO	McBSP Receive Clock

4.8 SPI

The McSPI ports supports the following main features:

- Serial clock with programmable frequency, polarity, and phase for each channel
- Wide selection of SPI word lengths ranging from 4 bits to 32 bits
- Up to four master channels or single channel in slave mode
- Master multichannel mode:
    - Full duplex/half duplex
    - Transmit-only/receive-only/transmit-and-receive modes
    - Flexible I/O port controls per channel
    - Two direct memory access (DMA) requests (read/write) per channel
- Single interrupt line for multiple interrupt source events
- Power management through wake-up capabilities
- Enable the addition of a programmable start-bit for SPI transfer per channel (start-bit mode)
- Support start-bit write command
- Support start-bit pause and break sequence
- 64 bytes built-in FIFO available for a single channel

VAR-SOM-OM35 MsSPI2 signals:

Signal	Pin #	Type	Description
MsSPI2_CLK	37	IO	MsSPI2 Clock
MsSPI2_SIMO	39	IO	MsSPI2 SIMO Signal
MsSPI2_SOMI	41	IO	MsSPI2 MISO Signal
MsSPI2_CS0	66	IO	MsSPI2 Chip Select 0 Signal

4.9 I2C

The I2C controller can be configured as a slave or master.

VAR-SOM-OM35 I2C3 signals:

Signal	Pin #	Type	Description
I2C3_SCL	63	IO	I2C3 I^2C Clock. Requires 4k pull-up to 1.8v
I2C3_SDA	61	IO	I2C3 I^2C Data. Requires 4k pull-up to 1.8v

4.10 HDQ/1-Wire

The HDQ/1-Wire module implements the hardware protocol of the master functions of the Benchmark HDQ and the Dallas Semiconductor 1-Wire® protocols. These protocols use a single wire for communication between the master (HDQ/1-Wire controller) and the slave (HDQ/1-Wire external compliant device).

VAR-SOM-OM35 1-Wire / HDQ signals:

Signal	Pin #	Type	Description
HDQ	82	IO	HDQ / 1-Wire IO Signal

4.11 SD / MMC

The VAR-SOM-OM35 has two SD / MMC interfaces

The MMC/SD/SDIO host controllers deal with MMC/SD/SDIO protocol at transmission level, data packing, adding cyclic redundancy checks (CRC), start/end bit, and checking for syntactical correctness.

The application interface can send every MMC/SD/SDIO command and either poll for the status of the adapter or wait for an interrupt request, which is sent back in case of exceptions or to warn of end of operation.

The application interface can read card responses or flag registers. It can also mask individual interrupt sources. All these operations can be performed by reading and writing control registers. The MMC/SD/SDIO host controller also supports two DMA channels.

MMC1 signals (Up to 8 data bits):

Signal	Pin #	Type	Description
MMC1_DAT0	36	IO	MMC1 Data
MMC1_DAT1	38	IO	MMC1 Data
MMC1_DAT2	40	IO	MMC1 Data
MMC1_DAT3	42	IO	MMC1 Data
MMC1_DAT4	27	IO	MMC1 Data
MMC1_DAT5	54	IO	MMC1 Data
MMC1_DAT6	34	IO	MMC1 Data
MMC1_DAT7	30	IO	MMC1 Data
MMC1_CLKO	32	O	MMC Clock
MMC1_CMD	43	O	MMC command
MMC1_CD	91	I	MMC Card Detect

MMC2 signals (SD Card / SDIO 4 data bits max):

- Automatic Card detection not included in BSP
- 3.3v Devices require external transceiver. Consult support for 3.3v devices.

Signal	Pin #	Type	Description
MMC2_DAT0	168	IO	MMC2 Data
MMC2_DAT1	170	IO	MMC2 Data
MMC2_DAT2	172	IO	MMC2 Data
MMC2_DAT3	174	IO	MMC2 Data
MMC2_CLK	164	O	MMC2 Clock
MMC2_CMD	166	O	MMC2 command
MMC2_DIR_CMD	174	IO	MMC2 CMD line direction. For External 1.8v -> 3.3v transceiver.

MMC2_DIR_DAT_0	164	O	MMC2 Data lines direction. For External 1.8v -> 3.3v transceiver.
MMC2_CMD_CLKING	166	O	MMC2 clock-in loopback

4.12 PWM

The VAR-SOM-OM35 outputs PWM line from the TPS65930 Companion Chip.

Signal	Pin #	Type	Description
PWM0	189	O	pulse width modulation

PWM outputs from the OMAP processor (Not Supported by default BSP):

Signal	Pin #	Type	Description
MsSPI2_SIMO	39	IO	MsSPI2 SIMO Signal
MsSPI2_SOMI	41	IO	MsSPI2 MISO Signal
MsSPI2_CS0	66	IO	MsSPI2 Chip Select 0 Signal

4.13 Local Bus

The general-purpose memory controller (GPMC) is used to interfacing external memory devices:

- SRAMs
- Asynchronous, synchronous, and page mode (only available in non-muxed mode) burst NOR flash devices
- NAND flash
- Pseudo-SRAM devices

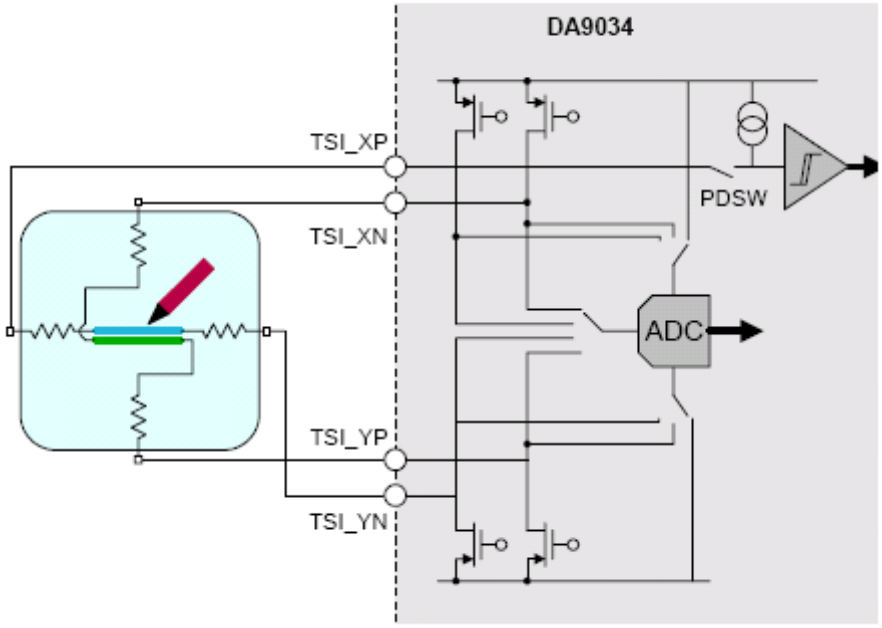
VAR-SOM-OM35 Local bus signals:

Signal	Pin #	Type	Description
LB_IO_0	149	IO	Local Bus Data
LB_IO_1	147	IO	Local Bus Data
LB_IO_2	145	IO	Local Bus Data
LB_IO_3	143	IO	Local Bus Data
LB_IO_4	141	IO	Local Bus Data
LB_IO_5	139	IO	Local Bus Data
LB_IO_6	137	IO	Local Bus Data
LB_IO_7	135	IO	Local Bus Data
LB_IO_8	133	IO	Local Bus Data
LB_IO_9	131	IO	Local Bus Data
LB_IO_10	129	IO	Local Bus Data
LB_IO_11	132	IO	Local Bus Data
LB_IO_12	138	IO	Local Bus Data
LB_IO_13	140	IO	Local Bus Data
LB_IO_14	134	IO	Local Bus Data
LB_IO_15	136	IO	Local Bus Data
LB_IO_A1	142	O	Local Bus Address
LB_IO_A2	144	O	Local Bus Address
LB_IO_A3	146	O	Local Bus Address
LB_IO_A4	150	O	Local Bus Address
LB_IO_A5	153	O	Local Bus Address
LB_IO_A6	155	O	Local Bus Address
LB_IO_A7	157	O	Local Bus Address
LB_IO_A8	130	O	Local Bus Address
LB_IO_A9	128	O	Local Bus Address
LB_CLE	152	O	Local Bus CLE
LB_nADV_ALE	154	O	Local Bus Address latch enables muxed with Local bus address valid
LB_WE_N	160	O	Local Bus Write enable (active low)
LB_RE_OE_N	125	O	Output enable (active low). Also used as read enable

LB_WAIT0	148	I	Local Bus Wait
LB_CLK	87	IO	Local Bus Clock
LB_nCS3	89	O	Local Bus Chip Select 3
LB_nCS4	52	O	Local Bus Chip Select 4
SYS_nDMAREQ	85	I	Local Bus SDMA Request 1

4.14 Touch Screen

- Compatible with 4-wire resistive Touch Screens
- Pen-detection and nIRQ generation
- Supports several schemes of measurement averaging to filter noise
- Maximum X & Y sample rate (without averaging): 5 kHz



The VAR-SOM-OM35 outputs Touch Screen Controller signals:

Signal	Pin #	Type	Description
TSPX	73	Analog	TSI interface X Plus
TSMY	75	Analog	TSI interface Y Minus
TSMX	77	Analog	TSI interface X Minus
TSPY	79	Analog	TSI interface Y Plus

4.15 Keypad

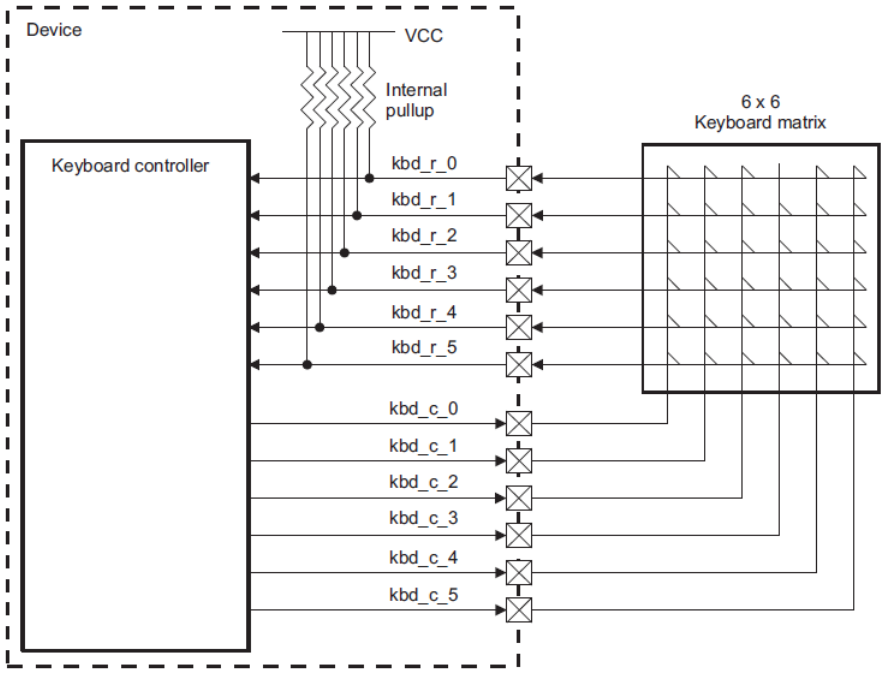
The VAR-SOM-OM35 uses the TPS65930 keypad controller.

When a key button of the keyboard matrix is pressed, the corresponding row and column lines are shorted. To allow key press detection, all input pins (KBR) are pulled up to VCC and all output pins (KBC) are driven to a low level.

Any action on a button generates an interrupt to the sequencer.

The decoding sequence is written to allow detection of simultaneous press actions on several key buttons. The keyboard interface can be used with a smaller keyboard area than 6 ´ 6. To use a 3 ´ 3 keyboard, KBR(4) and KBR(5) must be tied high to prevent any scanning process distribution.

Block Diagram



VAR-SOM-OM35 Touch Screen Controller signals:

Signal	Pin #	Type	Description
KPD.R0	184	I	Keypad Row
KPD.R1	182	I	Keypad Row
KPD.R2	180	I	Keypad Row
KPD.R3	178	I	Keypad Row
KPD.R4	176	I	Keypad Row
KPD.R5	175	I	Keypad Row
KPD.C0	177	I	Keypad Column

KPD.C1	179	I	Keypad Column
KPD.C2	181	I	Keypad Column
KPD.C3	183	I	Keypad Column
KPD.C4	185	I	Keypad Column
KPD.C5	187	I	Keypad Column

4.16 JTAG

The VAR-SOM-OM35 has a dedicated JTAG connector.

Signal	Pin #	Type	Description
JTAG_TDO	1		
JTAG_EMU1	2		
JTAG_nTRST	3		
JTAG_EMU0	4		
JTAG_TMS	5		
JTAG_RTCK	6		
JTAG_TDI	7		
JTAG_TCK	9		
GND	10		

4.17 Boot Option

The Boot option signal configures the boot sequence of the OMAP35xx processor. Use this signal to burn the Bootloader on NAND Flash.

VAR-SOM-OM35 boot signal:

Signal	Pin #	Type	Description
SYS_BOOT5	92	I	System Boot Option 5 [Low – Burn flash]

4.18 General Purpose IOs

Most of the SOM's IO pins can be used as GPIOs.

See Chapter 3 for a complete SBC connector signal list and GPIO multiplexing.

The following pins can be used as GPIOs only.

Signal	Pin #	Type	Description
GPIO26	119	IO	General Purpose IO
GPIO27	111	IO	General Purpose IO
GPIO139	164	IO	General Purpose IO
GPIO131	166	IO	General Purpose IO
GPIO132	168	IO	General Purpose IO
GPIO133	170	IO	General Purpose IO
GPIO134	172	IO	General Purpose IO
GPIO135	174	IO	General Purpose IO

4.19 General System signals

Signal	Pin #	Type	Description
RESET_IN_N	127	I	Hardware Reset
PWRON	121	I	Wake-up signal to PMIC Leave n.c. if unused.
RESET_OUT_N	97	O	Reset Signal to Base-Board Peripherals
CLK_OUT1	49	O	General Purpose Clock Out

4.20 RTC

VAR-SOM-OM35 has an on-board RTC clock which keeps running as long as RTC_BACKUP is above 2.5v.

RTC_BACKUP provides voltage to VRTC domain in TPS6930 PMIC.
TPS65930 can be configured to charge Li-ion RTC backup battery.

4.21 Power supply pins

VAR-SOM-OM35 power supply pins:

Signal	Pin #	Type	Description
VBAT	110	I	VAR-SOM-OM35 single DC-IN supply voltage. Voltage range: 3.3 – 4.5V
VBAT	112	I	
VBAT	114	I	
VBAT	116	I	
VCC33	158	O	3.3V Output, Up to 200ma
VCC33A	169	O	3.3 V Output to Ethernet Magnetics
VIO	117	O	1.8V Output, up to 200ma
REGEN	123	O	External Regulators Enable
RTC_BACKUP	126	I	RTC backup battery power supply

VAR-SOM-OM35 Ground pins:

Signal	Pin #	Type	Description
GND	47		Digital Ground
GND	48		Digital Ground
GND	51		Digital Ground
GND	58		Digital Ground
GND	60		Digital Ground
GND	81		Digital Ground
GND	83		Digital Ground
GND	113		Digital Ground
GND	115		Digital Ground
GND	151		Digital Ground
GND	156		Digital Ground
GND	159		Digital Ground
GND	162		Digital Ground

5 Operational Characteristics

Power supplies	Min	Max
Main Power supply, DC-IN	3.3v	4.5v
RTC Backup battery voltage	2.5v	3.2
LCD interface output I/O level	1.8v	
UART1, UART2 , UAR3 I/O level	1.8v	
Camera Interface I/O level	1.8v	
Local Bus interface I/O level	1.8v	
SPI, McBSP I/O level	1.8v	
SD / MMC signals	1.8v / 3v	
KeyPad Signals	1.8v	
HOST_nOC	1.8v	

Power consumption:

Power supplies	Min	Max
Main Power supply, DC-IN @ 3.7v	4ma	400ma

- Consult Technical Support for O.S support for deep sleep.

6 Absolute maximum Characteristics

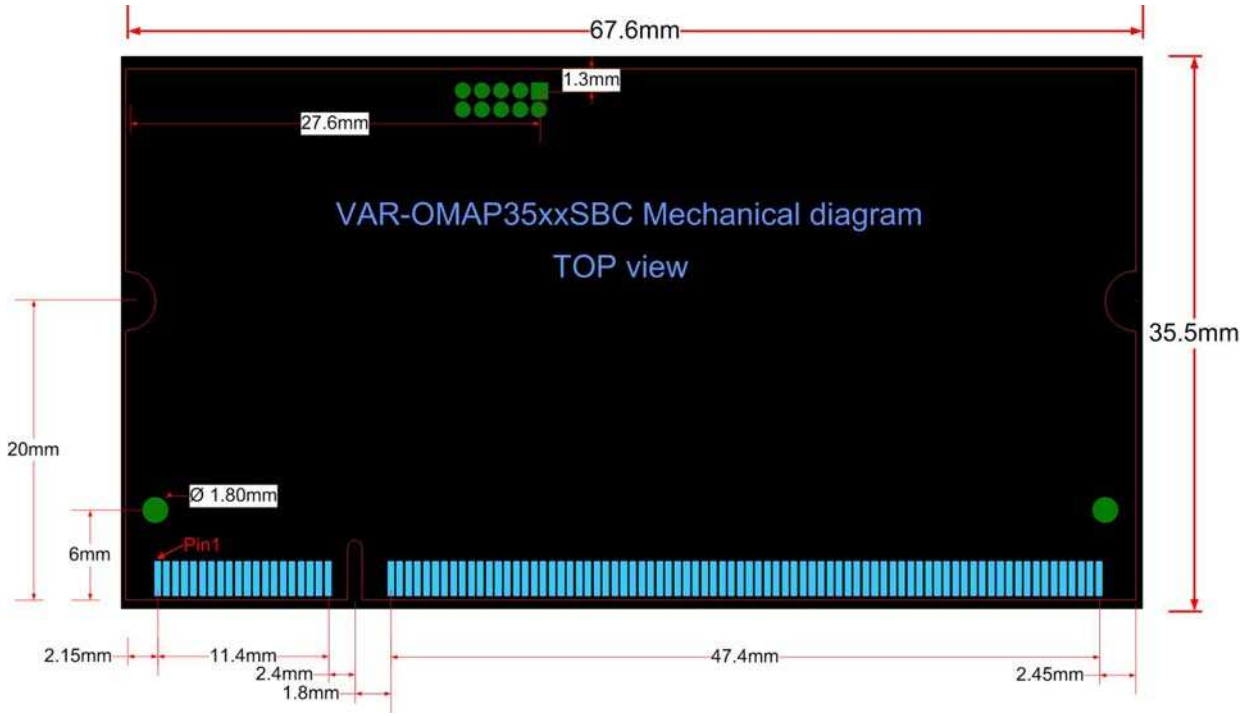
Power supplies	**Min**	**Max**
Main Power supply, DC-IN	-0.3V	5.5V
3.3V output supply		200ma
VIO 1.8v power output		200ma

7 Environmental specifications

	Min	Max
Commercial operating temperature range	0^0C	+70^0C
Extended operating temperature range	-25^0C	+85^0C
MTBF	100000hrs >	

Shock resistance	50G / 20 ms	
Vibration	20G / 0 - 600 Hz	

8 Mechanical drawings



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11 Contact information

Headquarters:

Variscite LTD
60 Medinat Hayehudim st.
P.O.B 12598
46722, Israel

Tel: +972 (9) 9562910
Fax: +972 (9) 9589477

Sales: sales@variscite.com
Technical support: support@variscite.com

Website: www.variscite.com