VARISCITE LTD.

VAR-SOM-OM37Datasheet

Texas Instruments DM/AM 37xx based System-On-Module

VARISCITE LTD.

VAR-SOM-OM37 Data Sheet

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Revision History

Revision	Date	Notes
1.0	01/07/2010	Initial
1.0.1	14/11/2010	USB analog inputs electrical characteristics
1.0.2	18/11/2010	DM3730 -> SOMDIMM 200 mapping
1.0.3	06/12/2010	GPIO limitations on CAM_x signals
1.0.4	23/1/2011	Section 4.16: JTAG adapter schematics
1.0.5	27/1/2011	Section 4.17: SOM SYS_BOOT pin configuration added. Boot select high for flashing.
1.0.6	27/2/2011	Industrial temp supported added for VAR-SOM-OM37
1.0.7	3/3/2011	Pin-out multiplexing table layout Revised block diagram
1.2	26/5/2011	Section 3: Added alternative functions to pin-out table Section 8: MTBF Clarifications Section 4.7: McBSP3 signals declaration fix Section 4.21: WLAN support added
1.22	9/10/2011	Section 3: Pin 99 Clarification
1.23	17/3//2012	Pin 106: GPIO 157, instead of GPIO 116 previously written.
1.3	17/5//2012	VAR-SOM-OM37 v2.3 Murata SP-9XSL-E Wi-Fi integrated to SOM instead of LSR TiWi-R2
1.31	17/8//2012	Revised mechanical drawing

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1 Overview

This chapter gives a short overview of the VAR-SOM-OM37

1.1 General Information

The VAR-SOM-OM37 is a low-power; high performance System-on-module which serves as a building block and easily integrates into any embedded solution. It includes all vital peripherals/interfaces and is ready to run any embedded operating system such as Linux and WinCE.

Supporting products:

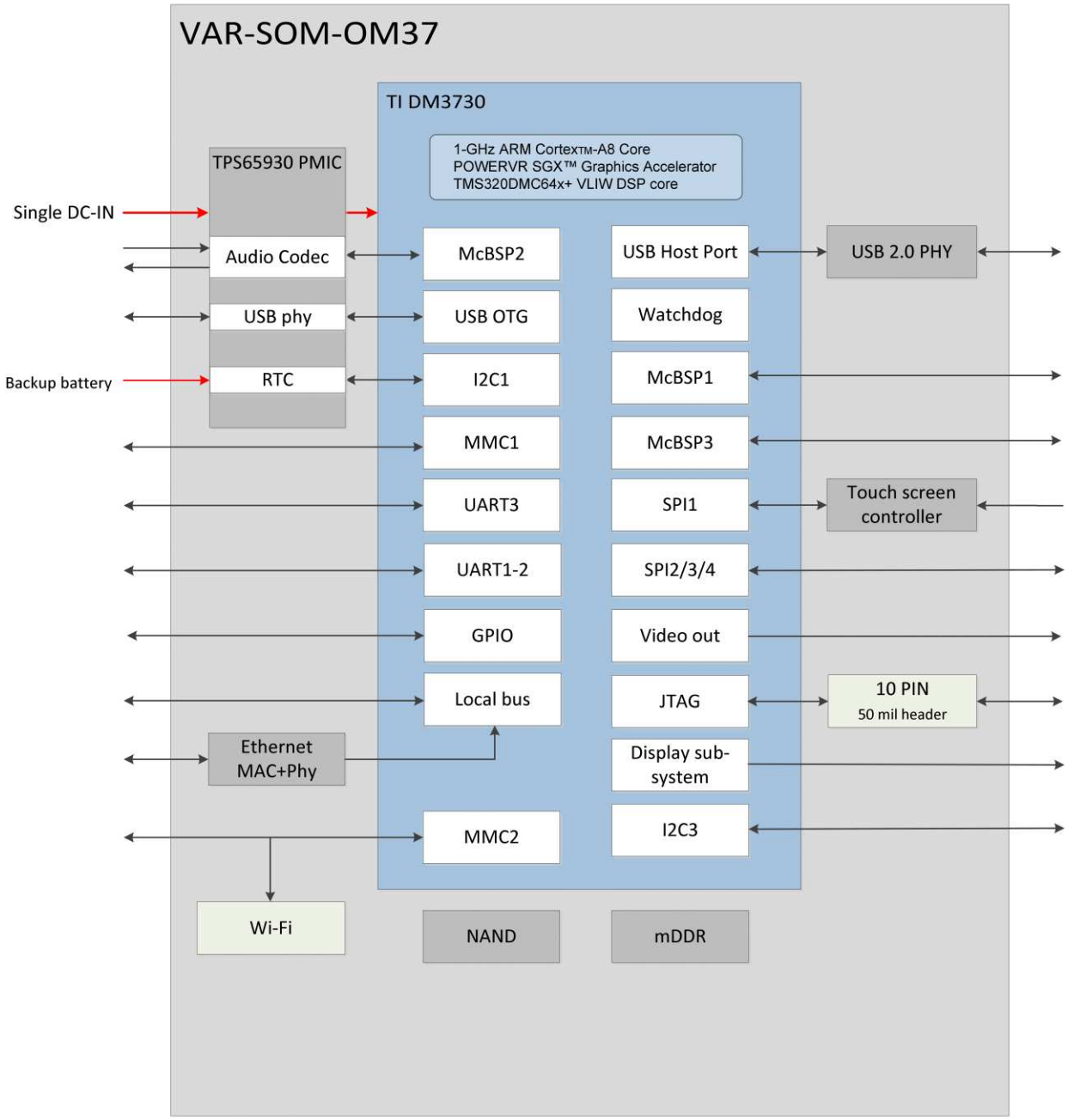
- Windows Embedded CE 6.0 R3BSP
- Linux BSP based on kernel 2.6.32
- VAR-37xxCustomBoard – evaluation board
  - ✓ Base-Board, compatible with VAR-SOM-OM37
  - ✓ Windows CE 6.0 run-time image
  - ✓ Linux Kernel 2.6.32 sources files
  - ✓ Schematics

Contact support for further information: mailto:support@variscite.com.

1.2 Feature Summary

- Texas Instruments DM/AM 37xx CPU
  - Up to 1000-MHz ARM Cortex™-A8 Core
  - NEON™ SIMD Coprocessor
  - High Performance Image, Video, Audio (IVA2.2™) Accelerator
  - POWERVR SG™ 2D/3D Graphics Accelerator (3730 Device Only)
  - 16kB/16kB Inst/ Data L1 cache
  - 256kB L2 cache
  - Internal 64kB SRAM
- 64-512MB 400MHz mDDR SDRAM.
- 256-512Mbytes Flash Disk
- LCD interface
- 2 SD card/SDIO/MMC card interface
- Power
  - Single 3.3-4.5V DC-IN power supply.(One lithium-ion cell battery)
  - Typical power consumption: 1W
- RAW image-sensor module interface
- 3 UART ports
- 100Mbit Ethernet controller
- Audio
  - 16-bit linear audio stereo DAC (96, 48, 44.1, and 32 kHz and derivatives)
  - 16-bit linear audio stereo ADC (48, 44.1, and 32 kHz and derivatives)
  - Microphone input
  - Line In and Out
- USB
  - USB 2.0 Host interface.
  - USB 2.0 OTG interface.
- Touch Screen interface
- Keypad interface
- Serial controllers
  - TDM interface (over McBSP1/3)
  - 3 x SPI interfaces
  - I2C interface
  - 1 – Wire/ HDQ
- WLAN - TiWi-R2 Module

1.3 Block Diagram



2 HW Components

This chapter shortly describes theVAR-SOM-OM37 HW components.

2.1 Texas Instruments DM / AM37xx

2.1.1 Overview

The DM/AM 37xx family of high-performance applications processors, are based on the enhanced OMAP™ 3 architecture and are integrated on TI's advanced 45-nm process technology.

Note: The OMAP 3 architecture is configured with different sets of features in different devices. This technical reference manual details all of the features available in current and future DM/AM 37xx devices.

The architecture is designed to provide best-in-class video, image, and graphics processing sufficient to support the following:

- Streaming video
- 2D/3D mobile gaming
- Video conferencing
- High-resolution still image
- Video capture in 2.5G wireless terminals, 3G wireless terminals, and rich multimedia-featured handsets, and high-performance personal digital assistants (PDAs).

This OMAP device also features the M-Shield™ mobile security technology to enable secure e-commerce applications and the replay of copyright-protected digital media content. Security features integrated on the devices support applications designed for:

- Protection against malicious attacks
- M-commerce
- Content protection for recordable media (CPRM)
- Digital rights management (DRM)

High-security (HS) devices rely on a security scheme based on hardware mechanisms and a secure read-only memory (ROM) code, ensuring that only trusted code can access the

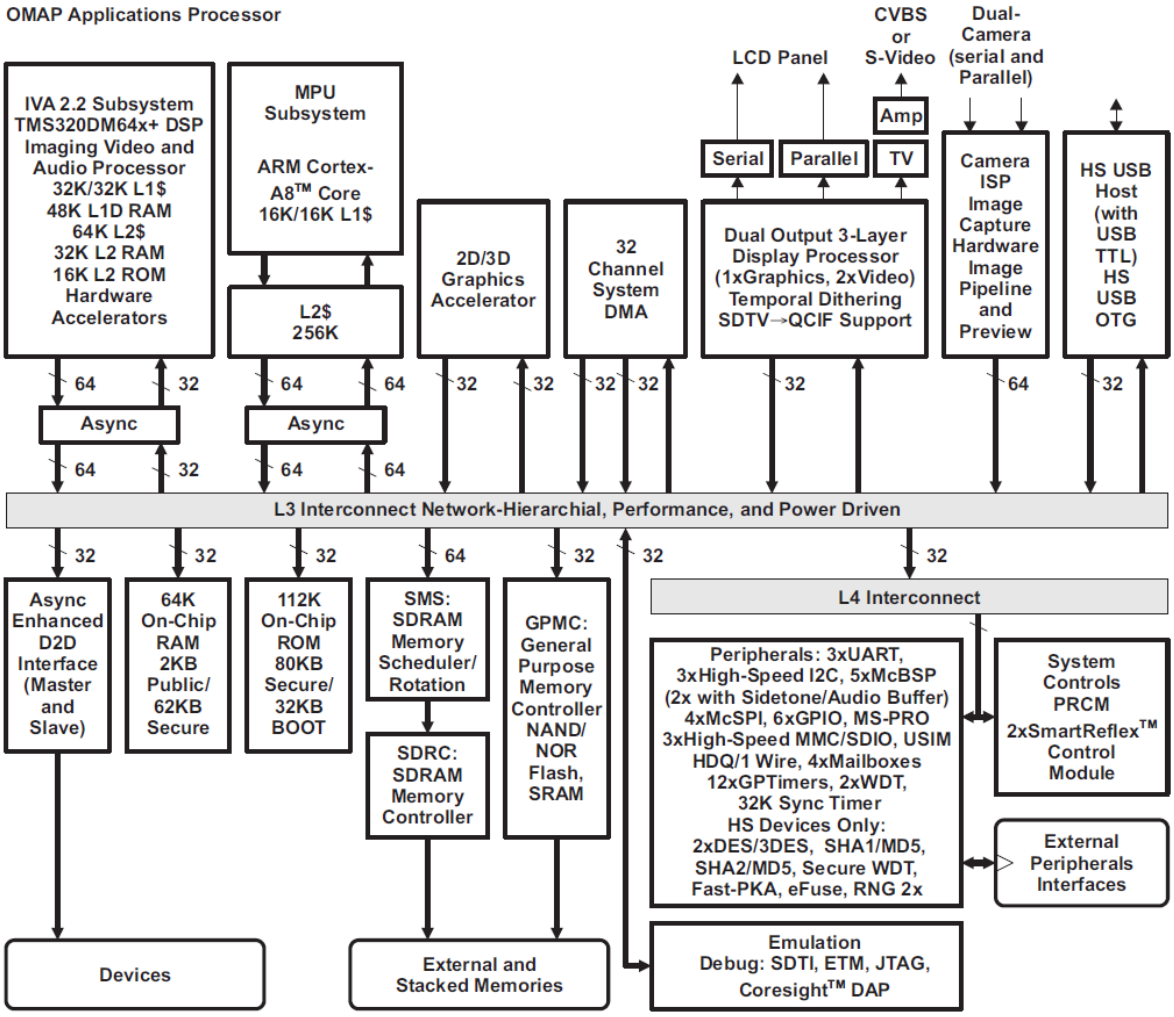
secure resources. These resources are in specific regions of memories as well as in peripherals, hardware cryptographicaccelerators, and eFuse keys. General-purpose (GP) devices do not include a security feature.

The following subsystems are part of the device:

- Microprocessor unit (MPU) subsystem based on the ARM® Cortex™-A8 microprocessor
- IVA2.2 subsystem with a C64x+ digital signal processor (DSP) core
- SGX subsystem for 2D and 3D graphics acceleration to support display and gaming effects
- Camera image signal processor (ISP) that supports multiple formats and interfacing options connected

Note: IVA2.2 and SGX are not available on all devices.

2.1.2 DM/AM37xx Block Diagram



2.1.3 MPU Subsystem

The MPU subsystem integrates the following modules:

- ARM subchip

  – ARM® Cortex™-A8 core

  – ARM Version 7™ ISA: Standard ARM instruction set + Thumb®-2, Jazelle® RCT Java accelerator, and media extensions

  – NEON™ SIMD coprocessor (VFP lite + media streaming instructions)

- Cache memories

  –Level 1: 16KB instruction and 16KB data—4-way set associative cache, 64 bytes/line

  –Level 2: 256kB.

- Interrupt controller (MPU IN TC) of 96 synchronous interrupt lines

- Asynchronous interface with core logic

- Debug, trace, and emulation features: ICE-Crusher, ETM, ETB modules.

2.1.4 IVA2.2 Subsystem

The device includes a high-performance imaging video and audio (IVA2.2) accelerator based on the Texas Instruments TMS320DMC64x+ VLIW DSP core.

Read TI DM / AM 37xx documentation for further information.

Note: IVA2.2 is not available on all devices.

2.1.5 On-Chip Memory

On-chip memory configuration offers memory resources for program and data storage:

- 112KB ROM
- 64KB single-access static random access memory (SRAM)

2.1.6 External Memory Interfaces

The device includes two external memory interfaces:

- General-purpose memory controller (GPMC)
  – NOR flash, NAND flash (with ECC Hamming code calculation), SRAM and Pseudo-SRAMasynchronous and synchronous protocols
  – Flexible asynchronous protocol control for external ASIC or peripheral interfacing
  – 16-bit data, up to 8 chip-selects (CSs)
  – 128M-byte addressable per chip-select, 1G-byte total address space
  – Nonmultiplexed device with limited address (2K bytes)
- SDRAM controller (SDRC)
  – Mobile single data rate (M-SDR) SDRAM and low-power double data rate (LPDDR) SDRAM
  – 16-bit or 32-bit data, 2 chip-selects, configurations for a maximum of 1 G-byte address space perchip-select
  – Work in conjunction with the SDRAM memory scheduler (SMS) companion module

2.1.7 DMA Controllers

- The device embeds one generic DMA controller, the system DMA (sDMA) controller, used formemory-to-memory, memory-to-peripheral, and peripheral-to-memory transfers:
- One read port, one write port
- 32 prioritizable logical channels
- 96 hardware requests
- 256 x 32-bit FIFO dynamically allocable between active channels

2.1.8 Multimedia

The device uses the following multimedia accelerators for display and gaming effects as well as high-endimaging and video applications:

- 2D and 3D graphics accelerator (SGX)
  – 2D and 3D graphics and video codecs supported on common hardware
  – Tile-based architecture
  – Universal scalable shader engine (USSE™) multithreaded engine incorporating pixel and vertexshader functionality reducing die area
  – Advanced shader feature set in excess of Microsoft VS3.0, PS3.0, and OGL2.0
  – Industry standard API support Direct3D mobile, OGL-ES 1.1 and 2.0, OpenVG 1.0, OpenMax
  – Fine-grained task switching, load balancing, and power management
  – Programmable high-quality image anti-aliasing
  – Advanced geometry DMA driven operation for minimum CPU interaction
  – Fully virtualized memory addressing for OS operation in a unified memory architecture
  – Advanced and standard 2D operations (that is, vector graphics, BLTs, ROPs, etc.)
  – Programmable video encode and decode support for H.264, H.263, MPEG4 (SP), WMV9, andJPEG

Note: Multimedia accelerators are not available on all devices.

- Camera interface
  – Supports most of the raw image sensors available in the market
  – Includes video processing hardware
  – 12-bit parallel interface supported
  – Pixel clock up to 83 MHz
- Display interface
  – Display controller
  – Color and monochrome displays up to 2048 x 2048 x 24-bpp resolution
  – 256 x 24-bit entries palette in red, green, blue (RGB)
  – 3,375 colors, 15 grayscales
  – Picture-in-picture (overlay), color-space conversion, rotation, color-phase rotation, and resizingsupport
  – Remote frame buffer interface
  – Liquid-crystal display (LCD) pixel interfaces (MIPI DPI 1.0) and LCD bus interfaces (MIPI DBI 1.0)supported
  – NTSC/PAL video encoder outputs with integrated digital-to-analog converters (DACs) output aresupported on CVBS and S-video TV analog output signals
  – Serial display interface implements high-speed differential output buffers to support FlatLink3G™,Mobile CMADS and MIPI DSI 1.0 formats
  – Embedded DMA controller

2.1.9 Peripherals

The device supports a comprehensive set of peripherals to provide flexible and high-speed interfacing andon-chip programming resources. The following tableprovides a list and description of the peripherals available onthe VAR-SOM-OM37 device.

Type	Name	Description
Serial Communication	Multi-channel Buffered	The McBSPs provide a full-duplex direct serial interface between Serial Ports (McBSPs) the device and other devices in a system such as audio and voice codecs and other application chips. McBSP1, McBSP2, and McBSP3 serve as general purpose serial ports while McBSP2 and McBSP3 include additional audio-loopback capability.
	Multi-channel Serial Port	The McSPIs provide a master/slave interface to SPI devices. Interface (McSPI)
	High-speed USB OTG	High-speed USB2.0 OTG controller that offers high-speed data Controller
	HDQ/1-Wire	The HDQ/1-Wire interface supports the Benchmark HDQ protocol and the Dallas Semiconductor 1-Wire protocol.
	Universal Asynchronous	Serial communication interfaces compatible to the industry Receiver/Transmitter standard TL16C550 asynchronous communications element. (UART) UART1 and UART 2 are general serial communication interfaces. UART3 provides additional support for infrared data association (IrDA) and consumer infrared (CIR) communications
	High-speed (HS) I2C	Master/slave I2C high-speed standard interfaces with support for Inter-integrated Circuit standard mode (up to 100K bits/s), fast mode (up to 400K (I2C) Controllers bits/s), and high-speed mode (up to 3.4M bits/s).
Removable Media	Multimedia Card/Secure Digital/Secure Digital IO (MMC/SDIO) Card Interface	MMC memory card, SD memory card, or SDIO cards interface.
Miscellaneous	GP timers	Twelve general-purpose timers
	Watchdog timers	Three watchdog timers (WDTs)
	32-kHz synchronization timer	32-kHz clock timer
	General-purpose input/output (GPIO)	General-purpose input/output pins controlled by six GPIO controllers.
	Mailbox	MPU/IVA2.2 inter-processor communications mailboxes. All six mailboxes are available in chassis mode, however, only two mailboxes are available in stand-alone mode.
	Control module	I/O multiplexing and chip-configuration control.
Security Modules		RNG, Fast PKA, 2xDES/3DES, SHA1/MD5, SHA2/MD5, 2xAES, Secure Watchdog Timer, and universal subscriber identity module (USIM).

2.2 TPS65930 PMIC

The VAR-SOM-OM37 uses the TI TPS65930 companion chip.

The TPS65930 is a power-management IC dedicatedfor the OMAP3™ Platform. The TPS65930 includes:Power regulators, universal serial bus (USB) high-speed (HS) transceiver, analog-to-digital converter (ADC), real-time clock (RTC) and embedded power control (EPC). In addition, the TPS65930 includes an audio codec with two digital-to-analog converters (DACs) and two ADCs to implement dual voice channels and a stereo downlink channel that can play all standard audio sample rates, through a multiple format inter-integrated sound (I2S™)/time division multiplexing (TDM) interface.

The RTC can be powered by a backup battery when the main supply is not present.

2.3 Memory

2.3.1 400MHZ mDDR

The VAR-SOM-OM37 is assembled with 64-512MB of mDDR with clock rate of 400MHz.

DDR memory is 32-bit wide

2.3.2 Non volatile storage memory

The VAR-SOM-OM37supports up to 512MB of SLC NAND flash.

The NAND flash is used for Flash Disk purposes, O.S. run-time-image and the Bootloader (Boot from NAND).

2.4 SMSC LAN9220 Ethernet controller

The LAN9220 is a full-featured, single-chip 10/100 Ethernet controller. The LAN9220 is an IEEE 802.3 10BASE-T and 802.3u 100BASE-TX compliant, and supports HP Auto-MDIX.

Qualified and Suggested Magnetics:

Magnetics listed under “Qualified” title have been tested in order to verify the proper operation with LAN9220 device. Magnetics in “Suggested” category was evaluated on the vendor-supplied datasheet level, but have not been tested.

Qualified Magnetics:

Vendor	Part Number	Package	Cores	Temp	Configuration
Pulse	H1102	16-pin SOIC	4	0 -+70o C	HP Auto-MDX
Halo	TG110-RP55N5	16-pin SOIC	4	0 -+70o C	HP Auto-MDX
Halo	HFJ11-RP26E-L12RL	Integrated RJ45	4	0 -+70o C	HP Auto-MDX POE
Delta	RJSE1R5310A	Integrated RJ45	4	0 -+70o C	HP Auto-MDX

Suggested Magnetics:

Vendor	Part Number	Package	Cores	Temp	Configuration
Pulse	J0011D01B	Integrated RJ45	4	0 -+70o C	HP Auto-MDX
Midcom	TG110-RP55N5	Cardbus	4	0 -+70o C	HP Auto-MDX
Bothhand	HFJ11-RP26E-L12RL	16-pin SOIC	4	0 -+70o C	HP Auto-MDX
Bothhand	RJSE1R5310A	Integrated RJ45	4	0 -+70o C	HP Auto-MDX

3 SOM Connectors

The VAR-SOM-OM37 exposes an SO–DIMM 200 pin mechanical standard interface. The recommended mating connector for base board interfacing is FCI 10033853-052FSLF or equivalent.

SOM connector signal list:

Pin	Pin Name	Mode	Dir	Type	Description	Ball
1	DSS_DATA1 UART1_RTS GPIO_71 SAFE_MODE	0 2 4 7	I O I/O	Digital	LCD Data 1	AB19
2	DSS_DATA0 UART1_CTS GPIO_70 SAFE_MODE	0 2 4 7	O I I/O	Digital	LCD Data 0	AC19
3	DSS_DATA3 GPIO_73 SAFE_MODE	0 4 7	O I/O	Digital	LCD Data 3	AC20
4	DSS_DATA2 GPIO_72 SAFE_MODE	0 4 7	O I/O	Digital	LCD Data 2	AD20
5	DSS_DATA5 UART3_TX GPIO_75 SAFE_MODE	0 2 4 7	O O I/O	Digital	LCD Data 5	AC21
6	DSS_DATA4 UART3_RX GPIO_74 SAFE_MODE	0 2 4 7	O I I/O	Digital	LCD Data 4	AD21
7	DSS_DATA7 UART1_RX GPIO_77 HW_DBG15 SAFE_MODE	0 2 4 5 7	O I I/O O	Digital	LCD Data 7	E23
8	DSS_DATA6 UART1_RX GPIO_76 HW_DBG14 SAFE_MODE	0 2 4 5 7	O O I/O O	Digital	LCD Data 6	D24

9	DSS_DATA9 UART3_TX GPIO_79 HW_DBG17 SAFE_MODE	0 2 4 5 7	I/O O I/O O	Digital	LCD Data 9	F23
10	DSS_DATA8 UART3_RX GPIO_78 HW_DBG16 SAFE_MODE	0 2 4 5 7	I/O I I/O O	Digital	LCD Data 8	E24
11	DSS_DATA11 GPIO_81 SAFE_MODE	0 4 7	O I/O	Digital	LCD Data 11	AC23
12	DSS_DATA10 GPIO_80 SAFE_MODE	0 4 7	O I/O	Digital	LCD Data 10	AC22
13	DSS_DATA13 GPIO_83 SAFE_MODE	0 4 7	O I/O	Digital	LCD Data 13	Y22
14	DSS_DATA12 GPIO_82 SAFE_MODE	0 4 7	O I/O	Digital	LCD Data 12	AB22
15	DSS_DATA15 GPIO_85 SAFE_MODE	0 4 7	O I/O	Digital	LCD Data 15	V22
16	DSS_DATA14 GPIO_84 SAFE_MODE	0 4 7	O I/O	Digital	LCD Data 14	W22
17	DSS_DATA17 GPIO_87 SAFE_MODE	0 4 7	O I/O	Digital	LCD Data 17	G23
18	CAM_D5 GPIO_104 HW_DBG7 SAFE_MODE	0 4 5 7	I I/O O	Digital	ISP Data 5	B21
19	DSS_DATA19 McSPI3_SIMO DSS_DATA1 GPIO_89 SAFE_MODE	0 2 3 4 7	O I/O I/O I/O	Digital	LCD Data 19	H23

20	DSS_DATA18 McSPI3_CLK DSS_DATA0 GPIO_88 SAFE_MODE	0 2 3 4 7	O I/O I/O I/O	Digital	LCD Data 18	G24
21	DSS_DATA21 McSPI3_CS0 DSS_DATA1 GPIO_91 SAFE_MODE	0 2 3 4 7	O I/O I/O I/O	Digital	LCD Data 21	K22
22	DSS_DATA20 McSPI3_SOMI DSS_DATA2 GPIO_90 SAFE_MODE	0 2 3 4 7	O I/O I/O I/O	Digital	LCD Data 20	D23
23	DSS_DATA23 DSS_DATA5 GPIO_93 SAFE_MODE	0 3 4 7	O I/O I/O	Digital	LCD Data 23	W21
24	DSS_DATA22 McSPI3_CS1 DSS_DATA4 GPIO_92 SAFE_MODE	0 2 3 4 7	O O I/O I/O	Digital	LCD Data 22	V21
25	CAM_XCLKA GPIO_96 SAFE_MODE	0 4 7	O I/O	Digital		B22
26	DSS_HSYNC GPIO_67 HW_DBG13 SAFE_MODE	0 4 5 7	O I/O O	Digital	LCD Horizontal Sync	E22
27	GPIO_126 SAFE_MODE	4 7	I/O	Digital		N22
28	DSS_PCLK GPIO_66 HW_DBG12 SAFE_MODE	0 4 5 7	O I/O O	Digital	LCD Pixel Clock	G22
29	UART3_CTS GPIO_163 SAFE_MODE	0 4 7	I/O I/O	Digital	UART3 CTS	A23
30	GPIO_129 SAFE_MODE	4 7	I/O	Digital		P24

31	UART3_RTS GPIO_164 SAFE_MODE	0 4 7	O I/O	Digital	UART3 RTS	B23
32	MMC1_CLKO GPIO_120 SAFE_MODE	0 4 7	O I/O	Digital	MMC1 Clock	M23
33	UART3_RX GPIO_165 SAFE_MODE	0 4 7	I I/O	Digital	UART3 RX	B24
34	GND	N/A	N/A	Power		
35	UART3_TX GPIO_166 SAFE_MODE	0 4 7	O I/O	Digital	UART3 TX	C23
36	MMC1_DAT0 GPIO_122 SAFE_MODE	0 4 7	I/O I/O	Digital	MMC1 Data 0	M22
37	McSPI2_CLK HSUSB2_DATA7 GPIO_178 SAFE_MODE	0 3 4 7	I/O I/O I/O	Digital		N5
38	MMC1_DAT1 GPIO_123 SAFE_MODE	0 4 7	I/O I/O	Digital	MMC1 Data 1	M21
39	McSPI2_SIMO GPT_9_PWM_EVT HSUSB2_DATA4 GPIO_179 SAFE_MODE	0 1 3 4 7	I/O I/O I/O I/O	Digital		N4
40	MMC1_DAT2 GPIO_124 SAFE_MODE	0 4 7	I/O I/O	Digital	MMC1 Data 2	M20
41	McSPI2_SOMI GPT_10_PWM_EVT HSUSB2_DATA5 GPIO_180 SAFE_MODE	0 1 3 4 7	I/O I/O I/O I/O	Digital		N3
42	MMC1_DAT3 GPIO_125 SAFE_MODE	0 4 7	I/O I/O	Digital	MMC1 Data 3	N23
43	MMC1_CMD GPIO_121 SAFE_MODE	0 4 7	I/O I/O	Digital	MMC1 Command	L23

44	CAM_D6 GPIO_105 SAFE_MODE	0 4 7	I I	Digital	ISP Data 6 • (2)	L24
45	DSS_DATA16 GPIO_86 SAFE_MODE	0 4 7	O I/O	Digital	LCD Data 16	J22
46	DSS_VSYNC GPIO_68 SAFE_MODE	0 4 7	O I/O	Digital	LCD Vertical Sync	F22
47	GND	N/A		Power		
48	GND	N/A		Power		
49	SYS_CLKOUT1 GPIO_10 SAFE_MODE	0 4 7	O I/O	Digital	General Purpose Clock-out 1	Y7
50	CAM_D4 GPIO_103 HW_DBG6 SAFE_MODE	0 4 5 7	I I/O O	Digital	ISP Data 4	G20
51	GND	N/A		Power		
52	LB_nCS4 SYS_nDMAREQ1 McBSP4_CLKX GPT_9_PWM_EVT GPIO_55 SAFE_MODE	0 1 2 3 4 7	O I I I/O I/O	Digital	Local bus Chip Select 4	F4
53	CAM_D7 GPIO_106 SAFE_MODE	0 4 7	I I	Digital	ISP Data 7 • (2)	K24
54	TV-OUT			Analog		
55	CAM_D3 GPIO_102 HW_DBG5 SAFE_MODE	0 4 5 7	I I/O O	Digital	ISP Data 3	F19
56	CAM_D2 GPIO_101 HW_DBG4 SAFE_MODE	0 4 5 7	I I/O O	Digital	ISP Data 2	G19

57	CAM_WEN CAM_SHUTTER GPIO_167 HW_DBG10 SAFE_MODE	0 2 4 5 7	I O I/O O	Digital	ISP write-enable signal	F18
58	GND	N/A		Power		
59	CAM_PCLK GPIO_97 HW_DBG2 SAFE_MODE	0 4 5 7	I/O I/O O	Digital	ISP Parallel interface pixel clock	J19
60	GND	N/A		Power		
61	I2C3_SDA GPIO_185 SAFE_MODE	0 4 7	I/OD I/O	Digital	I2C#3 SDA (data)	AC12
62	CAM_STROBE GPIO_126 HW_DBG11 SAFE_MODE	0 4 5 7	O I/O O	Digital	CAM_STROBE	J20
63	I2C3_SCL GPIO_184 SAFE_MODE	0 4 7	I/OD I/O	Digital	I2C#3 SCL (clock)	AC13
64	DSS_ACBIAS GPIO_69 SAFE_MODE	0 4 7	O I/O	Digital	LCD AC bias/Data enable	J21
65	McBSP3_DX UART2_CTS GPIO_140 SAFE_MODE	0 1 4 7	I/O I I/O	Digital	McBSP3 data out UART#2 CTS	V6
66	McSPI2_CS0 GPT_11_PWM_EVT HSUSB2_DATA6 GPIO_181 SAFE_MODE	0 1 3 4 7	I/O I/O I/O I/O	Digital	McSPI2 Chip Select 0	M5
67	McBSP3_DR UART2_RTS GPIO_141 SAFE_MODE	0 1 4 7	I O I/O	Digital	McBSP3 data in UART#2 RTS	V5
68	CAM_D11 GPIO_110 HW_DBG9 SAFE_MODE	0 4 5 7	I I/O I/O	Digital	ISP Data 11	G21

69	McBSP3_CLKX UART2_TX GPIO_142 SAFE_MODE	0 1 4 7	I/O O I/O	Digital	McBSP3 clock UART#2 TX	W4
70	CAM_D10 GPIO_109 HW_DBG8 SAFE_MODE	0 4 5 7	O I/O O	Digital	ISP Data 10	F21
71	McBSP3_FSX UART2_RX GPIO_143 SAFE_MODE	0 1 4 7	I I I/O	Digital	McBSP3 frame sync UART#2 RX	V4
72	CAM_D9 GPIO_108 SAFE_MODE	0 4 7	I I	Digital	ISP Data 9 • (2)	K23
73	TSPX	N/A	I	Analog	Touch Screen X Plus	N/A
74	CAM_D8 GPIO_107 SAFE_MODE	0 4 7	I I	Digital	ISP Data 8 • (2)	J23
75	TSPY	N/A	I	Analog	Touch Screen Y Plus	N/A
76	CAM_VS GPIO_95 HW_DBG1 SAFE_MODE	0 4 5 7	IO I/O O	Digital	ISP Frame trigger signal	E18
77	TSMX	N/A	I	Analog	Touch Screen X Minus	N/A
78	CAM_HS GPIO_94 HW_DBG0 SAFE_MODE	0 4 5 7	IO I/O O	Digital	ISP Line trigger signal	A22
79	TSMY	N/A	I	Analog	Touch Screen Y Minus	N/A
80	CAM_FLD CAM_RESET GPIO_98 HW_DBG3 SAFE_MODE	0 2 4 5 7	I/O O IO O	Digital	ISP Field ID signal	H24
81	GND	N/A		Power		

82	HDQ SYS_ALTCLK I2C2_SCCBE I2C3_SCCBE GPIO_170 SAFE_MODE	0 1 2 3 4 7	I/O I O O I/O	Digital	HDQ / 1-Wire Line	A24
83	GND	N/A		Power		
84	UART1_TX GPIO_148 SAFE_MODE	0 4 7	O I/O	Digital	UART#1 TX	W7
85	LB_WAIT3 SYS_nDMAREQ1 UART3_CTS GPIO_65 SAFE_MODE	0 1 2 4 7	I I I I/O	Digital	Local Bus Wait for CS3 Local Bus SDMA Request 1	C2
86	UART1_RTS GPIO_149 SAFE_MODE	0 4 7	O I/O	Digital	UART#1 RTS	W6
87	LB_CLK GPIO_59	0 4	O I/O	Digital	Local Bus clock	W2
88	UART1_CTS GPIO_150 SAFE_MODE	0 4 7	I I/O	Digital	UART#1 CTS	AC2
89	LB_nCS3 SYS_nDMAREQ0 GPIO_54 SAFE_MODE	0 1 4 7	O I I/O	Digital	Local bus Chip Select 3	D2
90	UART1_RX McBSP1_CLKR McSPI4_CLK GPIO_151 SAFE_MODE	0 2 3 4 7	I I I/O I/O	Digital	UART#1 RX	V7
91	MMC1_CD			Digital	Card Detect (from PMIC)	
92	SYS_BOOT5 MMC2_DIR_DAT3 DSS_DATA22 GPIO_7 SAFE_MODE	0 1 3 4 7	I O O I/O	Digital	Flash burning switch	AB16
93	CAM_D1 GPIO_100 SAFE_MODE	0 4 7	I I	Digital	ISP Data 1 • (2)	AC18
94	GND	N/A		Power		

95	CAM_D0 GPIO_99 SAFE_MODE	0 4 7	I I	Digital	ISP Data 0 • (2)	AB18
96	GND	N/A		Power		
97	RESET_OUT_N	N/A	O	Digital	Reset signal to base-board peripherals	N/A
98	McBSP1_CLKX McBSP3_CLKX GPIO_162 SAFE_MODE	0 2 4 7	I/O I/O I/O	Digital		V18
99	TPS65930 LEDA GPIO	N/A	N/A	Digital		
100	McBSP1_FSX McSPI4_CS0 McBSP3_FSX GPIO_161 SAFE_MODE	0 1 2 4 7	I/O I/O I/O I/O	Digital		AA19
101	HOST_nOC	N/A	N/A	Digital		
102	McBSP1_DR McSPI4_SOMI McBSP3_DR GPIO_159 SAFE_MODE	0 1 2 4 7	I I/O I I/O	Digital	McBSP#1 Receive data	Y18
103	USBHOST1_DP	N/A	IO	Diff	USB Host #1 Data Positive	N/A
104	McBSP1_DX McSPI4_SIMO McBSP3_DX GPIO_158 SAFE_MODE	0 1 2 4 7	I/O I/O I/O I/O	Digital	McBSP#1 Transmit data	W18
105	USBHOST1_DN	N/A	I/O	Diff	USB Host #1 Data Negative	N/A
106	McBSP1_FSR GPIO_157 SAFE_MODE	0 4 7	I/O I/O	Digital		AB20
107	USBHOST1_VBUS	N/A	I	Analog	USB Host #1VBUS 5v indicator	N/A
108	McBSP1_CLKR McSPI4_CLK GPIO_156 SAFE_MODE	0 1 4 7	I/O I/O I/O	Digital	McBSP1 Receive Clock	W19

109	ETK_D14 HSUSB2_DATA0 GPIO_28 MM2_RXRCV HW_DBG16	0 3 4 5 7	O I/O	Digital		AC11
110	VBAT	N/A	I	Power		N/A
111	ETK_D13 HSUSB2_NXT GPIO_27 MM2_RXDM SAFE_MODE	0 3 4 5 7	O I I/O I/O	Digital		AD11
112	VBAT	N/A	I	Power	DC-IN supply voltage. Voltage range: 3.3 – 4.5V	
113	GND	N/A		Power		
114	VBAT	N/A	I	Power	DC-IN supply voltage. Voltage range: 3.3 – 4.5V	
115	GND	N/A		Power		
116	VBAT	N/A	I	Power	DC-IN supply voltage. Voltage range: 3.3 – 4.5V	
117	VIO 1.8V	N/A	O	Power	Digital IO Output Voltage. Up to 200ma	
118	USB_OTG_VBUS	N/A	I	Analog	USB 2.0 OTG VBUS indicator	
119	ETK_D12 HSUSB2_DIR GPIO_26 HW_DBG14	0 3 4 7	O I I/O O	Digital		AC10
120	USB_OTG_DP	N/A	IO	Diff	USB 2.0 OTG Data Positive	
121	PWRON	N/A	IO	Digital		
122	USB_OTG_DN	N/A	IO	Diff	USB 2.0 OTG Data Negative	
123	REGEN	N/A	IO	Digital		
124	USB_OTG_ID	N/A	I	Analog	USB OTG Host/Device ID	
125	LB_RE_OE_N	0	O	Digital		F2
126	RTC_BACKUP	N/A	I	Power	RTC backup-battery power supply	
127	RESET_IN_N	N/A	I	Digital	Hardware Reset	N/A

128	LB_IO_A9 SYS_nDMAREQ2 GPIO_42 SAFE_MODE	0 1 4 7	O I I/O	Digital	Local bus address 9	H2
129	LB_IO_10 SAFE_MODE	0 7	I/O	Digital	Local bus data 10	U1
130	LB_IO_A8 GPIO_41 SAFE_MODE	0 4 7	O I/O	Digital	Local bus address 8 • (1)	H1
131	LB_IO_9 SAFE_MODE	0 7	I/O I/O	Digital	Local bus data 9	T2
132	LB_IO_11 SAFE_MODE	0 7	I/O I/O	Digital	Local bus data 11	R3
133	LB_IO_8 SAFE_MODE	0 7	I/O I/O	Digital	Local bus data 8	R2
134	LB_IO_14 SAFE_MODE	0 7	I/O I/O	Digital	Local bus data 14	V1
135	LB_IO_7	0	I/O	Digital	Local bus data 7	R1
136	LB_IO_15 SAFE_MODE	0 7	I/O I/O	Digital	Local bus data 15	V2
137	LB_IO_6	0	I/O	Digital	Local bus data 6	P2
138	LB_IO_12 SAFE_MODE	0 7	I/O I/O	Digital	Local bus data 12	T3
139	LB_IO_5	0	I/O	Digital	Local bus data 5	P1
140	LB_IO_13 SAFE_MODE	0 7	I/O I/O	Digital	Local bus data 13	U2
141	LB_IO_4	0	I/O	Digital	Local bus data 4	M3
142	LB_IO_A1 GPIO_34 SAFE_MODE	0 4 7	O I/O	Digital	Local bus address 1 • (1)	K4
143	LB_IO_3	0	I/O	Digital	Local bus data 3	N2

144	LB_IO_A2 GPIO_35 SAFE_MODE	0 4 7	O I/O	Digital	Local bus address 2 • (1)	K3
145	LB_IO_2	0	I/O	Digital	Local bus data 2	M2
146	LB_IO_A3 GPIO_36 SAFE_MODE	0 4 7	O I/O	Digital	Local bus address 3 • (1)	K2
147	LB_IO_1	0	I/O	Digital	Local bus data 1	M1
148	LB_WAIT0	0	I	Digital	Local bus CS0 wait signal	C1
149	LB_IO_0	0	I/O	Digital	Local bus data 0	L2
150	LB_IO_A4 GPIO_37 SAFE_MODE	0 4 7	O I/O	Digital	Local bus address 4 • (1)	J4
151	GND	N/A		Power		
152	LB_nBE0_CLE GPIO_60	0 4	O I/O	Digital	Local bus Output enable for static memory, muxed with CLE	K5
153	LB_IO_A5 GPIO_38 SAFE_MODE	0 4 7	O I/O	Digital	Local bus address 5 • (1)	J3
154	LB_nADV_ALE	0	O	Digital	Local bus Address Latch Enable, muxed with Address Valid	F1
155	LB_IO_A6 GPIO_39 SAFE_MODE	0 4 7	O I/O	Digital	Local bus address 6 • (1)	J2
156	GND	N/A		Power		
157	LB_IO_A7 GPIO_40 SAFE_MODE	0 4 7	O I/O	Digital	Local bus address 7 • (1)	J1
158	VCC33	N/A	O	Power	Output voltage for general use. Up to 200ma	
159	GND	N/A		Power		
160	LB_WE_N	0	O	Digital	Local bus Write enable (active low)	G3
161	LINK_LED	N/A	O	Open Drain	Ethernet Link LED	
162	GND	N/A		Power		

163	SPEED_LED	N/A	O	Open Drain	Ethernet Speed LED	
164	MMC2_CLK McSPI3_CLK GPIO_130 SAFE_MODE	0 1 4 7	O I/O I I/O	Digital	MMC2 Clock	Y1
165	ETH_TXN	N/A	O	Diff	Ethernet TX Negative	
166	MMC2_CMD McSPI3_SIMO GPIO_131 SAFE_MODE	0 1 4 7	I/O I/O O I/O	Digital	MMC2 CMD	AB5
167	ETH_TXP	N/A	O	Diff	Ethernet TX Positive	
168	MMC2_DAT0 McSPI3_SOMI GPIO_132 SAFE_MODE	0 1 4 7	I/O I/O O I/O	Digital	MMC2 Data 0	AB3
169	VCC33A		O	Power	3.3V Output to Ethernet Magnetics	
170	MMC2_DAT1 GPIO_133 SAFE_MODE	0 4 7	I/O I I/O	Digital	MMC2 Data 1	Y3
171	ETH_RXN		I	Diff	Ethernet RX Negative	
172	MMC2_DAT2 McSPI3_CS1 GPIO_134 SAFE_MODE	0 1 4 7	I/O O I/O	Digital	MMC2 Data 2	W3
173	ETH_RXP		I	Diff	Ethernet RX Positive	
174	MMC2_DAT3 McSPI3_CS0 GPIO_135 SAFE_MODE	0 1 4 7	I/O I/O I/O	Digital	MMC2 Data 3	V3
175	KPD.R5	N/A	I/O	Digital	Keypad controller row 5	
176	KPD.R4	N/A	I/O	Digital	Keypad controller row 4	
177	KPD.C0	N/A	I/O	Digital	Keypad controller col. 0	
178	KPD.R3	N/A	I/O	Digital	Keypad controller row 3	
179	KPD.C1	N/A	I/O	Digital	Keypad controller col. 1	
180	KPD.R2	N/A	I/O	Digital	Keypad controller row 2	
181	KPD.C2	N/A	I/O	Digital	Keypad controller col. 2	

182	KPD.R1	N/A	I/O	Digital	Keypad controller row 1	
183	KPD.C3	N/A	I/O	Digital	Keypad controller col. 3	
184	KPD.R0	N/A	I/O	Digital	Keypad controller row 0	
185	KPD.C4	N/A	I/O	Digital	Keypad controller col. 4	
186	CODEC_AUXADC1	N/A	I	Analog		
187	KPD.C5	N/A	I/O	Digital	Keypad controller col. 5	
188	CODEC_AUXADC2	N/A	I	Analog		
189	PWM0	N/A	O	Digital	PWM0 signal	
190	HP_LOUT	N/A	O	Analog	Headphones Left	
191	MMC2_DAT6 MMC2_DIR_CMD CAM_SHUTTER MMC3_DAT2 GPIO_138 SAFE_MODE	0 1 2 3 4 7	I/O O O I/O I/O	Digital	MMC2 Data 6	Y2
192	HP_ROUT	N/A	O	Analog	Headphones right	
193	MMC2_DAT4 MMC2_DIR_DAT0 MMC3_DAT0 GPIO_136 SAFE_MODE	0 1 3 4 7	I/O O I/O I/O	Digital	MMC2 Data 4	AB2
194	CODEC_LINEIN	N/A	I	Analog		
195	MMC2_DAT7 MMC2_CLKIN MMC3_DAT3 GPIO_139 MM3_RXDM SAFE_MODE	0 1 3 4 6 7	I/O I I/O I/O I/O	Digital	MMC2 Data 7	AA1
196	MIC_BIAS	N/A	O	Analog	Microphone Bias voltage	
197	MIC_N	N/A	I	Analog	Microphone in	
198	AUD_GND	N/A		Power		
199	MIC_P	N/A	I	Analog		
200	AUD_GND	N/A		Power		

- (1) Local Bus address signals 1-7 can be used as GPIOs only if Ethernet controller is not assembled

- (2) Input only signals

4 Interfaces

4.1 Display interface

Supported display modes:

– Color and monochrome displays up to 2048 x 2048 x 24-bpp resolution
– 256 x 24-bit entries palette in red, green, blue (RGB)

LCD interface signals:

Signal	Pin #	Type	Description
DSS_PCLK	28	O	LCD Pixel clock
DSS_HSYNC	26	O	LCD Horizontal Sync
DSS_VSYNC	46	O	LCD Vertical Sync
DSS_ACBIAS	64	O	LCD AC bias/Data enable
DSS_D0	2	O	LCD Data line
DSS_D1	1	O	LCD Data line
DSS_D2	4	O	LCD Data line
DSS_D3	3	O	LCD Data line
DSS_D4	6	O	LCD Data line
DSS_D5	5	O	LCD Data line
DSS_D6	8	O	LCD Data line
DSS_D7	7	O	LCD Data line
DSS_D8	10	O	LCD Data line
DSS_D9	9	O	LCD Data line
DSS_D10	12	O	LCD Data line
DSS_D11	11	O	LCD Data line
DSS_D12	14	O	LCD Data line
DSS_D13	13	O	LCD Data line
DSS_D14	16	O	LCD Data line
DSS_D15	15	O	LCD Data line
DSS_D16	45	O	LCD Data line
DSS_D17	17	O	LCD Data line
DSS_D18	20	O	LCD Data line
DSS_D19	19	O	LCD Data line
DSS_D20	22	O	LCD Data line
DSS_D21	21	O	LCD Data line
DSS_D22	24	O	LCD Data line
DSS_D23	23	O	LCD Data line

TV-OUT interface signals

Signal	Pin #	Type	Description
TV-OUT	54	O	NTSC/PAL TV-OUT

4.2 Analog audio

The VAR-SOM-OM37 uses the TPS65930 built-in Audio codec

Audio signals:

Signal	Pin #	Type	Description
HP_LOUT	190	O	Pre-amped Headphones, Left out
HP_ROUT	192	O	Pre-amped Headphone, Right Out
CODEC_AUXADC1	186	I	Auxiliary ADC IN 1
CODEC_AUXADC2	188	I	Auxiliary ADC IN 2
CODEC_LINEIN	194	I	Line IN
MIC_BIAS	196	I	Mic Bias Voltage
MIC_N	197	I	Mic Negative In
MIC_P	199	I	Mic Positive In
AUD_GND	198, 200		Audio Ground. Connect to GND if Audio not used!

4.3 Camera Interface

The VAR-SOM-OM37 uses the DM/AM 37 Camera interface.

Image sensor:

- Interface with various image sensors:
  - R, G, B primary colors
  - Ye, Cy, Mg, G complementary colors
- Support for electronic rolling shutter (ERS) and global-release reset shutters

· **Parallel interface:** The parallel interface supports two modes:

- **SYNC mode:** In this mode, the image-sensor module provides horizontal and vertical synchronization signals to the parallel interface, along with the pixel clock. This mode works with 8-, 10-, 11-, and 12-bit data (above 10-bit RAW data, the processing pipe cannot be used; data must be transferred to memory). SYNC mode supports progressive and interlaced image-sensor modules.
- **ITU mode:** In this mode, the image-sensor module provides an ITU-R BT 656-compatible data stream. The horizontal and vertical synchronization signals are not provided to the interface. Instead, the data stream embeds start-of-active (SAV) and end-of-active video (EAV) synchronization code. This mode works in 8- and 10-bit configurations. It supports only progressive image-sensor modules.

Note:

- Up to 8-bit data at 130 MHz can be transferred to memory.
- Up to 10-bit data at 75 MHz can be processed by the image pipeline or transferred to memory.
- Up to 12-bit data at 75 MHz can be transferred to memory as is, or after processing inside the CCDC. It can also be internally converted to 10-bit data for full processing.

VAR-SOM-OM37 ISP signals:

Signal	Pin #	Type	Description
CAM _PCLK	59	I	Parallel interface pixel clock
CAM _HS	78	IO	Line trigger input/output signal
CAM _VS	76	IO	Frame trigger input/output signal
CAM _FLD	80	IO	Field identification input/output signal
CAM _WEN	57	I	External write-enable signal
CAM _XCLKA	25	O	External clock for the image-sensor module
CAM _STROBE	62	O	Flash strobe control signal
CAM_D0	95	I	ISP Data
CAM _D1	93	I	ISP Data
CAM _D2	56	I	ISP Data
CAM _D3	55	I	ISP Data
CAM _D4	50	I	ISP Data

CAM _D5	18	I	ISP Data
CAM _D6	44	I	ISP Data
CAM _D7	53	I	ISP Data
CAM _D8	74	I	ISP Data
CAM _D9	72	I	ISP Data
CAM _D10	70	I	ISP Data
CAM _D11	68	I	ISP Data

4.4 Ethernet

The VAR-SOM-OM37provides one full-featured 10/100 Mbit Ethernet port using the SMSC LAN9220/1 Ethernet controller.

LAN9221 offers higher data throughput.

Features:

- Fully compliant with IEEE 802.3/802.3u standards
- Integrated Ethernet MAC and PHY
- 10BASE-T and 100BASE-TX support
- Full- and Half-duplex support
- Full-duplex flow control
- Backpressure for half-duplex flow control
- Preamble generation and removal
- Automatic 32-bit CRC generation and checking
- Automatic payload padding and pad removal
- Auto-negotiation
- Automatic polarity detection and correction

VAR-SOM-OM37 Ethernet Controller signals:

Signal	Pin #	Type	Description
ETH_TXN	165	O	Transmit Negative
ETH_TXP	167	O	Transmit Positive
ETH_RXN	171	I	Receive Negative
ETH_RXP	173	I	Receive Positive
LINK_LED	161	O	Activity Indicator
LINK_SPEED	163	O	Speed Indicator
VCC33A	169	O	3.3 V Output to Ethernet Magnetics

4.5 UARTs

The VAR-SOM-OM37has 3 UART ports.

Each UART includes a programmable baud-rate generator. Each port supports baud rates up to 3.6Mbits.

Receive and transmit FIFO fill and drain operations can be done using programmed IO or DMA transfers. To minimize CPU overhead for UART communications, device driver software can setup interrupts and DMA for data transfers to/from memory.

All three UARTs support the 16550A and 167502 functions.

VAR-SOM-OM37 UART1 signals:

Signal	Pin #	Type	Description
UART1_TX	84	O	UART Transmit
UART1_RX	90	I	UART Receive
UART1_RTS	86	O	UART HW Flow Control RTS
UART1_CTS	88	I	UART HW Flow Control CTS

VAR-SOM-OM37 UART2 signals:

Signal	Pin #	Type	Description
UART2_TX	69	O	UART Transmit
UART2_RX	71	I	UART Receive
UART2_RTS	67	O	UART HW Flow Control RTS
UART2_CTS	65	I	UART HW Flow Control CTS

VAR-SOM-OM37 UART3 signals:

Signal	Pin #	Type	Description
UART3_TX	35	O	UART Transmit
UART3_RX	33	I	UART Receive
UART3_RTS	31	O	UART HW Flow Control RTS
UART3_CTS	29	I	UART HW Flow Control CTS

4.6 USB 2.0

4.6.1 USB 2.0 Host

The VAR-SOM-OM37uses the DM/AM 37 USB 2.0 Host controller.

- The EHCI controller, based on the Enhanced Host Controller Interface (EHCI) specification for USBRelease 1.0, is in-charge of high-speed traffic (480M bit/s), over the ULPI/UTMI interface

Note:
- USB1.1 devices can be connected to the USB2.0 host port only through a USB2.0 Hub.
- USB 1.1 devices can be connected directly to the USB OTG port.

VAR-SOM-OM37 USB 2.0 Host signals:

Signal	Pin #	Type	Description
USBHOST_DP	103	IO	USB Host Data Positive
USBHOST_DN	105	IO	USB Host Data Negative
USBHOST_VBUS	107	I	USB Host VBUS 5V indicator
HOST_nOC	101	I	USB Host over-current indicator
nEN_USB_PWR	99	O	USB 2.0 Host Power Enable

4.6.2 USB 2.0 On-The-Go

The VAR-SOM-OM37 uses the DM/AM37 USB 2.0 OTG controller

Features:
- Supports USB 2.0 peripheral at High Speed (480 Mbps) and Full Speed (12 Mbps)
- Supports USB 2.0 host at High Speed (480 Mbps), Full Speed (12 Mbps), and Low Speed (1.5 Mbps)
- Operates either as the function controller of a high-/full-speed USB peripheral or as the host/peripheral in point-to-point or multipoint communications with other USB functions
- Complies the USB 2.0 standard for high-speed (480 Mbps) functions and with the on-the-go (OTG) supplement (Revision 1.0a)
- Each endpoint can support all transfer types (control, bulk, interrupt, and isochronous)
- Supports USB extensions for Session Request (SRP) and Host Negotiation (HNP)
- Supports suspend/resume and remote wakeup
- Supports high-bandwidth Isochronous and Interrupt Transfers
- Supports 15 Transmit and 15 Receive endpoints in addition to control endpoint 0
- Each endpoint has its own FIFO, with the following properties:
    - Implemented within a single, 16K-byte internal RAM

- Can be dynamically sized by software
- Can be configured to hold multiple packets (up to 8192 bytes per FIFO)
- can be accessed either by direct access of by DMA controller

- Software connect/disconnect option for peripheral
- Performs all transaction scheduling in hardware

VAR-SOM-OM37 USB 2.0 OTG signals:

Signal	Pin #	Type	Description
USB_OTG_DN	122	IO	USB OTG Data Negative
USB_OTG_DP	120	IO	USB OTG Data Positive
USB_OTG_VBUS	118	I	USB OTG VBUS indicator
USB_OTG_ID	124	I	USB OTGnHost/Client ID Low : Host mode High: Client

TPS65930 PMIC supplies maximum of 100ma on USB_OTG_VBUS , therefore, external LDO is required in host mode.

- USB_OTG_VBUS functionality:

Client mode: used as an indication of host presence.
Host mode: not used.

4.7 McBSP

The multi-channel buffered serial ports (McBSP) provide full-duplex direct serial interface between the device and other devices in a system such as audio and voice codecs.

McBSP1signals:

Signal	Pin #	Type	Description
McBSP1_CLKX	98	IO	McBSP Transmit Clock
McBSP1_FSX	100	IO	McBSP Transmit Frame Synchronization
McBSP1_DR	102	I	McBSP Receive Serial Data
McBSP1_DX	104	(I)O	McBSP Transmit Serial Data
McBSP1_FSR	106	IO	McBSP Receive Frame Synchronization
McBSP1_CLKR	108	IO	McBSP Receive Clock

McBSP3 signals:

Signal	Pin #	Type	Description
MCBSP_CLKX/ UART2_TX	69	I/O	McBSP Clock
McBSP3_FSX/ UART2_RX	71	I	McBSP Frame Synchronization
McBSP3_DR/ UART2_RTS	67	I	McBSP Receive Serial Data
McBSP3_DX/ UART2_CTS	65	O	McBSP Transmit Serial Data

4.8 SPI

The VAR-SOM-OM37 supports 2 SPI ports.

The McSPIports supports the following main features:

- Serial clock with programmable frequency, polarity, and phase for each channel
- Wide selection of SPI word lengths ranging from 4 bits to 32 bits
- Up to four master channels or single channel in slave mode
- Master multichannel mode:
    - Full duplex/half duplex
    - Transmit-only/receive-only/transmit-and-receive modes
    - Flexible I/O port controls per channel
    - Two direct memory access (DMA) requests (read/write) per channel
- Single interrupt line for multiple interrupt source events
- Power management through wake-up capabilities
- Enable the addition of a programmable start-bit for SPI transfer per channel (start-bit mode)
- Support start-bit write command
- Support start-bit pause and break sequence
- 64 bytes built-in FIFO available for a single channel

VAR-SOM-OM37 MsSPI2 signals:

Signal	Pin #	Type	Description
McSPI2_CLK	37	IO	MsSPI2 Clock
McSPI2_SIMO	39	IO	MsSPI2 SIMO Signal
McSPI2_SOMI	41	IO	MsSPI2 MISO Signal
McSPI2_CS0	66	IO	MsSPI2 Chip Select 0 Signal

VAR-SOM-OM37 McSPI4 signals[1]:

Signal	Pin #	Type	Description
McSPI4_CLK/McBSP1_CLKR	108	IO	MsSPI4 Clock
McSPI4_SIMO/McBSP1_DX	104	IO	MsSPI4 SIMO Signal
McSPI4_SOMI/McBSP1_DR	102	IO	MsSPI4 MISO Signal
McSPI4_CS0/McBSP1_FSX	100	IO	MsSPI4 Chip Select 0 Signal

~~(*) Note: multiplexed with McBSP1 signals.~~

[1] Multiplexed with McBSP1 signals

VAR-SOM-OM37 McSPI3 signals:

Signal	Pin #	Type	Description
McSPI3_CLK /MMC2_CLK	164	IO	MsSPI3 Clock
McSPI3_SIMO / MMC2_CMD	166	IO	MsSPI3 SIMO Signal
McSPI3_SOMI / MMC2_DAT0	168	IO	MsSPI3SOMI Signal
McSPI3_CS0 / MMC2_DAT3	174	IO	MsSPI3 Chip Select 0 Signal
McSPI3_CS1 / MMC2_DAT2	172	IO	MsSPI3 Chip Select 1 Signal

(*) Note: multiplexed with MMC2 signals.

4.9 I2C

The I2C controller can be configured as a slave or master.

VAR-SOM-OM37 I2C3 signals:

Signal	Pin #	Type	Description
I2C3_SCL	63	IO	I2C3 I^2C Clock. Requires 4k pull-up to 1.8v
I2C3_SDA	61	IO	I2C3 I^2C Data. Requires 4k pull-up to 1.8v

4.10 HDQ/1-Wire

The HDQ/1-Wire module implements the hardware protocol of the master functions of the BenchmarkHDQ and the Dallas Semiconductor 1-Wire® protocols. These protocols use a single wire forcommunication between the master (HDQ/1-Wire controller) and the slave (HDQ/1-Wire externalcompliant device).

VAR-SOM-OM371-Wire / HDQ signals:

Signal	Pin #	Type	Description
HDQ	82	IO	HDQ / 1-Wire IO Signal

4.11 SD /MMC

The VAR-SOM-OM37has two SD / MMC interfaces

The MMC/SD/SDIO host controllers deal with MMC/SD/SDIO protocol at transmission level, data packing, adding cyclic redundancy checks (CRC), start/end bit, and checking for syntactical correctness.

The application interface can send every MMC/SD/SDIO command and either poll for the status of the adapter or wait for an interrupt request, which is sent back in case of exceptions or to warn of end of operation.

The application interface can read card responses or flag registers. It can also mask individual interrupt sources. All these operations can be performed by reading and writing control registers. The MMC/SD/SDIO host controller also supports two DMA channels.

MMC1 signals (Up to 4 data bits):

Signal	Pin #	Type	Description
MMC1_DAT0	36	IO	MMC1 Data
MMC1_DAT1	38	IO	MMC1 Data
MMC1_DAT2	40	IO	MMC1 Data
MMC1_DAT3	42	IO	MMC1 Data
MMC1_CLKO	32	O	MMC Clock
MMC1_CMD	43	O	MMC command
MMC1_CD	91	I	MMC Card Detect

MMC2signals (Up to 4 data bits):

- Automatic Card detection not included in BSP
- 3.3v Devices require external transceiver. Consult support for 3.3v devices.

Signal	Pin #	Type	Description
MMC2_DAT0	168	IO	MMC2 Data
MMC2_DAT1	170	IO	MMC2 Data
MMC2_DAT2	172	IO	MMC2 Data
MMC2_DAT3	174	IO	MMC2 Data
MMC2_CLK	164	O	MMC2 Clock
MMC2_CMD	166	O	MMC2 command
MMC2_DIR_CMD	191	IO	MMC2 CMD line direction. For External 1.8v -> 3.3v transceiver.
MMC2_DIR_DAT_0	193	O	MMC2 Data lines direction. For External 1.8v -> 3.3v transceiver.
MMC2_CMD_CLKING	195	I	MMC2 clock-in loopback

4.12 PWM

The VAR-SOM-OM37provides a PWM line from the TPS65930 Companion Chip.

Signal	Pin #	Type	Description
PWM0	189	O	PWM signal

Other PWM outputs from the DM/AM 37xx processor (Not Supported by default BSP):

Signal	Pin #	Type	Description
MsSPI2_SIMO	39	IO	GPT9
MsSPI2_SOMI	41	IO	GPT10
MsSPI2_CS0	66	IO	GPT11

4.13 Local Bus

The general-purpose memory controller (GPMC) is used to interface external memory devices:

- SRAMs
- Asynchronous, synchronous, and page mode (only available in non-muxed mode) burst NOR flash devices
- NAND flashes
- Pseudo-SRAM devices

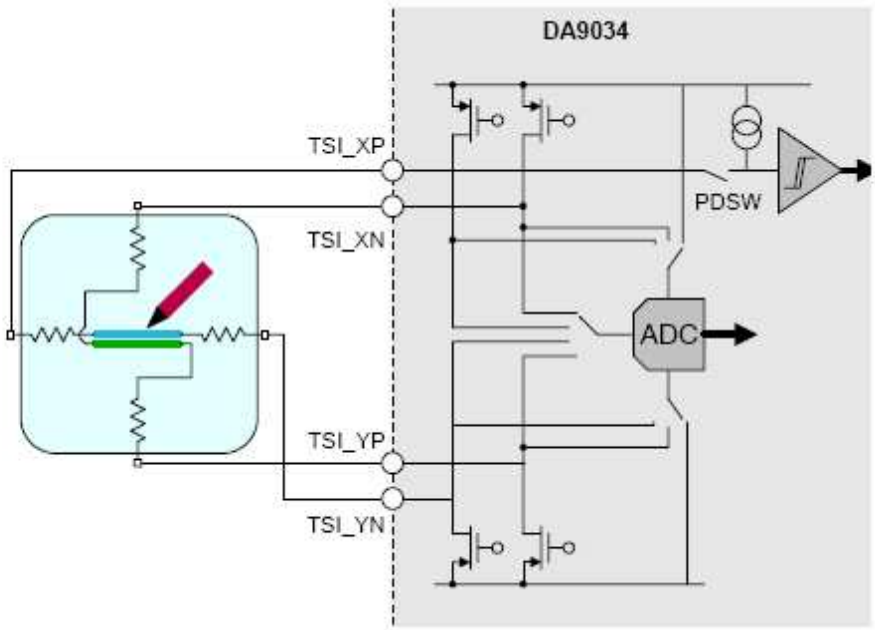
VAR-SOM-OM37Local bus signals:

Signal	Pin #	Type	Description
LB_IO_0	149	IO	Local Bus Data
LB_IO_1	147	IO	Local Bus Data
LB_IO_2	145	IO	Local Bus Data
LB_IO_3	143	IO	Local Bus Data
LB_IO_4	141	IO	Local Bus Data
LB_IO_5	139	IO	Local Bus Data
LB_IO_6	137	IO	Local Bus Data
LB_IO_7	135	IO	Local Bus Data
LB_IO_8	133	IO	Local Bus Data
LB_IO_9	131	IO	Local Bus Data
LB_IO_10	129	IO	Local Bus Data
LB_IO_11	132	IO	Local Bus Data
LB_IO_12	138	IO	Local Bus Data
LB_IO_13	140	IO	Local Bus Data
LB_IO_14	134	IO	Local Bus Data
LB_IO_15	136	IO	Local Bus Data
LB_IO_A1	142	O	Local Bus Address
LB_IO_A2	144	O	Local Bus Address
LB_IO_A3	146	O	Local Bus Address
LB_IO_A4	150	O	Local Bus Address
LB_IO_A5	153	O	Local Bus Address
LB_IO_A6	155	O	Local Bus Address
LB_IO_A7	157	O	Local Bus Address
LB_IO_A8	130	O	Local Bus Address
LB_IO_A9	128	O	Local Bus Address
LB_CLE	152	O	Local Bus CLE
LB_nADV_ALE	154	O	Local Bus Address latch enables muxed with Local bus address valid
LB_WE_N	160	O	Local Bus Write enable (active low)
LB_RE_OE_N	125	O	Output enable (active low). Also used as read enable

LB_WAIT0	148	I	Local Bus Wait
LB_CLK	87	IO	Local Bus Clock
LB_nCS3	89	O	Local Bus Chip Select 3
LB_nCS4	52	O	Local Bus Chip Select 4
SYS_nDMAREQ	85	I	Local Bus SDMA Request 1

4.14 Touch Screen

- Compatible with 4-wire resistive Touch Screens
- Pen-detection and nIRQ generation
- Supports several schemes of measurement averaging to filter noise
- Maximum X & Y sample rate (without averaging): 100hz



The VAR-SOM-OM37Touch-screen controller signals:

Signal	Pin #	Type	Description
TSMX	77	I	Touch Screen X Minus
TSMY	79	I	Touch Screen Y Minus
TSPX	73	I	Touch Screen X Plus
TSPY	75	I	Touch Screen Y Plus

4.15 Keypad

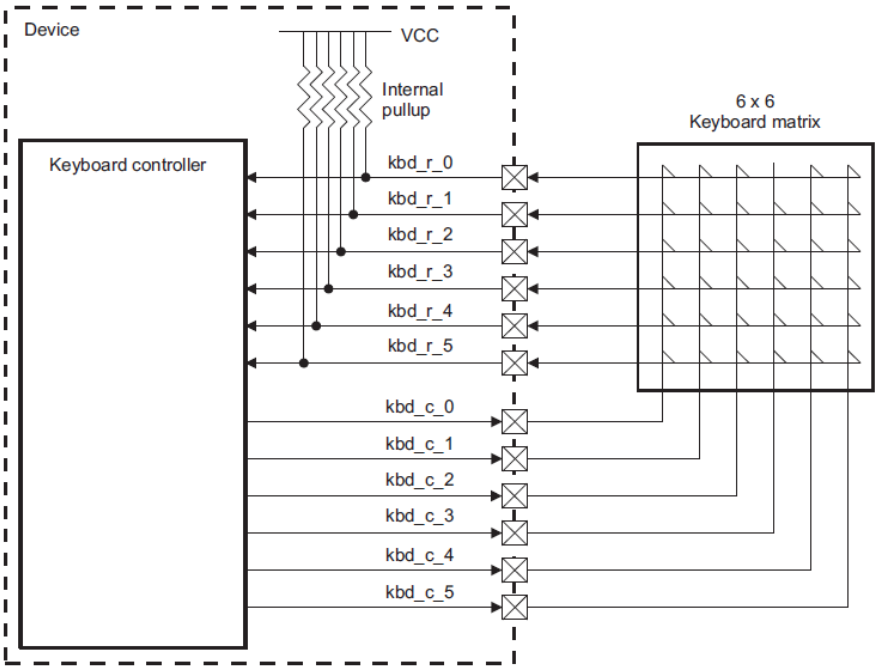
The VAR-SOM-OM37uses the TPS65930 keypad controller.

When a key button of the keyboard matrix is pressed, the corresponding row and column lines are shorted. To allow key press detection, all input pins (KBR) are pulled up to VCC and all output pins (KBC) are driven to a low level.

Any action on a button generates an interrupt to the sequencer.

The decoding sequence is written to allow detection of simultaneous press actions on several key buttons. The keyboard interface can be used with a smaller keyboard area than 6 ´ 6. To use a 3 ´ 3 keyboard, KBR(4) and KBR(5) must be tied high to prevent any scanning process distribution.

Block Diagram



VAR-SOM-OM37 Touch Screen Controller signals:

Signal	Pin #	Type	Description
KPD.R0	184	I	Keypad Row
KPD.R1	182	I	Keypad Row
KPD.R2	180	I	Keypad Row
KPD.R3	178	I	Keypad Row
KPD.R4	176	I	Keypad Row
KPD.R5	175	I	Keypad Row
KPD.C0	177	I	Keypad Column

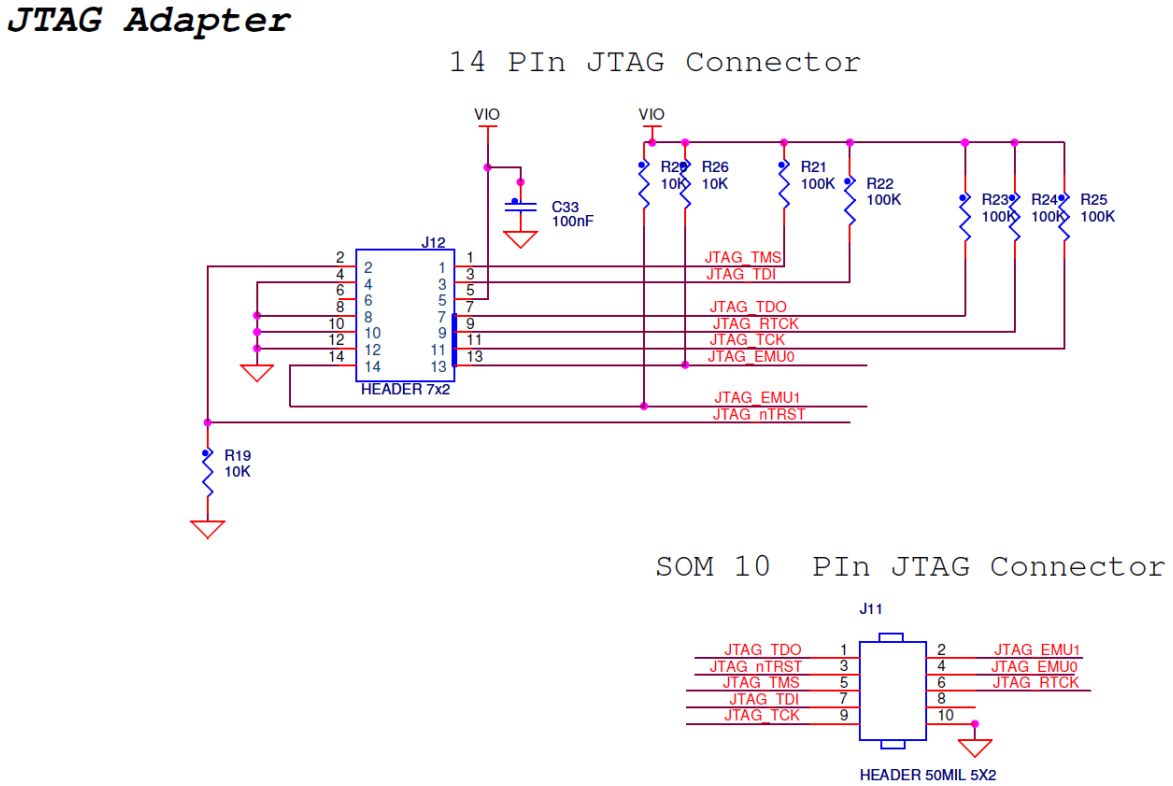
KPD.C1	179	I	Keypad Column
KPD.C2	181	I	Keypad Column
KPD.C3	183	I	Keypad Column
KPD.C4	185	I	Keypad Column
KPD.C5	187	I	Keypad Column

4.16 JTAG (J1 on SOM)

The VAR-SOM-OM37 has a dedicated JTAG connector

Signal	Pin #	Type	Description
JTAG_TDO	1		
JTAG_EMU1	2		
JTAG_nTRST	3		
JTAG_EMU0	4		
JTAG_TMS	5		
JTAG_RTCK	6		
JTAG_TDI	7		
JTAG_TCK	9		
GND	10		

Standard 14pin header -> SOM JTAG connector adapter can be found on VAR-CB103 extension board.



4.17 Boot Option

The Boot option signal configures the boot sequence of the DM/AM 37xx processor. Use this signal to burn theBootloader on NAND Flash.

VAR-SOM-OM37boot signal:

Signal	Pin #	Type	Description
SYS_BOOT5	92	I	System Boot Option 5 [High – Burn flash]

SYS_BOOT pin configuration of SOM:

SYS_BOOT_PIN	LOGIC STATE
SYS_BOOT_0	1
SYS_BOOT_1	1
SYS_BOOT_2	1
SYS_BOOT_3	1
SYS_BOOT_4	0
SYS_BOOT_5	Boot Select
SYS_BOOT_6	1

4.18 General Purpose IOs

Most of the SOM' IO pins can be used as GPIOs.

See Chapter 3 for a complete SBC connector signal list and GPIO multiplexing.

4.19 General System signals

Signal	Pin #	Type	Description
RESET_IN_N	127	I	Hardware Reset
PWRON	121	I	Control command to start or stop the system. Pull up to VBAT via 1K resistor if unused
RESET_OUT_N	97	O	Reset Signal to Base-Board Peripherals
CLK_OUT1	49	O	General Purpose Clock Out

4.20 RTC

VAR-SOM-OM37 has an on-board RTC clock which is running as long as RTC_BACKUP voltage is above 2.5v or VBAT is present

RTC_BACKUP supplies power to VRTC domain in the TPS6930 PMIC.
TPS65930 can be configured to charge Li-ion RTC backup battery.

4.21 WLAN

As from VAR-SOM-OM37 v2.3, Murata SP-9XSL-E WLAN module can be mounted on SOM, instead of the previous LSR extension board.

The WLAN module consists of the same TI WL1271 chipset => therefore no software modifications are required

WLAN module uses MMC2 interface.

The following SOM pins should be left N.C. if WLAN is installed: 164,166,168,170,172,174

4.22 Power supply pins

VAR-SOM-OM37 power supply pins:

Signal	Pin #	Type	Description
VBAT	110,112,114,116	I	VAR-SOM-OM37 single DC-IN supply voltage. Voltage range: 3.3 – 4.5V
VCC33	158	O	3.3V Output, Up to 200ma
VCC33A	169	O	3.3 V Output to Ethernet Magnetics
VIO	117	O	1.8V Output, up to 200ma
REGEN	123	O	External Regulators Enable
RTC_BACKUP	126	I	RTC backup-battery power supply

VAR-SOM-OM37 Ground pins:

Signal	Pin #	Type	Description
GND	34,47,48,51,58,60,81,83,113,115,151,156,159,162		Digital Ground

5 Absolute maximum Characteristics

Power supplies	Min	Max	Unit
Main Power supply, DC-IN	-0.3	5.5	V
3.3V output supply	3.21	3.3	V
3.3V output supply		200	ma
VIO 1.8v power output	1.79	1.82	V
VIO 1.8v power output		200	ma

6 Operational Characteristics

Power supplies	Min	Typical	Max	Unit
Main Power supply, DC-IN	3.3	3.7	4.5	V
RTC Backup battery voltage	2.5	3.0	3.2	V

Power consumption:

Power supplies	Min	Max
Main Power supply, DC-IN @ 3.7v	4ma	400ma

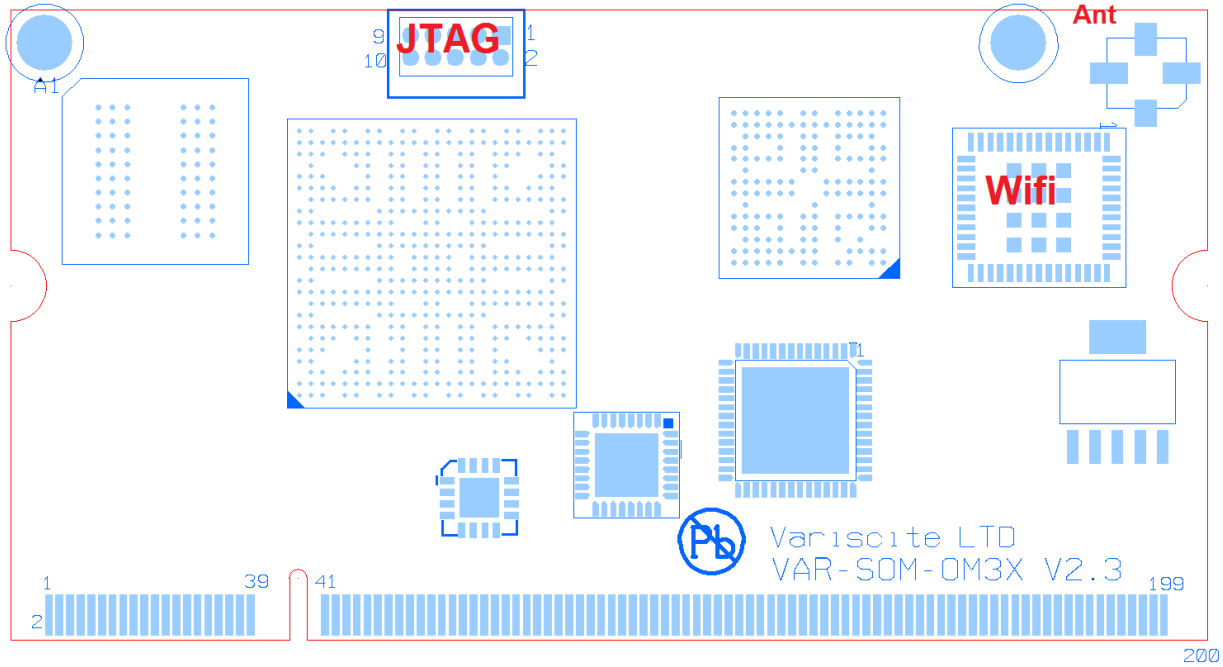
7 DC electrical characteristics

Parameter	Operating Conditions	Min	Typ	Max	Unit
MMC-1					
V_{IH}	VCC_MMC = 3.0V	1.85		3.3	V
V_{IL}		-0.2		0.6	V
V_{OH}		2.3			V
V_{OL}				0.3	V
1.8v Digital IO (UARTs, LCD, MMC2, ISP, SPI, McBSP,I2C,Local Bus, JTAG)					
V_{IH}		1.15		2.1	V
V_{IL}		-0.2		0.6	V
V_{OH}		1.4			V
V_{OL}				0.4	V
nEN_USB_PWR – TPS65930 open drain					
V_{Imax}	Max Vin			4.5	V
I_{drain}	Max current draw			60	ma
HOST_nOC– TPS65930 GPIO1					
V_{IH}		1.15		2.0	V
V_{IL}		-0.2		0.6	V
V_{OH}		1.4			V
V_{OL}				0.4	V
USB_OTG_VBUS– OTG VBUS detection					
V_{IH}		4.4		5.05	V
V_{IL}		-0.2		0.8	V
USB_OTG_ID – OTG ID					
V_{IH}		2.5		5.25	V
V_{IL}		-0.2		0.8	V
USBHOST_VBUS – Host VBUS detection					
V_{IH}		4.4		5.05	V
V_{IL}		-0.2		0.8	V

8 Environmental specifications

	Min	Max
Commercial operating temperature range	0^0C	+70^0C
Extended operating temperature range	-25^0C	+70^0C
Industrial	-40^0C	+85^0C
Variscite uses MIL-HDBK-217F-2 Parts count reliability prediction method Model: 50Deg Celsius, Class B-1, GM 50Deg Celsius, Class B-1, GB	 125 Khrs > 1450 Khrs >	
Shock resistance	50G / 20 ms	
Vibration	20G / 0 - 600 Hz	

9 Mechanical drawings



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