Ultra-low power microcontroller with 4 high drive outputs

Features

- Low Power typical 1.8µA active mode
  typical 0.5µA standby mode
  typical 0.1µA sleep mode
  @ 1.5V, 32kHz, 25 °C
- Low Voltage 1.2 to 3.3 V
- ROM 2k × 16 (Mask Programmed)
- RAM 96 × 4 (User Read/Write)
- 2 clocks per instruction cycle
- RISC architecture
- 5 software configurable 4-bit ports
- 1 High drive output port
- Up to 20 inputs (5 ports)
- Up to 16 outputs (4 ports)
- buzzer three tone
- Serial Write buffer – SWB
- Supply Voltage level detection (SVLD).
- Analogue and timer watchdog
- 8 bit timer / event counter
- Internal interrupt sources (timer, event counter, prescaler)
- External interrupt sources (portA + portC)

Description

The EM6607 is a single chip low power, mask programmed CMOS 4-bit microcontroller. It contains ROM, RAM, watchdog timer, oscillation detection circuit, combined timer / event counter, prescaler, voltage level detector and a number of clock functions. Its low voltage and low power operation make it the most suitable controller for battery, stand alone and mobile equipment. The EM6607 microcontroller is manufactured using EM's Advanced Low Power CMOS Process.
In 24 Pin package it is direct replacement for EM6603.

Typical Applications

- sensor interfaces
- domestic appliances
- clocks
- security systems
- bicycle computers
- automotive controls
- TV & audio remote controls
- measurement equipment
- R/F and IR. control
- motor driving

Figure 1. Architecture

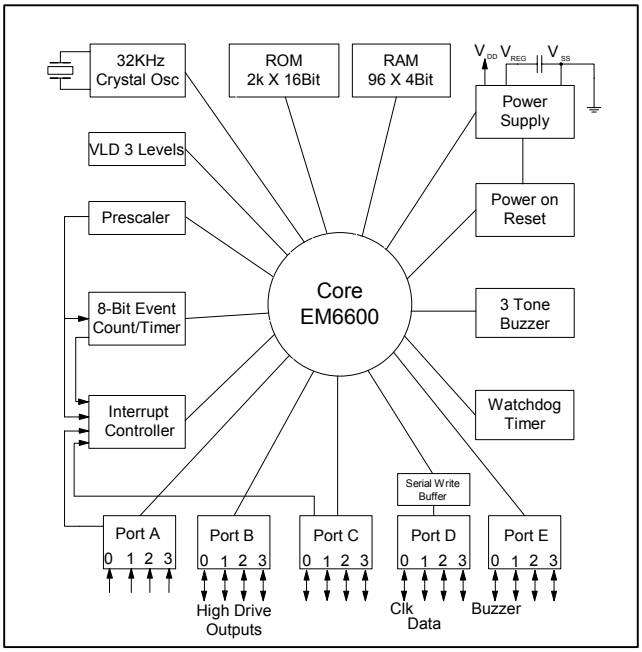
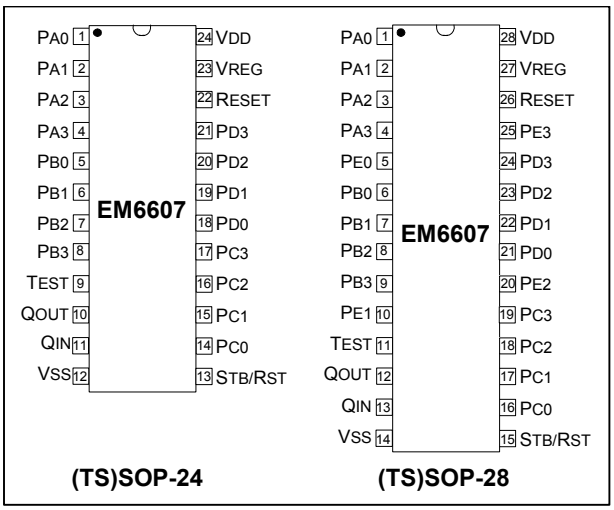


Figure 2. Pin Configuration



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EM6607 at a glance

❑ **Power Supply**
- Low Voltage, low power architecture including internal voltage regulator
- 1.2V ... 3.3 V battery voltage
- 1.8µA in active mode
- 0.5µA in standby mode
- 0.1µA in sleep mode @ 1.5V, 32kHz, 25 °C
- 32 kHz Oscillator or external clock

❑ **RAM**
- 96 x 4 bit, direct addressable

❑ **ROM**
- 2048 x 16 bit metal mask programmable

❑ **CPU**
- 4 bit RISC architecture
- 2 clock cycles per instruction
- 72 basic instructions

❑ **Main Operating Modes and Resets**
- Active mode (CPU is running)
- Standby mode (CPU in Halt)
- Sleep mode (No clock, Reset State)
- Initial reset on Power-On (POR)
- External reset pin
- Watchdog timer (time-out) reset
- Oscillation detection watchdog reset
- Reset with input combination on PortA

❑ **4-Bit Input PortA**
- Direct input read
- Debounced or direct input selectable (reg.)
- Interrupt request on input's rising or falling edge, selectable by register.
- Pull-down or Pull-up selectable by metal mask
- Software test variables for conditional jumps
- PA3 input for the event counter
- Reset with input combination on PortA (metal option)

❑ **4-Bit Input/Output PortB**
- Separate input or output selection by register
- Pull-up, Pull-down or none, selectable by metal mask if used as Input
- Buzzer output on PB0 (24-pin) / PE0 (28-pin)

❑ **4-Bit Input/Output PortC**
- Input or Output port as a whole port
- Debounced or direct input selectable (reg.)
- Interrupt request on input's rising or falling edge, selectable by register.
- Pull-up, pull-down or none, selectable by metal mask if used as input
- CMOS or N-channel open drain mode

❑ **4-Bit Input/Output PortD**
- Input or Output port as a whole port
- Pull-up, Pull-down or none, selectable by metal mask if used as Input
- CMOS or N-channel open drain mode
- Serial Write Buffer clock and data output

❑ **4-Bit Input/Output PortE**
- Separate input or output selection by register
- Pull-up, Pull-down or none, selectable by metal mask if used as Input

❑ **Serial (output) Write Buffer**
- max. 256 bits long clocked with 16/8/2/1kHz
- automatic send mode
- interactive send mode : interrupt request when buffer is empty

❑ **Buzzer Output**
- if used output on PB0 (24 pin) or PE0 (28 pin)
- 3 tone buzzer - 1kHz, 2kHz, 2.66kHz/4kHz (TBC)

❑ **Prescaler**
- 32kHz output possible on the STB/RST pin
- 15 stage system clock divider down to 1 Hz
- 3 interrupt requests: 1Hz/8Hz/32Hz
- Prescaler reset (from 8kHz to 1Hz)

❑ **8-bit Timer / Event Counter**
- 8-bit auto-reload count-down timer
- 6 different clocks from prescaler
- or event counter from the PA3 input
- parallel load
- interrupt request when comes to 00 hex.

❑ **Supply Voltage Level Detector**
- 3 software selectable levels (1.3V, 2.0V, 2.3V or user defined between 1.3V and 3.0V)
- Busy flag during measure
- Active only on request during measurement to reduce power consumption

❑ **Interrupt Controller**
- 9 external interrupt sources: 4 from PortA, 4 from PortC.
- 3 internal interrupt sources, prescaler, timer and Serial Write Buffer
- Each interrupt request is individually selectable
- Interrupt request flag is cleared automatically on register read

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1 Pin Description for EM6607

Pin Nb 24 pin	Pin Nb 28 pin	Pin Name	Function	Remarks
1	1	port A, 0	input 0 port A	interrupt request; tvar 1
2	2	port A, 1	input 1 port A	interrupt request; tvar 2
3	3	port A, 2	input 2 port A	interrupt request; tvar 3
4	4	port A, 3	input 3 port A	interrupt request; event counter input
-	5	port E, 0	input / output 0 port E	buzzer output in 28 pin package
5	6	port B, 0	input / output 0 port B	buzzer output in 24 pin package
6	7	port B, 1	input / output 1 port B	
7	8	port B, 2	input / output 2 port B	
8	9	port B, 3	input / output 3 port B	
-	10	port E, 1	input / output 1 port E	
9	11	test	test input terminal	for EM test purpose only (internal pull-down)
10	12	Q_{out}/osc 1	crystal terminal 1	
11	13	Q_{in}/osc 2	crystal terminal 2 (input)	Can accept trimming capacitor tw. V_{SS}
12	14	V_{SS}	negative power supply terminal	
13	15	STB/RST	strobe / reset status	µC reset state + port B, C, D write
14	16	port C, 0	input / output 0 port C	interrupt request
15	17	port C, 1	input / output 1 port C	interrupt request
16	18	port C, 2	input / output 2 port C	interrupt request
17	19	port C, 3	input / output 3 port C	interrupt request
-	20	port E, 2	input / output 2 port E	
18	21	port D, 0	input / output 0 port D	SWB Serial Clock Output
19	22	port D, 1	input / output 1 port D	SWB Serial Data Output
20	23	port D, 2	input / output 2 port D	
21	24	port D, 3	input / output 3 port D	
-	25	port E, 3	input / output 3 port E	
22	26	RESET	reset terminal	Active high (internal pull-down)
23	27	V_{REG}	internal voltage regulator	Needs typ. 100nF capacitor tw. V_{SS}
24	28	V_{DD}	positive power supply terminal	

Table 1. Pin Description

Figure 3. Typical Configuration: V_{DD} 1.4V up to 3.3V

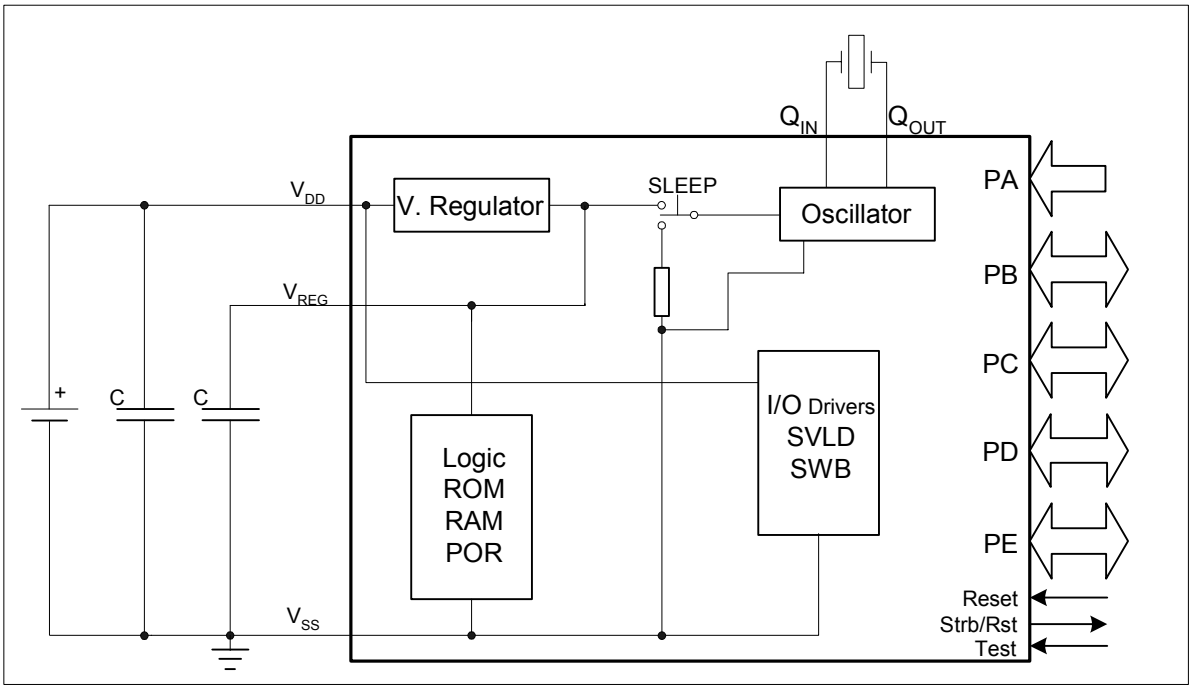
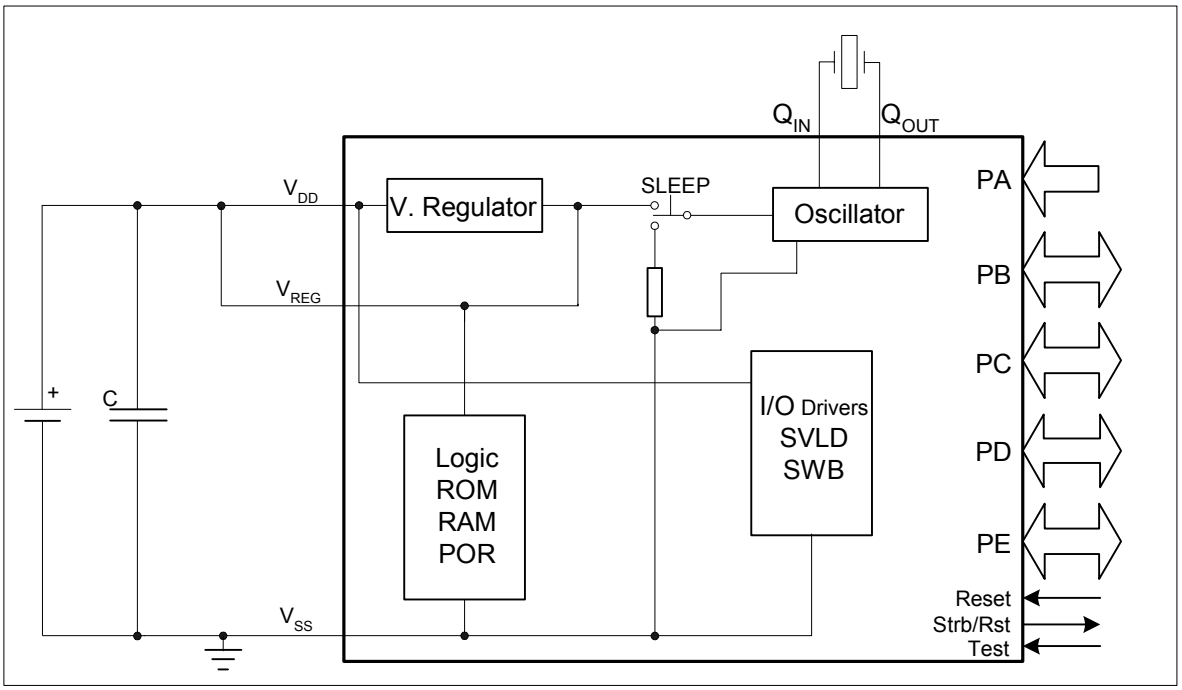


Figure 4. Typical Configuration: V_{DD} 1.2V up to 1.8V



2 Operating modes

The EM6607 has two low power dissipation modes: STANDBY and SLEEP. Figure 5 is a transition diagram for these modes.

2.1 Active Mode

The active mode is the actual CPU running mode. Instructions are read from the internal ROM and executed by the CPU. Leaving active mode via the halt instruction to go into standby mode, the **Sleep** bit write to go into Sleep mode or a reset from port A to go into reset mode.

2.2 STANDBY Mode

Executing a HALT instruction puts the EM6607 into STANDBY mode. The voltage regulator, oscillator, Watchdog timer, interrupts and timer/event counter are operating. However, the CPU stops since the clock related to instruction execution stops. Registers, RAM, and I/O pins retain their states prior to STANDBY mode. A RESET or an Interrupt request cancel STANDBY mode.

2.3 SLEEP MODE

Writing the SLEEP* bit in the IntRq* register puts the EM6607 in SLEEP mode. The oscillator stops and most functions of the EM6607 are inactive. To be able to write the SLEEP bit, the SLmask bit must be first set to 1 in register WD. In SLEEP mode only the voltage regulator and RESET input are active. The RAM data integrity is maintained. SLEEP mode may be cancelled only by a RESET at the terminal pin of the EM6607 or by the selected port A input reset combination. This combination is a metal option, see paragraph 15.1.2. The RESET port must be high for at least 10µsec.

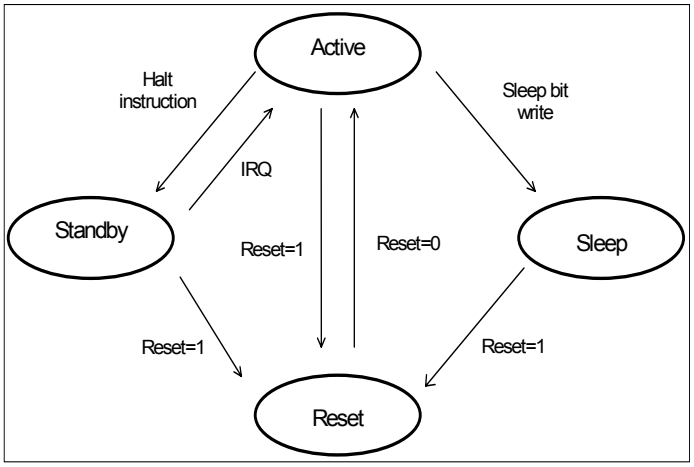


Figure 5. Mode Transition Diagram

Due to the cold start characteristics of the oscillator, waking up from SLEEP mode may take some time to guarantee that the oscillator has started correctly. During this time the circuit is in RESET state and the strobe output STB/RST is high. Waking up from SLEEP mode clears the **SLEEP** flag but not the **SLmask** bit. By reading **SLmask** it can therefore determine if the EM6607 was powered up (**SLmask** = 0), or woken from SLEEP mode (**SLmask** = 1).

Table 1. IntRq register

Bit	Name	Reset	R/W	Description
3	**INTPR**	0	R	Prescaler interrupt request
2	**INTTE**	0	R	Timer/counter interrupt request
1	**INTPC**	0	R	PortC Interrupt request
0	**INTPA**	0	R	PortA Interrupt request
2	**SLEEP**	0	W*	SLEEP mode flag

* Write bit 2 only if **SLmask**=1

Table 2. Watchdog register - WD

Bit	Name	Reset	R/W	Description
3	**WDRST**	-	R/W	Watchdog timer reset
2	**Slmask**	-	R/W	SLEEP mask bit
1	**WD1**	0	R	WD Timer data 1/4 Hz
0	**WD0**	0	R	WD Timer data 1/2 Hz

Table 3 shows the status of different EM6607 blocks in these three main operating modes.

Table 3. Internal state in Active, Stand-by and Sleep mode

Peripheral /// EM6607 mode	**ACTIVE** mode	**STAND-BY** mode	**SLEEP** mode
POR (static)	On	On	On
Voltage regulator	On	On	On (Low-Power)
Quartz 32768 Hz oscillator	On	On	Off
Clocks (Prescaler & RC divider)	On	On	Off
CPU	Running	In HALT – Stopped	Stopped
Peripheral register	"On"	"On" retain value	retain value
RAM	"On"	retain value	retain value
Timer/Counter	"On"	"On" if activated before	stopped
Supply Voltage Level Det.=SVLD	can be activated	can not be activated	Off
PortA /C, Reset pad debounced	Yes	Yes	No
Interrupts / events	Yes - possible	Yes - possible	No – not possible
Watch-Dog timer	On / Off (soft selectable)	On / Off (soft selectable)	No
Analogue Watchdog (osc.detect)	On/Off (soft select.)	"On" if activated before	Off

3 Power Supply

The EM6607 is supplied by a single external power supply between V_{DD} and V_{SS}, the circuit reference being at V_{SS} (ground). A built-in voltage regulator generates V_{REG} providing regulated voltage for the oscillator and internal logic. Output drivers are supplied directly from the external supply V_{DD}. A typical connection configuration is shown in figure 4.

For V_{DD} less then 1.4V it is recommended that V_{DD} is connected directly to V_{REG} connected

For V_{DD} >1.8V then the configuration shown in Figure 4 should be used.

*registers are marked in bold and underlined like **IntRq**

*Bits/Flags in registers are marked in bold only like **SLEEP**

4 Reset

To initialize the EM6607, a system RESET must be executed. There are five methods of doing this:

(1) Initial RESET from the oscillation detection circuit.
(2) External RESET from the RESET PIN.
(3) External RESET by simultaneous high input to terminals PA0..PA3.
(Combinations defined by metal option)
(4) Watchdog RESET (software option).
(5) Software Power-On-Reset by writing **S0ftPOR** bit in **Option2** register to "1"

During any of these RESET's the STB/RST output pin is high.

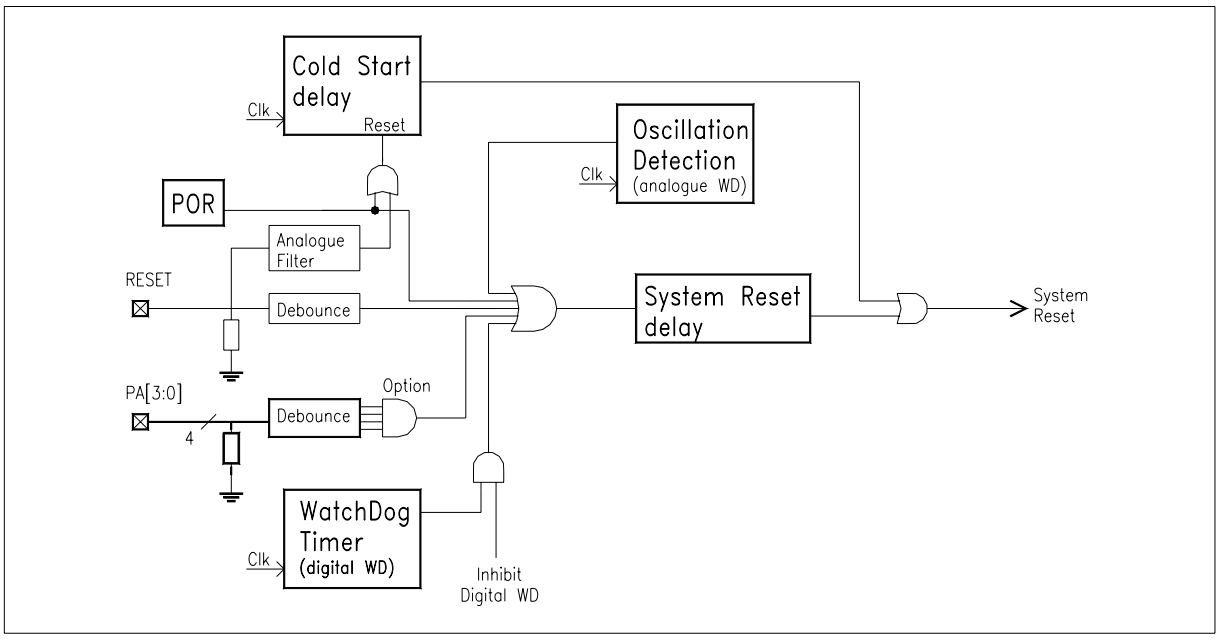


Figure 6. System reset generation

4.1 Oscillation detection circuit

At power on, the built-in voltage regulator starts to follow the supply voltage until V_{DD} becomes higher than V_{REG}. Since it is V_{REG} which supplies the oscillator and this needs time to stabilise, Power-On-Reset with the oscillation detection circuit therefore counts the first 32768 oscillator clocks after power-on and holds the system in RESET. The system will consequently remain in RESET for at least one second after power up.
After power up the Analogue Watchdog circuit monitors the oscillator. If it stops for any reason other then SLEEP mode, then a RESET is generated and the STB/RST pin is driven high.

4.2 Reset Pin

During active or STANDBY mode the RESET terminal has a debouncer to reject noise and therefore must be active high for at least 2ms or 16ms (CLK = 32kHz) - software selectable by **DebCK** in **CIRQD** register. (See Table 37)
When cancelling sleep mode, the debouncer is not active (no clock), however, reset passes through an analogue filter with a time constant of typical. 5µs. In this case Reset pin must be high for at least 10 µs to generate a system reset.

4.3 Input port (PA0..PA3) RESET

With a mask option it is possible to choose from eleven PortA reset combinations. The selected ports must be simultaneously high for at least 2ms/16ms (CLK = 32kHz) due to the presence of debouncers. Note also, that RESET with port A is not possible during SLEEP mode.

Below are the combinations of Port A (PA0..PA3) inputs, which can be used to generate a RESET. They can be selected by metal « **PortA RESET** » mask option, described in chapter 14.

Table 4. PortA Inputs RESET options (metal Hardware option)

Function	Opt. Code
NO inputs RESET	**rstpa_no**
RESET = PA0 *AND* PA1	**rstpa_3h**
RESET = PA0 *AND* PA2	**rstpa_5h**
RESET = PA1 *AND* PA2	**rstpa_6h**
RESET = PA0 *AND* PA1 *AND* PA2	**rstpa_7h**
RESET = PA0 *AND* PA3	**rstpa_9h**
RESET = PA1 *AND* PA3	**rstpa_ah**
RESET = PA0 *AND* PA1 *AND* PA3	**rstpa_bh**
RESET = PA2 *AND* PA3	**rstpa_ch**
RESET = PA0 *AND* PA2 *AND* PA3	**rstpa_dh**
RESET = PA1 *AND* PA2 AND PA3	**rstpa_eh**
RESET = PA0 *AND* PA1 *AND* PA2 *AND* PA3	**rstpa_fh**

4.4 Watchdog Timer RESET

The Watchdog Timer RESET is a software option and if used it will generate a RESET if it is not cleared. See section 5. Watchdog timer for details.

Table 5. Watchdog-Timer Option (software option)

Watchdog Function	**NoWD** bit in **Option** register
Without Watchdog Time-out reset	1
With Watchdog Time-out reset	0

4.5 Software Power-On-Reset

This is software generation of POR, which can be used mainly to reset the circuit and start again the Power-Check function if enabled to be sure that V_{DD} supply is high enough when circuit will start to work again due to increased V_{DD}.
When V_{DD} starts to decrease due to any reason and software by periodically testing the V_{DD} min by SVLD function detects this, user can generate POR at V_{DD} min and like that the circuit will go in Reset until Power-Check level is satisfied again to guarantee the proper circuit operation, not to fall in a grey zone below V_{DD} min until Static POR does it job at typ. 0.9V.

Table 6. Software Power-On-Reset

Software POR function	**SoftPOR** in **RegSoftPOR** register
Software POR start	1
No Software POR	0

4.6 CPU State after RESET

RESET initialises the CPU as shown in the table below.

Table 7. Initial Value after RESET

name	bits	symbol	initial value
Program counter 0	12	PC0	$000 (as a result of Jump 0)
Program counter 1	12	PC1	undefined
Program counter 2	12	PC2	undefined
stack pointer	2	SP	SP(0) selected
index register	7	IX	undefined
Carry flag	1	CY	undefined
Zero flag	1	Z	undefined
HALT	1	HALT	0
Instruction register	16	IR	Jump 0
periphery registers	4		see peripheral memory map

4.7 POR with Power-Check Reset

POR and Power-Check are supervising the V_{REG} (digital) which follows more or less the V_{DD} supply voltage on start-up to guarantee proper operation after Power-On. The ***resetcold*** signal is released when the V_{DD} supply voltage is high enough for the IC to function correctly.

During power-up of the EM6607 static POR (Power-On-Reset) cell supervising the V_{REG} with level of typ. 0.9V is checked to give initial reset. Reset can be prolonged also with Power-Check function if enabled by metal option. In this case V_{DD} must come above V_{L1} of the SVLD described in Chapter 11 **Supply Voltage Level Detector (SVLD)** to release the circuit reset signal and starts to execute instructions.

When Power-Check is enabled a power-check logic is switched-on with POR signal high and starts to check periodically V_{DD} against the SVLD-V_{L1} level which keeps ***resetcold*** active high until $V_{DD} > V_{L1}$. When used with external quartz first V_{DD} check starts in the middle of quartz Cold-Start sequence – after first 16384 system clocks with the same timing as in normal SVLD operation. If $V_{DD} > V_{L1}$ Power-Check condition is met and system reset will wait until first 32768 clocks needed for Quartz Cold-Start is finished and release System reset.

In case $V_{DD} < V_{L1}$, comparison will be repeated with every next 8 Hz system clock until $V_{DD} > V_{L1}$. In case of a very slow rising V_{DD}, it might happen that Quartz Cold-Start is finished. System reset will keep the EM6607 under reset until first time V_{DD} becomes higher as V_{L1} to guarantee good operating conditions (oscillator stabilized during its Cold-Start delay and V_{DD} is high enough to avoid “grey” zone between static POR and V_{L1}).

IMPORTANT: special care should be taken, when Power Supply starts to fall close to or below V_{DD} min. Frequent checking of the SVLD V_{L1} (1.3V) must be done. Between minimum V_{DD} supply of 1.2V and static POR level of 0.9V there is a grey zone, which must be avoided for proper operation.

5 Oscillator

A built-in crystal oscillator circuit generates the system-operating clock for the CPU and peripheral circuits from an externally connected crystal (typ. 32.768kHz) and trimmer capacitor (from Qin tw. V_{SS}). The regulated voltage, V_{REG}, supplies the oscillator circuit. In SLEEP mode the oscillator is stopped.
With **Fout** bit in **PA3cnt** register we can put the system 32.768 Hz frequency on STB/RST pin as output.

5.1 Prescaler

The input to the prescaler is the system clock signal. The prescaler consists of a fifteen (15) element divider chain which delivers clock signals for the peripheral circuits such as the timer/counter, buzzer, I/O debouncers and edge detectors, as well as generating prescaler interrupts.

Table 8. Prescaler interrupts source

Interrupt frequency	PSF1	PSF0
mask(no interrupt)	0	0
1 Hz	0	1
8 Hz	1	0
32 Hz	1	1

The frequency of prescaler interrupts is software selectable, as shown in Table 8.

Table 9. Prescaler control register - PRESC

Bit	Name	Reset	R/W	Description
3	**MTim**	0	R/W	Timer/Counter Interrupt Mask
2	**PRST**	-	R/W	Prescaler reset
1	**PSF1**	0	R/W	Prescaler Interrupt select 1
0	**PSF0**	0	R/W	Prescaler Interrupt select 0

6 Watchdog timer

If for any reason the CPU crashes, then the watchdog timer can detect this situation and output a system reset signal. This function can be used to detect program overrun. For normal operation the watchdog timer must be reset periodically by software at least once every three seconds (CLK = 32kHz) or a system reset signal is generated to CPU and periphery. The watchdog is active during STANDBY. Setting the **NoWD** bit to 1 in the **Option** register deactivates the watchdog-reset function.

In worst case because of prescaler reset function WD time-out can come down to 2 seconds.

Writing 1 to the WDRST bit resets the watchdog timer. Writing 0 to **WDRST** has no effect.

The watchdog timer also operates in STANDBY mode. It is therefore necessary to reset it if this mode continues for more than three seconds. One method to do so is to use the prescaler 1Hz interrupt such, that the watchdog is reset every second.

Table 10. Watchdog register - WD

Bit	Name	Reset	R/W	Description
3	**WDRST**	-	R/W	Watchdog timer reset
2	**Slmask**	-	R/W	SLEEP mask bit
1	**WD1**	0	R	WD Timer data 1/4 Hz
0	**WD0**	0	R	WD Timer data 1/2 Hz

7 INPUT and OUTPUT ports

The EM6607 has five independent 4-bit ports, as shown in Table below

Table 11. Input / Output Ports Overview

Port	Mode	Mask Options	Function(s)
PA(0:3)	Input	Pull-Up/Down (*)Debouncer (*) + or – IRQ edge RESET combination	Input Interrupt Software Test Variable PA3 input for event counter RESET input(s)
PB(0:3)	Individual input or output (high Current)	Nch open drain output Pull-Up/Down on input	Input or Output PB0 for buzzer output in 24-pin version High Current outputs
PC(0:3)	Port input or output	Pull-Up/Down (*)+ or – IRQ edge (*)Debouncer Nch open drain output	Input or Output Port Interrupt
PD(0:3)	Port input or Output	Pull-Up/Down on Input Nch open drain output	Input or Output Port PD0 -SWB serial clock output PD1 -SWB serial data output
PE(0:3)	Individual input or output	Pull-Up/Down on Input Nch open drain output	Input or Output Port PE0 for buzzer output in 28-pin version

(*) Some options can be set also by **Option** register.

Table 12. Option register - Option

Bit	Name	Reset	R/W	Description
3	**IRQedgeR**	0	R/W	Rising edge interrupt for portA&C
2	**debPCN**	0	R/W	PortC without/with debouncer
1	**debPAN**	0	R/W	PortA without/with debouncer
0	**NoWD**	0	R/W	WatchDog timer Off

IRQedgeR : Valid for both PortA and PortC input interrupt edge. By default interrupt are active on a falling edge. When set to 1 the rising edge is active.

debPAN : By default (after a reset) debouncers are enabled on whole PortA. Writing 1 removes the debouncers from the PortA.

debPCN : By default debouncers are enabled on whole PortC. Writing 1 removes the debouncers from the PortC.

NoWD : By default Watchdog timer is On (NoWD=0). Writing 1 removes the watchdog timer.

7.1 PortA

The EM6607 has one 4-bit general purpose input port. Each of the input port terminals PA3..PA0 has an internal pull-Up/Down resistor, which can be selected with mask options. Port information is directly read from the pin into a register.

On inputs PA0, PA1, PA2 and PA3 debouncers for noise rejection are added by default. For interrupt generation, either direct input and debounced input can be chosen. With the **debPAN** written to 0 in the Option register all the PortA inputs are debounced and with the **debPAN** bit at 1 none of the PortA inputs are debounced. With the debouncer selected the input must be stable for two rising edges of 1024Hz or 128Hz clocks (at 32kHz). This corresponds to a worst case of 1.95ms or 15.62msec. PortA terminals PA0, PA1 and PA2 are also used as input conditions for conditional software branches as shown on the next page:

Debounced ***PA0*** is connected to CPU ***TestVar1***
Debounced ***PA1*** is connected to CPU ***TestVar2***
Debounced ***PA2*** is connected to CPU ***TestVar3***

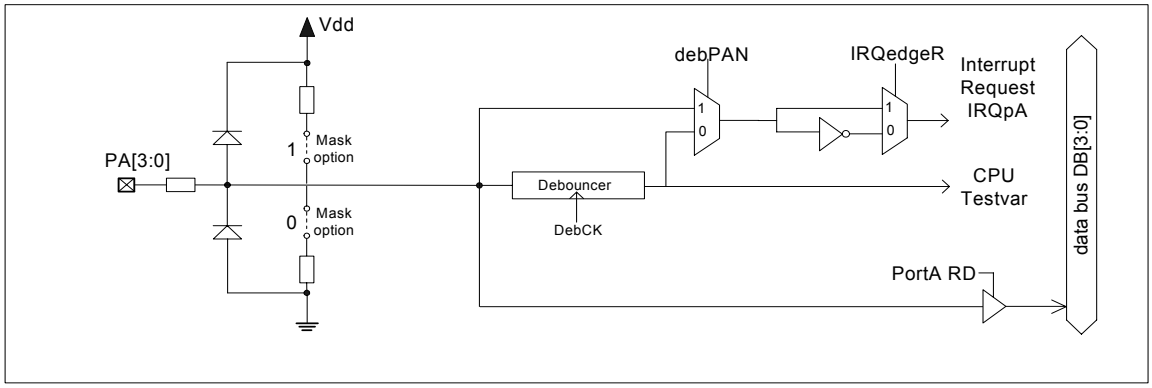


Figure 7. Port A

Additionally, PA3 can also be used as the input terminal for the event counter.

The input port PA(0:3) has also individually selectable interrupts. Each port has its own interrupt mask bit in the **MPortA** register. When an interrupt occurs, reading of the **IRQpA** and the **IntRq** registers allows identifying the source of the interrupt. The **IRQpA** register is automatically cleared by reading the register or by a RESET,. Reading **IRQpA** register also clears the **INTPA** flag in **IntRq** register. At initial RESET the **MPortA** is set to 0, thus disabling any input interrupts.

See paragraph 9 for further details about the interrupt controller.

7.1.1 PortA registers

Table 13. PortA input status register - PortA

Bit	Name	Reset	R/W	Description
3	**PA3**	-	R	PA3 input status
2	**PA2**	-	R	PA2 input status
1	**PA1**	-	R	PA1 input status
0	**PA0**	-	R	PA0 input status

Table 14. PortA Interrupt request register - IRQpA

Bit	Name	Reset	R/W	Description
3	**IRQpa3**	0	R	input PA3 interrupt request flag
2	**IRQpa2**	0	R	input PA2 interrupt request flag
1	**IRQpa1**	0	R	input PA1 interrupt request flag
0	**IRQpa0**	0	R	input PA0 interrupt request flag

Table 15. PortA interrupt mask register - MportA

Bit	Name	Reset	R/W	Description
3	**MPA3**	0	R/W	interrupt mask for input PA3
2	**MPA2**	0	R/W	interrupt mask for input PA2
1	**MPA1**	0	R/W	interrupt mask for input PA1
0	**MPA0**	0	R/W	interrupt mask for input PA0

7.2 PortB

Port B is a 4-bit general-purpose I/O port. Outputs on this port are high current outputs. Each bit PB(0:3) can be separately configured by software to be either input or output by writing to the corresponding bit of the **CIOPortB** control register. The **PortB** register is used to read data when in input mode and to write data when in output mode. On each terminal controlled Pull-Up/Down resistor can be selected by metal option, which are active only when selected as input. Special case is when we want to use internal Strong Pull-Up resistor also when PortB terminal is declared as N-channel open drain output and internal Pull-Up resistor is used to pull up the output (not-controlled Pull-Up). This is a special option "**sod**" = strong Pull-Up for Open drain- active all the time (when terminal is input or output).

Writing 0 to the corresponding bit in the CIOPortB register sets input mode. This results in a high impedance state with the status of the pin being read from register **PortB.** Writing 1 to the corresponding bit in the CIOPortB register sets output mode. Consequently the output terminal follows the status of the bits in the **PortB** register. At initial RESET the **CIOPortB** register is set to 0, thus setting the port to input. Additionally, PB0 can also be used as a three-tone buzzer output. For details see section 7, Buzzer.

7.2.1 PortB registers

Table 16. PortB input/output status register - PortB

Bit	Name	Reset	R/W	Description
3	**PB3**	-	R/W	PB3 I/O data
2	**PB2**	-	R /W	PB2 I/O data
1	**PB1**	-	R/W	PB1 I/O data
0	**PB0**	-	R /W	PB0 I/O data

Table 17. PortB Input/Output control register - CIOportB

Bit	Name	Reset	R/W	Description
3	**CIOPB3**	0	R/W	PB3 Input/Output select
2	**CIOPB2**	0	R/W	PB2 Input/Output select
1	**CIOPB1**	0	R/W	PB1 Input/Output select
0	**CIOPB0**	0	R/W	PB0 Input/Output select

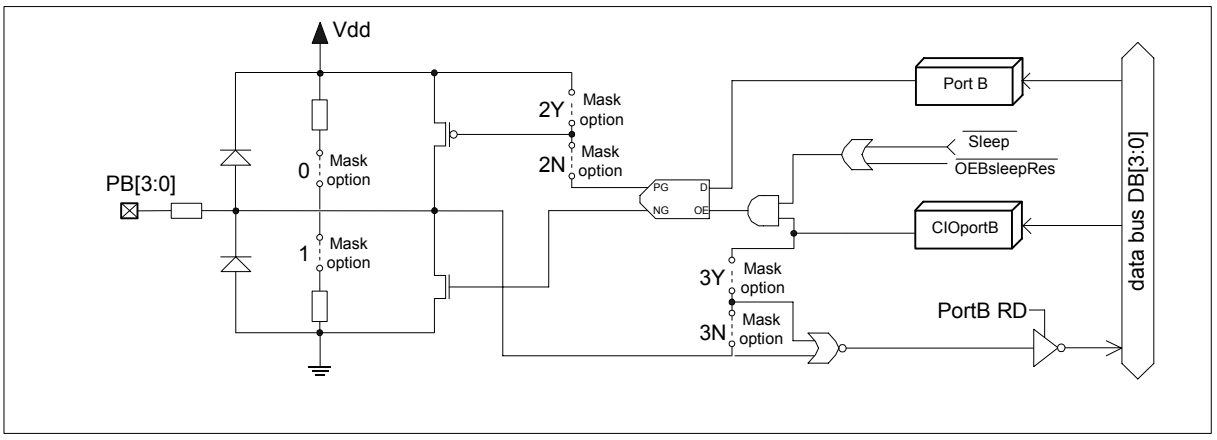


Figure 8. Port B

If metal mask option ***3Y*** (Input blocked when Output) is used and port is declared as Output (**CIOPortB** = 1111b) the real port information cannot be read directly. In this case no direct logic operations (like AND **PortB**) on Output ports are possible. This logic operation can be made with an image of the Port saved in the RAM which we store after on the output port. This is valid for PortB, PortC and PortD when declared as output and the metal Option ***3Y*** is used. In the case of metal option ***3N*** selected direct logic operations on output ports are possible.

If **OEBsleepRes** bit in **Option2** register is set to "1" (Output Hi-Z in SLEEP mode) the active Output will go tri-state when the circuit goes into SLEEP mode. In the case of **OEBsleepRes** at "0", output stays active also in the SLEEP mode.

7.3 PortC

This port can be configured as either input or output (but it is not bitwise selectable). When in input mode it implements the identical interrupt functions as PortA. The **PortC** register is used to read data when input mode and to write data when in output mode. Input mode is set by writing 0 in the I/O control bit **CIOPC** in register **CPIOB,** the input becomes high impedance. On each terminal controlled Pull-Up/Down resistor can be selected by metal option, which are active only when port is input. When we want to use internal Strong pull-up resistor also when PortC terminal is declared as N-channel open drain output and internal pull-up resistor is used to pull up the output (not-controlled pull-up). This is a special option "**sod**" = strong pull-up for Open drain- active all the time (when terminal is input or output).

The output mode is selected by writing 1 to **CIOPC** bit, and the terminal follows the bits in the **PortC** register. When PortC is used as an input, interrupt functions as described for PortA can be enabled. Input to the interrupt logic can be direct or via a debounced input. With the **debPCN** bit at 0 in the Option register all the PortC inputs are debounced and with the **debPCN** bit at 1 none of the PortC inputs are debounced. **MPortC** is the interrupt mask register for this port and **IRQpC** is the portC interrupt request register. See also section 9.

By writing the **PA&C** bit in the **CPIOB** data register it is possible to combine PortA and PortC interrupt requests (logic AND) as shown in Table 17

At initial reset, the **CPIOC** control register is set to 0, and the port is in input mode. The **MPortC** register is also set to 0, therefore disabling interrupts.

Table 18. Ports A&C Interrupt

IRQPA	IRQPC	PA&C	Request to CPU
0	0	X	No
0	1	0	Yes
1	0	0	Yes
1	1	0	Yes
0	1	1	No
1	0	1	No
1	1	1	Yes

7.3.1 PortC registers

Table 19. PortC input/output register - PortC

Bit	Name	Reset	R/W	Description
3	**PC3**	-	R/W	PC3 I/O data
2	**PC2**	-	R /W	PC2 I/O data
1	**PC1**	-	R/W	PC1 I/O data
0	**PC0**	-	R /W	PC0 I/O data

Table 20. PortC Interrupt request register - IRQpC

Bit	Name	Reset	R/W	Description
3	**IRQpc3**	0	R	input PC3 interrupt request flag
2	**IRQpc2**	0	R	input PC2 interrupt request flag
1	**IRQpc1**	0	R	input PC1 interrupt request flag
0	**IRQpc0**	0	R	input PC0 interrupt request flag

Table 21. PortC interrupt mask register - MportC

Bit	Name	Reset	R/W	Description
3	**MPC3**	0	R/W	interrupt mask for input PC3
2	**MPC2**	0	R/W	interrupt mask for input PC2
1	**MPC1**	0	R/W	interrupt mask for input PC1
0	**MPC0**	0	R/W	interrupt mask for input PC0

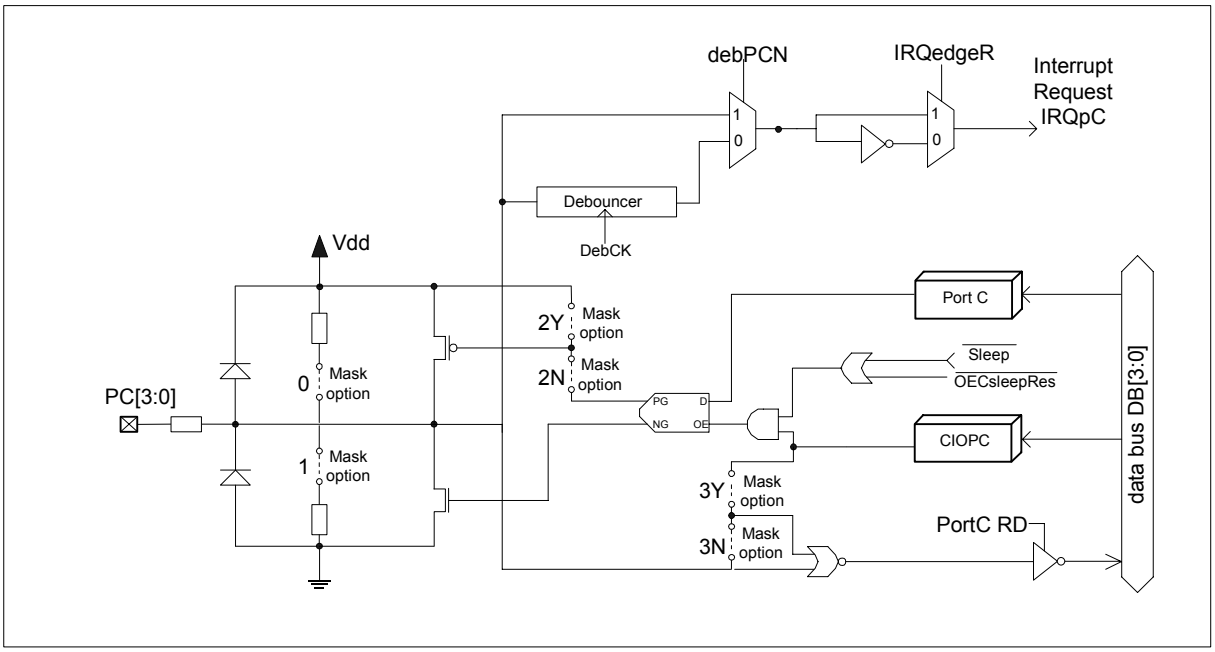


Figure 9. Port C

If **OECsleepRes** bit in **Option2** register is set to "1" (=***6Y*** (Output Hi-Z in SLEEP mode)) the active Output will go tri-state when the circuit goes into SLEEP mode. In the case of ***6N*** - **OECsleepRes** at "0", output stay active also in the SLEEP mode.

Table 22. Option2 register - Option2

Bit	Name	Reset	R/W	Description
3	**OEDsleepRes**	0	W	PortD Output Enable reset by Sleep mode
2	**OECsleepRes**	0	W	PortC Output Enable reset by Sleep mode
1	**OEBsleepRes**	0	W	PortB Output Enable reset by Sleep mode
0	**BuzzerPE0**	0	W	Buzzer on PE0 if 1, on PB0 if 0

7.4 PortD

The EM6607 has one all purpose I/O port similar to PortC but without interrupt capability. The **PortD** register is used to read input data when an input and to write output data for output. The input line can be pulled Up/Down (metal option) when the port is used as input. Input mode is set by writing 0 to the I/O control bit **CIOPD** in register **CPIOB**, and the terminal becomes high impedance. On each terminal controlled Pull-Up/Down resistor can be selected by metal option which are active only when selected as input. Special case is when we want to use internal Strong pull-up resistor also when PortC terminal is declared as N-channel open drain output and internal pull-up resistor is used to pull up the output (not-controlled pull-up). This is a special option "**sod**" = strong pull-up for Open drain- active all the time (when terminal is input or output).

Output mode is set by writing 1 to the control bit **CIOPD.** Consequently, the terminal follows the status of the bits in the **PortD** register. If Serial Write Buffer function is enabled PD0 and PD1 terminals of PortD output serial clock and serial data respectively. For details see **11.0 Serial Write Buffer**.

7.4.1 PortD registers

Table 23. PortD Input/Output register - PortD

Bit	Name	Reset	R/W	Description
3	**PD3**	0	R/W	PD3 I/O data
2	**PD2**	0	R/W	PD2 I/O data
1	**PD1**	0	R/W	PD1 I/O data
0	**PD0**	0	R/W	PD0 I/O data

Table 24. Ports control register - CPIOB

Bit	Name	Reset	R/W	Description
3	-	-	R/W	not used
2	**CIOPD**	0	R/W	I/O PortD select
1	**CIOPC**	0	R/W	I/O PortC select
0	**PA&C**	0	R/W	Logical AND of IRQ's from PortA & PortC

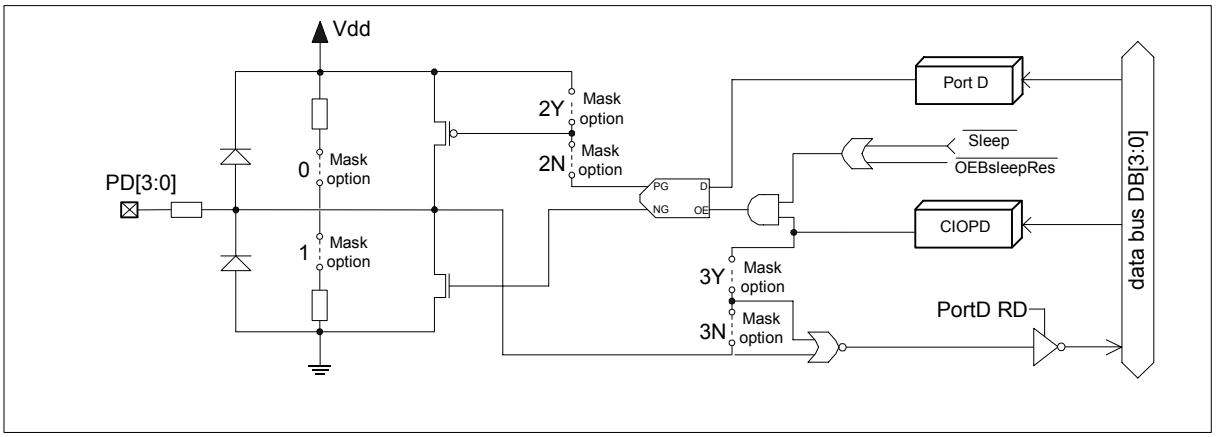


Figure 10. Port D

If **OEDsleepRes** bit in **Option2** register is set to "1" (Output Hi-Z in SLEEP mode) the active Output will go tri-state when the circuit goes into SLEEP mode. In the case of **OEDsleepRes** at "0", output stay active also in the SLEEP mode.

7.5 PortE

PortE is a 4-bit I/O port where each pad PE(0:3) can be separately configured by software to be either input or output by writing to the corresponding bit of the **CIOPortE** control register. The **PortE** register is used to read data when in input mode and to write data when in output mode. On each terminal controlled Pull-Up/Down resistor can be selected by metal option which are active only when selected as input. Special case is when we want to use internal Strong pull-up resistor also when PortC terminal is declared as N-channel open drain output and internal pull-up resistor is used to pull up the output (not-controlled pull-up). This is a special option "**sod**" = strong pull-up for Open drain- active all the time (when terminal is input or output).

Input mode is set by writing 0 to the corresponding bit in the **CIOPortE** register. This results in a high impedance state with the status of the pin being read from register **PortE.** Output mode is set by writing 1 to the corresponding bit in the **CIOPortE** register. Consequently the output terminal follows the status of the bits in the **PortE** register. At initial RESET the **CIOPortE** register is set to 0, thus setting the port to an input.

7.5.1 PortE registers

Table 25. PortE Input/Output status register - PortE

Bit	Name	Reset	R/W	Description
3	**PE3**	-	R/W	PE3 I/O data
2	**PE2**	-	R /W	PE2 I/O data
1	**PE1**	-	R/W	PE1 I/O data
0	**PE0**	-	R /W	PE0 I/O data

Table 26. PortE Input/Output control register - CIOPortE

Bit	Name	Reset	R/W	Description
3	**CIOPE3**	0	R/W	PE3 Input/Output select
2	**CIOPE2**	0	R/W	PE2 Input/Output select
1	**CIOPE1**	0	R/W	PE1 Input/Output select
0	**CIOPE0**	0	R/W	PE0 Input/Output select

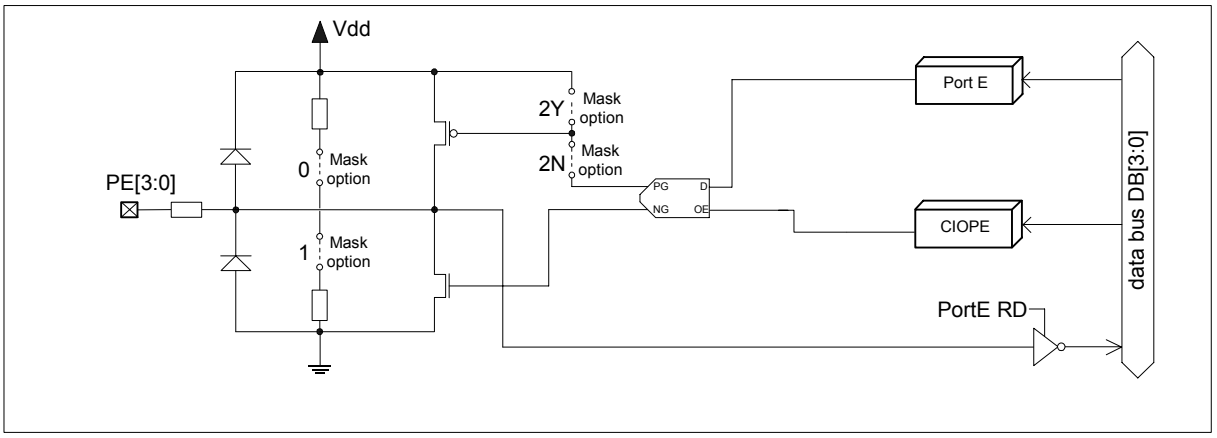


Figure 11. Port E

8 BUZZER

The EM6607 has one 50% duty cycle output with three different frequencies, which can be used to drive a buzzer. I/O terminal PB0 in 24-pin package or PE0 in 28-pin package (**BuzzerPE0** option) is used for this function when the buzzer is enabled by setting the **BUen** bit to 1 . Table 22 below shows how to select the frequency by writing to the **BCF1** and **BCF0** control flags in the **BEEP** register.

After writing to the buzzer control register **BEEP**, the chosen frequency (or silence) is selected immediately. With the **BUen** bit set to 1, the selected frequency is output at PB0 when **BuzzerPE0** is 0. When the **BUen** is set to 0 PB0 is used as a normal I/O terminal of PortB. The **BUen** bit has a higher priority over the I/O control bit **CIOPB0** in the **CIOPortB** register. In case when **BuzzerPE0** is 1 and **BUen** is set to 1 PE0 becomes output and PB0 is not influenced by buzzer function.

Tone frequency	BCF1	BCF0
silence	0	0
1024 Hz	0	1
2048 Hz	1	0
2667 Hz	1	1

Table 2. Buzzer frequency selection

8.1 Buzzer Register

Table 27. Buzzer control register - BEEP

Bit	Name	Reset	R/W	Description
3	**TimEn**	0	R/W	Timer/counter enable
2	**BUen**	0	R/W	Buzzer enable
1	**BCF1**	0	R/W	Buzzer Frequency control
0	**BCF0**	0	R/W	Buzzer Frequency control

Table 28. Buzzer output pad allocation

Buzzer on PB0 or PE0	**BuzzerPE0** in register **Option2**
Buzzer output on PE0	1
Buzzer output on PB0	0

Table 29. PB0 & PE0 function used with BUen and **BuzzerPE0** control bits

CIOPB0	CIOPE0	BUen	BuzzerPE0	Function distributions on PB0 and PE0 pads
0	0	0	X	PB0 and PE0 are Inputs
1	1	0	X	PB0 and PE0 are independent outputs
X	0	1	0	PB0 is Buzzer output, PE0 is input
0	X	1	1	PB0 is input, PE0 is Buzzer output
1	X	1	1	PB0 is general output, PE0 is Buzzer output

9 Timer/Event Counter

The EM6607 has a built-in 8 bit countdown auto-reload Timer/Event counter that takes an input from either the prescaler or Port PA3. If the Timer/Event counter counts down to $00 the interrupt request flag **IntTim** is set to 1. If the Timer/Event counter interrupt is enabled by setting the mask flag **MTimC** set to 1, then an interrupt request is generated to the CPU. See also section 9. If used as an event counter, pulses from the PA3 terminal are input to the event counter. See figure 10 and tables 28 and 29 on the next page for PA3 source selection (debounced or not, Rising/Falling edge). By default rising and debounced PA3 input is selected.

The timer control register **TimCtr** selects the auto-reload function and input clock source. At initial RESET this bit is cleared to 0 selecting no auto-reload. To enable auto-reload **TimAuto** must be set to 1. The Timer/Event counter can be enabled or disabled by writing to the **TIMen** control bit in the **BEEP** register. At initial RESET it is cleared to 0. When used as timer, it is initialised according to the data written into the timer load/status registers **LTimLS** (low 4 bits) and **HTimLS** (high four bits). The timer starts to count down as soon as the **LTimLS** value is written. When loading the Timer/Event counter registers the correct order must be respected: First, write either the control register **TimCtr** or the high data nibble **HTimLS.** The last register written should be the low data nibble **LTimLS**. During count down, the timer can always be reloaded with a new value, but the high four bits will only be accepted during the write of the low four bits.

In the case of the auto-reload function, the timer is initialised with the value of the load registers **LTimLS** and **HTimLS**. Counting with the auto-reload function is only enabled during the write to the low four bits, (writing **TimAuto** to 1 does not start the timer counting down with the last value in the timer load registers but it waits until a new **LTimLS** load). The timer counting to $00 generates a timer interrupt event and reloads the registers before starting to count down again. To stop the timer at any time, a write of $00 can be made to the timer load registers, this sets the **TimAuto** flag to 0. If the timer is stopped by writing the **TimEn** bit to 0, the timer status can be read. The current timer status can be always obtained by reading the timer registers **LTimLS** and **HTimLS**. For proper operation read ordering should be respected such that the first read should be of the **LTimLS** register followed by the **HTimLS** register. Example: To have continous 1sec timer IRQ with 128Hz one has to write 128dec (80hex) in Timer registers with auto-reload.

Using the Timer/Event Counter as the event counter allows several possibilities:

1.) Firstly, load the number of PA3 input edges expected into the load registers and then generate an interrupt request when counter reaches $00.

2.) The second is to write timer/counter to $FF, then select the event counter mode, and lastly enable the event counter by setting the **TimEn** bit to 1, which starts the count.

Because the counter counts down, a binary complement has to be done in order to get the number of events at the PA3 input.

3) Another option is to use the Timer/Event counter in conjunction with the prescaler interrupt, such that it is possible to count the number of the events during two consecutive 32Hz, 8Hz or 1Hz prescaler interrupts.

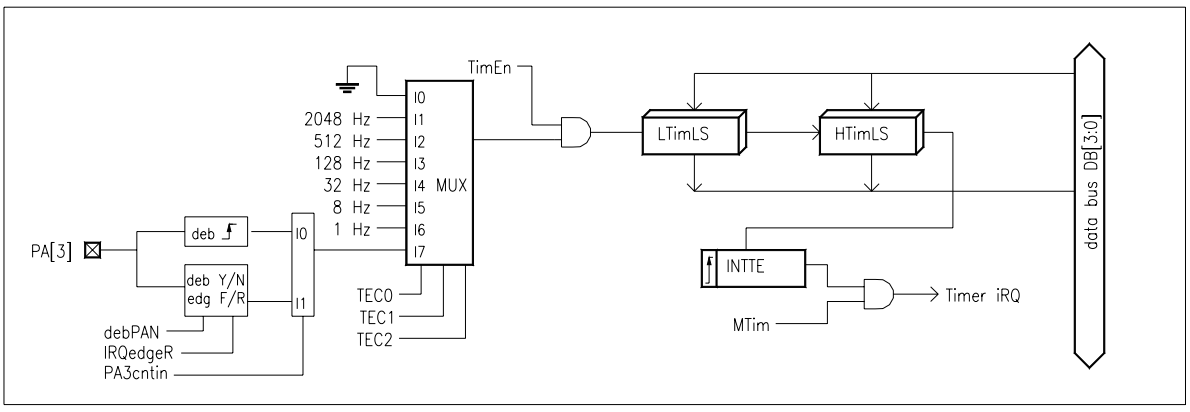


Figure 12. Timer / Event Counter

Table below shows the selection of inputs to the Timer/Event counter.

Table 30. Timer Clock Selection

TEC2	TEC1	TEC0	Timer/Counter clock source
0	0	0	not active
0	0	1	2048 Hz from prescaler
0	1	0	512 Hz from prescaler
0	1	1	128 Hz from prescaler
1	0	0	32 Hz from prescaler
1	0	1	8 Hz from prescaler
1	1	0	1 Hz from prescaler
1	1	1	PA3 input terminal (see tables 28 and 29)

9.1 Timer/Counter registers

Table 31. Timer control register - TimCtr

Bit	Name	Reset	R/W	Description
3	**TimAuto**	0	R/W	Timer/Counter AUTO reload
2	**TEC2**	0	R/W	Timer/Counter mode 2
1	**TEC1**	0	R/W	Timer/Counter mode 1
0	**TEC0**	0	R/W	Timer/Counter mode 0

Table 32. LOW Timer Load/Status register - LTimLS (4 low bits)

Bit	Name	Reset	R/W	Description
3	**TL3/TS3**	0	R/W	Timer load/status bit 3
2	**TL2/TS2**	0	R/W	Timer load/status bit 2
1	**TL1/TS1**	0	R/W	Timer load/status bit 1
0	**TL0/TS0**	0	R/W	Timer load/status bit 0

Table 33. HIGH Timer Load/Status register - HTimLS (4 high bits)

Bit	Name	Reset	R/W	Description
3	**TL7/TS7**	0	R/W	Timer load/status bit 7
2	**TL6/TS6**	0	R/W	Timer load/status bit 6
1	**TL5/TS5**	0	R/W	Timer load/status bit 5
0	**TL4/TS4**	0	R/W	Timer load/status bit 4

Table 34. PA3 counter input selection register - PA3cnt

bit	Name	Reset	R/W	Description
3	-	0	-	empty
2	**WDanadis**	0	R/W	Analogue WD disable
1	**Fout**	0	R/W	System freq. output on STB/RST pad
0	**PA3cntin**	0	R/W	PA3 input status

Table 35. PA3 counter input selection

PA3cntin	debPAN	IRQedgeR	Counter source
0	X	X	PA3 debounced rising edge
1	0	0	PA3 debounced falling edge
1	0	1	PA3 debounced rising edge
1	1	0	PA3 not debounced falling edge
1	1	1	PA3 not debounced rising edge

X (Don't care)

10 Interrupt Controller

The EM6607 has 12 different interrupt sources, each of which is maskable. These are:

External (9)	- PortA PA3..PA0 inputs
	- PortC PC3..PC0 inputs
	- Combined AND of PortA * PortC
Internal (3)	- Prescaler (32Hz / 8Hz / 1Hz)
	- Timer/Event counter
	- SWB in interactive mode

For an interrupt to the CPU to be generated, the interrupt request flag must be set (**INTxx**), and the corresponding mask register bit must be set to 1 (**Mxx**), the general interrupt enable flag (**INTEN**) must also be set to 1. The interrupt request can be masked by the corresponding interrupt mask registers **MPortx** for each input interrupt and by **PSF0** ,**PSF1** and **MTim** for internal interrupts. At initial reset the interrupt mask bits are set to 0. **INTEN** bit is set automatically to 1 by Halt Instruction except when starting the Automatic SWB transfer (see Serial Write Buffer (SWB) chapter 11)

The CPU is interrupted when one of the interrupt request flags is set to 1 in register **IntRq** and the **INTEN** bit is enabled in the control register **CIRQD**. **INTTE** and **INTPR** flags are cleared automatically after a read of the **IntRq** register. The other two interrupt flags **INTPA** (IRQ from PortA) and **INTPC** (IRQ from PortC) in the **IntRq** register are cleared only after reading the corresponding Port interrupt request registers **IRQpA** and **IRQpC**. At the Power on reset and in SLEEP mode the **INTEN** bit is also set to 0 therefore not allowing any interrupt requests to the CPU until it is set to 1 by software.

Since the CPU has only one interrupt subroutine and because the **IntRq** register is cleared after reading, the CPU does not miss any of the interrupt requests which come during the interrupt service routine. If any occur during this time a new interrupt will be generated as soon as the CPU comes out of the current interrupt subroutine. Interrupt priority can be controlled through software by deciding which flag in the **IntRq** register should be serviced first.

For SWB interactive mode interrupt see section 11.0 Serial Write Buffer.

10.1 Interrupt control registers

Table 36. Main Interrupt request register - IntRq (Read Only)*

Bit	Name	Reset	R/W	Description
3	**INTPR**	0	R	Prescaler interrupt request
2	**INTTE**	0	R	Timer/counter interrupt request
1	**INTPC**	0	R	PortC Interrupt request
0	**INTPA**	0	R	PortA Interrupt request
2	**SLEEP**	0	W*	SLEEP mode flag

* Write bit 2 only if **SLmask**=1

If the **SLEEP** flag is written with 1 then the EM6607 goes immediately into SLEEP mode (**SLmask** was at 1).

Table 37. Register - CIRQD

Bit	Name	Reset	R/W	Description
3	-	0	R/W	Reserved, must written to 0
2	-	0	R/W*	Reserved, must written to 0
1	**DebCK**	0	R/W	Debouncer clock select (0=2ms : 1=16ms)
0	**INTEN**	0	R/W	Enable interrupt to CPU (1=enabled)

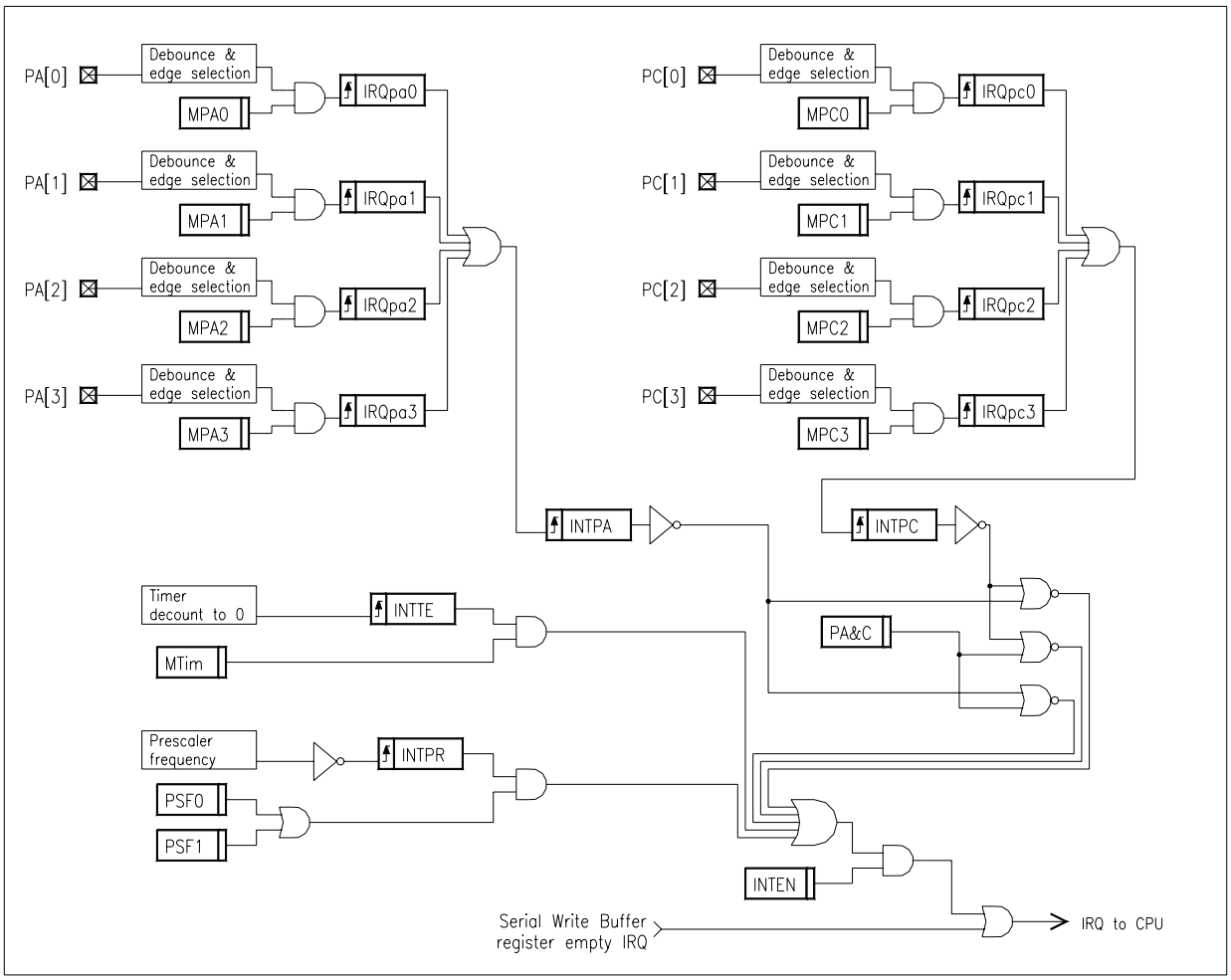


Figure 13. Interrupt Request generation

IRQ mask bit which can be written to 0 or 1 (1 to enable an interrupt)

interrupt request flag which is set on the input rising edge.

Timer IRQ flag **INTTE** and prescaler IRQ flag **INTPR** arrive independent of their mask bits not to loose any timing information. But the µprocessor will be interrupted only with mask set to 1.

11 Supply Voltage Level Detector (SVLD)

The EM6607 has a software configurable Supply Voltage Level detector. Three levels can be defined within the power supply range. During SLEEP mode this function is disabled.
Voltage level detector can be used also for Power-Check on Start-up of the EM6607 micro-controller when V_{DD} is applied (see Chapter 4.7 POR with Power-Check Reset).

The required voltage compare level is selected by writing the bits **VLC1** and **VLC2** in the **SVLD** control register that also activates the compare measurement. Since the measurement is not immediate the busy flag remains high during the measurement and is automatically cleared low when the measurement is finished. Reading the VLDR flag indicates the result. If the result is 0 then the voltage level is higher than the selected compare level. And if 1 it is lower than the compare level. The result **VLDR** of the last measurement remains until the new one is finished. The new result overwrites the previous one.

During the SVLD operation power consumption increases by approximately 3µA for 3.9msec. The measurement internally starts with the rising 256Hz edge following the SVLD test command. The additional SVLD consumption stops after the falling edge of the 256Hz internal clock.
Table below lists the voltage level selection

Table 38. SVLD Level selection

Voltage level	VLC1	VLC0	Possible levels implementations
SVLD disabled	0	0	
V_{L1}	0	1	V_{L1} : possible levels are from 1.3V to 3V by step of 100mV.
V_{L2}	1	0	V_{L2} : possible levels are 2.3V ; 2.6V to 3.5V by step of 100mV ; 3.7V and 4V
V_{L3}	1	1	V_{L3} : possible levels are 2.6V to 3.5V by step of 100mV ; 3.7V and 4V

V_{L1} level is also the level used for Power check if activated (table 15.1.1).

Table 39. SVLD control register - SVLD

Bit	Name	Reset	R/W	Description
3	**VLDR**	0	R	SVLD result (0=higher 1=lower)
2	**busy**	0	R	measurement in progress
1	**VLC1**	0	R/W	SVLD level control 1
0	**VLC0**	0	R/W	SVLD level control 0

12 Serial Write Buffer – SWB

The EM6607 has a simple Serial Write Buffer (SWB) which outputs serial data and serial clock.

The SWB is enabled by setting the bit **V03** in the **CLKSWB** register as well as setting port D to output mode. The combination of the possible PortD mode is shown in Table 34. In SWB mode the serial clock is output on port D0 and the serial data is output on port D1.

The signal TestVar[3], which is used by the processor to make conditional jumps, indicates "Transmission finished" in automatic send mode or "SWBbuffer empty" in interactive send mode. In interactive mode, TestVar[3] (see port A section) is equivalent to the interrupt request flags stored in **IntRq** register : it permits to recognise the interrupt source. (See also the interrupt handling section 9.Interrupt Controller for further information). To serve the "SWBbuffer empty " interrupt request, one only has to make a conditional jump on TestVar[3].

Bits ClkSWB0 and ClkSWB1 in the **ClkSWB** register select the Serial Write Buffer output clock frequency. The possible values are 1kHz (default), 2kHz, 8kHz or 16kHz and are shown in Table below:

Table 40. SWB clock selection

SWB clock output	CkSWB1	CkSWB0
1024 Hz	0	0
2048 Hz	0	1
8192 Hz	1	0
16384 Hz	1	1

Table 41. SWB clock selection register - ClkSWB

Bit	Name	Reset	R/W	Description
3	**V03**	0	R/W	Serial Write buffer selection
2	-	0	R	RESERVED - read 0
1	**CkSWB1**	0	R/W	SWB clock selector 1
0	**CkSWB0**	0	R/W	SWB clock selector 0

Table 42. PortD status

PortD status	ClOPD	V03	PD0	PD1	PD2	PD3
« NORMAL »	0	0	input	input	input	input
« NORMAL »	0	1	input	input	input	input
« NORMAL »	1	0	output PD0	output PD1	output PD2	output PD3
« SWB »	1	1	serial clock Out	SWB serial data	output PD2	output PD3

When the SWB is enabled by setting the bit **V03** TestVar[3], which is used to make conditional jumps, is reassigned to the SWB and indicates either "SWBbuffer empty " interrupt or "Transmission finished" . After Power-on-RESET **V03** is cleared at "0" and TestVar[3] is consequently assigned to PA2 input terminal.

The SWB data is output on the rising edge of the clock. Consequently, on the receiver side the serial data can be evaluated on falling edge of the serial clock edge.

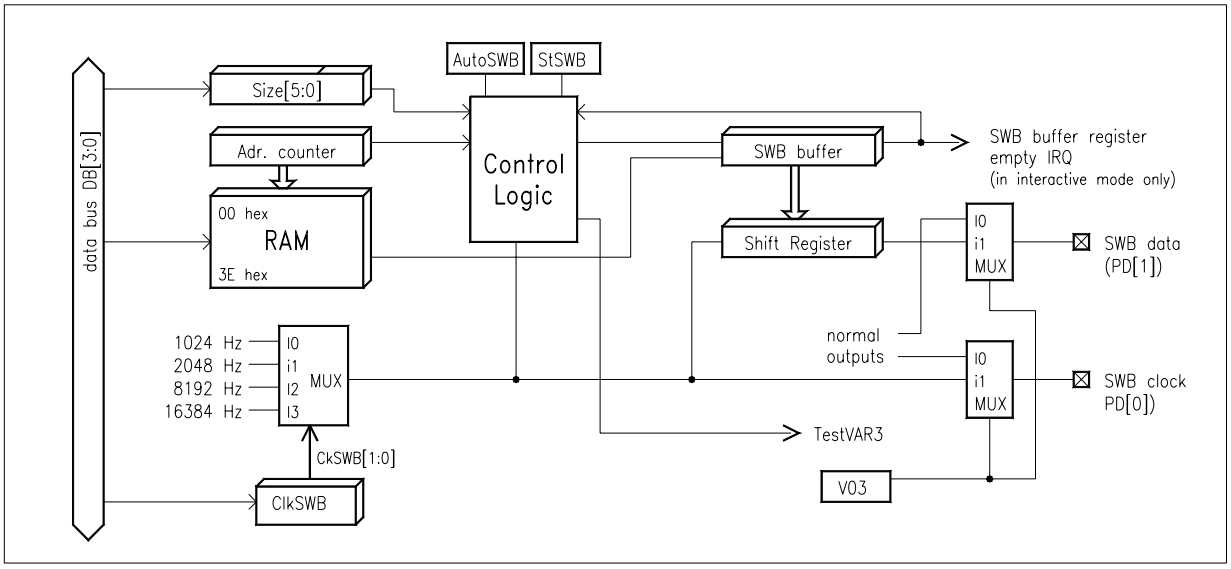


Figure 14. Serial write buffer

Table 43. SWB buffer register - SWbuff

Bit	Name	Reset	R/W	Description
3	**Buff3**	1	R/W	SWB buffer D3
2	**Buff2**	1	R/W	SWB buffer D2
1	**Buff1**	1	R/W	SWB buffer D1
0	**Buff0**	1	R/W	SWB buffer D0

Table 44. SWB Low size register - LowSWB

Bit	Name	Reset	R/W	Description
3	**Size[3]**	0	R/W	Auto mode buffer size bit3
2	**Size[2]**	0	R/W	Auto mode buffer size bit2
1	**Size[1]**	0	R/W	Auto mode buffer size bit1
0	**Size[0]**	0	R/W	Auto mode buffer size bit0

Table 45. SWB High size register – HighSWB

Bit	Name	Reset	R/W	Description
3	**AutoSWB**	0	R/W	SWB Automatic mode select
2	**StSWB**	0	R/W	SWB start interactive mode
1	**Size[5]**	0	R/W	Auto mode buffer size bit5
0	**Size[4]**	0	R/W	Auto mode buffer size bit4

The SWB has two operational modes, automatic mode and interactive mode.

12.1 SWB Automatic send mode

Automatic mode enables a buffer on a predefined length to be sent at high transmission speeds (up to 16khz). In this mode user prepares all the data to be sent (minimum 8 bits, maximum 256 bits) in RAM. The user then selects the clock speed, sets the number of data nibbles to be sent, selects automatic transmission mode (**AutoSWB** bit set to 1) and enters STANDBY mode by executing a HALT instruction. Once the HALT instruction is activated the SWB peripheral module sends the data in register **SWBuff** followed by the data in the RAM starting at address 00 up to the address specified by the bits **size[5:0**] located in the **LowSWB**, **HighSWB** registers.

During automatic transmission the general **INTEN** bit is disabled automatically to prevent other Interrupts to reset the standby mode. At the end of automatic transmission EM6607 leaves standby mode and sets TestVar[3] high. TestVar[3] = 1 is signaling SWB transmission is terminated. Once the transmission is finished, do not forget to enable the general **INTEN** bit if necessary.

The data to be sent must be prepared in the following order:

First nibble to be sent must be written in the **SWBuff** register . The other nibbles must be loaded in the RAM from address 0 (second nibble at adr.0, third at adr.1,...) up to the address with last nibble of data to be send = "size" address. Max. address space for SWB is 3E ("size" 3E hex) what gives with **SWBuff** up to 64 nibbles (256 bits) of possible data to be sent. The minimum possible data length we can send in Automatic SWB mode is 8 bits when the last RAM address to be sent is 00 ("size" = 00)

Once data are ready in the RAM and in the **SWBuff**, user has to load the "size" (adr. of the last nibble to be send - bits **size[5:0]**) into the **LowSWB** and **HighSWB** register together with **AutoSWB** bit = 1.

Now everything is ready for serial transmission. To start the transmission one has to put the EM6607 in standby mode with the HALT instruction. With this serial transmission starts. When transmission is finished the TESTvar[3] (can be used for conditional jumps) becomes active High, the **AutoSWB** bit is cleared, the processor is leaving the Standby mode and **INTEN** is switched on.

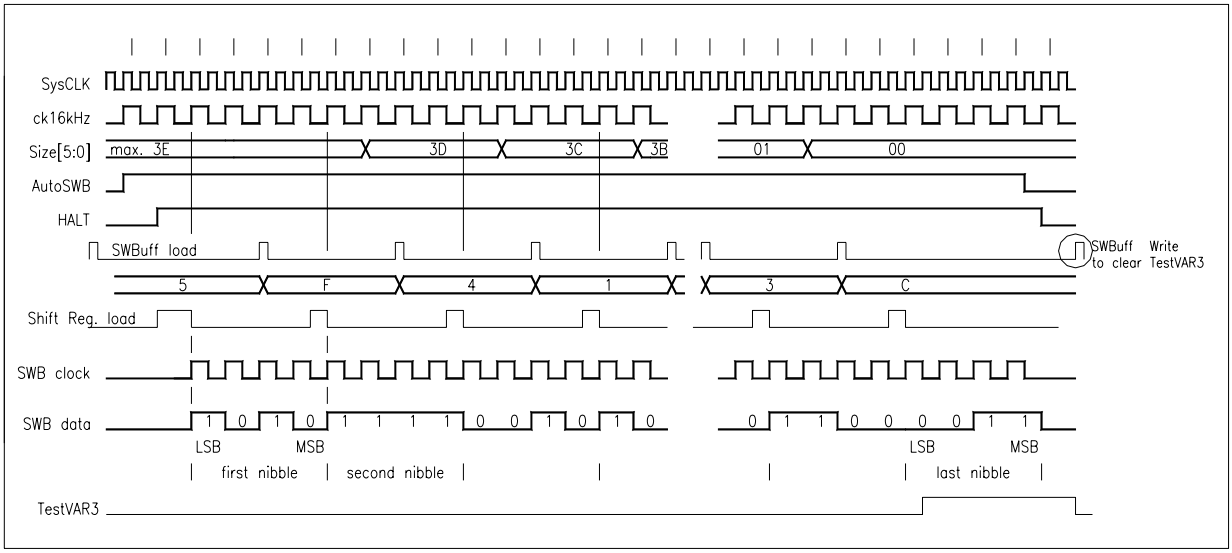


Figure 15. Automatic Serial Write Buffer transmission

The processor now starts to execute the first instruction placed after the HALT instruction (for instance write of **SWBuff** register to clear TESTvar[3]), except if there was a IRQ during the serial transmission. In this case the CPU will go directly in the interrupt routine to serve other interrupt sources.
TestVar[3] stays high until **SWBuff** is rewritten. Before starting a second SWB action this bit must be cleared by performing a dummy write on **SWBuff** address.

Because the data in the RAM are still present one can start transmitting the same data once again only by recharging the **SWBuff** , **LowSWB** and **HighSWB** register together with **AutoSWB** bit and putting the EM6607 in HALT mode will start new transmission.

12.2 SWB Interactive send mode

In interactive SWB mode the reloading of the data transmission register **SWBbuff** is performed by the application program. This means that it is possible to have an unlimited length transmission data stream. However, since the application program is responsible for reloading the data a continuous data stream can only be achieved at 1kHz or 2kHz transmission speeds. For the higher transmission speeds a series of writes must be programmed and the serial output clock will not be continuous.

Serial transmission using the interactive mode is detailed in Figure 14. Programming of the SWB in interactive is achieved in the following manner:

Select the transmission clock speed using the bits **ClkSW0** and **ClkSW1** in the **ClkSWB** register.

Load the first nibble of data into the SWB data register **SWBbuff**

Start serial transmission by selecting the bit **StSWB** in the register **HighSWB** register.

Once the data has been transferred into the serial transmission register a non maskable interrupt (SWBEmpty) is generated and TESTvar[3] goes high. The CPU goes in the interrupt routine, with the JPV3 as first instruction in the routine one can immediately jump to the SWB update routine to load the next nibble to be transmitted into the **SWBuff** register. If this reload is performed before all the serial data is shifted out then the next nibble is automatically transmitted. This is only possible at the transmission speeds of 1KHz or 2KHz due to the number of instructions required to reload the register. At the higher transmission speeds of 8khz and 16khz the application must restart the serial transmission by writing the **StSWB** in the High **SWBHigh** register after writing the next nibble to the **SWBbuff** register.

Each time the **SWBuff** register is written the "SWBbuffer empty interrupt" and TestVar[3] are cleared to "0". For proper operation the **SWBuff** register must be written before the serial clock drops to low during sending the last bit (MSB) of the previous data.

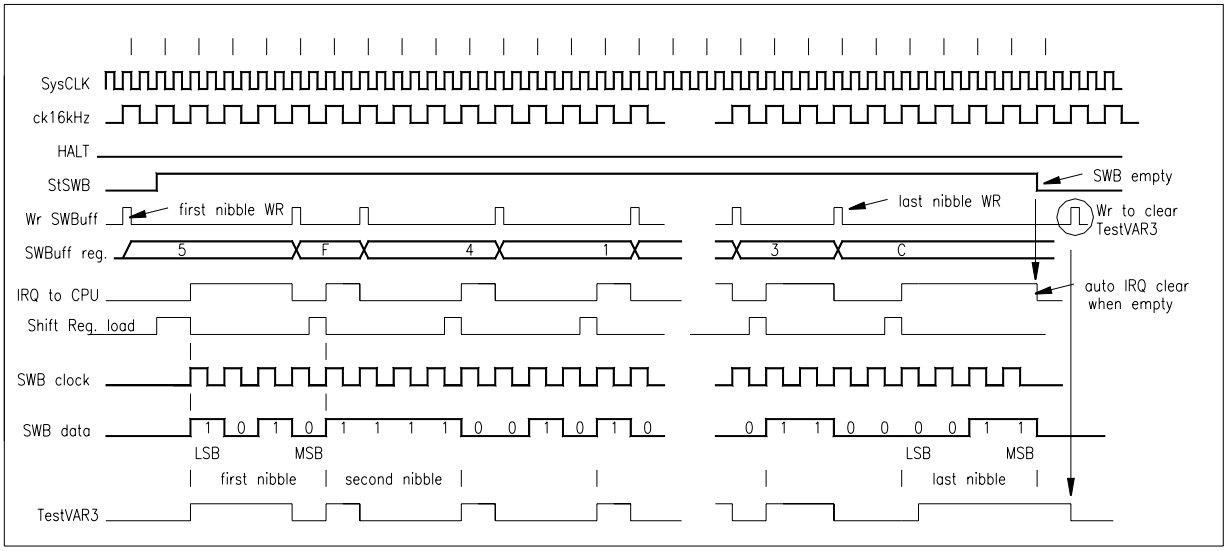


Figure 16. Interactive Serial Write Buffer transmission

After loading the last nibble in the **SWBbuff** register a new interrupt is generated when this data is transferred to an intermediate Shift Register. Precaution must be made in this case because the SWB will give repetitive interrupts until the last data is sent out completely and the **STSWB** bit goes low automatically. One possibility to overcome this is to check in the Interrupt subroutine that the **STSWB** bit went low before exiting interrupt. Be careful because if **STSWB** bit is cleared by software transmission is stopped immediately.

At the end of transmission a dummy write of **SWBuff** must be done to clear TESTvar[3] and "SWBbuffer empty interrupt" or the next transmission will not work.

13 STroBe / ReSeT Output

The STB/RST output pin is used to indicate the EM6607 RESET condition as well as write operations to ports B, C and D. For a PortB, PortC and PortD write operation the STROBE signal goes high for half of the system clock period. Write is effected on falling edge of the strobe signal and it can this be used to indicate when data changes at the output port pins. In addition, any EM6607 internal RESET condition is indicated by a continuous high level on STB/RST for the period of the RESET.

14 Test at EM - Active Supply Current test

For this purpose, five instructions at the end of the ROM will be added.

```
Testloop:   STI00H, 0AH
            LDR     1BH
            NXORX
            JPZ     Testloop
            JMP     00H
```

To stay in the testloop, these values must be written in the corresponding addresses before jumping in the loop:

```
1BH:    0101b
32H:    1010b
6EH:    0010b
6FH:    0011b
```

Free space after last instruction: JMP 00H (0000)

Remark: empty space within the program are filled with NOP (FOFF).

15 Metal Mask Options

The following options can be selected at the time of programming the metal mask ROM.

Table 46. input/output Ports

		Pull-Down Yes / No Strong / Weak	**Pull-Up Yes / No Strong / Weak**	**Nch-open drain Yes / No**	**Input blocked when Output Yes / No**	**Output Hi-Z in SLEEP mode Yes / No**
		0	**1 (*1)**	**2 (*1)**	**3 (*2)**	**4**
A0	PA0 input					
A1	PA1 input					
A2	PA2 input					
A3	PA3 input					
B0	PB0 In/Out					**OEBsleepRes** Bit in Option2 register. Yes =1, No=0
B1	PB1 In/Out					
B2	PB2 In/Out					
B3	PB3 In/Out					
C0	PC0 In/Out					**OECsleepRes** Bit in Option2 register. Yes =1, No=0
C1	PC1 In/Out					
C2	PC2 In/Out					
C3	PC3 In/Out					
D0	PD0 In/Out					**OEDsleepRes** Bit in Option2 register. Yes =1, No=0
D1	PD1 In/Out					
D2	PD2 In/Out					
D3	PD3 In/Out					
E0	PE0 In/Out					
E1	PE1 In/Out					
E2	PE2 In/Out					
E3	PE3 In/Out					

Put one letter (Y, N) in each BOX from proposed for the column.
For Pull-Up/Down if "Y" add also one letter (S,W) to define type of resistor. (see 18.5 electrical parameters also)
***1** When used as N-channel Open drain output not-controlled Pull-Up (**Y-SOD**) can be used. Pull Up active during Output also if **Y-S** is set in Pull-Up & **Y** for Nch-open drain an external resistor is needed to make output High !!!! because Pull Up is active during input only ! This is applicable only for Ports B,C,D and E which can be outputs also.
***2** Port-wise for PortC and PortD (one possibility for the whole port); PortB bit-wise

Table 47. PortB Hi Current Drive capability

		Driving to V_{SS} (negative supply) Possible options are **4n** (weak), **10n**, **18n** (strong)	Driving to V_{DD} (positive supply) Possible options are **6p** (weak), **14p**, **24p** (strong)
B0	PB0 output		
B1	PB1 output		
B2	PB2 output		
B3	PB3 output		

At higher V_{DD} scaling of this buffer is needed not to overcome the Maximum V_{DD} and V_{SS} current for the IC.
Put in each box one of 3 possibilities mentioned in the title of column like 18n, 24p (strongest configuration). Numbers above state for number of active N and P transistors in output buffer. See electrical parameters to know what to expect at different option. Important Note: Maximum V_{DD} and V_{SS}current MUST be limited to 90 mA !! Only 2 PortB High current terminals can switch at the same time in strongest configuration to limit the spikes generated by switching.

15.1.1 Power-Check Level Option

Option Name		Default Value	User Value
		A	B
PwCheck	Power-Check Yes / No	NO	

Power Check function can be enabled or disabled. For EM6603 compatibility the default selection is **NO**, but can be set to **YES** to be sure V_{DD} on Power-Up came over SVLD level $\mathbf{V_{L1}}$ before internal Reset is released and circuit starts to execute instructions.

15.1.2 PortA reset Option, see paragraph 4.3

Option Name		Default Value	User Value
		A	B
RA	PortAreset	rstpa_no	

Refer to chapter 4.3 Input port (PA0..PA3) RESET to select the PortA reset option. Possible options are **rstpa_no**, **rstpa_*x*h** where x={3,5,6,7,9,a,b,c,d,e,f}

15.1.3 SVLD levels Option, see paragraph 11 SVLD

Option Name		typ. V_{L1} level [V]	typ. V_{L2} level [V]	typ. V_{L3} level [V]
V_{LX}	SVLD level in Volts			

$\mathbf{V_{L1}}$ level is also the level used for Power check if activated (table 15.1.1).
$\mathbf{V_{L1}}$: possible levels are from 1.3V to 3V by step of 100mV.
$\mathbf{V_{L2}}$: possible levels are 2.3V ; 2.6V to 3.5V by step of 100mV ; 3.7V and 4V
$\mathbf{V_{L3}}$: possible levels are 2.6V to 3.5V by step of 100mV ; 3.7V and 4V

Software name is : _____.bin, dated _____

The customer should specify the required options at the time of ordering.
A copy of this sheet, as well as the « Software ROM characteristic file » generated by the assembler (*.STA) should be attached to the order.

16 PERIPHERAL MEMORY MAP

The following table shows the peripheral memory map of the EM6607. The address space is between $00 and $7F (Hex). Any addresses not shown can be considered to be reserved.

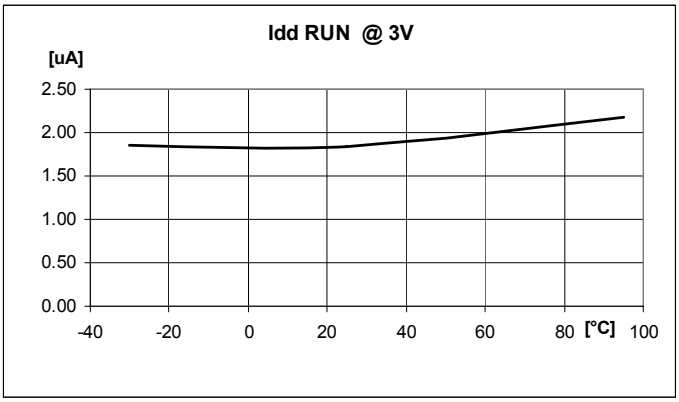
Register name	add hex	add dec	power up value	write_bits	read_bits	Remarks
			b'3210	Read/Write_bits		
RAM	00-5f	0-95	xxxx	0: D0 1: D1 2: D2 3: D3		direct addressing
LTimLS	60	96	0000	0: TL0 1: TL1 2: TL2 3: TL3	0: TS0 1: TS1 2: TS2 3: TS3	low nibble of 8bit timer load and status register
HTimLS	61	97	0000	0: TL4 1: TL5 2: TL6 3: TL7	0: TS4 1: TS5 2: TS6 3: TS7	high nibble of 8bit timer load and status register
TimCtr	62	98	0000	0: TEC0 1: TEC1 2: TEC2 3: TimAuto		timer control register with frequency selector
Option	63	99	0000	0: NoWD 1: debPAN 2: debPCN 3: IRQedgeR		Watch dog timer off Debouncer on port A disabled Debouncer on port C disabled Rising edge interrupt
Option2	64	100	0000	0: BUZZERPE0 1: OEBsleepRes 2: OECsleepRes 3: OEDsleepRes		Buzzer on PE0 enable PortB OE reset by Sleep PortC OE reset by Sleep PortD OE reset by Sleep
PA3cnt	65	101	0000	0: PA3cntin 1: Fout 2: WDdisana 3: 0		PA3 counter input Frequency output on STRB Disable analogue WD
PortE	66	102	xxxx	0: PE0 1: PE1 2: PE2 3: PE3		Port E Input/Output
CIOportE	67	103	0000	0: CIOPE0 1: CIOPE1 2: CIOPE2 3: CIOPE3		Port E Input/Output individual control
ClkSWB	68	104	0000	0: CkSWB0 1: CkSWB1 2: 0 3: V03		Clock selector for SWB
SWBuff	69	105	1111	0: Buff0 1: Buff1 2: Buff2 3: Buff3		SWB intermediate buffer
LowSWB	6A	106	0000	0: size[0] 1: size[1] 2: size[2] 3: size[3]		low nibble to define the size of data to be send in Automatic mode
HighSWB	6B	107	0000	0: size[4] 1: size[5] 2: StSWB 3: AutoSWB		the size of the data to be sent & SWB control
Register name	**add hex**	**add dec**	**power up value**	**write_bits**	**read_bits**	**Remarks**

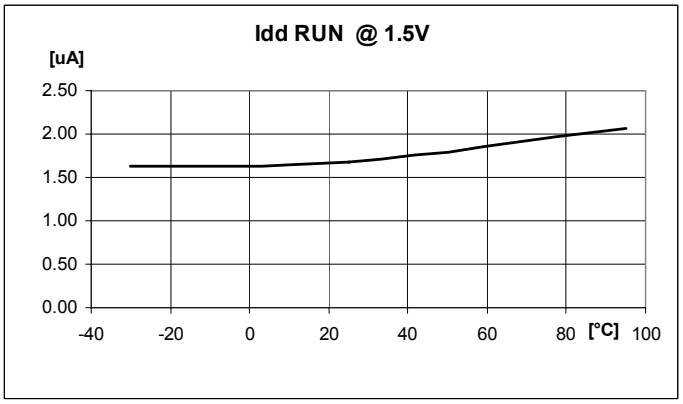
			b'3210	Read/Write_bits		
SVLD	6C	108	0000	0: VLC0 1: VLC1 2: - 3: -	0: VLC0 1: VLC1 2: busy 3: VLDR	voltage level detector control
CIRQD	6D	109	0000	0: INTEN 1: DebCK 2: 0 3: 0		global interrupt enable debouncer clock IRQ Comp Bit IRQ Comp Mask
Index LOW	6E	110	xxxx			internally used for INDEX register
Index HIGH	6F	111	xxxx			internally used for INDEX register
IntRq	70	112	0000	0: - 1: - 2: SLEEP 3: -	0: INTPA 1: INTPC 2: INTTE 3: INTPR	interrupt requests sleep mode
WD	71	113	0000	0: - 1: - 2: SLmask 3: WDrst	0: WD0 1: WD1 2: SLmask 3: 0	WatchDog timer control and SLEEP mask
PortA	72	114	xxxx		0: PA0 1: PA1 2: PA2 3: PA3	Port A status
IRQpA	73	115	0000		0: IRQpa0 1: IRQpa1 2: IRQpa2 3: IRQpa3	Port A interrupt request
MPortA	74	116	0000	0: MPA0 1: MPA1 2: MPA2 3: MPA3		Port A mask
PortB	75	117	xxxx	0: PB0 1: PB1 2: PB2 3: PB3		Port B Input/Output
CIOportB	76	118	0000	0: CIOPB0 1: CIOPB1 2: CIOPB2 3: CIOPB3		Port B Input/Output individual control
PortC	77	119	xxxx	0: PC0 1: PC1 2: PC2 3: PC3		Port C Input/Output
IRQpC	78	120	0000		0: IRQpc0 1: IRQpc1 2: IRQpc2 3: IRQpc3	Port C interrupt request
MPortC	79	121	0000	0: MPC0 1: MPC1 2: MPC2 3: MPC3		Port C mask
PortD	7A	122	xxxx	0: PD0 1: PD1 2: PD2 3: PD3		Port D Input/Output

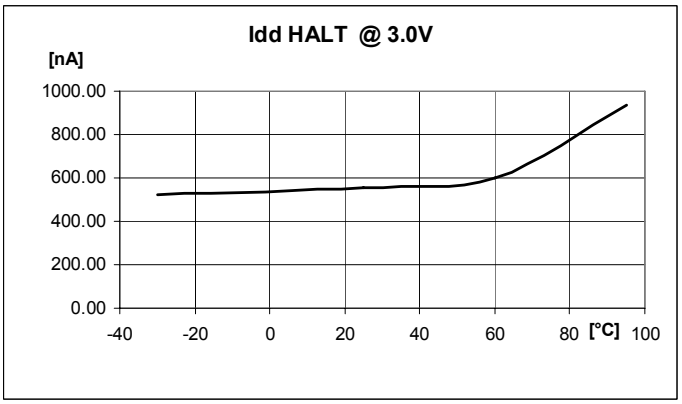
Register name	add hex	add dec	power up value	write_bits	read_bits	Remarks
			b'3210	Read/Write_bits		
RegSoftPOR	7B	123	0000	0: 0 1: 0 2: -- 3: SOFTPOR	0: 0 1: 0 2: -- 3:	Software POR
CPIOB	7C	124	x000	0: PA&C 1: CIOPC 2: CIOPD 3: 0		PortAirq AND PortCirq PortC In/Out PortD In/Out
PRESC	7D	125	0000	0: PSF0 1: PSF1 2: PRST 3: MTim	0: PSF0 1: PSF1 2: 0 3: MTim	Prescaler control timer mask
BEEP	7E	126	0000	0: BCF0 1: BCF1 2: BUen 3: TimEn		Buzzer control Timer Enable
RegTestEM	*7F*	*127*	----	----	----	*reserved*

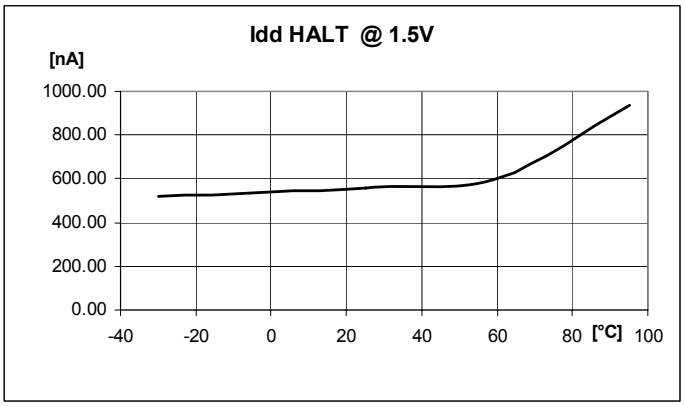
17 Temperature and Voltage Behaviours

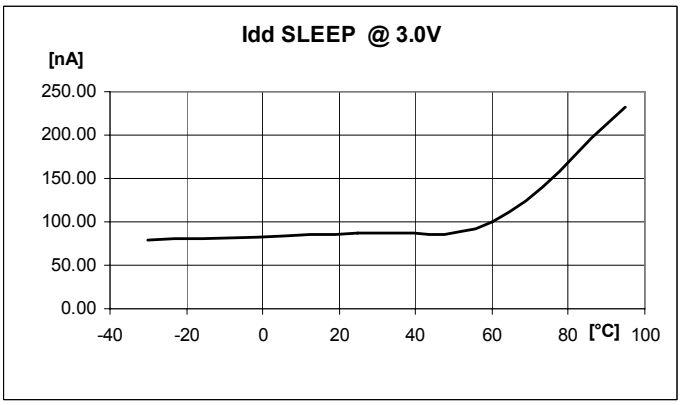
17.1 IDD Current (Typical)

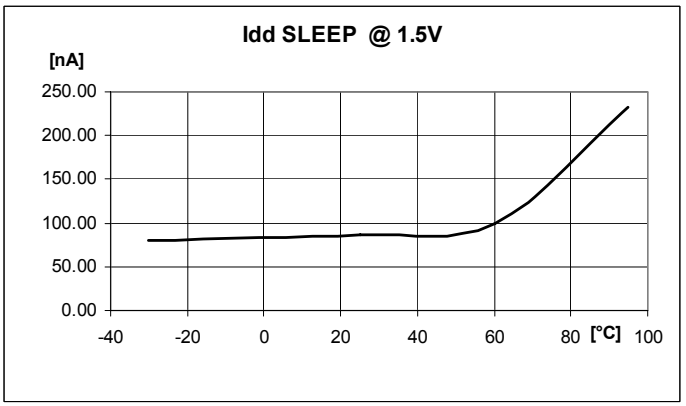




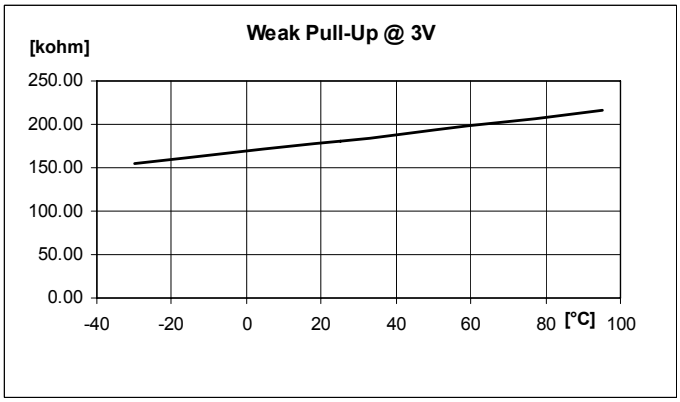


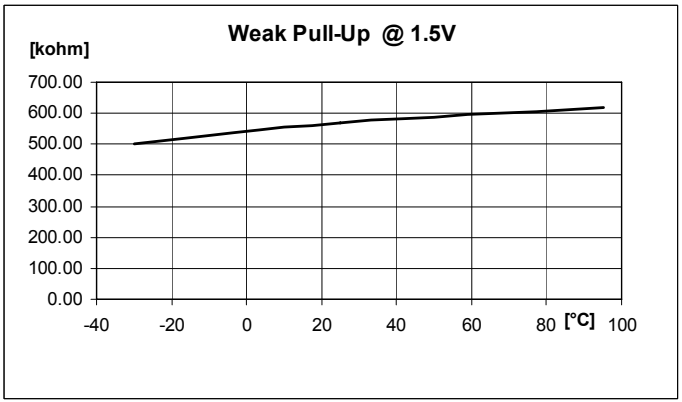


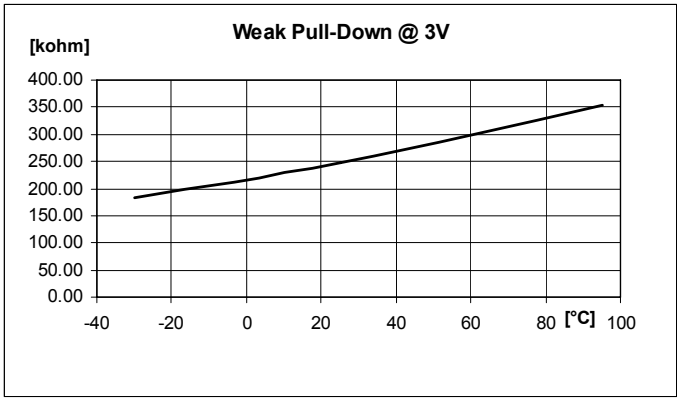


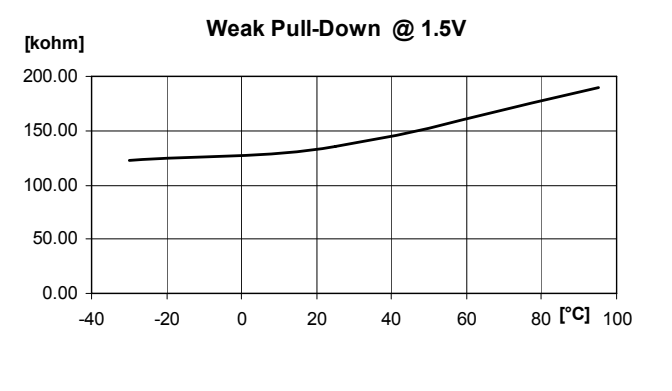


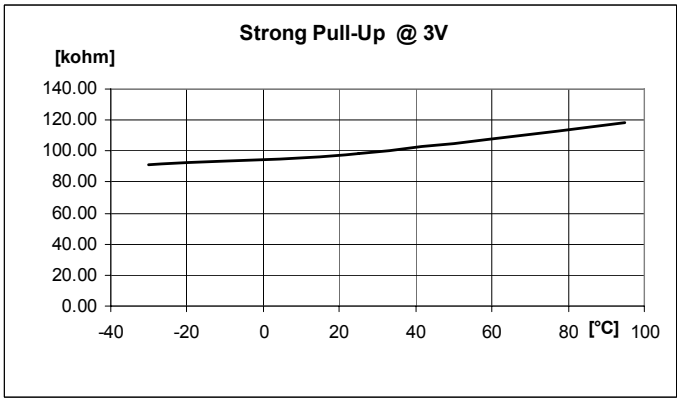
17.2 Pull-down resistance (Typical)

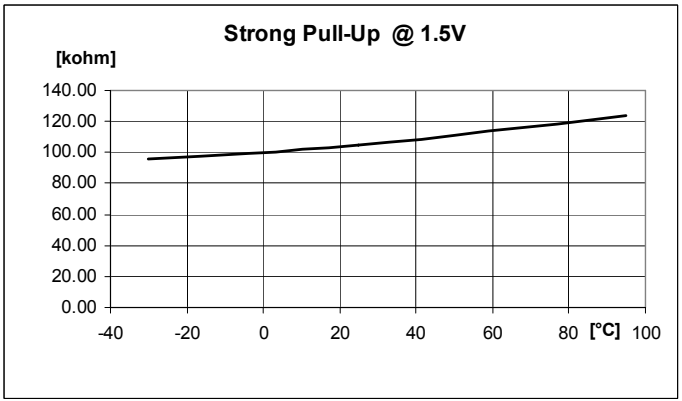


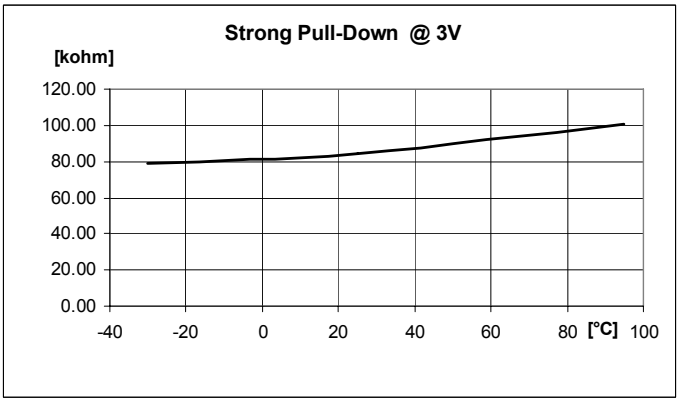


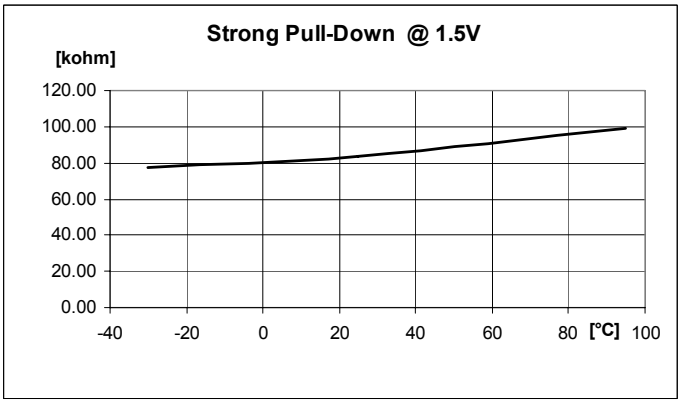




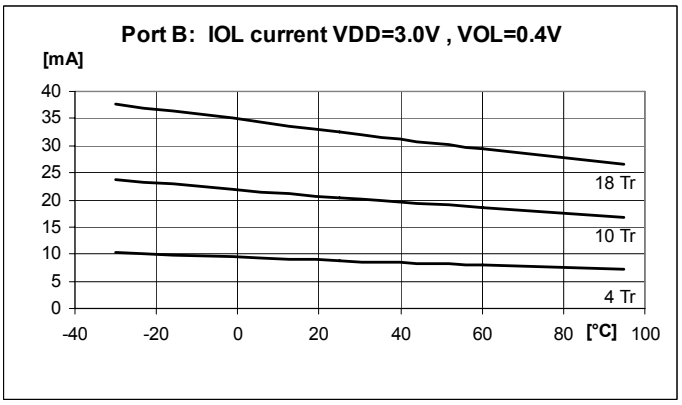


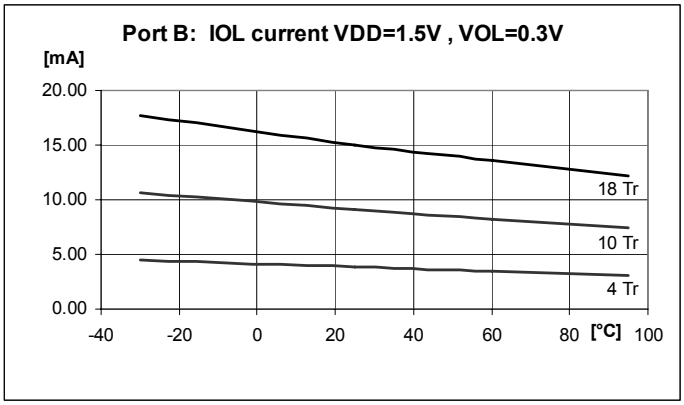


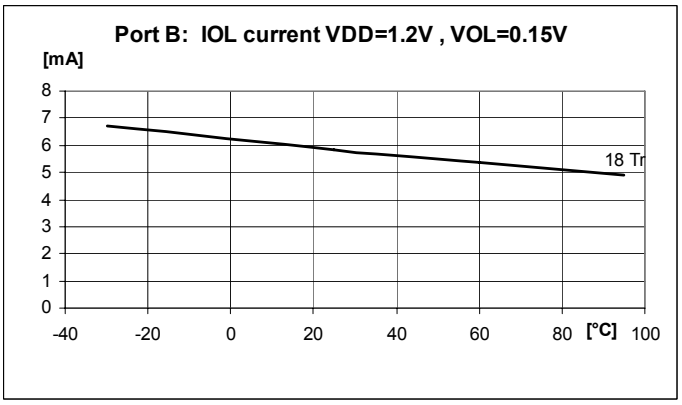


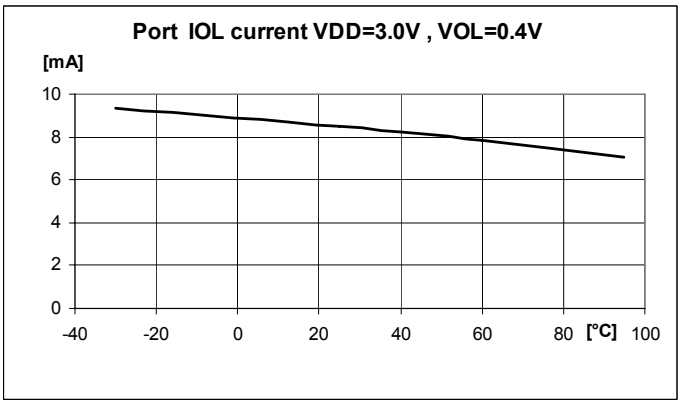


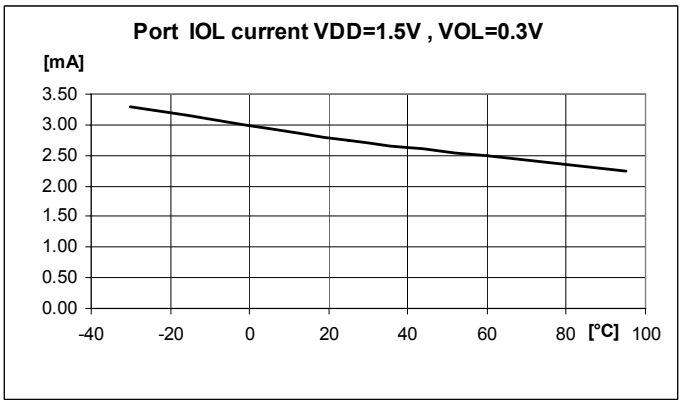
17.3 Output Currents (Typical)

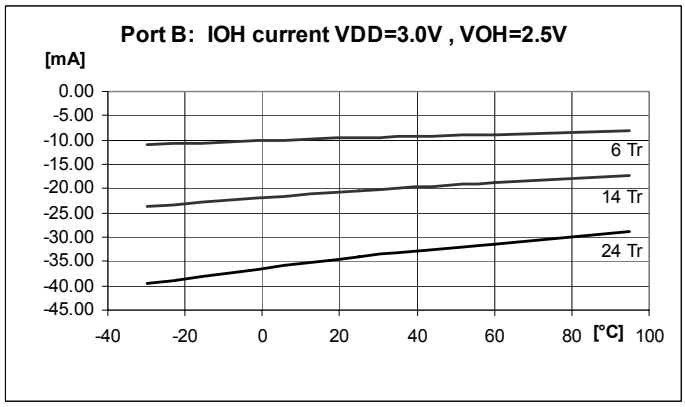


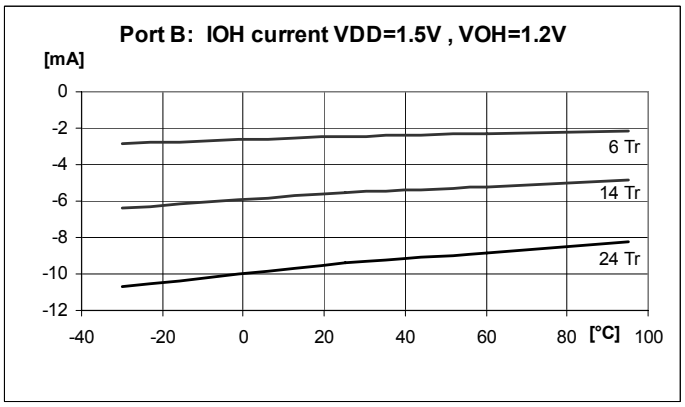


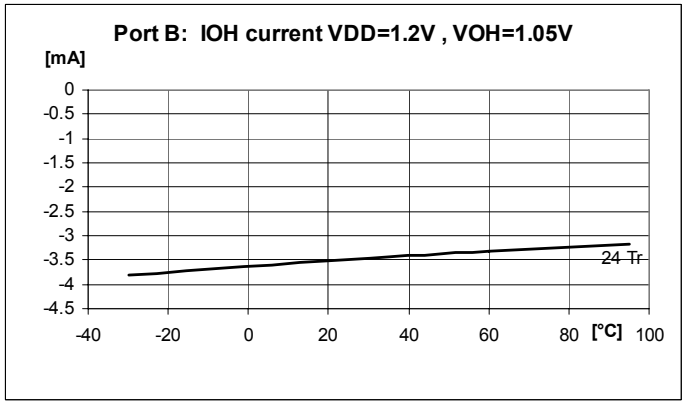


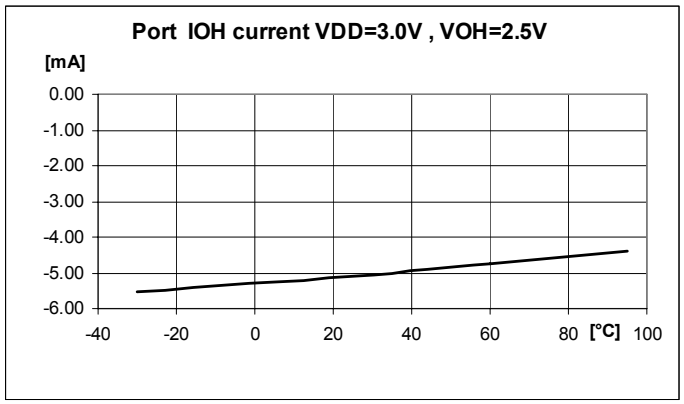


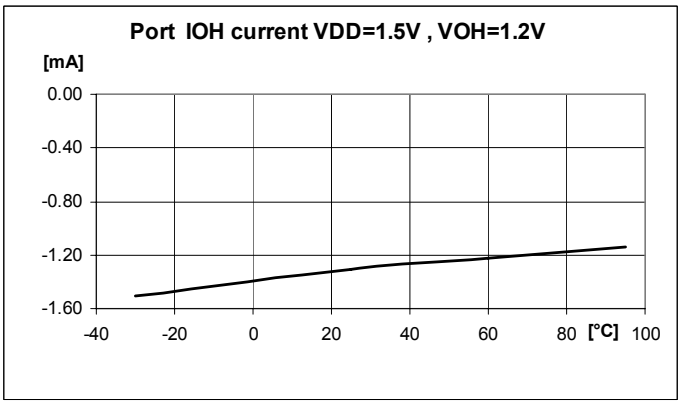












18 Electrical specifications

18.1 Absolute maximum ratings

Parameter	min.	max.	unit
Supply voltage V_{DD}-V_{SS}	- 0.2	+ 3.6	V
V_{DD} current (DC)		90	mA
V_{SS} current (DC)		90	mA
Input voltage	V_{SS} - 0.2	V_{DD}+0.2	V
Storage temperature	- 40	+ 125	°C

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified electrical characteristics may affect device reliability or cause malfunction.

18.2 Standard Operating Conditions

Parameter	value	Description
Temperature	-20°C to +85°C	
V_{DD_range1}	1.4V to 3.3V	With internal voltage regulator
V_{DD_range2} (V_{REG} = V_{DD}) (note 1)	1.2V to 1.8V	Without internal voltage regulator
V_{SS}	0V (reference)	
CV_{REG}	min. 100nF	regulated voltage capacitor tow. V_{SS}
fq	32768Hz	nominal frequency
R_{QS}	35kΩ	typical quartz serial resistor
C_L	8.2pF	typical quartz load capacitance
df/f	± 30ppm	quartz frequency tolerance

18.3 Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions should be taken as for any other CMOS component.

Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range.

18.4 DC characteristics - Power Supply Pins

Conditions: V_{DD}=V_{REG}=1.5V, T=25°C (note 5) (unless otherwise specified)

Parameter	Conditions	Symb.	Min.	Typ. (note1)	Max.	Unit
ACTIVE Supply Current	+25°C (note2)	I_{VDDa}		1.8	3.0	µA
ACTIVE Supply Current (in active mode)	(note2) (note2) -20°C to +85°C	I_{VDDa}			4.5	µA
STANDBY Supply Current	+25°C	I_{VDDh}		0.5	1.0	µA
STANDBY Supply Current (in Halt mode)	(note3) -20°C to +85°C	I_{VDDh}			1.8	µA
SLEEP Supply Current	+25°C	I_{VDDs}		0.1	0.4	µA
SLEEP Supply Current (SLEEP =1)	(note3) -20°C to +85°C	I_{VDDs}			1.2	µA
POR voltage		V_{POR}		0.7	1.0	V
RAM data retention		V_{RD}	1.1			V
Regulated Voltage	V_{REG} not at V_{DD}	V_{REG}	1.10		1.5	V

Conditions: V_{DD}=3.0V, T=25°C (note 5) (unless otherwise specified), V_{REG} not shorted to V_{DD}

Parameter	Conditions	Symb.	Min.	Typ. (note 2)	Max.	Unit
ACTIVE Supply Current	+25°C (note 3)	I_{VDDa}		1.8	3.0	µA
ACTIVE Supply Current (in active mode)	(note 3) (note 4) -20°C to +85°C	I_{VDDa}			4.5	µA
STANDBY Supply Current	+25°C	I_{VDDh}		0.5	1.0	µA
STANDBY Supply Current (in Halt mode)	(note 4) -20°C to +85°C	I_{VDDh}			1.8	µA
SLEEP Supply Current	+25°C	I_{VDDs}		0.1	0.4	µA
SLEEP Supply Current (SLEEP =1)	(note 4) -20°C to +85°C	I_{VDDs}			1.2	µA
POR voltage		V_{POR}		0.7	1.0	V
RAM data retention		V_{RD}	1.1			V
Regulated Voltage	-20°C to +85°C	V_{REG}	1.10		1.90	V

Note 1 Because of the voltage regulator drop at low voltages V_{REG} = V_{DD} when V_{DD}<1.8V

Note 2: For current measurement typical quartz described in Operating Conditions is used. All I/O pins without internal Pull Up/Down are pulled to V_{DD} externally.

Note 3: Test loop with successive writing and reading of two different addresses with an inverted values (five instructions should be reserved for this measurement),

Note 4: NOT tested if delivered in chip form.

Note 5: Test conditions for ACTIVE and STANDBY Supply current mode are: Q_{IN} = external square wave, from rail to rail of V_{REG} (regulated voltage) with 100nF capacitor on V_{REG}. fQ_{IN} = 32kHz.

18.5 DC characteristics - Input/Output Pins

Conditions: V_{DD}=1.5V / 3.0V, -20°C <T<85°C (unless otherwise specified)

Parameter	Conditions	Symb.	Min.	Typ.	Max.	Unit
Input Low voltage						
I/O ports A,B,C,D,E	Pin at hi-impedance	V_{IL}	V_{SS}		$0.3V_{DD}$	V
TEST, Reset			V_{SS}		$0.3V_{DD}$	V
Q_{IN} (Note5)			V_{SS}		$0.3V_{REG}$	V
Input High voltage						
I/O ports A,B,C,D,E	Pin at hi-impedance	V_{IH}	$0.7V_{DD}$		V_{DD}	V
TEST, Reset			$0.7V_{DD}$		V_{DD}	V
Q_{IN} (Note5)			$0.9V_{REG}$		V_{REG}	V
Output Low Current	VOL = 0.15V, V_{DD} = 1.2V	I_{OL}				
Port B 18 transistors			3.0	6.0		mA
Output Low Current	VOL = 0.3V, V_{DD} = 1.5V	I_{OL}				
Port B 18 transistors			9.5	15.0		mA
Port B 10 transistors			5.0	8.0		mA
Port B 4 transistors			1.5	3.5		mA
Port C,D,E, STRB/RST			1.0	2.5		mA
Output Low Current	VOL = 0.4V, V_{DD} = 3.0V	I_{OL}				
Port B 18 transistors			23.0	33.0		mA
Port B 10 transistors			13.0	20.5		mA
Port B 4 transistors			5.4	8.8		mA
Port C,D,E, STRB/RST			5.4	7.8		mA
Output High Current	VOH = 1.05V, V_{DD} = 1.2V	I_{OH}				
Port B 24 transistors				-3.5	-2.5	mA
Output High Current	VOH = 1.2V, V_{DD} = 1.5V	I_{OH}				
Port B 24 transistors				-9.4	-6.0	mA
Port B 14 transistors				-5.0	-3.0	mA
Port B 6 transistors				-2.5	-1.5	mA
Port C,D,E, STRB/RST				-1.2	-0.6	mA
Output High Current	VOH = 2.5V, V_{DD} = 3.0V	I_{OH}				
Port B 24 transistors				-33.0	-23.0	mA
Port B 14 transistors				-20.0	-15.0	mA
Port B 6 transistors				-9.0	-3.0	mA
Port C,D,E, STRB/RST				-4.5	-3.0	mA
Output load on Port B	V_{DD} = 3.0V,Port B 18/24 transistors option					
Capacitor	with 4 toggling ports.				50	nF
Resistor			150			Ω
Input pull-down strong	Pin at V_{DD} = 1.5V, 25°C	R_{IN}				
I/O ports A,B,C,D,E (option)			50	90	350	kΩ
Reset			50	110	200	kΩ
Test			10	18	35	kΩ
Input pull-down strong	Pin at V_{DD} = 3.0V, 25°C	R_{IN}				
I/O ports A,B,C,D,E (option)			50	90	160	kΩ
Reset			50	110	200	kΩ
Test			10	18	35	kΩ
Input pull-down weak	Pin at V_{DD} = 1.5V, 25°C	R_{IN}				
I/O ports A,B,C,D,E (option)			80	130	350	kΩ
Input pull-down weak	Pin at V_{DD} = 3.0V, 25°C	R_{IN}				
I/O ports A,B,C,D,E (option)			50	250	600	kΩ
Input pull-up strong	Pin at V_{DD} = 1.5V, 25°C	R_{IN}				
I/O ports A,B,C,D,E (option)			50	100	250	kΩ
Input pull-up strong	Pin at V_{DD} = 3.0V, 25°C	R_{IN}				
I/O ports A,B,C,D,E (option)			50	100	200	kΩ
Input pull-up weak	Pin at V_{DD} = 1.5V, 25°C	R_{IN}				
I/O ports A,B,C,D,E (option)			300	550	1000	kΩ
Input pull-up weak	Pin at V_{DD} = 3.0V, 25°C	R_{IN}				
I/O ports A,B,C,D,E (option)			100	180	400	kΩ

Note 5: Q_{OUT} is used only with crystal.

18.6 DC characteristics - Supply Voltage Detector Levels

Conditions: T= +25°C (unless otherwise specified)

Parameter	Conditions	Symb.	Min.	Typ.	Max.	Unit
Supply Voltage Detector						
SVLD lev3		V_{L3}	0.88 x V_{L3}	V_{L3}	1.12 x V_{L3}	V
SVLD lev2		V_{L2}	0.88 x V_{L2}	V_{L2}	1.12 x V_{L2}	V
SVLD lev1		V_{L1}	0.88 x V_{L1}	V_{L1}	1.12 x V_{L1}	V
Supply Voltage Detector	0°C to +65°C					
SVLD lev3		V_{L3}	0.88 x V_{L3}	V_{L3}	1.12 x V_{L3}	V
SVLD lev2		V_{L2}	0.88 x V_{L2}	V_{L2}	1.12 x V_{L2}	V
SVLD lev1		V_{L1}	0.88 x V_{L1}	V_{L1}	1.12 x V_{L1}	V

SVLD typical level values must be selected with a precision of 100 mV.

18.7 Oscillator

Conditions: T=25°C (unless otherwise specified)

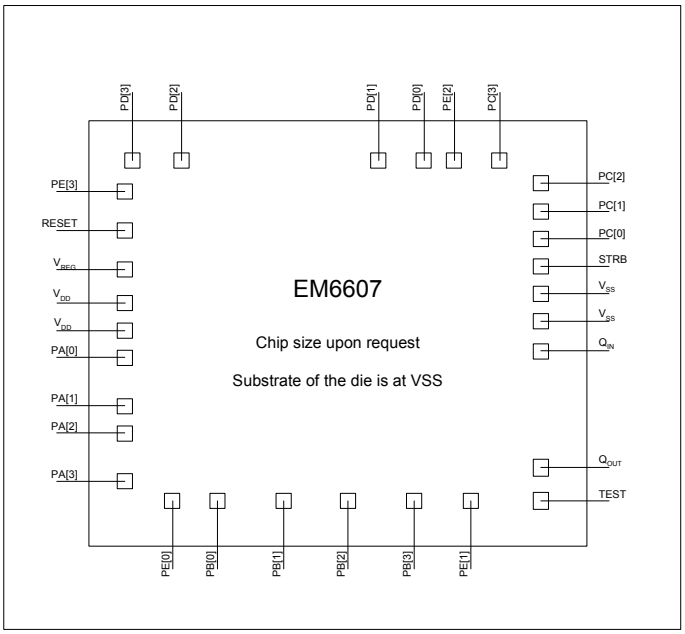
Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Temperature stability	+15°C to +35 °C	df/f x dT			0,3	ppm /°C
Voltage stability	V_{DD}=1,4V to 1,6 V	df/f x dU			5	ppm /V
Input capacitor	Ref. on V_{SS}	CIN	5,6	7	8,4	pF
Output capacitor	Ref. on V_{SS}	CIN	12,1	14	15,9	pF
Transconductance	50mVpp,V_{DD} min	Gm	2.5		15.0	µA/V
Oscillator start voltage	T_{START}< 10 s	U_{START}	V_{DD} min			V
Oscillator start time	V_{DD} > V_{DD} Min	t_{DOSC}		0.5	3	s
System start time (oscillator + cold-start + reset)		t_{DSYS}		1.5	4	s
Oscillation detector frequency	V_{DD} > V_{DD} min	$t_{DetFreq}$		6	12	kHz

18.8 Input Timing characteristics

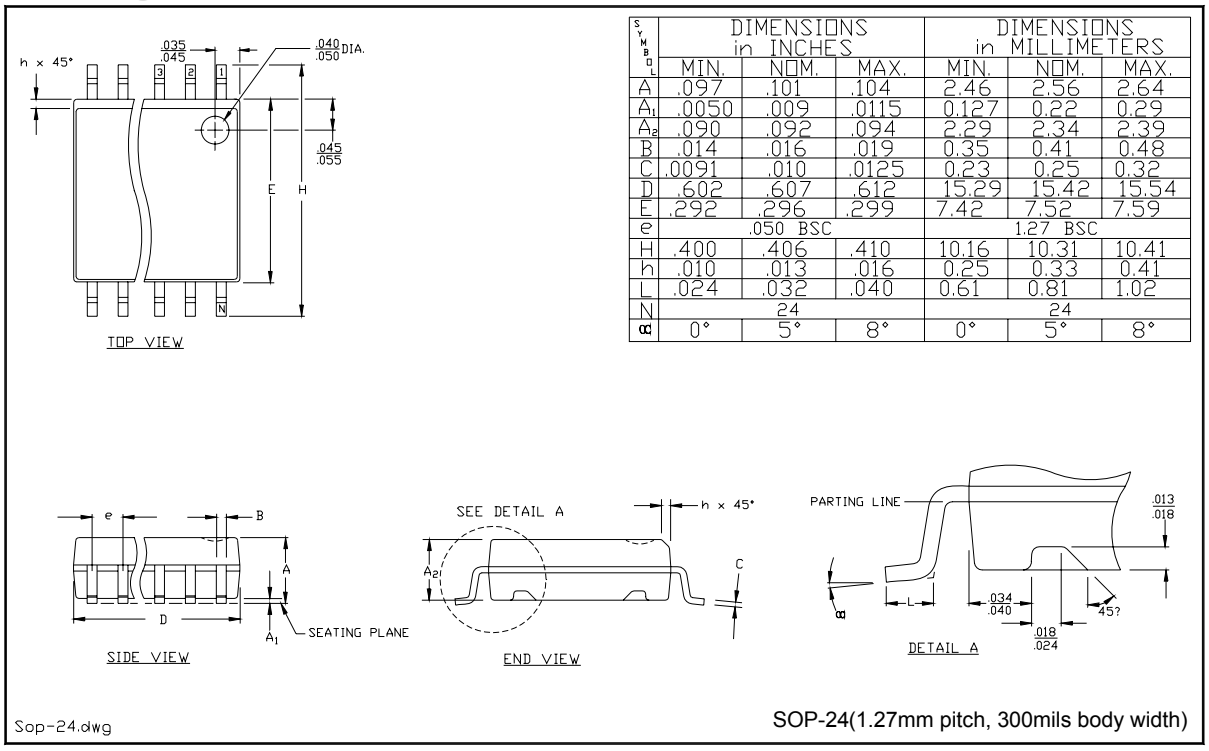
Conditions: 1.5V<V_{DD}<3.0V, -20°C <T<85°C (unless otherwise specified)

Parameter	Conditions	Symb.	Min.	Unit
RESET pulse length to exit SLEEP mode	RESET from SLEEP	tRESsl	2	µs
RESET pulse length (debounced) PortA , C pulse length (debounced)	DebCK = 0 DebCK = 0	tdeb0 tdeb0	2 2	ms ms
RESET pulse length (debounced) PortA , C pulse length (debounced)	DebCK = 1 DebCK = 1	tdeb1 tdeb1	16 16	ms ms

19 Pad Location Diagram

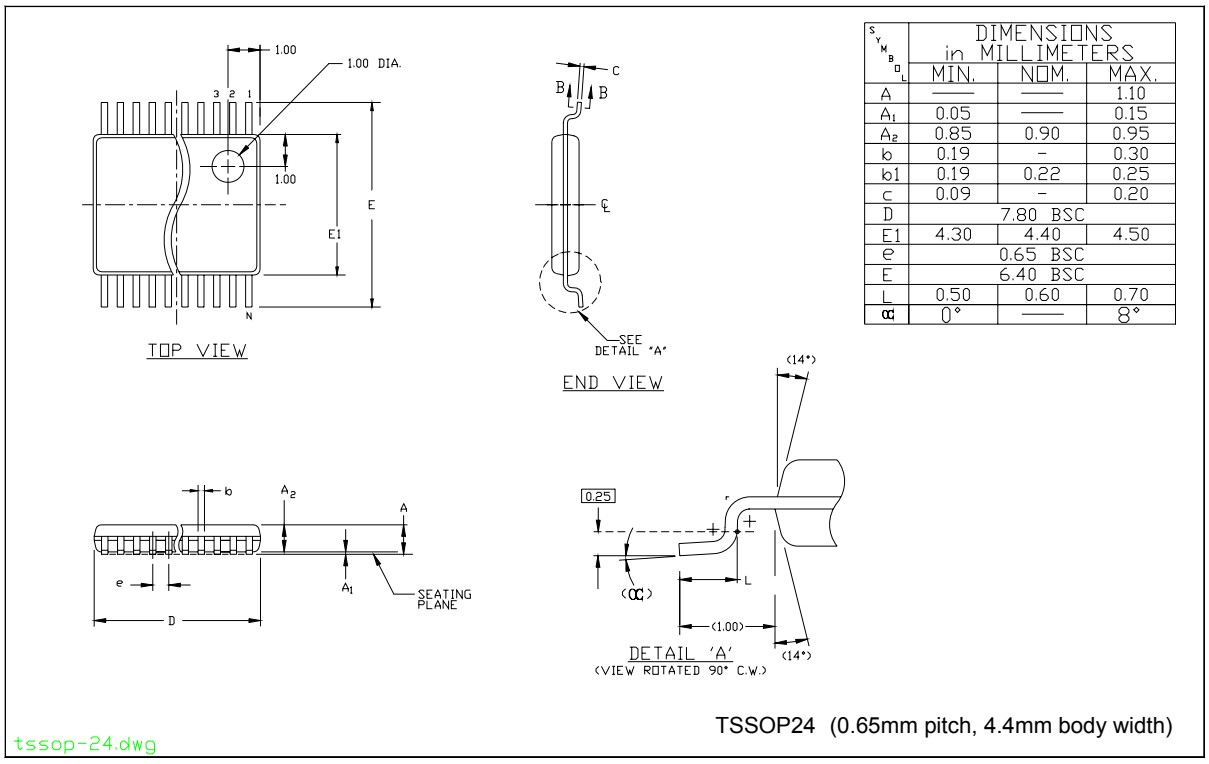


20 Package Dimensions



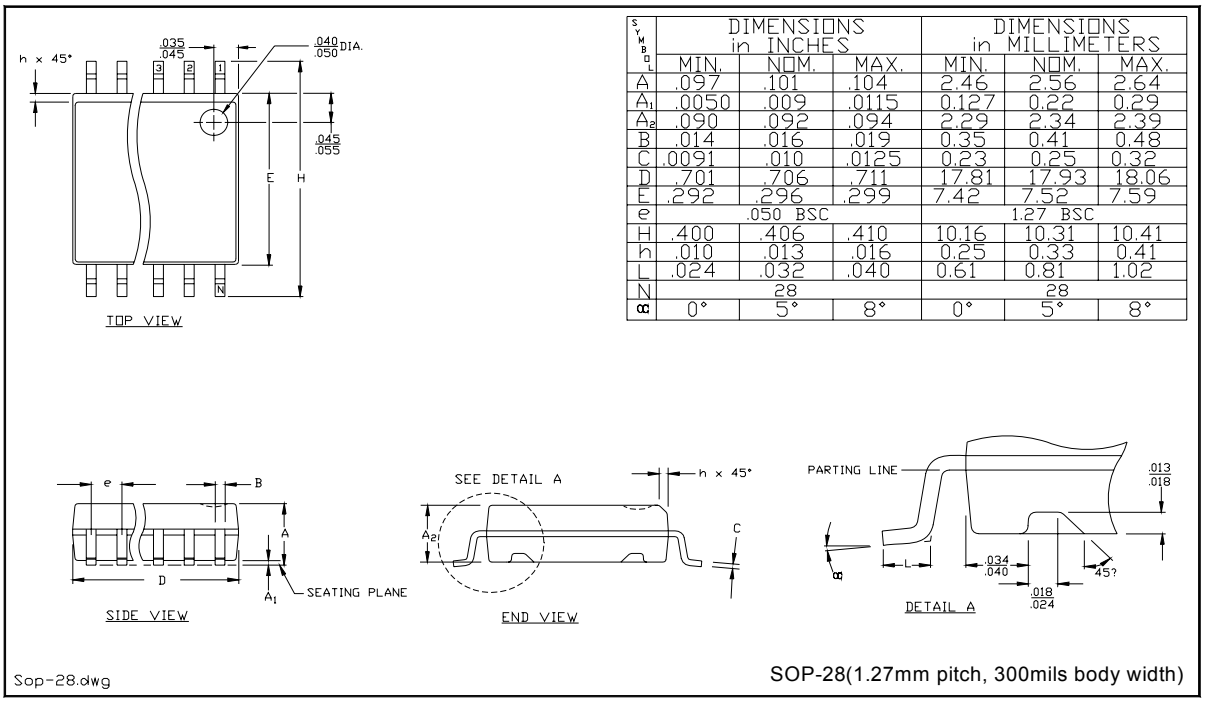
SYMBOL	DIMENSIONS in INCHES			DIMENSIONS in MILLIMETERS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	.097	.101	.104	2.46	2.56	2.64
A_1	.0050	.009	.0115	0.127	0.22	0.29
A_2	.090	.092	.094	2.29	2.34	2.39
B	.014	.016	.019	0.35	0.41	0.48
C	.0091	.010	.0125	0.23	0.25	0.32
D	.602	.607	.612	15.29	15.42	15.54
E	.292	.296	.299	7.42	7.52	7.59
e	.050 BSC			1.27 BSC		
H	.400	.406	.410	10.16	10.31	10.41
h	.010	.013	.016	0.25	0.33	0.41
L	.024	.032	.040	0.61	0.81	1.02
N	24			24		
α	0°	5°	8°	0°	5°	8°

Figure 17. Dimensions of SOP24 Package SOIC



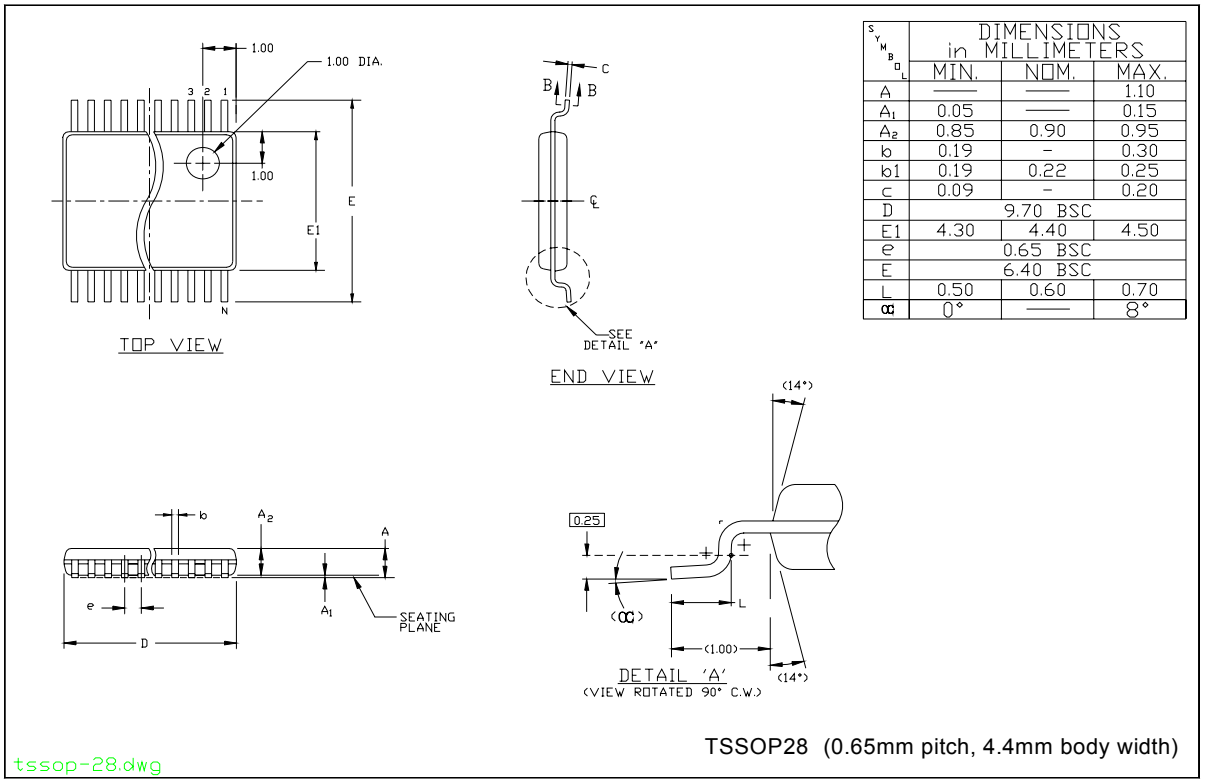
SYMBOL	DIMENSIONS in MILLIMETERS		
	MIN.	NOM.	MAX.
A	——	——	1.10
A_1	0.05	——	0.15
A_2	0.85	0.90	0.95
b	0.19	-	0.30
b1	0.19	0.22	0.25
c	0.09	-	0.20
D	7.80 BSC		
E1	4.30	4.40	4.50
e	0.65 BSC		
E	6.40 BSC		
L	0.50	0.60	0.70
α	0°	——	8°

Figure 18. Dimensions of TSSOP24 Package



SYMBOL	DIMENSIONS in INCHES			DIMENSIONS in MILLIMETERS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	.097	.101	.104	2.46	2.56	2.64
A_1	.0050	.009	.0115	0.127	0.22	0.29
A_2	.090	.092	.094	2.29	2.34	2.39
B	.014	.016	.019	0.35	0.41	0.48
C	.0091	.010	.0125	0.23	0.25	0.32
D	.701	.706	.711	17.81	17.93	18.06
E	.292	.296	.299	7.42	7.52	7.59
e	.050 BSC			1.27 BSC		
H	.400	.406	.410	10.16	10.31	10.41
h	.010	.013	.016	0.25	0.33	0.41
L	.024	.032	.040	0.61	0.81	1.02
N	28			28		
α	0°	5°	8°	0°	5°	8°

Figure 19. Dimensions of SOP28 Package SOIC



SYMBOL	DIMENSIONS in MILLIMETERS		
	MIN.	NOM.	MAX.
A	——	——	1.10
A_1	0.05	——	0.15
A_2	0.85	0.90	0.95
b	0.19	–	0.30
b1	0.19	0.22	0.25
c	0.09	–	0.20
D	9.70 BSC		
E1	4.30	4.40	4.50
e	0.65 BSC		
E	6.40 BSC		
L	0.50	0.60	0.70
α	0°	——	8°

Figure 20. Dimensions of TSSOP28 Package

21 Ordering Information

Packaged Device:

EM6607 SO28 A - %%%

Package:
SO28 = 28 pin SOIC
SO24 = 24 pin SOIC
TP28 = 28 pin TSSOP
TP24 = 24 pin TSSOP

Delivery Form:
A = Stick
B = Tape&Reel

Customer Version:
customer-specific number
given by EM Microelectronic

Device in DIE Form:

EM6607 WS 11 - %%%

Die form:
WW = Wafer
WS = Sawn Wafer/Frame
WP = Waffle Pack

Thickness:
11 = 11 mils (280um), by default
27 = 27 mils (686um), not backlapped
(for other thickness, contact EM)

Customer Version:
customer-specific number
given by EM Microelectronic

Ordering Part Number (selected examples)

Part Number	Package/Die Form	Delivery Form/ Thickness
EM6607SO28A-%%%	28 pin SOIC	Stick
EM6607SO28B-%%%	28 pin SOIC	Tape&Reel
EM6607SO24A-%%%	24 pin SOIC	Stick
EM6607SO24B-%%%	24 pin SOIC	Tape&Reel
EM6607TP28B-%%%	28 pin TSSOP	Tape&Reel
EM6607TP24B-%%%	24 pin TSSOP	Tape&Reel
EM6607WS11-%%%	Sawn wafer	11 mils
EM6607WP11-%%%	Die in waffle pack	11 mils

Please make sure to give the complete Part Number when ordering, including the 3-digit customer version. The customer version is made of 3 numbers %%% (e.g. 008 , 012, 131, etc.)

21.1 Package Marking

24/28-pin SOIC marking:

First line:	E	M	6	6	0	7		%	%	%	Y
Second line:	P	P	P	P	P	P	P	P	P	P	P
Third line:	C	C	C	C	C	C	C	C	C	C	C

24-pin TSSOP marking:

E	M	6	6	0	7	%	%
P	P	P	P	P	P	P	P
		C	C	C	C	Y	P

28-pin TSSOP marking:

First line:	E	M	6	6	0	7		%	%	%	Y
Second line:	P	P	P	P	P	P	P	P	P	P	P
Third line:				C	C	C	C	C	C	C	C

Where: %%% or %% = customer version, specific number given by EM (e.g. 008, 012, 131, etc.)
PP…P = Production identification (date & lot number) of EM Microelectronic
Y = year of assembly
CC…C = Customer specific package marking on third line, selected by customer

21.2 Customer Marking

There are **11** digits available for customer marking on **SO24/28, 4** for **TSSOP24,** and **8** for **TSSOP14.**