3D Active Long Range Front-End

General Description

The EM4083 is a CMOS integrated circuit intended for hands-free or multidimensional wireless communication systems at 125kHz.
It integrates a high sensitivity low frequency AM receiver together with digital functions accessible through a Serial Standard Interface.
EM4083 provides a wake-up signal to an external microcontroller upon reception of a valid programmable header and then a high-speed data transfer and decoding for long range applications at 125kHz.

Applications

- Keyless entry systems
- Tire pressure systems
- Intelligent sensors
- Intelligent access control

Features

- 115kHz –140kHz Frequency Bandwidth.
- 3 antennas interface for 3D reception.
- Low current consumption < 3.5µA.
- High sensitivity (1mV$_{pp}$)
- More than 2.5m distance in typical applications.
- 32x16 bits EEPROM (432 bits user memory).
- On Chip capacitors for antenna tuning
- On Chip resistor for Antenna Quality Factor tuning
- 4 wires Microcontroller Serial interface (SPI).
- 8 bits (EEPROM programmable) Header detection.
- Manchester data decoder (data rate 4Kbd).
- Data transmission performed by 100% amplitude modulation (OOK) in Up-Link.
- -40°C to +85°C Temperature range.
- 3V power supply battery
- TSSOP16 package.

Typical Application

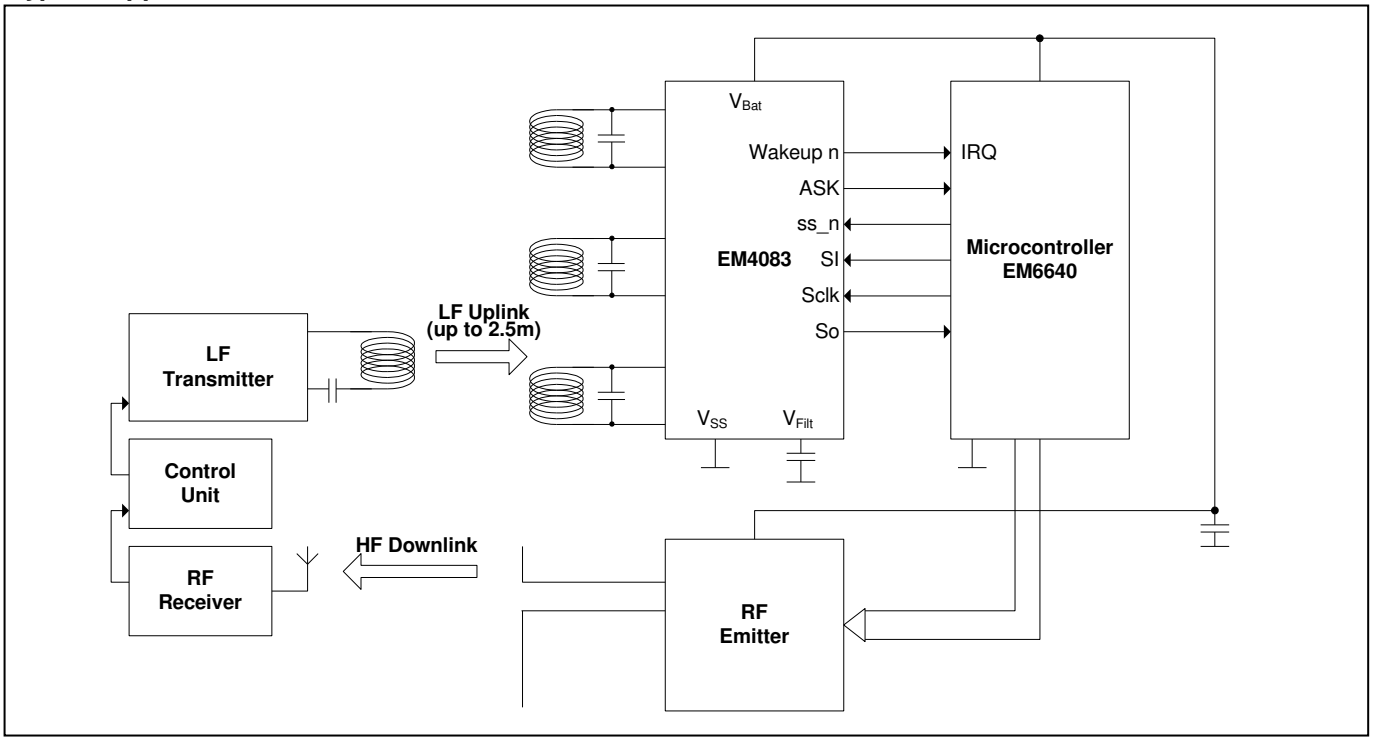


Fig.1

TABLE OF CONTENTS

1. Block Diagram

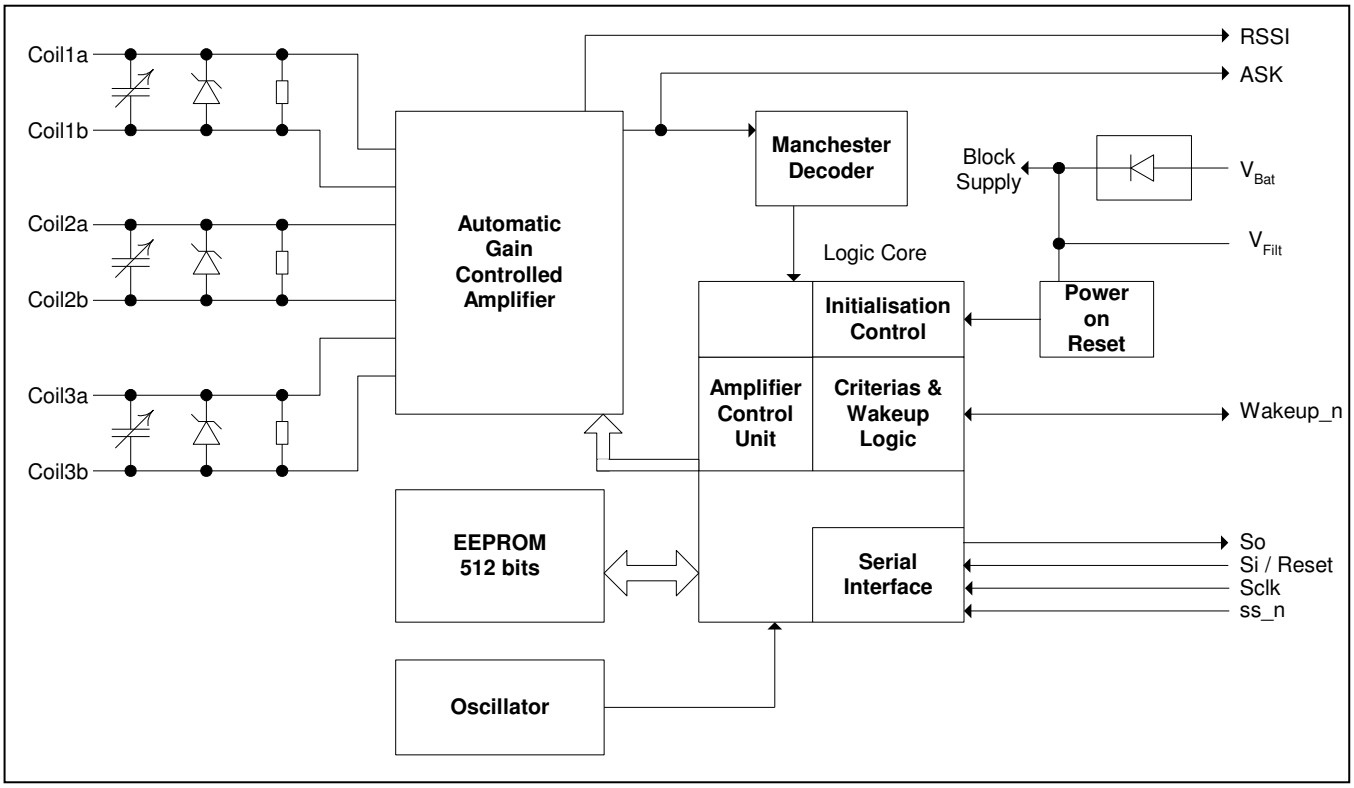


Fig. 2

2. Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions should be taken as for any other CMOS components. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within supply voltage range.

3. Electrical Specifications

3.1 Absolute Maximum Ratings

V_{SS} = 0V

Parameter	Symbol	Min	Max.	Unit
Extreme Supply Voltage	V_{BATEX}	-0.3	5.5	V
Voltage at any other pin except Coils	V_{PIN}	V_{SS}-0.3	V_{Bat}+0.3	V
Storage temperature	T_{STORE}	-55	125	℃
Maximum AC peak current induced on Coils	I_{COILEX}	-30	30	mA
Electrostatic discharge according to MIL-STD 883C, method 3015	V_{esd}	-2000	+2000	V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operation section of this specification is not implied. Exposure beyond specified electrical characteristics may affect reliability or cause malfunction.

3.2 Operating Conditions

V_{SS} = 0V

Parameter	Symbol	Min	Typ.	Max.	Unit
Supply Voltage	V_{Bat}	2.2	3	4	V
Operating temperature	T_{OP}	-40	25	85	℃
AC peak current induced on Coils inputs	I_{COILOP}	-10	-	10	mA

Exposure beyond these parameters range may cause malfunction.

3.3 Electrical Characteristics

Unless otherwise specified: V_{Bat} = 3V, T_A = -40 to +85℃.

Parameters	Symbol	Conditions	Min.	Typ.	Max.	Unit
Current Consumption						
ModeOff	I_{OFF}	S_{TDBY} period		1.6	3.0	µA
ModeOn	I_{ON}	S_{CAN} period		15	22	µA
Power On Reset						
Power On reset level	V_{POR_f}	POR inactive Vfilt decreasing	0.9	1.4	2.0	V
Power On reset level	V_{POR_r}	POR inactive Vfilt increasing	1.0	1.5	2.1	V
VBAT diode						
Forward drop	V_F	I_{charge} = 100µA on **V_{FILT}**		60	100	mV
Reverse current leakage	I_r	V_{Bat} = 0V @25℃ V_{FILT} = 3V		20	80	nA
Input Coil Limitors						
Maximum coil voltage	V_{limMax}	+ 10mA DC forced with reference to V_{SS}	7.6	9	10.6	V

Electrical Characteristics (continued)
Unless otherwise specified: V_{Bat} = 3V, T_A = -40 to +85°C.

Parameters	Symbol	Conditions	Min.	Typ.	Max.	Unit
EEPROM						
Read/Write Voltage	V_{EE}		2.2		4	V
Supply current / read	I_{RD}	Read mode		6	20.0	µA
Supply current / write	I_{WR}	Write mode		45	100	µA
Digital I/O						
Output logic High	V_{OH}	V_{Bat} = 2.2V I_{OH} = 500uA	V_{Bat} -0.5			V
Output logic Low	V_{OL}	V_{Bat} = 2.2V I_{OL} = 1mA			0.52	V
Digital input logic Low	V_{iL}	V_{Bat} = 2.2V	Vss		0.3 V_{Bat}	V
Digital input logic High	V_{iH}	V_{Bat} = 2.2V	0.85 V_{Bat}		V_{Bat}	V
Input Sensitivity in Receive mode	V sens	T_A = 25°C	0.7	1	1.3	mV_{pp}
			0.15	1	2	mV_{pp}
Antenna Tuning						
Coil resonant capacitor tuning on each antenna	C_{COIL}	**CoilxQ[3:0]**				
		00000		0.8		pF
		00001 (note 2)		2		pF
		00010 (note 2)		4		pF
		00100 (note 2)		8		pF
		01000 (note 2)		16		pF
		10000 (note 2)		32		pF
Switch resistor off	R_{Switch}	(note 4)	10			MΩ
Switch resistor on		(note 4)			2	KΩ
Coil resistor tuning on each antenna	R_{COIL}	**CoilxQ[3:0]** (note1)				
		0001	15	27	40	kΩ
		0100	30	54	80	kΩ
		0010	60	105	160	kΩ
		1000	120	210	320	kΩ
		0000 (note3)	20			MΩ

Note1: Other codes are forbidden.
Note2: Parasitic capacitors are not included
Note3: Open circuit parasitic resistor, with Vcoil <10mVpp. Value guaranteed by design.
Note4: Guaranteed by design

3.4 Timing Characteristics

Unless otherwise specified: V_{bat} = 3V, T_A = -40 to +85°C.

Parameters	Symbol	Conditions	Min.	Typ.	Max.	Unit
EEPROM						
EEPROM data endurance	N_{CY}	Erase all / write all, V_{Bat} = 4V	100'000			cycles
EEPROM retention	T_{RET}	T_{OP}= 55°C, after 100000 cycles (note1)	10			years
EEPROM write time	T_{WREE}	(note 2)			30	ms
Power On Reset						
POR Delay	T_{POR}	(note 3)			2	ms
Initialisation time	T_{init}	(note 4)			30	ms
Serial Interface (see Fig. 3)						
SS_n setup time to CLK pos edge	Tcsset	V_{Bat} = 2.2V	450			ns
SS_n hold time to CLK neg edge	Tcshold	V_{Bat} = 2.2V	450			ns
SI setup time to CLK pos edge	Tdset	V_{Bat} = 2.2V	450			ns
SI hold time to CLK pos edge	Tdhold	V_{Bat} = 2.2V	100			ns
Access time CLK to So	tacct	V_{Bat} = 2.2V			500	ns
CLK period	Tperi		4			µs
Timing of Manchester coding						
Half bit duration: 0 →0 transition 1 →1 transition	T_{short}	(note 5)	113	128	160	µs
Bit duration: 0 →1 transition 1 →0 transition	T_{long}	(note 5)	220	256	290	µs

Note 1: Based on 1'000 hours at 150°C.
One should take care when writing the EEPROM. The EEPROM content is guaranteed only if write operation is done at a supply voltage (V_{FILT}) higher than 2.2V.

Note 2: T_{WREE} Includes Erase & Write time.

Note 3: A delay T_{POR} is added in order to assure a proper reset of the EM4083.

Note 4: After a reset (through SPI or supply voltage), the EM4083 needs a maximum of 30ms to set EM4083 configuration according to the EEPROM bits. During the T_{init} period, the EM4083 should not be used.

Note 5: Emitter must be adapted to respect these timings on the EM4083 (refer to Fig 12).

Serial interface access timing

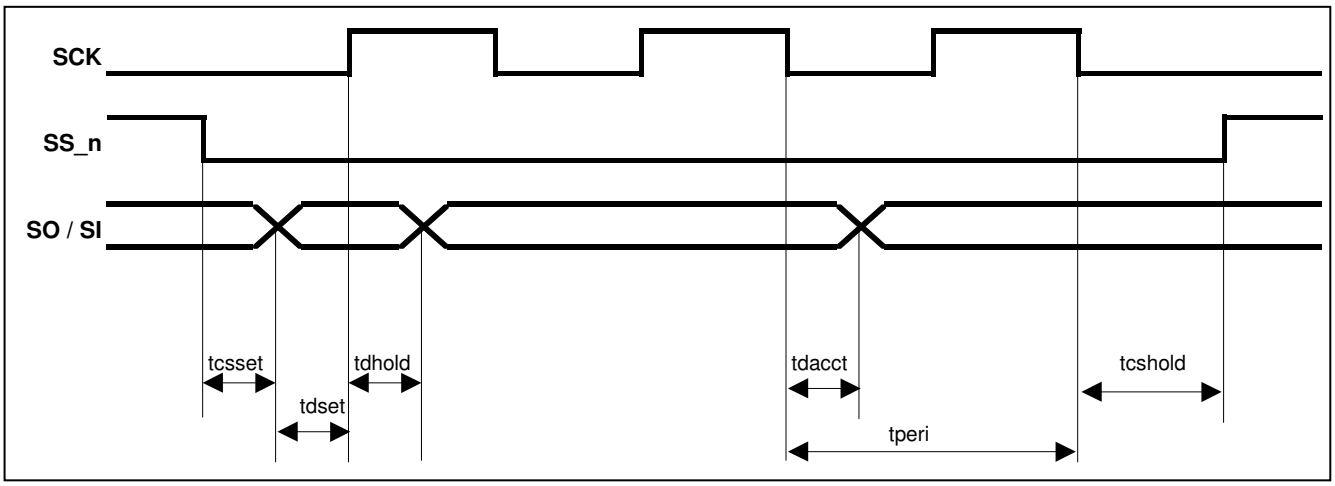


Fig. 3

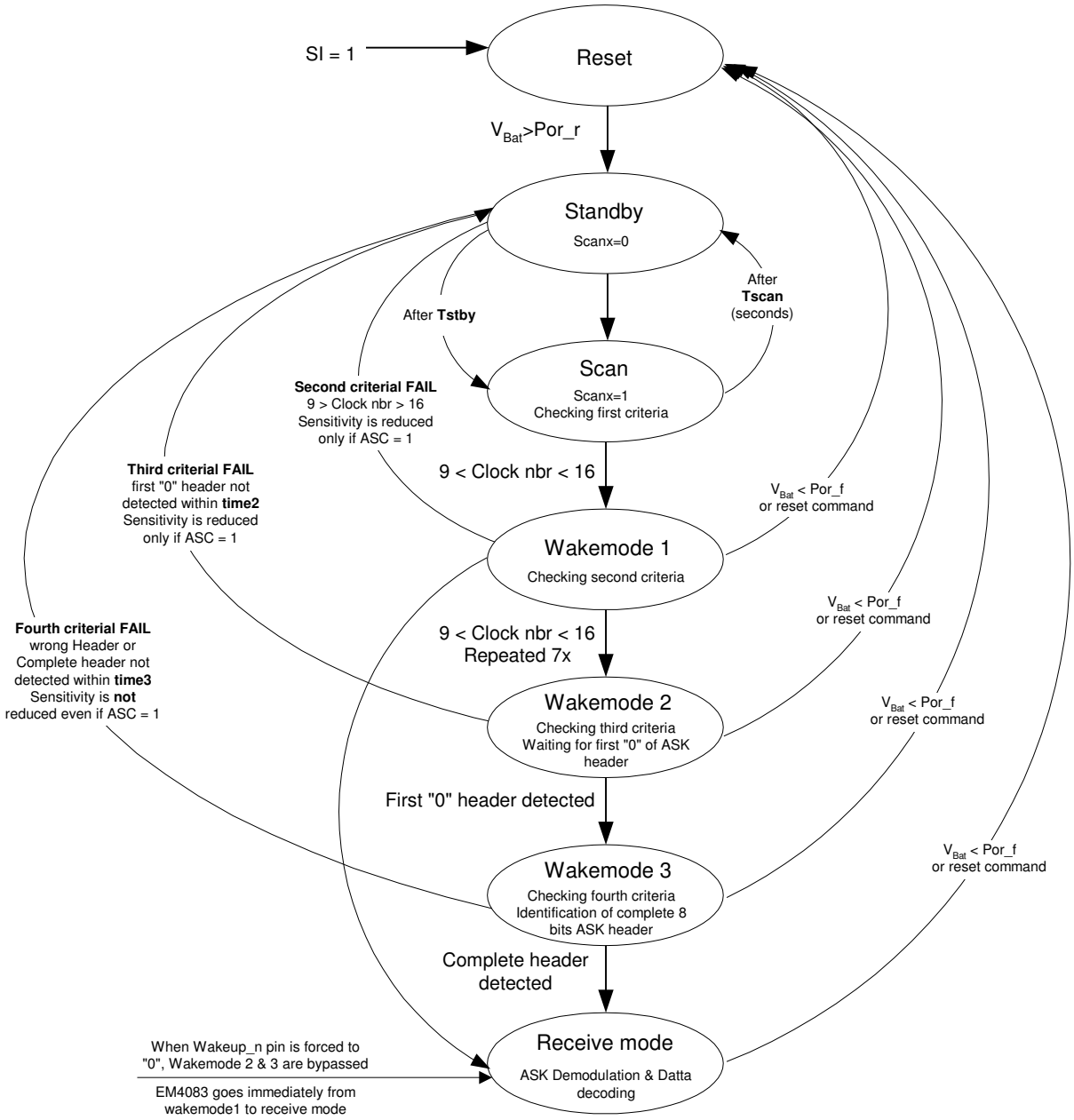
4. General Description

EM4083 provides a high-speed (4Kbd) data transfer and decoding for long range applications at 125KHz.
It also provides an external acknowledge (wakeup_n pin) to wakeup a microcontroller when the correct 8bit header has been detected.
7 bits of this header are user free and can be programmed in the EEPROM using a 4 wire serial interface.
After the header detection, the chip enters in a receive mode and allows to decode data continuously on the selected antenna.

4.1 Wake Up Description

This chapter explains how the C4083 goes from the scanning mode to the receive mode.
To wake up the C4083, clocks and envelope of the field are analysed and several criteria must be fulfilled. The following state machine describes all of these criteria.

EM4083 State Machine



4.1.1 Scanning mode

In order to reduce the consumption of EM4083, a scanning of coil input signal is done.
The scan period can be programmed and adjusted for a dedicated application. With short standby duration, the complete wake up sequence will be also shorter. In this case, the average device consumption comes higher.
During the scan window, the circuit periodically switches on its field clock extractor block in order to detect a LF signal.
The scanning is done alternatively on the 3 antennas (coil1, coil2, and coil3).
When this block is "off"" the circuit is in Standby mode (Consumption $\mathbf{I_{off}}$) otherwise in Scan mode (Consumption $\mathbf{I_{on}}$).
Without any signal, after a fixed period ($\mathbf{T_{scan}}$) it switches off this block and returns to a minimum current consumption state during a programmable period $\mathbf{T_{stby}}$.
This mode of operation results in a trade off between the DC current consumption and the scanning time.

The EM4083 automatically scans the 3 antennas in order to detect a carrier sent by the Control Unit (LF emitter).
The detection of the field presence is called the first criteria.

4.1.2 First criteria

When the device is in a scan window, a counter is used to count the extracted field clocks during 100µs.
If the clock number is comprised between 9 and 16, the first criteria succeeds (digital filter).
In that case, the chip goes in the wakemode1 and the receiver will remind on the same antenna.

If the number of clocks is 9 > nbr clocks > 16, the first criteria fails, the EM4083 goes back to the standby mode and the scan will go on with the following antenna.
By this way, the input signal frequency bandwidth is reduced, and in the worst case, no wakeup is possible outside 80KHz –200KHz bandwidth, even with large magnitude signals.
This first criteria is repeated antenna per antenna until it succeeds on one of the 3 antennas.

Scanning mode on Coil1, Coil2 and Coil3

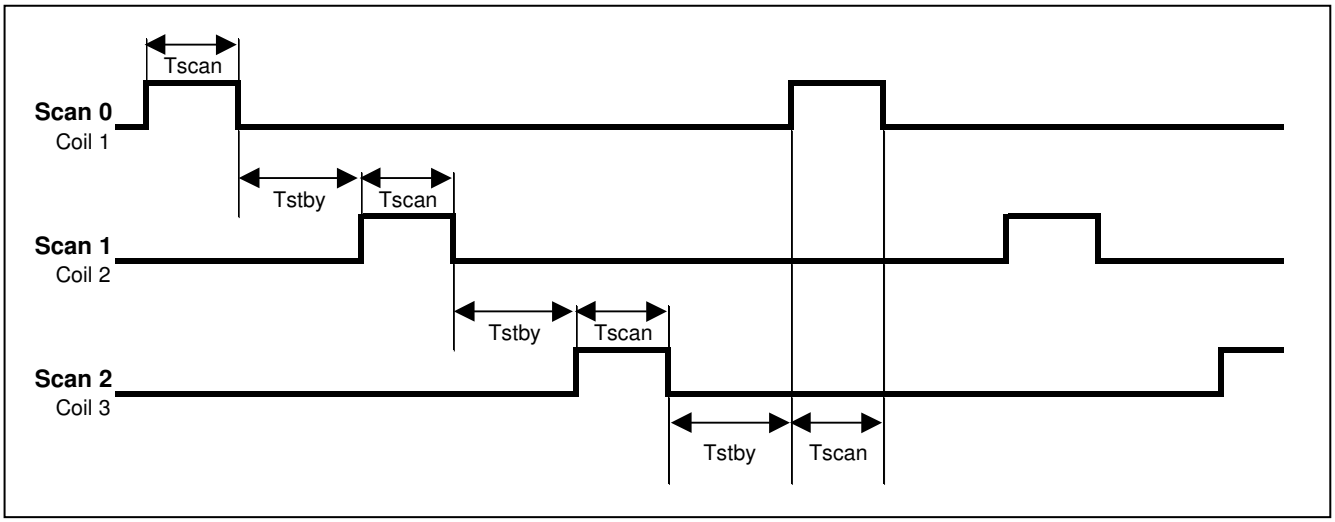


Fig. 4

4.1.3 Wakemode1 (Second criteria):

In this mode, the check of field strength will go on with the same antenna that succeeds with the first criteria.
The clock counts (9 < nbr clocks < 16) must be confirmed 7 times in order to succeed.
During the last count (7^{th}), the EM4083 checks that the ASK (envelop detector) is also stable during at least 100µs.
If the 7 checks succeed (field presence), the EM4083 Analog Front End exits the current mode and enters in the third criteria.
If the 7 checks fails (missing clocks in weak field), the chips goes back to the standby mode and the scan will go on with the following antenna in order to check once again the criteria1.

4.1.4 Wakemode2 (Third criteria):

In the Wakemode2, the EM4083 is waiting for the first bit of the header (Start bit must be " 0 ").
The " 0 " header detection consists of the identification of the following pattern:

Start bit Header " 0 "

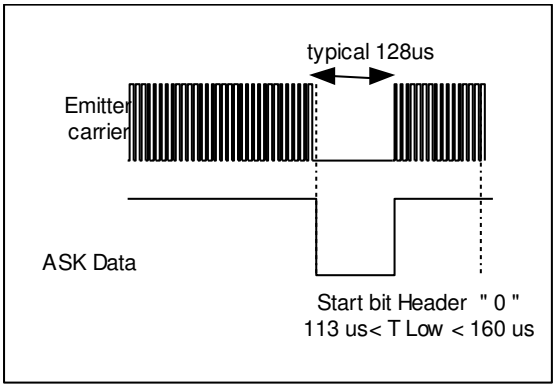


Fig. 5

As soon as the second criteria has been detected, a timer based on an internal oscillator starts.
After a timeout time2 (see table 1), if the "0" has not been detected, the chip goes back to the standby mode.

This timer is used to avoid the chip to stay in a dead lock state once he has detected a parasitic carrier.
After the detection of the start bit of header, the EM4083 goes to the Wakemode3.

4.1.5 Wakemode3 (Fourth criteria):

The fourth criteria consists of the detection of the complete 8 bits header ("0" + 7 bits programmable through Word 4 of EEPROM).
The bitclock signal extracted from the Manchester decoder is used to decode the data stream on the falling edge.
This signal can be used by a microcontroller on pin SO when the serial interface (SPI) is not used (SS_n ="1").
If the complete header is correctly identified, within the time 3 (see table 1), and the chip goes in the receive mode.

EM4083 will stay in receive mode until it receives a reset command or a power down (Vbat < V_{POR_f}).
If the header detection fails (due to wrong header, parasitic signal, …) the chip goes back to the scanning mode.

4.1.6 Procedure to succeed in a complete header detection:

- **ASK pin** provide the envelope of the input signal on the selected antenna.
- **SO pin** provides the clock bit used to decode ASK data. This signal is generated by the internal Manchester Decoder.
- **WAKEUP_N pin** provides an acknowledge (negative pulse 100µs, typical) when all criterias succeed. After this acknowledge, the device is in receive mode.

Correct Header Detection & Data transmission

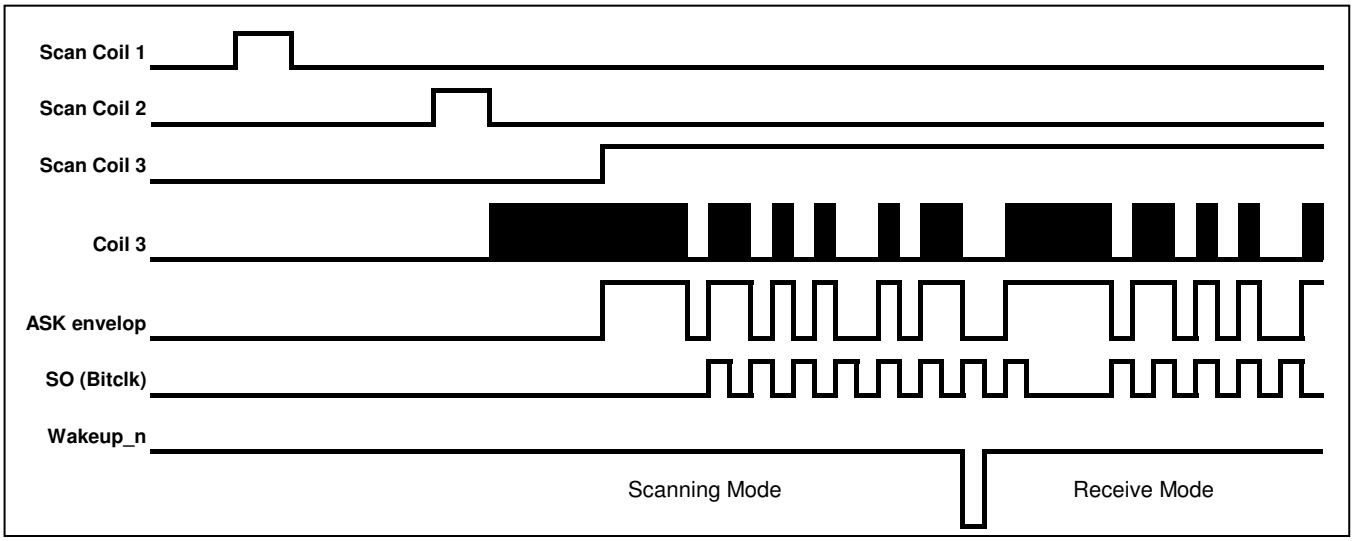


Fig. 6

Zoom on Wakemode1 & Wakemode2

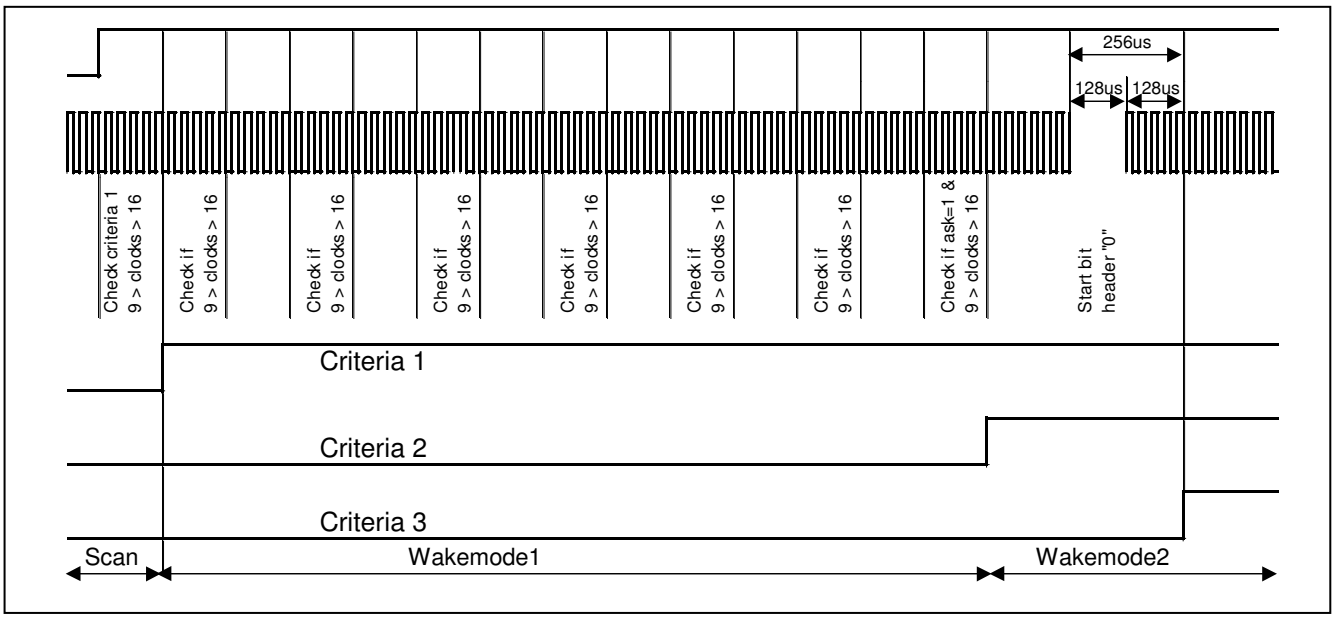


Fig. 7

Zoom on Header detection

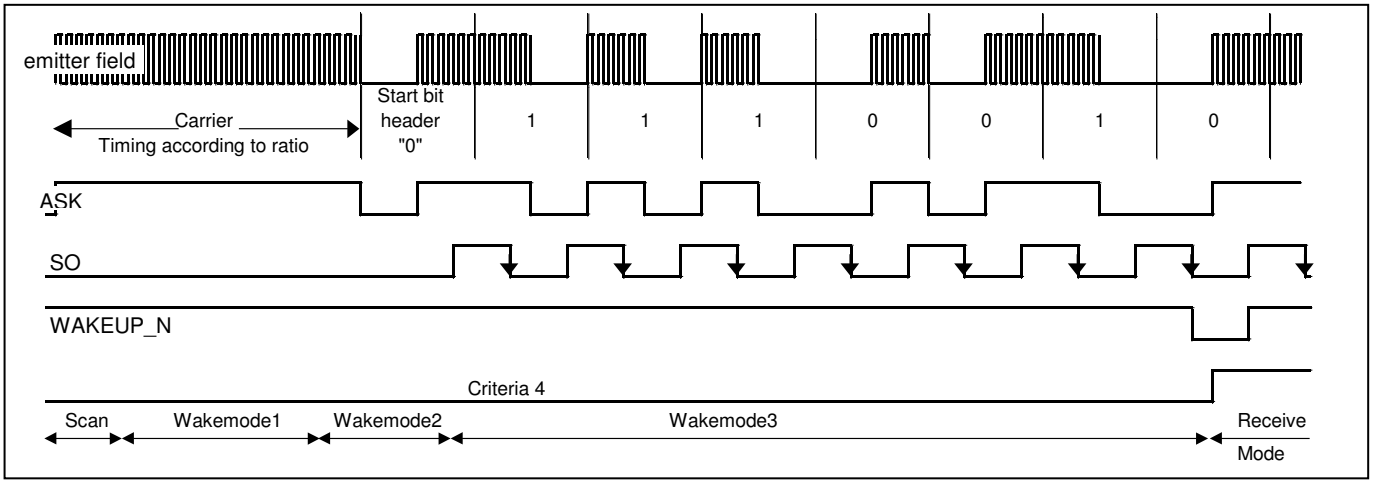


Fig. 8

Timings for wakeup and header detection

Ratio	Code	Tstby (note 1)	Tscan (note 1)	Tcarmin	Tcarmax	Tcarrier recommended	Time2 (note 1)	Time3 (note 1)	Unit
Ratio 1/2	000	200	200	3122	3780	3451	3780	5760	µs
Ratio 1/3	001	400	200	3791	4320	4056	4320	6300	µs
Ratio 1/4	010	600	200	4460	4860	4660	4860	7020	µs
Ratio 1/5	011	800	200	5129	5580	5355	5580	7740	µs
Ratio 1/6	100	1000	200	5798	6120	5959	6120	8280	µs
Ratio 1/7	101	1200	200	6467	6660	6564	6660	8820	µs
Ratio 1/8	110	1400	200	7136	7200	7168	7200	9360	µs
Ratio 1/9	111	1600	200	7805	7920	7863	7920	10080	µs

Table. 2

Note1: These timings are controlled by the internal oscillator.

5. Blocks Description

EM4083 includes the following main blocks:

- Manchester decoder
- Reset mode
- Amplifier with Automatic Gain Control (AGC)
- Automatic Sensitivity change (ASC)
- Resonant capacitor tuning
- Coils input limiters
- Quality factor tuning
- Power supply filtering bloc
- EEPROM
- Serial Peripheral Interface (SPI)
- RSSI Function

5.1 Manchester Decoder

A Manchester decoder is used to extract data on the selected antenna.
Using the ASK signal (signal envelop extracted from the coils), the chip provides the bitclock signal on SO pin.
This signal can be used to latch the data on the falling edge.
The decoder starts providing the bitclock as soon as, a first “0” of the header is detected. One may notice that the bitclock signal (SO) appears only after the start bit detection in the header.

Examples of data decoded data streams

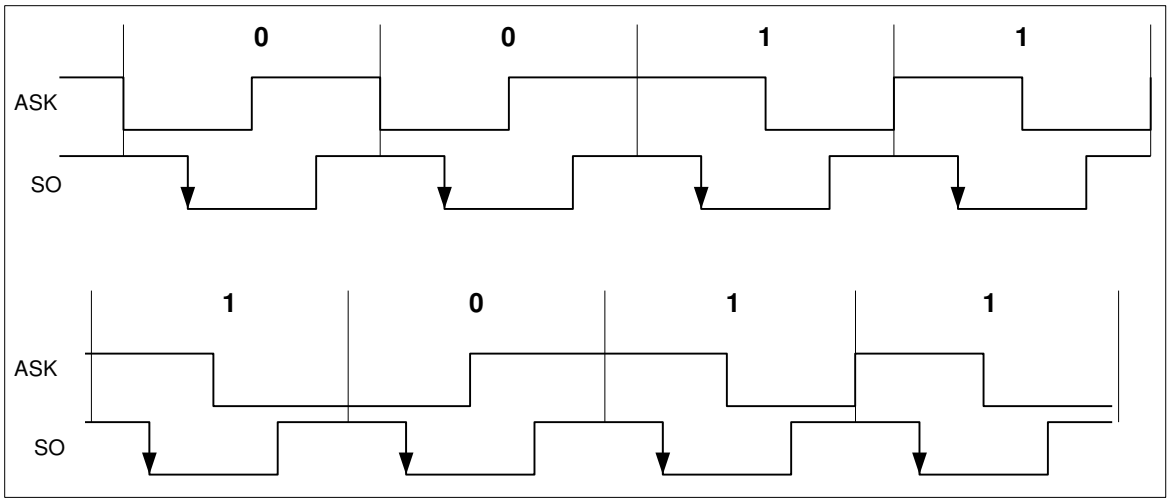


Fig. 10

An unlimited pure carrier can be send between two data streams.
The Only constraint is that the end of the data stream must stop by a “1” Manchester coded and start by a “0” Manchester coded bit in order to keep the decoding functionality.

Transition to receive mode or between two data streams

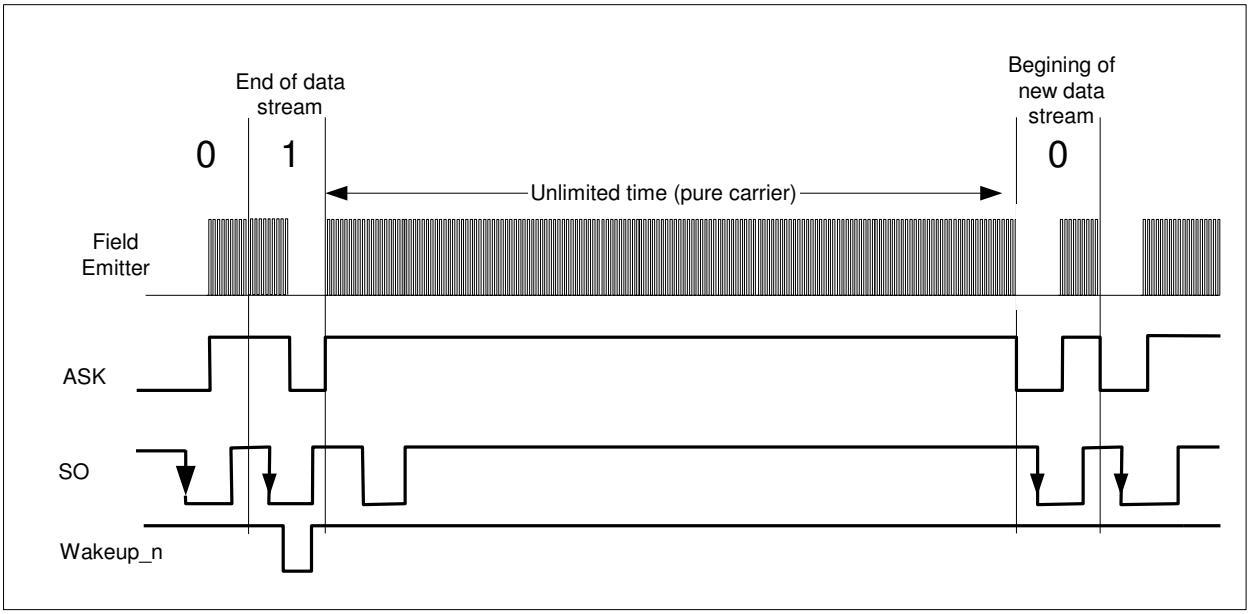


Fig. 11

Manchester decoder limits of functionality

The data stream decoding is limited by the ASK signal distortion mainly due to the antenna effects (Qfactor, signal damping).
One has to take care of the way of the amplitude modulation and the Q factors of antennas (emitter & EM4083) in order to keep the EM4083 functionality.
A delay of the falling edge of ASK may appear in the case of high Q factors and slow damping of emitter.

The modulation length from the emitter side must be adapted in order to keep the ASK signal, as specified in the chapter 3.4 Timing Characteristics, in weak field and in strong field.

Timing definition of Manchester coding

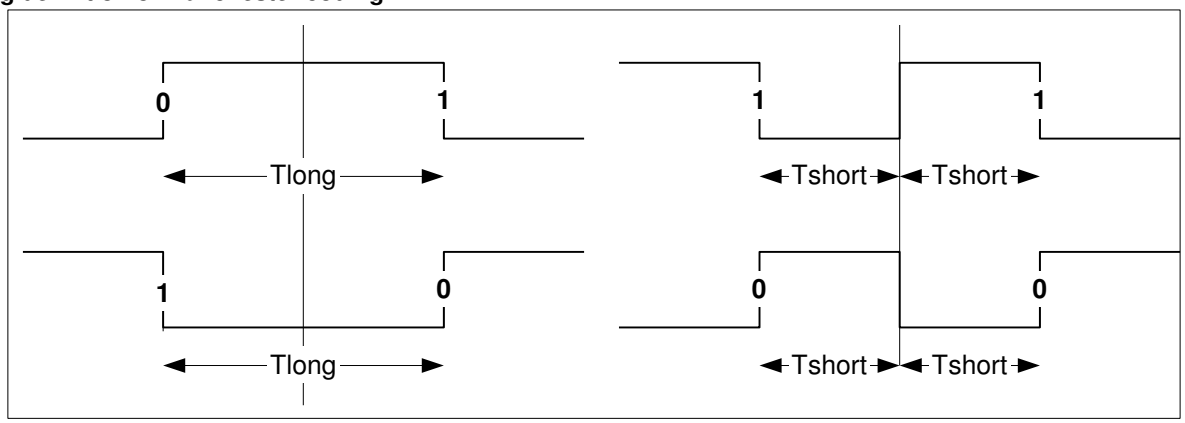


Fig. 12

5.2 **Reset Mode**

It is possible to reset the EM4083 by 3 ways:

1. The V_{FILT} voltage is monitored in order to reset the EM4083 in the case of power down.
   When V_{FILT} goes down the Vpor_f value, the chip will go in the reset state.
   The chip is kept in this mode until V_{FILT} goes up Vpor_r.
   A hysteresis is provided to avoid improper operation at limit level.

2. It is also possible to reset the chip by software, using the SPI. Once, the EM4083 is in reset state, it will stay in this mode until SS_N = **" 0 "**.(cf SPI chapter).

3. When the SPI is not used (SS_N = **"** 1 **"**) and a high level **"** 1 **"** is applied on pin SI, the EM4083 goes to a reset state and reminds in this mode until the level on SI pad returns to a low level **" 0 "**. SI pin can be used as a reset pin and as the SPI data input when the SPI interface is selected.

When the chip goes out of reset mode, the EM4083 initialisation starts. During this timing (T_{init}), the EM4083 is not functional.

Reset modes of EM4083

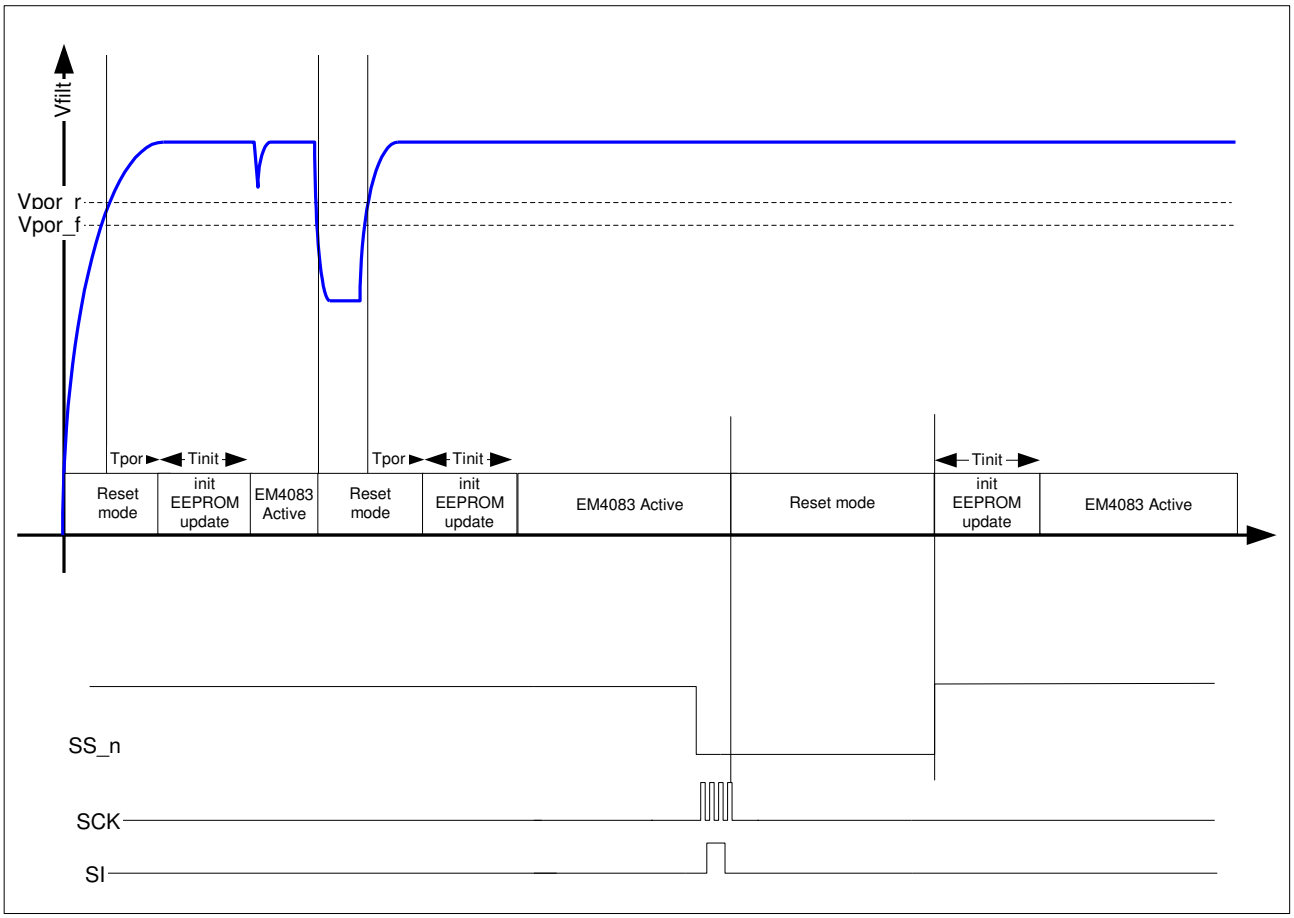


Fig. 13

5.3 **Amplifier with Automatic Gain Control (AGC)**

This block is used to extract the field clock and the envelope of the coil signal.

One may notice that the EM4083 contains only one amplifier chain and the scanning is done on the 3 antennas.

With that kind of architecture, the dispersions are reduced from one antenna to the other one because the amplifier is the same for each antenna.

The amplifier chain is **A**utomatic **G**ain **C**ontrolled amplifier. With that kind of amplifier, it is possible to amplify a large range of input signal.

The Gain is automatically adjusted according to the input signal on the scanned antenna, in order to keep a constant magnitude on the output of the amplifier.

EM4083 amplifier diagram

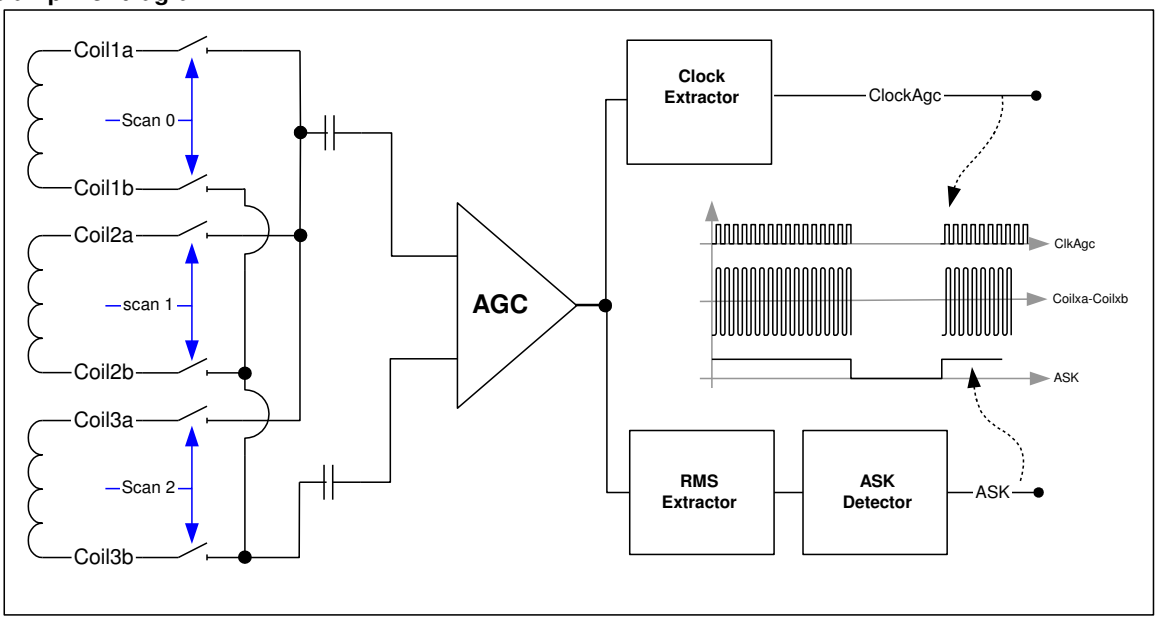


Fig. 14

AGC startup, calibration and demodulation

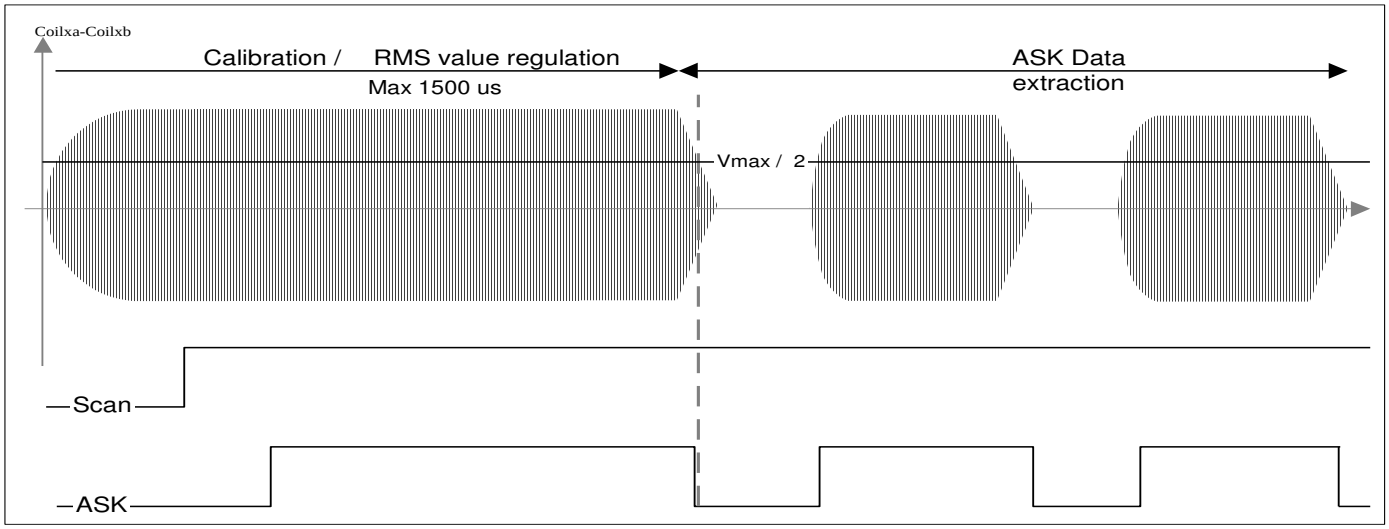


Fig. 15

Clock extraction:
The amplifier chain output is used to extract the clock issue from the antenna on which the scanning is done.
This clock is used to check criteria1 & criteria2.
This signal is used in wakemode1 & wakemode2, when checking criteria: *9 < nbr clocks < 16*.

ASK envelope extraction:
The amplifier chain output is also used to extract the envelope of the incoming signal on the antenna.
The modulation extraction is done when the coil signal reaches 50% of the magnitude of the calibration signal.
To ensure a correct timing of pause detection, the input voltage level must not decrease by more than 20% from burst to burst.

5.4 Automatic Sensitivity Change (ASC)

The Automatic Sensitivity Change can be used to reduce the power consumption in the case of parasitic field.
In fact when this function is disabled, and when the chip is put in a parasitic field (80Khz- 200Khz), the criteria 1&2 will always be successful.
The chip will always goes back to the scan mode when timer 3 occurs (ie no " 0 " header detected).
This will induce in higher power consumption since the ratio between standby duration and scan duration is disturbed by the detection of parasitic field.
This function is optional and can be disabled using the ASC bit in EEPROM (b[0], Word4).

Power consumption increase in the case of parasitic carrier

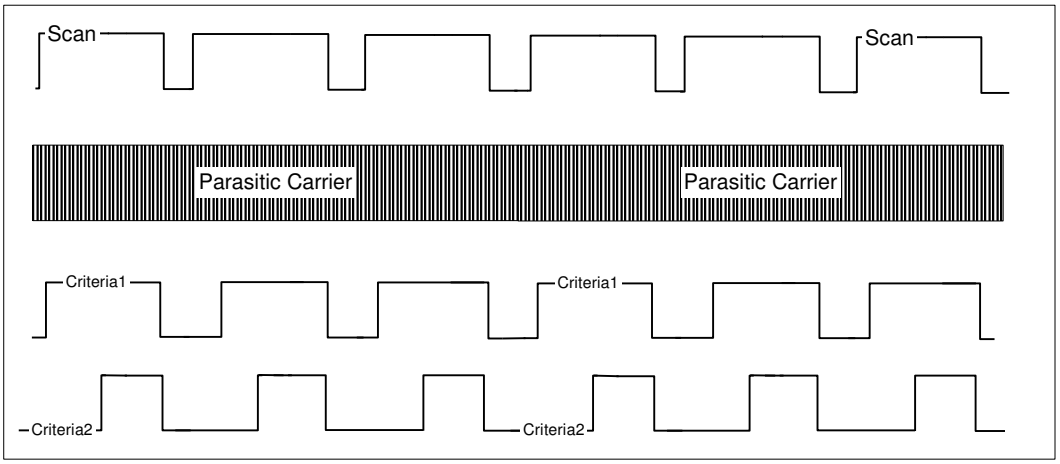


Fig. 16

The Sensitivity reduction function:
When EM4083 goes back to scan mode from Wakemode1 (after time1 occurs) & Wakemode2 (after time2 occurs), the sensitivity level of the input amplifier is reduced during Timepar in order not to wakeup once again on a parasitic carrier.
For example, after detection of a parasitic carrier the chip goes from Wakemode2, back to scan mode with a new level (4mVpp) of sensitivity for the next scan window.
If the parasitic magnitude is higher than $4mV_{pp}$, the chip wakes up once again (criteria 1 & 2 detected)

Sensitivity reduction duration (Timepar)

Ratio	Timepar	Unit
Ratio 1/2	102	ms
Ratio 1/3	153	ms
Ratio 1/4	204	ms
Ratio 1/5	255	ms
Ratio 1/6	306	ms
Ratio 1/7	357	ms
Ratio 1/8	408	ms
Ratio 1/9	459	ms

Table. 3

According to the selected ratio, Timepar gives the sensitivity reduction time.
A counter that starts at the first parasitic carrier detected is used to reset the ASC function so that the maximum sensitivity (typ $1mV_{pp}$) is re-established after Timepar.

Sensitivity reduction steps during scan mode & header detection
Unless otherwise specified: V_{Bat} = 3V, T_A = 25°C

Parameter	Symbol	Typ.	Unit	Level [2:0]
Normal sensitivity level	V_{SENS1}	1	mV_{pp}	000
Occurs after 1st parasitic carrier detection	V_{SENS2}	5.6	mV_{pp}	001
Occurs after 2nd parasitic carrier detection	V_{SENS3}	9.8	mV_{pp}	010
Occurs after 3rd parasitic carrier detection	V_{SENS4}	21	mV_{pp}	011
Occurs after 4th parasitic carrier detection	V_{SENS5}	50	mV_{pp}	100
Occurs after 5th parasitic carrier detection	V_{SENS6}	123	mV_{pp}	101
Occurs after 6th parasitic carrier detection	V_{SENS7}	282	mV_{pp}	110
Occurs after 7th parasitic carrier detection	V_{SENS8}	598	mV_{pp}	111

Table. 4

Sensitivity reduction state machine

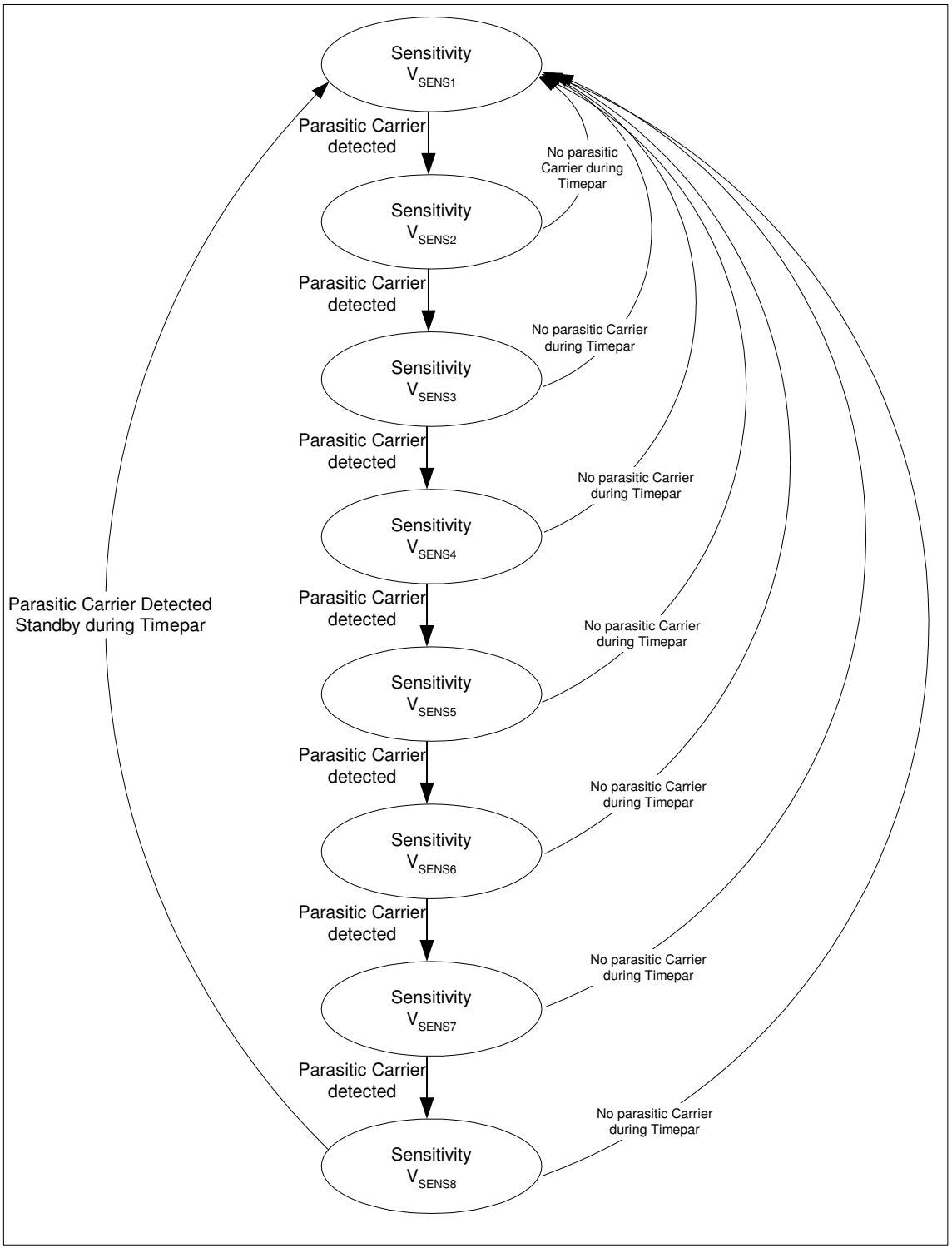


Fig. 17

Example with a parasitic carrier of 5mVpp magnitude:
In this example, a pure carrier of 5mVpp is sent to the antennas, so that criteria1&2 succeeds during the first scan window.
During the second window, the sensitivity of amplifier is reduce to 4mVpp, but because the carrier magnitude is still higher (5mVpp), the criteria1&2 succeeds once again in the second scan window.
During the third scan window, the sensitivity of amplifier is reduced to 8mVpp and then criteria1&2 fails.
The amplifier will stay in this reduced sensitivity mode during timepar.

Example with a parasitic carrier of $5mV_{pp}$

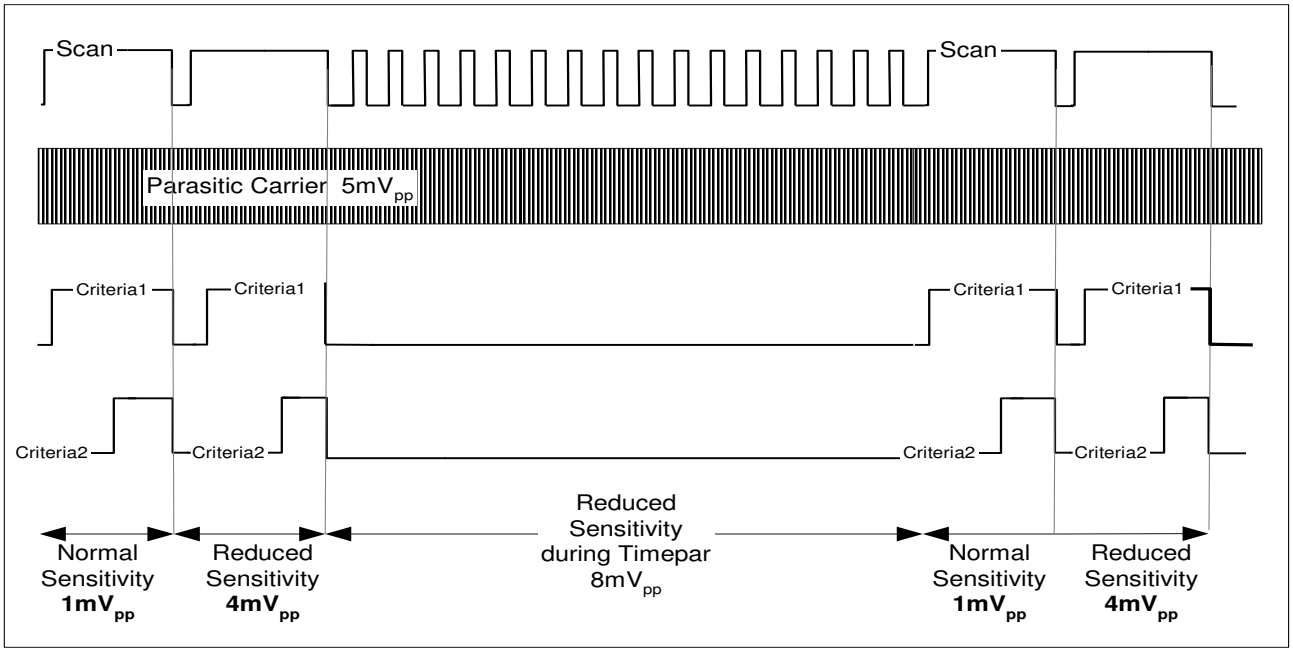


Fig. 18

This ASC function is only active during the scan or wakeup procedures.
Once the EM4083 is in receive mode (header detected), the ASC function is disabled and the sensitivity is given by the level [2:0] configuration. (EEPROM Word4).

EM4083 Sensitivity according level
It is possible to select a different level of sensitivity once the EM4083 is in receive mode.
This configuration affects only the receive mode sensitivity, after header detection.
During wakeup procedure, the normal sensitivity level is 1mVpp.

Sensitivity selection in receive mode

Level[2:0]	Vsens typ
000	V_{SENS1}
001	V_{SENS2}
010	V_{SENS3}
011	V_{SENS4}
100	V_{SENS5}
101	V_{SENS6}
110	V_{SENS7}
111	V_{SENS8}

Table. 5

Sensitivity selection example in receive mode

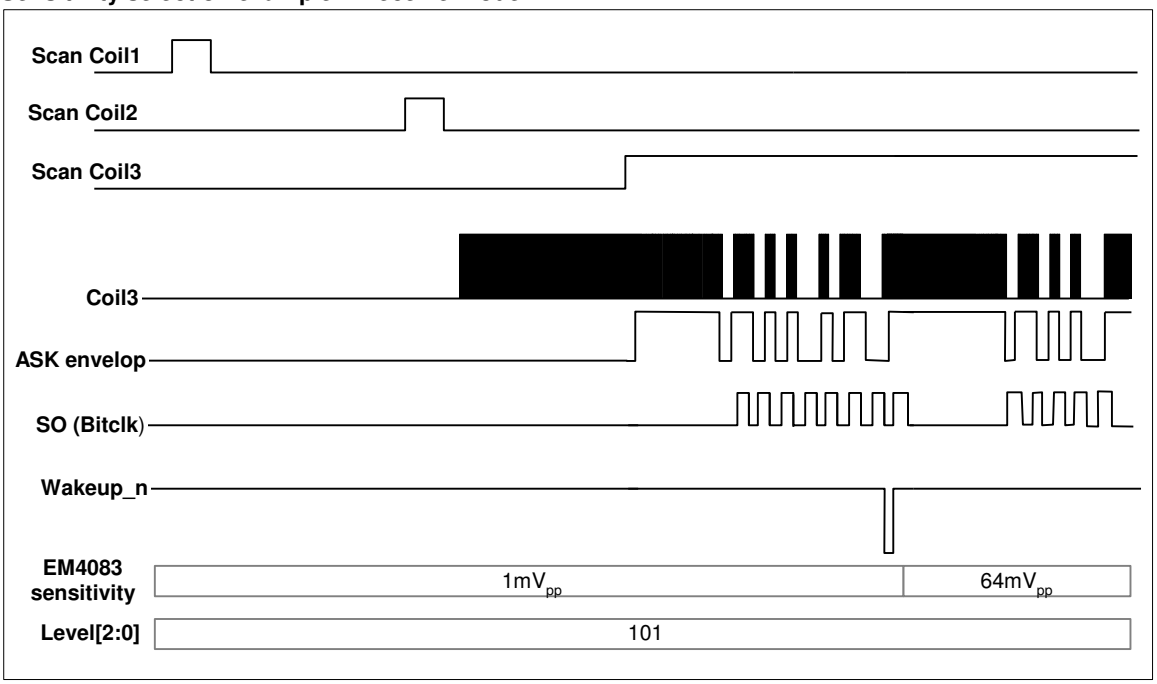


Fig. 19

5.5 Resonant capacitor tuning

One has the possibility to tune the resonant capacitor of the antenna using EEPROM bits (word 2).

Input capacitor Tuning

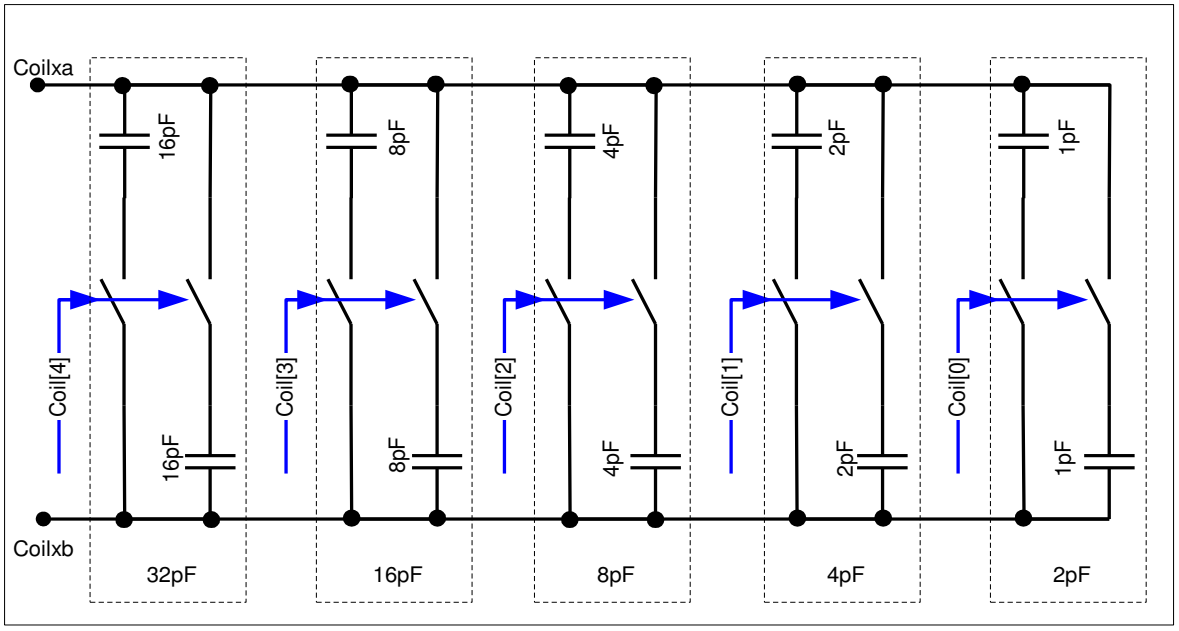


Fig. 20

Equivalent schematic for -400mV$_{peak}$ ≤ V$_{coil}$ ≤ 400 mV$_{peak}$

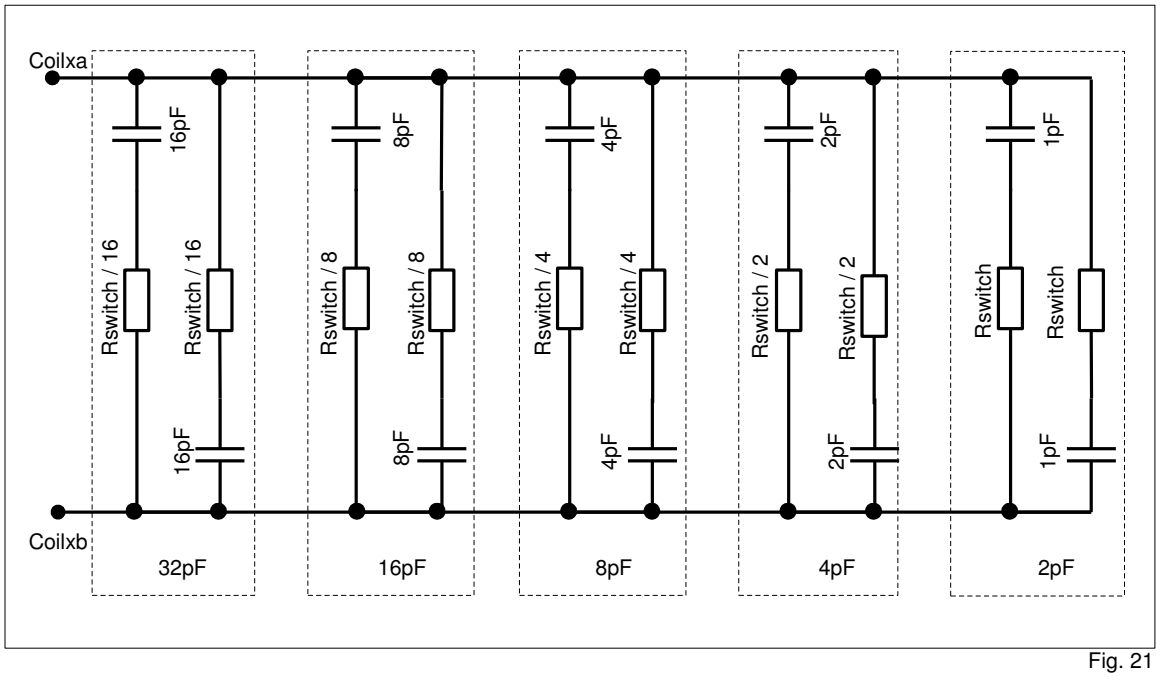


Fig. 21

Equivalent schematic for absolute Vcoil ≥ ± 400 mV$_{peak}$

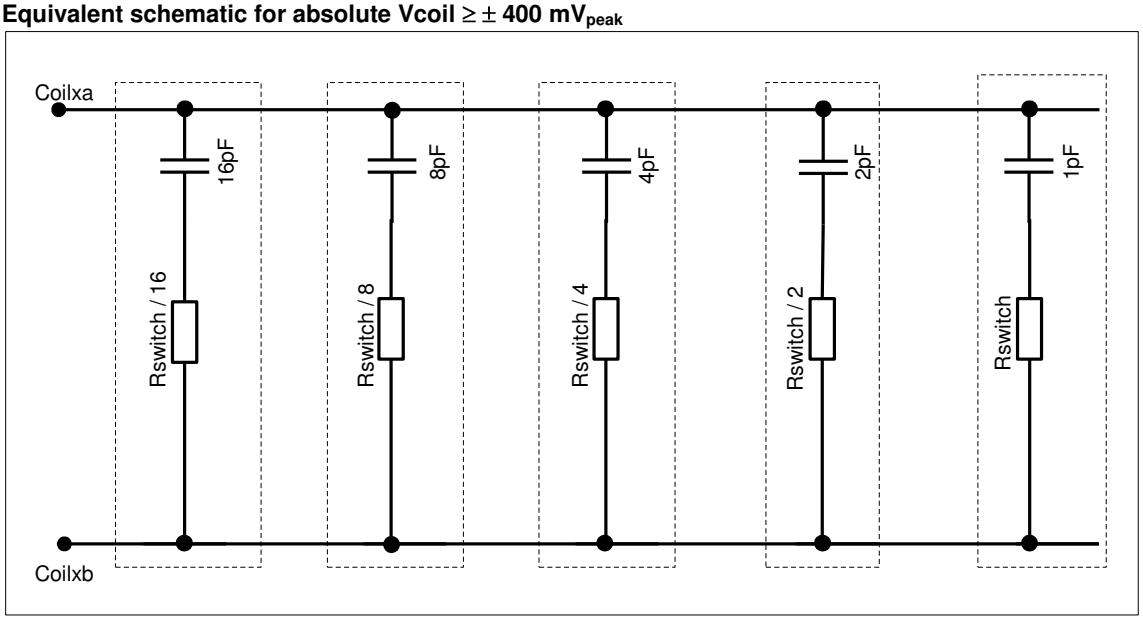


Fig. 22

Coil capacitor according Coilx[4:0]

Parameter	Symbol	Conditions	Typ.	Unit
Coil resonant capacitor tuning on each antenna	C_{COIL}	**Coilx[4:0]**		
		00000	0	pF
		00001	2	pF
		00010	4	pF
		00100	8	pF
		01000	16	pF
		10000	32	pF

Table. 6

According to Coilx[4:0] values, the total resonant capacitor can be adjusted from 2pF up to 62pF. For switch characteristics, see Electrical Characteristics.

5.6 Quality Factor Tuning

One has the possibility to tune the quality factor of the antenna using EEPROM bits (word 3).

Coil resistor according CoilxQ[3:0]

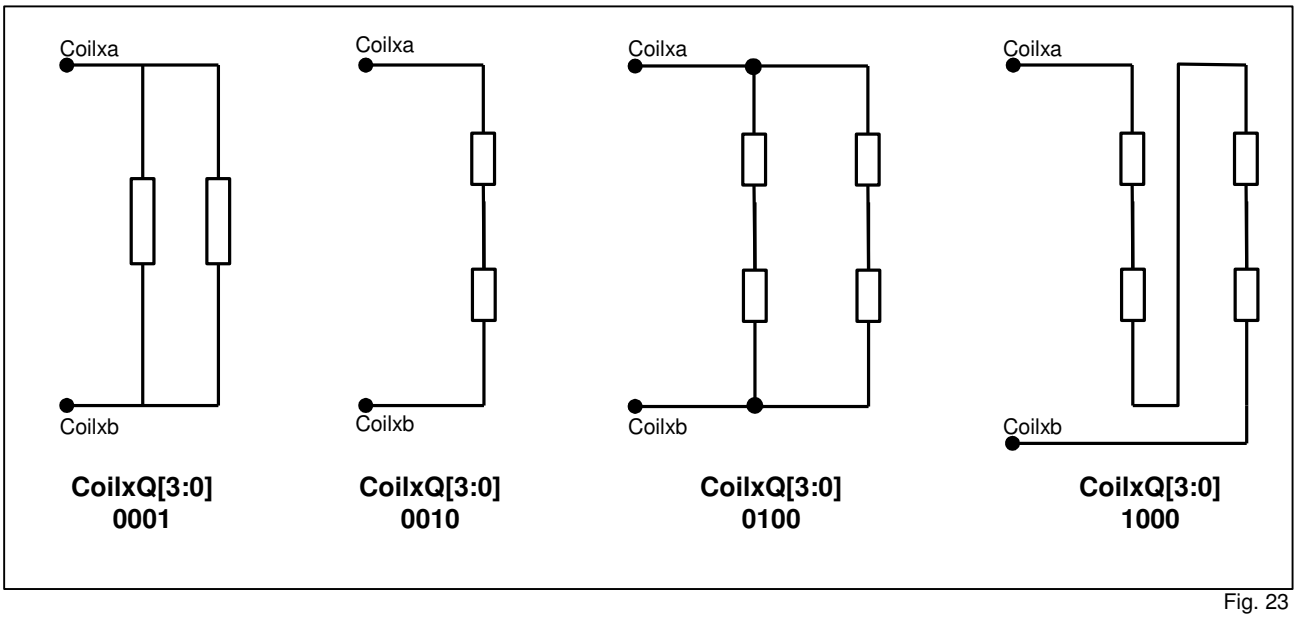


Fig. 23

Coil resistor according Coilx[3:0]

Parameter	Symbol	Conditions	Typ.	Unit
Coil resistor tuning on each antenna	R_{COIL}	**CoilxQ[3:0]** (note6)		
		0001	27	kΩ
		0100	54	kΩ
		0010	105	kΩ
		1000	210	kΩ
		0000	(Note 5)	

Table. 7

Note 5: Open Circuit parasitic resistor (Min 20M Ohms).
Note 6: Other codes are forbidden.

5.7 Coils Input Limiters

Limiters are used on each coil to prevent damages to the circuit due to high voltage (can be several hundred volts in the case of strong field without limiter).

Maximum and minimum voltage is defined by forcing ±10mA on each coil.

Typical I/V Coil characteristics

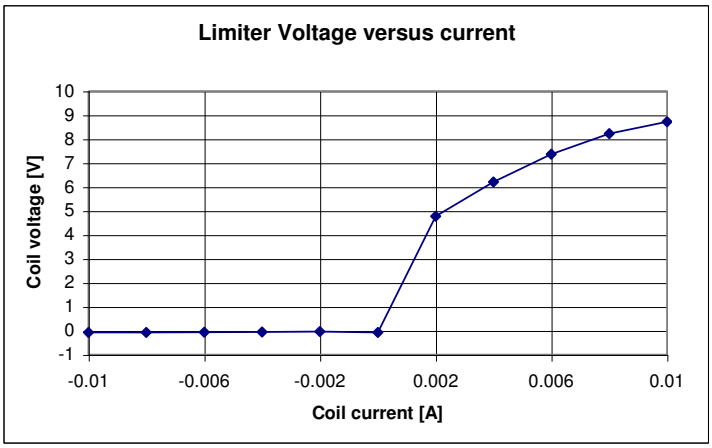


Fig. 24

Coil input signal in strong field

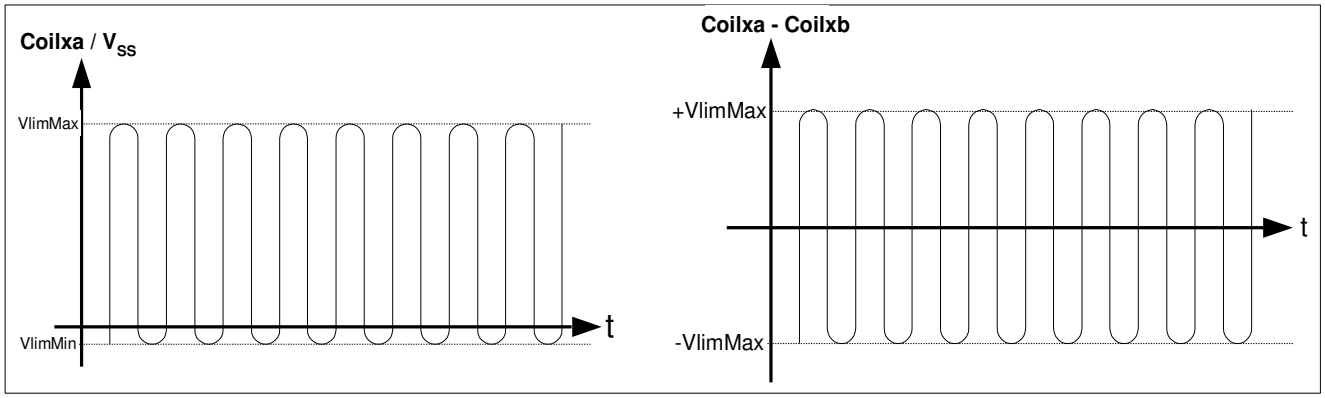


Fig. 25

5.8 **Power Supply Filtering Block:**

The EM4083 Battery is filtered in order to avoid perturbations due to strong voltage drop on V_{Bat} when using microcontroller or other consuming blocks. However, a 100nF capacitor is recommended between V_{Bat} and V_{SS}.

An active diode is used to filter the power supply on V_{FILT} Pad.

VBAT diode symbol

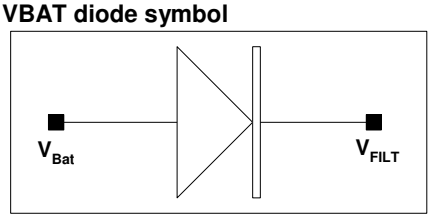


Fig. 26

Note:

This diode is only used for EM4083 power supply Filtering.

It is recommended to use an external capacitor (Cex = 2.2µF) on V_{FILT}.

VBAT diode behavior

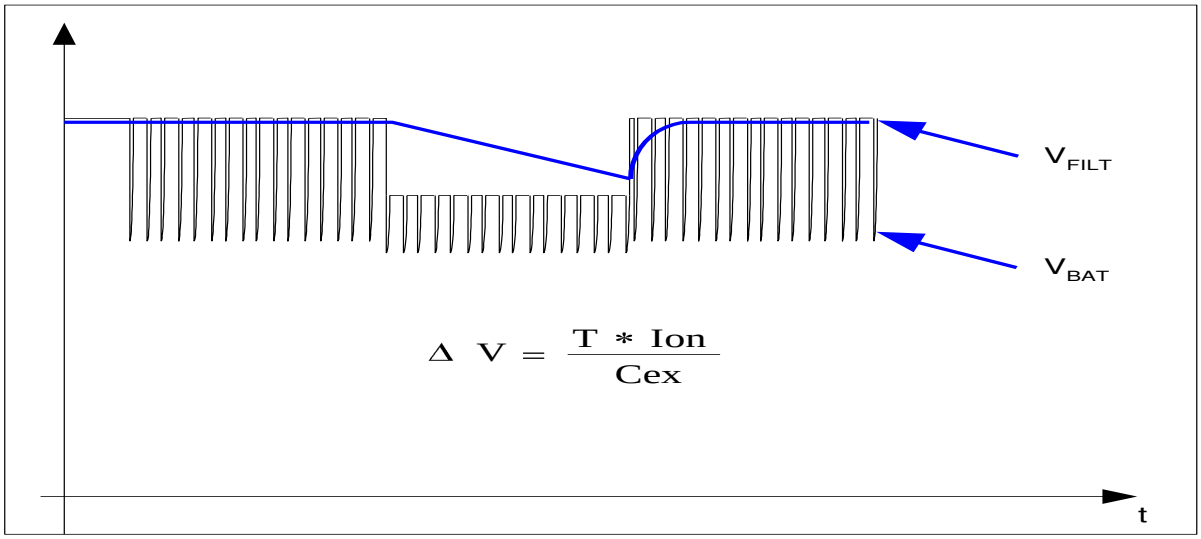


Fig. 27

5.9 Input Impedance Characteristics:

EM4083 input model

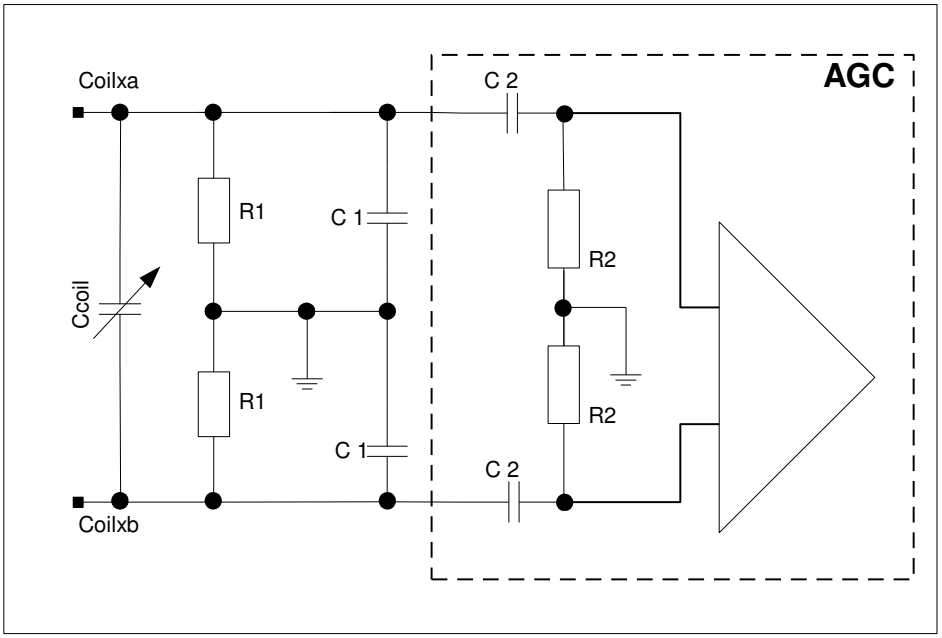


Fig. 28

Coil input characteristics

All the Min, Typ and Max values are guaranteed by design.

Parameters	Symbol	Conditions	Min	Typ	Max	Unit
Input parasitic capacitor	C1	$V_{coil} \leq 10mV_{pp}$ (note 6)	0.45	0.8	1.1	pF
Amplifier decoupling capacitor	C2	$V_{coil} \leq 10mV_{pp}$ (note 6)	5	6	7	pF
Coilx input resistor	R1	$V_{coil} \leq 10mV_{pp}$ (note 6)	10			MΩ
AGC input resistor	R2	$V_{coil} \leq 10mV_{pp}$ Scan period or receive mode : AGC ON (note 6)	10			MΩ

Table. 8

Note 6:

- R2 is equal to 0 (AGC input connected to Vss) in the following situations:
  - AGC is switched OFF (standby period),
  - In receive mode, on the unselected antennas
- Coil1A & Coil1B are in all the configurations floating inputs (receive mode or stand by period).
- C1 value takes into account the TSSOP16 package parasitic capacitor.

5.10 Receive Signal Strength Indicator Function (RSSI)

This function provides a DC voltage that reflects the AC signal on the selected antenna, without disturbing the antenna characteristics.
The voltage present on the RSSI output is directly extract from the AGC feedback loop.

The RSSI Block is used for antennas tuning with the on chip capacitors (during the mass production Test Bench). This function is not intended for distance measurement base on the electro magnetic field strength

Antenna selection for RSSI measurements

Antenna selection is done using a dedicated command which is described in the application note AN415.

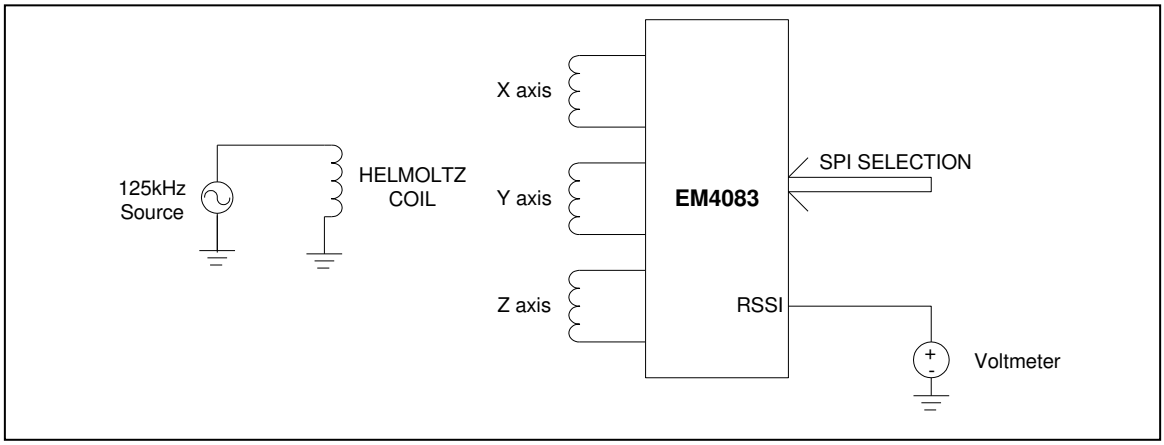


Fig. 29

5.11 EEPROM

EEPROM Mapping

	B[15]	B[14]	B[13]	B[12]	B[11]	B[10]	B[9]	B[8]	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
Word 0	X	**CC [6]**	**CC [5]**	**CC [4]**	**CC [3]**	**CC [2]**	**CC [1]**	**CC [0]**	X	X	X	X	X	X	X	X
Word 1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Word 2	X	Coil3 [0]	Coil3 [1]	Coil3 [2]	Coil3 [3]	Coil3 [4]	Coil2 [0]	Coil2 [1]	Coil2 [2]	Coil2 [3]	Coil2 [4]	Coil1 [0]	Coil1 [1]	Coil1 [2]	Coil1 [3]	Coil1 [4]
Word 3	0	1	0	X	coil3 Q [0]	coil3 Q [1]	coil3 Q [2]	coil3 Q [3]	Coil2 Q [0]	Coil2 Q [1]	Coil2 Q [2]	Coil2 Q [3]	Coil1 Q [0]	Coil1 Q [1]	Coil1 Q [2]	Coil1 Q [3]
Word 4	WKb [6]	WKb [5]	WKb [4]	WKb [3]	WKb [2]	WKb [1]	WKb [0]	Level [2]	Level [1]	Level [0]	ASK / ID	Ratio [2]	Ratio [1]	Ratio [0]	X	ASC
Word 5	User memory (27 x16 bits)															

Word 30																
Word 31																

	B[15]	B[14]	B[13]	B[12]	B[11]	B[10]	B[9]	B[8]	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
Word 0	X	Customer code dedicated to a specific customer							X	X	X	X	X	X	X	X
Word 1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Word 2	X	Tuning antenna3 Resonant Capacitor					Tuning antenna2 Resonant Capacitor					Tuning antenna1 Resonant Capacitor				
Word 3	0	1	0	X	Tuning antenna3 QFactor				Tuning antenna2 QFactor				Tuning antenna1 QFactor			
Word 4	Programmable Wakeup Byte							Sensitivity reduction in receive mode	ASK / ID	Scan Ratio				X	ASC	
Word 5	User memory (27 x16 bits)															

Word 30																
Word 31																

Notes :

1. if ASK/ID =**"0"** ***Wakeup byte*** is used for the wakeup header (7 bits programmable).
   if ASK/ID =**"1"** ***Customer code*** is used for the wakeup header (fixed code).

2. if ASC =**"0"** Automatic Sensitivity Change (ASC) function is OFF.
   if ASC =**"1"** Automatic Sensitivity Change (ASC) function is ON.

3. X not used

4. Words 0 & 1 are factory locked and are accessible as read only.

5. Bits 13 to 15 of word3 must always be written as indicated.

5.12 Serial Peripheral Interface (SPI)

The EM4083 contains a SPI (**S**erial **P**eripheral **I**nterface) compatible serial interface. This Interface is a full duplex synchronous protocol with data shifted MSB first. The EM4083 SPI interface is a slave device and it is connected to a master driver by 4 wires (SS_N, SI, SO, SCK).

The SS_N input pin enables SPI interface of the EM4083.

Serial Interface Top diagram

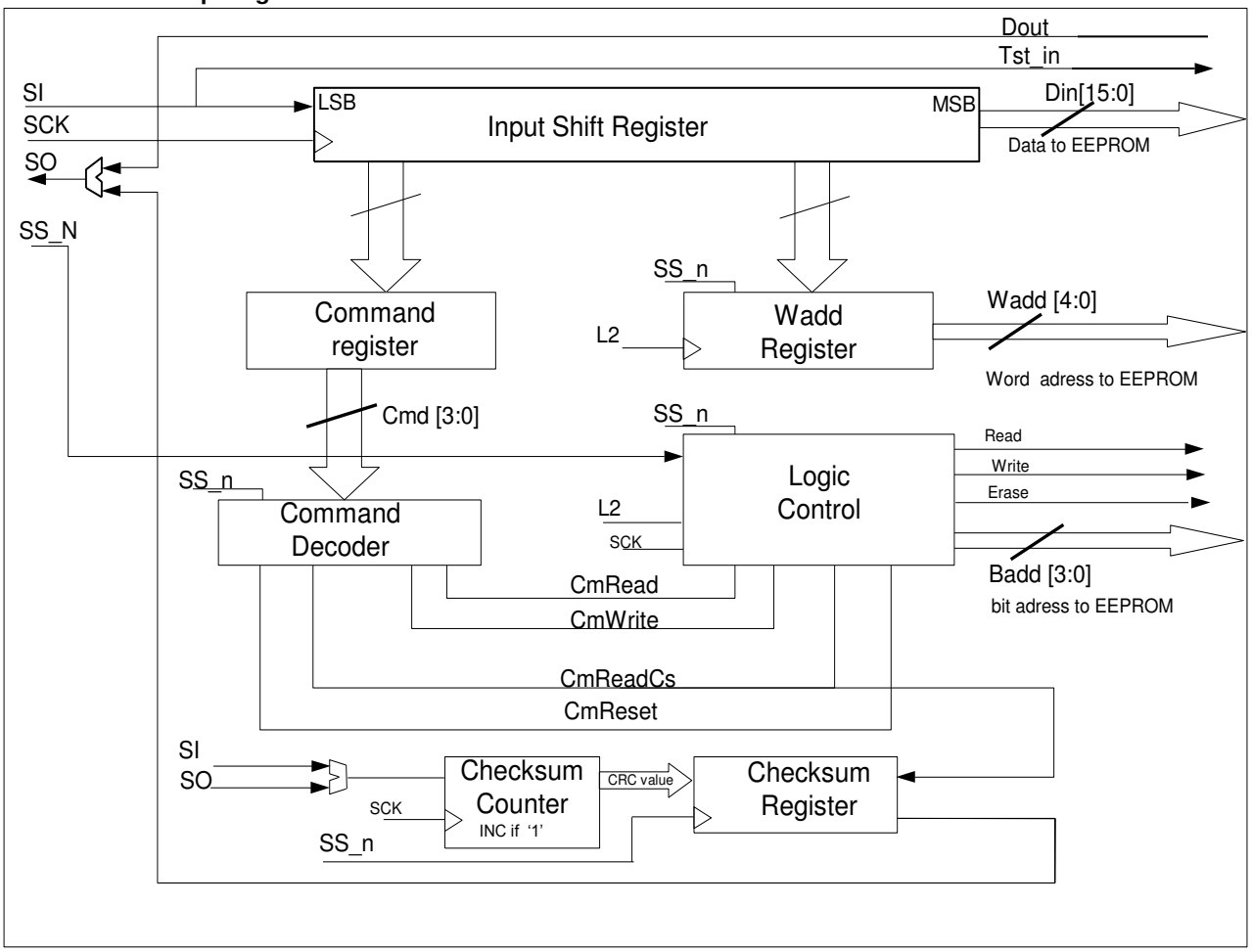


Fig. 30

SPI Pin Description

Pin	IN/OUT	Description
SCK	I	Serial clocks
SS_N	I	Chip Enable with
SI	I	Slave Input. Slave receives data from this pin
SO	O	Slave Output. Slave sends data to this pin.

Table. 9

Using the SPI, it is possible to set the chip in 4 different modes.

SPI Modes Description

Command	Code	Description
READ	1010	Read operation of EEPROM.
WRITE	1100	Writing operation of EEPROM.
RESET	0110	EM4083 software reset
READCS	1011	Read operation of Checksum register

Table.10

5.12.1 **Read Mode**

In this mode, the whole EEPROM can be accessed for read operations.
The read operation starts by pulling down the SS_n line.

The master transfers the command (Cmd[3:0]) and the address (Wadd[4:0]) on the falling clock edge (SCK) into the serial input shift register through SO pin. SO pin is driven low by EM4083.

The read mode is identified by a READ COMMAND (Cmd[3:0] = 1010). The address bits are sampled into the Wadd register (after 9th negative SCK edge). Then the master has to send 7 additional dummy bits to round up number of send bits to 16. Dummy bits should be zero.

When all 16 bits are transferred (4 bits command, 5 bits address, 7 dummy bits) slave starts to send requested data from address Wadd from internal EEPROM. The slave transfers these data bits to SO pin of SPI. The master drives SI pin low. The data are repeatedly shifted out until the SS_n signal gets high again. When all 16 data bits are send master stops clocks (SCK) with last falling edge and de-asserts SS_N high. At this time the serial interface will go in reset state.

For detailed timing see EEPROM Read & Write Access chapter.

SPI Read Operation

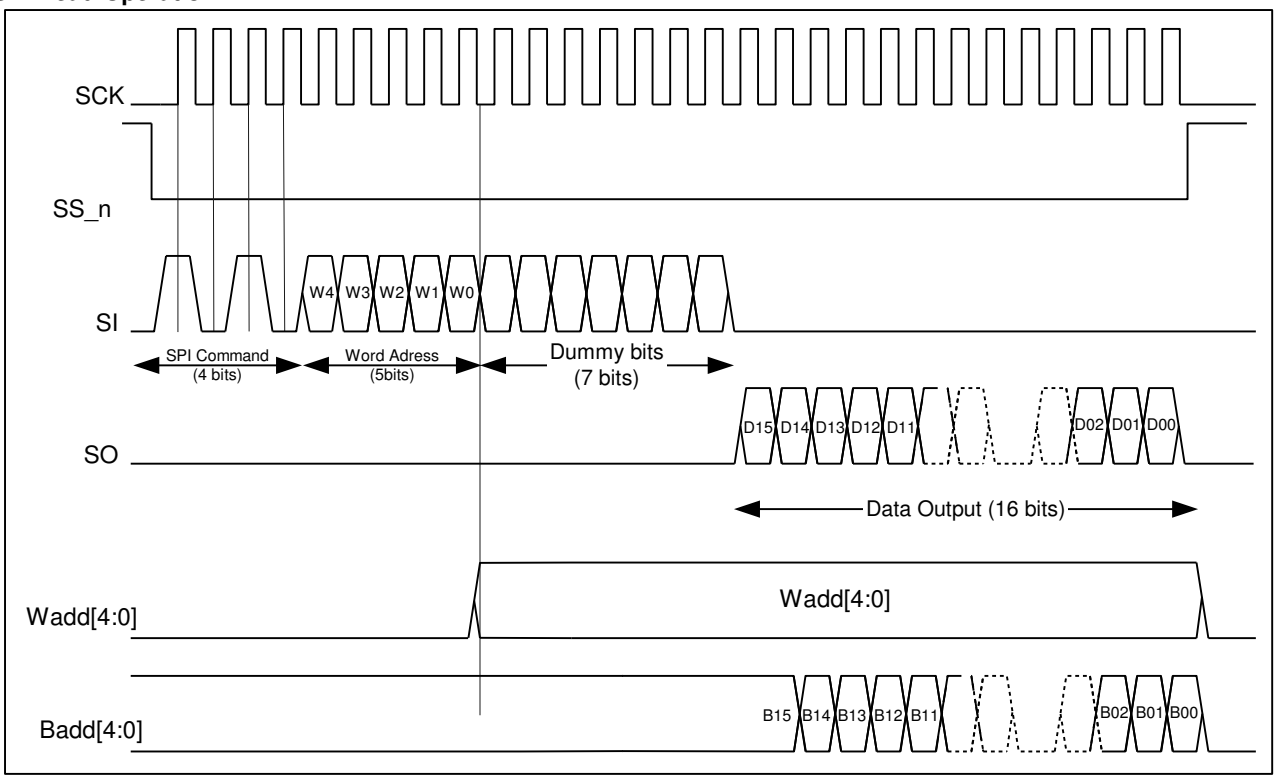


Fig. 31

5.12.2 **Write Mode**

In this mode, the whole EEPROM can be accessed for write operations.

The write operation starts by pulling low the SS_N line.The write mode is identified by a WRITE COMMAND (Cmd[3:0] = 1100). The command (Cmd[3:0]), the address (Wadd[4:0]) and the Data [15:0]bits are transferred on the negative clock edge (SCK) into the serial input shift register.

The address bits are latched into the Wadd latch register (after 9th negative Clk edge). Then the master has to send other 7 dummy bits to round up number of send bits to 16. Dummy bits should be zero. After command master transfers 16 bits of data which will be stored to EEPROM on appropriate address.

When 16 bits of data bits are serially shifted in, the EEPROM Write sequence starts. At the next falling edge erase signal is asserted to erase requested word. After erase and delay time between write and erase, write signal is asserted and writing is in process. After write and delay time occur status bit '1' is sent out on line SO. This signifies to the master that write sequence was completed and the master can spot clock (SCK) with last falling edge and de-asserts SS_N high. At this time the serial interface will go in reset state.

The words 0-3 are locked and they are not accessible for writing. When an attempt to write these addresses appears the status bit 1 is sent out immediately and no write or erase operation is done.

For detailed timing of writing sequence see EEPROM Read & Write Access chapter.

SPI Write Operation

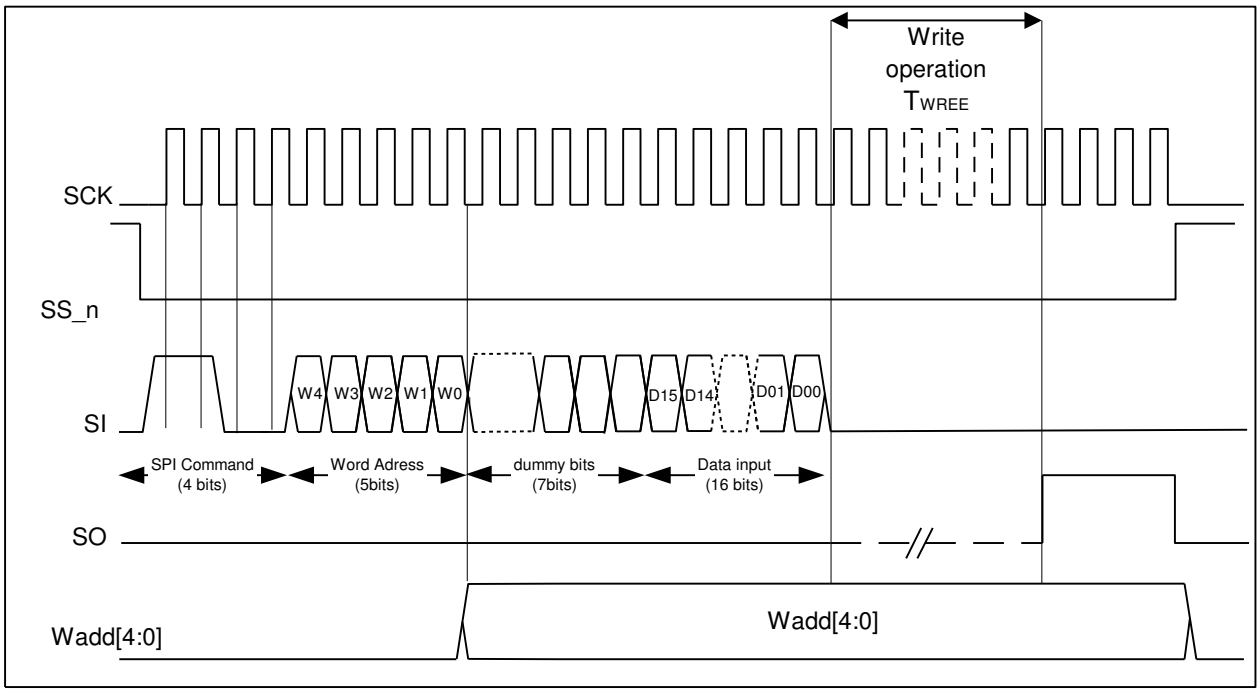


Fig. 32

Note:

The master has to leave SS_N line low during whole write sequence. The de-asserting causes reset of SPI and failure of write. The master should provide clocks during whole write sequence and when slave send '1' on SO pin write sequence is completed.

Warning: One has to check that the voltage V_{FILT} is higher than V_{EE} min before writing the EEPROM.

5.12.3 **Reset Mode**

The reset mode command (Cmd[3:0] = 0110) is used to put the EM4083 in a reset mode.
Once, the EM4083 is in reset state, it will stay in this mode until SS_N = “0”.

SPI reset mode

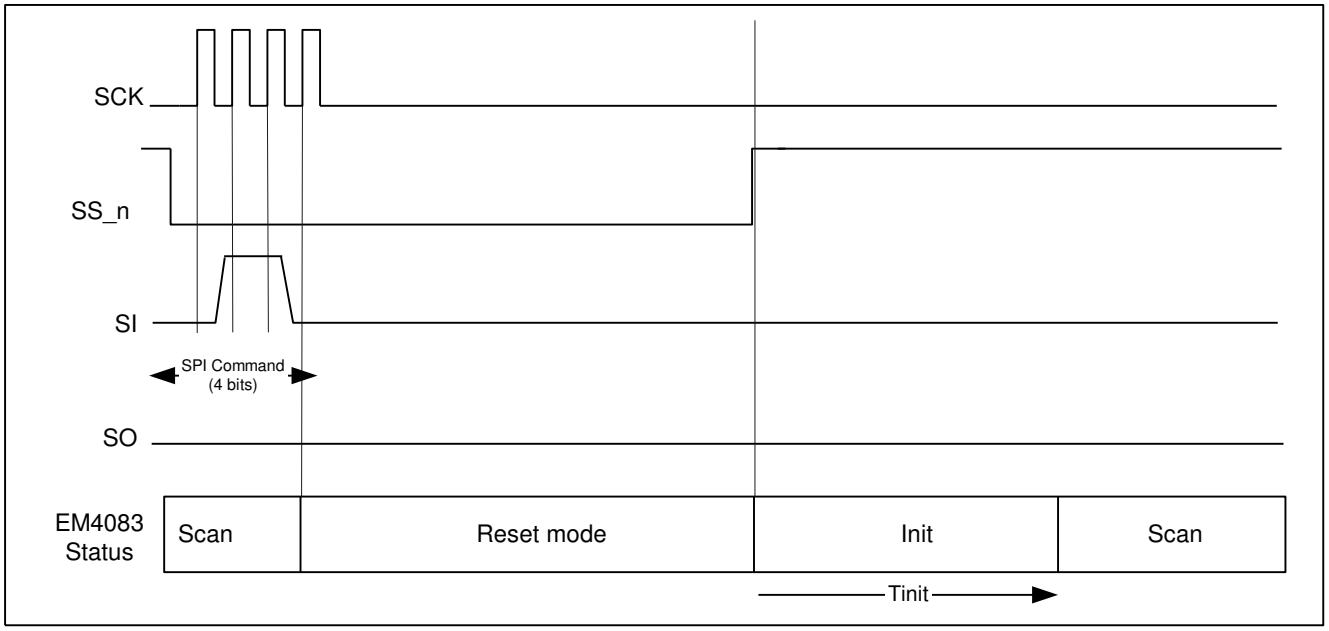


Fig. 33

5.12.4 **ReadCs Mode**

A checksum is generated throughout the whole data transfer in order to enable the master driver to check for correct data transfer. This checksum is based on a modulo 8 counter. On each positive clock edge the counter increments by 1 if the SO or SI signal is ´1´. The checksum is saved at the end of data transfer in a 3-bit register accessible on ReadCs mode only by the serial interface. The modulo 8 is realised by a free running cyclic 3 bit counter.

The value stored into a 3-bit Checksum Register corresponds to the counter value at the time at the end of the data transfer.

Whenever the interface is not active (SS_N = ‘1’) the whole interface is in reset state, except the Checksum register. All registers are cleared when SS_N = ‘1’ and the interface is ready to receive a new command.

SPI Checksum

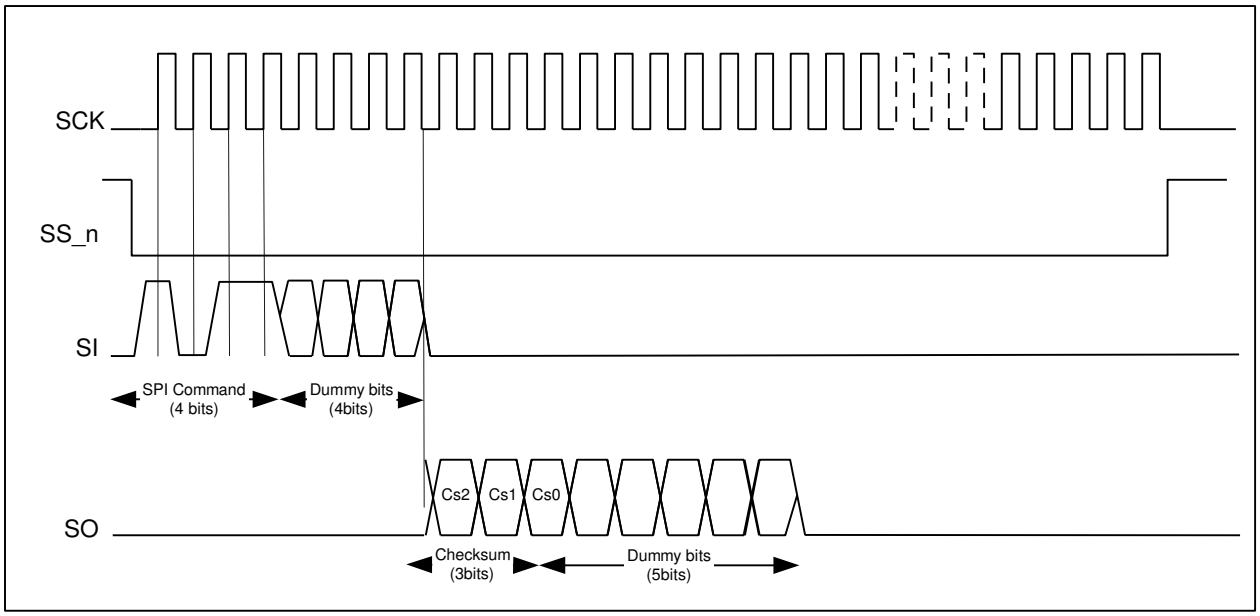


Fig. 34

5.12.5 Checksum Function:

Example of Checksum on read

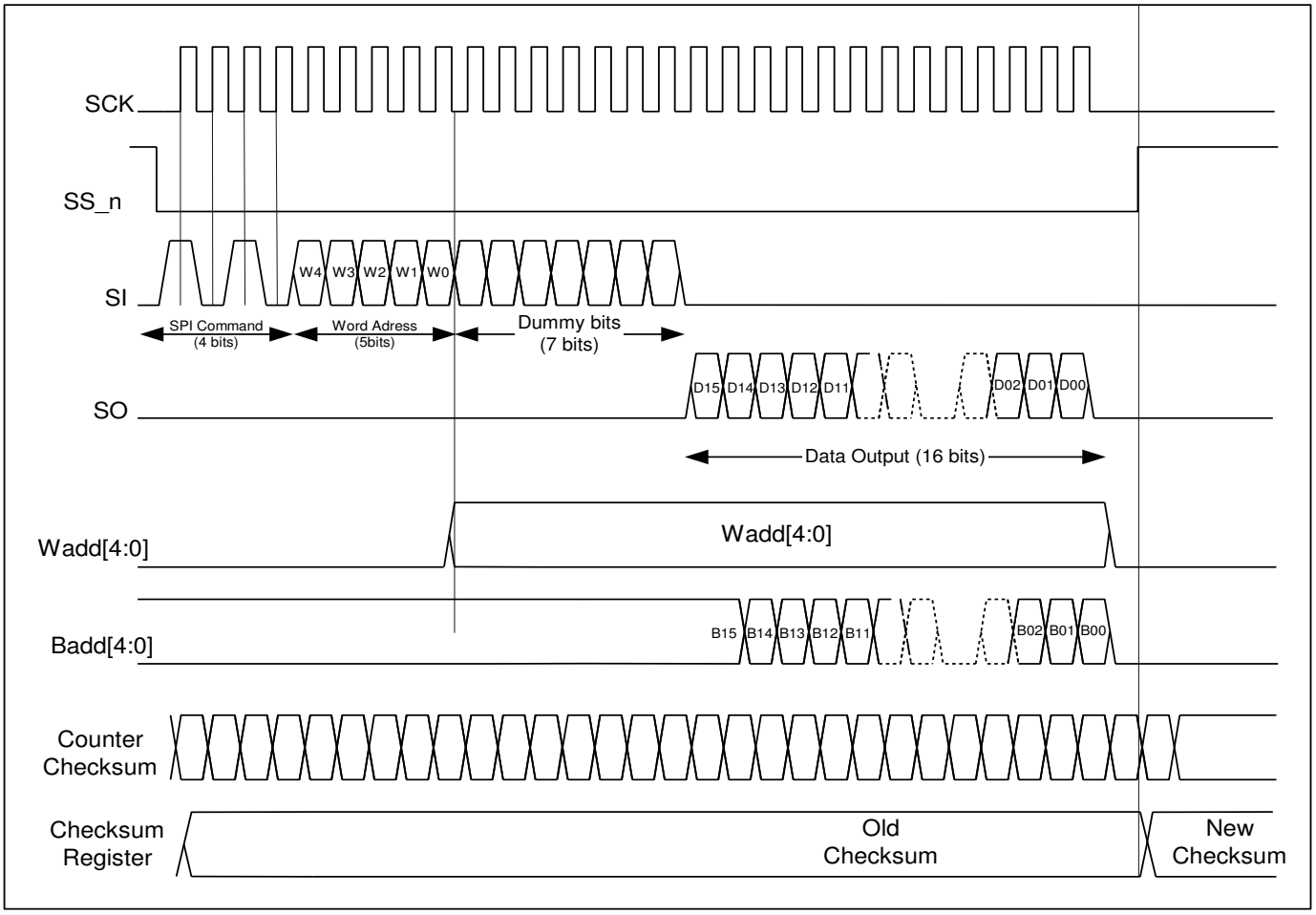


Fig. 35

It allows the previous data transfer to be checked for correctness.

Read mode : Checksum = modulo 8 of (Sum of ´1´)
Sum of ´1´s =(Sum of Command bits == '1' + Sum of address bits == ´1´ + Sum of data bits == ´1´*)*

Write mode : Checksum = modulo 8 of (Sum of ´1´s)
Sum of ´1´s =(Sum of Command bits == '1' + Sum of address bits == ´1´ + Sum of data bits == ´1´*)*

Reset mode :
There is no checksum, in this mode.
The checksum register is in reset state.

ReadCs mode : Checksum = modulo 8 of (Sum of ´1´s)
Sum of ´1´s =(Sum of Command bits == '1' +Sum of checksum bits == ´1´*)*

Checksum Register - RegCheckSum
Read only, it contains the 3-bit number of detected ones during the previous data transfer.
The updated checksum value is stored at the end of each data transfer.

RegCheckSum

Bit 2	Bit 1	Bit 0
Csum[2]	Csum[1]	Csum[0]

The register (Read only) is cleared on power up or after a reset command.

5.12.6 EEPROM READ & WRITE ACCESS

The EEPROM is a system with parallel write operation and serial, sense-amplifier operated, read operation. The system includes the EEPROM matrix, the charge pump and all peripheral circuits.
The EM4083 EEPROM is made of 512 bits, organised in 32 words of 16 bits. The read operation is performed serially, using one sense-amplifier. The sense-amplifier ensures proper read operation even with very noisy power supply.

Read operation:

Once, the EM4083 is in the read mode (CmRead = 1 after 4th negative edge of CLK) and the Wadd[4:0] is latched in the Wadd register (9th negative edge), the Wadd is connected to EEPROM address bus and Badd[4:0] is set to 15 because data will be sent out from EEPROM MSB first. At the next negative edge, when Wadd[4:0] is stable, the read signal is set to 1. The Badd[4:0] is then decremented on each negative SCLK edge and appropriate data are send out through D_{out} / D_{in} pin.

Notes for the read operation:
- Wadd[5:0] has to be stable during the read operation
- Badd[4:0] can change during the read operation, the delay between the change of badd and the validity of the new D_{out} value is Tdacct.
- In order to read a new word, a complete read sequence has to be restarted.

6. Pin description of TSSOP-16 package

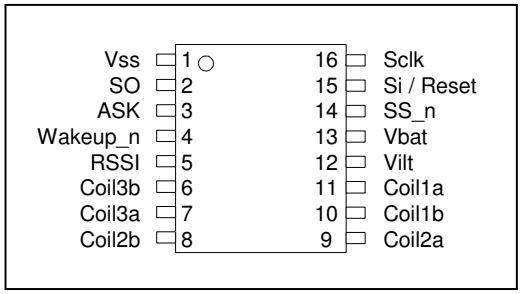
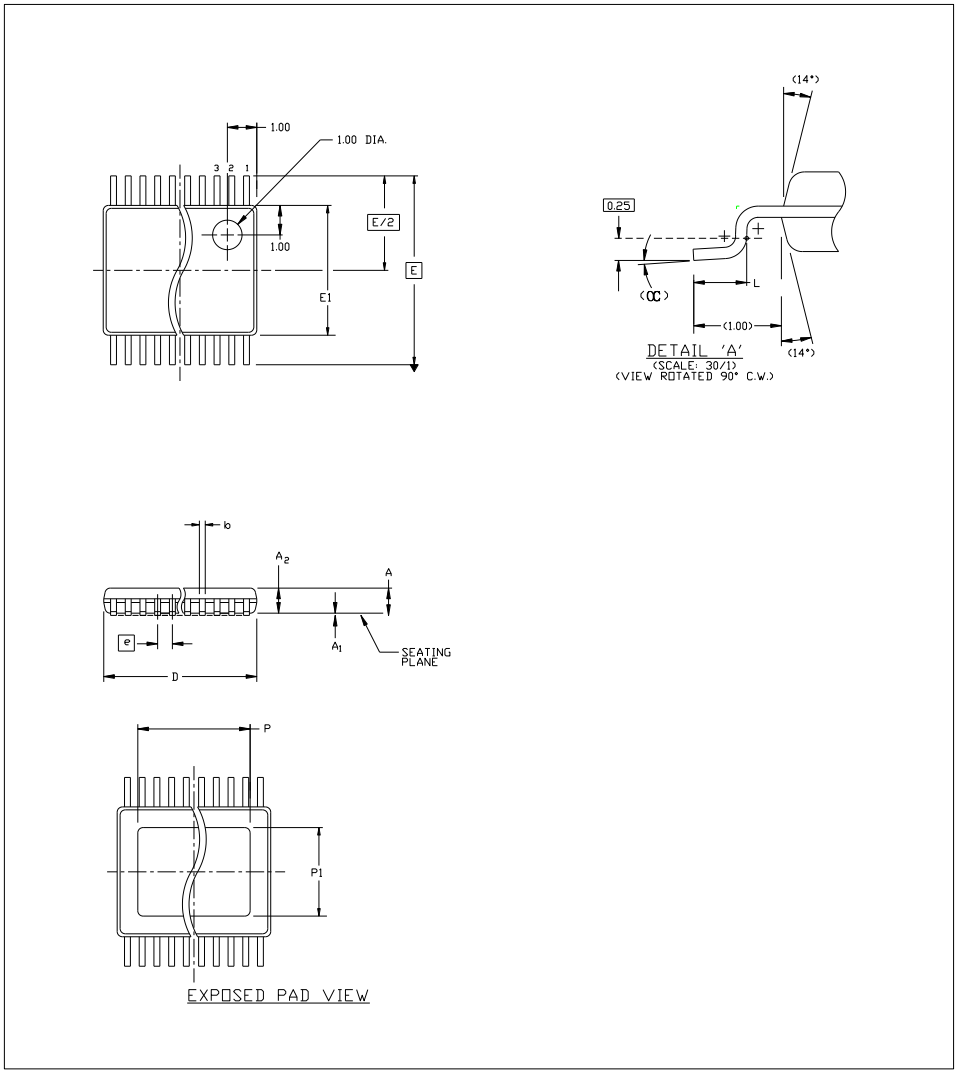


Fig.36

Pin N°	Name	I/O	Description	Coupling
1	Vss	ANA	Digital Negative DC supply	
2	SO	DIGITAL Output	SS_n = 0 → SO = Serial Interface Output SS_n = 1 → SO = Bitclock (Data decoder)	
3	ASK	DIGITAL Output	ASK Data Output	
4	Wakeup_n	I/Open drain	Wakeup signal	Bi-directional Internal Pull-Up 30kΩ
5	RSSI	ANA	Field strength monitoring	Serial resistor 1KΩ
6 7	Coil3b Coil3a	ANA ANA	Antenna n°3	AC
8 9	Coil2b Coil2a	ANA ANA	Antenna n°2	AC
10 11	Coil1b Coil1a	ANA ANA	Antenna n°1	AC
12	V_{FILT}	ANA	Positive DC rectified voltage	
13	V_{Bat}	ANA	Positive DC supply battery	
14	SS_n	DIGITAL input	Serial Interface selection	Internal Pull-Up 100kΩ
15	SI / RESET	DIGITAL Input	SS_n = 0 → SI = Serial Interface Input SS_n = 1 → SI = Reset pin	Internal Pull-down 100kΩ
16	SCLK	DIGITAL input	Serial Interface clock	Internal Pull-down 100kΩ

7. Package Outline



Symbol	Min (mm)	Nom (mm)	Max (mm)
A			1.10
A1	0.05	0.1	0.15
A2	0.85	0.90	0.95
D		5.00	
E		6.40	
E1	4.30	4.40	4.50
e		0.65	
L	0.5	0.6	0.7
∝	0°	5°	8°
X	2.16	2.36	2.54
P			3.00
P1			3.00

8. Ordering Information

This device is available in TSSOP-16 package.

Please order the following part number:

Part Number	Delivery Form
EM4083TP16A-007+	Stick, 96 pieces
EM4083TP16B-007+	Tap & reel, 2500 pieces