Digital Audio Delay

■**Package**

■ **General Description**

The NJU26904 offers digital audio delay.

The NJU26904 has internal delay memory. Delay function can adjust output time of a six-channel signal.

This delay functions are suitable for delay time adjustment such as Audio products and time alignment such as Car Audio.

NJU26904V-C2

■ **FEATURES**

- 6-channel Digital Audio Delay

  Delay Time 84msec for monaural channel, 42msec for stereo channel at Fs=96kHz

  Delay Time 169msec for monaural channel, 85msec for stereo channel at Fs=48kHz

  Delay Time 254msec for monaural channel, 127msec for stereo channel at Fs=32kHz

- Delay data width is 24 bits.

  Digital Audio Format: I^2S 24bit, Left-Justified, Right-Justified, BCK: 32/64fs

- Adjustable Delay Time with 1sample units for 8,121 samples at maximum.

- Selectable input sources for each channel output freely.

- To make long delay time, the NJU26904 can be connected serially.

- Non-Audio Format is possible.

- Hardware

- Maximum System Clock Frequency : 12.288MHz Max. built-in PLL Circuit
- Digital Audio Interface : 3 Input ports / 3 Output ports
- Digital Audio Format : I^2S 24bit, Left- Justified, Right-Justified, BCK : 32/64fs
- Master / Slave Mode
    - Master Mode, MCK : 384fs @32kHz, 256fs @48kHz
- Host Interface : I^2C bus (Fast-mode/400kbps)
- Power Supply : 3.3V
- Input terminal : 5V Input tolerant
- Package : SSOP24-C2 (Pb-Free)

NJU26904

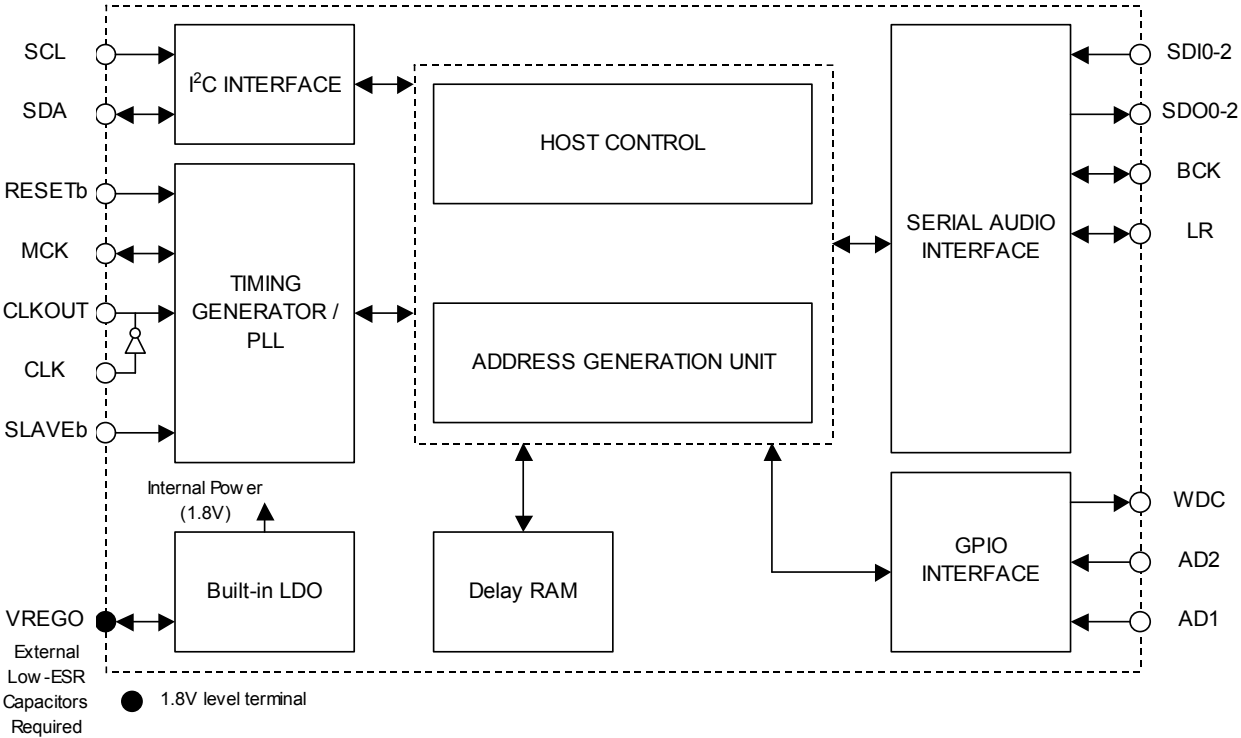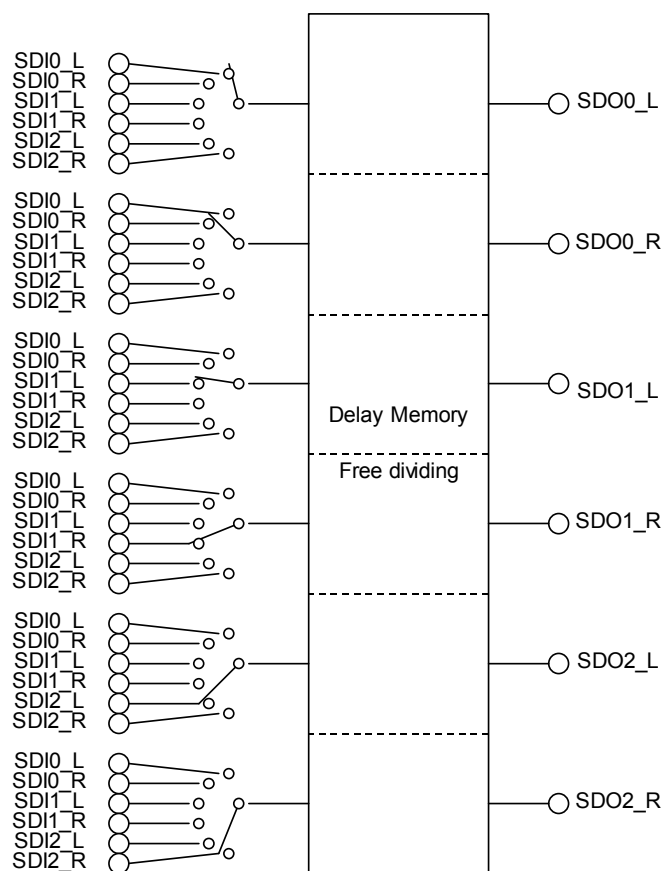**■ Function Block Diagram**

Fig. 1   NJU26904 Block Diagram

■ DSP Block Diagram

Fig. 2   NJU26904 Function Diagram

NJU26904

■ **Pin Configuration**

RESETb	1	24	TEST
LR	2	23	SCL
BCK	3	22	SDA
SDI2	4	21	SDO2
SDI1	5	20	SDO1
SDI0	6	19	SDO0
MCK	7	18	WDC
VDD	8	17	AD2
VSS	9	16	AD1
STBYb	10	15	SLAVEb
VSS	11	14	CLK
VREGO	12	13	CLKOUT

NJU26904

SSOP24-C2
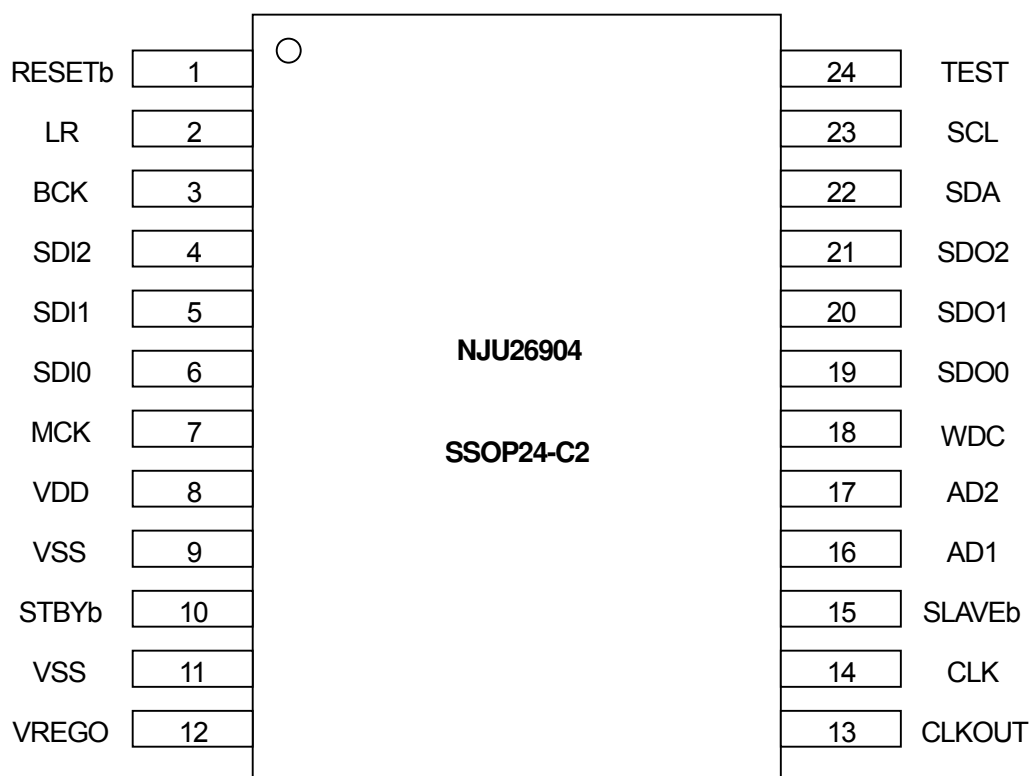
Fig. 3   NJU26904 Pin Configuration

■ **Pin Description**

Table 1   Pin Description

No.	Symbol	I/O	Description	No.	Symbol	I/O	Description
1	RESETb	I	RESET (active Low)	13	CLKOUT	O	OSC Output
2	LR	I/O	LR Clock	14	CLK	I	OSC Clock Input
3	BCK	I/O	Bit Clock	15	SLAVEb	I	Slave select
4	SDI2	I	Audio Data Input 2 L/R	16	AD1	I	I^2C Address 1
5	SDI1	I	Audio Data Input 1 L/R	17	AD2	I	I^2C Address 2
6	SDI0	I	Audio Data Input 0 L/R	18	WDC	OD	Clock for Watch Dog Timer
7	MCK	I/O	Master Clock	19	SDO0	O	Audio Data Output 0 L/R
8	VDD	-	Power Supply +3.3V	20	SDO1	O	Audio Data Output 1 L/R
9	VSS	-	GND	21	SDO2	O	Audio Data Output 2 L/R
10	STBYb	I	For TEST (Connected to VDD)	22	SDA	OD	I^2C I/O
11	VSS	-	GND	23	SCL	I	I^2C Clock
12	VREGO	PI	Built-in Power Supply Bypass	24	TEST	I	For TEST(Connected to VSS)

*   I : Input, O : Output, I/O: Bi-directional, OD: Open-Drain I/O, PI: Power Supply Bypass

AD1 (No.16) pin and AD2 (No.17) pin are input pins. WDC (No.18) pin is open-drain pin with pull-up resistance. However, these pins operate as bi-directional pins. No.11pin and No.12pin connect with V_{DD} or V_{SS} through 3.3kΩ resistance. No.18pin do not connect or connect with V_{DD} through 3.3kΩ resistance when unused.

VREGO (No.12) pin is a built-in power supply bypass pin. Connect low-ESR capacitor of 4.7uF and 0.01uF in parallel between VSS (No.11) pin. A built-in power supply is used only for NJU26904 operation. Be not short-circuited of this pin. Do not take out the current, and connect other power supplies.

■ Absolute Maximum Ratings

Table 2   Absolute Maximum Ratings   (V_{SS}=0V=GND, Ta=25℃)

Parameter		Symbol	Rating	Units
Supply Voltage *		V_{DD}	-0.3 to 4.2	V
Supply Voltage Bypass *		V_{REGO}	-0.3 to 2.3	V
Pin Voltage *	In	$V_{x(IN)}$	-0.3 to 5.5 ($V_{DD} \geq$ 3.0V) -0.3 to 4.2 ($V_{DD} <$ 3.0V)	V
	I/O, OD	$V_{x(I/O)}$, $V_{x(OD)}$		
	Out	$V_{x(OUT)}$	-0.3 to 4.2	
	CLK	$V_{x(CLK)}$	-0.3 to 4.2	
	CLKOUT	$V_{x(CLKOUT)}$		
Power Dissipation		P_D	565	mW
Operating Voltage		T_{OPR}	-40 to 85	℃
Storage Temperature		T_{STR}	-40 to 125	℃

* The LSI must be used inside of the "Absolute maximum ratings". Otherwise, a stress may cause permanent damage to the LSI.

* V_{DD} : 8 pin
* V_{REGO} : 12 pin
* $V_{x(IN)}$: 1, 4, 5, 6, 10, 15, 23, 24 pin
* $V_{x(OD)}$: 22 pin
* $V_{x(I/O)}$: 2, 3, 7, 16, 17, 18 pin
* $V_{x(OUT)}$: 19, 20, 21 pin
* $V_{x(CLK)}$: 14 pin
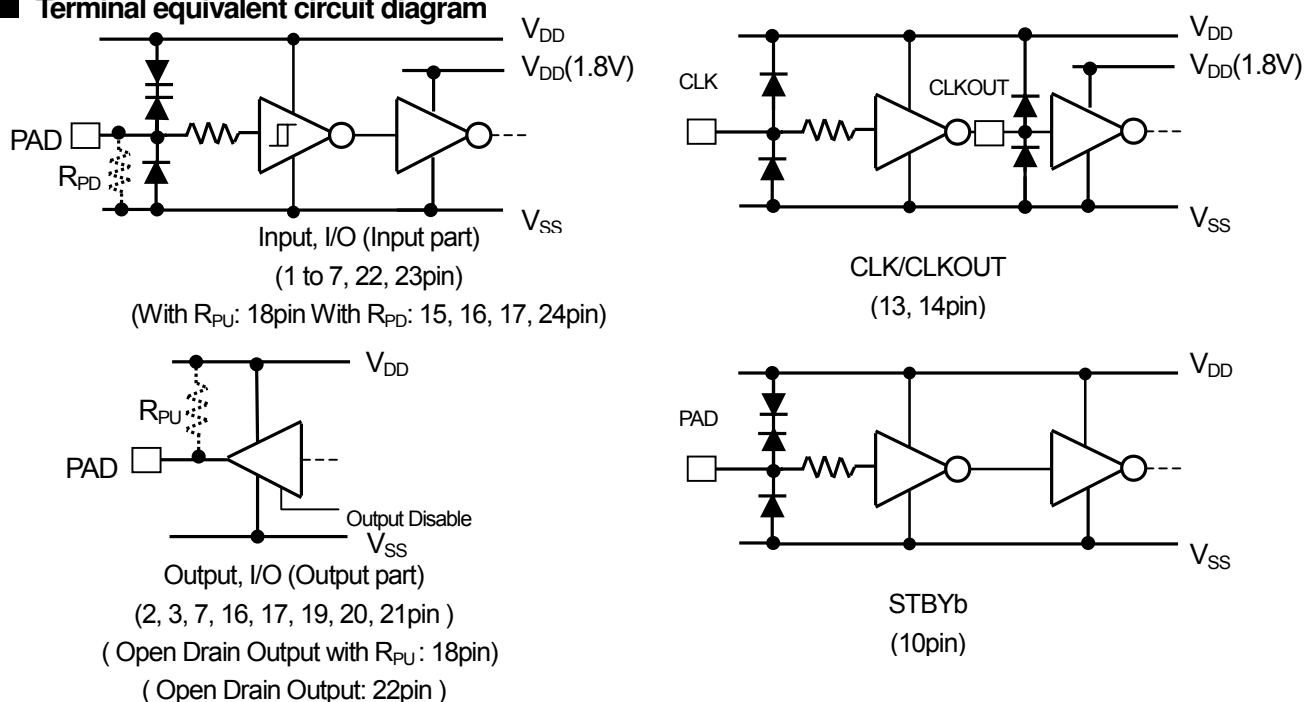* $V_{x(CLKOUT)}$: 13 pin

■ Terminal equivalent circuit diagram

Input, I/O (Input part)
(1 to 7, 22, 23pin)
(With R_{PU}: 18pin With R_{PD}: 15, 16, 17, 24pin)

CLK/CLKOUT
(13, 14pin)

Output, I/O (Output part)
(2, 3, 7, 16, 17, 19, 20, 21pin)
(Open Drain Output with R_{PU} : 18pin)
(Open Drain Output: 22pin)

STBYb
(10pin)

Fig.4   NJU26904 Terminal equivalent circuit diagram

NJU26904

■ Electric Characteristics

Table 3   Electric Characteristics   (V_{DD}=3.3V, f_{OSC}=12.288MHz, Ta=25°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Operating Voltage [1]	V_{DD}	V_{DD} pin	3.0	3.3	3.6	V
Operating Current	I_{DD}	At no load	-	20	35	mA
High Level Input Voltage	V_{IH}		V_{DD} x 0.7	-	V_{DD} [2]	
Low Level Input Voltage	V_{IL}		0	-	V_{DD} x 0.3	
High Level Output Voltage [3]	V_{OH}	(I_{OH}= -1mA)	V_{DD} x 0.8	-	V_{DD}	V
Low Level Output Voltage	V_{OL}	(I_{OL}= 1mA)	0	-	V_{DD} x 0.2	
Leakage Current [4]	I_{IN}	V_{IN} = V_{SS} to V_{DD}	-10	-	10	µA
	$I_{IN(PU)}$		-120	-	10	
	$I_{IN(PD)}$		-10	-	120	
Clock Frequency	f_{OSC}		10	12.288	13	MHz
Clock Jitter [5]	$f_{JIT(CC)}$	CLK, MCK [6]	0	-	3.0	ns
Clock Duty Cycle	r_{EC}		45	50	55	%

   [1]   Supply voltage must be within recommended operating voltage. Furthermore supplying power voltage must be linear, quick and smooth to prevent abnormal operation. Once the power supply is set up, supply voltage must be kept within the operating voltage range. After setting up the power supply, even if the supply voltage dropped off and recovered to normal range, reset function and the all following operations can not be guaranteed. After using this DSP, power supply must be dropped to V_{SS} level.

   [2]   Input pin, Output pin and Open-Drain input/output pin are +5.0V tolerant except CLK input pin.

   [3]   Except No.18pin: WDC (Open-Drain output) and No.22: SDA (Open-Drain input/output).

   [4] $I_{IN(PU)}$: 18pin, $I_{IN(PD)}$: 15, 16, 17, 24 pin

   [5]   Clock Jitter shows Cycle-to-cycle period jitter (JEDEC JESD65).

   [6]   Provide clock frequency for f_{OSC} spec. NJU26904 needs clock frequency 12.288MHz when sampling rate is 48kHz.

1. Power Supply, Input/Output terminal, Clock, Reset

1.1 Power Supply

The NJU26904 has a power supply V_{DD}. To setup good power supply condition, the decoupling capacitors should be implemented at the all power supply terminals.

The NJU26904 include a built-in power supply (LDO) for internal logic. A built-in power supply generates 1.8V (-10% to +10%). VREGO (No.12) pin is a built-in power supply bypass pin. Connect low-ESR capacitor of 4.7uF and 0.01uF in parallel between VSS (No.11) pin.
A built-in power supply is used only for NJU26904 operation. Be not short-circuited of this pin. Do not take out the current, and connect other power supplies.

1.2 Input/Output terminal

It restricts, when the input terminals (AD1, AD2, RESETb, SDI0, SDI1, SDI2, STBYb, SLAVEb, SCL, TEST pins), the input/output terminals (LR, BCK, MCK pins) and the bi-directional Open-drain terminal (SDA pin) of NJU26904, and V_{DD} are supplied on regular voltage (V_{DD}=3.3V), and it becomes +5V Input tolerant.

1.3 Clock

The NJU26904 CLK pin requires the system clock. The system clock is usually 12.288MHz into CLK pin.

It is possible to be generated the system clock by connecting a crystal oscillator between CLK and CLKOUT. CLK/CLKOUT pins are not 5V tolerant, so check the voltage level of these pins.
When SLAVEb pin is fixed on Low level, NJU26904 supplies the system clock from MCK pin. Fix the clock input pin not used to Low level because either the CLK pin or the MCK pin is supplied in NJU26904.

The frequency divider for Master mode matched to the clock 256 times of Fs is installed in NJU26904. When clock except 256 times of Fs is used by Master mode, be careful to use because a dividing frequency of Master mode changes. Please check enough and decide parameter.

1.4   Reset

To initialize the NJU26904, RESETb pin should be set Low level during some period. After some period of Low level, RESETb pin should be High level. This procedure starts the initialization of the NJU26904. After the power supply and the oscillation of the NJU26904 becomes stable, RESETb pin must be kept Low-level more than t_{RESETb} period. (Fig.5)

After RESETb pin level goes to "High" (after reset release), a setup of the internal hardware of a Serial Host Interface completes NJU26904 within 10msec. Then, it will be in the state which can communicate.
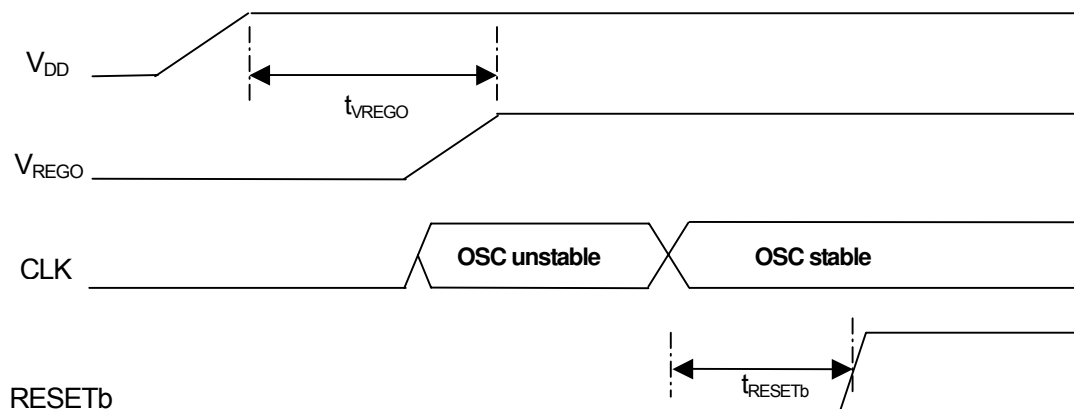
Fig.5   Reset Timing

Table 4   Reset Time

Symbol	Time
t_{VREGO}	$\geq$ 10msec
t_{RESETb}	$\geq$ 1.0msec

Note :

Don't stop the supply of a clock while operating. NJU26904 installs PLL circuit internally. If the supply of a clock is stopped, PLL circuit cannot be sent a clock to the inside and NJU26904 does not operate normally.

If supply of a clock is stopped or the NJU26904 is reset again, putting a normal clock into CLK terminal, the period RESETb terminal of t_{RESETb} is kept "Low" level.(Table 4) Next, the NJU26904 is reset. Then redo from initial setting.

2. Digital Audio Clock

Digital audio data needs to synchronize and transmit between digital audio systems.
The NJU26904 - master mode / slave mode - both of the modes are supported.

- In Master mode;
     Use the clock of BCKO and a LRO pin output clock for digital audio data transfer.
- In Slave mode;
     The clock output from a master device is needed for the input terminal of BCKI and LRI.

A device in the system generates the transmitted clock become a standard. The other devices are set according to the transmitted clock. The device generating transmitted clock is called Master Device. The device according to the transmitted clock is called Slave Device. NJU26904 usually operates Slave Device. However, NJU26904 becomes Master Device in case of SLAVEb set the High level and NJU26904 is set Master mode by firmware command. In Slave mode, clock inputted to the BCK pin and the LR pin is used to digital audio signal transmission. In Master mode, clock outputted to the BCK pin and the LR pin is used to digital audio signal transmission.

2.1 Audio Clock

Three kinds of clocks are needed for digital audio data transfer.
(1) LR clock (LR) is needed by serial-data transmission. It is the same as the sampling frequency of a digital audio signal.
(2) Bit clock (BCK) is needed by serial-data transmission. It becomes the multiple of LR clock.
(3) Master clock (MCK) is needed by A/D, D/A converter, etc. It becomes the multiple of LR clock. It is not related to serial audio data transmission.

In SLAVEb is High level, the MCK pin becomes buffer output pin for input clock to the CLK pin after NJU26904 resets. The MCK output is able to be stopped by firmware command.

In SLAVEb is Low level, MCK pin becomes system clock input pin. It is not insure to change the logical switch of SLAVEb pin during operating. If it is necessary to change SLAVEb pin setting, reset NJU26904 every time.

Table 5 SLAVEb, BCK, LR, MCK

SLAVEb and firmware setting	LR pin	BCK pin	MCK pin
SLAVEb="Low" Firmware: each	LR clock input DSP slave operating	Bit clock input DSP slave operating	NJU26904 operating clock input (MCK or CLK)
SLAVEb="High" Firmware: Slave			Master clock output (Buffer of CLK)
SLAVEb="High" Firmware: Master	LR clock output DSP Master operating	Bit clock output DSP Master operating	

In NJU26904 is used by 256 times of Maximum sampling frequency, NJU26904 is able to output LR clock of same sampling rate and two-third times of sampling rate, and output BCK clock of 32 times sampling rate and 64 times sampling rate in Master mode.

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Table 6 Input clock (In Slave mode at fosc=12.288MHz)

Mode	Clock Signal	Multiple Frequency	32kHz	44.1kHz	48kHz	96kHz	192kHz
DSP Slave	LR	1fs	32kHz	44.1kHz	48kHz	96kHz	192kHz
	BCK (32fs)	32fs	1.024MHz	1.4112MHz	1.536MHz	3.072MHz	6.144MHz
	BCK (64fs)	64fs	2.048MHz	2.822MHz	3.072MHz	6.144MHz	12.288MHz
	MCK (SLAVEb="L")	Input terminal: Clock is generated by MCK or CLK					
	MCK (SLAVEb="H")	Buffer output of CLK	12.288MHz				

Table 7 Output clock (In Master mode at fosc=12.288MHz)

Mode	Clock Signal	Multiple Frequency	Output from BCK/LR			
			32kHz	48kHz	64kHz	96kHz
DSP Master	LR	1fs	32kHz	48kHz	64kHz	96kHz
	BCK (32fs)	32fs	1.024MHz	1.536MHz	2.048MHz	3.072MHz
	BCK (64fs)	64fs	2.048MHz	3.072MHz	4.096MHz	6.144MHz
	MCK	-	12.288MHz			

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3. Digital Audio Interface

3.1 Digital Audio Data Format

The NJU26904 can use three kinds of formats hereafter as industry-standard digital audio data format.

(1) I^{2}S : MSB is put on the 2nd bit of LR clock change rate.(1 bit is delayed to left stuffing)
(2) Left-Justified : LR clock -- MSB is placed for changing.
(3) Right-Justified: LSB is placed just before LR clock change rate.
The main differences among three kinds of formats are in the position relation between LR clock (LR) and an audio data (SDI, SDO).

- In every format: : a left channel is transmitted previously.
- In Right/Left-Justified : LR clock ='High' shows a left channel.
- I^{2}S : LR clock="Low" shows a left channel.
- The Bit clock BCK is used as a shift clock of transmission data. The number of clocks more than the number of sum total transmission bits of a L/R channel is needed at least.
- One cycle of LR clock is one sample of a stereo audio data. The frequency of LR clock becomes equal to a sample rate (Fs).
- The NJU26904 supports serial data format which includes 32(32fs) or 64(64fs) BCK clocks. This serial data format is applied to both MASTER and SLAVE mode.

3.2 Serial Audio Data Input/output

The NJU26904 audio interface includes 3 data input lines: SDI0, SDI1 and SDI2 (Table 8). 3 data output lines: SDO0, SDO1 and SDO2. (Table 9).

Table 8 Serial Audio Input Pin Description

Pin No.	Symbol	Description
6	SDI0	Audio Data Input 0 L/R
5	SDI1	Audio Data Input 1 L/R
4	SDI2	Audio Data Input 2 L/R

Table 9 Serial Audio Output Pin Description

Pin No.	Symbol	Description
19	SDO0	Audio Data Output 0 L/R
20	SDO1	Audio Data Output 1 L/R
21	SDO2	Audio Data Output 2 L/R

The input terminal is selectable for the output terminal freely.
Refer to Figure 2 NJU26904 Function Diagram.

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The NJU26904 can use three kinds of formats hereafter as industry-standard digital audio data format; (1) I^{2}S (2) Left-Justified (3) Right-Justified and 24 / 20 / 18 / 16bits data length. (Fig.6-1 to Fig6-12)
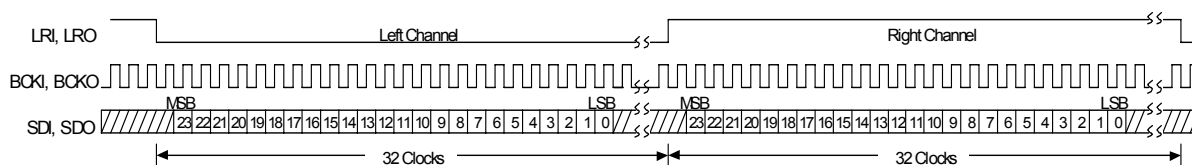An audio interface input and output data format become the same data format.
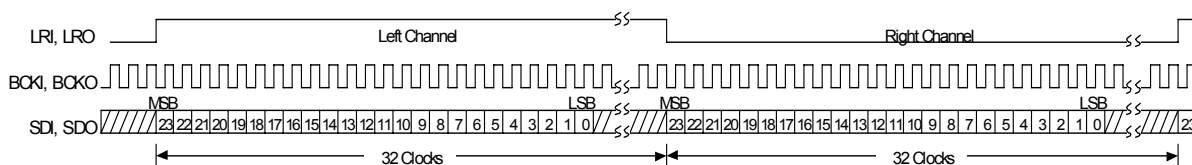

Fig.6-1 I^{2}S Data Format 64fs, 24bit Data
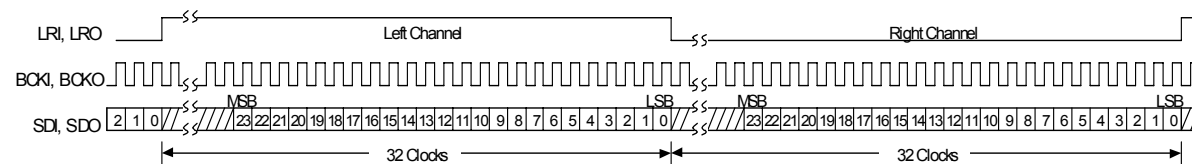

Fig.6-2 Left-Justified Data Format 64fs, 24bit Data
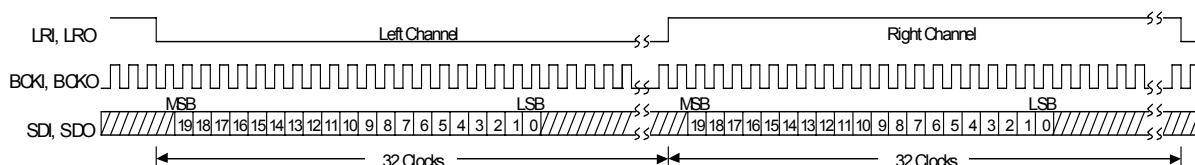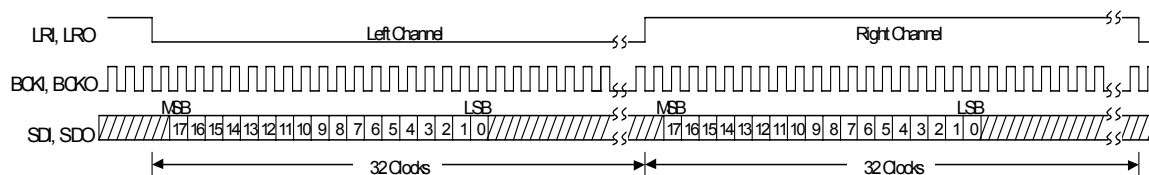

Fig.6-3 Right-Justified Data Format 64fs, 24bit Data

Fig.6-4   I^{2}S Data Format 64fs, 20bit Data
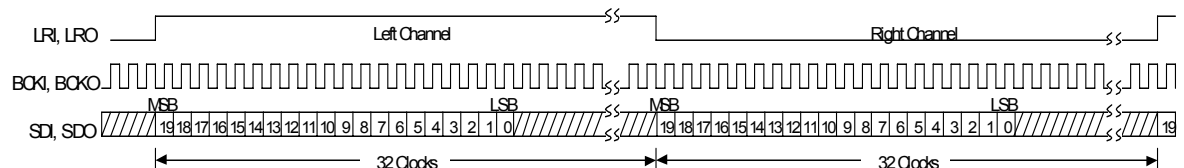
Fig.6-5   Left-Justified Data Format 64fs, 20bit Data
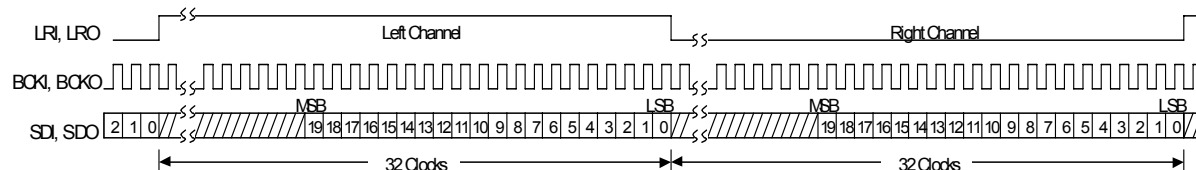
Fig.6-6   Right-Justified Data Format 64fs, 20bit Data

Fig.6-7   I²S Data Format 64fs, 18bit Data
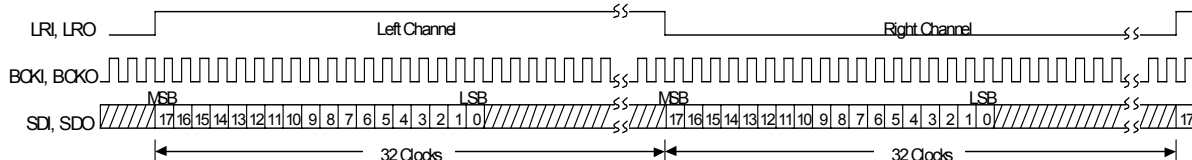
Fig.6-8   Left-Justified Data Format 64fs, 18bit Data
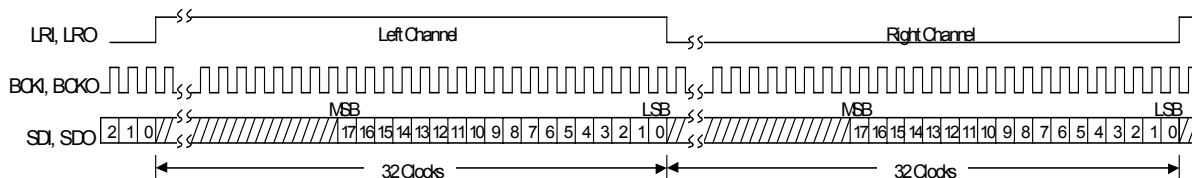
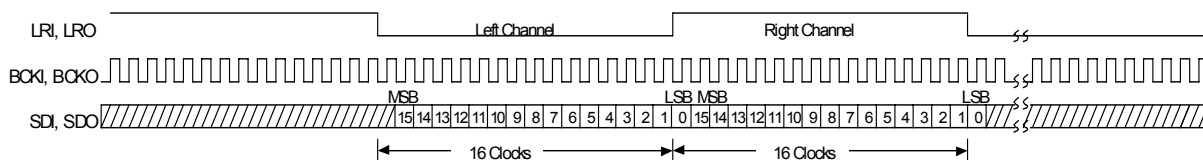**Fig.6-9   Right-Justified Data Format 64fs, 18bit Data**

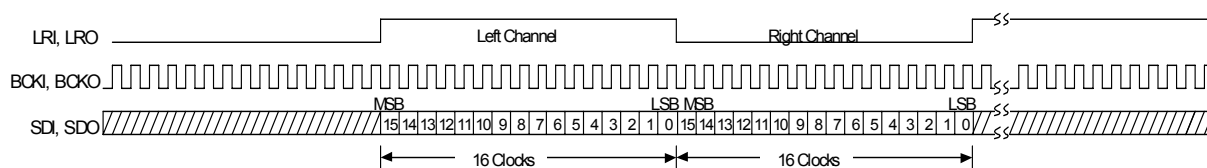**Fig.6-10 I²S Data Format 32fs, 16bit Data**
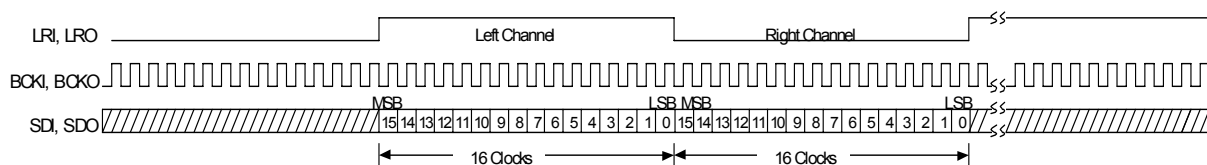

Fig.6-11 Left-Justified Data Format 32fs, 16bit Data

Fig.6-12 Right-Justified Data Format 32fs, 16bit Data

3.3 Serial Audio Input Timing

Table 10 Serial Audio Input Timing Parameters (V_{DD}=3.3V, fosc=12.288MHz, Ta=25°C)

Parameter	Symbol	Test Condition	Min	Typ.	Max	Units
BCK Frequency *	f_{BCKI}		-	-	13	MHz
BCK Period * Low Pulse Width High Pulse Width	t_{SIL} t_{SIH}		35 35	- 	- 	ns
BCK to LR Time **	t_{SLI}		15	-	-	ns
LR to BCK Time **	t_{LSI}		15	-	-	ns
Data Setup Time	t_{DS}		15	-	-	ns
Data Hold Time	t_{DH}		15	-	-	ns

* It is the regulation of absolute maximum ratings. Maximum frequency of BCK is limited.
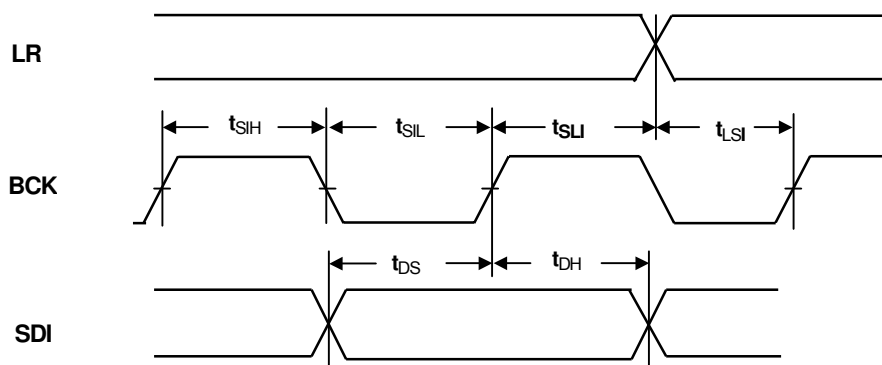** It is the regulation in slave mode.

Fig.7   Serial Audio Input Timing

Table 11   Serial Audio Output Timing Parameters (V_{DD}=3.3V, Ta=25°C)

Parameter	Symbol	Test Condition	Min	Typ.	Max	Units
BCK to LR Time *	t_{SLO}	C_L=25pF	-15	-	15	ns
Data Output Delay	t_{DOD}		-	-	15	ns

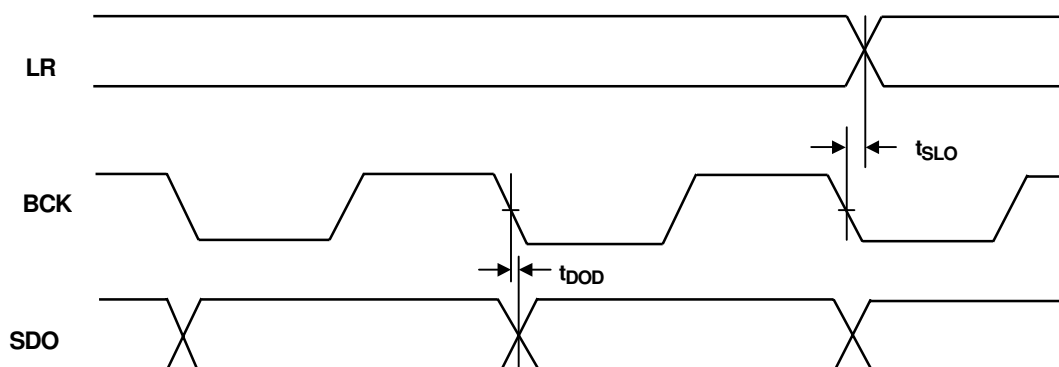* It is the regulation in Master mode.

Fig.8   Serial Audio Input Timing

■ Host Interface

The NJU26904 can be controlled via Serial Host Interface (SHI) using I^2C bus. Data transfers are in 8 bit packets (1 byte) when using either format. Refer to serial Host Interface Pin Description.(Table 12)

Table 12   Serial Host Interface Pin Description

Pin No.	Symbol (I^2C bus)	I^2C bus Format
16	AD1	I^2C bus address Bit 1
17	AD2	I^2C bus address Bit 2
22	SDA	Serial Data Input/Output (Open Drain Input/Output)
23	SCL	Serial Clock

Note : SDA pin (No.22) is a bi-directional open drain terminal. This pin requires a pull-up resister.

AD1 (No.16) pin and AD2 (No.17) pin are input pins with pull-down. AD1 (No.16) pin and AD2 (No.17) pin are connected with V_{DD} or V_{SS} through 3.3kΩ resistance.

When NJU26904 is stopped by power supply VDD, SDA pin and SCL pin become Hi-Z. But these pins are not 5V tolerant when VDD stops.

■ I^2C bus

I^2C bus interface transfers data to the SDA pin and clocks data to the SCL pin. SDA pin is a bi-directional open drain and requires a pull-up resister.

AD1 pin and AD2 pin are used to configure the seven-bit SLAVE address of the serial host interface. (Table 13) This offers additional flexibility to a system design by four different SLAVE addresses of the NJU26904. An address can be arbitrarily set up by the AD1 pin and AD2 pin. The I^2C address of AD1 and AD2 pin are decided by connection of AD1 pin and AD2 pin.

Table 13 I^2C bus SLAVE Address

bit7	bit6	bit5	bit4	bit3	AD2 bit2	AD1 bit1	R/W bit0
0	0	1	1	1	0	0	
0	0	1	1	1	0	1	RW
0	0	1	1	1	1	0	
0	0	1	1	1	1	1	

Start bit	Slave Address (7bit)	R/W bit	ACK

* SLAVE address is 0 when AD1 and AD2 are "Low".

SLAVE address is 1 when AD1 and AD2 are "High".

* SLAVE address is 0 when R/W is "W". SLAVE address is 1 when R/W is "R".

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Parameter	Symbol	Min	Max	Units
SCL Clock Frequency	f$_{SCL}$	0	400	kHz
Start Condition Hold Time	t$_{HD:STA}$	0.6	-	µs
SCL "Low" Duration	t$_{LOW}$	1.3	-	µs
SCL "High" Duration	t$_{HIGH}$	0.6	-	µs
Start Condition Setup Time	t$_{SU:STA}$	0.6	-	µs
Data Hole Time [*1]	t$_{HD:DAT}$	0	0.9	µs
Data Setup Time	t$_{SU:DAT}$	250	-	ns
Rising Time	t$_R$	-	1000	ns
Falling Time	t$_F$	-	300	ns
Stop Condition Setup Time	t$_{SU:STO}$	0.6	-	µs
Bus Release Time [*2]	t$_{BUF}$	1.3	-	µs
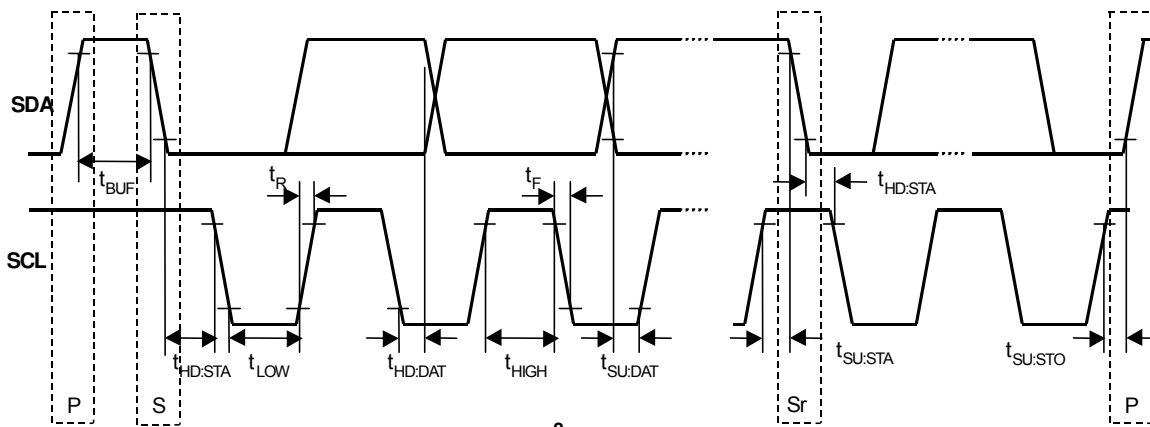
Fig.9   I^{2}C bus Timing

Note :

    *1   t$_{HD:DAT}$: Keep data 100ns hold time to avoid indefinite state by SCL falling edge.

    *2   This item shows the interface specification. The interval of a continuous command is specified separately.

■ **WatchDog Clock**

The NJU26904 outputs clock pulse through WDC (No.18) pin during normal operation.

The NJU26904 generates a clock pulse through the WDC terminal after resetting the NJU26904. The WDC clock is useful to check the status of the NJU26904 operation. For example, a microcomputer monitors the WDC clock and checks the status of the NJU26904. When the WDC clock pulse is lost or not normal clock cycle, the NJU26904 does not operate correctly. Then reset the NJU26904 and set up the NJU26904 again.

Watchdog clock output cycle is set by a command.

Note: If input and output of an audio signal stop and an audio interface stops, WDC can't output.
That is because it has controlled based on the signal of an audio interface.
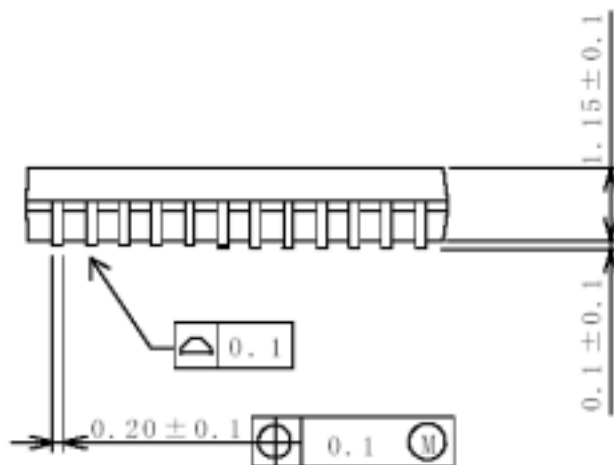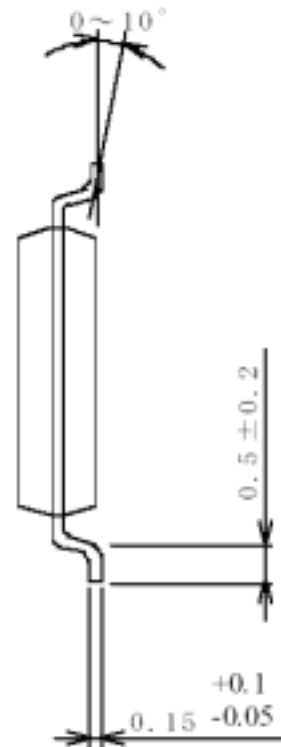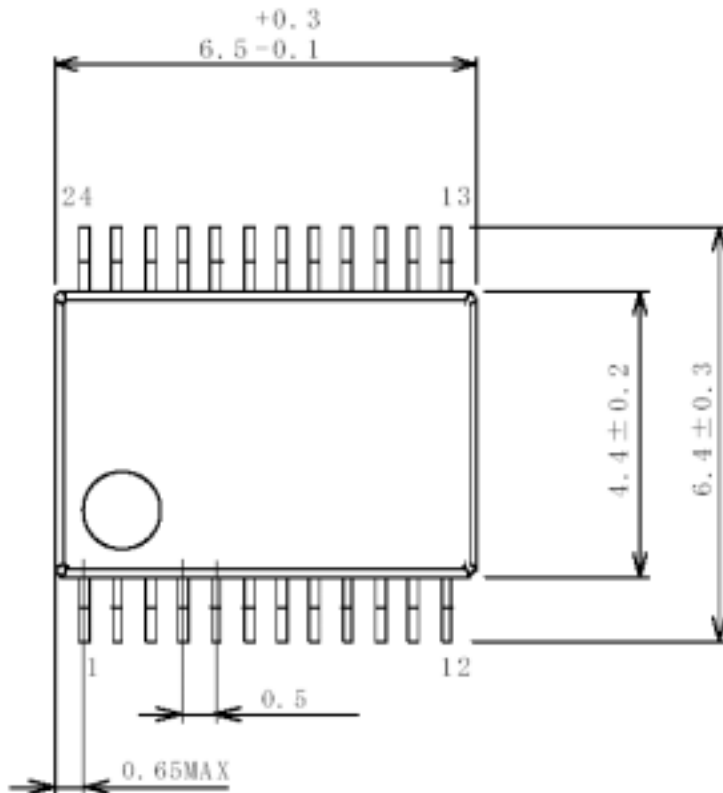
■ **NJU26904 Command Table**

Table 15   NJU26904 Command

No.	Command	No.	Command
1	System State Config (MCK, BCK, CLK, Data width etc.)	8	SDO Input Select Config Read
2	I/O Config (SDO Source Select, Setup SDO)	9	SDO Delay Setup Read
3	Delay Setup (8,121 samples, 1 sample step, Setup SDO)	10	Watchdog Setup Read
4	Watchdog Setup	11	Version Number
5	Re-Initialize Command	12	Software Reset
6	Task State Read	13	Auto Buffer Clear Disable / enable
7	System State Config Read	14	Start / Stop

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NJU26904

■ Package

SSOP24-C2, Pb-Free