# Digital Signal Processor

## ■ General Description

The NJU26126 is a high performance 24-bit digital signal processor.
The NJU26126 provides L/R channel independent 10bands PEQ, Low/High bandwidth independent DRC of FIR filter adoption, Tone Control, Lip sync Audio Delay, eala & eala Rebirth of NJRC Original Sound Enhancement, Dynamic Bass Boost, two systems Limiter, and 5.1 channel output function. These kinds of sound functions are suitable for TV, mini-component, CD radio-cassette, Sound bar and speakers system.

## ■ Package

NJU26126VC2

## ■ FEATURES

**- Software**

- NJRC Original Sound Enhancement (eala, eala Rebirth, Dynamic Bass Boost)
- HPF, LPF, Center/Sub woofer and Surround output function
- 10bands PEQ (Parametrical Equalizer) : L/R channel independent operation
- DRC (Dynamic Range Compression) : 2-bands independent operation (FIR filter adoption)
- Tone Control (Bass / Treble)
- Limiter (SDO0 / SDO1)
- Lip sync Audio Delay (fs=48kHz : Max. 22msec)
- Signal level detector
- Watchdog Clock Output

**- Hardware**

- 24bit Fixed-point Digital Signal Processing
- Maximum System Clock Frequency : 12.288MHz Max. built-in PLL Circuit
- Digital Audio Interface : 3 Input ports / 3 Output ports
- Digital Audio Format : $I^2S$ 24bit, Left- justified, Right-justified, BCK : 32/64fs
- Master / Slave Mode
  - Master Mode, MCK : 384fs @32kHz, 256fs @48kHz
- Host Interface : $I^2C$ bus (Fast-mode/400kbps)
- Power Supply : 3.3V
- Input terminal : 5V Input tolerant
- Package : SSOP24-C2 (Pb-Free)

## ■ Function Block Diagram

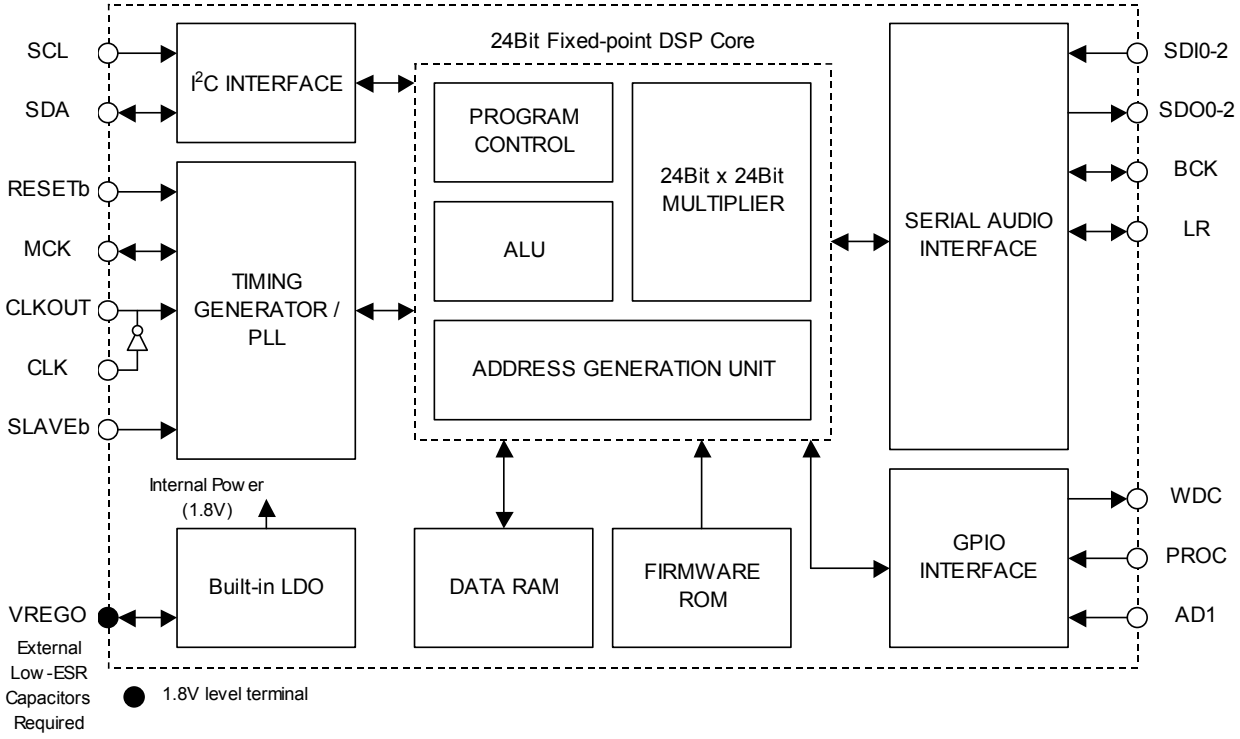



**Fig. 1 NJU26126 Block Diagram**

## ■ DSP Block Diagram

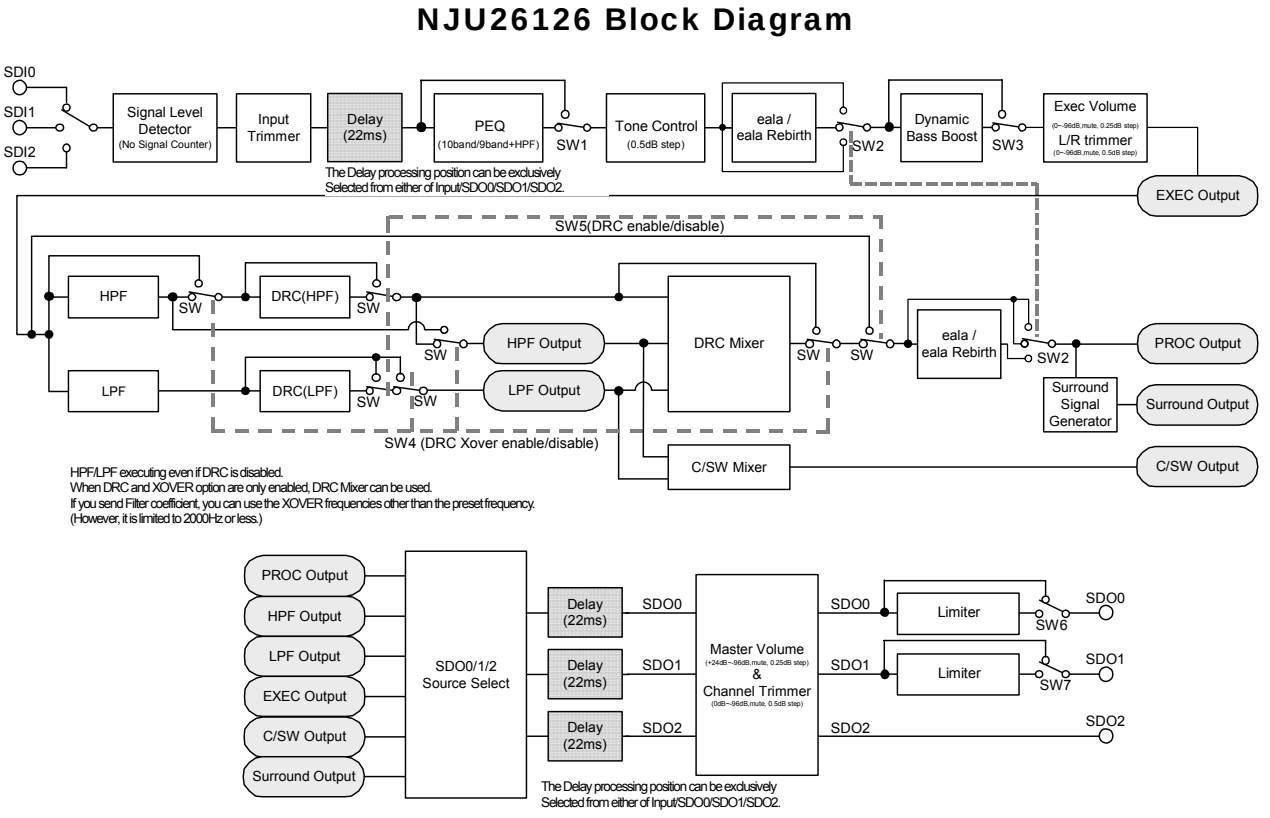



**Fig. 2 NJU26126 Function Diagram**

## ■ Pin Configuration

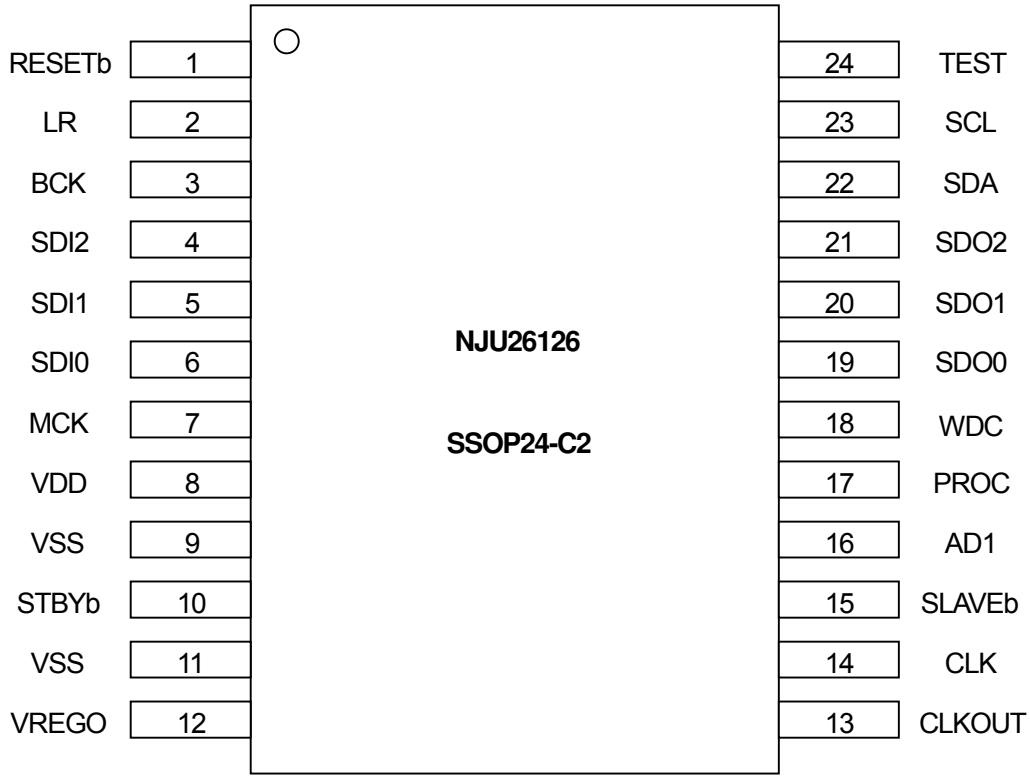



**Fig. 3 NJU26126 Pin Configuration**

## ■ Pin Description

**Table 1 Pin Description**

| No. | Symbol | I/O | Description |
|---|---|---|---|
| 1 | RESETb | I | RESET (active Low) |
| 2 | LR | I/O | LR Clock |
| 3 | BCK | I/O | Bit Clock |
| 4 | SDI2 | I | Audio Data Input 2 L/R |
| 5 | SDI1 | I | Audio Data Input 1 L/R |
| 6 | SDI0 | I | Audio Data Input 0 L/R |
| 7 | MCK | I/O | Master Clock |
| 8 | VDD | - | Power Supply +3.3V |
| 9 | VSS | - | GND |
| 10 | STBYb | I | For TEST (Connected to VDD) |
| 11 | VSS | - | GND |
| 12 | VREGO | PI | Built-in Power Supply Bypass |

| No. | Symbol | I/O | Description |
|---|---|---|---|
| 13 | CLKOUT | O | OSC Output |
| 14 | CLK | I | OSC Clock Input |
| 15 | SLAVEb | I | Slave select |
| 16 | AD1 | I | $I^2C$ Address |
| 17 | PROC | I | Status select after Reset DSP |
| 18 | WDC | OD | Clock for Watch Dog Timer |
| 19 | SDO0 | O | Audio Data Output 0 |
| 20 | SDO1 | O | Audio Data Output 1 |
| 21 | SDO2 | O | Audio Data Output 2 |
| 22 | SDA | OD | $I^2C$ I/O |
| 23 | SCL | I | $I^2C$ Clock |
| 24 | TEST | I | For TEST(Connected to VSS) |

* I : Input, O : Output, I/O: Bi-directional, OD: Open-Drain I/O, PI: Power Supply Bypass

AD1 (No.16) pin and PROC (No.17) pin are input pins. WDC (No.18) pin is open-drain pin with pull-up resistance. However, these pins operate as bi-directional pins. No.16pin and No.17pin connect with $V_{DD}$ or $V_{SS}$ through 3.3kΩ resistance. No.18pin do not connect or connect with $V_{DD}$ through 3.3kΩ resistance when unused.

VREGO (No.12) pin is a built-in power supply bypass pin. Connect low-ESR capacitor of 4.7uF and 0.01uF in parallel between VSS (No.11) pin. A built-in power supply is used only for NJU26126 operation. Be not short-circuited of this pin. Do not take out the current, and connect other power supplies.

## ■ Absolute Maximum Ratings

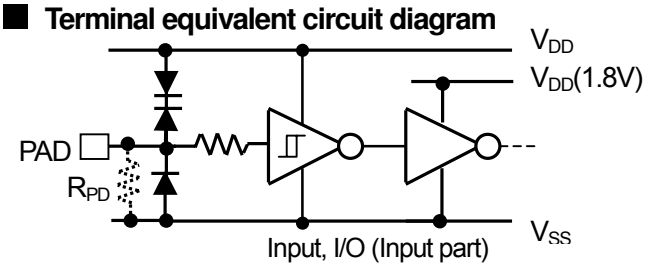
**Table 2 Absolute Maximum Ratings** **( $V_{SS}$=0V=GND, Ta=25°C )**

| Parameter | | Symbol | Rating | Units |
|---|---|---|---|---|
| Supply Voltage * | | $V_{DD}$ | -0.3 to 4.2 | V |
| Supply Voltage Bypass * | | $V_{REGO}$ | -0.3 to 2.3 | V |
| Pin Voltage * | In | $V_{x(IN)}$ | -0.3 to 5.5 ($V_{DD}$≥ 3.0V)<br>-0.3 to 4.2 ($V_{DD}$< 3.0V) | V |
| | I/O, OD | $V_{x(I/O)}$ , $V_{x(OD)}$ | | |
| | Out | $V_{x(OUT)}$ | -0.3 to 4.2 | |
| | CLK | $V_{x(CLK)}$ | | |
| | CLKOUT | $V_{x(CLKOUT)}$ | | |
| Power Dissipation | | $P_D$ | 565 | mW |
| Operating Voltage | | $T_{OPR}$ | -40 to 85 | °C |
| Storage Temperature | | $T_{STR}$ | -40 to 125 | °C |

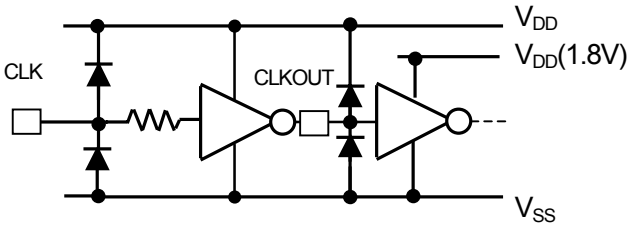
* The LSI must be used inside of the “Absolute maximum ratings”. Otherwise, a stress may cause permanent damage to the LSI.

* $V_{DD}$ : 8 pin
* $V_{REGO}$ : 12 pin
* $V_{x(IN)}$ : 1, 4, 5, 6, 10, 15, 23, 24 pin
* $V_{x(OD)}$ : 22 pin
* $V_{x(I/O)}$ : 2, 3, 7, 16, 17, 18 pin
* $V_{x(OUT)}$ : 19, 20, 21 pin
* $V_{x(CLK)}$ : 14 pin
* $V_{x(CLKOUT)}$ : 13 pin

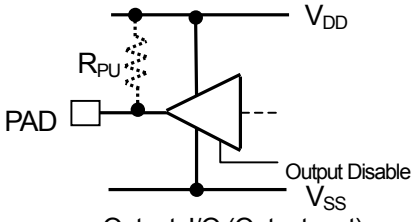
## ■ Terminal equivalent circuit diagram



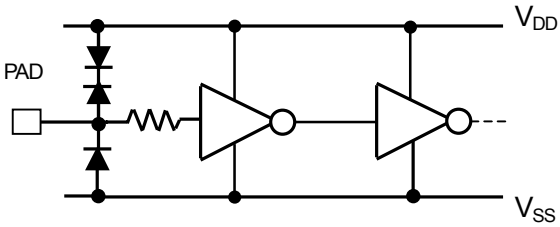

Input, I/O (Input part)
(1 to 7, 22, 23pin)
(with $R_{PU}$ : 18pin , With $R_{PD}$: 15, 16, 17, 24pin)




CLK/CLKOUT
(13, 14pin)




Output, I/O (Output part)
(2, 3, 7, 16, 17, 19, 20, 21pin )
( Open Drain Output with $R_{PU}$ : 18pin)
( Open Drain Output: 22pin )




STBYb
(10pin)

**Fig.4 NJU26126 Terminal equivalent circuit diagram**

## ■ Electric Characteristics

**Table 3 Electric Characteristics** **( $V_{DD}$=3.3V, $f_{OSC}$=12.288MHz, Ta=25°C )**

| Parameter | Symbol | Test Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Operating Voltage *1 | $V_{DD}$ | $V_{DD}$ pin | 3.0 | 3.3 | 3.6 | V |
| Operating Current | $I_{DD}$ | At no load | - | 20 | 35 | mA |
| High Level Input Voltage | $V_{IH}$ | | $V_{DD}$ x 0.7 | - | $V_{DD}$ *2 | V |
| Low Level Input Voltage | $V_{IL}$ | | 0 | - | $V_{DD}$ x 0.3 | |
| High Level Output Voltage *3 | $V_{OH}$ | ($I_{OH}$= -1mA) | $V_{DD}$ x 0.8 | - | $V_{DD}$ | |
| Low Level Output Voltage | $V_{OL}$ | ($I_{OL}$= 1mA) | 0 | - | $V_{DD}$ x 0.2 | |
| Leakage Current *4 | $I_{IN}$ | $V_{IN}$ = $V_{SS}$ to $V_{DD}$ | -10 | - | 10 | µA |
| | $I_{IN(PU)}$ | | -120 | - | 10 | |
| | $I_{IN(PD)}$ | | -10 | - | 120 | |
| Clock Frequency | $f_{OSC}$ | CLK, MCK *6 | 10 | 12.288 | 13 | MHz |
| Clock Jitter *5 | $f_{JIT(CC)}$ | | 0 | - | ±3.0 | ns |
| Clock Duty Cycle | $r_{EC}$ | | 45 | 50 | 55 | % |

*1 VDD of The NJU26126 should be within electric characteristics. When turn on VDD, the voltage should be increase monotonously. After rise up the voltage to within electric characteristics, the voltage should be not under electric characteristics. When re-start the NJU26126 after cut the power, the voltage of VDD should be drop to GND level.

*2 Input pin, Output pin and Open-Drain input/output pin are +5.0V tolerant except CLK input pin.

*3 Except No.18pin: WDC (Open-Drain output) and No.22: SDA (Open-Drain input/output).

*4 $I_{IN(PU)}$: 18pin, $I_{IN(PD)}$ : 15, 16, 17, 24 pin

*5 Clock Jitter shows Cycle-to-cycle period jitter (JEDEC JESD65).

*6 Provide clock frequency for $f_{OSC}$ spec. NJU26126 needs clock frequency 12.288MHz when sampling rate is 48kHz.

## 1. Power Supply, Input/Output terminal, Clock, Reset

### 1.1 Power Supply

The NJU26126 has a power supply $V_{DD}$. To setup good power supply condition, the decoupling capacitors should be implemented at the all power supply terminals.

$V_{DD}$ of The NJU26126 should be within electric characteristics. When turn on $V_{DD,}$ the voltage should be increase monotonously. After rise up the voltage to within electric characteristics, the voltage should be not under electric characteristics. When re-start the NJU26126 after cut the power, the voltage of $V_{DD}$ should be drop to GND level.

The NJU26126 include a built-in power supply (LDO) for internal logic. A built-in power supply generates 1.8V (-10% to +10%). VREGO (No.12) pin is a built-in power supply bypass pin. Connect low-ESR capacitor of 4.7uF and 0.01uF in parallel between VSS (No.11) pin.
A built-in power supply is used only for NJU26126 operation. Be not short-circuited of this pin. Do not take out the current, and connect other power supplies.

### 1.2 Input/Output terminal

It restricts, when the input terminals (AD1, PROC, RESETb, SDI0, SDI1, SDI2, STBYb, SLAVEb, SCL, TEST pins), the input/output terminals (LR, BCK, MCK pins) and the bi-directional Open-drain terminal (SDA pin) of NJU26126, and $V_{DD}$ are supplied on regular voltage ($V_{DD}$=3.3V), and it becomes +5V Input tolerant.

### 1.3 Clock

The NJU26126 CLK pin requires the system clock that should be related to the sample frequency 256 Fs.

(For example : Fs=48kHz  CLK=12.288MHz )

It is possible to be generated the system clock by connecting a crystal oscillator between CLK and CLKOUT. CLK/CLKOUT pins are not 5V tolerant, so check the voltage level of these pins.
When SLAVEb pin is fixed on Low level, NJU26126 supplies the system clock from MCK pin. Fix the clock input pin not used to Low level because either the CLK pin or the MCK pin is supplied in NJU26126.

The frequency divider for Master mode matched to the clock 256 times of Fs is installed in NJU26126. When clock except 256 times of Fs is used by Master mode, be careful to use because a dividing frequency of Master mode changes. Please check enough and decide parameter.

### 1.4 Reset

To initialize the NJU26126, RESETb pin should be set Low level during some period. After some period of Low level, RESETb pin should be High level. This procedure starts the initialization of the NJU26126. After the power supply and the oscillation of the NJU26126 becomes stable, RESETb pin must be kept Low-level more than $t_{RESETb}$ period. (Fig.5)

After RESETb pin level goes to "High" (after reset release), a setup of the internal hardware of a Serial Host Interface completes NJU26126 within 10msec. Then, it will be in the state which can communicate.

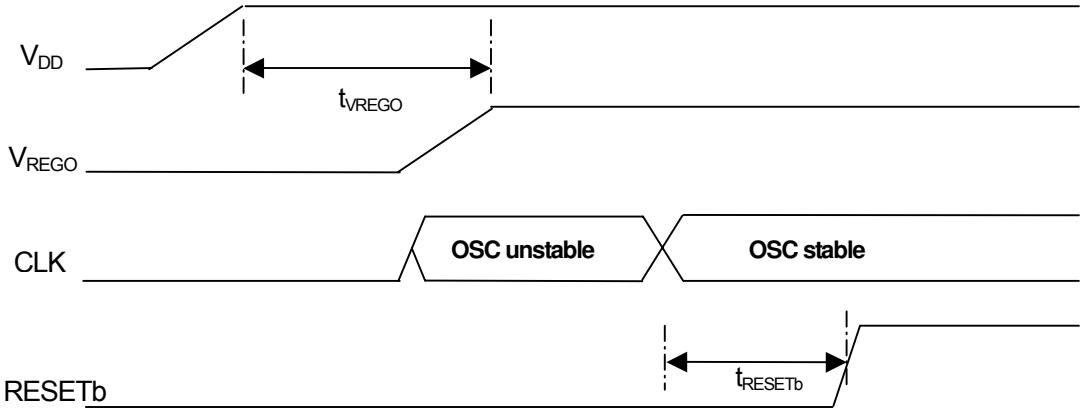



**Fig.5 Reset Timing**

**Table 4 Reset Time**

| Symbol | Time |
|---|---|
| $t_{VREGO}$ | ≥ 10msec |
| $t_{RESETb}$ | ≥ 1.0msec |

**Note :**

All the I/O terminals and the Open-Drain I/O terminals compulsorily enter the state of the high-impedance when it is made RESETb=Low. However, the pull-up/pull-down of the terminal that has adhered the pull-up/pull-down is effective.

Don't stop the supply of a clock while operating. NJU26126 installs PLL circuit internally. If the supply of a clock is stopped, PLL circuit cannot be sent a clock to the inside and NJU26126 does not operate normally.

If supply of a clock is stopped or the NJU26126 is reset again, putting a normal clock into CLK terminal, the period RESETb terminal of $t_{RESETb}$ is kept "Low" level.(Table 4) Next, the NJU26126 is reset. Then redo from initial setting.

## 2. Digital Audio Clock

Digital audio data needs to synchronize and transmit between digital audio systems. Thus, a device in the system generates the transmitted clock become a standard. The other devices are set according to the transmitted clock. The device generating transmitted clock is called Master Device. The device according to the transmitted clock is called Slave Device. NJU26126 usually operates Slave Device (In this specifications, called Slave mode). However, NJU26126 becomes Master Device in case of SLAVEb set the High level and NJU26126 is set Master mode by firmware command. In Slave mode, clock inputted to the BCK pin and the LR pin is used to digital audio signal transmission. In Master mode, clock outputted to the BCK pin and the LR pin is used to digital audio signal transmission.

### 2.1 Audio Clock

Three kinds of clocks are needed for digital audio data transfer.

(1) LR clock (LR) is needed by serial-data transmission. It is the same as the sampling frequency of a digital audio signal.
(2) Bit clock (BCK) is needed by serial-data transmission. It becomes the multiple of LR clock.
(3) Master clock (MCK) is needed by A/D, D/A converter, etc. It becomes the multiple of LR clock. It is not related to serial audio data transmission.

In SLAVEb is High level, the MCK pin becomes buffer output pin for input clock to the CLK pin after NJU26126 resets. The MCK output is able to be stopped by firmware command.

In SLAVEb is Low level, MCK pin becomes system clock input pin. It is not insure to change the logical switch of SLAVEb pin during operating. If it is necessary to change SLAVEb pin setting, reset NJU26126 every time.

**Table 5 SLAVEb, BCK, LR, MCK**

| SLAVEb and firmware setting | LR pin | BCK pin | MCK pin |
|---|---|---|---|
| SLAVEb=”Low” Firmware: each | LR clock input DSP slave operating | Bit clock input DSP slave operating | NJU26126 operating clock input (MCK or CLK) |
| SLAVEb=”H” Firmware: Slave | | | Master clock output (Buffer of CLK) |
| SLAVEb=”H” Firmware: Master | LR clock output DSP Master operating | Bit clock output DSP Master operating | |

In NJU26126 is used by 256 times of Maximum sampling frequency, NJU26126 is able to output LR clock of same sampling rate and two-third times of sampling rate, and output BCK clock of 32 times sampling rate and 64 times sampling rate in Master mode.

**Table 6 Input clock (In Slave mode)**

| Mode | Clock Signal | Multiple Frequency | 32kHz | 44.1kHz | 48kHz |
|---|---|---|---|---|---|
| DSP Slave | LR | 1fs | 32kHz | 44.1kHz | 48kHz |
| | BCK (32fs) | 32fs | 1.024MHz | 1.4112MHz | 1.536MHz |
| | BCK (64fs) | 64fs | 2.048MHz | 2.822MHz | 3.072MHz |
| | MCK (SLAVEb="L") | Input terminal: used for a clock for NJU26126 is generated by MCK or CLK terminal | | | |
| | MCK (SLAVEb="H") | Buffer output of CLK | 12.288MHz | | |

**Table 7 Output clock (In Master mode)**

| Mode | Clock Signal | Multiple Frequency | CLK pin frequency | | |
|---|---|---|---|---|---|
| | | | 32kHz | 44.1kHz | 48kHz |
| DSP Master | LR | 1fs | 32kHz | - | 48kHz |
| | BCK (32fs) | 32fs | 1.024MHz | - | 1.536MHz |
| | BCK (64fs) | 64fs | 2.048MHz | - | 3.072MHz |
| | MCK | Buffer output of CLK | 12.288MHz | | |

## 3. Digital Audio Interface

### 3.1 Digital Audio Data Format

The NJU26126 can use three kinds of formats hereafter as industry-standard digital audio data format.

(1) $I^2S$ : MSB is put on the 2nd bit of LR clock change rate.(1 bit is delayed to left stuffing)
(2) Left-justified : LR clock -- MSB is placed for changing.
(3) Right-justified : LSB is placed just before LR clock change rate.
The main differences among three kinds of formats are in the position relation between LR clock (LR) and an audio data (SDI, SDO).

- In every format: : a left channel is transmitted previously.
- In Right/Left-justified : LR clock ='High' shows a left channel.
- $I^2S$ : LR clock="Low" shows a left channel.
- The Bit clock BCK is used as a shift clock of transmission data. The number of clocks more than the number of sum total transmission bits of a L/R channel is needed at least.
- One cycle of LR clock is one sample of a stereo audio data. The frequency of LR clock becomes equal to a sample rate (Fs).
- The NJU26126 supports serial data format which includes 32(32fs) or 64(64fs) BCK clocks. This serial data format is applied to both MASTER and SLAVE mode.

### 3.2 Serial Audio Data Input/output

The NJU26126 audio interface includes 3 data input lines: SDI0, SDI1 and SDI2 (Table 8). 3 data output lines: SDO0, SDO1 and SDO2. (Table 9).

**Table 8 Serial Audio Input Pin Description**

| Pin No. | Symbol | Description |
|---|---|---|
| 6 | SDI0 | Audio Data Input 0 L/R |
| 5 | SDI1 | Audio Data Input 1 L/R |
| 4 | SDI2 | Audio Data Input 2 L/R |

**Table 9 Serial Audio Output Pin Description**

| Pin No. | Symbol | Description |
|---|---|---|
| 19 | SDO0 | Audio Data Output 0 |
| 20 | SDO1 | Audio Data Output 1 |
| 21 | SDO2 | Audio Data Output 2 |

The NJU26126 can use three kinds of formats hereafter as industry-standard digital audio data format; (1) $I^2S$ (2) Left-Justified (3) Right-justified and 16 / 18 / 20 / 24bits data length. (Fig.6-1 to Fig6-12)
An audio interface input and output data format become the same data format.

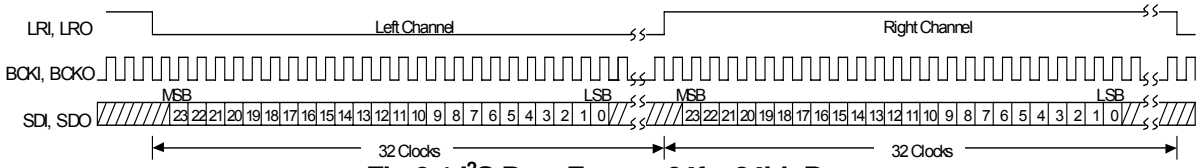



**Fig.6-1 $I^2S$ Data Format 64fs, 24bit Data**

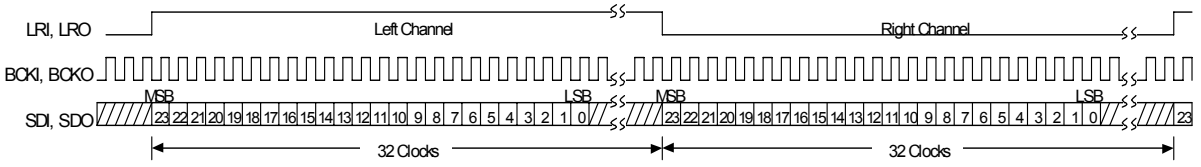



**Fig.6-2 Left-Justified Data Format 64fs, 24bit Data**

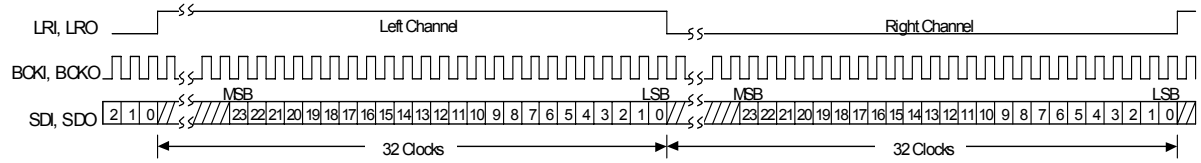



**Fig.6-3 Right-Justified Data Format 64fs, 24bit Data**

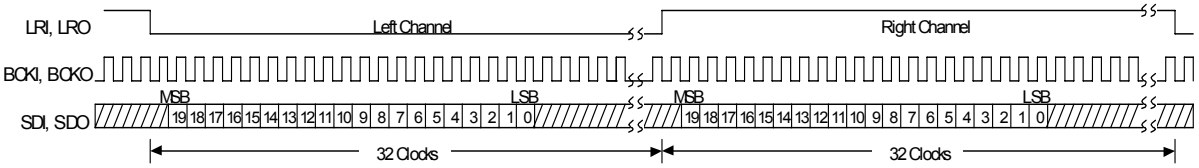



**Fig.6-4 $I^2S$ Data Format 64fs, 20bit Data**

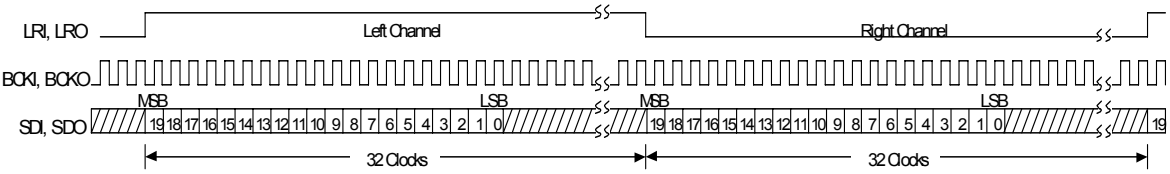



**Fig.6-5 Left-Justified Data Format 64fs, 20bit Data**

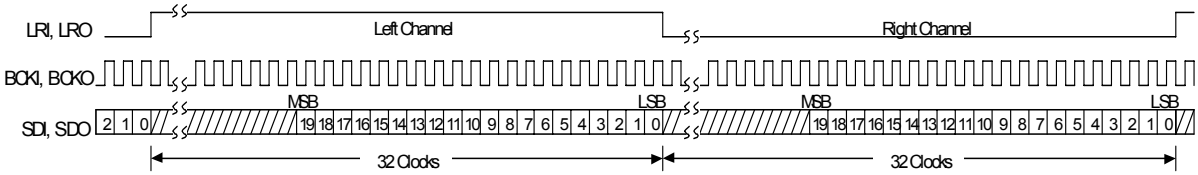



**Fig.6-6 Right-Justified Data Format 64fs, 20bit Data**

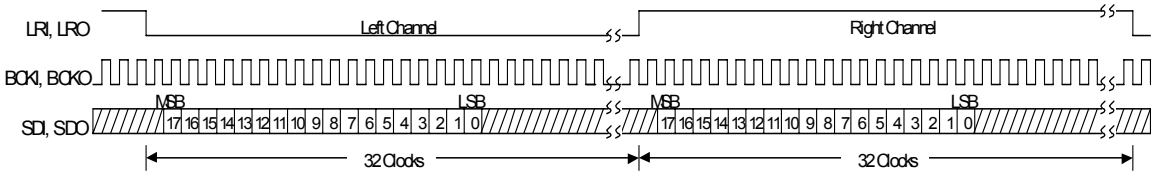



**Fig.6-7 I²S Data Format 64fs, 18bit Data**

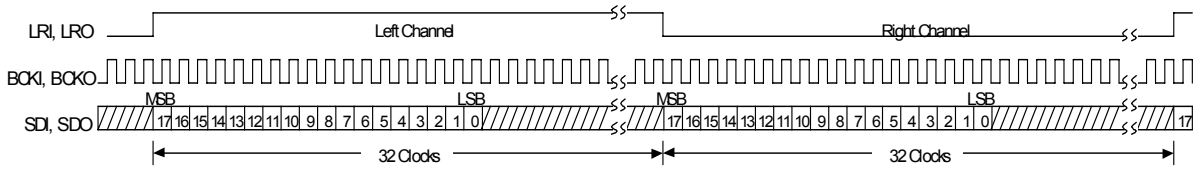



**Fig.6-8 Left-Justified Data Format 64fs, 18bit Data**

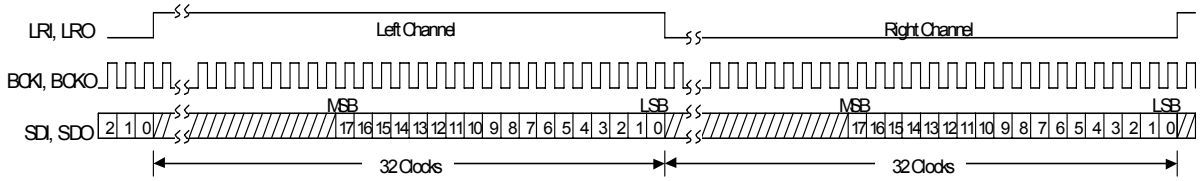



**Fig.6-9 Right-Justified Data Format 64fs, 18bit Data**

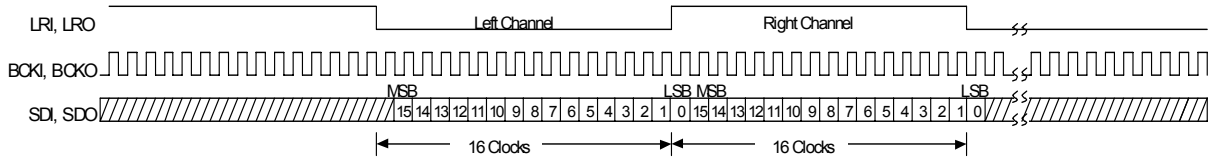



**Fig.6-10 I²S Data Format 32fs, 16bit Data**

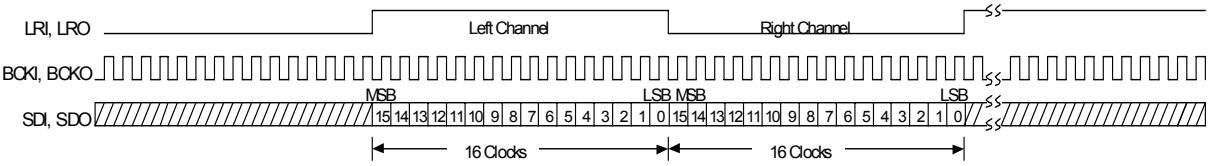



**Fig.6-11 Left-Justified Data Format 32fs, 16bit Data**

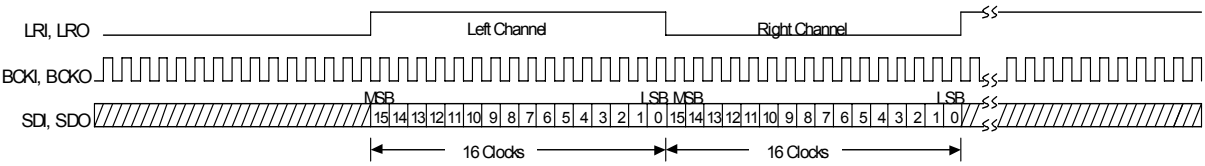



**Fig.6-12 Right-Justified Data Format 32fs, 16bit Data**

### 3.3 Serial Audio Input Timing

**Table 10 Serial Audio Input Timing Parameters** **( $V_{DD}$=3.3V, Ta=25°C )**

| Parameter | Symbol | Test Condition | Min | Typ. | Max | Units |
|---|---|---|---|---|---|---|
| BCK Frequency * | $f_{BCKI}$ | | - | - | 6.5 | MHz |
| BCK Period * | | | | | | |
| Low Pulse Width | $t_{SIL}$ | | 75 | - | - | ns |
| High Pulse Width | $t_{SIH}$ | | 75 | | | |
| BCK to LR Time ** | $t_{SLI}$ | | 40 | - | - | ns |
| LR to BCK Time ** | $t_{LSI}$ | | 40 | - | - | ns |
| Data Setup Time | $t_{DS}$ | | 15 | - | - | ns |
| Data Hold Time | $t_{DH}$ | | 15 | - | - | ns |

* It is the regulation of absolute maximum ratings. Maximum frequency of BCK is limited.
** It is the regulation in slave mode.

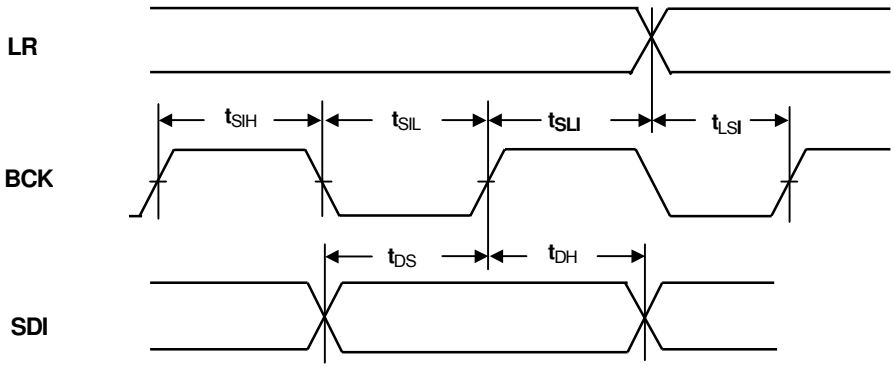



**Fig.7 Serial Audio Input Timing**

**Table 11 Serial Audio Output Timing Parameters** **( $V_{DD}$=3.3V, Ta=25°C )**

| Parameter | Symbol | Test Condition | Min | Typ. | Max | Units |
|---|---|---|---|---|---|---|
| BCK to LR Time * | $t_{SLO}$ | $C_L$=25pF | -15 | - | 15 | ns |
| Data Output Delay | $t_{DOD}$ | | - | - | 15 | ns |

* It is the regulation in Master mode.

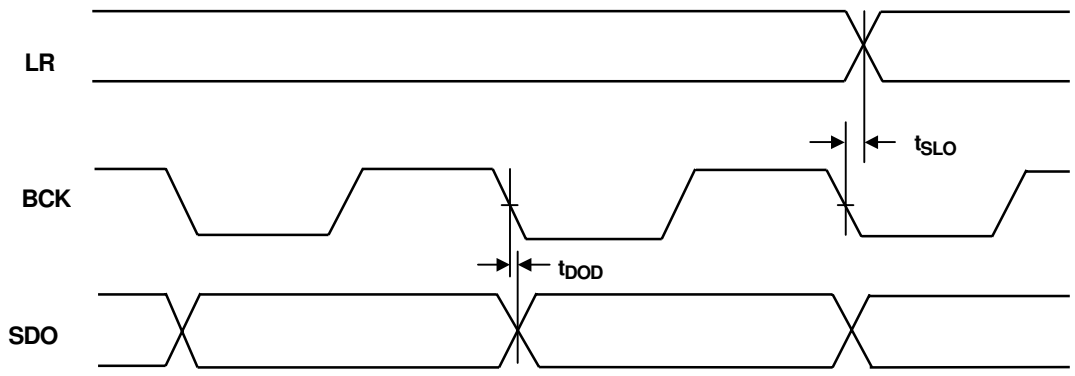



**Fig.8 Serial Audio Input Timing**

## ■ Host Interface

The NJU26126 can be controlled via Serial Host Interface (SHI) using $I^2C$ bus. Data transfers are in 8 bit packets (1 byte) when using either format. Refer to serial Host Interface Pin Description.(Table 12)

**Table 12 Serial Host Interface Pin Description**

| Pin No. | Symbol ($I^2C$ bus) | $I^2C$ bus Format |
|---|---|---|
| 16 | AD1 | $I^2C$ bus address Bit |
| 22 | SDA | Serial Data Input/Output (Open Drain Input/Output) |
| 23 | SCL | Serial Clock |

**Note :** SDA pin (No.22) is a bi-directional open drain terminal. This pin requires a pull-up resister.

AD1 (No.16) pin is input pin with pull-down. AD1 (No.16) pin is connected with $V_{DD}$ or $V_{SS}$ through 3.3kΩ resistance.

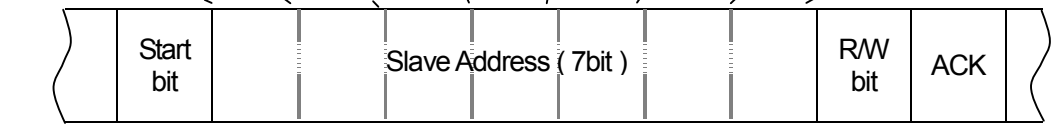
When NJU26126 is stopped by power supply VDD, SDA pin and SCL pin become Hi-Z. But these pins are not 5V tolerant when VDD stops.

## ■ $I^2C$ bus

$I^2C$ bus interface transfers data to the SDA pin and clocks data to the SCL pin. SDA pin is a bi-directional open drain and requires a pull-up resister. AD1 pin (pin#16) is used to configure LSB of the seven-bit SLAVE address of the serial host interface. Two addresses are supported by fixed value (Table 13) and connection of AD1 pin.

**Table 13 $I^2C$ bus SLAVE Address**

| Fixed value | | | | | | AD1 | R/W |
|---|---|---|---|---|---|---|---|
| bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | R/W |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | |




* SLAVE address is 0 when AD1 is “Low”. SLAVE address is 1 when AD1 is “High”.
* SLAVE address is 0 when R/W is “W”. SLAVE address is 1 when R/W is “R”.

**Note :** The serial host interface supports “Standard-Mode (100kbps)” and “Fast-Mode (400kbps)” $I^2C$ bus data transfer.

**Table 14 I²C bus Interface Timing Parameters** **( $V_{DD}$=3.3V, $f_{OSC}$=12.288MHz, Ta=25°C )**

| Parameter | Symbol | Min | Max | Units |
|---|---|---|---|---|
| SCL Clock Frequency | $f_{SCL}$ | 0 | 400 | KHz |
| Start Condition Hold Time | $t_{HD:STA}$ | 0.6 | - | µs |
| SCL "Low" Duration | $t_{LOW}$ | 1.3 | - | µs |
| SCL "High" Duration | $t_{HIGH}$ | 0.6 | - | µs |
| Start Condition Setup Time | $t_{SU:STA}$ | 0.6 | - | µs |
| Data Hole Time *1 | $t_{HD:DAT}$ | 0 | 0.9 | µs |
| Data Setup Time | $t_{SU:DAT}$ | 250 | - | Ns |
| Rising Time | $t_R$ | - | 1000 | Ns |
| Falling Time | $t_F$ | - | 300 | Ns |
| Stop Condition Setup Time | $t_{SU:STO}$ | 0.6 | - | µs |
| Bus Release Time *2 | $t_{BUF}$ | 1.3 | - | µs |

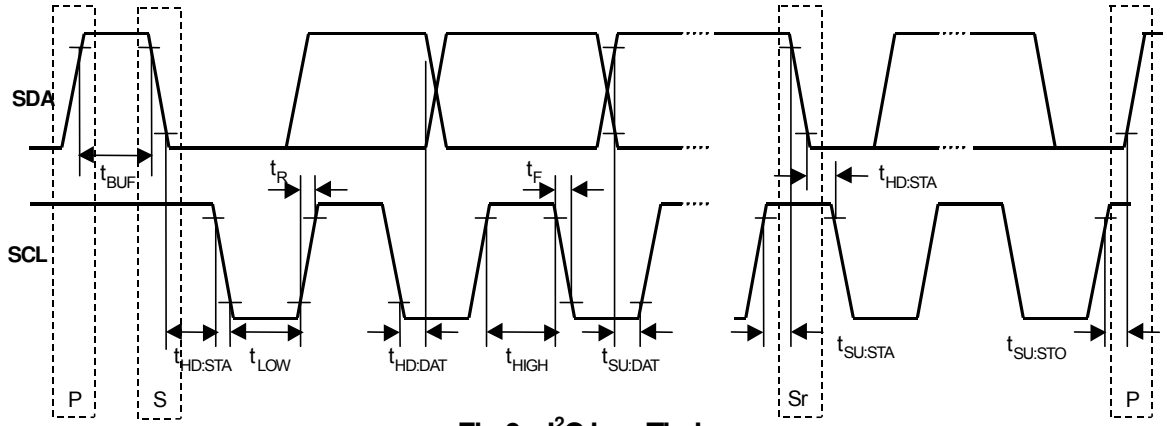



**Fig.9 I²C bus Timing**

**Note :**

*1 $t_{HD:DAT}$: Keep data 100ns hold time to avoid indefinite state by SCL falling edge.

*2 This item shows the interface specification. The interval of a continuous command is specified separately.

## ■ Pin setting

The NJU26126 operates default command setting after resetting the NJU26126. In addition, the NJU26126 restricts operation at power on by setting PROC pin (No.17) (Table 15). This pin is input pin. However, this pin operates as bi-directional pin. Connect with $V_{DD}$ or $V_{SS}$ through 3.3kΩ resistance.

**Table 15 Pin setting**

| Pin No. | Symbol | Setting | Function |
|---|---|---|---|
| 17 | PROC | "High" | The NJU26126 does not operate after reset. Sending start command is required for starting operation. |
| | | "Low" | The NJU26126 operates default setting after reset. The default value of Master Volume is Mute. |

## ■ WatchDog Clock

The NJU26126 outputs clock pulse through WDC (No.18) pin during normal operation. In the audio processing, WDC terminal notify NJU26126 operate correctly to other device by toggled (Low/High) output constantly. The unusual condition can be detected, to monitor WDC terminal by a microcomputer or a WDT IC.
Watchdog clock output cycle is about 170msec.

**Note:** If input and output of an audio signal stop and an audio interface stops, WDC can't output.
That is because it has controlled based on the signal of an audio interface.

## ■ NJU26126 Command Table

**Table 16 NJU26126 Command**

| No. | Command |
|---|---|
| 1 | Set Task |
| 2 | Fs Select |
| 3 | Smooth Control setup |
| 4 | Input Select |
| 5 | SDO0 output source select |
| 6 | SDO1 output source select |
| 7 | SDO2 output source select |
| 8 | DRC mode select |
| 9 | DRC Xover frequency select |
| 10 | Delay setup |
| 11 | System Status Configuration |
| 12 | Tone Control (Bass@100Hz) |
| 13 | Tone Control (Treble@10kHz) |
| 14 | Limiter (SDO0) time constant setup |
| 15 | Limiter (SDO0) ratio / limit &boost level setup |
| 16 | Limiter (SDO1) time constant setup |
| 17 | Clipper (SDO1) ratio / limit &boost level setup |
| 18 | Trimmer Setup |
| 19 | DRC (HPF) ratio & time constant setup |
| 20 | DRC (LPF) ratio & time constant setup |

| No. | Command |
|---|---|
| 21 | DRC (HPF) threshold level setup |
| 22 | DRC (LPF) threshold level setup |
| 23 | PEQ Setup |
| 24 | eala / eala Rebirth setup |
| 25 | User define Xover filter coefficient setup |
| 26 | User define Xover filter Freq. select |
| 27 | D.B.B ratio & time constant setup |
| 28 | D.B.B threshold level setup |
| 29 | D.B.B filter setup |
| 30 | Signal detection setup |
| 31 | Firmware Version Number |
| 32 | Firmware Revision Number |
| 33 | Software Reset |
| 34 | No signal counter read |
| 35 | No signal counter reset |
| 36 | No signal detection output enable |
| 37 | No signal detection output disable |
| 38 | Boot with Mute |
| 39 | Boot with Un-mute |
| 40 | No Operation (Nop) |

.

Please demand details of the command separately.

## ■ Package

SSOP24-C2, Pb-Free