



AUDIO PROCESSOR with Input Selector

■ GENERAL DESCRIPTION

The **NJW1185** is a sound processor with input selector includes all of functions processing audio signal for TV, such as input selector, tone control, balance, volume, and mute functions.

Also the **NJW1185** includes eala and voice enhancement.

The eala reproduces a natural surround sound with clear vocal orientation. And also, voice enhancement gives clear sound such as dialogs.

All of internal status and variables are controlled by I²C BUS interface.

■ PACKAGE OUTLINE

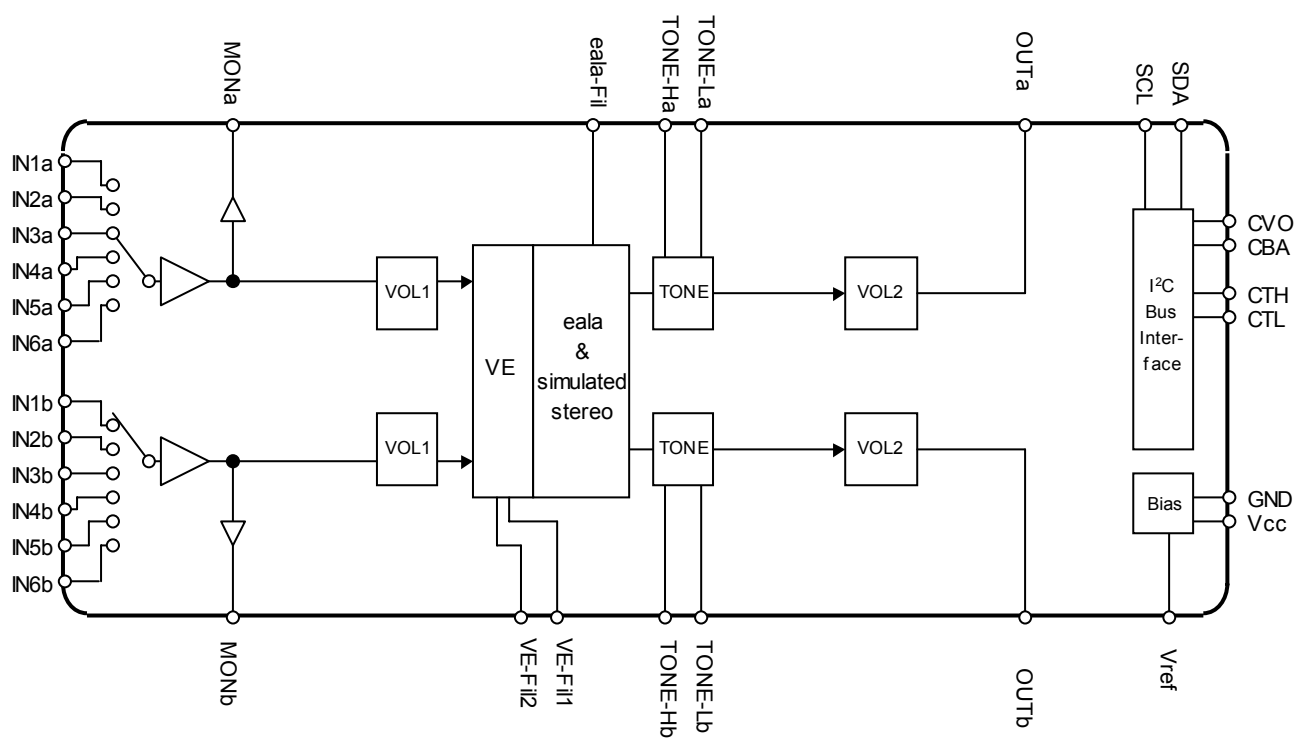


NJW1185V

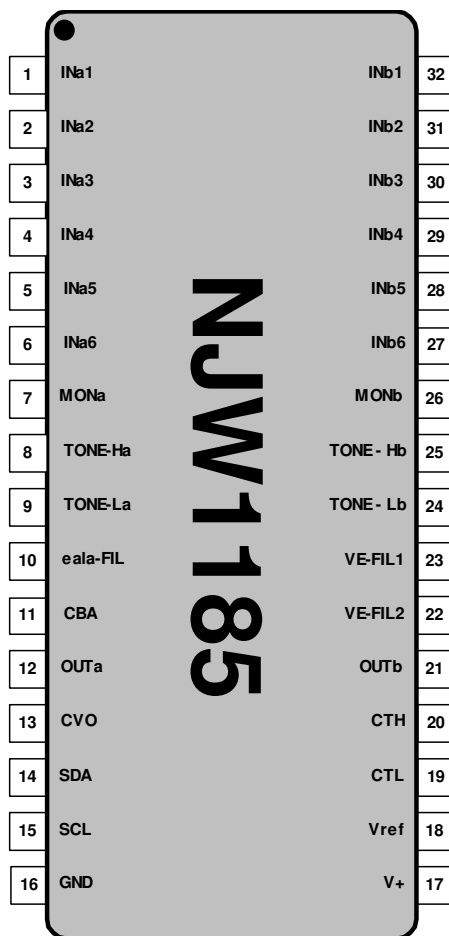
■ FEATURES

- Operating Voltage 7.5 to 13V
- 6ch Input Selector
- Tone Control Bass / Treble
- eala(NJRC Original Surround System)
- Simulated Stereo
- Voice Enhancement System
- I²C BUS Interface
- Bi-CMOS Technology
- Package Outline SSOP32

■ BLOCK DIAGRAM



PIN CONFIGURATION



No.	Symbol	Function	No.	Symbol	Function
1	INa1	Ach input terminal 1	17	V+	Supply voltage terminal
2	INa2	Ach input terminal 2	18	Vref	Reference voltage terminal
3	INa3	Ach input terminal 3	19	CTL	DAC output terminal for tone control (bass)
4	INa4	Ach input terminal 4	20	CTH	DAC output terminal for tone control (treble)
5	INa5	Ach input terminal 5	21	OUTb	Bch output terminal
6	INa6	Ach input terminal 6	22	VE-FIL2	Voice Enhancement Filter Capacitor terminal 2
7	MONa	Ach monitor output terminal	23	VE-FIL1	Voice Enhancement Filter Capacitor terminal 1
8	TONE-Ha	Ach tone control (treble) filter terminal	24	TONE-Lb	Bch tone control (bass) filter terminal
9	TONE-La	Ach tone control (bass) filter terminal	25	TONE-Hb	Bch tone control (treble) filter terminal
10	eala-FIL	eala Filter Capacitor terminal	26	MONb	Bch monitor output terminal
11	CBA	Pop Noise Reduction Capacitor for Balance terminal	27	INb6	Bch input terminal 6
12	OUTa	Ach output terminal	28	INb5	Bch input terminal 5
13	CVO	Pop Noise Reduction Capacitor for Volume terminal	29	INb4	Bch input terminal 4
14	SDA	I ² C data terminal	30	INb3	Bch input terminal 3
15	SCL	I ² C clock terminal	31	INb2	Bch input terminal 2
16	GND	Ground terminal	32	INb1	Bch input terminal 1

■ ABSOLUTE MAXIMUM RATING (Ta=25°C)

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V ⁺	15	V
Power Dissipation	P _D	(*)800 NOTE: EIA/JEDEC STANDARD Test board (76.2x114.3x1.6mm, 2layer, FR-4) mounting	mW
Operating Temperature Range	Topr	-20 to +75	°C
Storage Temperature Range	Tstg	-40 to +125	°C

■ ELECTRICAL CHARACTERISTICS

(Ta=25°C, V+=9V, R_L=47kΩ, Vin=100mVrms/1kHz unless otherwise specified)

PARAMETER	SYMBOL	Condition	Input		Output	MIN.	TYP.	MAX.	UNIT
			INa	INb					
Operating Voltage	V ⁺		-	-	-	7.5	9.0	13.0	V
Supply Current	I _{CC}	No Signal	-	-	-	-	13	25	mA
Reference Voltage	V _{REF}	No Signal	-	-	-	4.0	4.5	5.0	V
Maximum Input Voltage	V _{IM}	VOL=-20dB, THD=10%	V _{in}	-	OUTa	2.8	3.0	-	Vrms
			-	V _{in}	OUTb				
			-	V _{in}	OUTb				
Maximum Output Voltage	V _{OM}	VOL=0dB, THD=1%	V _{in}	-	OUTa	-	2.5	-	Vrms
			-	V _{in}	OUTb				
Monitor Output Gain	G _{VMON}	MON OUT	V _{in}	-	OUTa	-	0	-	dB
			-	V _{in}	OUTb				
Channel Balance	G _{CB}	VOL=0dB	-	-	-	-1.5	0.0	1.5	dB
Balance Boost A	BA _{BST}	CHS="0", BAL="111111"	V _{in}	V _{in}	OUTa	-2.0	0.0	2.0	dB
Balance Cut A	BA _{CUT}	CHS="1", BAL="111111" Vin = 1Vrms	V _{in}	V _{in}	OUTa	-	-	-70	dB
Balance Boost B	BB _{BST}	CHS="1", BAL="111111"	V _{in}	V _{in}	OUTb	-2.0	0.0	2.0	dB
Balance Cut B	BB _{CUT}	CHS="0", BAL="111111" Vin = 1Vrms	V _{in}	V _{in}	OUTb	-	-	-70	dB
Total Harmonic Distortion	THD	Vo=0.5Vrms, BW=400Hz to 30kHz	V _{in}	-	OUTa	-	-	0.5	%
			-	V _{in}	OUTb				
Maximum Gain	G _{VMAX}	VOL=0dB	V _{in}	-	OUTa	-2.0	0.0	2.0	dB
			-	V _{in}	OUTb				
Minimum Gain	G _{VMIN}	VOL=MUTE Vin=1Vrms	V _{in}	-	OUTa	-	-	-80	dB
			-	V _{in}	OUTb				
Cross Talk	CT	Vin=1Vrms A-Weighted Selected Input : No signal Unselected Inputs : Signal	V _{in}	-	OUTa	-	-	-70	dB
			-	V _{in}	OUTb				
Channel Separation	CS	Vin=1Vrms A-Weighted	V _{in}	-	OUTb	-	-80	-70	dB
			-	V _{in}	OUTa				
Output Noise Voltage 1	V _{NO1}	VOL=0dB A-Weighted	-	-	-	-	-90 (31.6)	-85 (56.2)	dBV (μVrms)
Output Noise Voltage 2	V _{NO2}	VOL=MUTE A-Weighted	-	-	-	-	-106 (5.0)	-96 (15.8)	dBV (μVrms)

BW : Band Width

■ ELECTRICAL CHARACTERISTICS

(Ta=25°C, V+=9V, R_L=47kΩ, V_{in}=100mVrms/1kHz unless otherwise specified)

PARAMETER	SYMBOL		Condition			MIN.	TYP.	MAX.	UNIT
			Input		Output				
			INa	INb					
◆TONE									
High Frequency Boost	HF _{BST}	BCT="1" TREB=+15dB, f=10kHz	V _{in}	-	OUTa	12.5	15.0	17.5	dB
			-	V _{in}	OUTb				
High Frequency Flat	HF _{FLT}	TREB=0, f=10kHz	V _{in}	-	OUTa	-2.0	0.0	2.0	dB
			-	V _{in}	OUTb				
High Frequency Cut	HF _{CUT}	BCT="0" TREB=-15dB, f=10kHz	V _{in}	-	OUTa	-	-15.0	-	dB
			-	V _{in}	OUTb				
Low Frequency Boost	LF _{BST}	BCB="1" BASS=+15dB, f=100Hz	V _{in}	-	OUTa	12.5	15.0	17.5	dB
			-	V _{in}	OUTb				
Low Frequency Flat	LF _{FLT}	BASS=0, f=100Hz	V _{in}	-	OUTa	-2.0	0.0	2.0	dB
			-	V _{in}	OUTb				
Low Frequency Cut	LF _{CUT}	BCB="0" BASS=-15dB, f=100Hz	V _{in}	-	OUTa	-	-15.0	-	dB
			-	V _{in}	OUTb				
◆SURROUND									
Surround Gain1	SR _{GAIN1}	f=100Hz, SUR1 Surround Effect1	V _{in}	-	OUTa	8.0	10.0	12.0	dB
			-	V _{in}	OUTb				
Surround Gain2	SR _{GAIN2}	f=100Hz, SUR1 Surround Effect1	V _{in}	-	OUTb	5.0	7.0	9.0	dB
			-	V _{in}	OUTa				
Surround Gain3	SR _{GAIN3}	f=100Hz, SUR1 Surround Effect2	V _{in}	-	OUTa	14.0	16.0	18.0	dB
			-	V _{in}	OUTb				
Simulated Stereo1	SR _{SIM1}	f=1kHz, Simulated Stereo	V _{in}	V _{in}	OUTa	1.0	3.0	5.0	dB
Simulated Stereo2	SR _{SIM2}	f=1kHz, Simulated Stereo	V _{in}	V _{in}	OUTb	1.0	3.0	5.0	dB
◆ VOICE ENHANCEMENT									
PARAMETER	SYMBOL		Condition			MIN.	TYP.	MAX.	UNIT
			Input		Output				
			INa	INb					
Voice Enhancement Gain 1	VE _{GAIN1}	f=5kHz, VE1 Voice Enhancement Effect 1	V _{in}	V _{in}	OUTa	3.5	6.0	8.5	dB
			V _{in}	V _{in}	OUTb				
Voice Enhancement Gain 2	VE _{GAIN2}	f=5kHz, VE2 Voice Enhancement Effect 2	V _{in}	V _{in}	OUTa	7.5	10.0	12.5	dB
			V _{in}	V _{in}	OUTb				
Voice Enhancement Gain 3	VE _{GAIN3}	f=5kHz, VE3 Voice Enhancement Effect 3	V _{in}	V _{in}	OUTa	10.5	13.0	15.5	dB
			V _{in}	V _{in}	OUTb				

■ TERMINAL DESCRIPTION

PIN NO.	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	TERMINAL DC VOLTAGE
1, 32 2, 31 3, 30 4, 29 5, 28 6, 27	INa1, INb1 INa2, INb2 INa3, INb3 INa4, INb4 INa5, INb5 INa6, INb6	Ach Input terminal 1, Bch Input terminal 1 Ach Input terminal 2, Bch Input terminal 2 Ach Input terminal 3, Bch Input terminal 3 Ach Input terminal 4, Bch Input terminal 4 Ach Input terminal 5, Bch Input terminal 5 Ach Input terminal 6, Bch Input terminal 6		$V^+/2$
7 26 12 21	MONa MONb OUTa OUTb	Ach monitor output terminal Bch monitor output terminal Ach Output terminal Bch Output terminal		$V^+/2$
8 25 9 24 23	TONE-Ha TONE-Hb TONE-La TONE-Lb VE-FIL1	Ach tone control (treble) filter terminal Bch tone control (treble) filter terminal Ach tone control (bass) filter terminal Bch tone control (bass) filter terminal Voice Enhancement Filter Capacitor terminal 1		$V^+/2$
10	eala-FIL	eala Filter Capacitor terminal		$V^+/2$

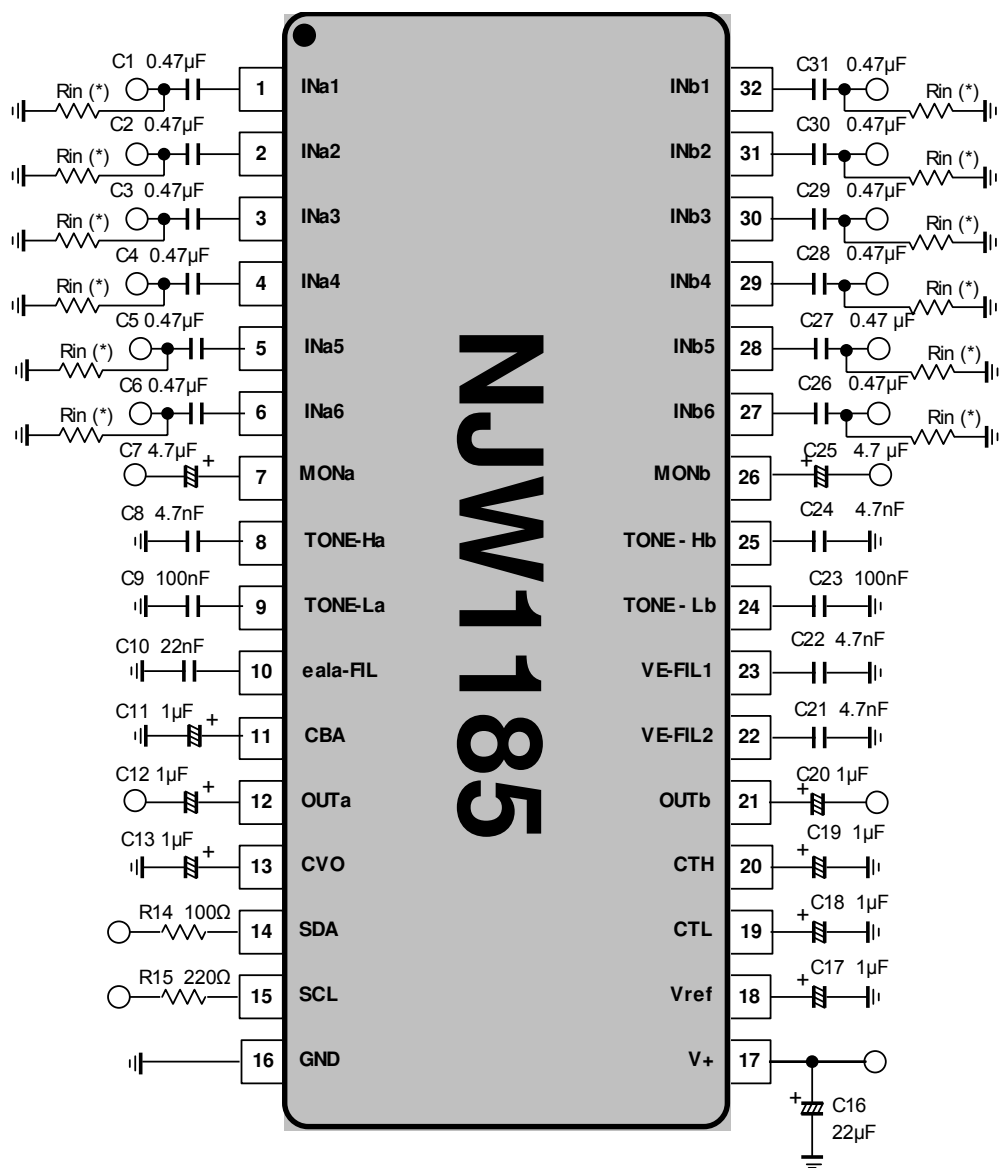
■ TERMINAL DESCRIPTION

PIN NO.	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	TERMINAL DC VOLTAGE
11 19 20	CBA CTL CTH	Pop Noise Reduction Capacitor for Balance terminal DAC output terminal for tone control (bass) DAC output terminal for tone control (treble)	PIN.11: 24k PIN.19,20:8k	$V^+/2 - 1.4$
13	CVO	Pop Noise Reduction Capacitor for Volume terminal	8k	$V^+/2 - 0.7$
14 15	SDA SCL	I ² C data terminal I ² C clock terminal	VREG 5V V+ 9V 4k 8k SCL:GND SDA:ACK	-
18	Vref	Reference voltage terminal	220k 220k	$V^+/2$

■ TERMINAL DESCRIPTION

PIN NO.	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	TERMINAL DC VOLTAGE
22	VE-FIL2	Voice Enhancement Filter Capacitor terminal 2	The diagram shows a feedback loop. On the left, there are two transistors. The top transistor's collector is connected to a supply rail. Its emitter is connected to the base of the bottom transistor. The bottom transistor's collector is connected to a supply rail. Its emitter is connected to ground. A feedback path goes from the collector of the bottom transistor, through an 8k resistor, to the base of the top transistor. The label 'FB' is placed near the 8k resistor. On the right, there is a node connected to the 8k resistor. This node is also connected to a diode pointing up to a supply rail and a diode pointing down to ground. The output of this node is shown as a terminal symbol (a circle).	$V^+/2$

APPLICATION CIRCUIT

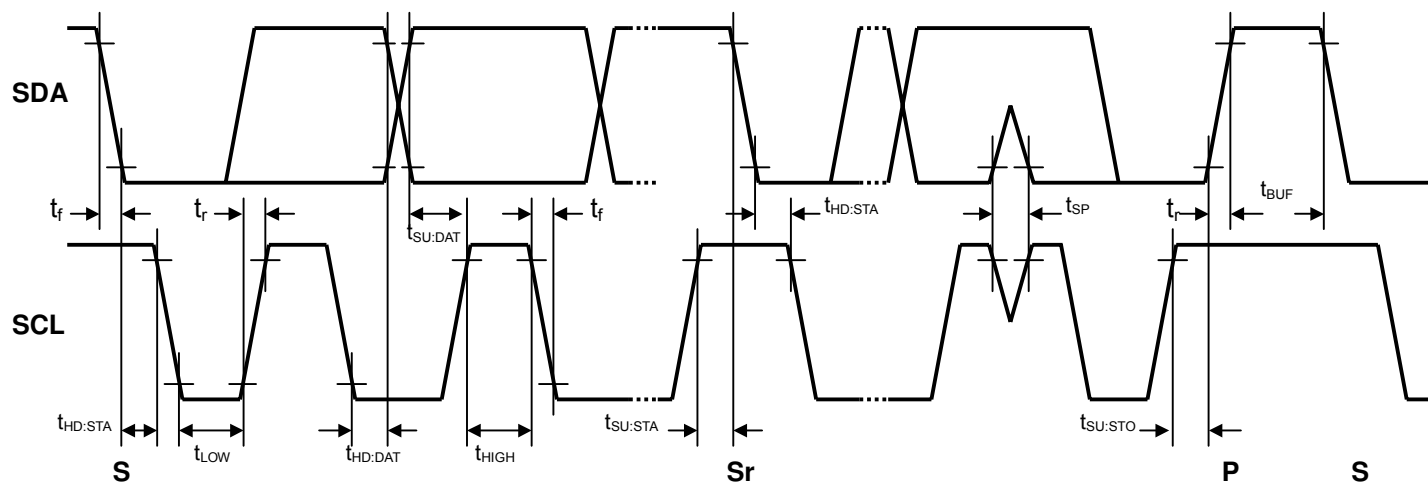


(*) Separate the I²C bus line and Signal line from the following terminals for avoiding digital noise problem and cross talk.

Pin No.	Symbol	Pin No.	Symbol
8	TONE-Ha	23	VE-Fil1
9	TONE-La	24	TONE-Lb
10	eala-Fil	25	TONE-Hb
22	VE-Fil2	-	-

(*) Cross talk performance may be effected by PCB patterning and Input resistor “Rin” in relation to input impedance. Widen intervals of input lines (1pin to 6pin, 27pin to 32pin) and put guard patterns (ground patterns) among input lines and Monitor outputs (7pin, 26pin) for avoiding cross talk problem.
Further, cross talk performance may be effected by input resistor “Rin”. The recommended “Rin” value is 20kΩ or less. In consideration of an actual operating condition, please decide Rin values after evaluating. (The NJW1185 input impedances are 48kΩtyp.)

■TIMING ON THE I²C BUS (SDA,SCL)



■CHARACTERISTICS OF I/O STAGES FOR I²C BUS (SDA,SCL)

I²C BUS Load Conditions

STANDARD MODE : Pull up resistance 4k Ω (Connected to +5V), Load capacitance 200pF (Connected to GND)

FAST MODE : Pull up resistance 4k Ω (Connected to +5V), Load capacitance 50pF (Connected to GND)

PARAMETER	SYMBOL	Standard mode			Fast mode			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Low Level Input Voltage	V_{IL}	0.0	-	1.5	0.0	-	1.5	V
High Level Input Voltage	V_{IH}	2.7	-	5.5	2.7	-	5.5	V
Low level output voltage (3mA at SDA pin)	V_{OL}	0	-	0.4	0	-	0.4	V
Input current each I/O pin with an input voltage between 0.1V _{DD} and 0.9V _{DDmax}	I_i	-10	-	10	-10	-	10	μ A

■CHARACTERISTICS OF BUS LINES (SDA,SCL) FOR I²C-BUS DEVICES

PARAMETER	SYMBOL	Standard mode			Fast mode			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
SCL clock frequency	f_{SCL}	-	-	100	-	-	400	kHz
Hold time (repeated) START condition.	$t_{HD:STA}$	4.0	-	-	0.6	-	-	μs
Low period of the SCL clock	t_{LOW}	4.7	-	-	1.3	-	-	μs
High period of the SCL clock	t_{HIGH}	4.0	-	-	0.6	-	-	μs
Set-up time for a repeated START condition	$t_{SU:STA}$	4.7	-	-	0.6	-	-	μs
Data hold time ^(NOTE)	$t_{HD:DAT}$	0	-	-	0	-	-	μs
Data set-up time	$t_{SU:DAT}$	250	-	-	100	-	-	ns
Rise time of both SDA and SCL signals	t_r	-	-	1000	-	-	300	ns
Fall time of both SDA and SCL signals	t_f	-	-	300	-	-	300	ns
Set-up time for STOP condition	$t_{SU:STO}$	4.0	-	-	0.6	-	-	μs
Bus free time between a STOP and START condition	t_{BUF}	4.7	-	-	1.3	-	-	μs
Capacitive load for each bus line	C_b	-	-	400	-	-	400	pF
Noise margin at the Low level	V_{nL}	0.5	-	-	0.5	-	-	V
Noise margin at the High level	V_{nH}	1	-	-	1	-	-	V

C_b ; total capacitance of one bus line in pF.

NOTE). Data hold time : $t_{HD:DAT}$

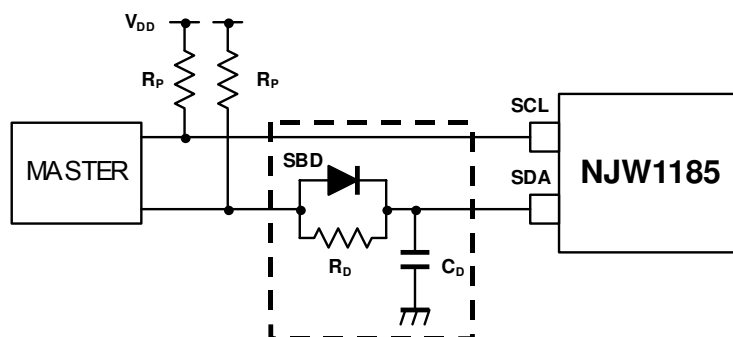
Please hold the Data Hold Time ($t_{HD:DAT}$) to 300ns or more to avoid status of unstable at SCL falling edge.

The SDA block in the NJW1185 does not hold data. Add external data-delay-circuit of the SDA terminal, in case of not providing a hold time of at least 300nsec for the SDA in the master device.

The time-consists of the data-delay-circuit of the SDA terminal are as follows.

- (a) Low level $\rightarrow$ High level : $T_{LH} \approx R_P \cdot C_D$
- (b) High level $\rightarrow$ Low level : $T_{HL} \approx R_D \cdot C_D$

In addition, Schottky barrier diode (SBD) influences a Low level at the Acknowledge. Therefore choose the low forward voltage (V_f) as much as possible.



■ DEFINITION OF I²C REGISTER

◆ I²C BUS FORMAT

MSB	LSB	MSB	LSB	MSB	LSB		
S	Slave Address	A	Select Address	A	Data	A	P
1bit	8bit	1bit	8bit	1bit	8bit	1bit	1bit

S: Starting Term

A: Acknowledge Bit

P: Ending Term

◆ SLAVE ADDRESS

Slave Address								Hex
MSB								LSB
1	0	0	0	0	0	0	0	80(h)

◆ CONTROL REGISTER TABLE

The select address sets each function (Volume, Balance, Tone Control, Surround, Voice Enhancement, Input Selector).

The auto increment function cycles the select address as follows.

00H*01H*02H*03H*00H

<Write Mode>

Select Address	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
00H	VOL							
01H	CHS	BAL					SUR	
02H	BCB	BASS				VE		*
03H	BCT	TREB				SEL		

* : Don't Care

◆ CONTROL REGISTER DEFAULT VALUE

Control register default value is all "0".

Select Address	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
00H	0	0	0	0	0	0	0	0
01H	0	0	0	0	0	0	0	0
02H	0	0	0	0	0	0	0	0
03H	0	0	0	0	0	0	0	0

■INSTRUCTION CODE

a) MASTER VOLUME SETTING

Select Address	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
00H	VOL							

- VOL Attenuation Level setting (0.33dB / step)

The volume control for both Ach and Bch(0.33dB/step).

The volume is consisted of volume1 and volume2 and the level is divided into half to each volume1 and volume2.

b) BALANCE, SURROUND SETTING

Select Address	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
01H	CHS	BAL					SUR	

- CHS : Channel select for balance control

“0” : Ach “Bch is attenuated”

“1” : Bch “Ach is attenuated”

- BAL : Balance control for both Ach and Bch (1dB/step)

The balance is consisted of volume1 and volume2.

<SUR : Surround Level Setting>

Surround Setting	D1	D0	Remarks
Bypass	0	0	Bypass
Simulated Stereo	0	1	Simulated Stereo
eala Effect1	1	0	Surround Effect Low(10dB typ.)
eala Effect2	1	1	Surround Effect High(16dB typ.)

c) TONE CONTROL BASS, VOICE ENHANCEMENT SETTING

Select Address	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
03H	BCB	BASS				VE		Don't Care

- BCB : Boost cut select for Bass control

“0” : Cut

“1” : Boost

- BASS : BASS Level Setting

Cut Level : -15 to 0dB(1dB/Step)

Boost Level : 0 to +15dB(1dB/Step)

<VE : Voice Enhancement Setting>

VE Setting	D2	D1	Remarks
By-Pass	0	0	Bypass
VE Effect 1	0	1	Voice Enhancement Effect Low (6dB typ.)
VE Effect 2	1	0	Voice Enhancement Effect Mid (10dB typ.)
VE Effect 3	1	1	Voice Enhancement Effect High (13dB typ.)

Note) Surround, Voice Enhancement mode switch settings

The click noise may be generated by changing the Surround, the Voice Enhancement mode.

Provide the external circuit for avoiding the click noise on above condition.

d) TONE CONTROL TREBLE, INPUT SELECTOR SETTING

Select Address	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
4H	BCT	TREB				SEL		

•BCT : Boost cut select for Treble control

“0” : Cut

“1” : Boost

•TREB : TREBLE Level Setting

Cut Level : -15 to 0dB(1dB/Step)

Boost Level : 0 to +15dB(1dB/Step)

<SEL : Input Selector Setting>

SEL Setting	D2	D1	D0
Input 1	0	0	0
Input 2	0	0	1
Input 3	0	1	0
Input 4	0	1	1
Input5	1	0	0
Input6	1	0	1

■MASTER VOLUME (Select Address : 00H)

		VOL							
Gain (dB)	HEX	D7	D6	D5	D4	D3	D2	D1	D0
0	FF	1	1	1	1	1	1	1	1
-1	FC	1	1	1	1	1	1	0	0
-2	F9	1	1	1	1	1	0	0	1
-3	F6	1	1	1	1	0	1	1	0
-4	F3	1	1	1	1	0	0	1	1
-5	F0	1	1	1	1	0	0	0	0
-6	ED	1	1	1	0	1	1	0	1
-7	EA	1	1	1	0	1	0	1	0
-8	E7	1	1	1	0	0	1	1	1
-9	E4	1	1	1	0	0	1	0	0
-10	E1	1	1	1	0	0	0	0	1
-11	DE	1	1	0	1	1	1	1	0
-12	DB	1	1	0	1	1	0	1	1
-13	D8	1	1	0	1	1	0	0	0
-14	D5	1	1	0	1	0	1	0	1
-15	D2	1	1	0	1	0	0	1	0
-16	CF	1	1	0	0	1	1	1	1
-17	CC	1	1	0	0	1	1	0	0
-18	C9	1	1	0	0	1	0	0	1
-19	C6	1	1	0	0	0	1	1	0
-20	C3	1	1	0	0	0	0	1	1
-21	C0	1	1	0	0	0	0	0	0
-22	BD	1	0	1	1	1	1	0	1
-23	BA	1	0	1	1	1	0	1	0
-24	B7	1	0	1	1	0	1	1	1
-25	B4	1	0	1	1	0	1	0	0
-26	B1	1	0	1	1	0	0	0	1
-27	AE	1	0	1	0	1	1	1	0
-28	AB	1	0	1	0	1	0	1	1
-29	A8	1	0	1	0	1	0	0	0
-30	A5	1	0	1	0	0	1	0	1
-31	A2	1	0	1	0	0	0	1	0
-32	9F	1	0	0	1	1	1	1	1
-33	9C	1	0	0	1	1	1	0	0
-34	99	1	0	0	1	1	0	0	1
-35	96	1	0	0	1	0	1	1	0
-36	93	1	0	0	1	0	0	1	1
-37	90	1	0	0	1	0	0	0	0
-38	8D	1	0	0	0	1	1	0	1
-39	8A	1	0	0	0	1	0	1	0
-40	87	1	0	0	0	0	1	1	1
-41	84	1	0	0	0	0	1	0	0
-42	81	1	0	0	0	0	0	0	1

■MASTER VOLUME (Select Address : 00H)

Gain (dB)	HEX	VOL							
		D7	D6	D5	D4	D3	D2	D1	D0
-43	7E	0	1	1	1	1	1	1	0
-44	7B	0	1	1	1	1	0	1	1
-45	78	0	1	1	1	1	0	0	0
-46	75	0	1	1	1	0	1	0	1
-47	72	0	1	1	1	0	0	1	0
-48	6F	0	1	1	0	1	1	1	1
-49	6C	0	1	1	0	1	1	0	0
-50	69	0	1	1	0	1	0	0	1
-51	66	0	1	1	0	0	1	1	0
-52	63	0	1	1	0	0	0	1	1
-53	60	0	1	1	0	0	0	0	0
-54	5D	0	1	0	1	1	1	0	1
-55	5A	0	1	0	1	1	0	1	0
-56	57	0	1	0	1	0	1	1	1
-57	54	0	1	0	1	0	1	0	0
-58	51	0	1	0	1	0	0	0	1
-59	4E	0	1	0	0	1	1	1	0
-60	4B	0	1	0	0	1	0	1	1
-61	48	0	1	0	0	1	0	0	0
-62	45	0	1	0	0	0	1	0	1
-63	42	0	1	0	0	0	0	1	0
-64	3F	0	0	1	1	1	1	1	1
-65	3C	0	0	1	1	1	1	0	0
-66	39	0	0	1	1	1	0	0	1
-67	36	0	0	1	1	0	1	1	0
-68	33	0	0	1	1	0	0	1	1
-69	30	0	0	1	1	0	0	0	0
-70	2D	0	0	1	0	1	1	0	1
-71	2A	0	0	1	0	1	0	1	0
-72	27	0	0	1	0	0	1	1	1
-73	24	0	0	1	0	0	1	0	0
-74	21	0	0	1	0	0	0	0	1
-75	1E	0	0	0	1	1	1	1	0
-76	1B	0	0	0	1	1	0	1	1
-77	18	0	0	0	1	1	0	0	0
-78	15	0	0	0	1	0	1	0	1
-79	12	0	0	0	1	0	0	1	0
-80	0F	0	0	0	0	1	1	1	1
-81	0C	0	0	0	0	1	1	0	0
-82	09	0	0	0	0	1	0	0	1
-83	06	0	0	0	0	0	1	1	0
-84	03	0	0	0	0	0	0	1	1
Mute*	00	0	0	0	0	0	0	0	0

* : Default Value

■BALANCE (Select Address : 01H)

Channel Select (CHS)	D7
Ach(Bch is attenuate)	0
Bch(Ach is attenuate)	1

	BAL				
Gain(dB)	D6	D5	D4	D3	D2
0*	0	0	0	0	0
-1	0	0	0	0	1
-2	0	0	0	1	0
-3	0	0	0	1	1
-4	0	0	1	0	0
-5	0	0	1	0	1
-6	0	0	1	1	0
-7	0	0	1	1	1
-8	0	1	0	0	0
-9	0	1	0	0	1
-10	0	1	0	1	0
-11	0	1	0	1	1
-12	0	1	1	0	0
-13	0	1	1	0	1
-14	0	1	1	1	0
-15	0	1	1	1	1
-16	1	0	0	0	0
-17	1	0	0	0	1
-18	1	0	0	1	0
-19	1	0	0	1	1
-20	1	0	1	0	0
-21	1	0	1	0	1
-22	1	0	1	1	0
-23	1	0	1	1	1
-24	1	1	0	0	0
-25	1	1	0	0	1
-26	1	1	0	1	0
-27	1	1	0	1	1
-28	1	1	1	0	0
-29	1	1	1	0	1
-30	1	1	1	1	0
Mute	1	1	1	1	1

* : Default Value

■Tone Control(Bass Setting) (Select Address : 02H)

Bass Cut or Boost	BCB D7
Cut*	0
Boost	1

		BASS			
Cut Gain(dB)	Boost Gain(dB)	D6	D5	D4	D3
-15	15	1	1	1	1
-14	14	1	1	1	0
-13	13	1	1	0	1
-12	12	1	1	0	0
-11	11	1	0	1	1
-10	10	1	0	1	0
-9	9	1	0	0	1
-8	8	1	0	0	0
-7	7	0	1	1	1
-6	6	0	1	1	0
-5	5	0	1	0	1
-4	4	0	1	0	0
-3	3	0	0	1	1
-2	2	0	0	1	0
-1	1	0	0	0	1
0*	0	0	0	0	0

* : Default value

■TONE CONTROL TREBLE (Select Address : 03H)

Treble Cut or Boost	BCT
	D7
Cut*	0
Boost	1

		TREB			
Cut Gain(dB)	Boost Gain(dB)	D6	D5	D4	D3
-15	15	1	1	1	1
-14	14	1	1	1	0
-13	13	1	1	0	1
-12	12	1	1	0	0
-11	11	1	0	1	1
-10	10	1	0	1	0
-9	9	1	0	0	1
-8	8	1	0	0	0
-7	7	0	1	1	1
-6	6	0	1	1	0
-5	5	0	1	0	1
-4	4	0	1	0	0
-3	3	0	0	1	1
-2	2	0	0	1	0
-1	1	0	0	0	1
0*	0	0	0	0	0

* : Default value

[CAUTION]

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