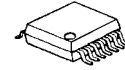


## Ground Referenced Stereo Headphone Amplifier

### ■ GENERAL DESCRIPTION

The **NJU72040** is an audio headphone amplifier .  
 Ground-referenced outputs eliminate output coupling capacitor. The pop noise suppression circuit removes a pop noise at the power-on and power-off.  
 It is suitable for audio headphone amplifier application

### ■ PACKAGE OUTLINE



NJU72040V

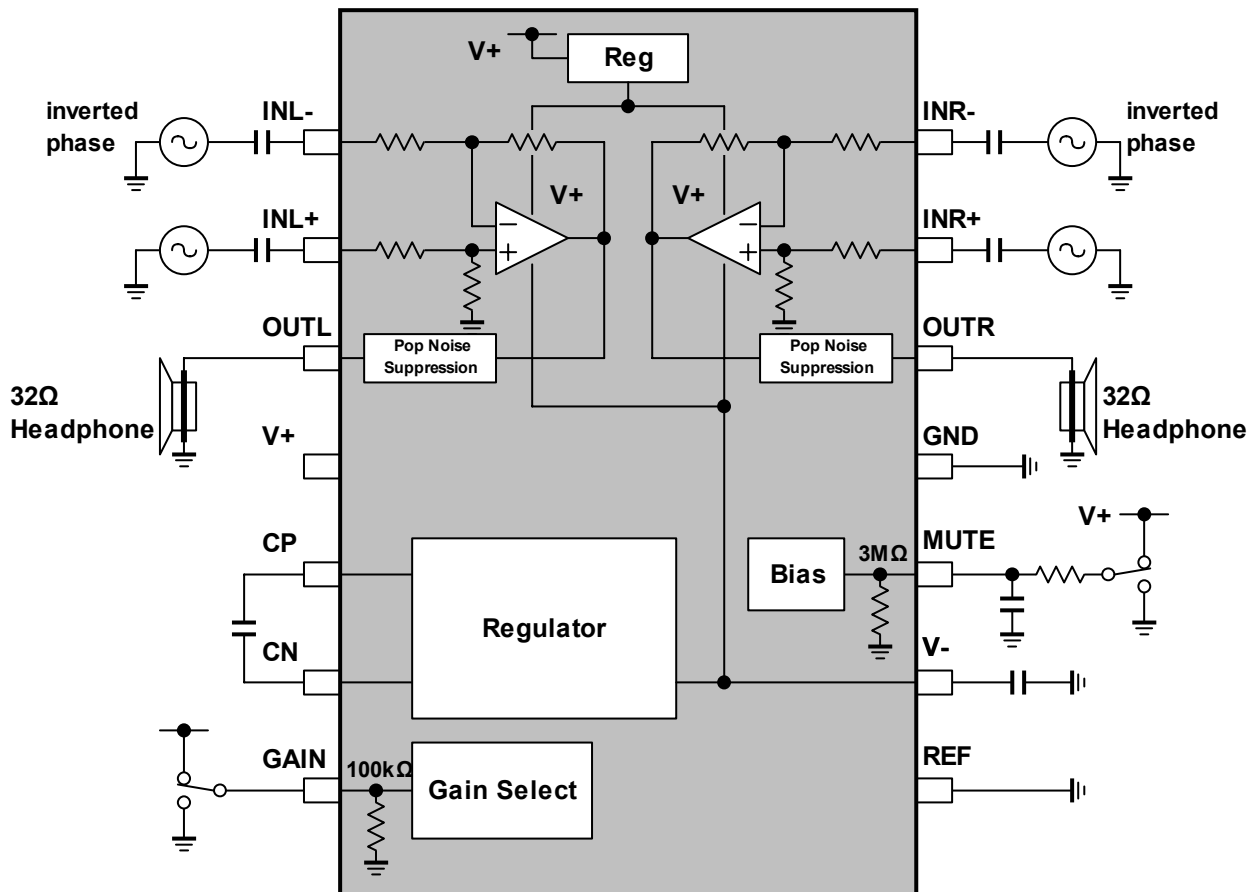
### ■ APPLICATIONS

- Audio applications which have audio headphone interface

### ■ FEATURES

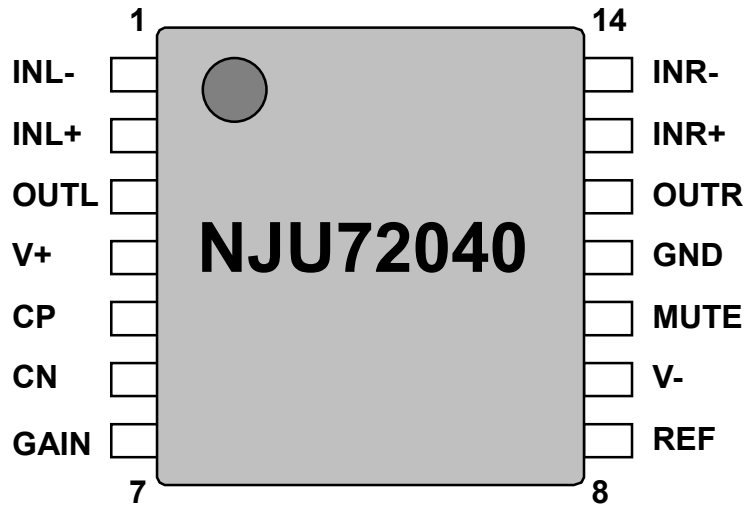
- Operating Voltage +2.7 to +3.6V
- Operating Current  $I_{DD}=10.5\text{mA typ.}$   
at  $V^+=3.3\text{V}$ , No load, No Signal
- Output Coupling Capacitor-less
- Pop Noise Suppression Circuit
- Gain Select
- C-MOS Technology
- Package Outline SSOP14

### ■ BLOCK DIAGRAM



# NJU72040

## ■ PIN CONFIGURATION



No.	Symbol	Function	No.	Symbol	Function
1	INL-	Lch Inverted Input	8	REF	Reference Voltage Input
2	INL+	Lch Noninverted Input	9	V-	V- Power Supply
3	OUTL	Lch Output	10	MUTE	MUTE / Pop Noise Suppression
4	V+	V+ Power Supply	11	GND	Ground
5	CP	Flying Capacitor Positive Terminal	12	OUTR	Rch Output
6	CN	Flying Capacitor Negative Terminal	13	INR+	Rch Inverted Input
7	GAIN	Gain Select	14	INR-	Rch Noninverted Input

## ■ ABSOLUTE MAXIMUM RATING (Ta=25°C)

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V <sup>+</sup>	+4	V
Power Dissipation	P <sub>D</sub>	SSOP14 : 550 <sup>(Note1)</sup>	mW
Maximum Input Voltage	V <sub>IM</sub>	V <sup>+</sup> +0.3	V
Operating Temperature Range	Topr	-40 ~ +85	°C
Storage Temperature Range	Tstg	-40 ~ +125	°C

(Note1) EIA/JEDEC STANDARD Test board (76.2x114.3x1.6mm, 2layer, FR-4) mounting

## ■ RECOMMENDED OPERATING CONDITIONS

(Ta=25°C unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V <sup>+</sup>		2.7	3.3	3.6	V

## ■ ELECTRICAL CHARACTERISTICS

(Ta=25°C, V<sup>+</sup>=3.3V, f=1kHz, Vin=0.1Vrms[differential input], Gv=6.4dB, MUTE=OFF, R<sub>L</sub>=32Ω unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I <sub>DD</sub>	No signal, No load	-	10.5	15.5	mA
Input Resistance1	R <sub>in1</sub>	INL-, INR-	49	61	73	kΩ
Input Resistance2	R <sub>in2</sub>	INL+, INR+	103	129	155	kΩ
Voltage Gain1	G <sub>V1</sub>	Gain Terminal=Low	5.4	6.4	7.4	dB
Voltage Gain2	G <sub>V2</sub>	Gain Terminal=High	11.4	12.4	13.4	dB
Voltage Gain3	G <sub>V3</sub>	Gain Terminal=Low, R <sub>L</sub> =10kΩ	6.6	7.1	7.6	dB
Voltage Gain4	G <sub>V4</sub>	Gain Terminal=High, R <sub>L</sub> =10kΩ	12.6	13.1	13.6	dB
Maximum Output Power1	P <sub>OMAX1</sub>	THD=3%, R <sub>L</sub> =32Ω Input=Lch or Rch	-	80	-	mW
Maximum Output Power2	P <sub>OMAX2</sub>	THD=3%, R <sub>L</sub> =32Ω Input=Lch and Rch	-	55	-	mW
Maximum Output Voltage Level	V <sub>OMAX</sub>	THD=1%, R <sub>L</sub> =10kΩ	-	2.2	-	Vrms
Mute Level	V <sub>MUTE</sub>	Rg=0Ω, Mute=ON	-	-90	-80	dB
Equivalent Input Noise Voltage	V <sub>NI</sub>	Rg=0Ω, BW:400Hz-22kHz	-	-100	-95	dBV
Total Harmonic Distortion1	THD1	BW:400Hz-22kHz, R <sub>L</sub> =32Ω	-	0.08	0.3	%
Total Harmonic Distortion2	THD2	BW:400Hz-22kHz, R <sub>L</sub> =10kΩ	-	0.007	0.05	%
Channel Separation1	CS1	Rg=600Ω, (*1)	65	75	-	dB
Channel Separation2	CS2	Rg=600Ω, f=10kHz, (*1)	55	65	-	dB
Output Offset Voltage	V <sub>OS</sub>	Rg=0Ω, Gv=12.4Db, No load	-	1	5	mV

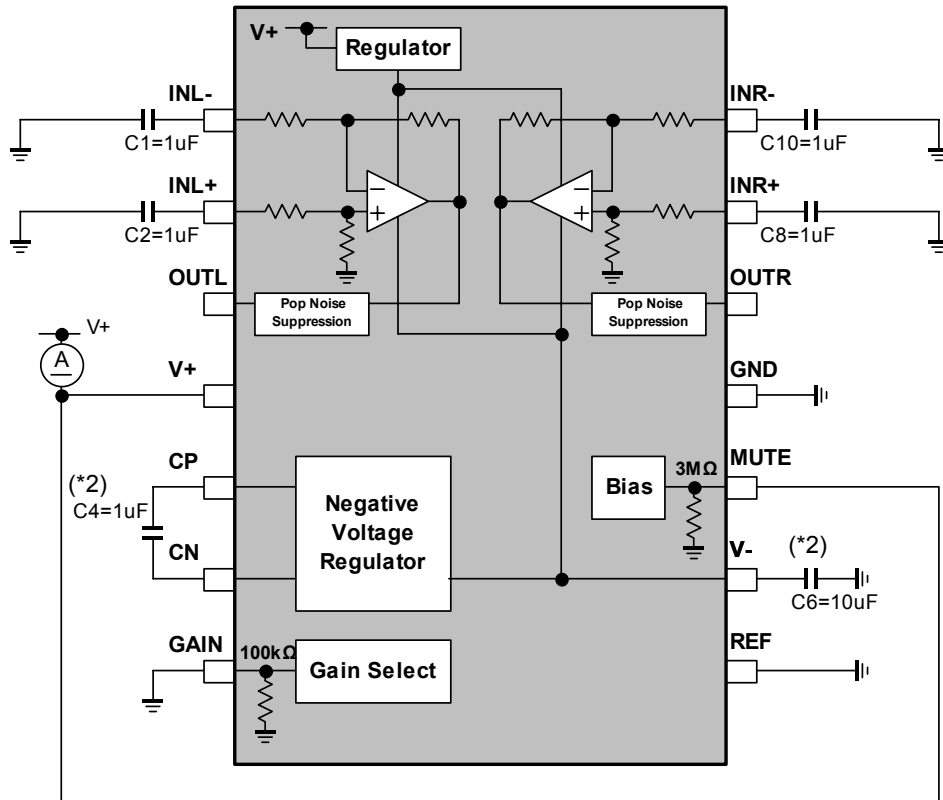
(\*1)OUTL(measured terminal): 20log(OUTR/OUTL), OUTR(measured terminal): 20log(OUTL/OUTR)

## ■ CONTROL CHARACTERISTICS

(Ta=25°C, V<sup>+</sup>=3.3V, Gv=6.4dB, MUTE=OFF, R<sub>L</sub>=32Ω unless otherwise specified)

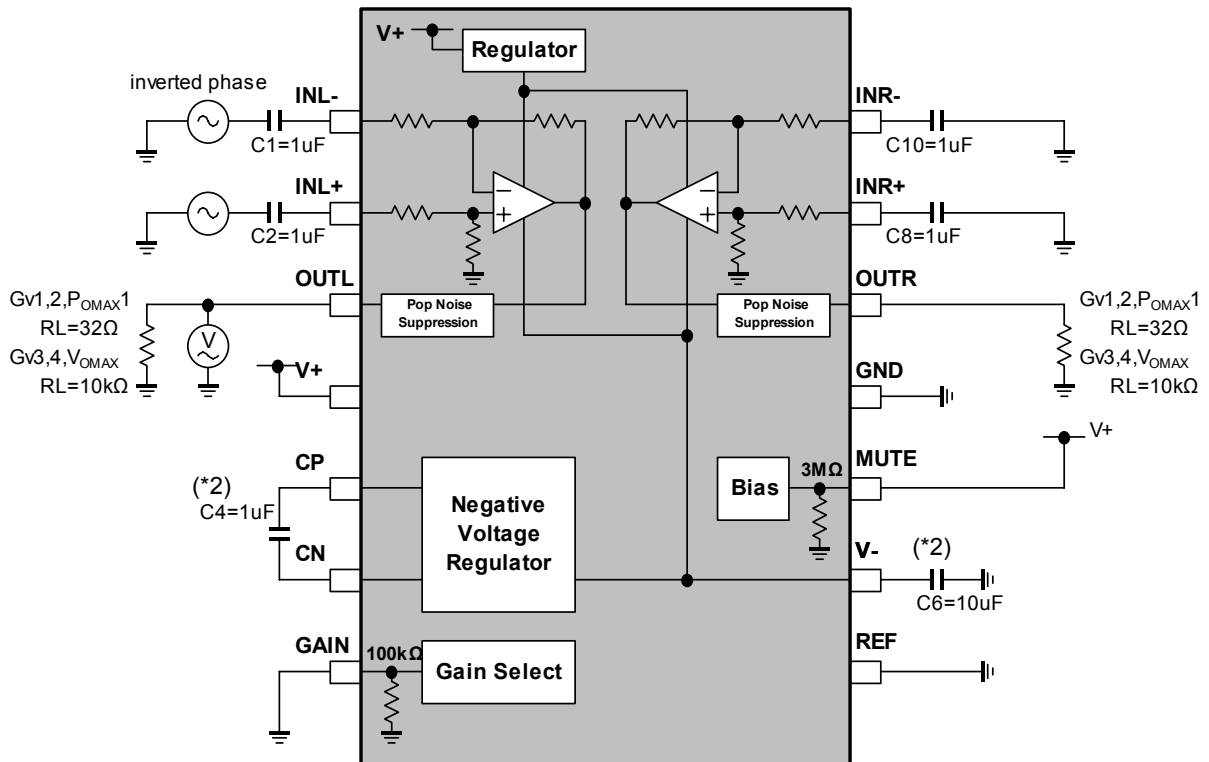
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Mute terminal High	MuteH	Mute=OFF	0.8 V <sup>+</sup>	-	V <sup>+</sup>	V
Mute terminal Low	MuteL	Mute=ON	0	-	0.2 V <sup>+</sup>	V
Gain terminal High	GainH	Gv=12.4dB	0.8 V <sup>+</sup>	-	V <sup>+</sup>	V
Gain terminal Low	GainL	Gv=6.4dB	0	-	0.2 V <sup>+</sup>	V

## ■ TEST CIRCUIT ( $I_{DD}$ )



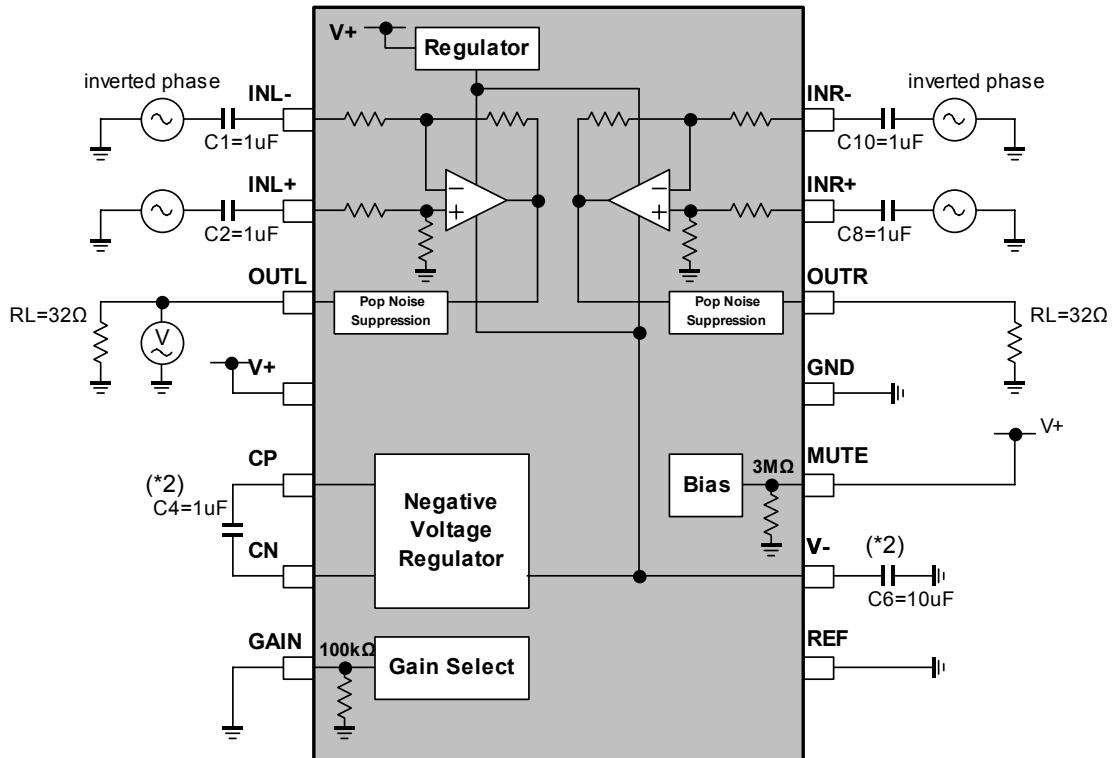
(\*2): Monolithic Ceramic Capacitors

## ■ TEST CIRCUIT ( $G_{V1}$ , $G_{V2}$ , $G_{V3}$ , $G_{V4}$ , $P_{OMAX1}$ , $V_{OMAX}$ )



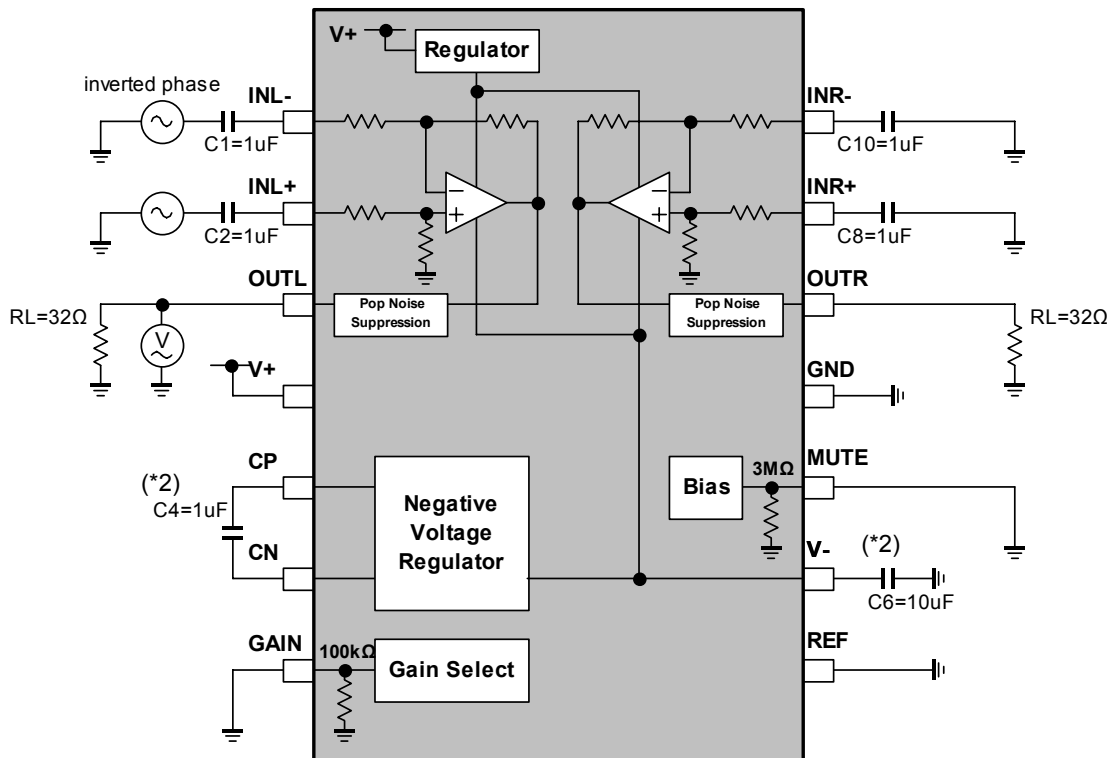
(\*2): Monolithic Ceramic Capacitors

## TEST CIRCUIT ( $P_{OMAX2}$ )



(\*2): Monolithic Ceramic Capacitors

## TEST CIRCUIT ( $V_{MUTE}$ )

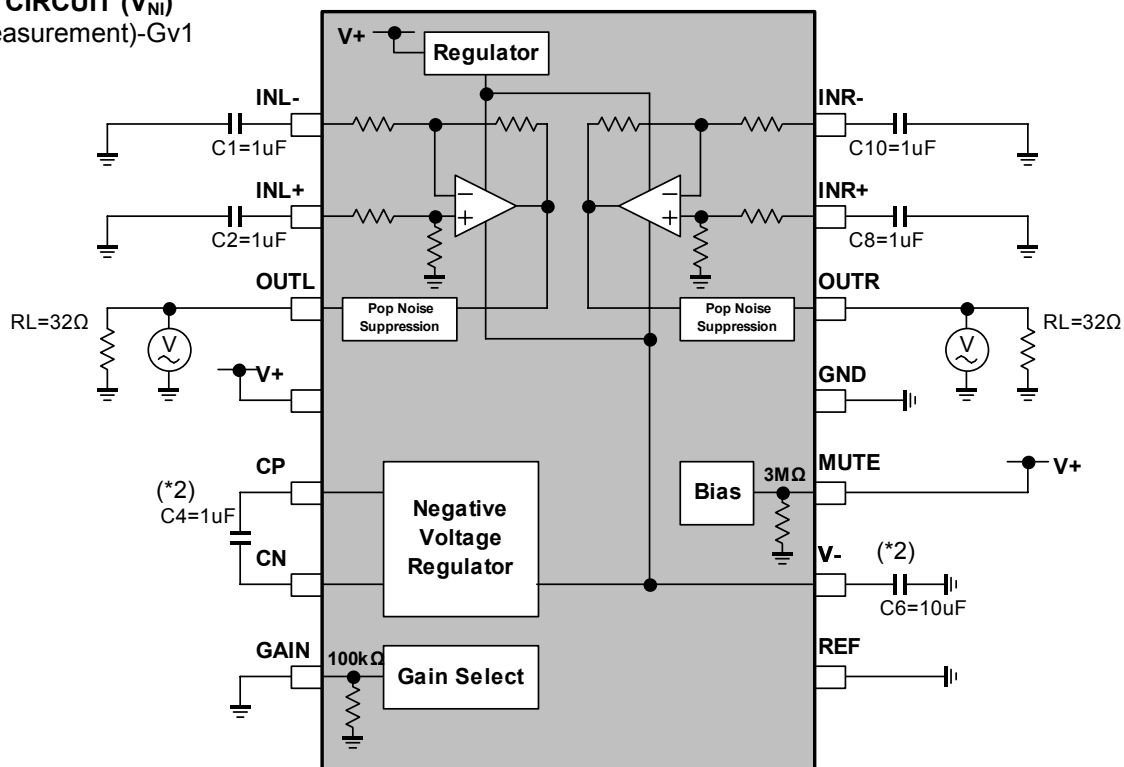


(\*2): Monolithic Ceramic Capacitors

# NJU72040

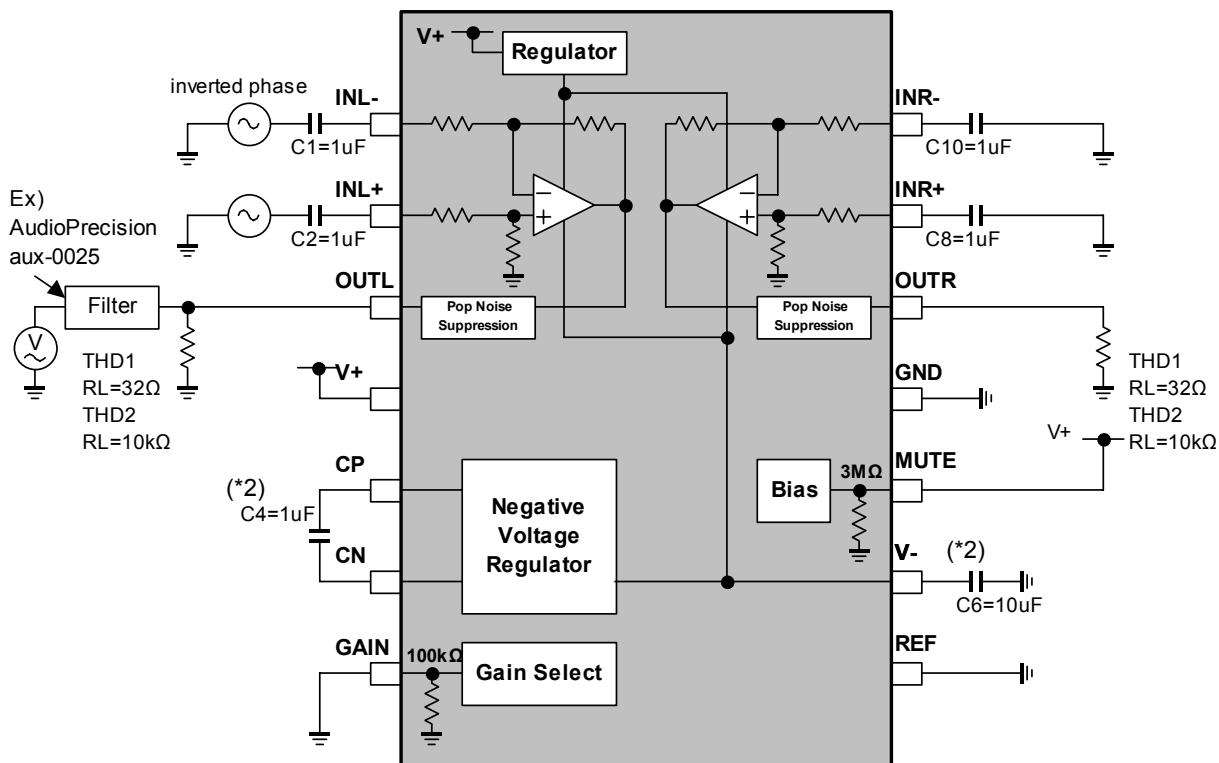
## TEST CIRCUIT (V<sub>NI</sub>)

$$V_{NI} = (\text{measurement}) - Gv1$$



(\*2): Monolithic Ceramic Capacitors

## TEST CIRCUIT (THD1, THD2)



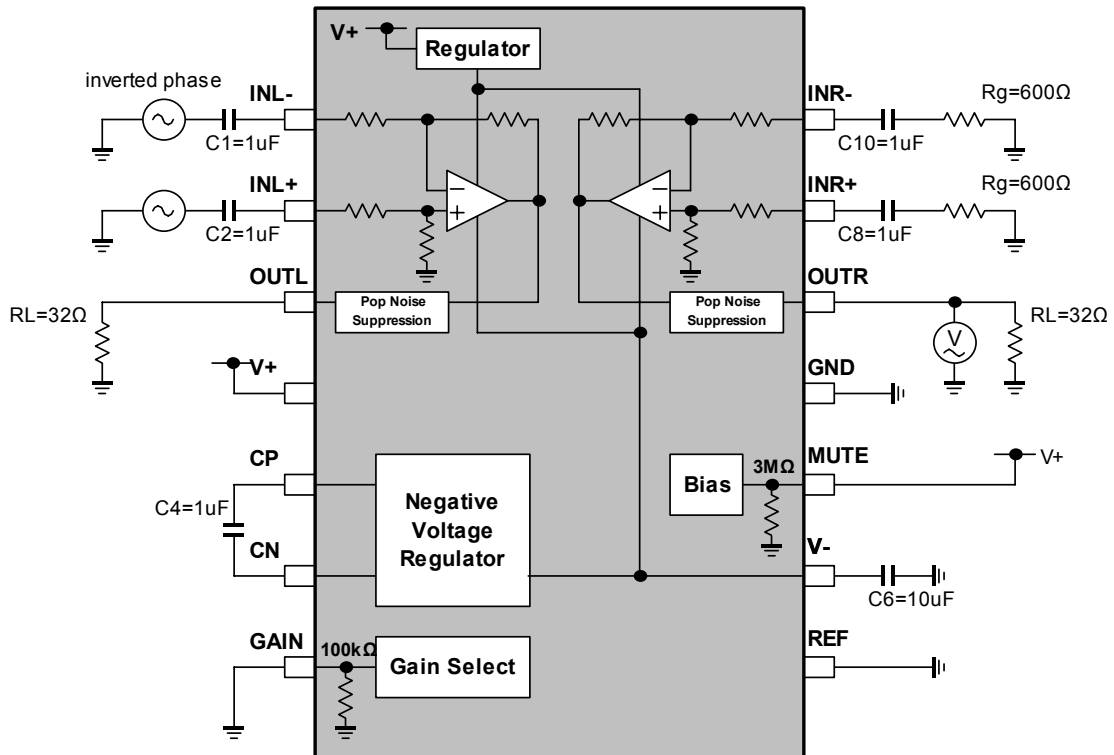
(\*2): Monolithic Ceramic Capacitors

(\*3): Connect a low-pass filter circuit with the corner frequency of more than 20kHz in front of an analyzer for rejecting the switching noise generated from NJU72040. Otherwise, the characteristic result may change because of the switching noise.

## TEST CIRCUIT (CS1, CS2)

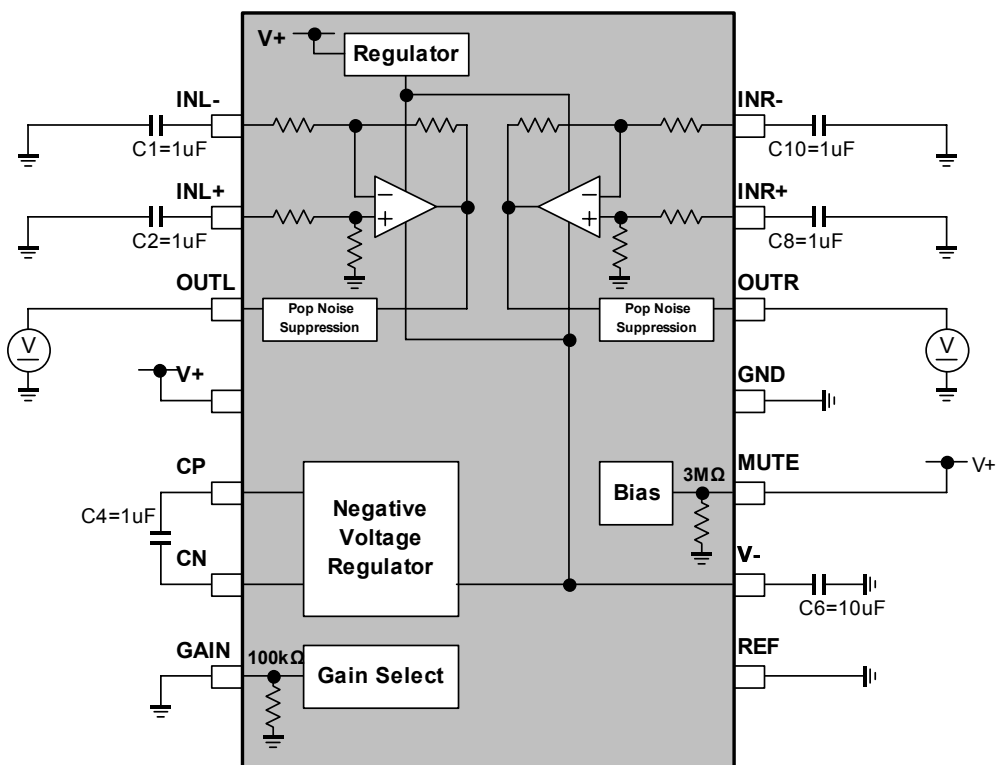
OUTL (measured terminal):  $CS1=CS2=20\log(OUTR/OUTL)$

OUTR (measured terminal):  $CS1=CS2=20\log(OUTL/OUTR)$



(\*2): Monolithic Ceramic Capacitors

## TEST CIRCUIT ( $V_{OS}$ )



(\*2): Monolithic Ceramic Capacitors

