450MHz Band LNA GaAs MMIC

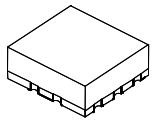
■GENERAL DESCRIPTION

NJG1128HB6 is a LNA IC designed for 450MHz band CDMA cellular phone. This IC has the function which bypasses LNA, and high gain mode or low gain mode can be chosen.

High IIP3 and a low noise are achieved at the High gain mode. And low current consumption can be achieved at the low gain mode because LNA enters the state of the standby.

A small and thin package of USB8 is adopted.

■PACKAGE OUTLINE



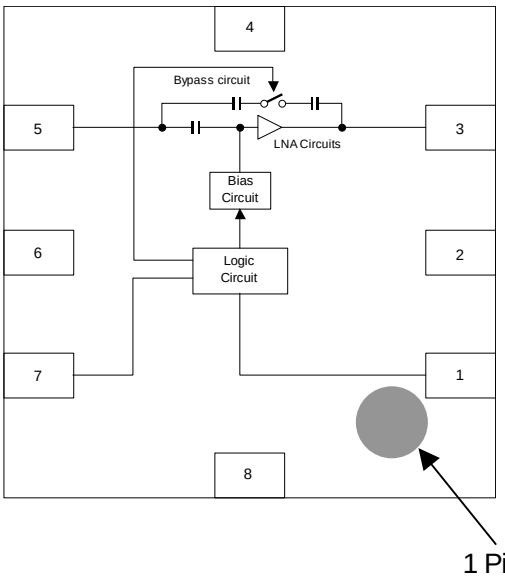
NJG1128HB6

■FEATURES

●Low voltage operation	+2.8V typ.	
●Low control voltage operation	+1.85V typ.	
[LNA High Gain Mode]		
●High Input IP3	+11.0dBm typ.	@ f=460-470MHz
●Low noise figure	1.4dB typ.	@ f=460-470MHz
[LNA Low Gain Mode]		
●Low current consumption	15uA typ.	
●High Input IP3	+21.0dBm typ.	@ f=460-470MHz
●Small & thin package	USB8-B6 (Package size: 1.5mm x1.5mm x 0.55mm typ.)	

■PIN CONFIGURATION

(Top View)



Pin Connection
1.V_{INV}
2.GND
3.RF OUT
4.GND
5.RF IN
6.GND
7. V_{CTL}
8. GND

Note: Specifications and description listed in this catalog are subject to change without prior notice.

■ABSOLUTE MAXIMUM RATINGS

(T_a=+25℃, Z_S=Z_l=50Ω)

PARAMETERS	SYMBOL	CONDITIONS	RATINGS	UNITS
Supply voltage	V_{DD}		5.0	V
Inverter supply voltage	V_{INV}		5.0	V
Control voltage	V_{CTL}		5.0	V
Input power	P_{in}		+15	dBm
Power dissipation	P_D	on PCB board, at Tjmax=150℃	160	mW
Operating temperature	T_{opr}		-40~+85	℃
Storage temperature	T_{stg}		-55~+150	℃

■ELECTRICAL CHARACTERISTICS 1 (DC CHARACTERISTICS)

(General Conditions: V_{DD}=V_{INV}=2.8V, T_a=+25℃, Z_S=Z_l=50Ω)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating voltage	V_{DD}		2.65	2.80	2.95	V
Inverter supply voltage	V_{INV}		2.65	2.80	2.95	V
Control voltage (High)	V_{CTL}(H)		1.80	1.85	V_{DD+}0.3	V
Control voltage (Low)	V_{CTL}(L)		-0.3	0	0.3	V
Operating current1 (LNA High Gain Mode)	I_{DD}1	RF OFF, V_{CTL}=1.85V	-	10.0	16.0	mA
Operating current2 (LNA Low Gain Mode)	I_{DD}2	RFOFF, V_{CTL}=0V	-	1	5	uA
Inverter current1 (LNA High Gain Mode)	I_{INV}1	RF OFF, V_{CTL}=1.85V	-	150	240	uA
Inverter current2 (LNA Low Gain Mode)	I_{INV}2	RF OFF, V_{CTL}=0V	-	15	40	uA
Control current	I_{CTL}	RF OFF, V_{CTL}=1.85V	-	5	15	uA

■**ELECTRICAL CHARACTERISTICS 2 (LNA High Gain Mode)**

(General Conditions: V_{DD}=V_{INV}=2.8V, V_{CTL}=1.85V, f_{RF}=460-470MHz, T_a=+25℃, Z_s=Z_l=50Ω)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Small signal gain1	Gain1		13.5	15.0	17.0	dB
Noise figure1	NF1	Exclude PCB & connector losses	-	1.4	1.8	dB
1dB gain compression output power1	P-1dB_1		+4.0	+9.0	-	dBm
3rd order Input Intercept Point1	IIP3_1	f1=f_{RF}, f2=f_{RF}+100kHz, P_{in}=-25dBm	+8.0	+11.0	-	dBm
RF IN VSWR1	$VSWR_i$_1		-	1.5	2.0	
RF OUT VSWR1	$VSWR_o$_1		-	2.3	2.7	

■**ELECTRICAL CHARACTERISTICS 3 (LNA Low Gain Mode)**

(General Conditions: V_{DD}=V_{INV}=2.8V, V_{CTL}=0V, f_{RF}=460-470MHz, T_a=+25℃, Z_s=Z_l=50Ω)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Small signal gain2	Gain2		-5.0	-3.0	0	dB
Noise figure2	NF2	Exclude PCB & connector losses	-	3.0	4.5	dB
1dB gain compression output power2	P-1dB_2		+1.0	+8.0	-	dBm
3rd order Input Intercept Point2	IIP3_2	f1=f_{RF}, f2=f_{RF}+100kHz, P_{in}=-12dBm	+15.0	+21.0	-	dBm
RF IN VSWR2	$VSWR_i$_2		-	2.3	2.7	
RF OUT VSWR2	$VSWR_o$_2		-	1.5	2.0	

■TERMINAL INFOMATION

No.	SYMBOL	DESCRIPTION
1	VINV	Supply voltage terminal for internal logic circuit (inverter).
2	GND	Ground terminal.
3	RFOUT	RF signal comes out from this terminal, and goes through an external matching circuit connected to this. Inductor L3 as shown in the application circuit is a part of an external matching circuit, and also provide DC power to LNA. Capacitor C3 as shown in the application circuit is a bypass capacitor.
4	GND	Ground terminal.
5	RFIN	RF input terminal. The RF signal is input through external matching circuit connected to this terminal. A DC blocking capacitor is not required.
6	GND	Ground terminal.
7	VCTL	Control port. A logic control signal is required to select High or Low gain mode of LNA. This terminal is set to more than +1.8V of logical high level for High gain mode of LNA, and set to –0.3~+0.3V of logical low level for Low gain mode.
8	GND	Ground terminal.

CAUTION

1) Ground terminal (No.2, 4, 6, 8) should be connected to the ground plane as close as possible for excellent RF performance, because distance to GND makes parasitic inductance.

■TRUTH TABLE

"H"=V_{CTL}(H), "L"=V_{CTL}(L)

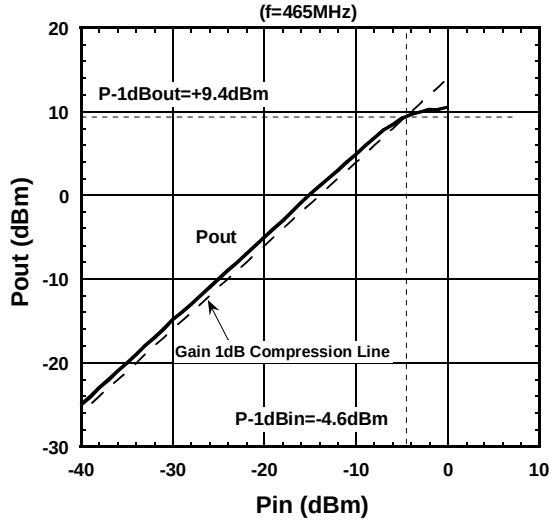
V_{CTL}	Gain Mode	LNA
L	Low	bypass
H	High	pass

■ELECTRICAL CHARACTERISTICS (LNA High Gain Mode)

(General Conditions: Ta=+25℃, V_{DD}=V_{INV}=2.8V, V_{CTL}=1.85V, Zs=Zl=50Ω)

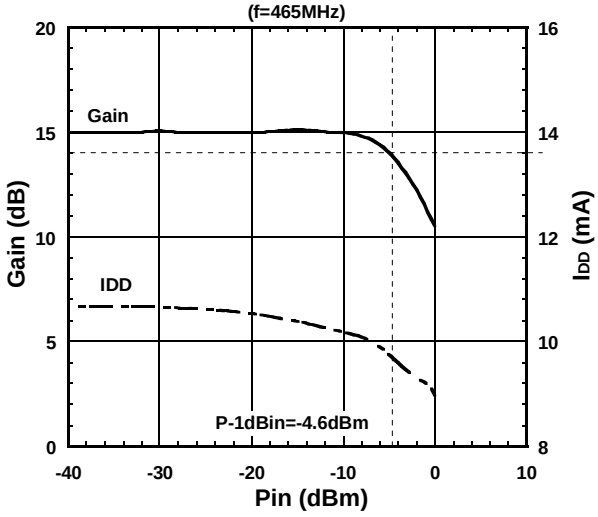
Pout vs. Pin

(f=465MHz)



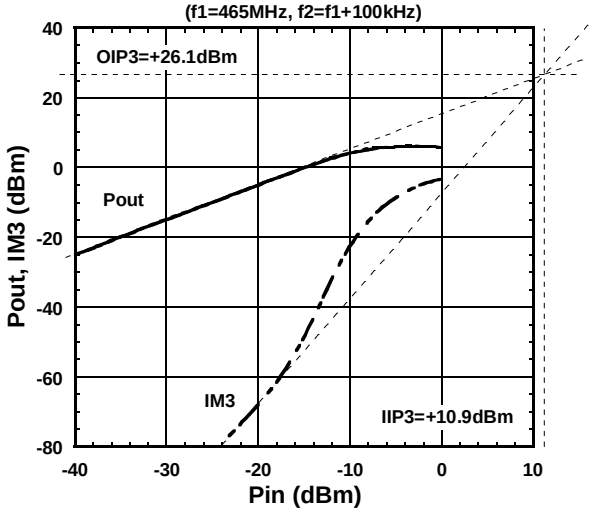
Gain, I_{DD} vs. Pin

(f=465MHz)



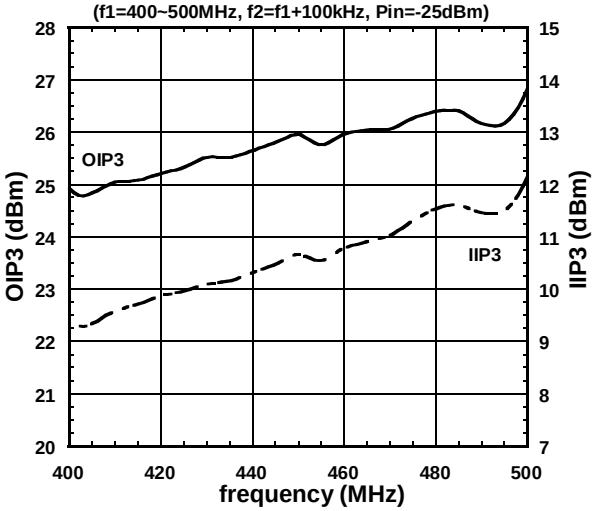
Pout, IM3 vs. Pin

(f1=465MHz, f2=f1+100kHz)



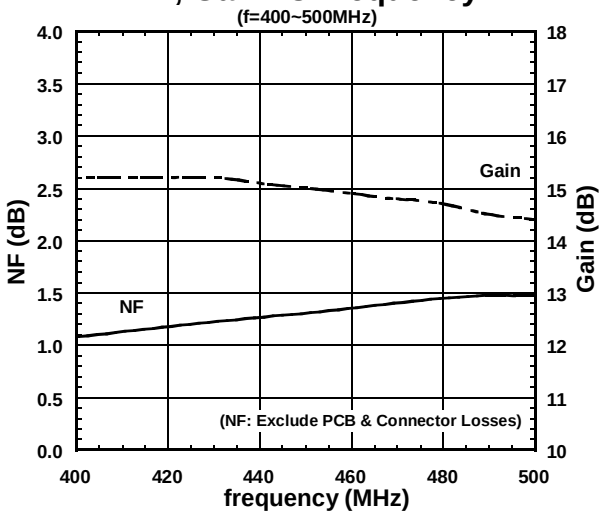
OIP3, IIP3 vs. frequency

(f1=400~500MHz, f2=f1+100kHz, Pin=-25dBm)



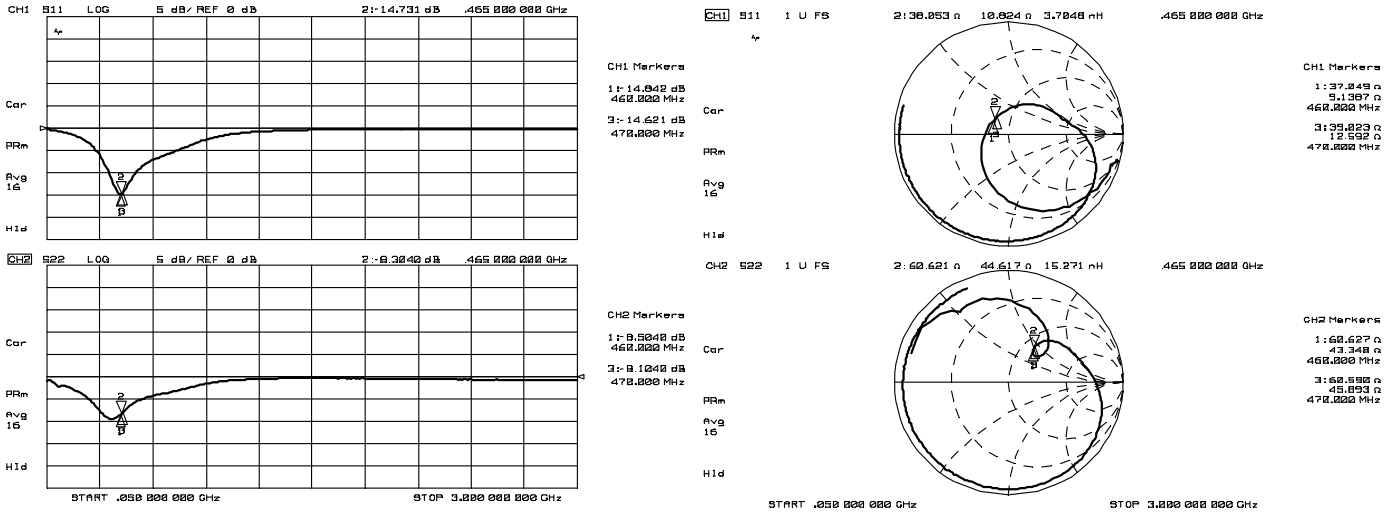
NF, Gain vs. frequency

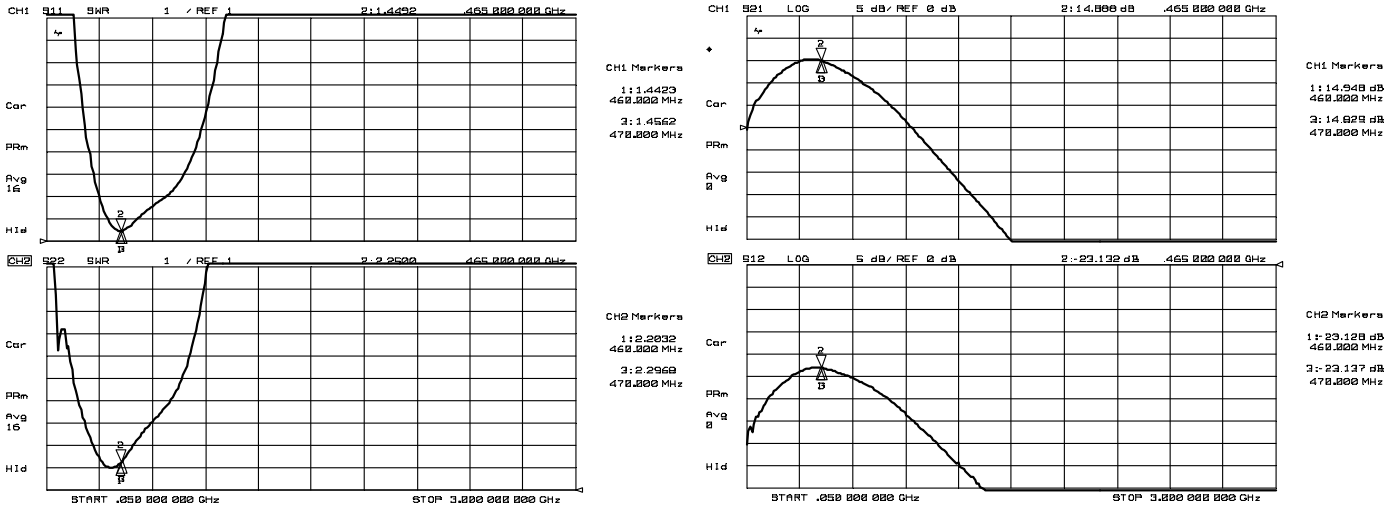
(f=400~500MHz)

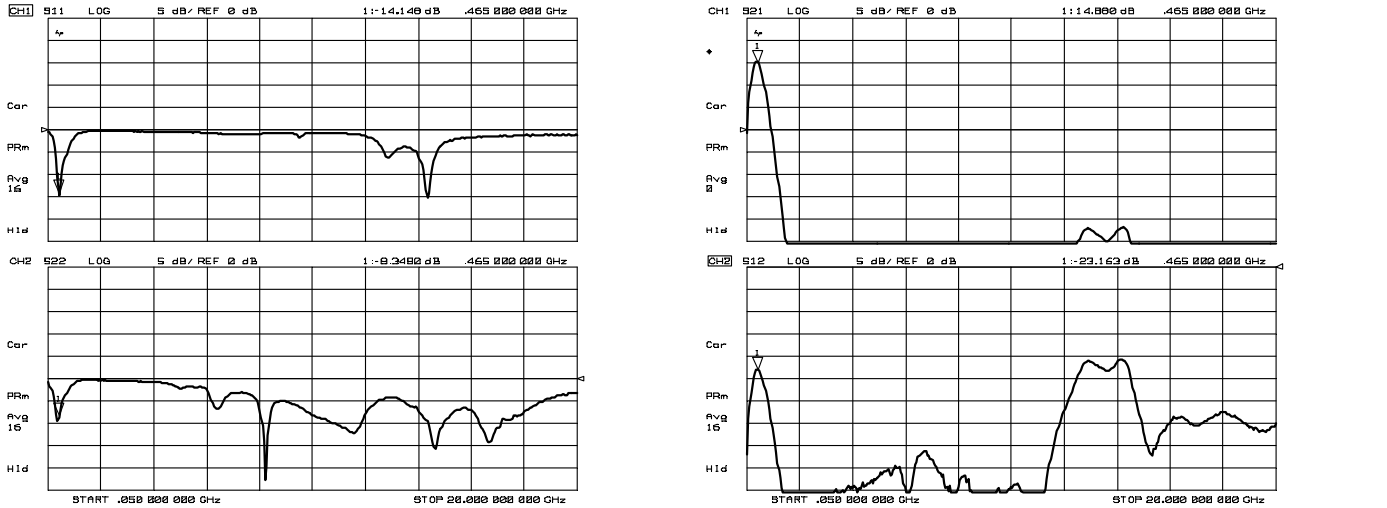


■ELECTRICAL CHARACTERISTICS (LNA High Gain Mode)

(General Conditions: Ta=+25℃, V_{DD}=V_{INV}=2.8V, V_{CTL}=1.85V, Zs=Zl=50Ω)



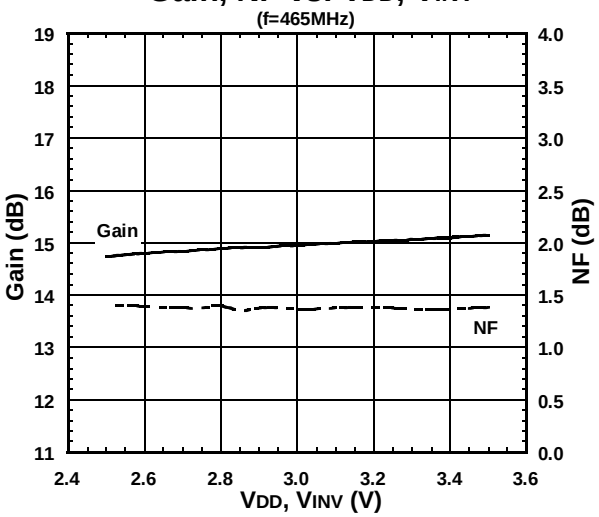




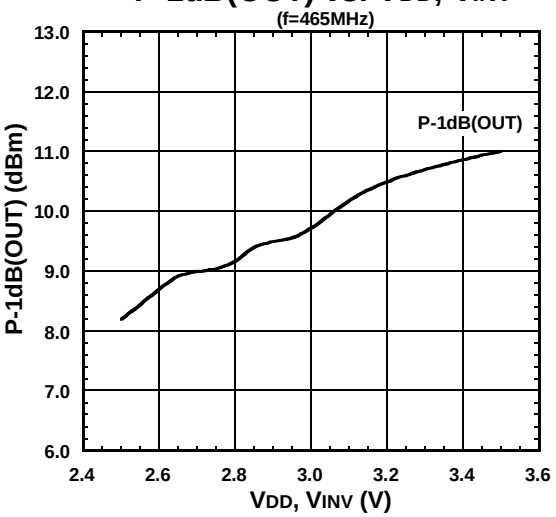
■ELECTRICAL CHARACTERISTICS (LNA High Gain Mode)

(General Conditions: Ta=+25℃, V_{DD}=V_{INV}=2.8V, V_{CTL}=1.85V, Zs=Zl=50Ω)

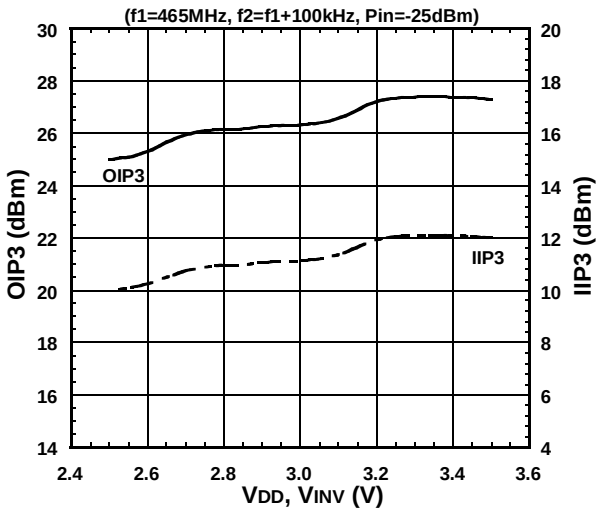
Gain, NF vs. VDD, VINV



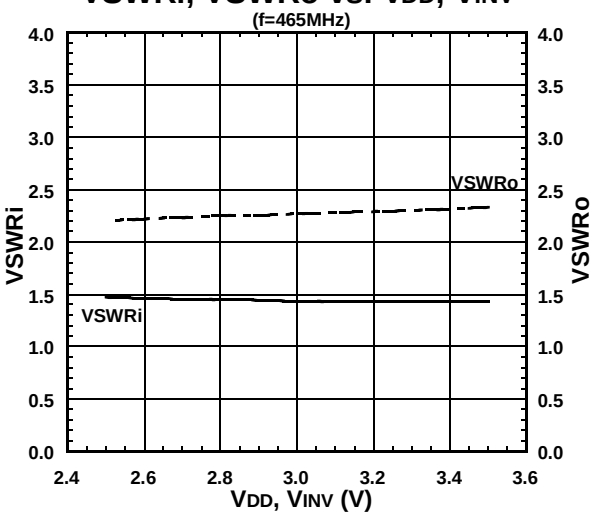
P-1dB(OUT) vs. VDD, VINV



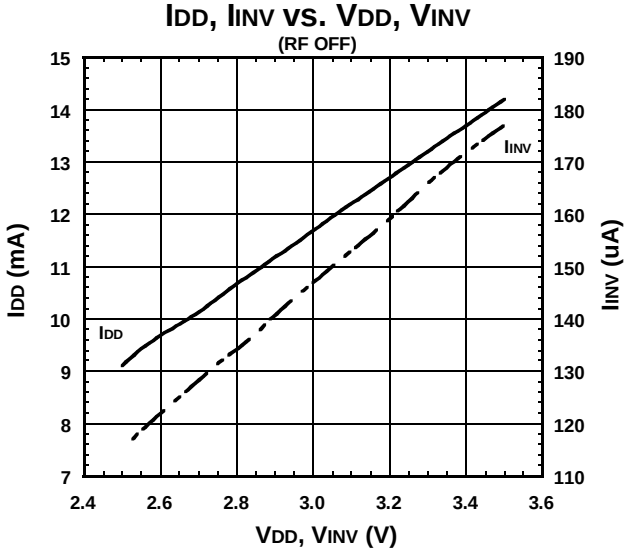
OIP3, IIP3 vs. VDD, VINV



VSWRi, VSWRo vs. VDD, VINV



IDD, IINV vs. VDD, VINV

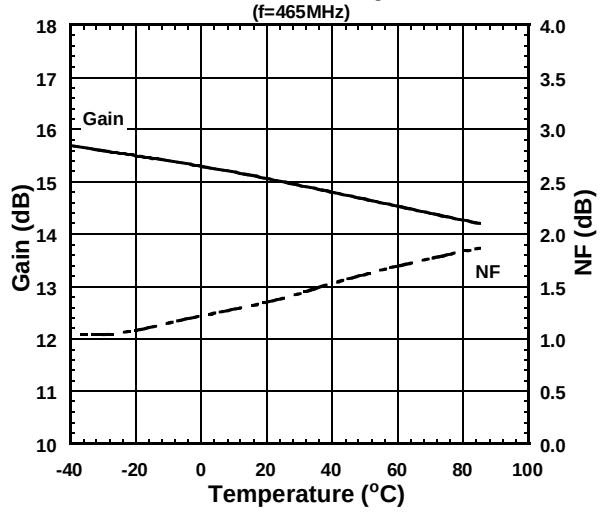


■ELECTRICAL CHARACTERISTICS (LNA High Gain Mode)

(General Conditions: Ta=+25℃, V_{DD}=V_{INV}=2.8V, V_{CTL}=1.85V, Zs=Zl=50Ω)

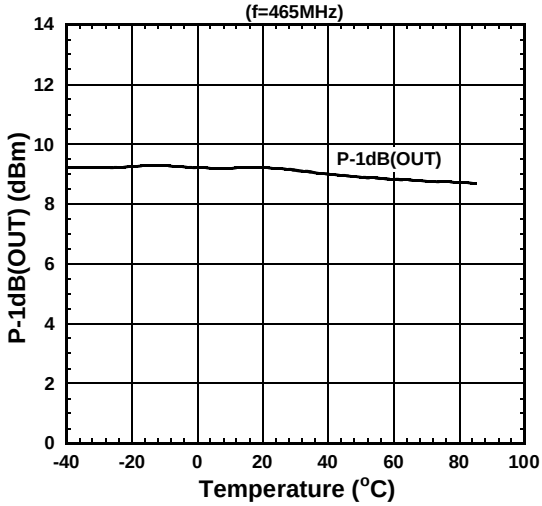
Gain, NF vs. Temperature

(f=465MHz)



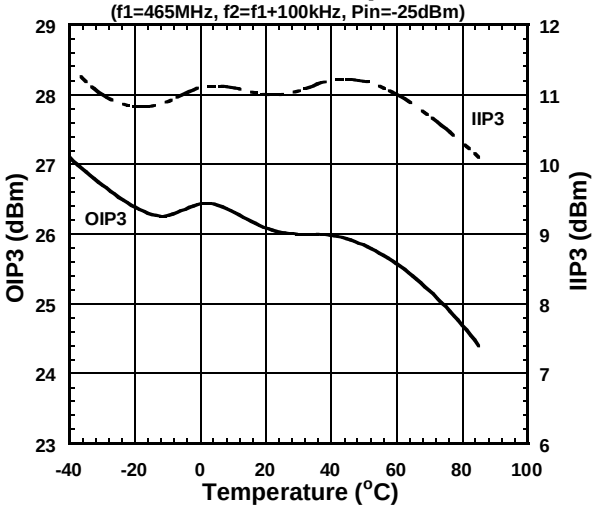
P-1dB(OUT) vs. Temperature

(f=465MHz)



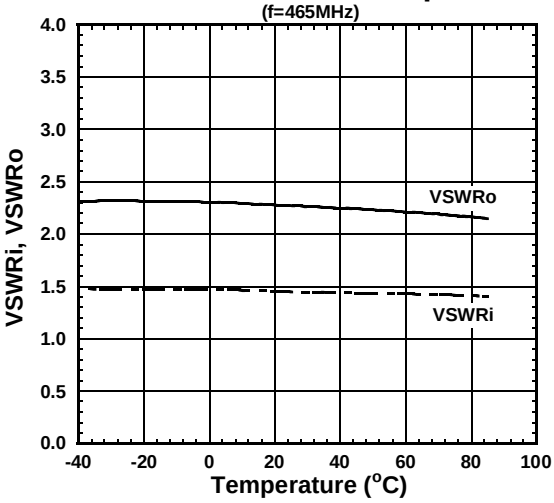
OIP3, IIP3 vs. Temperature

(f1=465MHz, f2=f1+100kHz, Pin=-25dBm)



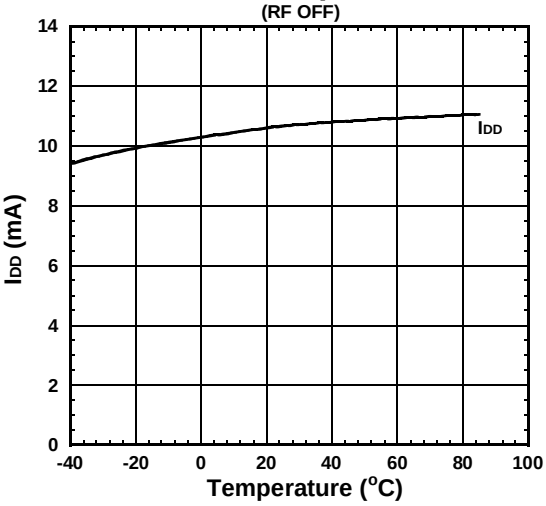
VSWRi, VSWRo vs. Temperature

(f=465MHz)



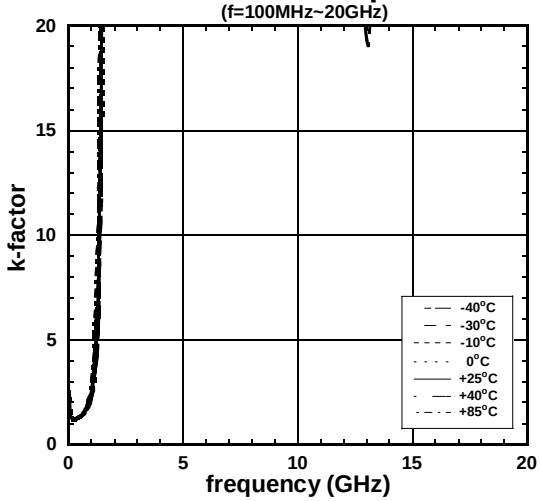
I_{DD} vs. Temperature

(RF OFF)



k-factor vs. Temperature

(f=100MHz~20GHz)

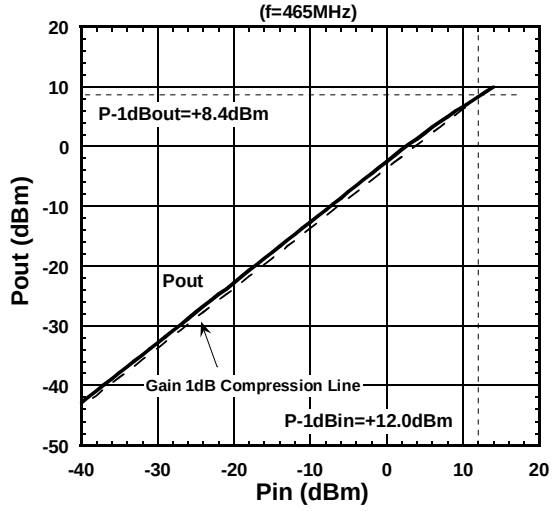


■ELECTRICAL CHARACTERISTICS (LNA Low Gain Mode)

(General Conditions: Ta=+25℃, V_{DD}=V_{INV}=2.8V, V_{CTL}=0V, Zs=Zl=50Ω)

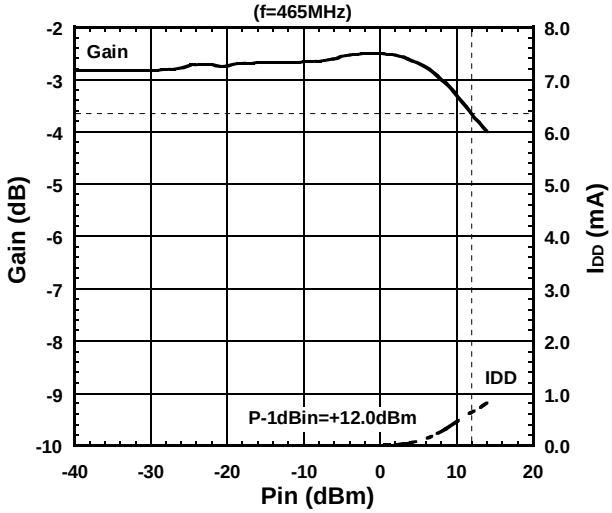
Pout vs. Pin

(f=465MHz)



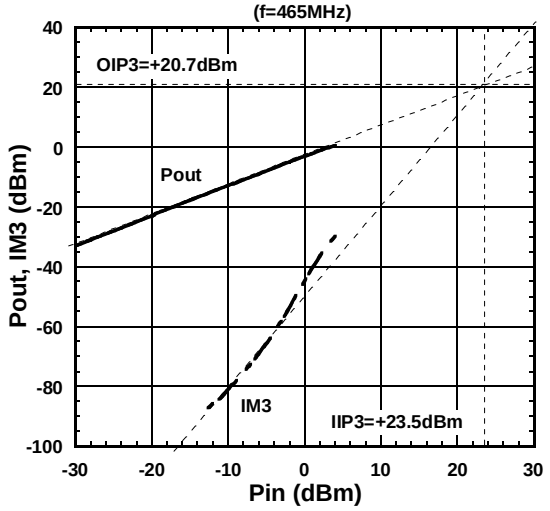
Gain, I_{DD} vs. Pin

(f=465MHz)



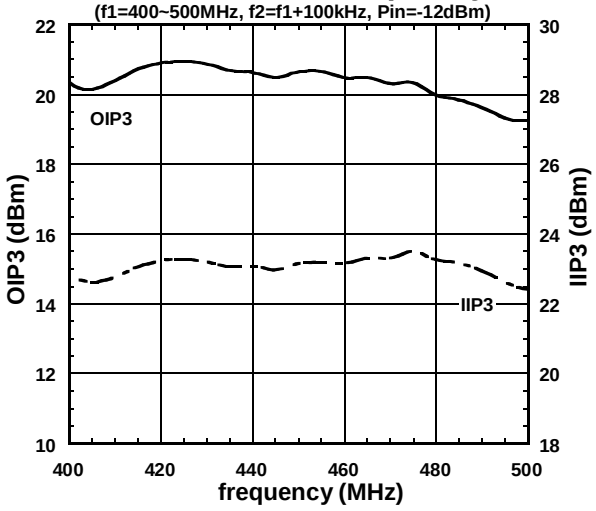
Pout, IM3 vs. Pin

(f=465MHz)



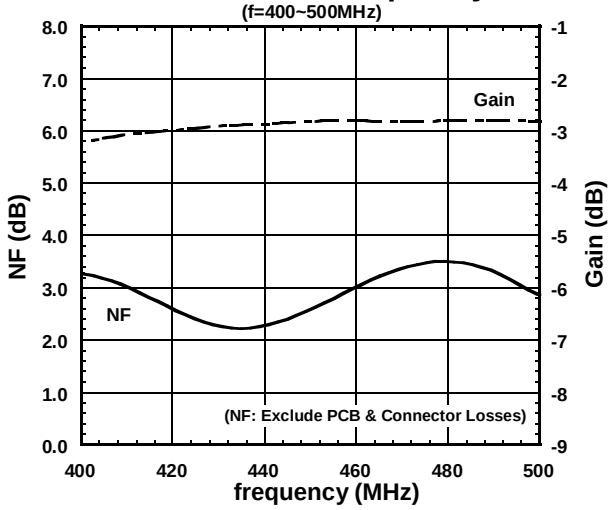
OIP3, IIP3 vs. frequency

(f1=400~500MHz, f2=f1+100kHz, Pin=-12dBm)



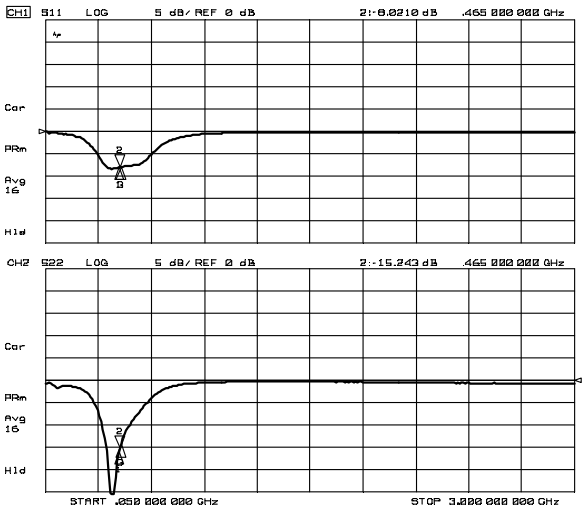
NF, Gain vs. frequency

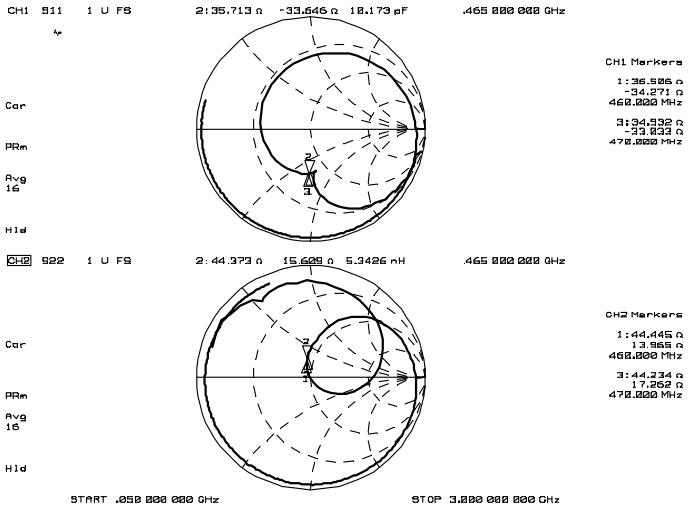
(f=400~500MHz)

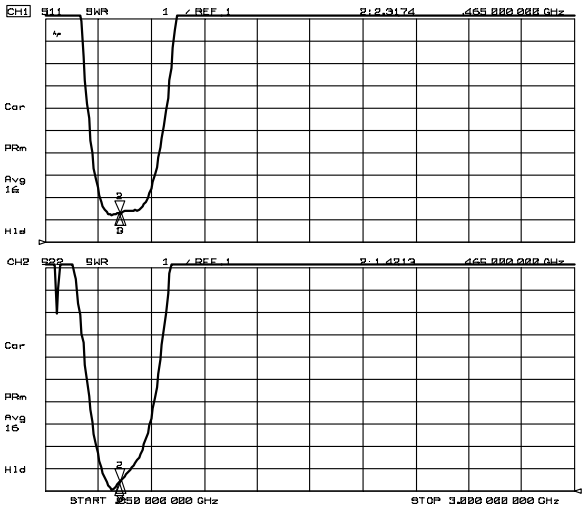


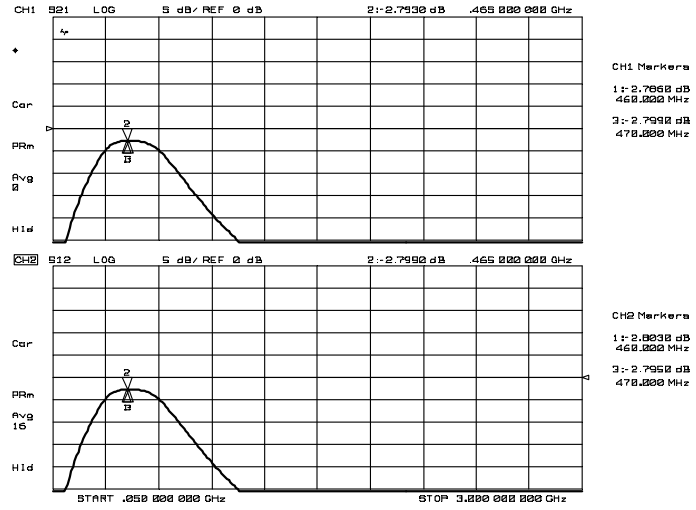
■ELECTRICAL CHARACTERISTICS (LNA Low Gain Mode)

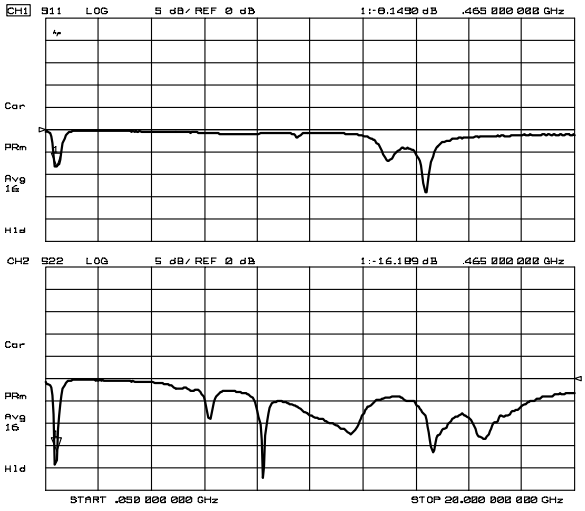
(General Conditions: Ta=+25℃, V_{DD}=V_{INV}=2.8V, V_{CTL}=0V, Zs=Zl=50Ω)

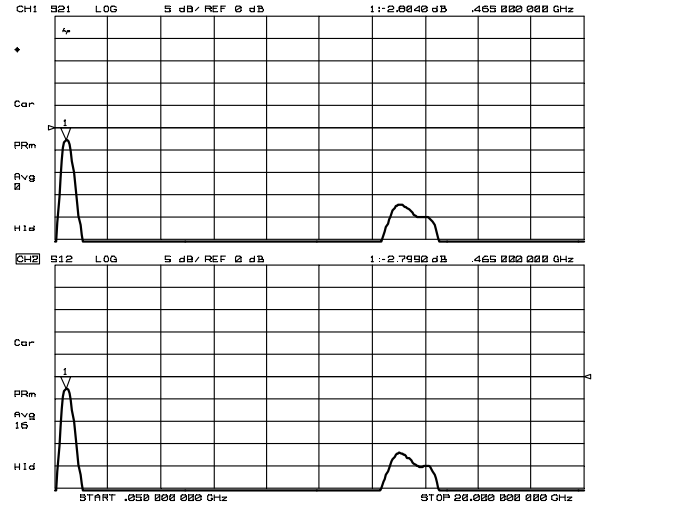








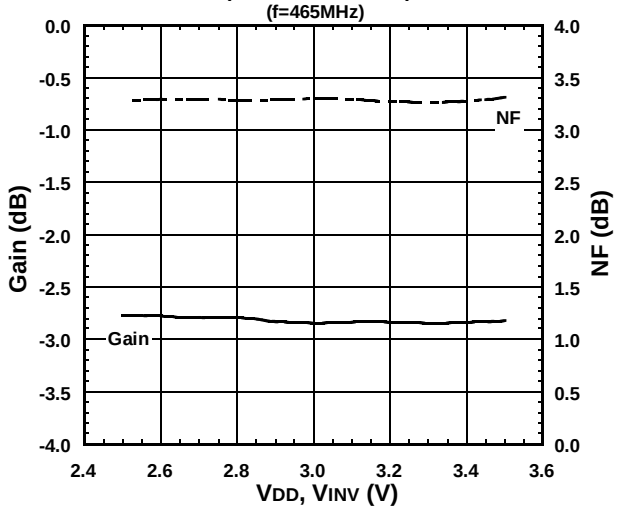




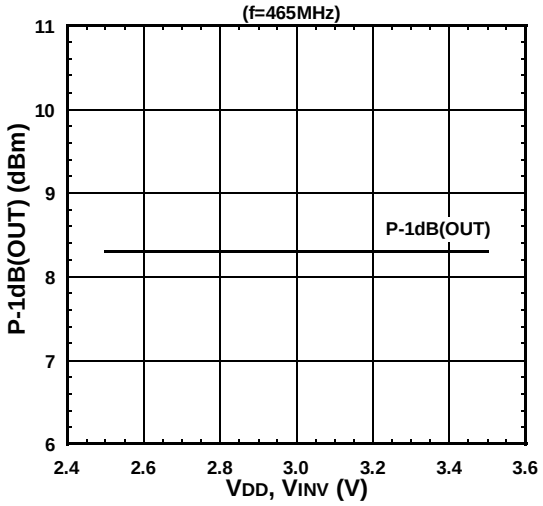
■ELECTRICAL CHARACTERISTICS (LNA Low Gain Mode)

(General Conditions: Ta=+25℃, V_{DD}=V_{INV}=2.8V, V_{CTL}=0V, Zs=Zl=50Ω)

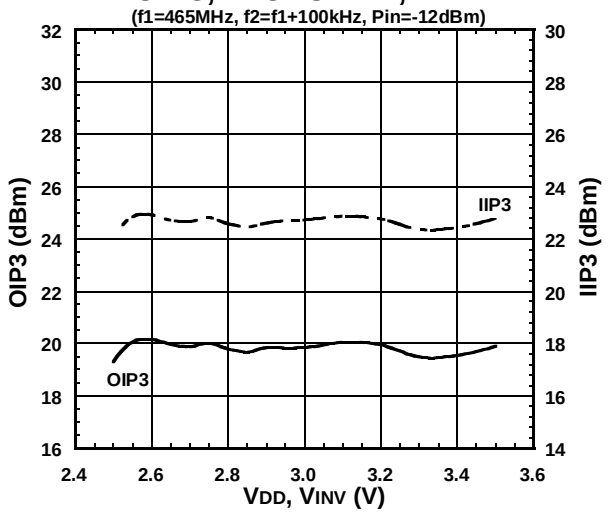
Gain, NF vs. VDD, VINV



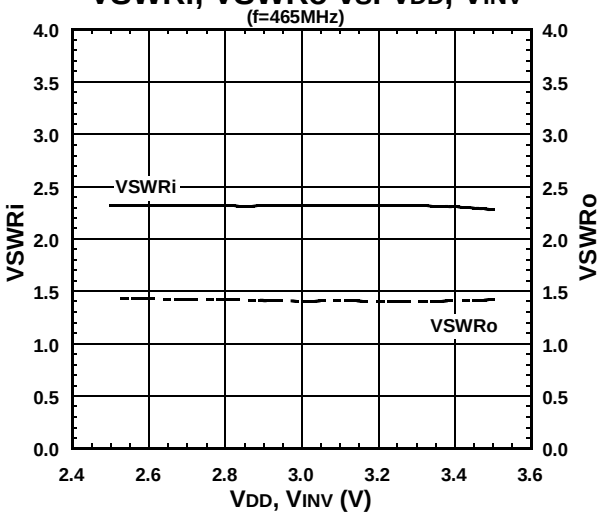
P-1dB(OUT) vs. VDD, VINV



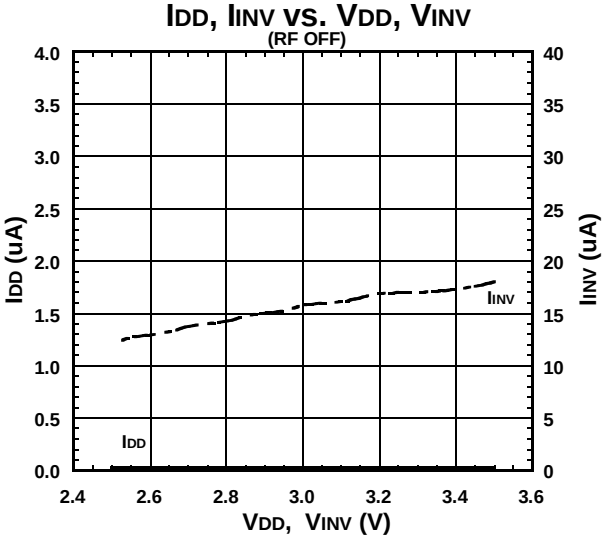
OIP3, IIP3 vs. VDD, VINV



VSWRi, VSWRo vs. VDD, VINV



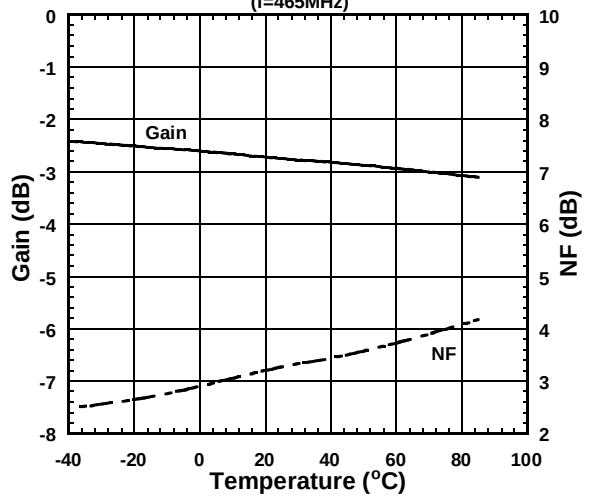
IDD, IINV vs. VDD, VINV



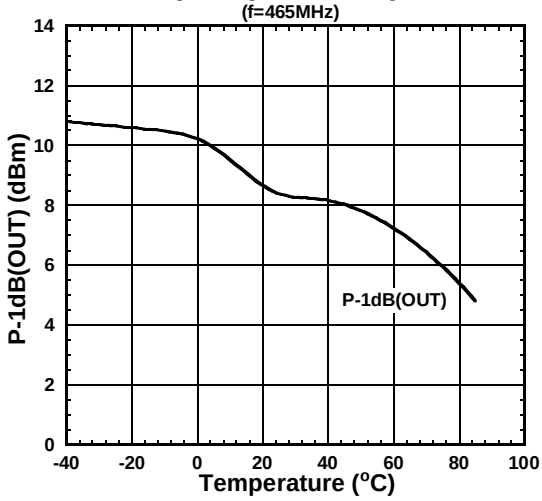
■ELECTRICAL CHARACTERISTICS (LNA Low Gain Mode)

(General Conditions: Ta=+25℃, V_{DD}=V_{INV}=2.8V, V_{CTL}=0V, Zs=Zl=50Ω)

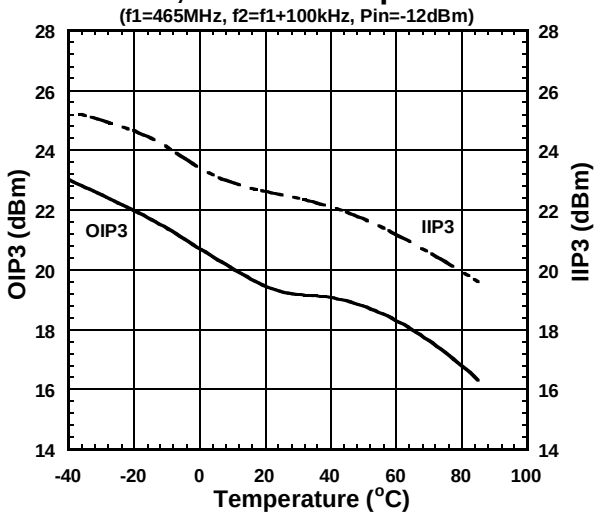
Gain, NF vs. Temperature



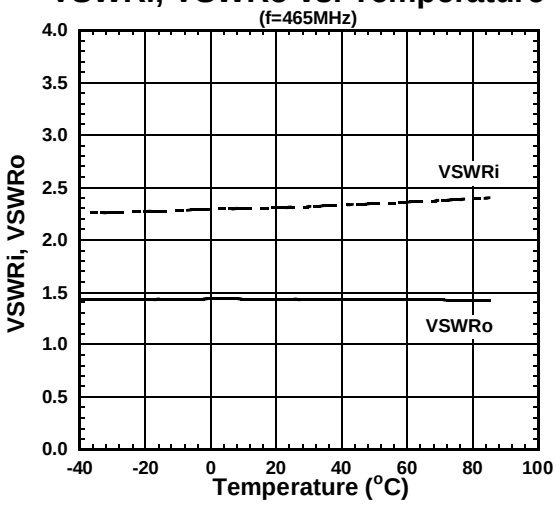
P-1dB(OUT) vs. Temperature



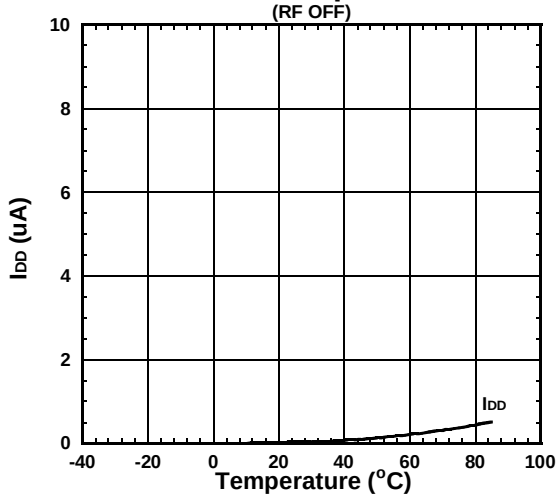
OIP3, IIP3 vs. Temperature



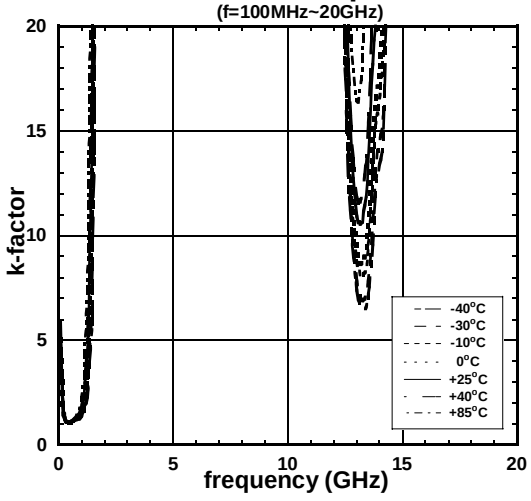
VSWRi, VSWRo vs. Temperature



I_{DD} vs. Temperature

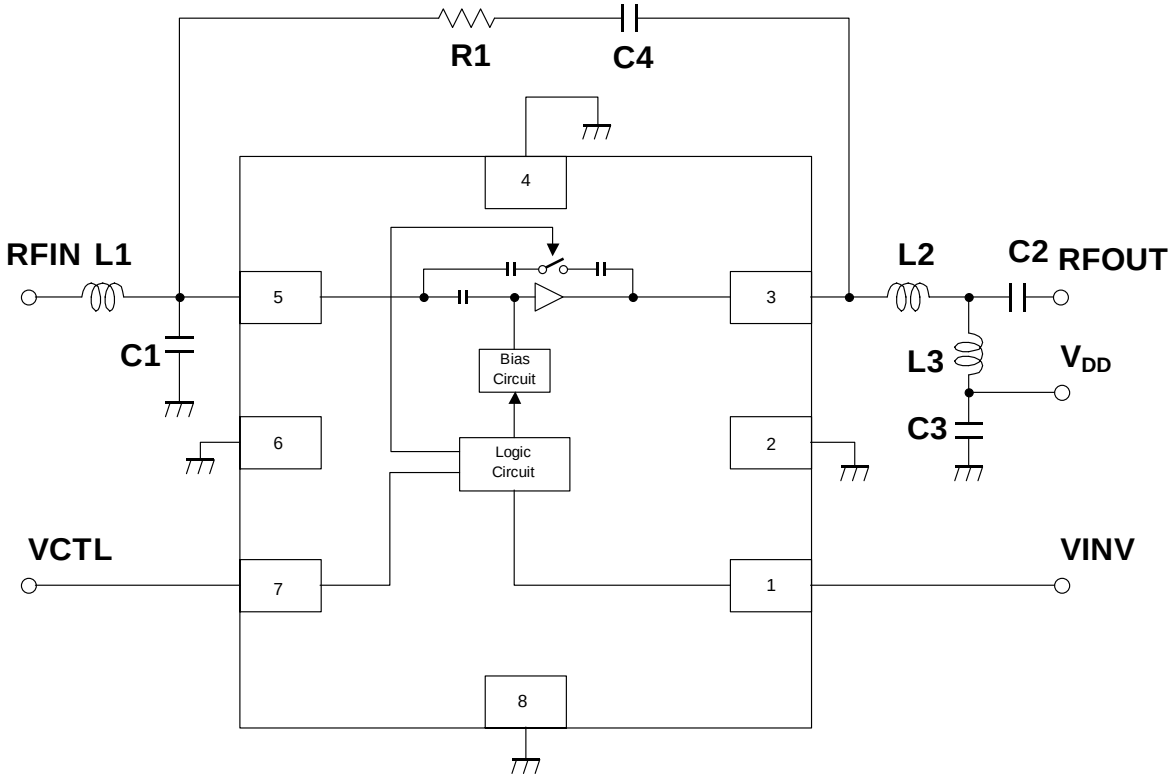


k-factor vs. Temperature



■APPLICATION CIRCUIT

(TOP VIEW)

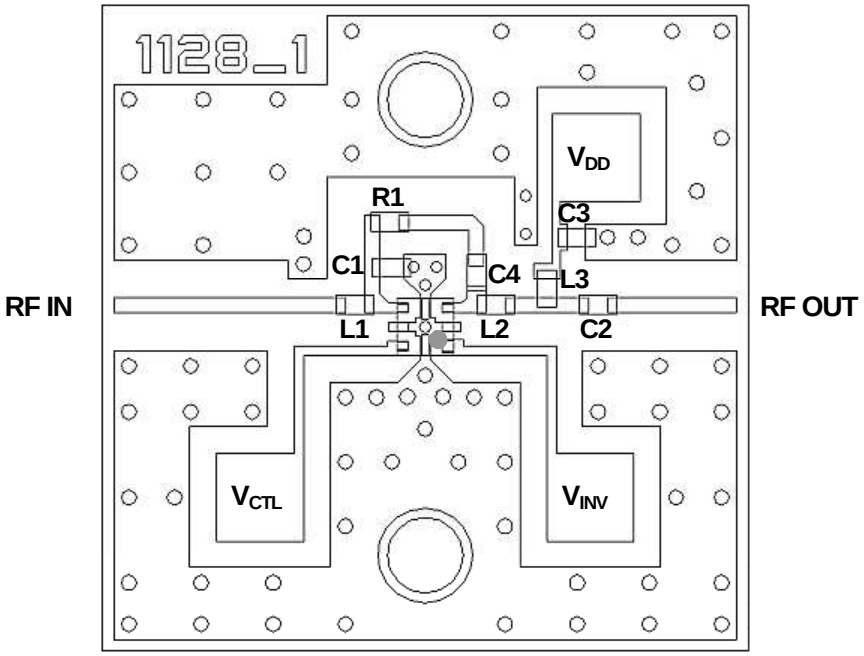


Parts List

PART ID	CONSTANTS	COMMENT
L1	27nH	MURATA (LQW15A)
L2	33nH	TAIYO-YUDEN (HK1005)
L3	33nH	TAIYO-YUDEN (HK1005)
C1	0.75pF	MURATA (GRM15)
C2	1000pF	MURATA (GRM15)
C3	1000pF	MURATA (GRM15)
C4	2pF	MURATA (GRM15)
R1	2.7kΩ	1005size

■TEST PCB LAYOUT

(Top View)

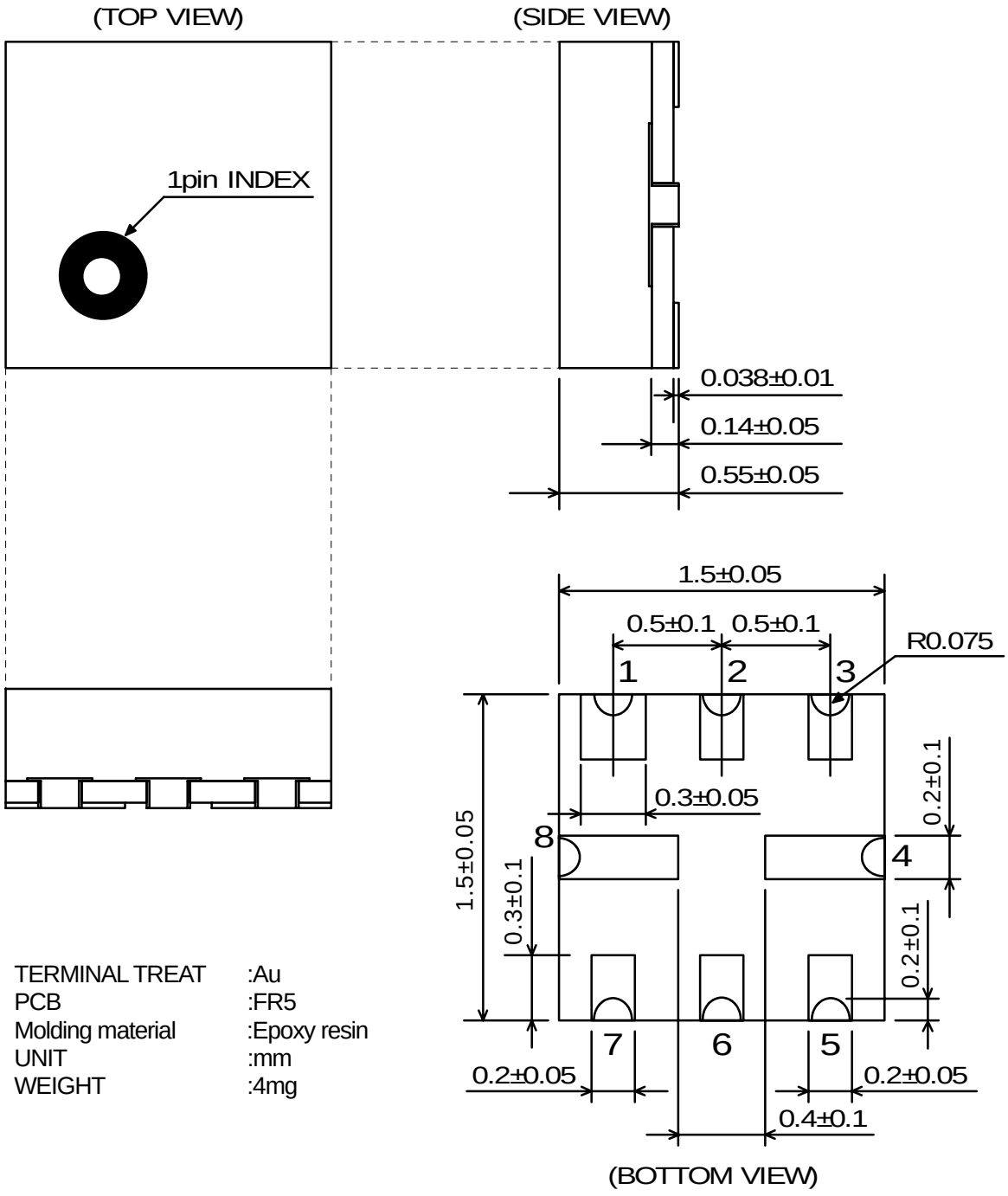


PCB(FR-4),t=0.2mm
MICROSTRIP LINE WIDTH=0.4mm(Z_O=50Ω)
PCB SIZE : 17.0 X 17.0mm

PRECAUTIONS

[1] C1 and L1 form the input matching circuit. They should be placed close to RFIN terminal (5th pin).
[2] L2 and L3 form the output matching circuit. They should be placed close to RFOUT terminal (3rd pin).
[3] R1 and C4 form the negative feedback circuit. The pattern between RFOUT terminal (3rd pin) and RFIN terminal (5th pin) should be designed as short as possible for good performance.
[4] C2 is a DC-blocking capacitor.
[5] C3 is a bypass capacitor, it should be placed close to L3.
[6] Ground terminals(2nd, 4th, 6th and 8th pin) should be connected to ground plane as close as possible for good performance.

■**PACKAGE OUTLINE** (USB8-B6)



TERMINAL TREAT	:Au
PCB	:FR5
Molding material	:Epoxy resin
UNIT	:mm
WEIGHT	:4mg

Cautions on using this product

This product contains Gallium-Arsenide (GaAs) which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.