PRELIMINARY

1/4 DUTY LCD DRIVER

■ GENERAL DESCRIPTION

The NJU6434 is a 1/4 duty LCD driver for segment type LCD panel.

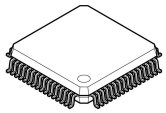
The LCD driver consists of 4-common and 50-segment drives up to 200 segments.

The NJU6434 is useful for the digital tuning system or others segment type display driver.

■ PACKAGE OUTLINE

NJU6434KS4

NJU6434C

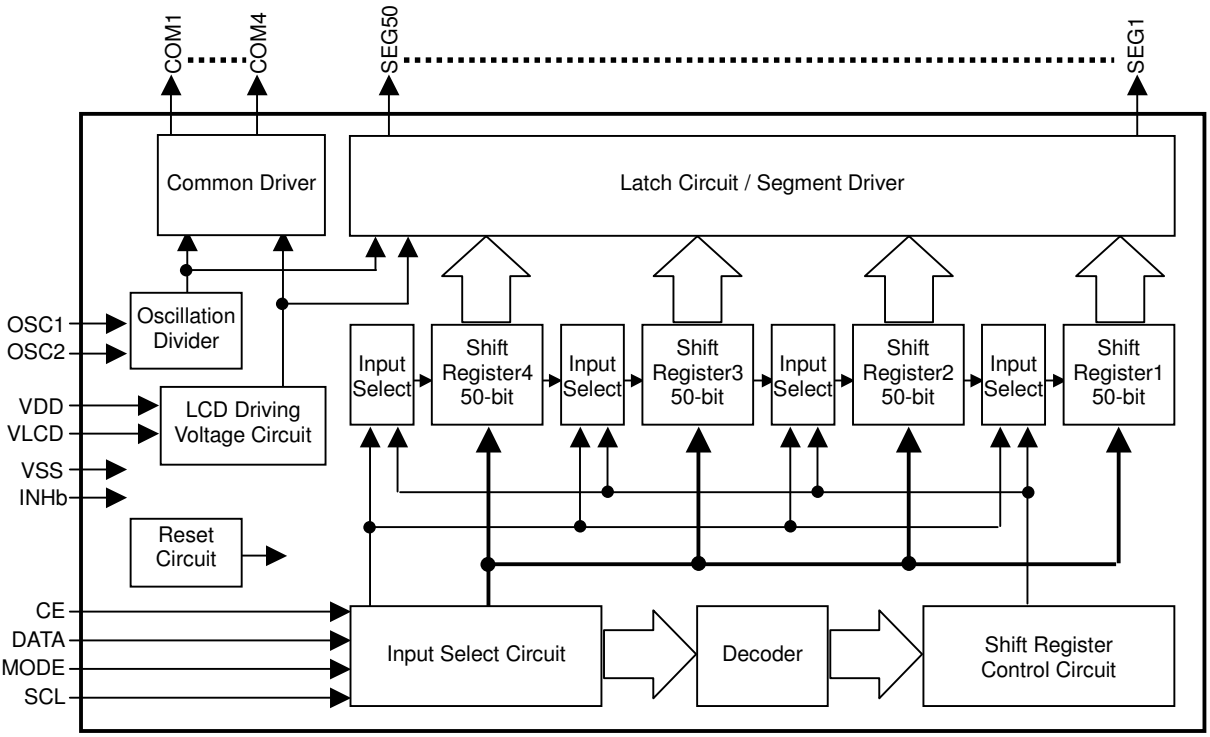


NJU6434FH2

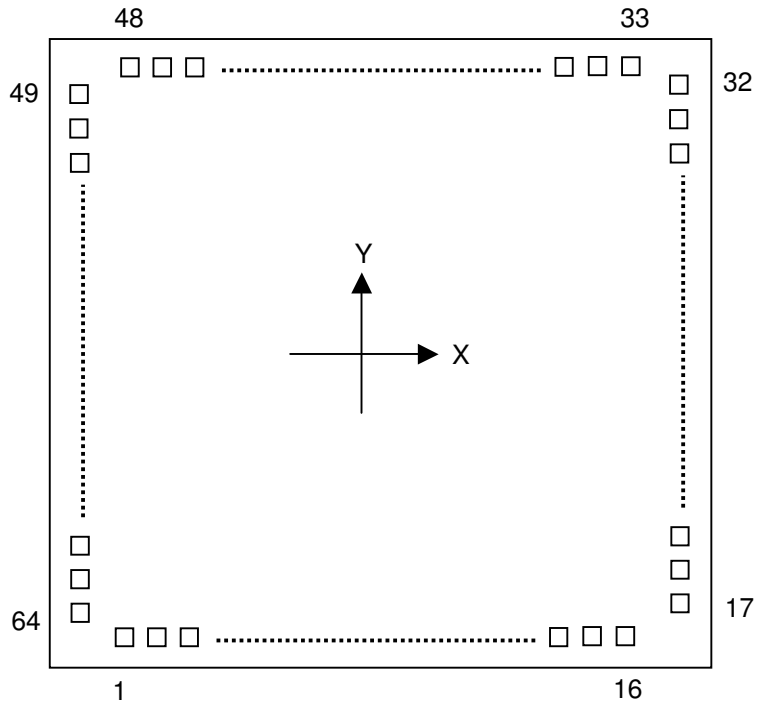
■ FEATURES

- 50 Segment Drivers
- Duty Ratio 1/4 (Up to 200-Segments)
- Serial Data Transmission (Shift Clock 2MHz max.)
- Oscillation Circuit On-chip (External Resistance Required, or External Clock Input)
- Display Off Function (INHb Terminal)
- Operating Voltage 2.4 to 5.5V
- LCD Driving Voltage 2.4 to 6.0V
- Package Outline Chip, QFN 64-S4, QFP64-H2
- C-MOS Technology P-Sub

■ BLOCK DIAGRAM



■ PAD LOCATION



Chip Center : X=0μm, Y=0μm
Chip Size : X=3.00 mm, Y=3.00 mm
Chip Thickness : 400 μm
PAD Size : X=70.0 μm, Y=70.0 μm
PAD Pitch : 99.0 μm (Min.)

■ PAD COORDINATES

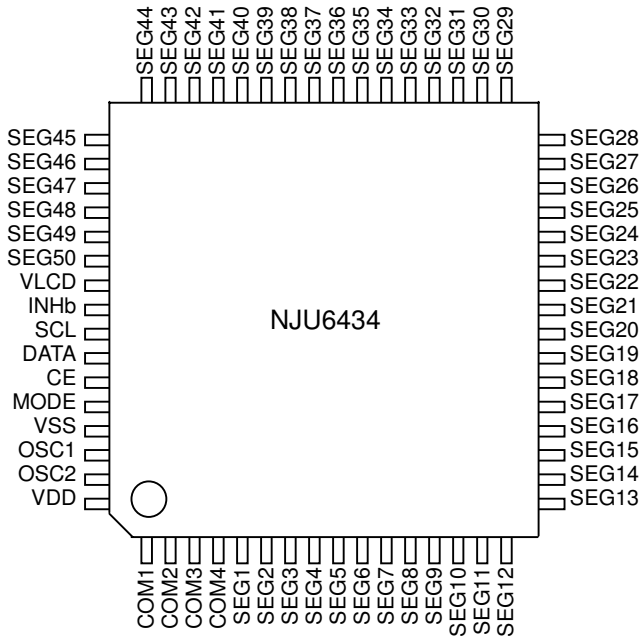
Chip Size 3.00 x 3.00 mm(Chip Center X=0μm, Y=0μm)

PAD No.	Terminal	X= μm	Y= μm
1	COM1	-994.5	-1366.3
2	COM2	-694.5	-1366.3
3	COM3	-549.5	-1366.3
4	COM4	-445.5	-1366.3
5	SEG1	-346.5	-1366.3
6	SEG2	-247.5	-1366.3
7	SEG3	-148.5	-1366.3
8	SEG4	-49.5	-1366.3
9	SEG5	49.5	-1366.3
10	SEG6	148.5	-1366.3
11	SEG7	247.5	-1366.3
12	SEG8	346.5	-1366.3
13	SEG9	445.5	-1366.3
14	SEG10	549.5	-1366.3
15	SEG11	694.5	-1366.3
16	SEG12	994.5	-1366.3
17	SEG13	1366.3	-994.5
18	SEG14	1366.3	-694.5
19	SEG15	1366.3	-549.5
20	SEG16	1366.3	-445.5
21	SEG17	1366.3	-346.5
22	SEG18	1366.3	-247.5
23	SEG19	1366.3	-148.5
24	SEG20	1366.3	-49.5

PAD No.	Terminal	X= μm	Y= μm
25	SEG21	1366.3	49.5
26	SEG22	1366.3	148.5
27	SEG23	1366.3	247.5
28	SEG24	1366.3	346.5
29	SEG25	1366.3	445.5
30	SEG26	1366.3	549.5
31	SEG27	1366.3	694.5
32	SEG28	1366.3	994.5
33	SEG29	994.5	1366.3
34	SEG30	694.5	1366.3
35	SEG31	549.5	1366.3
36	SEG32	445.5	1366.3
37	SEG33	346.5	1366.3
38	SEG34	247.5	1366.3
39	SEG35	148.5	1366.3
40	SEG36	49.5	1366.3
41	SEG37	-49.5	1366.3
42	SEG38	-148.5	1366.3
43	SEG39	-247.5	1366.3
44	SEG40	-346.5	1366.3
45	SEG41	-445.5	1366.3
46	SEG42	-549.5	1366.3
47	SEG43	-694.5	1366.3
48	SEG44	-994.5	1366.3

PAD No.	Terminal	X= μm	Y= μm
49	SEG45	-1366.3	994.5
50	SEG46	-1366.3	694.5
51	SEG47	-1366.3	549.5
52	SEG48	-1366.3	445.5
53	SEG49	-1366.3	346.5
54	SEG50	-1366.3	247.5
55	VLCD	-1366.3	148.5
56	INHb	-1366.3	49.5
57	SCL	-1366.3	-49.5
58	DATA	-1366.3	-148.5
59	CE	-1366.3	-247.5
60	MODE	-1366.3	-346.5
61	VSS	-1366.3	-445.5
62	OSC1	-1366.3	-549.5
63	OSC2	-1366.3	-694.5
64	VDD	-1366.3	-994.5

■ PIN CONFIGURATION



■ TERMINAL DESCRIPTION

No.	SYMBOL	FUNCTION
5~54	SEG1~SEG50	LCD Segment Output Terminals
1~4	COM1~COM4	LCD Common Output Terminals
62 63	OSC1 OSC2	Oscillation Terminals : External resistance is connected to these terminals. In External clock operation, the external clock input to OSC1 terminal. OSC2 terminal should be opened.
64	VDD	Power Supply (+5V)
61	VSS	Power Supply (0V)
55	VLCD	Power Supply for LCD Driving
59	CE	Chip Enable Signal Input Terminal : "H" : LCD display data and mode setting data input "L" : Disable Fall Edge : LCD display data latch
57	SCL	Serial Data Transmission Clock Input Terminal : LCD display and Mode setting data are input synchronized SCL clock signal rise edge.
58	DATA	Serial Data Input Terminal Data input timing : SCL clock rise edge
60	MODE	Data or Mode Select Terminal "H" : Data input mode "L" : LCD display data input mode (Refer the mode setting table for mode setting contents)
56	INHb	Display-Off Control Terminal : When display goes to off, the display data in the shift-register is retained. "H" : Display-On "L" : Display-Off

■ FUNCTIONAL DESCRIPTION

(1) Operation of each block

(1-1) Oscillation Circuit

The oscillation circuit operates by connecting external resistance (capacitance is incorporated). This circuit provides the clock signal to both common and segment drivers.

(1-2) Divider Circuit

This circuit divides the oscillating signal to generate the common and segment timing.

(1-3) Shift-Register

When the CE terminal is "H" (Enable mode), the display data is transferred to the shift-register synchronized by the shift clock on the SCL terminal.

(1-4) Latch Circuit and Segment Driver

When the CE signal falling, the display data is latched, and the data controls the segment signal of display-on/off.

(1-5) Common Driver

The Common driver generates driving waveform to common terminal.

(1-6) Reset Circuit

The Reset circuit is type of detectable voltage. It resets internal circuit when the power turns on.

(1-7) LCD Driving Voltage Generator Circuit

The LCD Driving voltage generator circuit generates the LCD bias voltage. (Refer to “(6) LCD Panel Drive” for details.)

(2) Mode Setting

The mode setting is composed of 4-bit, and selects the shift register that writes the display data by writing data in the mode setting register. (Refer to "(4) Data Input Timing" for details.)

When the data (1,1,1,1) is input, “0” (All Display-off) is written in all shift registers.

The mode setting register is selected by CE="H" and MODE="H". The data is latched at the rising edge of the SCL, and selected at falling edge of the CE.

Table 1. Mode Setting Table

Mode	Data	Description
1	(MSB) 1,0,0,0 (LSB)	Shift register 1 is selected.
2	0,1,0,0	Shift register 2 is selected.
3	1,1,0,0	Shift register 3 is selected.
4	0,0,1,0	Shift register 4 is selected.
5	1,0,1,0	All Shift register (1~4) is selected, and data is written continuously.
F	1,1,1,1	All shift register is “0”.

(3) Correspondence of the transfer data and output terminal

The display data is written by CE="H" and MODE="L". The data is latched at the rising edge of the SCL, and written at falling edge of the CE.

The correspondence of the data and the output terminals is as follows.

Output Terminal	COM1	COM2	COM3	COM4
SEG1	D1	D2	D3	D4
SEG2	D5	D6	D7	D8
SEG3	D9	D10	D11	D12
SEG4	D13	D14	D15	D16
SEG5	D17	D18	D19	D20
SEG6	D21	D22	D23	D24
SEG7	D25	D26	D27	D28
SEG8	D29	D30	D31	D32
SEG9	D33	D34	D35	D36
SEG10	D37	D38	D39	D40
SEG11	D41	D42	D43	D44
SEG12	D45	D46	D47	D48
SEG13	D49	D50	D51	D52
SEG14	D53	D54	D55	D56
SEG15	D57	D58	D59	D60
SEG16	D61	D62	D63	D64
SEG17	D65	D66	D67	D68
SEG18	D69	D70	D71	D72
SEG19	D73	D74	D75	D76
SEG20	D77	D78	D79	D80
SEG21	D81	D82	D83	D84
SEG22	D85	D86	D87	D88
SEG23	D89	D90	D91	D92
SEG24	D93	D94	D95	D96
SEG25	D97	D98	D99	D100

Output Terminal	COM1	COM2	COM3	COM4
SEG26	D101	D102	D103	D104
SEG27	D105	D106	D107	D108
SEG28	D109	D110	D111	D112
SEG29	D113	D114	D115	D116
SEG30	D117	D118	D119	D120
SEG31	D121	D122	D123	D124
SEG32	D125	D126	D127	D128
SEG33	D129	D130	D131	D132
SEG34	D133	D134	D135	D136
SEG35	D137	D138	D139	D140
SEG36	D141	D142	D143	D144
SEG37	D145	D146	D147	D148
SEG38	D149	D150	D151	D152
SEG39	D153	D154	D155	D156
SEG40	D157	D158	D159	D160
SEG41	D161	D162	D163	D164
SEG42	D165	D166	D167	D168
SEG43	D169	D170	D171	D172
SEG44	D173	D174	D175	D176
SEG45	D177	D178	D179	D180
SEG46	D181	D182	D183	D184
SEG47	D185	D186	D187	D188
SEG48	D189	D190	D191	D192
SEG49	D193	D194	D195	D196
SEG50	D197	D198	D199	D200

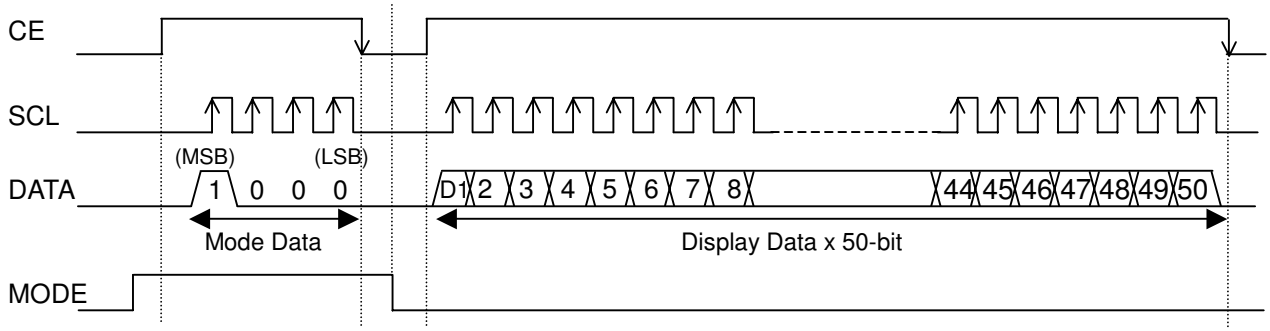
Correspondence of the transfer data and Segment Status

Transfer Data	Segment Status
”H”	ON
”L”	OFF

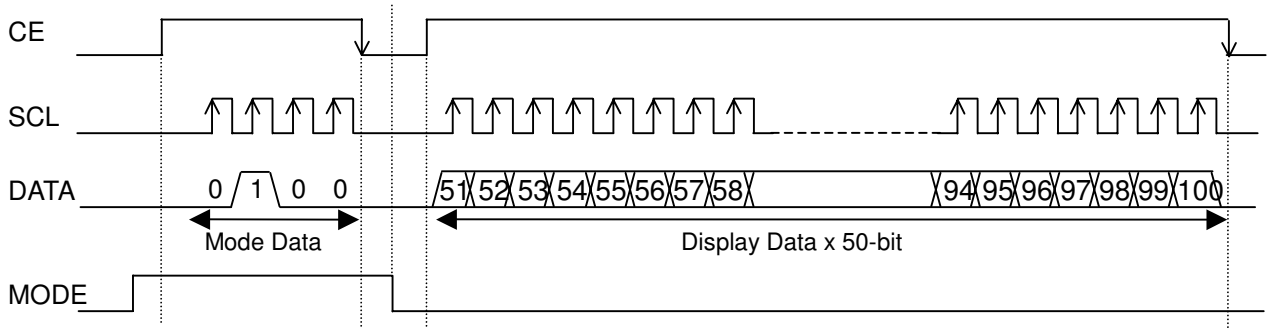
(4) Data Input Timing

The format of data is as follows. The mode data is input by 4-bit of MSB first, and after the shift register is selected, the display data is written

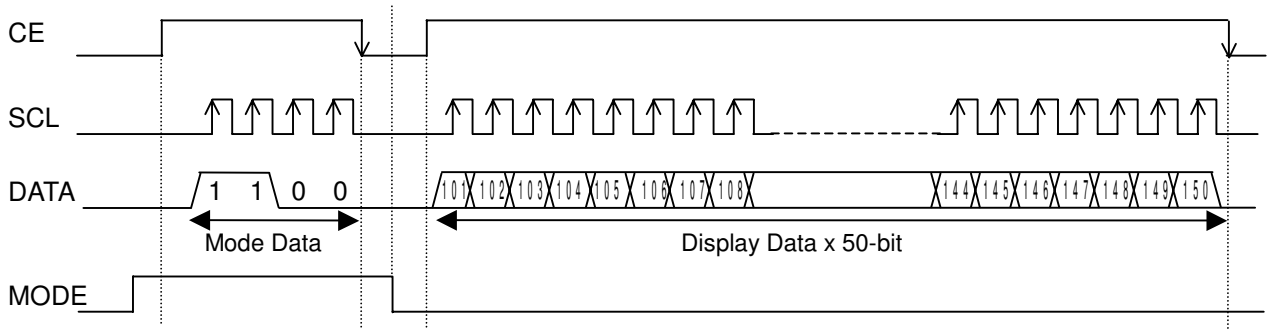
- Mode 1 : Shift Register 1 (D1~D50)



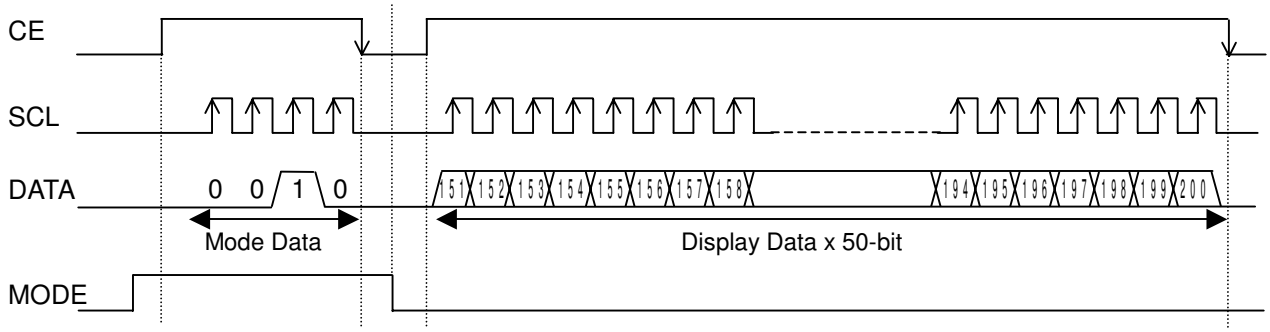
- Mode 2 : Shift Register 2 (D51~D100)



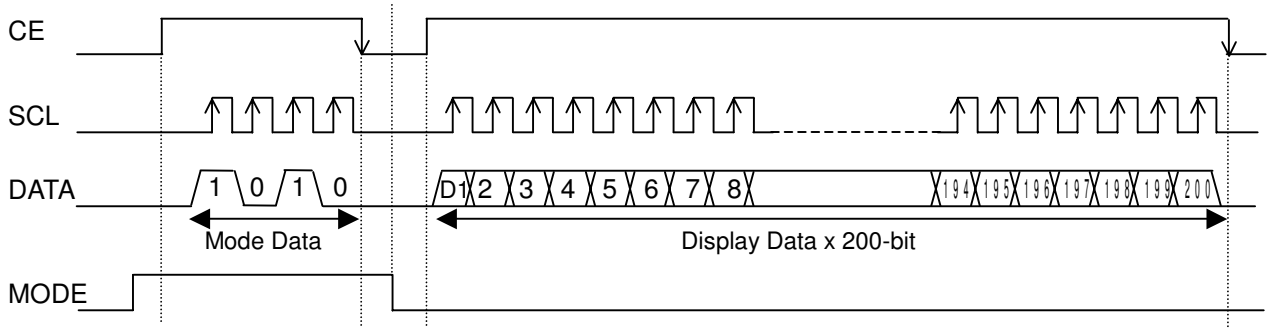
- Mode 3 : Shift Register 3 (D101~D150)



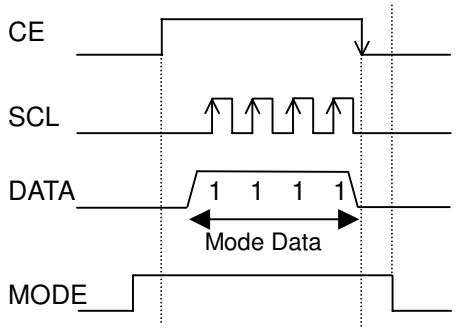
- Mode 4 : Shift Register 4 (D151~D200)



- Mode 5 : Shift Register 1~4 (D1~D200)



- Mode F : Shift Register 1~4 all "0"



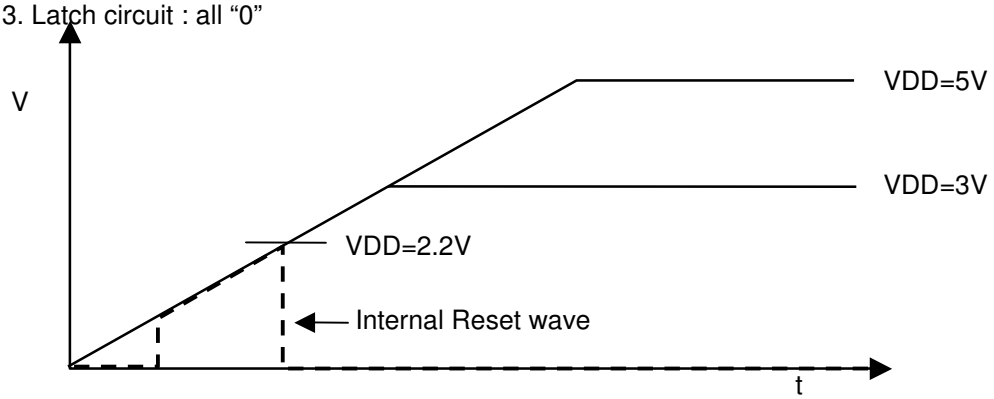
Note 1) All of display data should be transmitted within 30ms to keep the display quality, because huge display data D1 to D200 are transmitted at 4 times totally.
Note 2) Data is latched at the rising edge of the SCL.
Note 3) Mode data and display data are executed at the falling edge of the CE.
Note 4) In case of less than 4-bit data, the mode data remains the LSB side of the previous mode data.
Note 5) In case of over 4-bit data, the mode data is valid the previous 4-bit of the falling edge of the CE.
Note 6) In case of less than 50-bit data, the display data remains the last part of the previous display data.
Note 7) In case of over 50-bit data, the display data is valid the previous 50-bit of the falling edge of the CE.

(5) Initialization by Power On Reset

The **NJU6434** incorporates the reset circuit of the detectable voltage type, and when the power supply is turned on, it automatically initializes it (reset). When the VDD becomes 1V to 2.2V of the working voltage, the reset signal is generated internally. When the power supplies rise time should be over than 0.1ms. (Refer to "condition of the Power on reset" for details.)

(5-1) Status of Power On Reset

1. Mode setting release (nonselective status)
2. Shift register : all "0"
3. Latch circuit : all "0"

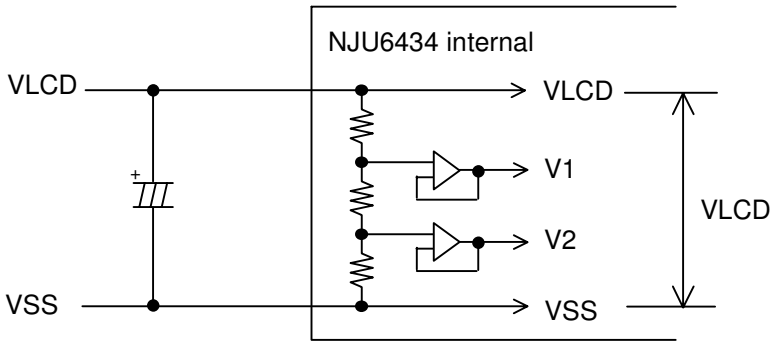


(6) LCD Panel Drive

(6-1) LCD driving volyage generation circuit

The LCD driving voltage generation circuit is consists of bleeder resistance and voltage follower.

This circuit generates LCD driving bias voltages V1 and V2 from input voltage terminal (VLCD-VSS). It is generated by the bleeder resistance in IC, and after impedance is converted by the voltage follower, it is supplied to the LCD driving circuit. The VLCD terminal requires external capacitors for bias voltage stabilization for display quality as shown in below.



■ ABSOLUTE MAXIMUM RATINGS

Ta=25°C

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Operating Voltage (1)	VDDmax	VDD Terminal, Ta=25°C	-0.3~+7.0	V
Operating Voltage (2)	VLCDmax	VLCD Terminal, Ta=25°C	-0.3~+7.0	V
Input Voltage (1)	VI	CE, SCL, DATA, MODE, INHb Terminals, Ta=25°C	-0.3~+7.0	V
Input Voltage (2)	VI	OSC1, OSC2 Terminals	-0.3~VDD+0.3	V
Output Voltage	VO	OSC1, OSC2 Terminals	-0.3~VDD+0.3	V
Power Dissipation	Pdmax	Glass epoxy board (4-layer) 76.2mm x 114.3mm x 1.6mm	1600(QFN64-S4) 1900(QFP64-H2)	mW
Operating Temperature	Topr	-	-40~+85	°C
Storage Temperature	Tstg	-	-55~+125	°C

Note 1) All voltage values are specified as VSS = 0V.

Note 2) If the LSI is used on condition above the absolute maximum ratings, the LSI may be destroyed. Using the LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electric characteristics conditions will cause malfunction and poor reliability.

Note 3) Turn on V_{DD} first then turn on V_{LCD} must be required.

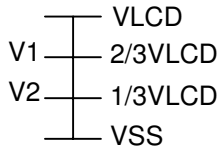
Note 4) Decoupling capacitor should be connected between V_{DD} and V_{SS} , V_{LCD} and V_{SS} due to the stabilized operation for the LSI.

■ ELECTRICAL CHARACTERISTICS

• DC Characteristics (VDD=2.4~3.6V, VLCD=VDD, Ta=-40~+85°C)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT	NOTE
Operating Voltage (1)	VDD	VDD Terminal		2.4	3.0	3.6	V	
Operating Voltage (2)	VLCD	VLCD Terminal		2.4		6	V	
"H" Input Voltage	VIH	CE, SCL, DATA, MODE, INHb		0.8VDD		VDD	V	
"L" Input Voltage	VIL			VSS		0.2VDD	V	
"H" Input Current	IIH	CE,SCL, DATA,MODE, INHb	VI=VDD			1	uA	
"L" Input Current	IIL		VI=VSS			1	uA	
"H" Output Voltage (1)	VOH(1)	SEG1~SEG50 VLCD=3V	Io=-10uA	VLCD-0.4		VLCD	V	
"L" Output Voltage (1)	VOL(1)		Io=+10uA	VSS		0.4	V	
Middle Level Voltage $^2/_3$ (1)	VMS$^2/_3$	SEG1~SEG50 Ta=25°C, VLCD=3V	Io=±10uA	V1-0.4	V1	V1+0.4	V	1
Middle Level Voltage $^1/_3$ (1)	VMS$^1/_3$		Io=±10uA	V2-0.4	V2	V2+0.4	V	
"H" Output Voltage (2)	VOH(2)	COM1~COM4 VLCD=3V	Io=-50uA	VLCD-0.5		VLCD	V	
"L" Output Voltage (2)	VOL(2)		Io=+50uA	VSS		0.5	V	
Middle Level Voltage $^2/_3$ (2)	VMC$^2/_3$	COM1~COM4 Ta=25°C, VLCD=3V	Io=±50uA	V1-0.5	V1	V1+0.5	V	1
Middle Level Voltage $^1/_3$ (2)	VMC$^1/_3$		Io=±50uA	V2-0.5	V2	V2+0.5	V	
Oscillating Frequency Range	fosc	OSC1, OSC2 Terminals Ta=25°C		10		20	kHz	
Oscillating Frequency	fosc	OSC1, OSC2, R=750kΩ Ta=25°C		12.6	15.4	18.2	kHz	
Operating Current (1)	IDD	VDD Terminal, Ta=25°C			15	30	uA	
Operating Current (2)	ILCD	VLCD Terminal, Ta=25°C			10	20	uA	
Hysteresis Voltage	VH	CE, SCL, DATA, MODE, INHb		0.3			V	

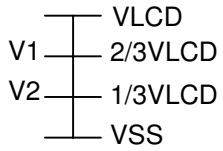
Note 1) V1=2/3VLCD, V2=1/3VLCD



- DC Characteristics (VDD=4.5~5.5V, VLCD=VDD, Ta=-40~+85°C)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT	NOTE
Operating Voltage (1)	VDD	VDD Terminal		4.5	5.0	5.5	V	
Operating Voltage (2)	VLCD	VLCD Terminal		2.4		6	V	
"H" Input Voltage	VIH	CE, SCL, DATA, MODE, INHb		0.8VDD		VDD	V	
"L" Input Voltage	VIL			VSS		0.2VDD	V	
"H" Input Current	IIH	CE,SCL, DATA,MODE, INHb	VI=VDD			1	uA	
"L" Input Current	IIL		VI=VSS			1	uA	
"H" Output Voltage (1)	VOH(1)	SEG1~SEG50 VLCD=5V	Io=-10uA	VLCD-0.4		VLCD	V	
"L" Output Voltage (1)	VOL(1)		Io=+10uA	VSS		0.4	V	
Middle Level Voltage $^2/_3$ (1)	VMS$^2/_3$	SEG1~SEG50 Ta=25°C, VLCD=5V	Io=±10uA	V1-0.4	V1	V1+0.4	V	1
Middle Level Voltage $^1/_3$ (1)	VMS$^1/_3$		Io=±10uA	V2-0.4	V2	V2+0.4	V	
"H" Output Voltage (2)	VOH(2)	COM1~COM4 VLCD=5V	Io=-100uA	VLCD-0.5		VLCD	V	
"L" Output Voltage (2)	VOL(2)		Io=+100uA	VSS		0.5	V	
Middle Level Voltage $^2/_3$ (2)	VMC$^2/_3$	COM1~COM4 Ta=25°C, VLCD=5V	Io=±100uA	V1-0.5.	V1	V1+0.5	V	1
Middle Level Voltage $^1/_3$ (2)	VMC$^1/_3$		Io=±100uA	V2-0.5	V2	V2+0.5	V	
Oscillating Frequency Range	fosc	OSC1, OSC2 Terminals Ta=25°C		10		20	kHz	
Oscillating Frequency	fosc	OSC1, OSC2, R=750kΩ Ta=25°C		12.6	15.4	18.2	kHz	
Operating Current (1)	IDD	VDD Terminal, Ta=25°C			25	50	uA	
Operating Current (2)	ILCD	VLCD Terminal, Ta=25°C			15	30	uA	
Hysteresis Voltage	VH	CE, SCL, DATA, MODE, INHb		0.3			V	

Note 1) V1=2/3VLCD, V2=1/3VLCD

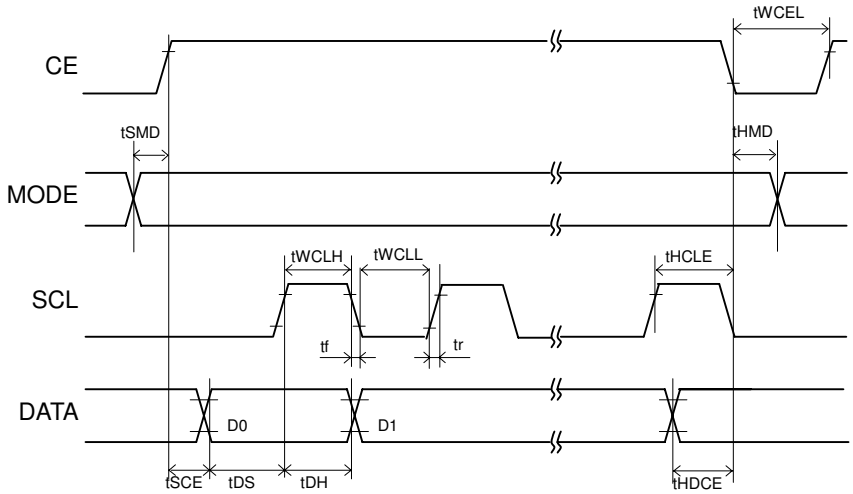


- AC Characteristics

(VDD=2.4~5.5V, Ta=-40~+85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
"L" Clock Pulse Width	tWCLL	SCL Terminal	0.25			us
"H" Clock Pulse Width	tWCLH	SCL Terminal	0.25			us
DATA Set-up Time	tDS	SCL, DATA Terminal	0.25			us
DATA Hold Time	tDH	SCL, DATA Terminal	0.25			us
CE Set-up Time	tSCE	CE, DATA Terminal	1.0			us
CE Hold Time (1)	tHDCE	CE, DATA Terminal	1.0			us
CE Hold Time (2)	tHCLE	CE, SCL Terminal	1.25			us
MODE Set-up Time	tSMD	MODE, CE Terminal	0.25			us
MODE Hold Time	tHMD	MODE, CE Terminal	0.25			us
"L" Chip Enable Pulse Width	tWCEL	CE Terminal	4.0			us

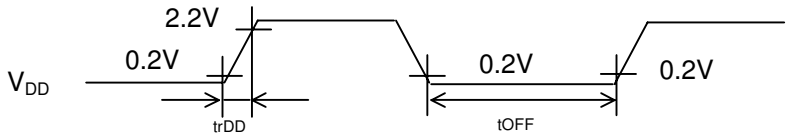
- Input Timing Characteristics



- Power on reset condition

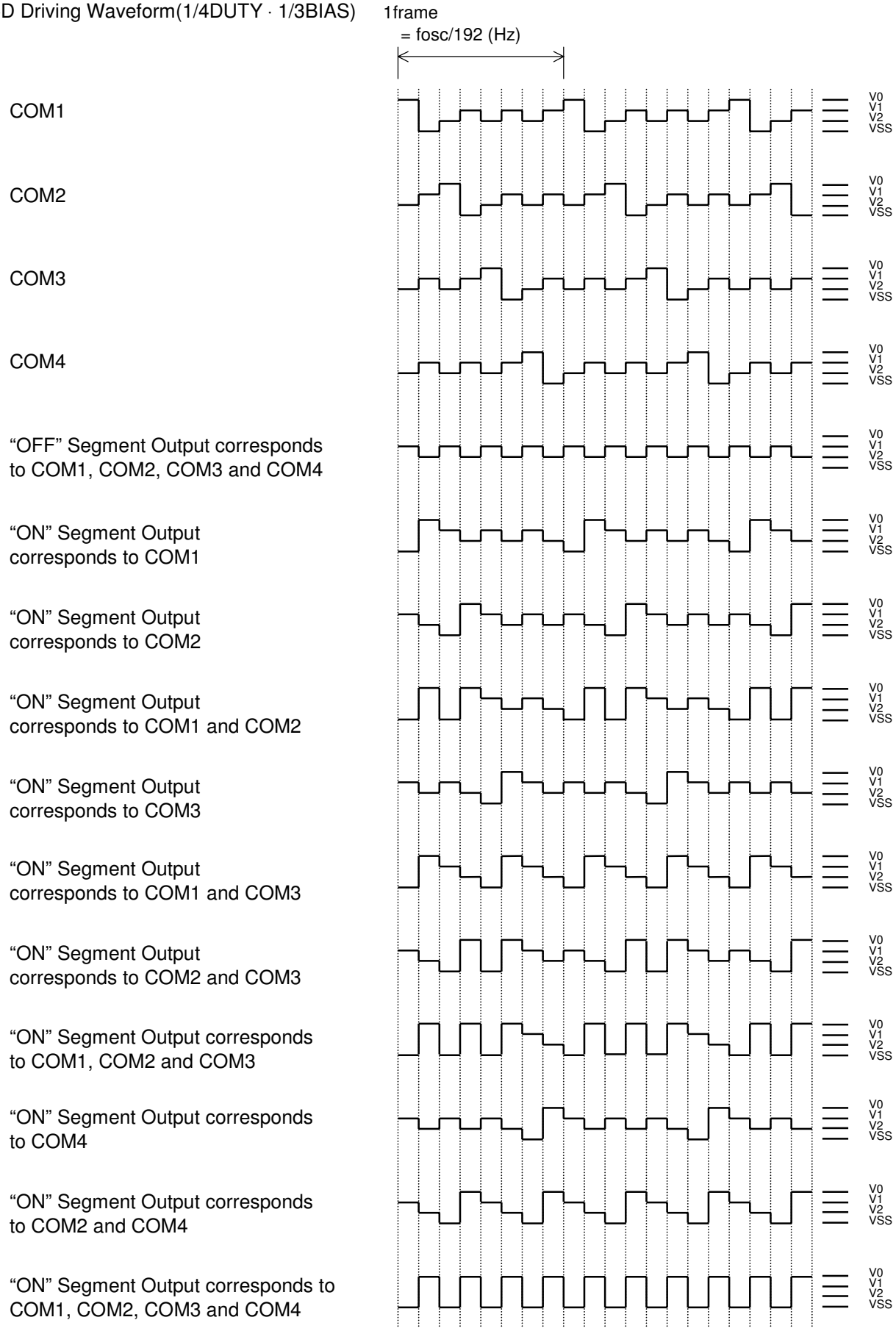
(VDD=2.4~5.5V, Ta=-40~+85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Power supply rise time	trDD	VDD Terminal	0.1			us
Power supply off time	tOFF	VDD Terminal	1			us

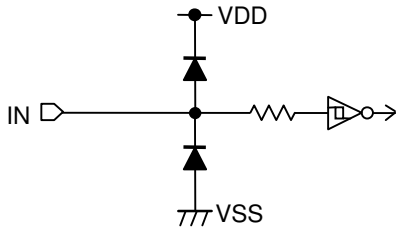


tOFF is the off time when power-supply turns off suddenly or cycle on/off.

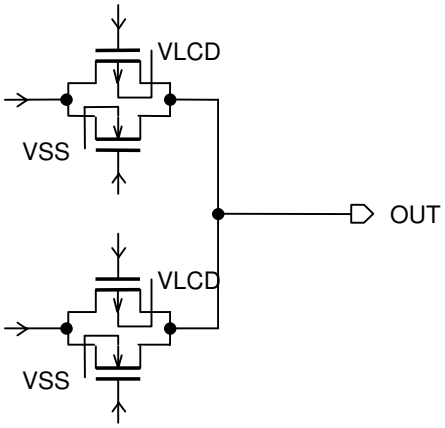
- LCD Driving Waveform(1/4DUTY · 1/3BIAS)



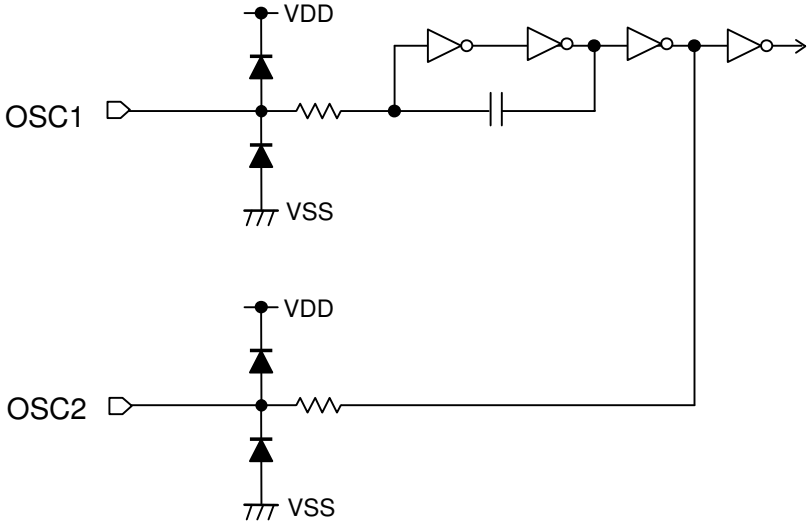
■ INPUT and OUTPUT TERMINAL STRUCTURE



CE, SCL, DATA, MODE, INHb



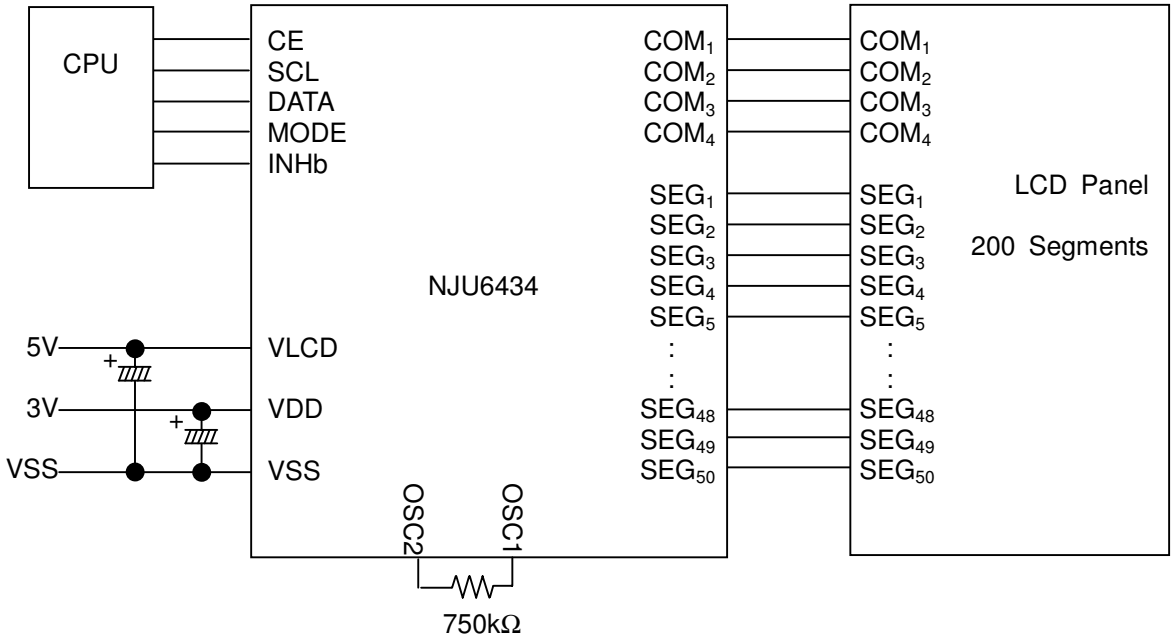
SEG1~SEG50, COM1~COM4



OSC1, OSC2

■ APPLICATION CIRCUIT

Example) VDD=3V, VLCD=5V



[CAUTION]
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